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Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics

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Compound semiconductors are the basis for many of the highest performance optical and electronic devices in use today. Their widespread commercial application has, however, been limited due to the high cost of substrates. Device costs can be significantly reduced if the substrate is reused in a simple, totally non-destructive and rapid process. Here, a method that allows the indefinite reuse and recycling of wafers is demonstrated, employing a combination of epitaxial "protection layers", plasma cleaning techniques that return the wafers to their original, pristine, and epi-ready condition following epitaxial layer removal, and adhesive-free bonding to a secondary plastic substrate. The generality of this process is demonstrated by fabricating high performance GaAs-based photovoltaic cells, light emitting diodes, and metal-semiconductor field effect transistors that are transferred without loss of performance onto flexible and lightweight plastic substrates, and then the parent wafer is recycled for subsequent growth of additional device layers. This process potentially leads to a transformational change in device cost, arising from the inevitable consumption of the wafer that accompanies conventional epitaxial liftoff followed by chemo-mechanical polishing.

1. Introduction

Compared to elemental semiconductors such as Si or Ge, compound semiconductors often have superior material properties useful in high performance optoelectronic devices, including high carrier mobilities, direct and indirect band-gap tuning, ability to form heterojunctions that confine optical fields and charge, and so forth.[1,2] However, wafers on which compound semiconductor active device regions are epitaxially grown are costly (e.g., GaAs costs ≈$20k m^{-2}), limiting their viability for use in the production of large area devices such as displays and solar cells. Epitaxial lift-off (ELO) was introduced to reduce costs of GaAs/AlGaAs devices by enabling the separation of single crystal active epitaxial layers from fragile and bulky substrates using hydrofluoric acid to selectively remove an AlAs sacrificial layer grown between the substrate and the device layers.[3] The ELO process is also advantageous in that it yields a flexible and lightweight thin film. Unfortunately, the promise of wafer reuse has not been fully realized, since the removal of the sacrificial layer results in residual surface damage, and leaves debris on the parent wafer surface. The most common method for preparing that surface for subsequent growth, therefore, has been by post lift-off chemo-mechanical polishing that reduces wafer thickness and ultimately inflicts additional damage, limiting reuse to only a very few growth and cleaning cycles.[4,5]

Recently, ELO using hydrochloric acid as a selective etchant for an AlInP sacrificial layer was introduced for wafer reuse without repolishing.[6] In that case, a pre-processing step, such as passivation or protection of In-containing layers due their high etching rate in HCl is required. This complication is required to allow compatibility with many devices such as high-efficiency multijuction solar cells with InGa(Al)P wide bandgap absorbers, and InGa(Al)P-based light emitting diodes (LEDs). Furthermore, many high efficiency GaAs solar cells employed InGa(Al)P based window and back-surface field layers instead of AlGaAs.[7] To ameliorate this issue, we choose to use the HF chemistry-based ELO process, and employ surface protecting layers that can be removed using chemically selective etchants.[8,9] These protection layers comprise alternating lattice-matched arsenide-based and phosphide-based materials that enable recovery of the "epi-ready" wafer surface for regrowth on the original wafer without any observable degradation in surface quality or device performance.

Here, we develop a completely non-destructive wafer reuse cycle to create multiple lightweight and flexible thin film optoelectronic devices including photovoltaic cells, LEDs and transistors from a parent wafer, without material composition limitations or the need for damage-inducing wafer polishing commonly used in ELO processes. Previously reported protection layer schemes are significantly improved by removing one

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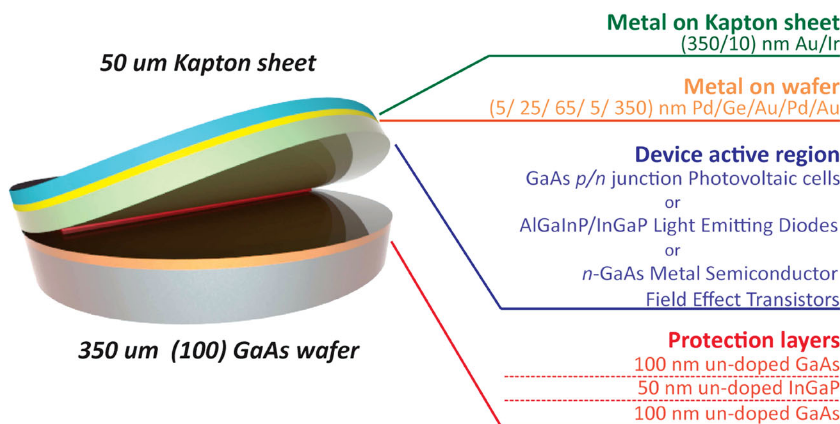

Figure 1. Schematic illustration of the generalized wafer structure used in non-destructive epitaxial lift-off (ND-ELO). The active thin film device region is lifted-off by selectively etching the AlAs sacrificial layer using dilute hydrofluoric acid. Details of the epitaxial layers, including the alternating GaAs-InGaP protection layers and the AlAs sacrificial layer are shown along with the metal layer used in cold-welding to the plastic substrate. The active region structure is varied according to the application requirements, e.g., a photovoltaic cell, light emitting diode, or metal semiconductor field effect transistor.

of those layers, and two-step surface cleaning and thermally assisted cold-weld bonding techniques are newly introduced to simplify the fabrication process.[9] The simplified scheme of non-destructive epitaxial lift off (ND-ELO) eliminates an interface between materials with different group-V species, whose addition requires temperature changes during growth that increases both the growth time and amount of material used. Specifically, we focus on characterizing the performance of various optoelectronic devices, and comparing their parameters to validate the method.

2. Results and Discussion

The ELO process and a generalized epitaxial structure used in non-destructive wafer recycling are illustrated in **Figure 1**. The epitaxial structure consists of the sequential growth of protection, sacrificial and active device layers. The InGaP (50 nm) and GaAs (100 nm) protection and buffer layers are grown by gas source molecular beam epitaxy (GSMBE) on a 2 inch diameter (100) GaAs parent wafer, although this process is fully compatible with growth by other common techniques. An AlAs sacrificial release layer is then grown onto the protection layer stack. Next, the active device region is grown in inverted order such that after bonding to the secondary plastic substrate, devices can be fabricated in their conventional orientation, thereby eliminating a second transfer step often employed in ELO device processing. For photovoltaic cells, a rear surface mirror allows for a thinner absorber layer than bulky substrate-based solar cells, saving growth time and reducing the use of costly materials while allowing increased efficiency via "photon recycling".[10] For LEDs, the rear surface mirror improves external quantum efficiency by allowing photons to be reflected back to the emitting surface instead of being absorbed in the wafer bulk.[11]

In conventional ELO, lifted-off layers are typically attached to flexible secondary handles using adhesives such as thermal releasing tape, wax, or glue.[3–6] These adhesives can be bulky, heavy, brittle and subject to degradation while also requiring an additional transfer following the separation of the epitaxy onto an intermediate "handle".[3–5] To eliminate all use of adhesives and the necessity of an intermediate handle transfer, we attach the epitaxial surface directly to the final flexible substrate following layer growth using a thermally-assisted cold-weld bond by applying pressure across the two surfaces to be bonded. To make the bond, the surfaces are pre-coated with layers of a similar noble metal. To prepare for cold-weld bonding; a 10 nm thick Ir adhesion layer is sputtered on a Kapton sheet. The Ir layer provides tensile strain to the substrate, which is confirmed by observing curvature of the flexible secondary substrate following Ir deposition. The tensile-strained Ir layer significantly reduces the wafer and substrate separation time (≈5 h) by more than 90% compared with the ELO process without the Ir layer (≈36 to 48 h). This process acceleration was confirmed by comparison with a sample with the same structure and ND-ELO process conditions but without the addition of the Ir film. The tensile stress from the film assists in creating a gap between the epitaxial layers and the substrate at the sacrificial layer etch interface allowing the rapid ingress of etchant, analogous to that observed for compressively stressed layers. Next, Pd (5 nm)/Ge (25 nm)/Au (65 nm)/Pd (5 nm) layers are deposited onto the substrate using e-beam evaporation to form an Ohmic contact with the 5×10^{18} cm^{-3} Si-doped n-type GaAs layer.[12] Next, a 350 nm thick Au layer is deposited on both sample surfaces to complete the cold-welding bonding surfaces. Cold-weld bonding is performed under vacuum (≈10^{-5} Torr) with an applied force of 4 MPa at a stage temperature of 175 °C. The process allows a ≈92% reduction in bonding pressure compared to conventional room temperature cold-welding under ambient conditions.[13] We note that Au conveniently acts as a back contact and mirror while being undamaged by exposure to HF used in the ELO process. Further, it is insensitive to oxidation that can increase the pressure needed to effect the cold-weld bond.

Once the GaAs substrate is bonded to the plastic substrate, the active device region is lifted off from the parent wafer by immersion in HF for approximately 5 h. Here, the sample is fully submerged and relaxed in dilute HF and assisted solely by tensile stress introduced by the Ir. Therefore, the etching process is initiated from all directions similar to prior ELO process demonstrations.[3,14,15] The induced curvature by tensile stress is kept below the fracture point of the GaAs thin film, and the sacrificial layer is etched faster from the two curved sides and more slowly from the other sides which eliminates damage to the film caused by stress concentrated within the small area. Then the separated epitaxial films are fabricated into photovoltaic cells, LEDs and MESFETs. The device performance variations are negligible with respect to its position on the film. Although ELO is an effective means to separate the substrate and active region to create a thin film device, it also results in

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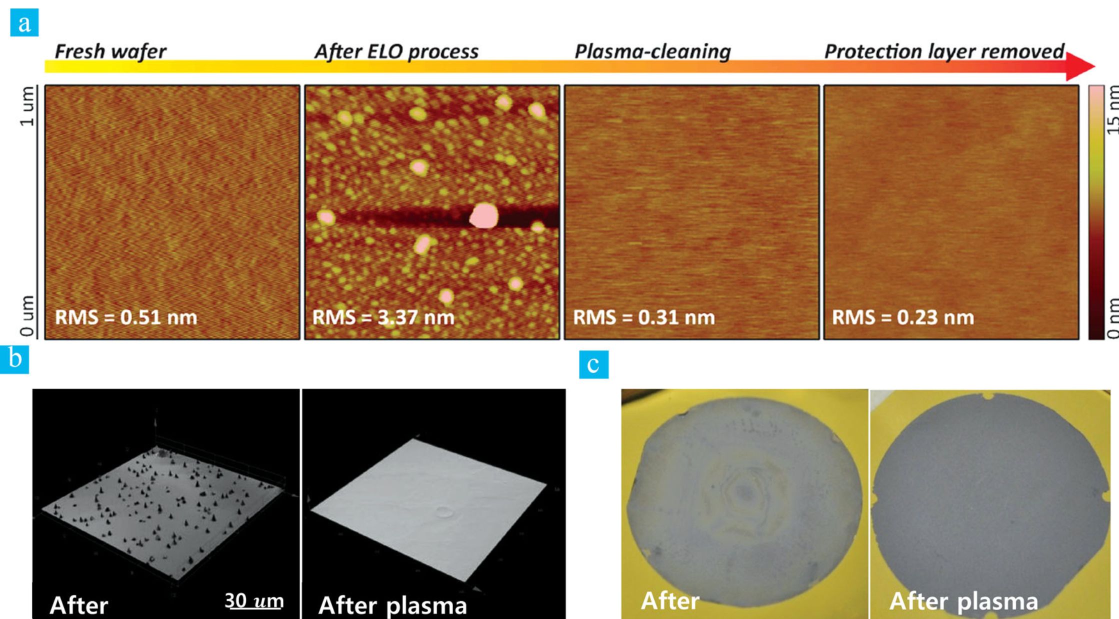

Figure 2. Comparison of wafer surface morphology before and after ELO. a) Atomic force microscope (AFM) images of the GaAs parent wafer substrate surface showing the root-mean-square (RMS) surface roughness (indicated by color bar) after each step. The growth starts with sub-nanometer surface roughness. However, immediately following ELO by etching the sacrificial layer, the roughness increases by an order of magnitude. Plasma cleaning reduces surface roughness by removing particulates while minor physical damage is incurred by the underlying GaAs protection layer. Wet chemical cleaning is used to remove the remaining InGaP protection layer, recovering the same surface morphology as the original wafer. b) Three dimensional laser microscope image of the surface immediately following ELO (left), and after plasma cleaning (right). c) The thin film surface following ELO (left), and after plasma cleaning (right).

roughening of the parent wafer surface, as well as the accumulation of contaminants, notably As_2O_3.[9,16] There is no evidence for etching of the GaAs layer adjacent to the sacrificial layer. Surface roughening is shown in the atomic force microscope (AFM) image of **Figure 2**a. This morphological degradation significantly and negatively impacts device performance in subsequently regrown layers; for example, it results in a 20–40% performance loss in solar cell power conversion efficiency (PCE).[4]

To recover the original surface quality, we have developed a completely non-destructive two-step cleaning procedure. The surface is pre-cleaned by an inductively coupled plasma using 50 SCCM of C_4F_8, a chemical etch gas to remove the oxides, mixed with 50 SCCM of Ar+ for 10s under 10 mTorr of base pressure at a substrate RF bias power of 110 W and a transformer coupled plasma RF power of 500 W. Figure 2b provides 3 dimensional laser microscopy images of the wafer surface before and after plasma cleaning, respectively. The image indicates that most of the contamination is apparently removed during the cleaning process, leaving a roughened surface. This cleaning procedure can be applied to the lifted-off film as well as the substrate, which are similarly contaminated following the ND-ELO process (Figure 2c). While they eliminate the ELO process residuals, they also physically and chemically damage the protection layer surface. Hence, InGaP and GaAs protection layers are grown on both the epi-side and the substrate-side (each in reverse order to the other starting with GaAs on the substrate) to address this problem. The roughened top GaAs protection layer is then removed using a phosphoric acid-based etchant (H_3PO_4:H_2O_2:H_2O (3:1:25)) until the etching stops at the InGaP layer. Next, the InGaP layer is removed through etching in diluted HCl acid (HCl:H_2O (1:1)), which provides complete etching selectivity with the GaAs buffer layer. The dilute HCl etch is well-known for preparing epi-ready surfaces through the removal of native oxides, allowing this last step of surface cleaning to provide a high quality regrowth interface.[6,17,18] The root mean square (RMS) surface roughness after each step is shown in Figure 2a, confirming the recovery of the original surface morphology after cleaning.

To demonstrate the effectiveness of wafer recycling using the above methods, the cleaned parent wafer was re-loaded into the GSMBE chamber for subsequent growth, and the same procedure was repeated multiple times with solar cells, LEDs and MESFETs fabricated after each growth/ND-ELO/cleaning cycle to ensure that no degradation of the original wafer was carried into the next cycle. For example, three identical GaAs p–n junction thin film photovoltaic cells on plastic substrates were fabricated from a single parent wafer and processed using conventional methods, into single junction solar cells (**Figure 3**a–c). The current density-voltage (*J*–*V*) characteristics of the cells measured under simulated AM 1.5G illumination at 1 sun (100 mW cm^{-2}) after the first, second, and third ND-ELO cycles are compared in Figure 3d. The external quantum efficiencies (*EQE*) are compared in **Figure 4**e. The *J*–*V* characteristics, short circuit current density (J_{SC}), open circuit voltage (V_{OC}), fill factor (FF) and PCE are nearly identical (with a standard deviation of 1.5% in *PCE*) for all devices without any apparent systematic degradation after a given cycle (see **Table 1**). Integration of the EQE spectra assuming an incident AM 1.5G solar spectrum gives J_{SC} = 23.2 ± 0.1 mA cm^{-2}, 23.0 ± 0.1 mA cm^{-2}, and 23.2 ± 0.1 mA cm^{-2} for the first, second, and third ND-ELO

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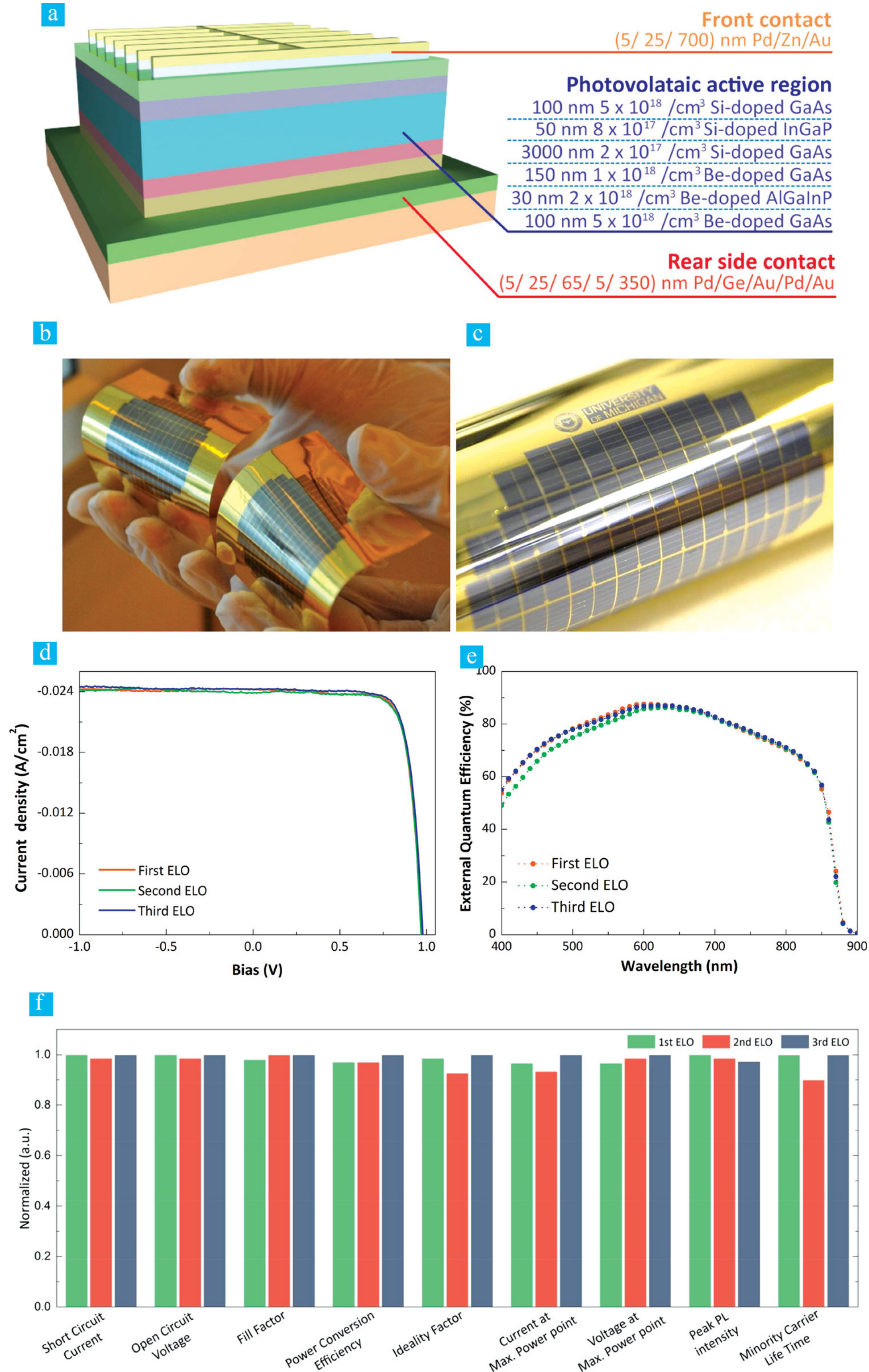

Figure 3. Thin-film GaAs single junction photovoltaic cells. a) Device structure of the thin film GaAs p–n junction photovoltaic cells. b) Fabricated GaAs thin film photovoltaic cells bonded by thermally assisted cold-welding to a plastic substrate following ND-ELO of 2 inch-diameter wafers. Both cell arrays are made from the same GaAs wafer using ND-ELO, wafer bonding, and parent wafer recycling. c) Close-up image of the GaAs thin film photovoltaic cell array. d) Current density versus voltage (*J*–*V*) characteristics measured under 1 sun, AM1.5G simulated solar illumination, and e) external quantum efficiency (EQE) measured from wavelengths between 400 nm and 900 nm after the first, second and third ND-ELO-processed photovoltaic cells originating from a single parent wafer. f) Comparison of photovoltaic cell performance, showing statistically identical device performance without systematic degradation from growth to growth.

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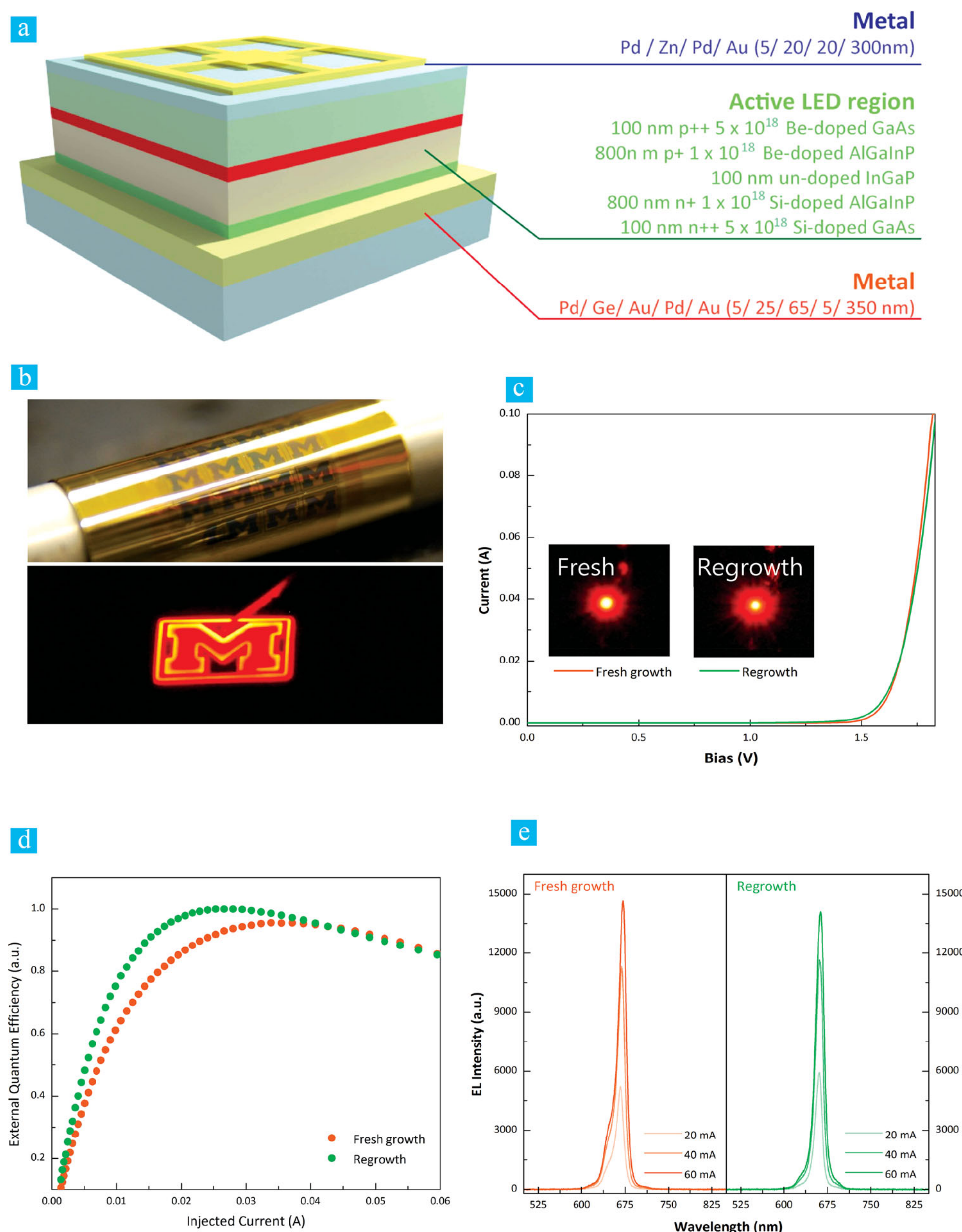

Figure 4. Thin-film AlGaInP/InGaP double heterostucture LEDs. a) Device structure of the thin film AlGaInP/InGaP LEDs. b) Images of patterned LEDs in the shape of the University of Michigan logo bonded by thermally assisted cold-welding to a Kapton substrate (above), and the same device under operation (below). The images were taken for the plastic wrapped around a 1.2 cm radius cylinder. c) Current density versus voltage (J–V) characteristics, d) external quantum efficiency (EQE) versus injected current, and e) electroluminescence (EL) spectrum intensity comparisons for LEDs after the first and second ND-ELO removal from the same parent wafer. Similar peak EL intensities and full width half maxima (FWHM) indicate identical device performance without systematic degradation from the wafer recycling process.

cycle, respectively. The discrepancy between the integrated J_{SC} and that extracted from the J–V characteristics is primarily due to absorption at wavelengths $\lambda < 400$ nm, which is not accounted for in the integration. Finally, we note that PCE = $18.1 \pm 0.1\%$, $18.0 \pm 0.3\%$, and $18.5 \pm 0.1\%$ were achieved for the three-cycle ND-ELO sequence. Furthermore, the current density-voltage (J–V) characteristics under the dark condition and transient photoluminescence intensities are measured to support the non-degraded device performance. Nomalized device performance parameters of the first, second and third cells are compared in Figure 4f. The non-systematic, small deviations confirm the feasibility of wafer reuse via ND-ELO and surface-protection layers.

Multiple cylces of AlGaInP/InGaP double heterojuction LEDs (Figure 4a) were also grown and fabricated to test the generality of our process approach. Figure 4b shows images of the thin film LEDs with and without current injection (bent over a 1.2 cm radius without incurring damage or performance degradation), confirming device flexibility as in the case of the solar cells in Figure 3. The J–V and EQE characteristics of the

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Table 1. Comparison of solar cell performances under AM1.5G simulated solar spectrum.

	J_{SC} [mA cm^{-2}]	V_{OC} [V]	FF [%]	PCE [%]	J_{max} [mA cm^{-2}]	V_{max} [V]	n
First ELO	24.2 ± 0.1	0.98	76.4 ± 0.6	18.1 ± 0.1	22.4 ± 0.2	0.81	1.95
Second ELO	23.9 ± 0.1	0.97	77.9 ± 1.3	18.0 ± 0.3	21.7 ± 0.3	0.83	1.83
Third ELO	24.2 ± 0.1	0.98	77.7 ± 0.1	18.5 ± 0.1	23.2 ± 0.2	0.84	1.98

first and second ELO-processed thin-film LEDs are compared in Figure 4c,d, respectively. Turn-on voltage (1.66 ± 0.01 V and 1.67 ± 0.01 V, respectively) and peak EQE (4% variation) are extracted from the data for the first and second ND-ELO cycles. Electroluminesence (EL) spectra for these same devices is provided in Figure 4e. The nearly identical performances of the first and second ND-ELO processed thin film LEDs is confirmed by the measured full width half maxima of 16.5 nm and 16.6 nm, and peak EL intensities (3% variation) at an injection current of 60 mA.

Finally, two iterations of *n*-GaAs MESFETs are fabricated from a single parent wafer and transferred to plastic, as shown in **Figure 5**a. The inverted MESFET structure is grown with the active channel layer closer to the growth interface compared with the substrate-based device, therefore the device performance is very sensitive to the growth interface quality. Figure 5b

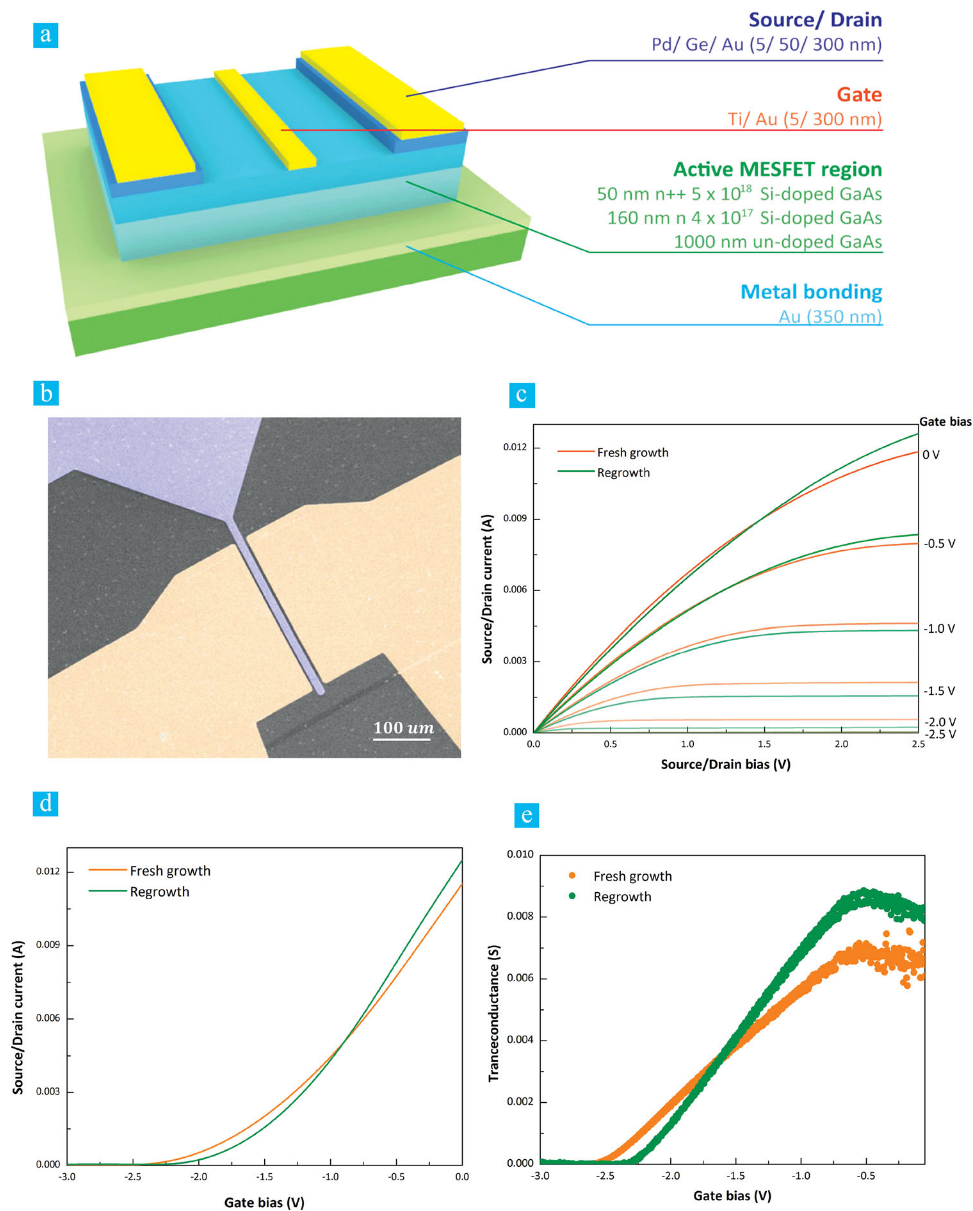

Figure 5. Thin-film *n*-GaAs MESFETs. a) Device structure of thin film *n*-GaAs MESFETs. b) Microscope image of the MESFET after transfer and thermally assisted cold-weld bonding to the plastic substrate. c) Source-drain current versus source-drain voltage (I_{DS}–V_{DS}) characteristics measured under various gate biases (V_G), d) source-drain current versus gate voltage (I_{DS}–V_G) transfer characteristics at V_{DS} = 3 V, and e) transconductance after the first and second ND-ELO-processed MESFETs from a single parent wafer. Differences in characteristics are due to variations in device processing from run to run.

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shows a scanning electron microscope image of a fabricated MESFET, Figure 5c,d present source drain current-gate voltage (I_{DS}–V_G) and transfer curves after the first and second ND-ELO cycles. The transconductance characteristics of thin film MESFETs are extracted from the transfer curve, and compared in Figure 5e. The similar transconductances of 7.5 ± 0.5 mS and 8.5 ± 0.5 mS for the first and second ND-ELO processed MESFETs which is more than twice that of MESFETs fabricated with similar technology on glass substrates,[15] shows that ND-ELO growth quality for these majority carrier electronic devices is not compromised by wafer recycling, epi-layer cleaning, and cold-weld bonding. Minor variations in device performance arise from variations in fabrication and growth from run-to-run.

The nearly identical performance of both minority (solar cells and LEDs) and majority (MESFETs) carrier devices that are grown and lifted-off from as-delivered and reused wafers confirms the feasibility of our ND-ELO wafer reuse process, as well as the generality of the fabrication methods using epitaxial protection layers and substrate cleaning combined with cold weld bonding to a secondary substrate. The protection layers preserve the surface quality during the ND-ELO process, as well as eliminating wafer thinning caused by the conventional polishing. Therefore, this method allows for potentially unlimited wafer recycling. Furthermore, all devices are directly fabricated on a flexible thin-film plastic substrate instead of rigid and bulky platforms such as glass or Si, thereby eliminating the need to transfer the fragile epitaxial active regions twice, as is required in conventional ELO processing. In addition, the acceleration of the lift-off process via external strain makes this process compatible for use with large area substrates. The extreme flexibility of this approach makes it useful for deploying the mounted substrates on compact roles prior to unfurling for a particular application (i.e., area coverage by solar cells for terrestrial or space-borne purposes), as well as lending itself to simplified attachment of devices on conformal or pre-deformed substrate surfaces.[19,20]

3. Conclusion

In summary, we have demonstrated a universal method for creating a variety of very low cost GaAs-based single crystalline thin film optoelectronic devices including photovoltaic cells, LEDs and MESFETs. The process involves a unique, non-destructive ELO process that allows multiple growth and active epitaxial film removal cycles, thereby transforming the conventional high cost of materials associated with the substrate to a capital cost. We developed unique methods for substrate bonding, wafer protection and cleaning, and combined them with ND-ELO to avoid the typically wafer consuming repolishing step. A non-destructive substrate reuse method without performance degradation provides the potential for dramatic production cost reduction along with extending the application of high performance group III-V optoelectronic devices by moving from bulky, two dimensional substrate-based platforms to conformal, flexible and light weight thin film devices. This technology is a critical step towards allowing III-V devices to overcome the cost barriers impeding their widespread acceptance in mainstream commercial applications.

4. Experimental Section

Epitaxial Growth: The epitaxial layer structures are grown by gas-source molecular beam epitaxy (GSMBE) on Zn-doped (100) p-GaAs substrates. For the protection layer, the growth starts with GaAs (0.1 μm)/$In_{0.49}Ga_{0.51}P$ (0.05 μm)/GaAs (0.1 μm) layers followed by a 20 nm thick AlAs sacrificial layer. Next, an inverted active device region is grown as follows: For the photovoltaic cells we grow a 0.1 μm thick, 5×10^{18} cm^{-3} Be-doped GaAs contact layer, 0.025 μm thick, 2×10^{18} cm^{-3} Be-doped $Al_{0.20}In_{0.49}Ga_{0.31}P$ window layer, 0.15 μm thick, 1×10^{18} cm^{-3} Be-doped p-GaAs emitter layer, 3.0 μm thick, 2×10^{17} cm^{-3} Si-doped n-GaAs base layer, 0.05 μm thick, 6×10^{17} cm^{-3} Si-doped $In_{0.49}Ga_{0.51}P$ back surface field (BSF) layer, and 0.1 μm thick, 5×10^{18} cm^{-3} Si-doped n-GaAs contact layer. For the light emitting diodes (LEDs) we grow a 0.1 μm thick, 5×10^{18} cm^{-3} Be-doped GaAs contact layer, 0.8 μm thick, 2×10^{18} cm^{-3} Be-doped $Al_{0.20}In_{0.49}Ga_{0.31}P$ layer, 0.1 μm thick un-doped $In_{0.49}Ga_{0.51}P$ layer, 0.8 μm thick, 2×10^{18} cm^{-3} Si-doped $Al_{0.20}In_{0.49}Ga_{0.31}P$ layer, 0.1 μm thick, 5×10^{18} cm^{-3} Si-doped n-GaAs contact layer. For the metal semiconductor field effect transistors (MESFETs) we grow a 0.05 μm thick, 5×10^{18} cm^{-3} Si-doped GaAs contact layer, 0.16 μm thick, 4×10^{17} cm^{-3} Si-doped GaAs channel layer, 1 μm thick un-doped GaAs layer. GaAs/ AlAs layers are grown at 600 °C and $Al_{0.20}In_{0.49}Ga_{0.31}P$/$In_{0.49}Ga_{0.51}P$ layers are grown at 480 °C.

Cold Weld Bonding: Two freshly deposited 350 nm thick Au films on opposing surfaces are bonded together with the application of pressure. Thus, the GaAs wafer with epitaxial layer is bonded to the Kapton® sheet using an EVG 520 wafer bonder under ~10^{-5} Torr vacuum immediately following Au deposition by e-beam evaporation. For a 2 inch-diameter substrate, 4 MPa of pressure is applied to establish a bond between the two gold films with a 80 N/sec ramping rate. Then the thermally assisted cold-weld bonding process is carried out by ramping the temperature at 25 °C min^{-1} to 175 °C and holding at the peak temperature for 3 min. The substrate temperature is subsequently reduced using active stage cooling. To apply a uniform force over the sample area, a reusable, soft graphite sheet is inserted between the sample and the press head.

Epitaxial Lift-Off: Once the GaAs substrate is bonded to the Kapton sheet, the thin active device region is removed from its parent substrate through the ND-ELO) process. The entire sample is immersed in a 20% HF solution maintained at 60 °C. The HF solution is agitated with a stir bar at 400 rpm. Due to the high etch selectivity between AlAs and the active compound semiconductor layers, dilute HF removes the 20 nm thick AlAs sacrificial layer between the wafer and active device region without attacking the adjacent protection layers. The total lift-off time for a 2 inch GaAs substrate is approximately 5 h.

GaAs Single Junction Photovoltaic Cells: After lift-off, the thin-film active region and flexible plastic secondary substrate is fixed to a rigid handle for convenience throughout the remainder of the fabrication process. The front finger grid is photolithographically patterned using an LOR 3A and S-1813 (Microchem) bi-layer photoresist process, then a Pd(5 nm)/Zn(20 nm)/Pd(15 nm)/Au(700 nm) metal contact is deposited by e-beam evaporation. The finger grid and bus bar widths are 25 μm and 80 μm, respectively, and the spacing between grid lines is 660 μm. The total coverage of the front contact is 5.8%. After the metal layer is lifted-off, an array of 5 mm × 5 mm device mesas are defined by photolithography using S-1827 (Microchem) and chemical etching using H_3PO_4:H_2O_2:deionized H_2O (3:1:25). The exposed, highly-doped 100 nm thick p+ GaAs contact layer is subsequently selectively removed using the same etchant. The thin-film solar cells are annealed for 1 h at 200 °C for Ohmic contact formation. Finally, to achieve a minimum surface reflection, a bilayer anti-reflection coating (ARC) consisting of TiO_2 (49 nm) and MgF_2 (81 nm) is deposited by e-beam evaporation.

Light-Emitting Diodes (LEDs): After the ND-ELO process, the thin-film active region and flexible plastic secondary substrate is fixed to a rigid substrate as in the case of the solar cell processing. The front finger grid is patterned by photolithography as in the case of the solar cells. Then, a Pd(5 nm)/Zn(20 nm)/Pd(15 nm)/Au(300 nm) metal contact is deposited by e-beam evaporation. The width of front grid is 25 μm, and a 300 μm × 300 μm contact pad is patterned at the center of the grid.

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The total coverage by the front contact is 22.7%. After the metal layer is lifted off, 680 μm × 680 μm mesas are defined by photolithography using S-1827 (Microchem) and chemical etching using the same etchants as for the solar cells. The thin-film LEDs are annealed for 1 h at 200 °C for Ohmic contact formation.

Metal Semiconductor Field Effect Transistors (MESFETs): After lift-off, 225 μm × 250 μm mesas for Ohmic contacts and channel layers are photolithographically defined as for solar cells. Then 210 μm deep mesas are etched with an inductively coupled plasma using a Plasmalab System 100 (Oxford Instruments). For plasma etching, the sample was attached to a Si wafer carrier using thermal paste and Kapton tape. During the etch process, the stage is actively cooled to 5 °C using LN_2. The source and drain contacts are patterned using photolithography, and a Pd(5 nm)/Ge(50 nm)/Au(300 nm) metal contact is deposited by e-beam evaporation. The width and length of channel are 250 μm and 25 μm, respectively. After the metal layer is lifted-off, a 50 nm highly n-doped GaAs contact layer and the 10 nm thick channel layer are selectively removed by inductively coupled plasma etching using the same procedure as above. The MESFETs are annealed for 1 h at 240 °C for Ohmic contact formation. Finally, the gate contact is patterned using photolithography, and a Ti(5 nm)/Au(300 nm) metal contact is deposited by e-beam evaporation. The patterned gate length is 11 μm measured by optical microscope.

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