Compound Semiconductor-Based Thin-Film and Flexible Optoelectronics

by

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To my parents, wife and son

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ABSTRACT

Compound semiconductors are the basis of modern optoelectronics due to their intrinsically superior optical and electronic properties compared with elemental semiconductors. However, their applications remain limited due to a prohibitive substrate cost. This limitation has driven the development of epitaxial lift-off (ELO) technology that separates the thin-film epitaxial layer from the substrate by selectively removing a sacrificial layer between them. However, ELO has its own limitations including a long process time, complicated transfer to a secondary, low cost host substrate, and wafer surface degradation which prevents wafer recycling.

In this thesis, we address all of these limitations by developing a new, non-destructive ELO (ND-ELO) process. When combined with adhesive-free cold-weld bonding of the wafer directly to a plastic substrate, ND-ELO provides an approximately 100 times reduction in process time, and a considerably simplified transfer process compared with conventional ELO. Furthermore, it allows indefinite wafer reuse by employing the epitaxial protection layers, eliminating surface degradation of the parent wafer encountered in conventional ELO. We demonstrate the feasibility and generality of this process by applying it to optoelectronic devices including photovoltaic cells, LEDs, MESFETs and photodetectors on two compound semiconductor systems, InP and GaAs. Furthermore, we present an approach that can achieve an estimated cost of only 3% that of conventional GaAs solar cells using an accelerated ND-ELO wafer recycling process, and integrated with lightweight, thermoformed plastic, truncated mini-compound parabolic concentrators (CPC) that avoid the need for active solar tracking. Using solar cell/CPC assemblies,

without daily solar tracking, the annual energy harvesting is increased by 2.8 times compared with planar solar cells. This represents a drastic cost reduction in both the module and balance of systems costs compared with heavy, rigid conventional modules and trackers that are subject to wind loading damage and high installation costs. The demonstration of cost-efficient and high performance compound semiconductor-based flexible thin-film optoelectronics is a critical step toward allowing their widespread deployment in mainstream state-of-the-art applications including wearable, flexible and conformal devices.

Chapter I

Introduction

Group III-V compound semiconductors consist of group III (Ga, In, Al, etc.) and V (N, As, P Sb, etc.) elements of the periodic table bonded predominantly by covalent and partly ionic forces mostly into a zinc-blend structure. Compound semiconductors provide the unique benefit of bandgap tuning by forming binary, ternary, quaternary or quinternary alloys. Furthermore, their intrinsic properties of high carrier mobility and capability of engineering to a direct or indirect bandgap make them attractive for many applications. Due to their superior intrinsic properties over elemental semiconductors, compound semiconductors are widely used, especially for optoelectronic devices such as lasers, LEDs, solar cells, photodectors, high frequency electronics, etc., which deal with the interaction between electronic and optical process usually accompanied by an energy conversion. This chapter introduces III-V compound semiconductor technology and outlines this thesis.

1.1 Overview of III-V compound semiconductors

1.1.1 Bonding in compound semiconductors

The attractive and repulsive forces that exist between atoms is determined by their interatomic distance.[1] At very small distances between two atoms, a repulsive interaction is

dominant, therefore the atoms push each other away. At large interatomic distances, attractive forces are dominant, hence the atoms are drawn to each other. The balance of forces between atoms results in an equilibrium atomic spacing (equal to lattice constant, a) which is slightly modified by lattice vibrations at room temperature due to thermal energy.[1] Figure 1.1 shows the interatomic forces in a solid.[2]

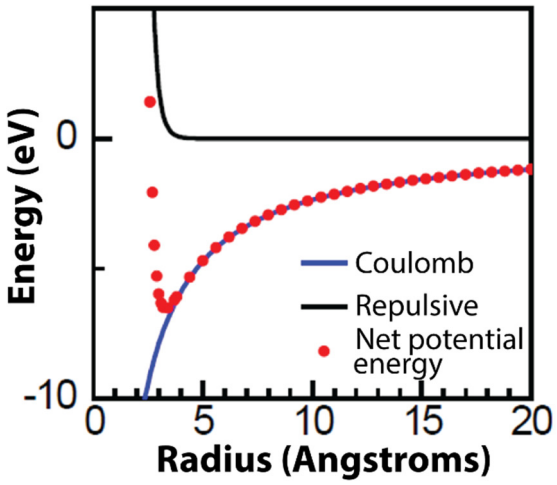


Fig 1.1: Interatomic forces. Balance of Coulombic and repulsive interaction depending on atomic separation. Reproduced from ref 2.

The binding energy E, the minimum energy to break the bond, is affected by the type of bonding. Bonding can be classified into four groups depending on the dominant attractive force. First, *van der Waals bonding* is created by the formation of dipoles arising from the relative distributions of atoms and the electrons. A second group is *metallic bonding* in which the conduction electrons are shared by many positively charged ions. Third, *ionic bonding* is the result of the attraction between positively and negatively charged ions. Lastly, *covalent bonding* involves the sharing of electrons between neighboring atoms to reduce the potential energy of a system by forming closed outer shells. The bonding in elemental semiconductors (e.g. Si and Ge)

is purely covalent. On the other hand, there is a small degree of charge transfer between group III and V atoms due to the difference of electronegativity between the two atoms, therefore the bonding in compound semiconductors has partial ionic content along with predominantly covalent forces.[3]

1.1.2 Crystalline structure of compound semiconductors

A crystal is characterized by having a periodic arrangement of atoms.[4] The smallest space-filling unit that contains the different elements which comprise the crystal is called a primitive unit cell. Silicon, which is the most intensively investigated elemental semiconductor, is crystallized into a diamond structure, thus each atom is surrounded by four nearest equivalent atoms, and the shared valence electrons form a complete outer atomic shell.[3] In a compound semiconductor, atoms are often crystallized in a zinc-blend structure (Fig. 1.2) which allows them to share the electrons with four nearest neighbor atoms similar to elemental semiconductors. A zinc-blende structure belongs to the tetrahedral configuration. It is two face-centered cubic (fcc) structures interpenetrate by one-quarter of a lattice constant. Hence, it is identical to a diamond structure except that there are two rather that one atom in the lattice, forming its basis. The bonds between the nearest group III and V elements and between the nearest equivalent atoms in zinc-blende structures are in the [111] and [110] directions, respectively.[3] The periodic arrangement of atoms determines the band structure and crystal potential of materials, which affects their electrical and optical properties.

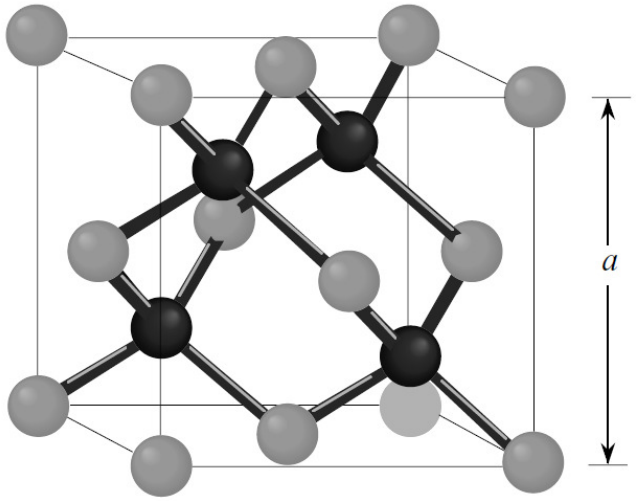


Fig 1.2: Zinc-blende crystal structure, consisting of two face-centered cubic (fcc) structures interpenetrated by one-quarter the lattice constant, a. Reproduced from reference 3.

Depending on the combination of elements in the alloy, the energy band gap can be engineered to meet high performance electronic and optoelectronic device requirements. Compound semiconductors alloys can be binary (GaAs, InP etc.), ternary (AlGaAs, InGaAs, GaAsP etc.), quaternary (InGaAsP, AlGaInP etc.) or quinternary (InGaAlAsP etc.) compounds by randomly mixing the group III or V lattice sites with various elements. Figure 1.3 shows lattice constants and energy bandgaps of several semiconductor alloys. In general, the lattice constant follows a linear relationship with composition; however, the energy bandgap does not exhibit a perfect linear dependence on the composition due to bandgap bowing caused by alloy disorder.[1] The alloy semiconductors are widely used for the applications to optoelectronic devices such as light emitting diodes that cover a wide range of the emission spectrum, and sources and detectors for optical communication.

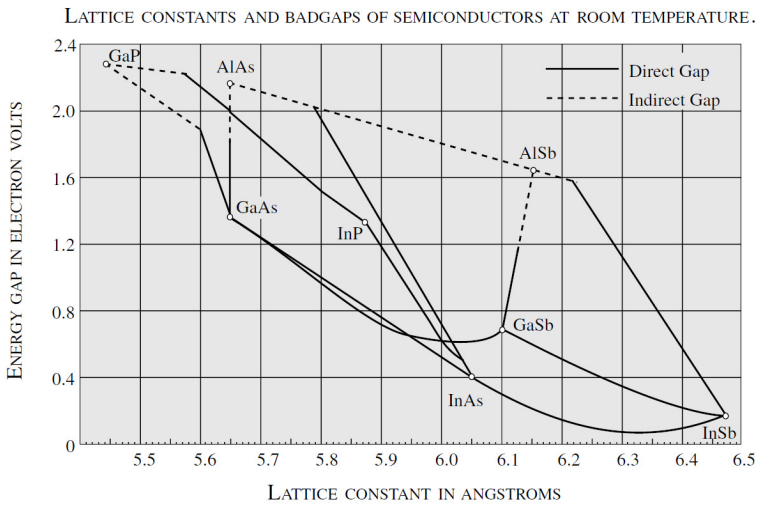


Fig 1.3: Lattice constants and energy bandgaps of semiconductors. Achievable bandgaps and lattice constants of III-V compound semiconductors at room temperature by various alloy formations. Reproduced from reference 3.

1.1.3 Built-in strain in compound semiconductors

One major limitation for energy bandgap engineering is lattice matching between the epi-layers and the substrate. To overcome this limitation, Matthews and Blakeslee investigated lattice-mismatched growth which results in built-in strain to the lattice mismatched layer when the thickness is less than a critical value.[5] The growth of this strained crystalline epitaxial layer growth is called *pseudomorphic.* Strain can be either tensile or compressive depending on the difference of the lattice constant between the epitaxial layer and the substrate.[3] The strain energy is affected by the thickness of the mismatched film; as it gets thicker, the strain increases. When the thickness of the strained film exceeds the critical thickness, dislocations are formed that relax the strain energy. The built-in strain is useful to modify the energy gaps of optoelectronic devices such as lasers or modulators that contain quantum wells. Furthermore, fully strain-relaxed pseudomorphic layers can be employed as growth buffer layers to create an effective interface with modified lattice constants.

1.2 Crystal growth methods

Crystal growth can be divided into two categories: bulk crystal growth for substrate preparation, and epitaxy of thin films on top of a crystalline substrate.

1.2.1 Bulk crystalline substrate growth

For crystalline substrate preparation, two kinds of bulk crystal growth techniques can be employed. Fig 1.4 shows a schematic of Czochralski (Cz) growth. Cz growth is used to create a single crystalline ingot by using a seed crystal dipped in a molten compound material, usually in a pyrolytic boron nitride (PBN) crucible under a pressurized vessel, and slowly pulled while being rotated at the same time.[3] The Cz growth method provides a high quality crystal and enables doping and orientation control; however, it requires very accurate control of temperature and ambient pressure to precisely control the ingot diameter and maintain a uniform stoichiometry.[3]

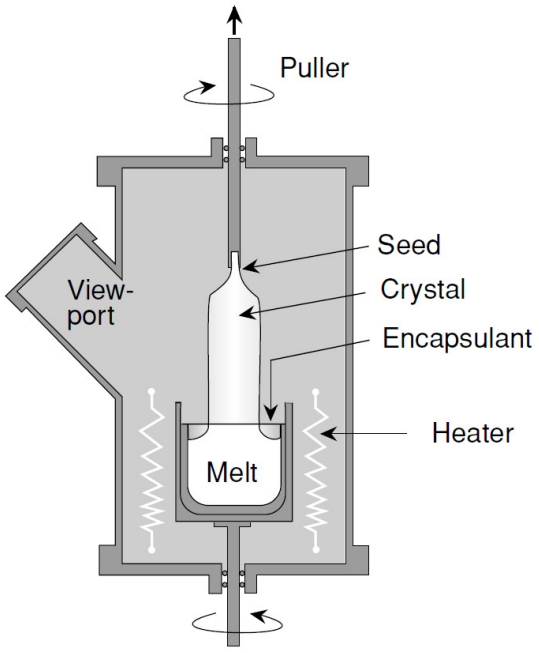


Fig 1.4: Schematic of Czochralski process. Ingots of crystalline semiconductor, such as Si, GaAs and InP are grown using the Czochralski process. Reproduced from reference 3.

Fig 1.5 shows a schematic of horizontal Bridgeman and gradient-freeze growths, which can also be used for preparation of single crystalline ingots. Both processes are furnace growth techniques where a seed crystal placed in a quartz boat that is heated in a sealed quartz tube. The material is crystallized by slowly lowering the boat temperature from the seeded end by either moving the hot zone of the furnace along the tube or slowly removing the boat from the hot zone.[3] This method is relatively inexpensive and especially useful to grow phosphorus-containing compound semiconductors which require a high group V overpressure. However, ingot size and shape control is limited by the boat geometry, and the contact with crucible during growth may cause dopant incorporation and stress at the interface between the boat and the crystal.[3]

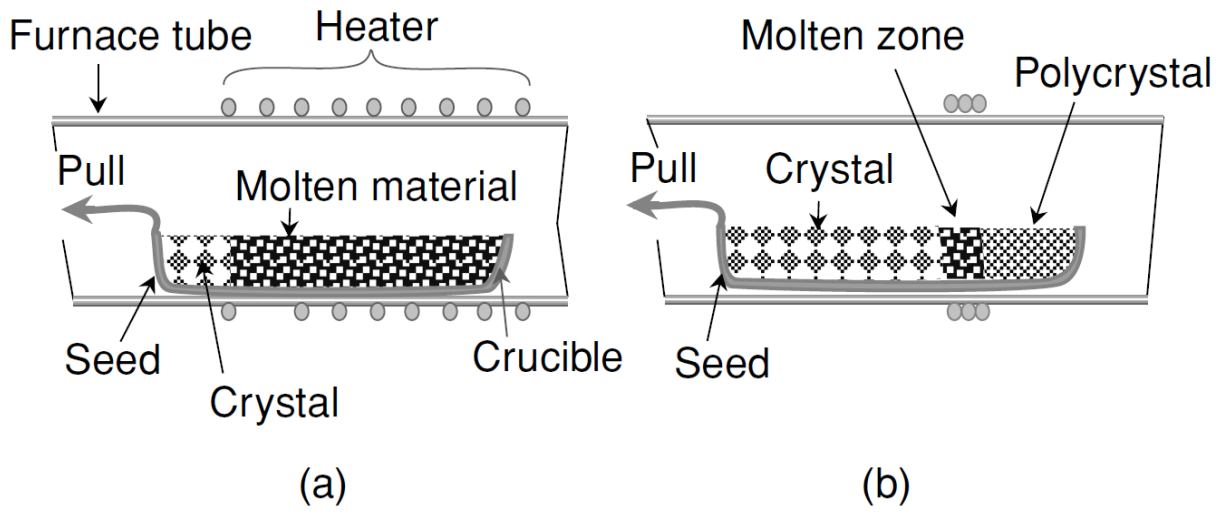


Fig 1.5: Schematic of horizontal bridgeman and gradient-freeze growths. Crystal growth by slowly lowering the boat temperature from the end with the seed by (a) moving the hot zone of furnace along the tube (horizontal bridgeman growth) or (b) slowly pulling out the boat (gradient-freeze growth). Reproduced from reference 3.

1.2.2 Epitaxy

Various epitaxial growth techniques have been developed to grow a crystalline thin film layer on top of the bulk substrate. The first demonstration of compound semiconductor epitaxy was by liquid phase epitaxy (LPE).[1] Fig 1.6(a) shows a schematic of LPE growth that occurs from a molten mixture of the constituent elements.[3] LPE provides high quality materials at a relatively low cost; however, it is difficult to grow abrupt junctions and immiscible alloys by LPE growth.[3] In contrast, vapor phase epitaxy (VPE) is a crystal growth process performed under a gaseous environment (Fig 1.6(b)). The crystal formation in VPE results from the chemical reaction of the supplied gases and the heated substrate.[3] VPE allows growth of extremely high purity materials.[3] Metal organic chemical vapor deposition (MOCVD) is a similar growth technique to VPE where the growth takes place via chemical reaction between precursors and the heated substrate. It enables the growth of high quality heterostructures with atomically abrupt interfaces.[3]

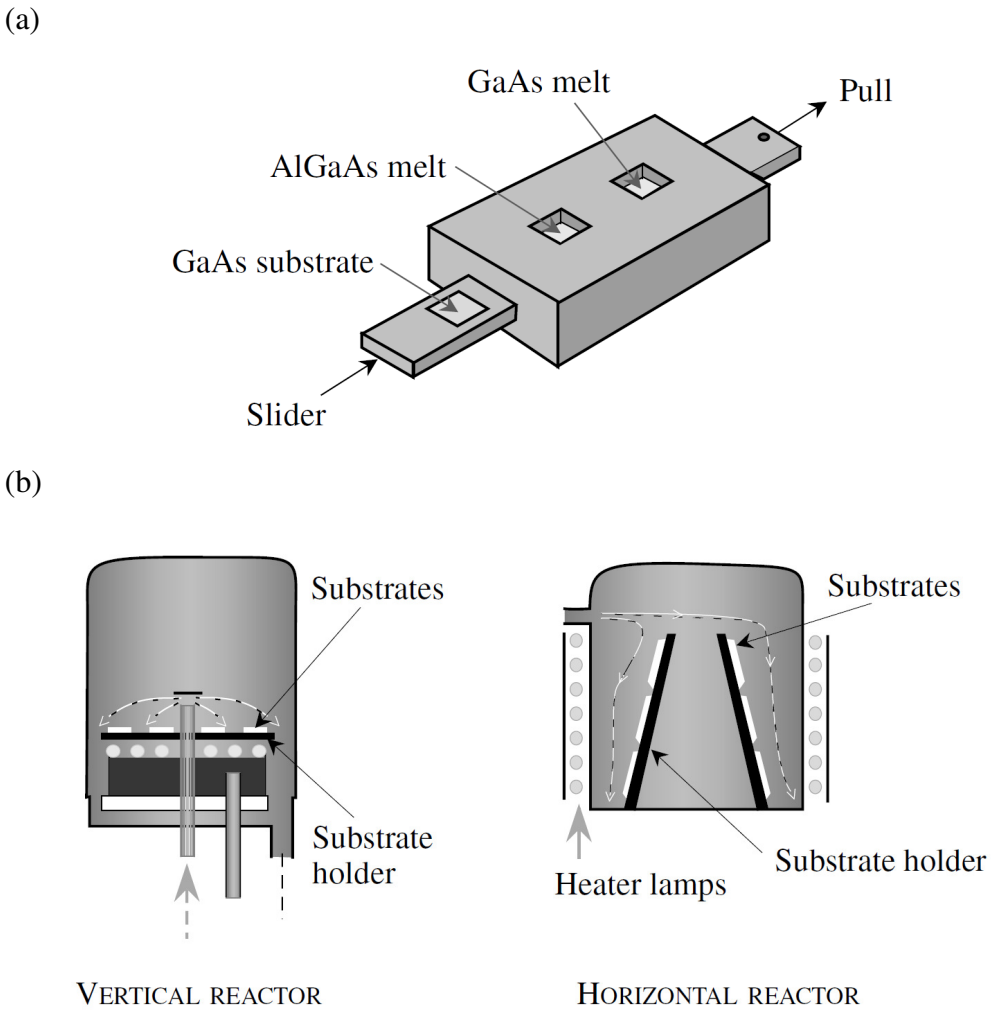


Fig 1.6: Schematic of LPE and VPE growths (a) The heterostructure can be grown by contacting the substrate with different melts using slider (LPE). (b) The crystal growth occurs in vertical or horizontal reactor via chemical reaction of the supplied gases with the heated substrate (VPE). Reproduced from reference 3.

Lastly, molecular beam epitaxy (MBE) can be employed as a growth process for almost every kind of compound semiconductor alloy. Fig 1.7(a) shows a schematic of an MBE chamber. Thin film growth occurs in MBE via reaction between thermally evaporated molecular beams of the constituent elements and a substrate surface[6]. MBE growth is carried out under an ultra-high vacuum with a cryogenically cooled shroud. The process is far from thermodynamic equilibrium,

and is governed mainly by the kinetics of the surface processes occurring when the impinging beam reacts with the outermost atomic layers of the substrate crystal[6]. This is distinguished from LPE and VPE that are at or near thermodynamic equilibrium, and are controlled by diffusion occurring in the crystallizing phase surrounding the substrate.[6] In this thesis work, we employed gas source MBE (GSMBE) for the epi-layer growth which has been developed for epitaxy of ternary and quaternary compound semiconductors on InP substrates using metaloganic group V sources (e.g. AsH_3 and PH_3).[7]

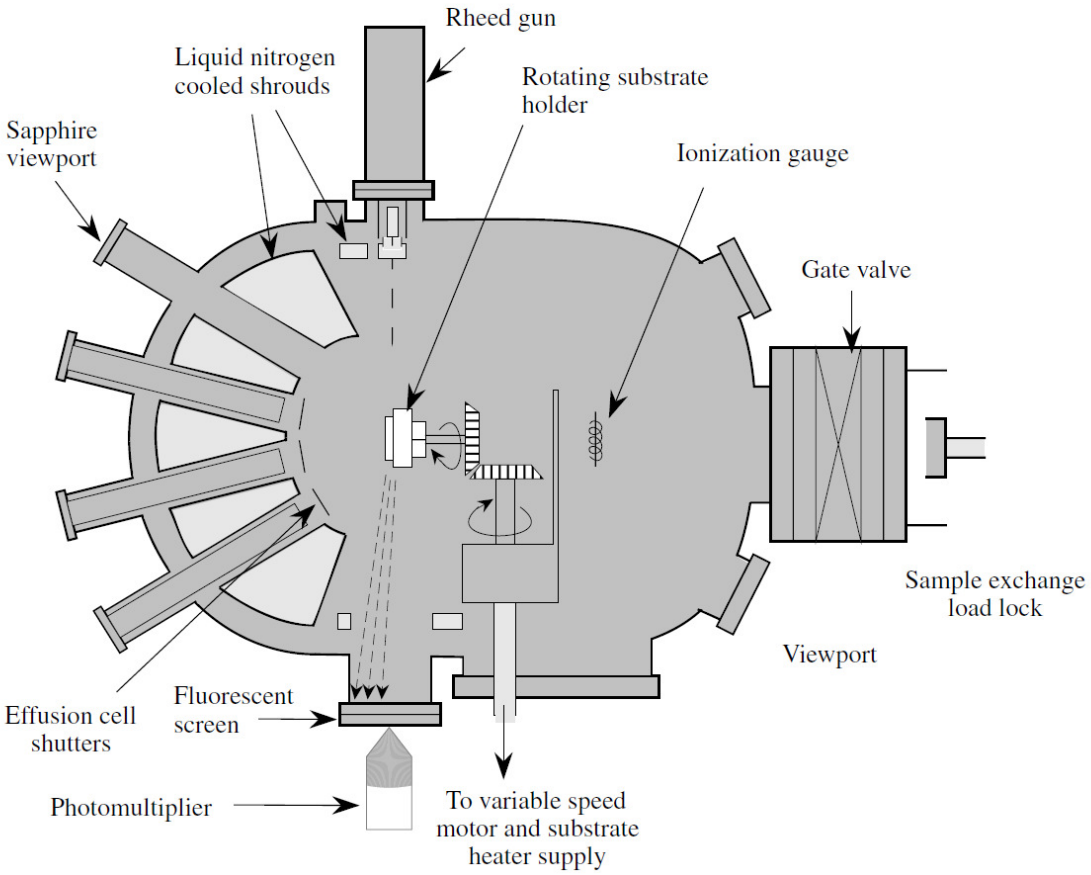


Fig 1.7: Schematic of MBE chamber. Reproduced from reference 3.

1.3 Application of compound semiconductors to optoelectronic devices

Compound semiconductors are widely used for a variety of optoelectronic devices due to their unique properties of high carrier mobility and tunable bandgaps. Here, we introduce several major applications of compound semiconductors.

1.3.1 Photovoltaic cells

Photovoltaic cells are a promising application for compound semiconductors. According to detailed balanced theory, GaAs has nearly the ideal bandgap energy (1.43 eV) to achieve the highest power conversion efficiency which approaches the thermodynamic limit.[8] GaAs is a direct bandgap semiconductor, therefore it requires a relatively thin active layer (~few microns) to achieve the full absorption of the solar spectrum within the bandgap range compared with an indirect bandgap semiconductor such as Si, which requires an active layer hundreds of microns thick to fully absorb the solar spectrum near its band edge at 1.1 eV. Furthermore, lattice matched, wide bandgap compound semiconductors such as InGaP and AlGaInP can be employed as window and back surface field (BSF) layers what prevent non-radiative recombination of the photogenerated carriers near the surface or at an interface. Moreover, the combination of bandgap tuning and metamorphic growth allows the production of multi-junction solar cells that enable the minimization of thermalization losses using a stack of single junctions, carefully matching the photogenerated current density between each cell. Multi-junction solar cells are especially suitable for space or concentrated photovoltaic applications. To date, four-junction compound semiconductor solar cells provide the highest power conversion efficiency (44.7% under 297 suns) among all solar cell technologies.[9]

1.3.2 Photodiodes

Compound semiconductors are widely used for photodetector applications. Photodetectors can be classified into three categories: photoconductors, *pin* photodiodes and avalanche photodiodes.[1] Photoconductors and avalanche photodiodes have internal gain, and *pin* photodiodes have a wide bandwidth without internal gain. Compound semiconductor-based photodiodes are mainly used for fiber optic communication systems to receive transmitted optical pulses and convert them into electronic pulses with a minimal loss of signal. Especially, InGaAs photodetectors grown on lattice matched InP substrates are widely used to cover the infrared wavelength range where optical glass fibers have minimum loss and dispersion. Furthermore, they provide high speed, reliability and sensitivity, low noise and wide bandwidth which are the figures of merit for photodiodes in optical communication systems. The photodetector can also be used for wavelength division multiplexing (WDM) or focal plane arrays (FPA) in imaging applications.

1.3.3 Light emitting diodes

Compound semiconductors are also intensively used for light emitting diode (LED) applications due to their capability of bandgap tuning to reach the desired emission spectrum by appropriately composition. The LED is an optoelectronic device that emits photons with energy corresponding to the bandgap of the active layer by radiative recombination of the injected carriers. In general, *p-n* junctions or double heterostructures are employed. LEDs are spontaneous emission sources. Until the 1980s, GaP-based LEDs were used for visible light emission from isoelectronic traps.[1] However, recent development of nitrogen-based wide bandgap compound semiconductors enable the emission of blue light; hence expanding the applications of LEDs to displays, indicator lamps and quasi-white lighting sources, etc. Furthermore, LEDs can be employed as a source in fiber optic communication links by designing the structure to emit infrared light.

1.3.4 Lasers

Unlike LEDs, lasers (light amplification by stimulated emission of radiation) are a stimulated rather than a spontaneous emission source.[1] Stimulated emission relies on population inversion; therefore, lasing requires gain and feedback by a combination of electrical and optical confinement within the active region. Gain occurs when the number of emitted photons are greater than the number lost to absorption. To enhance amplification, an optical feedback system, such as a *Fabry-Perot cavity,* is employed to make photons pass through the gain medium multiple times. Lasers can be demonstrated by making a diode with a quantum well using a heterostructure between compound semiconductors of different composition. Emission wavelength is controlled by tuning the width and depth of the quantum well. Furthermore, to efficiently capture injected carriers in the quantum wells, and to enhance the overlap between the optical mode and gain medium, single quantum well lasers can be modified into a *multiple quantum well* (MQW) structures or *graded-index separate confinement heterostructures* (GRINSCH).[1] Moreover, epitaxy of compound semiconductors enables the demonstration of *vertical-cavity surface emitting lasers* (VCSELs) by cladding the active region with *distributed Bragg reflectors* (DBRs) consisting of alternating compound semiconductor layers with different refractive indices. VCSELs are a top emission device, therefore coupling to optical fibers is convenient compared with edge emitting lasers.

1.3.5 Field effect transistors

Superior carrier mobilities of compound semiconductors compared with elemental semiconductors such as Si, enables the demonstration of the high speed field effect transistors. Among various compound semiconductor transistors, *high electron mobility transistors* (HEMTs) have a similar device structure with *metal oxide semiconductor field effect transistors* (MOSFETs)

except that they employ a wide bandgap semiconductor spacer layer instead of a gate oxide. HEMTs can operate at very high frequencies through reducing the scattering of channel electrons caused by the ionized impurities in a lightly doped channel layer. Therefore, carrier mobility can be further improved. Moreover, *metal semiconductor field effect transistors* (MESFETs) and *junction field effect transistors* (JFETs) have been demonstrated by using Schottky barrier or *p+/n* junction gates. Compound semiconductor-based transistors are an important element in optoelectronic integrated circuits (OEIC) when coupled with photonic devices. An OEIC on a single substrate enabled by monolithic growth, provides the potential to demonstrate high-speed, highly-sensitive, reliable and compact devices.[1]

1.4 Technology challenges

As described above, compound semiconductors provide many benefits over elemental semiconductors for numerous applications; however, these applications are mainly limited by the cost and quality of the starting substrates. High quality substrates are only available for few materials such as GaAs and InP, whereas only small and costly GaN and GaSb substrates are commercially available. Even for GaAs and InP which are produced by relatively mature bulk crystal growth technologies, the cost is much higher than for Si substrates Therefore, their applications are limited to only few special uses such as lasers, LEDs and space-borne solar cells. The best available commercial price for a 6" GaAs substrate is ~$150, approximately 100 times more expensive compared with the same volume of Si wafers. Therefore, it is essential to overcome the device production cost barrier caused by expensive substrates to allow compound semiconductor devices to leverage their applications into mainstream commercial technology.

The common drawback of single crystalline semiconductor technology, including both elemental and compound semiconductors, is that their application is mostly limited into 2 dimensional devices on a bulky, brittle and rigid substrates. This is due to the post-processing of bulk crystalline substrate growth which includes diffusion, implantation or epitaxy to form an active device region. However, to fulfill the requirements of current state-of-art applications, such as wearability, conformity or light-weight devices, it is necessary to implement thin-film devices onto lightweight, flexible, or stretchable platforms.

1.5 Thesis overview

This thesis is focused on addressing the potential solutions for two major technological challenges confronting compound semiconductors:

1. Production cost reduction by recycling the parent wafer multiple times
2. Demonstration of lightweight and flexible thin-film devices on a plastic substrates

Substrate recycling is a promising solution to dramatically reduce the device production cost by reducing the expensive wafer cost. This can be achieved by epitaxial lift-off (ELO) techniques that separate the active thin-film layer from the substrate by selectively etching a sacrificial layer of different composition inserted between the substrate and active device region. Therefore, the remaining parent substrate can be reused after the lift-off process. Furthermore, the ELO process creates a thin-film crystalline device; hence, the transfer of a thin-film active region to a lightweight and flexible platform such as plastic or metal foil can be realized. However, wafer recycling using conventional ELO processes has been limited since wet-etching the sacrificial layer leaves a degraded surface which prevents single crystalline epitaxy on its surface. Therefore,

chemo-mechanical polishing (CMP) processes generally are used after the ELO process, which restricts the number of wafer recycles, and incurs the cost of the CMP process itself. Furthermore, transfer of the thin-film device active region onto a flexible plastic substrate usually requires multiple steps that include use of adhesives. To overcome these issues, in this dissertation we demonstrate using epitaxial protection layers to preserve the surface quality during the ELO and cold-welding processes to simplify the thin film transfer process.

In Chapter 2, we review thin-film technologies based on compound semiconductors, including ELO processes and cold-welding methods. In chapter 3, we introduce a cold-welding process and epitaxial protection layers which are employed for wafer bonding and substrate recycling. In Chapter 4, we demonstrate multiple growths of InP/ITO Schottky barrier thin-film solar cells from a single wafer via the combination of ELO, epitaxial protection layer and cold-welding processes. In Chapter 5, a thin-film InGaAs *pin* photodiode on a flexible substrate with nearly 100% external quantum efficiency (EQE) and 100% array fabrication yield is demonstrated via ELO and cold-weld bonding from the InP substrate. In Chapter 6, we demonstrate non-destructive recycling of a GaAs substrate in the fabrication of various thin-film optoelectronic devices including *pn* junction GaAs solar cells, LEDs and MESFETs without performance degradation from run to run. In Chapter 7, we describe a method that dramatically reduces solar module production cost compared with conventional substrate-based and ELO-processed GaAs solar cells by integrating the non-destructive ELO (ND-ELO) processed thin-film GaAs solar cells with plastic-based, low-cost thermoformed non-tracking mini-compound parabolic concentrators (CPCs). In Chapter 8, a variety of applications using the ND-ELO process are described including multifunctional thin-film solar cell arrays embedded with an ultra-high frequency (UHF) antenna and an RF choke on a flexible substrate, and a kirigami-based solar

concentration/tracking system. In Chapter 9, we summarize the results and provide suggestions of future work to further expand the applications of thin-film and flexible compound semiconductor technologies.

CHAPTER I

Bibliography

1. Bhattacharya, P. *Semiconductor Optoelectronic Devices*. Prentice Hall (1997).

2. Renshaw, C. K. Hybrid Organic/Inorganic Optoelectronics. *Doctoral dissertation* (2014)

3. Singh, J. *Electronic and optoelectronic properties of semiconductor structures*. *Ann. Phys. (N. Y).* **54,** 258 (2003).

4. Sze, S. M. & Ng, K. K. in *Phys. Semicond. Devices, 3rd Ed. John Wiley Sons, Inc.* (2007).

5. Matthews, J. Defects in epitaxial multilayers I. Misfit dislocations. *J. Cryst. Growth* **27,** 118–125 (1974).

6. Herman, M. A. & Sitter, H. *Molecular Beam Epitaxy*. Springer Berlin Heidelberg, (1996).

7. Panish, M. B. & Temkin, H. *Gas Source Molecular Beam Epitaxy*. Springer Berlin Heidelberg (1993).

8. Shockley, W. & Queisser, H. J. Detailed Balance Limit of Efficiency of p-n Junction Solar Cells. *J. Appl. Phys.* **32,** 510 (1961).

9. Green, M. A., Emery, K., Hishikawa, Y., Warta, W. & Dunlop, E. D. Solar cell efficiency tables (version 44). *Prog. Photovoltaics Res. Appl.* **22,** 701–710 (2014).

Chapter II

Lift-Off Technologies for Advanced Optoelectronics

The development of various lift-off technologies enables the production of single crystalline thin-film optoelectronics by transplanting the active epitaxial device region from the bulk, rigid substrate to inexpensive, flexible and lightweight foils. Lift-off technologies present two major advancements for optoelectronic applications: cost reduction via wafer recycling, and improved performance in some devices via light trapping/photon recycling. Among various approache to achieving thin-film optoelectronics, of particular promise is epitaxial lift-off (ELO), a technology that creates single crystalline thin-film optoelectronics by selectively removing sacrificial layer between the substrate and the device epitaxial layers. Considerable efforts have been focused on the development of the ELO process. As a result, the conventional ELO process has been improved by the introduction of non-destructive ELO (ND-ELO), weight-induced ELO (WI-ELO), surface tension assisted ELO (STA-ELO), and multi-epitaxial layer release processes, etc., to establish a thin-film optoelectronics technology that overcomes many cost and technical barriers. Furthermore, other lift-off technologies, such as controlled spalling, cleavage of lateral epitaxial films for transfer (CLEFT), and exfoliation have also been demonstrated. Based on recent developments in lift-off technologies, various thin-film optoelectronic devices such as photovoltaic cells, photodiodes, lasers, and LEDs have been demonstrated with superior

performance over substrate-based, bulky devices. The advance of lift-off technologies is a critical step towards moving thin-film optoelectronic devices into mainstream commercial applications.

2.1 Introduction

Thin-film optoelectronics generally refer to the technology based on semiconductor devices with very thin active layers (typically the range of a few nm to tenths of μm) on arbitrary substrates created by deposition or spin-casting processes. Unique features of these thin-film devices can be utilized for various device applications that are impossible or difficult to achieve by conventional bulk and rigid substrate-based technologies. Therefore, a wide variety of materials systems based on amorphous or polycrystalline semiconductors such as organic molecules, metal-oxides, amorphous-Si, copper indium gallium selenide (CIGS), copper zinc tin sulfide (CZTS) and perovskites, etc. are intensively investigated for numerous device applications. However, single crystalline semiconductor based thin-film technologies are still in their infancy due to immature fabrication processes and costly device production in spite of their superior properties. As the need for single crystalline semiconductor-based high performance thin-film optoelectronics is growing, various lift-off technologies have been developed, including epitaxial lift-off (ELO)[1,2], controlled spalling[3], cleavage of lateral epitaxial films for transfer (CLEFT)[4], and exfoliation[5]. The development of lift-off technologies provides potential solutions for overcoming the main bottleneck in many optoelectronic device fields: high device production cost and limited rigid, and bulky structures. Among the various lift-off technologies, ELO has received the most attention due to its capability for wafer recycling and for creating high performance optoelectronic devices on flexible and lightweight substrates.[1,2] Intensive efforts to improve the conventional ELO process have resulted in significant advances in the technology,

such as non-destructive ELO[6], weight-induced ELO[7] and multi-layer release processes[8]. Advanced ELO techniques combined with unique features of thin-film technology, for example light trapping[9] and photon recycling,[10,11] leads to extremely high performance optoelectronic devices on conformal substrates. The following sections are focused on reviewing the traditional and advanced ELO technologies, and other lift-off and bonding technologies are also introduced as possible candidates to realize advanced thin-film optoelectronics.

2.2 Epitaxial Lift-Off (ELO)

2.2.1 History of ELO

The first demonstration of the ELO process was in 1978 by Konagai et al., using liquid phase epitaxy (LPE) to fabricate thin-film GaAs solar cells[1]. The process was named "*peeled film technology* (PFT)", but is equivalent in almost all respects to conventional ELO. The PFT process employed a 5 μm thick $Ga_{0.3}Al_{0.7}As$ sacrificial layer to separate the 30 μm thick *n*-GaAs active device region from the wafer by selective etching. Thin-film GaAs solar cells were demonstrated using this method, and showed a *power conversion efficiency* (*PCE*) of 13.5% under 1 sun illumination. Furthermore, "multi-peeled film technology" was introduced at the same time as a means to create numerous GaAs thin-films from a AlGaAs/GaAs multi-layer stack. Recently, the multi-PFT has been employed to compare the dependence of the etch rate of a sacrificial layer on the Al fraction[12] and to create multiple optoelectronic devices from a single GaAs substrate.[8]

Almost a decade later, Yablonovitch et al., improved the PFT process by employing sufficiently thin sacrificial and active layers (100 nm thick and 3 μm thick, respectively) to efficiently curl the thin-film active region using black wax as a handle to transfer the epitaxy from the parent substrate to a secondary, final substrate.[2] Furthermore, it was claimed that the ELO

process was limited by the out-diffusion of dissolved H_2 gas from the etching zone. Therefore, the thinner active layers with a strained handle improves the out-diffusion of the process reaction product by introducing tension near the edge where the thin-film is curled. Later, this process was re-named *epitaxial lift-off* (ELO) by Yablonovitch et al., in a report where *van der Waals* bonding was employed to transfer the lifted-off thin films onto arbitrary substrates[13]. However, both PFT and ELO utilize the extreme etching selectivity ($>10^7$) between the sacrificial and active layers to create a thin-film crystalline structure.

In the mid-1990s, researchers at Radboud University systematically investigated Al(Ga)As sacrificial layer etching and the parameters that affect the lift-off speed. They developed weight-induced ELO (WI-ELO) to accelerate the ELO speed. A very high efficiency single junction thin-film GaAs solar cell (*PCE* of 26.1%) was achieved using an WI-ELO process which broke the approximately 20 year old single junction GaAs solar cell efficiency record.[14] A new record efficiency has NOW been achieved by Alta Devices (*PCE* = 28.8%) using the same process with improved photon recycling, pushing Alta's cell toward the thermodynamic efficiency limit.[15,16]

Multiple recycling of a parent substrate was demonstrated by combining the ELO process with chemo-mechanical polishing (CMP), further showing the potential for production cost reduction. However, the practical application of wafer recycling is still limited due to the prohibitive CMP process cost, and the restricted number of wafer recycles due to wafer thinning.[17,18] To alleviate the limitations for wafer reuse, we introduce in this thesis the non-destructive ELO (ND-ELO) process for an indefinite number of growths on both InP and GaAs substrates by use of an epitaxial protection layers. [6,19] Epitaxial protection layers eliminate the need for CMP by preserving the surface quality and removing layers with a simple non-

destructive chemical etching processes after the completion of ELO. Therefore, significant cost reduction can be achieved. We describe this universal method to create multiple batches of various thin-film InP and GaAs optoelectronic devices without systematic performance degradation by combining ND-ELO and cold-welding techniques to allow adhesive-free bonding to plastic foil substrates. Furthermore, surface and growth quality before and after wafer reuse have been comprehensively investigated using numerous analysis methods to determine the effectiveness of the method.

2.2.2 AlAs sacrificial layer etching chemistry

The ELO process leaves a degraded surface; therefore, it prevents the subsequent epitaxial growth on the original wafer. To recover the surface quality for substrate reuse, it is essential to understand the chemical reactions between the AlAs sacrificial layer and the HF etchant, and the etching productions. Initially, Yablonovitch et al. proposed a diffusion limited model to explain chemical reactions:[20]

$$2AlAs + 6H^{+} \rightarrow 2As + 2Al^{3+} + 3H_2$$

This model assumed that the out-diffused H_2 gas through the etch zone between epi and substrate limits the lateral etch rate. In contrast, Voncken et al. proposed a different chemical reaction between AlAs and HF based on the measurements by the following analysis techniques: powder X-ray diffraction, gas chromatography and nuclear magnetic resonance (NMR), etc.[21] X-ray powder diffraction analysis of solid product from the AlAs and HF reaction confirmed the presence of aluminum fluoride. To investigate the aqueous reaction product, aluminum and fluorine NMR were employed, and they revealed the presence of dissolved aluminum compounds, $[AlF_n{\cdot}(H_2O)_{6-n}]^{(3-n)+}$ with n = 0, 1, 2, 3 and $[Al\ (H_2O)_6]^{3+}$ (Fig. 2.1(a) and (b)). For the investigation

of gaseous reaction products during HF etching of AlAs, gas chromatograpy/mass spectroscopy (GC/MS) measurements were employed. Figure 2.1(c) shows the peaks of ionized forms of AsH_3 (AsH_4^+, AsH_2^+, AsH^+, and As^+) and arsenic dimers and trimers which are matched with a spectrum of arsine gas from the MOVPE reactor (Fig. 2.1(d)). In contrast, analysis of the etching reaction gas using GC/thermal conductivity detector (TCD), which is suitable for hydrogen detection, showed only 0.007 mole of hydrogen gas production per one mole of AlAs. The detected hydrogen gas is possibly contributed by either the background concentration or decomposition of AsH_3, which indicates that H_2 is neither a major etch reaction product nor the limiting factor for lateral etching in ELO process.

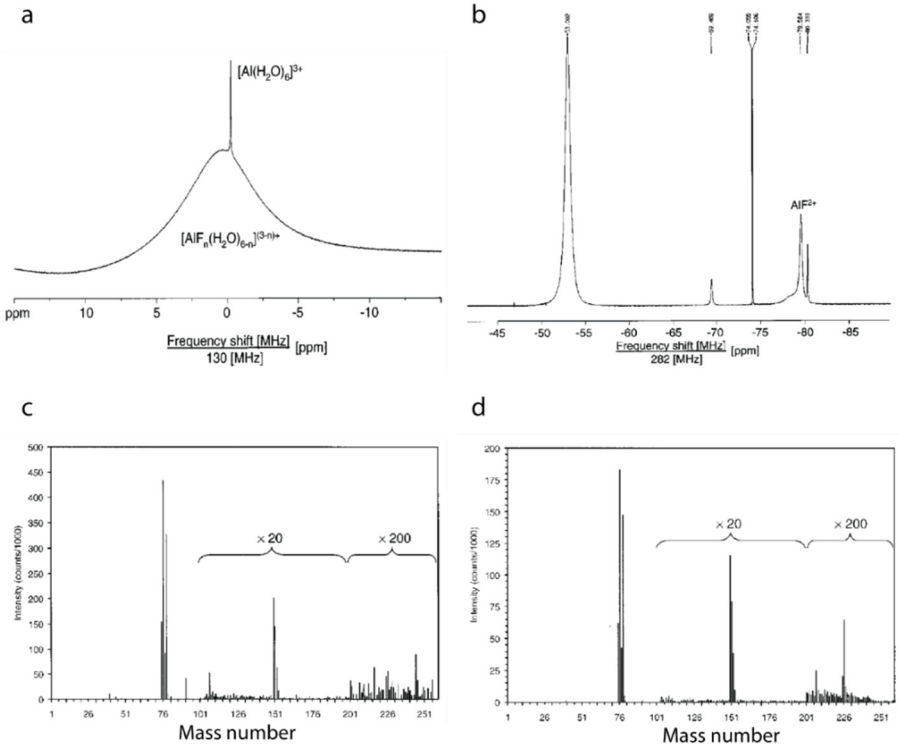


Fig. 2.1: Chemical reaction product from AlAs and HF solution reaction. (a) Aluminum NMR and (b) Fluorine NMR on the reaction products in solution. The wide peak of fig. (a) and peak at 79.6 ppm in fig. (b) are attributed to an $[AlF_n{\cdot}(H_2O)_{6-n}]^{(3-n)+}$ and AlF^{2+}, respectively. Mass spectrum (c) for the gaseous reaction products and (d) for arsine. Reproduced from ref. 23.

This proposed reaction mechanism for etching AlAs with dissociated and undissociated HF is shown in Fig 2.2, and expressed by:

$$AlAs + 3HF + 6H_2O \rightarrow AsH_3 + [AlF_n{\cdot}(H_2O)_{6-n}]^{(3-n)+} + (3-n)F^- + nH_2O$$

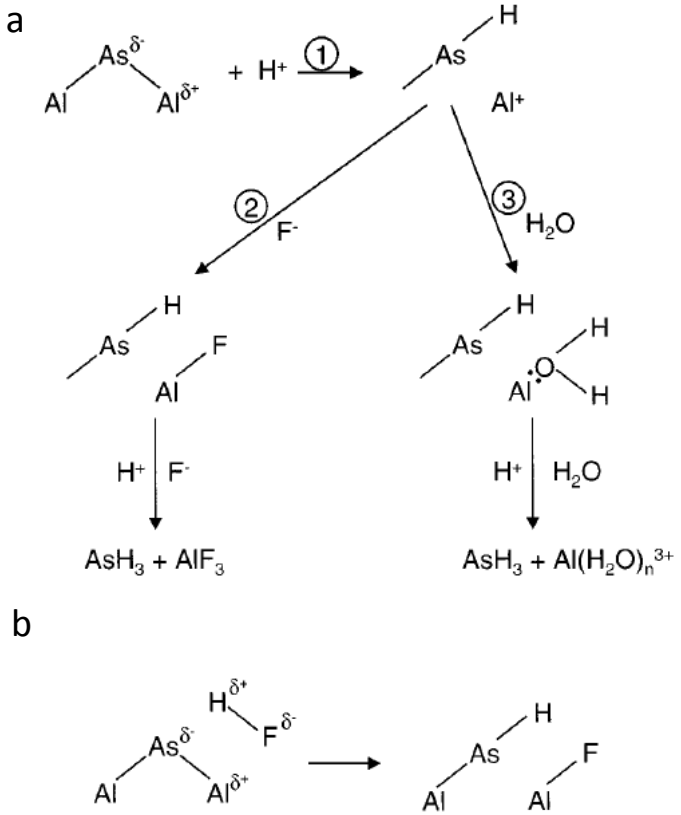


Fig. 2.2: Schematic of chemical reaction mechanism between AlAs and (a) dissociated HF or (b) undissociated HF. Reproduced from ref. 23.

As described above, this reaction model suggests that etch reaction production is the arsine and oxygen-related arsenic compounds, and the out-diffusion of hydrogen through the narrow etch opening does not limit the lateral etching rate. Moreover, it is found that the formation of an arsenic solid, or As_2O_3, is the source of substrate contamination after the ELO process, which prevents the direct recycling of substrate.[22]

2.2.3 Etch rate control factors

For practical purposes, it is essential to achieve a reasonably high etch process speed. According to the diffusion limit model[20], when the diffusion flux of gaseous reaction product from the etch interface is assumed to be the same with the etching flux, the maximum lateral etch rate is given by,

$$V_{max} = \frac{1}{3\pi\sqrt{Rt/2}}\frac{Dn}{N} \qquad (2.1)$$

where N and n are the molar concentrations of AlAs and dissolved H_2, respectively, D is the diffusion constant of gaseous reaction product, R is the radius of curvature of the film, and t is the thickness of the AlAs sacrificial layer. This model predicts the maximum lateral etch rate of approximately 3 μm/h at room temperature with a 5 cm curvature radius and 5 nm thick sacrificial layer; however, Voncken et al. claimed that the out-diffusion of gas reaction products may not be the limiting factor by experimentally showing a maximum etch rate of 3 mm/h using the WI-ELO process that can control the radius of the film curvature near the etch interface.[23]

Therefore, instead of the diffusion limited model, a reaction-rate limited model has been proposed based on the measurement of the sacrificial layer etch rate dependence on the Al fraction,[12] HF concentration[20] and the strain on the layers.[24] Eventually, a diffusion and reaction rate limit model (DR model) described by Niftrik et al. by combining the both models, suggests the etch rate is determined by both the diffusion of HF and its reaction at the etch interface.[25] According to the DR model, the etch rate V_e in mm/h is given by[25]

$$V_e = \frac{[HF]}{R_d + R_r} \qquad (2.2)$$

where [HF] is the HF concentration in M, R_d is the diffusion, and R_r is the reaction-related resistance in h·mol/mm, respectively. The model predicts a linear dependence of etch rate on the HF concentration; its validity was experimentally confirmed for [HF] < 15 mol/Kg (Fig. 2.3). The deviation from the model at higher [HF] is possibly due to the limited dissolution of the aluminum fluoride products at high concentrations.

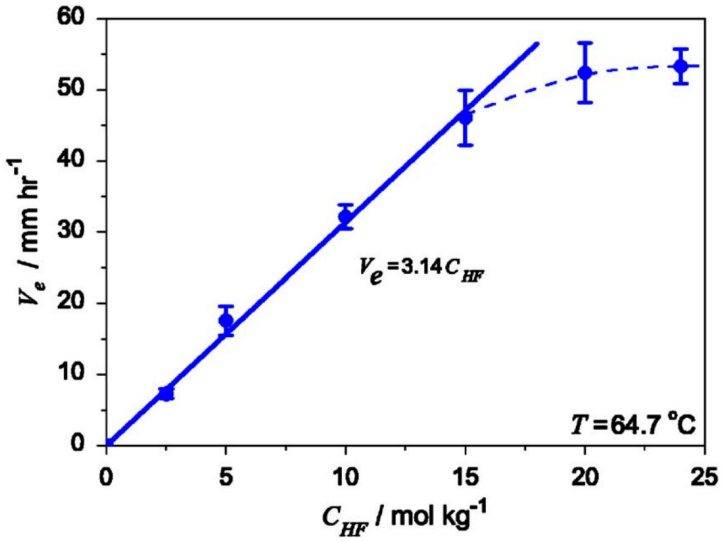


Fig. 2.3: Lateral etch rate depending on HF concentration. Solid line indicates the fitting of experimental data based on DR model. Reproduced from ref. 24.

The diffusion limited resistance R_d can be expressed as

$$R_d = \frac{\pi\sqrt{Rh}3[AlAs]}{\sqrt{2}D_o} e^{-\frac{E_{a,d}}{kT}} \qquad (2.3)$$

where R is the radius of curvature, h is the thickness of the sacrificial layer, [AlAs] is the molar concentration of solid AlAs in sacrificial layer ($Al_xGa_{(1-x)}As$ or $AlAs_{(1-y)}P_y$), D_o is the diffusion coefficient, $E_{a,d}$ is the activation energy for the HF diffusion, and T is the process temperature. To study the diffusion limited etch mechanism, the sacrificial layer thickness-dependent etch rate

were examined by the multiple release layer etch method shown in Fig. 2.4(a). Figure 2.4(b) shows a strain dependent etch rate. The $AlAs_{1-y}P_y$ sacrificial layer with y = 0.02, which minimizes strain, improves the etching rate by ~30% compared with the same thickness of sacrificial layer without phosphorus (Fig. 2.4(b)). Figure 2.4(c) shows the lateral etch rate dependence on the $AlAs_{0.98}P_{0.02}$ sacrificial layer thickness. The maximum etch rate was achieved with a ~10 nm thick sacrificial layer.

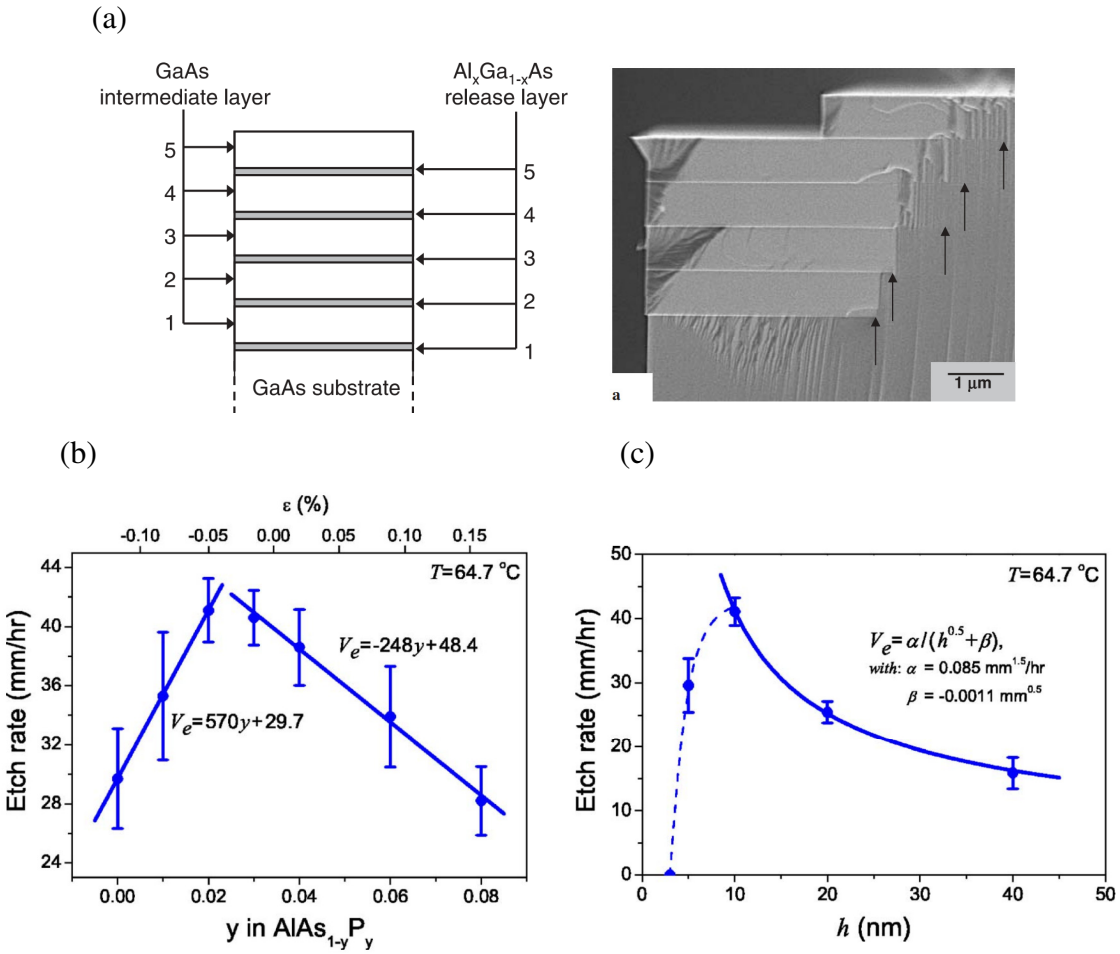


Fig. 2.4: Multi release layer etch test (a) Schematic of multi release layer etch method (left) and cross-sectional scanning electron microscope (SEM) image of sample (right). (b) Lateral etch rate depending on the strain of sacrificial layer. The strain was controlled by varying P composition. (c) Lateral etch rate depending on the sacrificial layer thickness. Reproduced from refs. 20 and 24.

The effect of the radius of curvature, R, on lateral etch rate was studied by using the WI-ELO process in Fig 2.5(a).[26] Fig 2.5(b) shows the lateral etch rate dependence on the curvature near the etch interface. The larger bending curvature assists the diffusion of HF by increasing the opening near the etch interface, and the experimental results confirm the dependency of etch rate on R.

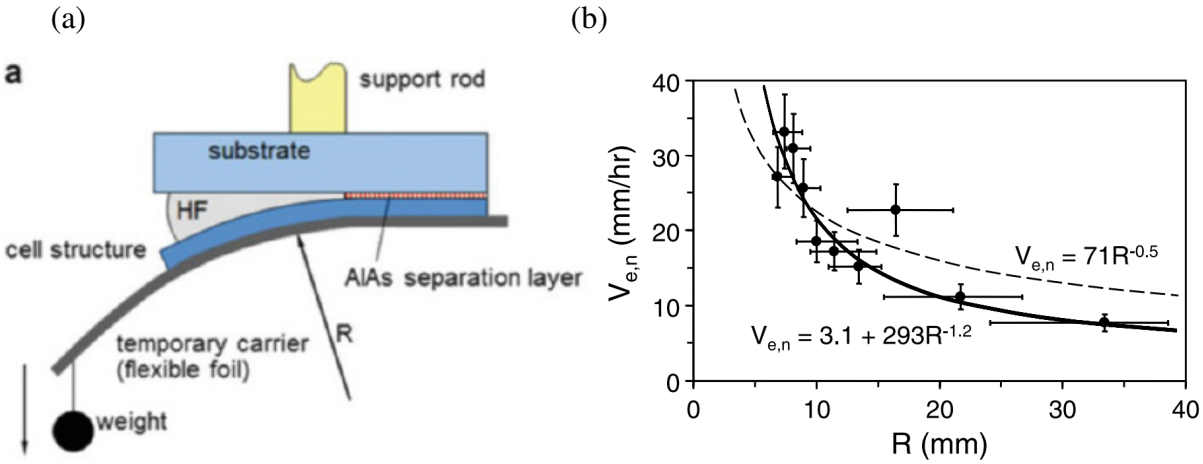


Fig. 2.5: Weight induced epitaxial lift-off (WI-ELO) process (a) Schematic illustration of WI-ELO process (b) Lateral etch rate depending on the curvature near the etch interface. Reproduced from ref. 7 and 26.

The reaction limited resistance R_r can be expressed as

$$R_r = \frac{1}{A} e^{-\frac{E_{a,r}}{kT}} \qquad (2.4)$$

where A is the Arrhenius constant and $E_{a,r}$ is the activation energy associated with the reaction barrier. The reaction limited etch rate can be confirmed by the dependence on Al fraction in the $Al_{(1-x)}Ga_xAs$ sacrificial layer (when x is < 0.4) and the dependence on the etch process temperature. Figure 2.6 shows the lateral etch rate dependence on the Al composition of the AlGaAs sacrificial layer.

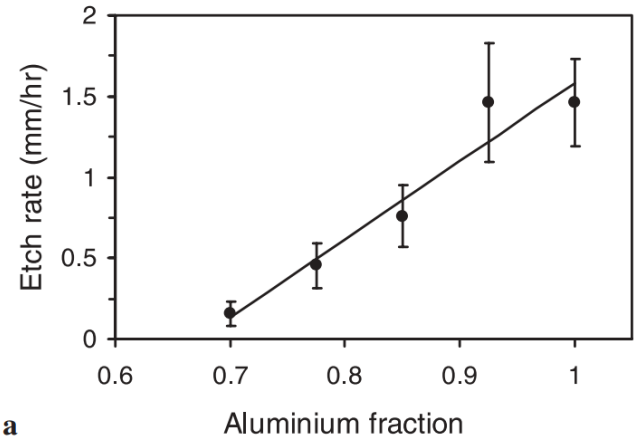


Fig. 2.6: Lateral etch rate depending on the Al composition of AlGaAs sacrificial layer. Reproduced from ref. 20.

Since both the reaction and diffusion process is affected by temperature, the DR model can be reduced to:

$$V_e = V_{e,0} e^{-\frac{E_a}{kT}} \qquad (2.5)$$

Figure 2.7 shows the etch rate depending on the process temperature for a sacrificial layer thickness of 10 nm. A lateral etch rate of > 40 mm/h is achievable at T = 70 °C.

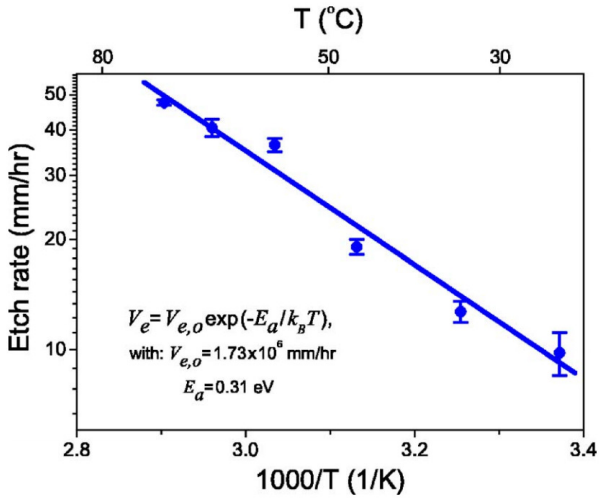


Fig. 2.7: Lateral etch rate depending on the process temperature. Reproduced from ref. 24.

Based on systematic research of the key parameters for lateral etch rate described above, an advanced WI-ELO process was developed that employed a guiding cylinder instead of applying a weight to the flexible carrier (Fig. 2.8(a)).[26] Previous WI-ELO process had the disadvantage that the flexible carrier bends too greatly, thus it resulted in cracking of the thin-film (Fig. 2.5(a)). In contrast, the advanced WI-ELO process can apply a constant radius of curvature near the etch interface by using a guiding cylinder with fixed radius. This process generally provides lateral etch rates exceeding 30 mm/h without creating cracks in the lifted-off epitaxial thin-film (Fig. 2.8(b)).

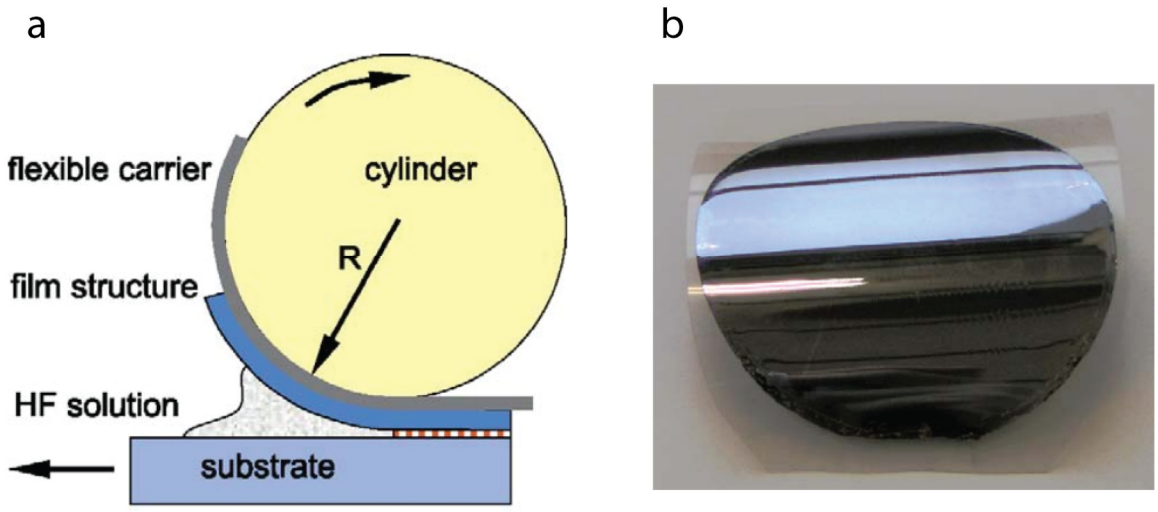


Fig. 2.8: Advanced WI-ELO process. (a) Schematic illustration of ELO set-up with a guiding cylinder that applies a stabilized radius of curvature near the etch interface. (b) Photograph of lifted-off 2" GaAs thin-film on a flexible plastic carrier via WI-ELO process. Reproduced from ref. 26.

2.3 Overview of thin-film bonding technology

Bonding is a process that joins two separate materials together into a single body. Thin-film bonding is an essential process to fabricate thin-film optoelectronic devices on a host substrate. However, conventional fusion-process based bonding technologies are difficult to employ for thin-

film lift-off processes mainly due to their high processing temperature exceeding the glass transition temperatures of the host substrate, or creating a strain to the thin-film due to mismatch of thermal expansion coefficients. In this section, we introduce various bonding technologies that can be employed for thin-film active layer transfer from the original parent substrate onto the permanent or temporary host substrate.

2.3.1 Cold-weld bonding

Cold-welding is the bonding process that forms an intimate metallic junction by bringing two clean metal surfaces into contact with an application of pressure.[27,28] This process is one of the oldest bonding techniques that was used by Mycenaean civilization mostly for decoration of metal products since the 2nd or 1st millennium B.C.[29] Figure 2.9 shows a photograph of a bronze dagger blade with cold-welded Au and Ag decoration from Mycena, Greece.[30] This ancient process used a shock pressure via hammering to join a malleable metal to a hard metal by reconstructing the interface by forming a metallic bond between them.

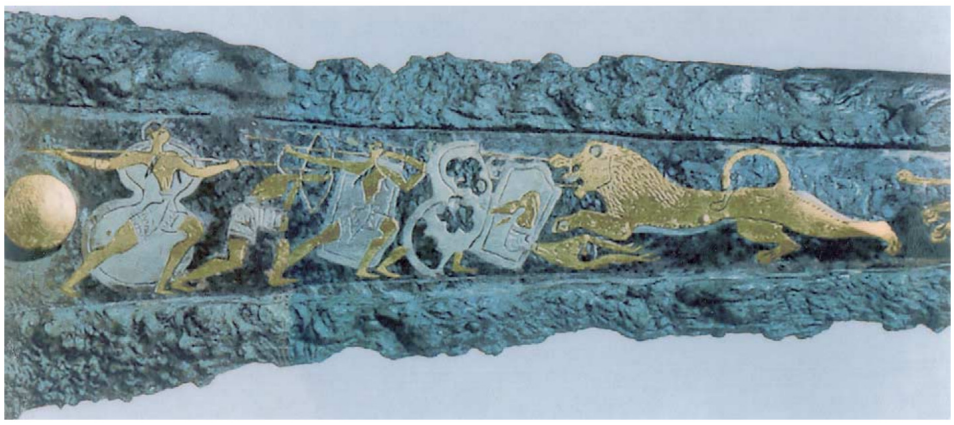


Fig. 2.9: Photograph of ancient cold-welding processed decoration. Cold-welded Au and Ag onto bronze blade. Reproduced from ref. 30.

More recent research showed that two interfaces can form an intimate metallic bond when the spacing between atomically flat surfaces falls below a critical thickness (Fig. 2.10).[31] For Ni (100), it is shown that two surfaces cannot be held apart when the interfacial separation is below 1.9 Å, which is slightly larger than bulk interatomic spacing.[31] Bonding can be achieved within 100 fs under ambient conditions by applying considerable pressure across the two interfaces to overcome surface imperfections such as oxide films and desorbed contaminants.[31] Ferguson et al. demonstrated the cold-welding of Au-Au interface using very low force (on the order of μN) applied by elastomeric supports in the presence of air, humidity and volatile organic contaminants.[28]

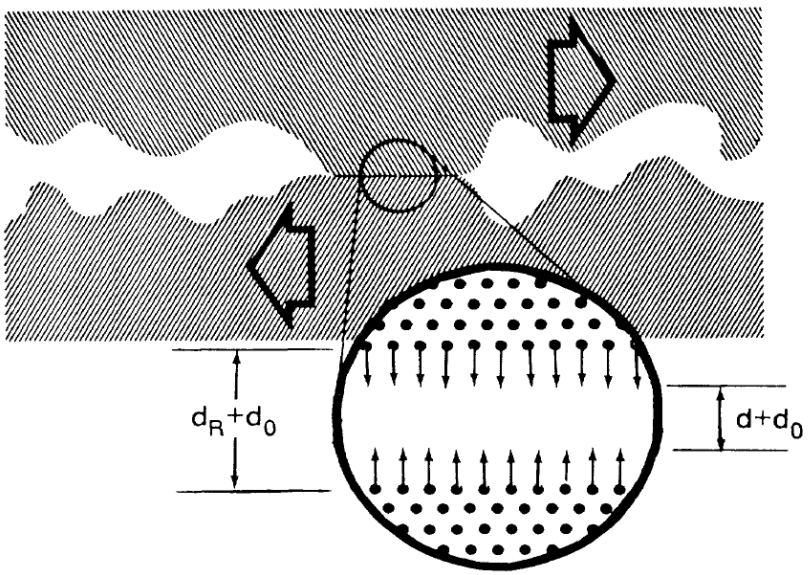


Fig. 2.10: Schematic of cold-welding process. When the interfacial separation is below the critical thickness, two metallic surface can collapse together. Reproduced from ref. 31.

The cold-weld bonding technique is especially helpful when it is combined with an ELO process by eliminating additional thin-film transferring processes. Thin-film optoelectronic devices such as solar cells, photodiodes and LEDs usually require a rear-side metal contact which

can be used as a bonding interface to directly transfer the thin-film to the permanent host substrate such as a plastic substrate coated with metal.

2.3.2 Van der Waals bonding

Van der Waals bonding can be achieved between two surfaces by using attractive intermolecular forces that are relatively weak compared to covalent or metallic bonds. Yablonovitch et al., demonstrated van der Waals bonding of ELO processed thin-film GaAs epi-layers onto arbitrary substrates.[13] Figure 2.11(a) and (b) show a schematic of the bonding process and cross-sectional transmission electron microscope image of a bonded interface. A de-ionized water droplet left after rinsing pulls the lifted-off thin-film down onto the substrate by natural intermolecular surface forces. Then, the trapped wafer is squeezed out by applying pressure (~1.5× 10^4 dynes/mm^2). Subsequently, the thin-film is baked under vacuum at 250 ℃ to dehydrate the dust particles.

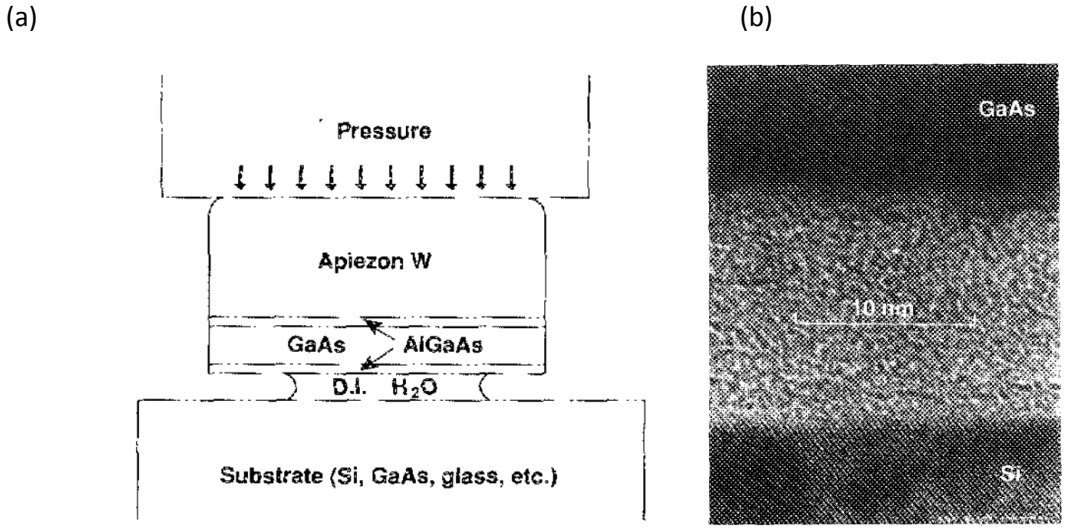


Fig. 2.11: Van der Waals bonding process. (a) Schematic illustration of van der waals bonding of ELO processed film to the arbitrary substrate. (b) Cross-sectional transmission electron microscope image of bonded interface. Reproduced from ref. 13.

Van der Waals bonding is a simple, adhesive free, low-temperature electrostatic process like cold-welding; however, this process is generally employed after the ELO process to bond the already lifted-off thin-film onto the permanent substrate. Therefore, it requires an additional processing step to attach a handle to the epi-layer that holds the thin-film during the ELO process, usually using black wax, which is a mixture of hydrocarbons. Moreover, there is a risk of film damage during post fabrication processing such as plasma etching, due to the relatively weak bonding between the lifted-off film and the substrate.

2.3.3 Additional bonding and transferring techniques

Yoon et al., demonstrated bonding of ELO processed thin-film epi-layers onto a partially cured polyimide-coated substrate via transfer printing.[8] Transfer printing is enabled by using the kinetically controlled adhesion of thin-film layers to an elastomeric stamp.[32] The bonding between thin-film and stamp is dominated by van der Waals interactions, and it is rate-sensitive adhesion owing to the viscoelastic behavior of the elastomer stamp.[32] Therefore, sufficiently high peel velocity (> 10 cm/s) results in separation of the thin-film from the substrate and adhererence to the stamp. In contrast, enough slow peel velocity (~1 mm/s) allows the thin-film to adhere to the host substrate and become separated from the stamp. Figure 2.12 shows a schematic illustration of the transfer printing process. Transfer printing includes spin coating and photolithography to form a small photoresist structure to tether the undercut etched thin-film onto the donor substrate to hold the lifted-off film in position. A polydimenthylsiloxane (PDMS) stamp is used to lift-off and transfer print the thin-film epi-layer onto a substrate coated with partially cured polyimide, followed by baking.

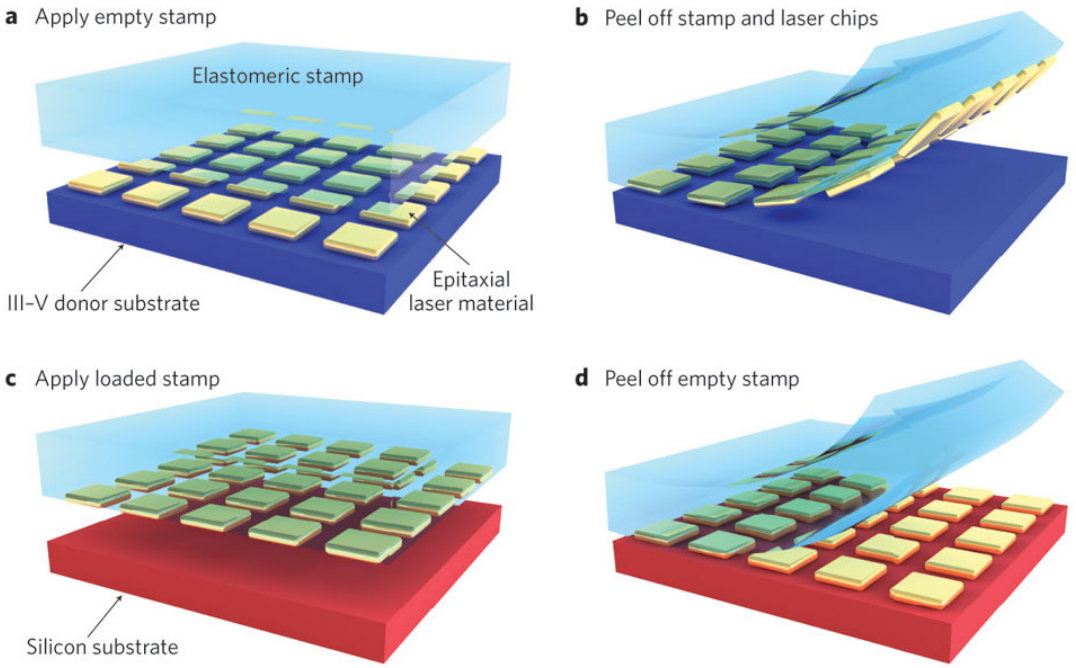


Fig. 2.12: Schematic illustration of transfer printing process.[35] The elastomeric stamp is used to pick up the lifted-off thin-film layers and transfer them to the host substrate. Reproduced from ref. 32.

Moreover, transferring using sticky tape was demonstrated by Lee et al.[33], and Cheng et al.[34] Thermally releasable tape was used as a temporary carrier[33], and Kapton tape that is durable to vacuum processes was employed as a permanent host substrate[34].

Most bonding processes of a thin-film onto a permanent substrate described above except the cold-welding process require some form of transfer process. Black wax (Apiezon W) can be employed as a handle layer during the ELO process since tension can be induced by annealing to create curvature near the etch interface that assists in HF diffusion into the gap between epi and substrate. Thermal release tape can also be used as a temporary handle to support the thin-film and is then removed after bonding the epi-layer onto the host substrate by weakening the adhesion with the application of heat.[33]

2.4 Advantage of thin-film optoelectronic devices

2.4.1 Light trapping

The original concept of light trapping was proposed for Si photodetectors to increase its response speed while maintaining high EQE in the NIR range via total internal reflection.[9,36] Subsequently, light trapping structures with a textured back-side mirror was employed for Si photovoltaic cells to overcome weak absorption of light.[37] The ideal light trapping structure with sufficiently textured surface and a perfect rear-side mirror provides a degree of intensity enhancement of $2n^2$ via total internal reflection.[9] In other words, a light ray in thin-film with refractive index of $n = 3.5$ can make ~25 passes within the absorbing layer using a light trapping structure before escaping. Therefore, the maximum effective absorption enhancement factor of light trapping is ~$4n^2$ by considering an angular average of the longer path length of oblique rays.[9] Figure 2.13 shows a schematic illustration of the light trapping structure that increases the number and length of absorption paths using total internal reflection compared to a film without a rear-side mirror or textured surface. A similar concept using integrated back side metal mirrors instead of a textured surface has been widely employed for various thin-film solar cell technologies including organic solar cells, and solar cells with a low absorption coefficient or short photogenerated carrier lifetime to enhance light absorption by increasing the optical path.

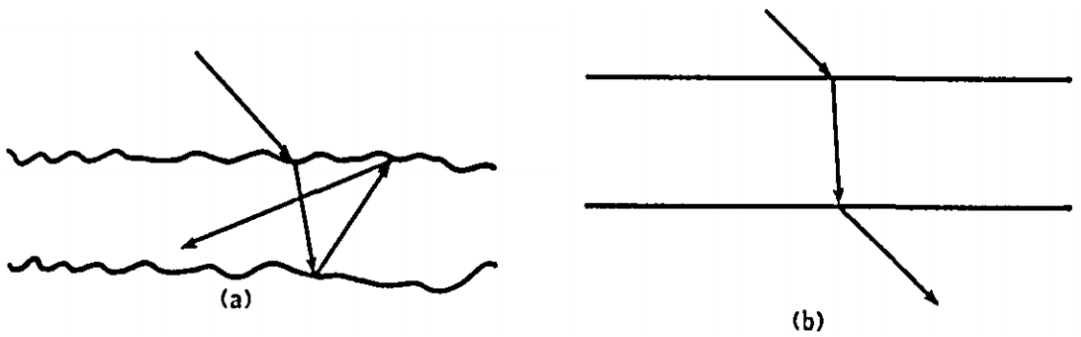


Fig. 2.13: The schematic illustration of light absorption in thin-film. (a) The light trapping structure using textured surface. (b) The thin-film without light trapping structure. Reproduced from ref. 9.

However, the light trapping concept for compound semiconductor-based photovoltaic cells was paid relatively small attention compared with Si-based photovoltaic cells because their absorption coefficient is sufficiently high to fully cover the solar spectrum below the band edge using a thin active layer (few μm). Furthermore, application of a rear-surface mirror in compound semiconductor devices faces structural limitations since the device is usually grown on a crystalline wafer. However, the ELO process enables replacing a bulk substrate with a reflector-coated epitaxial layer by transferring only a thin active region onto it. A light trapping structure with back-side mirror doubles the optical path by reflecting the incident photon back into the absorbing region; therefore, the active layer thickness can be reduced by half, which reduces the consumption of costly materials and growth time without performance loss.[14,26] The high refractive indices of compound semiconductors create a narrow escape cone near the surface for trapped or internally generated photons, therefore light trapping effects can be enhanced.[11]

There is a synergy especially for photovoltaic cells both with improvement in absorption, and also in open circuit voltage (V_{oc}) when light trapping is combined with photon recycling which will be discussed in the following section.[38] The light trapping structure effectively

confines internally generated photons via a radiative recombination process within the active device region, which eventually results in photon recycling. Moreover, the thin active region achieved by light trapping reduces bulk recombination losses. However, rear surface recombination is increased when generation near the surface becomes significant. Therefore, it is important to have a back surface field (BSF) layer with a high quality interface. Furthermore, bulk resistivity losses can be reduced since the photogenerated carrier density increases by using a reflective back side mirror, which in turn increases the conductivity.

Light trapping using a rear-side metal mirror is also effective for photodiode applications as originally suggested. The rear-side mirror that doubles the absorption path is especially useful for the NIR/IR range detection where the penetration depth is longer than the visible spectrum range. Therefore, the relatively thinner active layer in a photodetector can be employed, combined with a rear-side mirror to achieve enhanced absorption. The thinner active region also provides a fast response speed which is a figure of merit of a photodiode.

Furthermore, combination of a light trapping structure using a rear-side mirror with surface texturing enhances the external quantum efficiency (EQE) of LEDs by preventing the absorption loss of internally generated photons through the substrate.[39]

2.4.2 Photon recycling

Photon recycling is the self-absorption process of internally generated photons. This effect is especially advantageous for III-V photovoltaic cells that have a very high internal quantum efficiency to improve the power conversion efficiency (*PCE*) by increasing V_{oc}. Since 1950s, numerous researchers have described the effects of self-absorption of spontaneously emitted photons on the measured values of the minority carrier lifetime and diffusion length in GaAs

compared with absolute values.[10,40,41] The photoluminescence lifetime of a GaAs/AlGaAs double-heterojunction structure (τ_{PL}) can be written as:[10]

$$\frac{1}{\tau_{PL}} = \frac{1}{\tau_{nr}} + \frac{1}{\varphi\tau_r} + \frac{1}{\tau_s} \qquad (2.6)$$

where τ_{nr} is the carrier lifetime due to nonradiative recombination processes, τ_r is the radiative lifetime, τ_s is the surface recombination lifetime, and φ is a photon recycling factor. This model is used to explain why the carrier lifetime (τ_{PL}) extracted from transient photoluminescence (TRPL) is longer than calculation. Moreover, the photon recycling model predicts the dependence of φ on active region thickness due to self-absorption. TRPL measurements confirm the increased lifetime as active layer thickness increases, and the PL radiative lifetime approaches the radiative lifetime when *d* was sufficiently thin (Fig. 2.14).

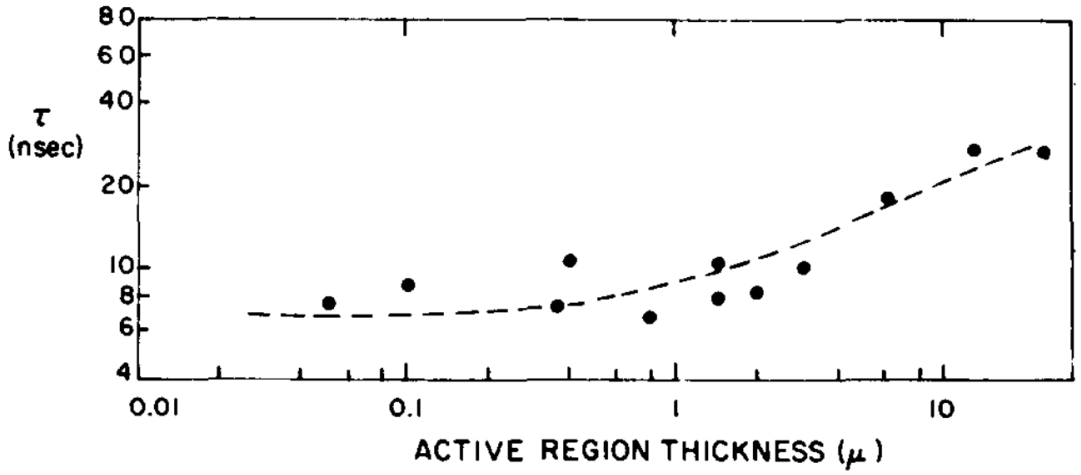


Fig. 2.14: Recombination lifetime *vs.* active layer thickness. The dots represents experimental data, and the dashed curve is the theoretical values. Reproduced from ref. 10.

Photon recycling was designed into GaAs-based semiconductor lasers to reduce a threshold current density in 1974 by Stern et al.[42] In their system, reabsorption of spontaneously

emitted photon with energy exceeding the bandgap decreased the externally supplied current density required to reach a given gain at room temperature. Later, Ahrenkiel et al. confirmed photon recycling by showing that the bulk minority-carrier lifetime in 1×10^{17} cm^{-3} doped GaAs provides ~5 times longer radiative lifetime than the calculation.[43] This effect was only detected for a sample with a high quality AlGaAs/GaAs interface grown at > 740 ℃.

In 1991, Lush et al. proposed the thin-film approach for III-V photovoltaic cells to improve efficiency by combining light trapping and photon recycling using a back-side mirror (Fig. 2.15).[44]

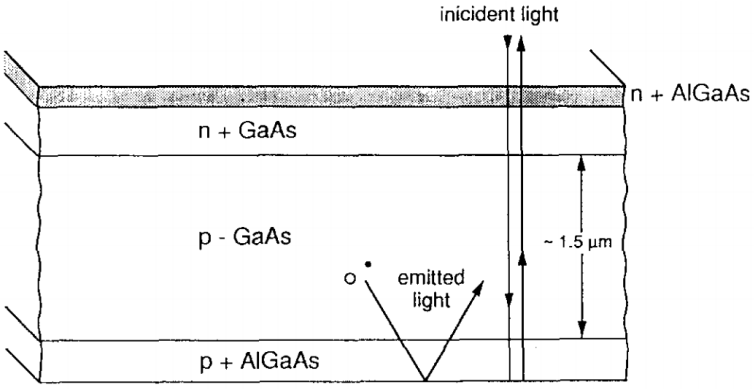


Fig. 2.15: GaAs solar cell structure for enhanced photon recycling. Reproduced from ref. 44.

According to the photon recycling model, when the dark current is dominated by recombination within the base layer of solar cell, the saturation current density(J_0) of a thin-film cell is approximated by:[44]

$$J_0 = q\frac{n_i^2}{N_A}W[\frac{1}{\tau_{nr}} + \frac{1}{\varphi\tau_r} + \frac{S}{W}] \qquad (2.7)$$

where W is width of the base layer, N_A is the base doping concentration, n_i is the intrinsic carrier density, and S is the back-surface recombination velocity. Photon recycling factors of ~10 leads to $J_0 = 2 \times 10^{-21}$ A/cm^2, based on a simplified relationship between V_{oc} and J_0 given by:

$$V_{oc} \approx \frac{kT}{q} \ln\left(\frac{J_{sc}}{J_0}\right) \qquad (2.8)$$

Using a reasonably high J_{sc} = 29 mA/cm^2, V_{oc} = ~1.15 V for thin-film GaAs solar cell is expected. Base on the thin-film approach, the enhanced photon recycling achieved by a light trapping structure was experimentally demonstrated by Lundstrom et al. using the substrate etch removal method.[45] This structure enables the reflection of spontaneously emitted photons into the active layer that was not considered in earlier calculations[10]. Therefore, the extremely long carrier lifetime (~1μs) in moderately doped GaAs thin-films via photon recycling and light trapping was achieved, showing the potential of a high efficiency GaAs solar cell using thin-film solar cell designs (Fig. 2.16(a) and (b)).

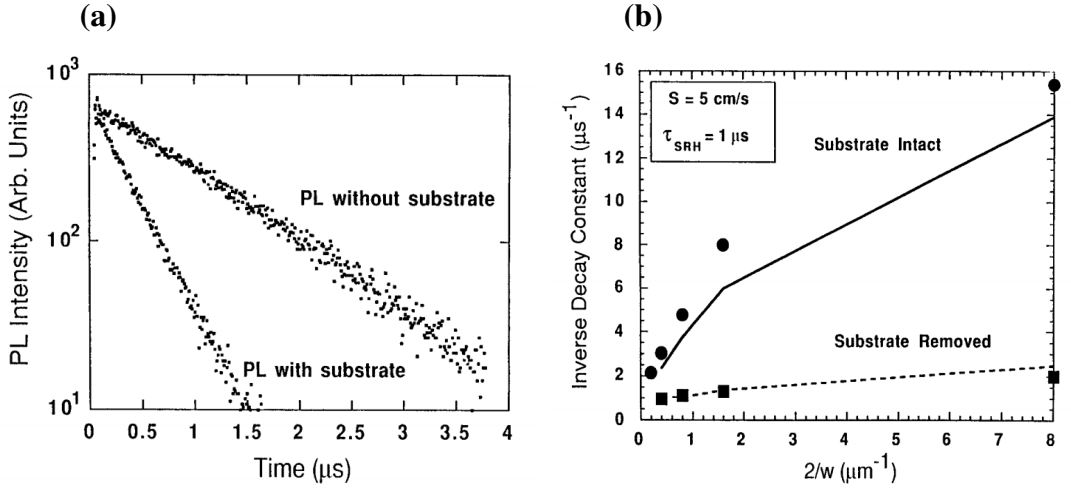


Fig. 2.16: Effect of substrate removal on minority carrier lifetime. (a) TRPL measurement on GaAs/AlGaAs thin film with and without substrate. (b) Inverse decay constant extracted from TRPL measurement dependence on active layer thickness. Reproduced from ref. 45.

Alta Devices employed photon recycling combined with light trapping by using the ELO process. Their solar cell provided a very high efficiency (28.8 %). The short circuit current density (J_{sc}) was similar between thin-film and substrate-based cells, however, there was a significant improvement in V_{oc} using a thin-film solar cell design with a back-side reflector as predicted. The probability of radiatively recombined photons within the GaAs active cell region escaping the front surface before reabsorption is only 1~2%, and over 96 % of internal luminescence can be re-absorbed using the back side mirror with high reflectance (Fig 2.17).[11]

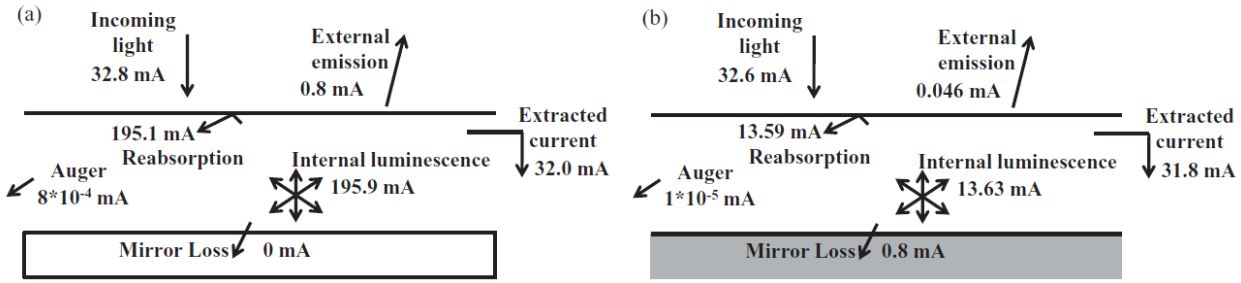


Fig. 2.17: Diagram of current at the operating point of photovoltaic cell (a) with a perfect mirror and (b) with an absorbing substrate. Both cells provide a comparable current, however, the significant incensement of internal luminescence via perfect mirror results in the improved V_{oc}. Reproduced from ref. 11.

Indeed, Alta Devices' GaAs thin-film solar cell showed a very low saturation current density of 6×10^{-21} A/cm^2, approximated by a two diode model. Estimated V_{oc} = 1.107 V based on Equation 2.8 matched with the measured value (V_{oc} = 1.107 V) by the National Renewable Energy Laboratory (NREL). Figure 2.18(a) and (b) shows the dark current density characteristic of the thin-film GaAs solar cell and its fit using the double diode model.

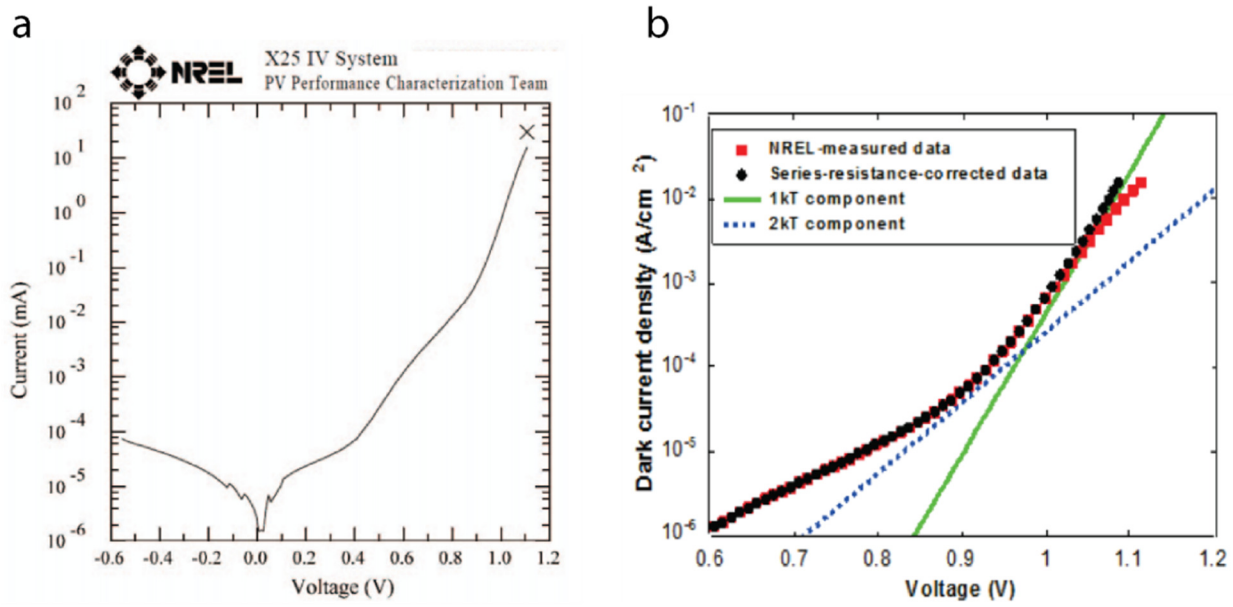


Fig. 2.18: Dark current density of Alta Devices' thin-film GaAs solar cells (a) measured by NREL and (b) fitted by double diode model. Reproduced from ref. 15.

Photon recycling can be further improved by combining a narrow band angle restrictor, such as a dielectric multilayer[46] or a double array of cone-like structures[47] on the cell. A double array of cone-like structures provides high transmission for normally incident light, but has a high reflectivity at oblique angles at the wavelength range of radiative recombination (Fig 2.19(a)-(d)).[47] Recently, there was an effort to enhance the photon recycling in thin-film multi-junction solar cells by confining the internal luminescence within the sub-cells using a low refractive index material such as an air gap between the cells instead of luminescence coupling into the adjacent cell.[48]

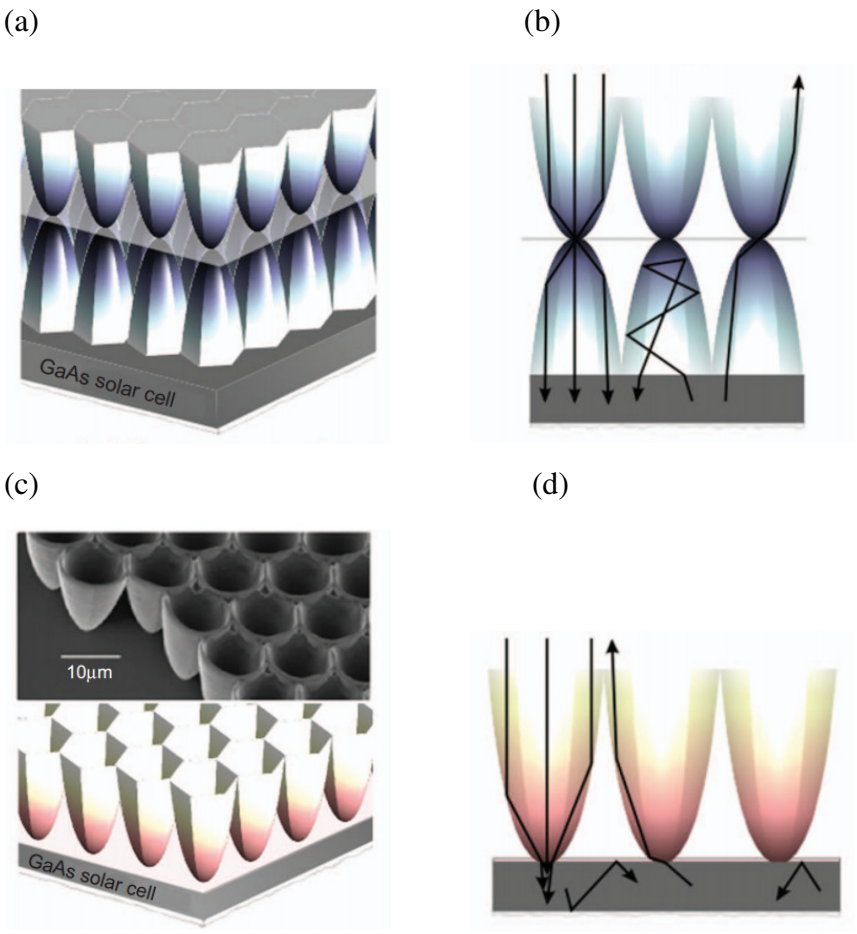


Fig. 2.19: Schematic illustration for a coupler structure enhancing photon recycling (a) Dielectric coupler consists of a double array of cone-like structures. The cone-like structures have a light trapping, randomizing back reflector. (b) Illustration of rays in a dielectric coupler structure in fig 2.19(a). (c) Schematic of a metal array coupler combined with GaAs solar cells. (d) Illustration of rays in metal array coupler structure in fig 2.19(c). Reproduced from ref. 47.

2.5 Advanced thin-film optoelectronic devices

2.5.1 Photovoltaic cells

Initially, the ELO process was developed to reduce the production cost of photovoltaic cells by recycling the wafer. The first ELO processed device was ~30 μm thick *n*-AlGaAs/*p*-GaAs hetrojunction thin-film solar cells with *PCE* of 13.5 % under the 1 sun illumination, and *PCE* =

9.4 % under the 109 suns concentrated condition.[1] The second ELO processed photovoltaic cells were demonstrated almost two decades after in 1996 by Lee at al. and Hageman at al. (Fig. 2.20(a)-(d)) However, their cells were small (1 mm × 1 mm size, Lee at al.[49]) or showed poor performance (*PCE* = 9.9 %, Hageman et al.[50]) due to an immature fabrication processes.

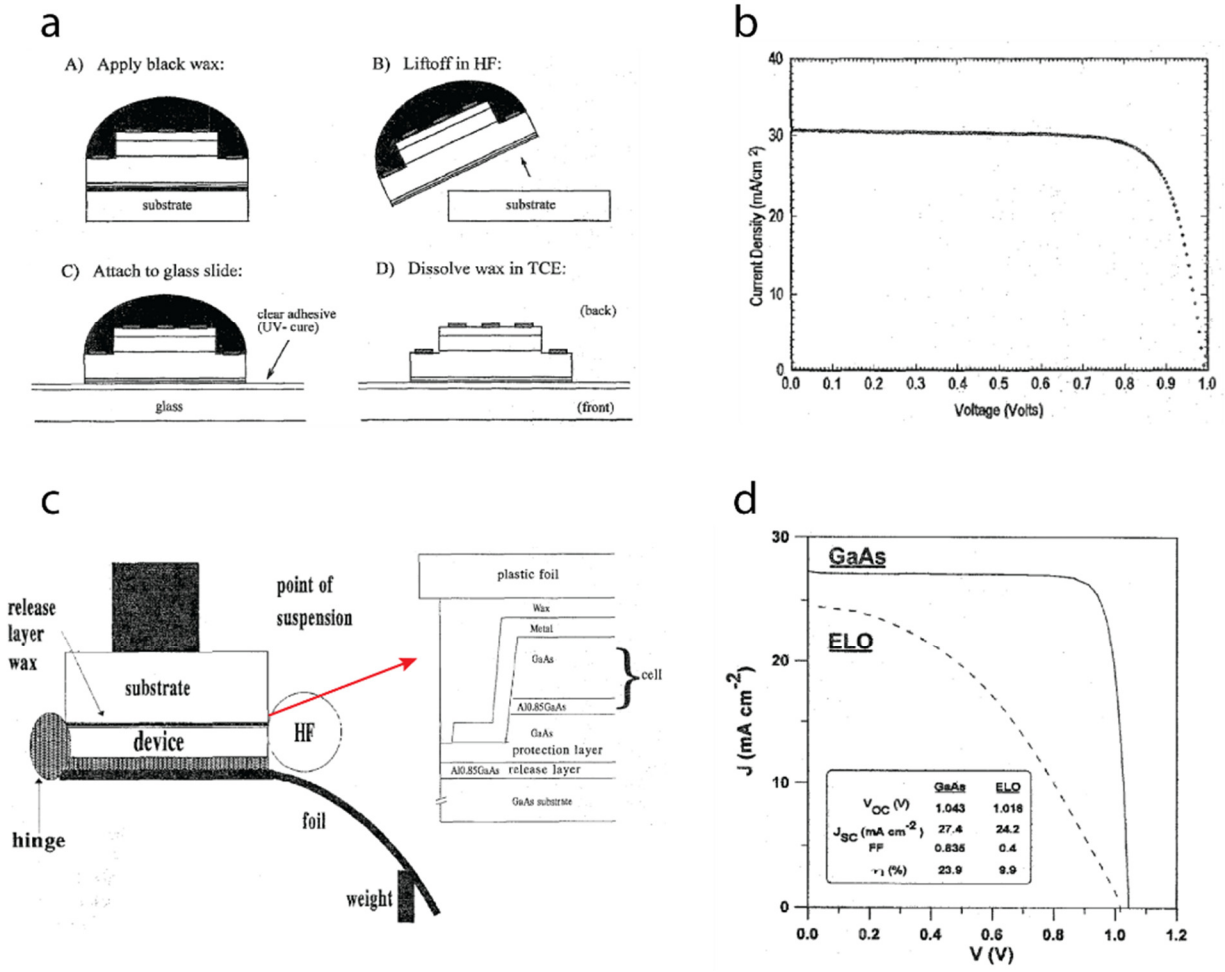


Fig. 2.20: ELO processed GaAs thin-film solar cells. (a) ELO process using black wax. Photovoltaic cells were first fabricated, then transferred onto glass substrate. (b) *J-V* characteristic under 1 sun (simultated AM1.0) illumination. (c) Schematic of WI-ELO process, and device structure for it. (d) *J-V* characteristic comparison between ELO cell and substrate cell under 1 sun illumination. Inset: Summary of device performances. Reproduced from ref. 49 and 50.

It took another decade to achieve *PCE* comparable to substrate-based GaAs solar cells. Eventually, the record efficiency of 26.1 % for a single junction GaAs solar cell was achieved using the ELO process by Bauhuis et al. in 2009.[14] The *PCE* of ELO-processed GaAs solar cells was further improved by Alta Devices (*PCE* = 28.8 %, in 2011[15]), and, remains the record efficiency among all single junction photovoltaic material systems to date, including mono-crystalline Si solar cells.[51] Figure 2.21 shows a *J-V* and EQE characteristic of Alta Devices' GaAs thin-film solar cells.[15]

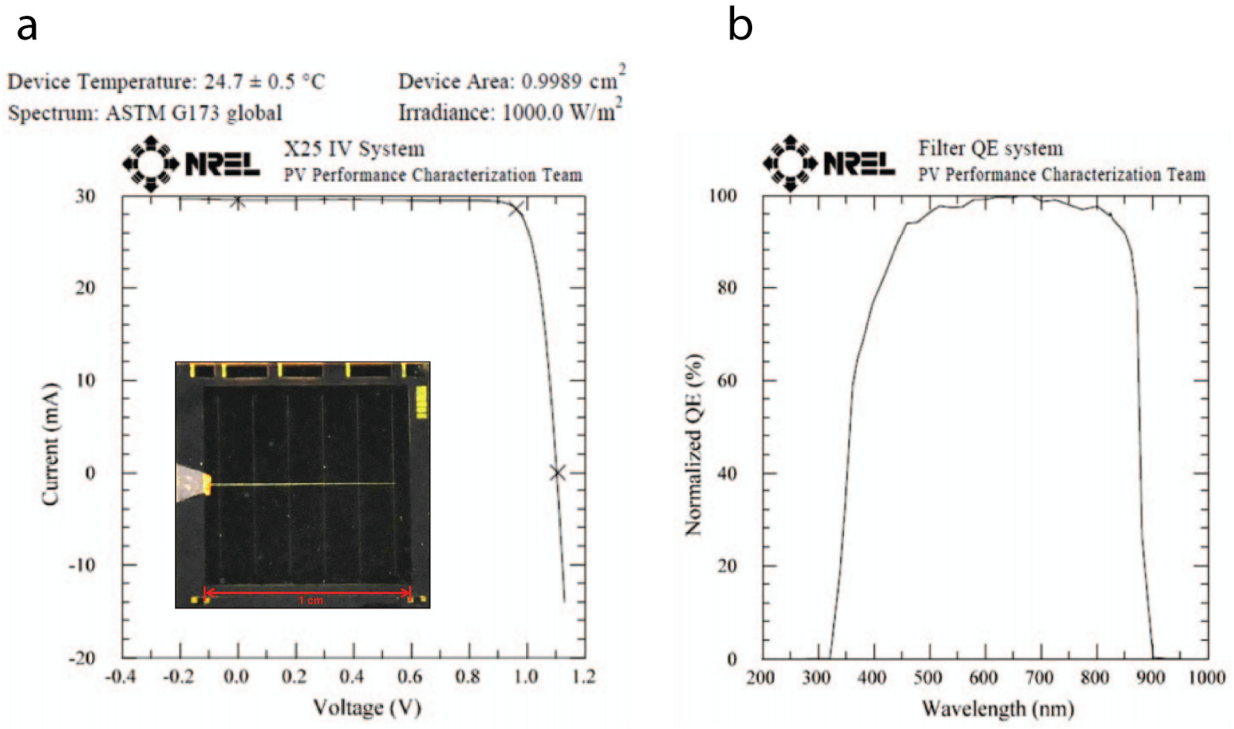


Fig. 2.21: Characteristic of Alta Devices' GaAs thin film solar cell certified by NREL (a) *J-V* characteristic under simulated AM1.5G 1 sun illumination. Inset: Photograph of device. (b) EQE of solar cell. Reproduced from ref. 15.

The improved performance of thin-film GaAs solar cells is mainly maintained by the high open circuit voltage (V_{oc}) compared to substrate-based solar cells, enabled by a rear-surface mirror

with high reflectivity immediately underneath the active solar cell region. The back-surface mirror provides two very important benefits of light trapping and photon recycling which was discussed above. As a result of these advantageous effects, the V_{oc} of the best thin-film GaAs solar cell reaches 1.11 eV which is considerably higher than that of the best substrate-based GaAs solar cells (V_{oc} = 1.03 eV) with similar structure. Furthermore, the ELO-processed thin-film GaAs solar cells provide numerous advantages over substrate-based solar cells such as lightweight, flexibility, reduced use of active materials and decreased growth time (only requiring a half thickness of absorption layer compared to bulk solar cells by having a mirror on the bottom of cell), effective heat management, and potential for wafer recycling, etc.

Moreover, ELO techniques can also be applied for multi-junction solar cell fabrication. The multi-junction solar cells are especially attractive for concentrated photovoltaic and space-borne applications mainly due to their high *PCE*. Recently, double and triple junction solar cells have been demonstrated using the ELO process (Fig. 2.22).[52,53] The quadruple junction solar cell was also demonstrated by mechanically stacking the lattice mismatched sub-cells and employing an index matched interlayer between sub-cells.[54] Furthermore, there have been attempts to improve the performance of multi-junction solar cells by converting luminescence coupling into a photon recycling effect.[48,55] This is possible by inserting a wavelength selection mirror between each sub-cell to confine the radiatively recombined photons inside each sub-cell region instead of being coupled to adjacent cells by using ELO.[48,55]

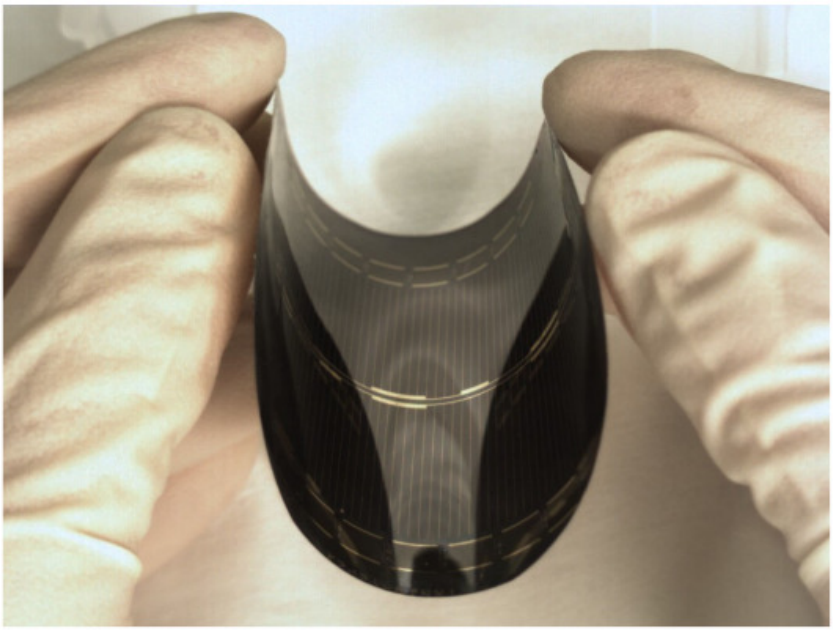


Fig. 2.22: Picture of ELO processed InGaP/GaAs double junction photovoltaic cells from 4 inch substrate. Reproduced from ref. 52.

2.5.2 Photodiodes

The working principle of photodiodes is similar to photovoltaic cells; however, it is designed to detect the optical signal instead of harvesting energy, therefore, it operates under reverse bias. The first demonstration of an ELO-processed photodetector was bottom illuminated InP/InGaAs *p-i-n* photodiode on a sapphire substrate in 1989 by Schumacher et al.[56] The devices were fabricated on top of the InP substrate, then the fabricated devices were transferred to a sapphire substrate. The ELO processed InGaAs *p-i-n* photodiode had a bandwidth of 13.5 GHz with a 90 % internal quantum efficiency at a wavelength of 1.3 μm. The device was a bottom illumination structure. Figure 2.23(a) and (b) show a schematic of device structure and measured pulse response of an ELO processed InGaAs *p-i-n* photodiode.

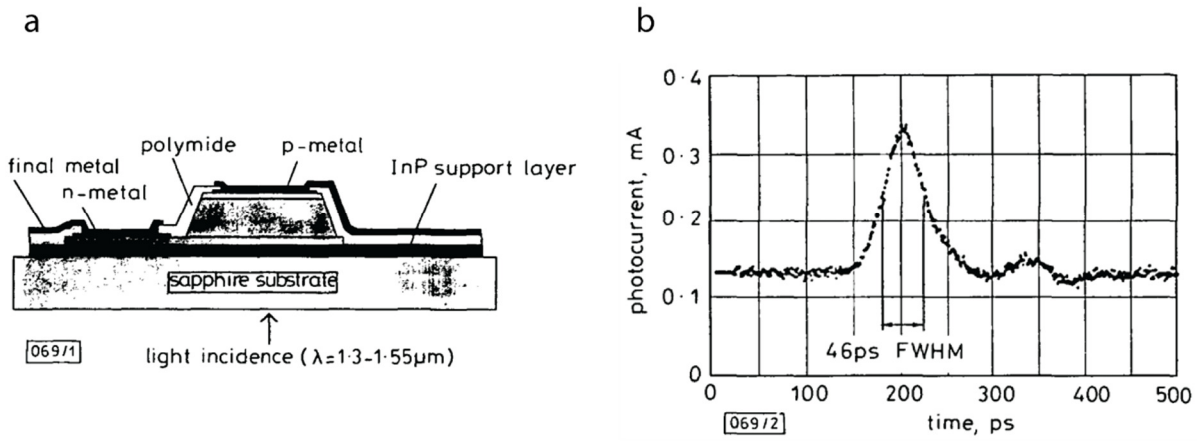


Fig. 2.23: ELO processed InGaAs *p-i-n* photodiode. (a) Schematic cross-section of fabricated device structure and (b) Pulse response of InGaAs *p-i-n* photodiode. Measurement shows 46 ps FWHM, and THE estimated intrinsic impulse response was 23 ps FWHM. Reproduced from ref. 56.

To further improve the performance of a photodetector using a resonant cavity, Yang et al. demonstrated the fabrication of an InGaAs *p-i-n* photodiode on top of an AlAs/GaAs *distributed Bragg reflector* (DBR) with maximum reflectivity at 1.3 μm.[57] However, their demonstration was limited to the fabrication and dark current measurement of a photodiode without characterizing the EQE and response speed even though those parameters are benefitted by employing a resonant cavity structure. The measured dark current was 4.4 nA at -0.5 V with a very small breakdown voltage (approximately -1 V).

For the GaAs-based photodetector, Au/GaAs Schottky photodiode was transferred to a glass substrate via ELO by Kobayashi et al.[58] An external quantum efficiency over 70% was demonstrated at a wavelength of 780 nm, which is 1.6 times higher than that of a conventional substrate-based photodiode (Fig. 2.24). Enhanced absorption was achieved by substrate-side illumination through the glass and light trapping using Au front contact mirror.

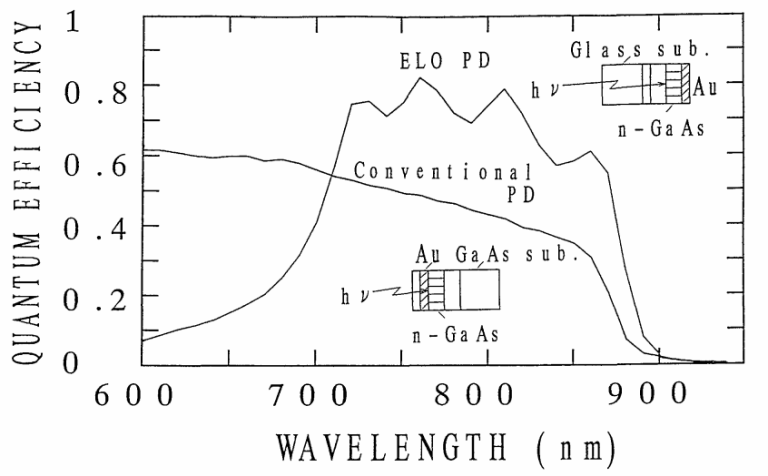


Fig. 2.24: Comparison of spectral response between substrate-based and ELO processed photodiode. Insets show a schematic of both device structure. Reproduced from ref. 58.

Recently, we demonstrated an InGaAs *p-i-n* photodiode both on Si and plastic substrates with almost a 100 % EQE at 1.3 μm wavelength with broad detection range from 1 μm to 1.6 μm by combining ELO and cold-welding processes. The light trapping structure using a rear-side mirror enables a thin active layer, therefore the response speed of the photodetector was maintained while the absorption improved. Furthermore, the detector was fabricated on a flexible platform, therefore it was able to curve into a cylindrical shape to achieve a 360° field of view.

2.3.3 Light emitting diodes

Although, compound semiconductors can provide an internal quantum efficiency over 99%, light emitting diodes usually suffer from a low external quantum efficiency due to the high refractive index contrast between the device and air. According to Snell's law, the escape cone of the semiconductor with refractive index of 3.5 is only ~16° which indicates only ~2% of radiatively recombined photons can be outcoupled into free space. Schnitzer et al. demonstrated a potential solution to improve the EQE of compound semiconductor-based LEDs using the ELO

process and surface texturing.[39] The ELO process enables the lifted-off thin-film to be mounted on the reflector. This minimizes the optical loss of internally generated photons through the substrate by trapping within the active device region till they escape through the surface (Fig 2.25). Furthermore, surface texturing provides angular randomization by scattering to improve outcoupling. Combining these methods, the EQE of GaAs LEDs was improved from 9% to 30%.

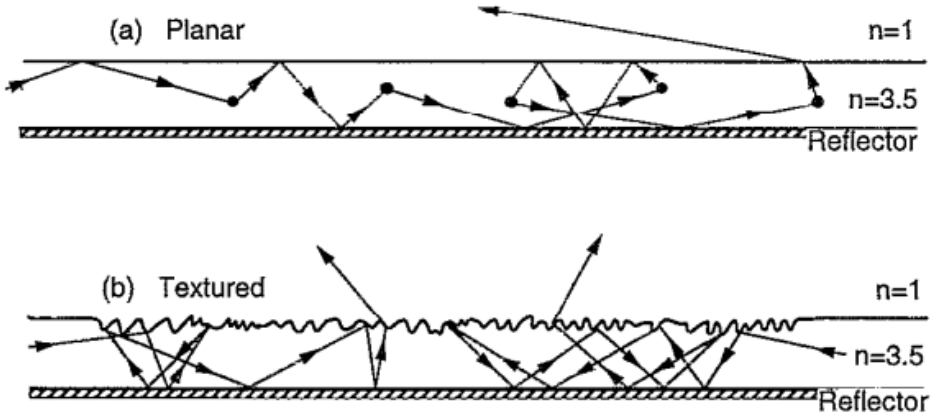


Fig. 2.25: The illustration of rays in thin-film light emitting structures (a) with planar surface and (b) with textured surface. The EQE is enhanced in thin-film structures with rear-side reflectors by self-absorption and re-emission processes, and further improvement can be achieved using angular randomization by strong surface scattering via a textured surface. Reproduced from ref. 39.

A GaAs/AlGaAs heterostructure nonresonant cavity LEDs (NRCLEDs) with 31% external quantum efficiency were demonstrated by outcoupling of lateral waveguide modes by Windisch et al.[59] Furthermore, Corbett et al. demonstrated resonant cavity LEDs (RCLEDs) with a narrow spectral width of 9 meV using two-metal mirrors and InP/InGaAs *p-i-n* structure via an ELO process.[60] The ELO process eliminates the necessity of complex and time-consuming growth of thick DBR stacks for RCLEDs by transferring the thin-film device onto a dielectric mirror.This structure also behaved as a detector under reverse bias.

2.5.4 Lasers

There are relatively small numbers of demonstrations for thin-film lasers using the ELO process. The first demonstration was the double heterostructure GaAs/AlGaAs thin film diode lasers on a glass substrate by Yablonovitch et al.[61] Van der Waals forces were employed to bond a thin-film onto the glass substrate. The laser showed almost identical threshold current density (~1000 A/cm^2) before and after the process. In 1991, a GaAs/AlGaAs graded-index separate-confinement heterostrucure (GRIN-SCH) single-quantum-well (SQW) laser diode on a Si substrate was demonstrated using ELO and the wedge-cleaving processes by Pollentier et al.[62] Figure 2.24(a)-(c) show a schematic illustration of the wedge-induced facet cleaving (WFC) process, device structure, and SEM image of a noncleaved wedge. Their structure contains an AlGaAs layer with Al composition exceeding 40% by using moat etch protection during ELO. The wedge-cleaving process used to form the facet initiates the cleavage using reactive ion etching (RIE) by slightly bending the thin-film. A threshold current of 640 A/cm^2 with the 15% /facet EQE was achieved, which is comparable to that of the reference device (460 A/cm^2). Figure 2.26(d) and (e) shows the spectral responses of WFC-ELO processed lasers at a pulsed input current of 225 mA, and output power-current (P-I) characteristic of WFC-ELO processed and conventional lasers.

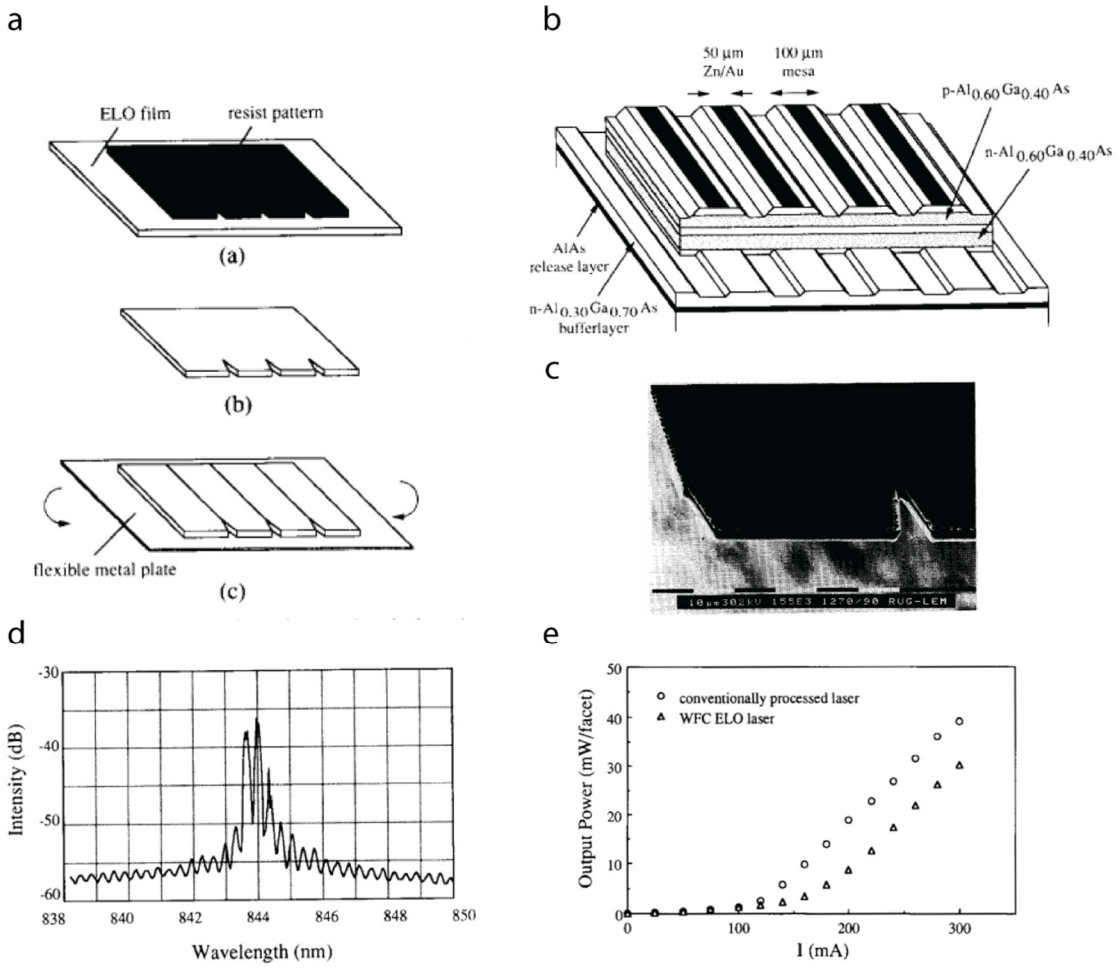


Fig. 2.26: Wedge-induced facet cleaving ELO (WFC-ELO) process for thin-film laser fabrication. (a) Schematic illustration of WFC process. Thin-film is patterned using photolithographic technique, then the facet is form initiate from the wedge by bending the flexible carrier. (b) Schematic of broad-area laser structure. (c) SEM image of noncleaved wedge. (d) Spectral response of WFC-ELO process laser at pulsed input current 225 mA. (e) *P-I* characteristic of a WFC-ELO processed and conventional lasers. Reproduced from ref. 62.

The lift-off process was also used to fabricate a rolled-up thin-film tubular structure to form ring resonators and lasers (Fig. 2.27).[63] The lifted-off film can be rolled by inserting the InGaAs strained layer between the AlAs sacrificial layer and the active device region. The diameter of rolled semiconductor tubes can be controlled in the range of tens of nm to tens of μm by using the

strain of an InGaAs layer which is determined by composition and thickness. The lifted-off thin-film is generally rolled along the <100> planes due to their small Young's modulus. Using this method, optically pumped micro-scale lasers with very low threshold powers (~4 μW) were demonstrated based on InGaAs/GaAs quantum dot tubes. However, the electrically injected tube laser has not been demonstrated due to the difficulty of defining the *p-n* junction in the rolled-up tube structure.

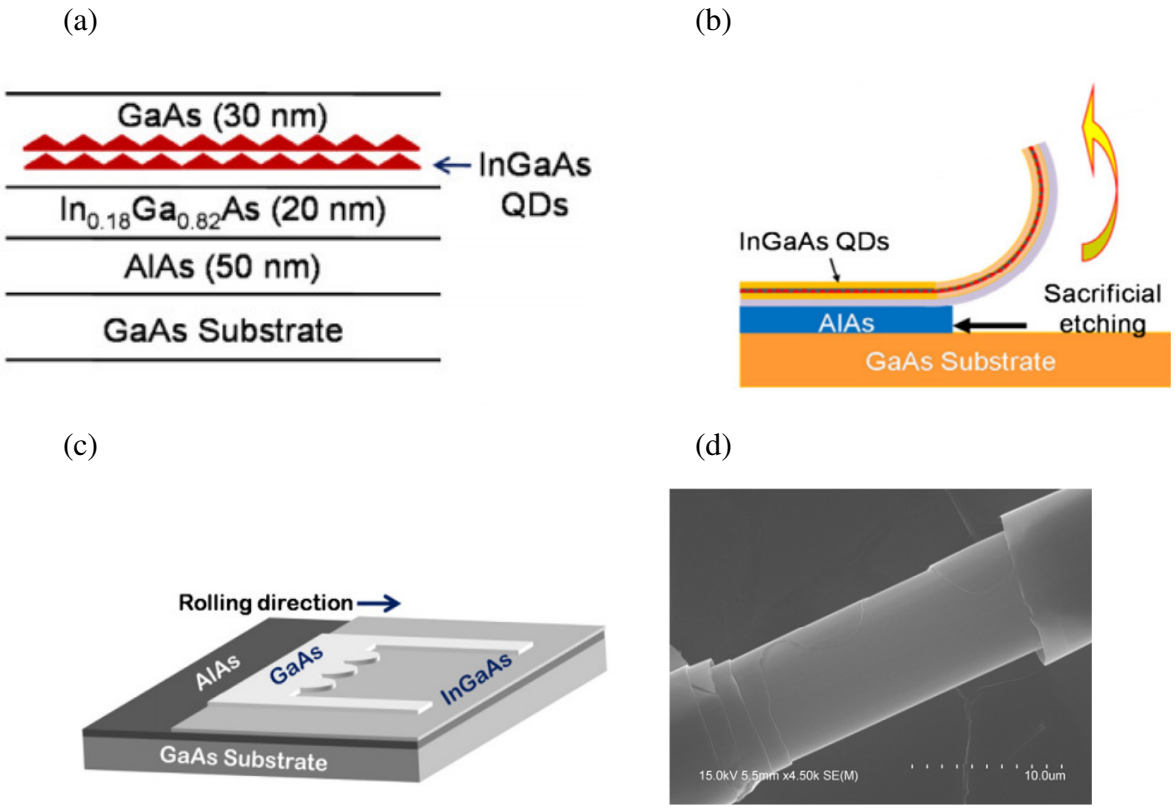


Fig. 2.27: Schematic and image of lift-off process of rolled-up quantum dot microtube. (a) The growth structure of InGaAs/GaAs quantum dot heterostructure for lift-off process. (b) Schematic illustration of fabrication process for microtube ring resonators. (c) The schematic of an etched U-shaped mesa (d) Scanning electron microscopy image of lifted-off rolled up microtube. Reproduced from ref. 63.

2.5.5 Transistors

ELO-processed transistors provide a potential for hybrid or monolithic integration of optoelectronic and RF circuits with Si-based very large scale integrated (VLSI) circuits. Therefore, various transistors have been demonstrated by ELO including high electron mobility field-effect transistors (HEMTs)[64,65], metal semiconductor field-effect transistors (MESFETs) [66,67] and heterojuction bipolar transistors (HBTs).[68]

At high frequency HEMTs into the millimeter wave range enables their use in commercial applications such as cell phones and radar equipment. The GaAs/AlGaAs heterostrucutre commonly used for HEMTs combined with the ELO process allows HEMTs created on host substrates such as Si and glass. Figure 2.28 shows DC and RF performance of wafer and ELO processed HEMTs.[64] The ELO processed HEMTs showed 15~20% degradation in electron mobility and maximum frequency f_{max} possibly due to the inhomogeneous stress in the bonded film which creates the spatial variations in the bandgap, or piezoelectric charges that scatter electrons. However, the ELO processed HEMTs exhibit stable or better (12~20 %) unit current gain cut-off frequency, f_T, while having similar DC and RF characteristics compared with those directly fabricated on a substrate.[64]

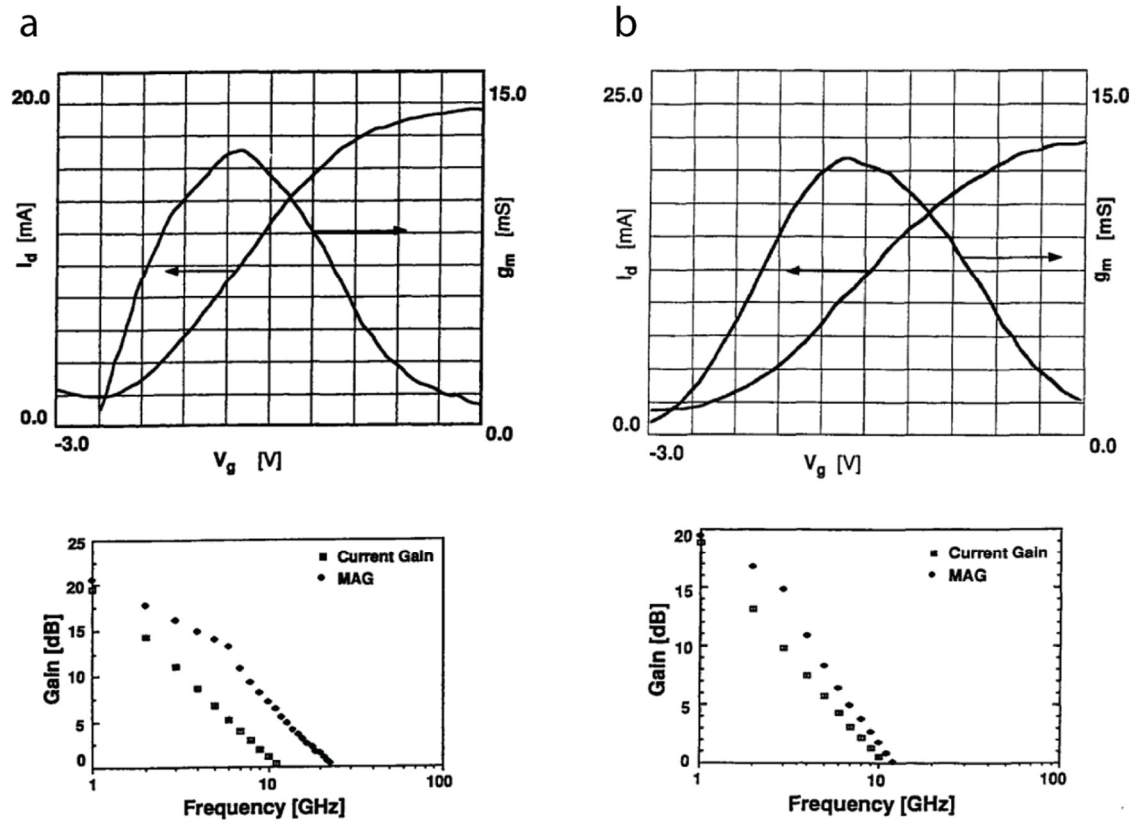


Fig. 2.28: Characteristic of GaAs HEMTs. DC transfer (top) and RF characteristic of (a) an on wafer GaAs HEMTs and (b) an ELO processed GaAs HEMTs. The HEMTs on wafer shows an $f_t = 11.5$ GHz and $f_{max} = 23$ GHz , and ELO processed HEMT shows shows an $f_t = 10.5$ GHz and $f_{max} = 12$ GHz. Reproduced from ref. 64.

MESFET also can be employed for high frequency applications such as military and satellite communications. The transplantation of MESFETs prefabricated by a commercial foundry (Philips Microwave Limeil) to polyimide coated InP substrates was demonstrated to confirm the feasibility of integration by Pollentier et al.[66] The transplanted MESFETs showed no significant DC and RF performance and reliability degradation after the ELO process (Fig. 2.29(a) and (b)). Furthermore, Moat et al. investigated effects of thermal conductivity of the host substrate on the operation temperature of ELO processed MESFETs. Figure 2.29(c) shows microscope images of ELO processed MESFETs on quartz. The maximum on-chip surface temperature was

significantly higher when the device was transferred onto the substrate with high thermal resistivity such as quartz (Fig. 2.29(d)).[67] In contrast, the transferred MESFETs onto low thermal resistivity materials such as Si showed minor effects on device performance, which confirms the potential for integration of MESFETs with CMOS circuits.

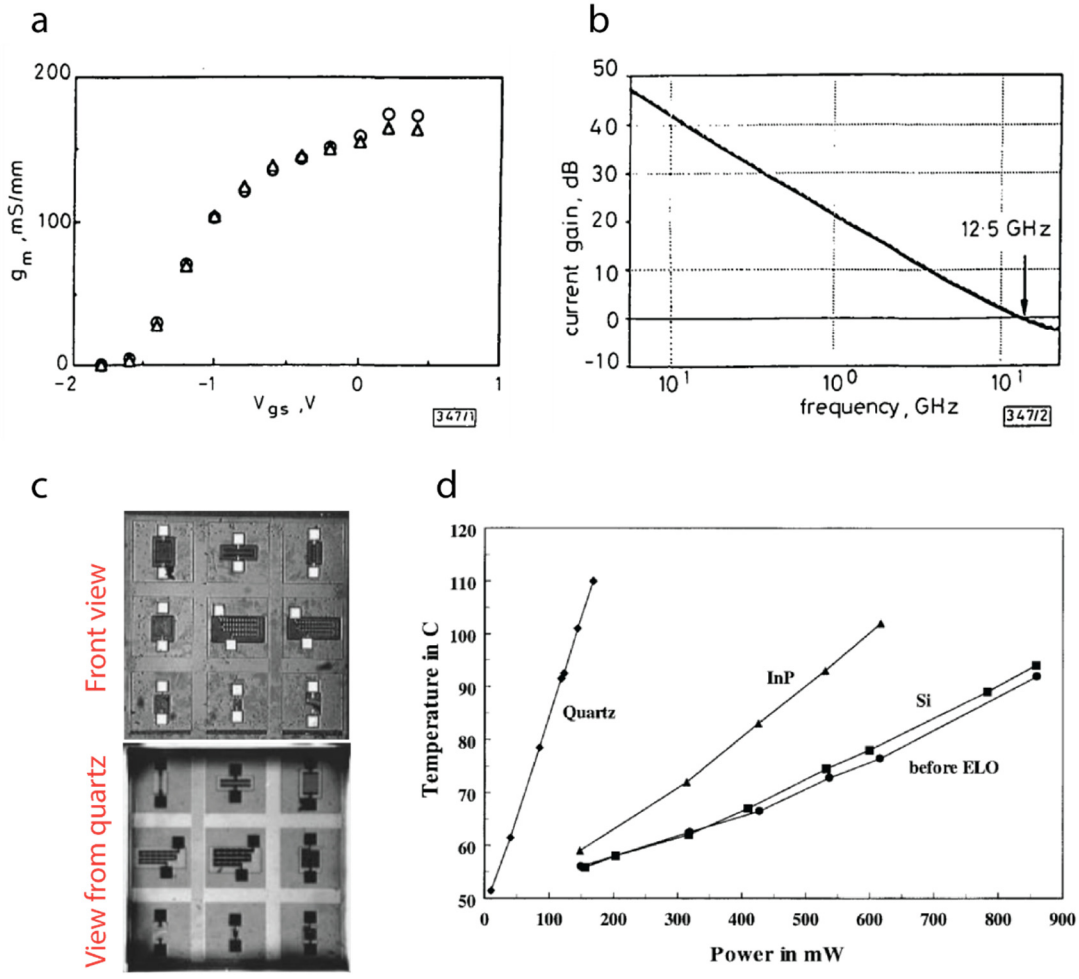


Fig. 2.29: Characteristic of MESFETs. (a) Transconductance of MESFETs before and after ELO process at V_{ds} = 3V. (b) RF behavior of MESFETs before and after ELO process (Solid line: after ELO, dashed line: before ELO). Measurements showed nearly no difference in DC and RF operation before and after ELO process. (c) Microscope images of ELO processed MESFETs on quartz (top : front view, bottom: view from quartz side). (d) Maximum on chip surface temperature of ELO processed films on various substrates measured by IR microscope. Reproduced from refs. 66 and 67.

AlGaAs/GaAs HBTs fabricated on Si substrates provide considerably higher current gain (550) compared to that of similar structures directly grown on Si (~100) since the structures were grown on lattice-matched substrates and then transferred onto host substrates.[68] The HBTs on Si provide a potential to combine high speed HBTs with Si VLSI. Furthermore, the power dissipation in HBTs can be reduced by transferring them onto Si which has higher thermal conductivity.

2.6 Substrate recycling

A major benefit of the ELO process is the potential for reusing the parent substrate which reduces the device production cost. However, wafer recycling followed by ELO processing has been limited due to a degraded surface quality left by the ELO process. This is partially due to the accumulation of contaminants on the surface, and surface roughening due to the slow etch of the wafer by HF.[22,69] To recover the surface quality of the parent wafer in preparation for its recycling, understanding the origin of the contaminants on GaAs is needed. Fig 2.30(a) shows an optical microscope image of a GaAs wafer surface without a sacrificial layer exposed to a 20% HF solution, then stored in air.[22] This image provides evidence that the accumulation of reaction product on the wafer surface not only originates from the AlAs etching, but also from the GaAs etching reaction. The etch rate of GaAs in HF was measured to be ~16 nm/hr with a weak dependence on HF concentration (Fig. 2.30(b)). The etching of GaAs in HF in the dark results in a brown haze on the surface (Fig. 2.30(c)). X-ray photoelectron spectroscopy (XPS) measurements on this brown deposit indicates an elemental arsenic peak with a small signal related to As_2O_3, but without GaAs related signals.[22] The SEM image shows the morphology of the brown haze on GaAs surface that consists of small hillocks (Fig. 2.30(d)). In contrast, no-

fluoride containing compounds were observed indicating that these reaction products are possibly dissolved in the etchant.

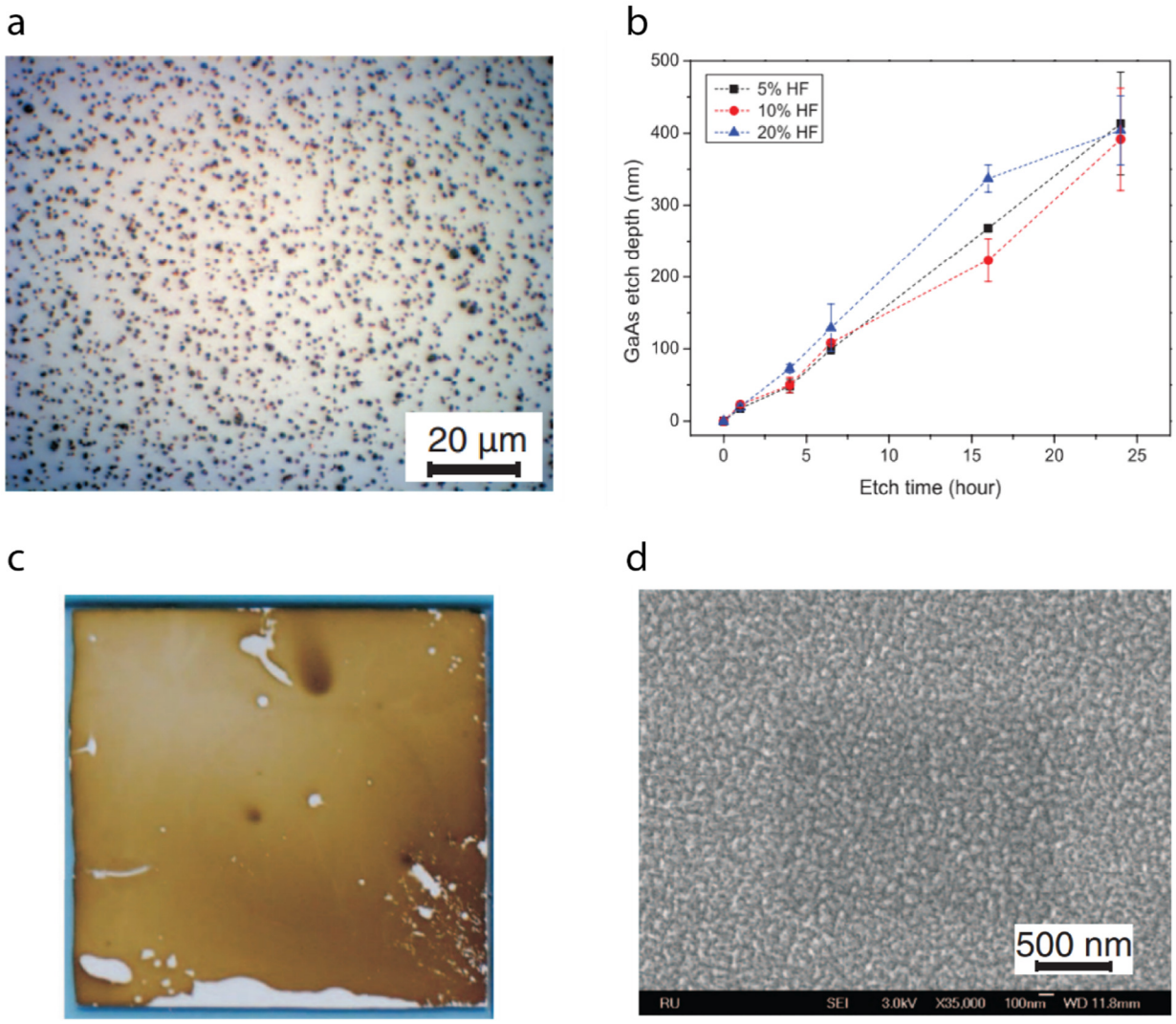


Fig. 2.30: Reaction of GaAs in HF etchant (a) Optical microscope image of GaAs surface after exposed to HF, and stored in ambient air. (b) Etch rate of GaAs in dilute HF etchant. (c) Optical microscope image of GaAs surface after exposed to HF while it is kept in dark during etching. (d) SEM image of the brown haze in fig. 2.15(b). Reproduced from ref. 22.

The reaction between GaAs and HF was further investigated by exposing the GaAs surface to HF solution under various condition. Figure 2.31(a)-(c) show a schematic overview of GaAs

reaction process in dilute HF under various conditions. In the dark, GaAs was very slowly etched by undissociated HF via a synchronous bond-exchange mechanism (Fig. 2.31(a)).[70] The Ga product is dissolved as a fluoride, and the arsine product is chemically decomposed (or via a redox reaction) into elemental arsenic that covers the GaAs surface (Fig. 2.31(d)). The accumulation of As on GaAs does not halt the etch of GaAs, and only a portion of etch reaction product (AsH_3) is formed into an As accumulation layer, since the 400 nm thick GaAs etching produces only a 20 to 30 nm thick As layer on its surface.

Figure 2.31(b) shows a schematic process for chemical reaction of GaAs in HF solution under illumination. Accumulation of elemental As from GaAs etching under illumination was observed to be more uniform and thin compared to the same chemical reaction resulting from etching in the dark. This is possibly due to electroless photoetching that occurs when a semiconductor in an etchant is exposed to supra-bandgap light.[70,71] The photogenerated electrons react with the oxygen in the HF solution, and photogenerated holes oxidize both Ga and As, or only Ga depending on the number of holes that participate in the process (6 and 3 holes, respectively).[22] Thus, chemical reactions assisted by photogenerated carriers help to nucleate more uniform As layers compared to that formed by the decomposition of AsH_3 in the dark. A similar influence of light in the etching process is also observed for AlAs epitaxial layer in HF etchant.[72]

Figure 2.31(c) shows a schematic process for the As_2O_3 micro-crystal formation during sample storage. The As layer reacts with H_2O in an ambient environment assisted by photogenerated holes, which leads to the growth of As_2O_3 micro-crystallites possibly by convection diffusion of AsO_2^- ions[73,74], and super-saturation/hydrolysis. This crystal formation process is a photocatalyzed reaction since it requires both air and light. Figure 2.31(d)-(f) show

SEM images of HF etchant-exposed GaAs surfaces for different storage times (immediately after etching, after 3hours and 4 weeks storage, respectively.) in ambient.

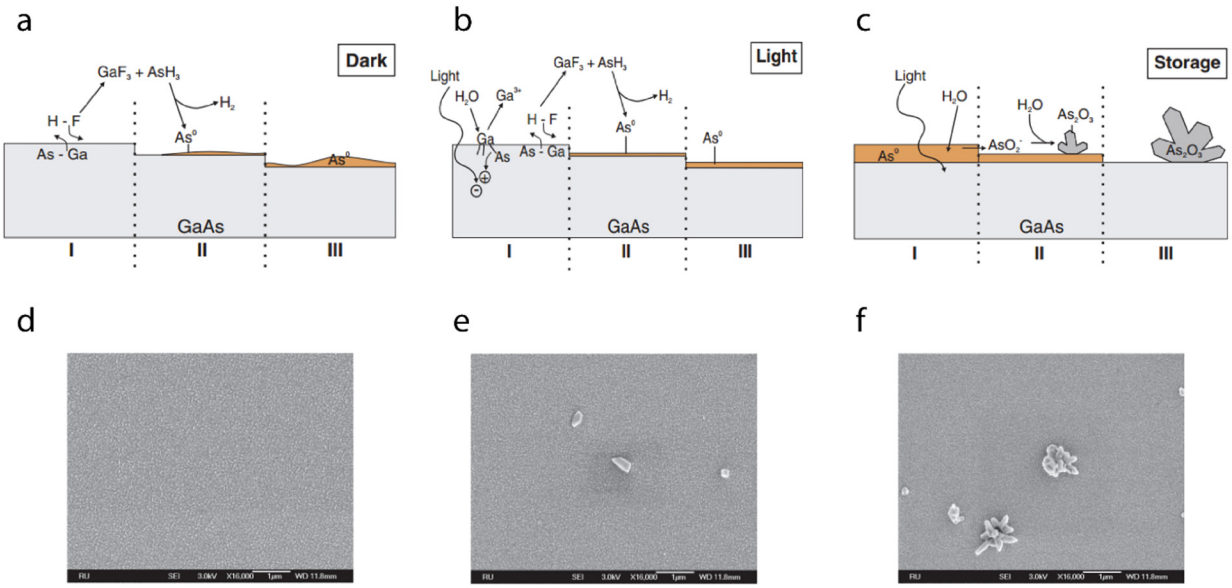


Fig. 2.31: Reaction of GaAs in HF etchant under dark and illumination condition. Schematic overview of reaction process on GaAs surface (a) during exposed to HF under dark condition, (b) under illumination and (c) during storage in ambient environment. SEM images of etched GaAs surface by HF (d) immediately after the etching, (e) after storage of sample for 3 hours and (f) for 4 weeks. Reproduced from ref. 22.

2.6.1 Chemo-mechanical polishing

To recover the surface quality, various chemical polishing processes have been tested (Fig. 2.32(a)). The devices grown and fabricated from chemically polished substrates followed by the ELO process exhibit the significantly degraded *IV* characteristics compared with those obtained from the fresh substrate (Fig. 2.32(b)).[17] Poor J_{sc} and V_{oc} of devices grown on a chemical polished wafers indicate reduced growth quality possibly due to the large scale surface roughness or surface contamination which is not completely removed by the chemical polishing process.

The CMP process is a more straightforward method to prepare the epi-ready surface. Bauhuis et al.[17] and Adams et al.[18] demonstrated wafer recycling using the CMP process without significant performance degradation. However, the CMP process has the limitation of production cost reduction due to the restriction on the number of wafer reuses. This restriction is caused by the wafer thinning, the relatively expensive cost for CMP process, and low yield especially when the wafer is thinned after a few cycles.[75]

(a)

Constituents	Volume ratio	R_a (nm)		
		Etchant	Anneal	Buffer
$H_2SO_4/H_2O_2/H_2O$	1:1:10	0.8	—	—
Br_2/CH_3OH	1:99	0.4	—	—
$NH_4OH/H_2O_2/H_2O$	2:1:10	0.5	0.4	0.2
$NH_4OH/H_2O_2/H_2O$	1:1:50	0.9	0.4	0.2
$HCl/H_2O_2/H_2O$	1:1:30	2.4	0.8	0.4
$NH_4OH/H_2O_2/H_2O$ +	1:1:50	0.8	0.7	0.3
$HCl/H_2O_2/H_2O$	1:1:30	—	—	—
$HCl/H_2O_2/H_2O$ +	1:1:30	1.5	1.3	0.5
$NH_4OH/H_2O_2/H_2O$	1:1:50	—	—	—
$HCl/H_2O_2/H_2O$ +	1:1:30	2.4	1.7	1.7
$NH_4OH/H_2O_2/H_2O$	2:1:10	—	—	—

(b)

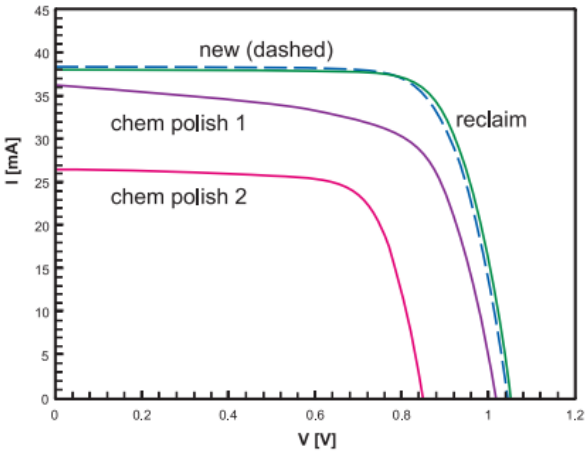


Fig. 2.32: Parent substrate recycling after ELO process (a) Test of various etchants for chemical polishing of an ELO processed GaAs wafer surface. (b) Comparisons of *IV*-characteristics between thin-film GaAs solar cells grown on fresh, chemical polished and chemo-mechanical polished substrate. Reproduced from ref. 17.

2.6.2 Epitaxial protection layers

Recently, we demonstrated wafer recycling for both InP and GaAs without CMP by employing epitaxial protection layers between the sacrificial layer and the wafer.[6,19] We analyzed the recovered surface quality by comparing the morphology and chemistry of the surface before

and after protection layer removal using various microscopic methods including atomic force microscopy, scanning electron microscopy, 3D laser scanning microscopy, energy dispersive X-ray spectroscopy, and X-ray photoelectron microscopy. Furthermore, the crystallinity, electrical and optical properties of the epi-layer grown on a reused wafer were determined using cross-sectional transmission electron microscopy, Hall effect and photoluminescence measurements, respectively. Moreover, multiple batches of optoelectronic devices, such as photovoltaic cells, LEDs and MESFETs were fabricated from a single parent wafer without any systematic performance degradation. This method will be discussed in detail throughout this thesis.

2.7 Various fabrication methods for thin-film optoelectronic devices

Complete removal of the substrate was a traditional method to create thin-film compound semiconductor crystalline layers, and we discussed the ELO process that is the most intensively investigated lift-off technology. In this section, we introduce various additional lift-off technologies to produce the thin-film optoelectronic devices.

2.7.1 Controlled spalling

Thin-film semiconductor layer can be created by the propagation of a spalling mode fracture within the substrate bulk, parallel to the surface. This process is called controlled spalling. It uses a tensile stressor layer (e.g. Ni) and flexible handle to mechanically guide the fracture front.[76,77] Figure 2.33(a)-(d) show a schematic illustration of controlled spalling and an image of a fabricated thin-film solar cells on a flexible foil produced by this method. This process can be used to create a single crystalline thin-film layer not only for compound semiconductors, but also for elemental semiconductors such as Si and Ge. Furthermore, the lift-off of the thin-film layer

directly from the ingot has been demonstrated using the spalling process.[77] To show its feasibility as a means for thin-film optoelectronic device production, this process was employed for the fabrication of dual and triple junction solar cells (Fig 2.33(a)-(d)) and CMOS circuits.[78] Lifted-off thin-film devices show comparable performance with the reference devices. However, the spalling process provides a relatively large spalled layer thickness variation (~1 μm), and the surface quality of lift-off film is affected by the semiconductor surface orientation.

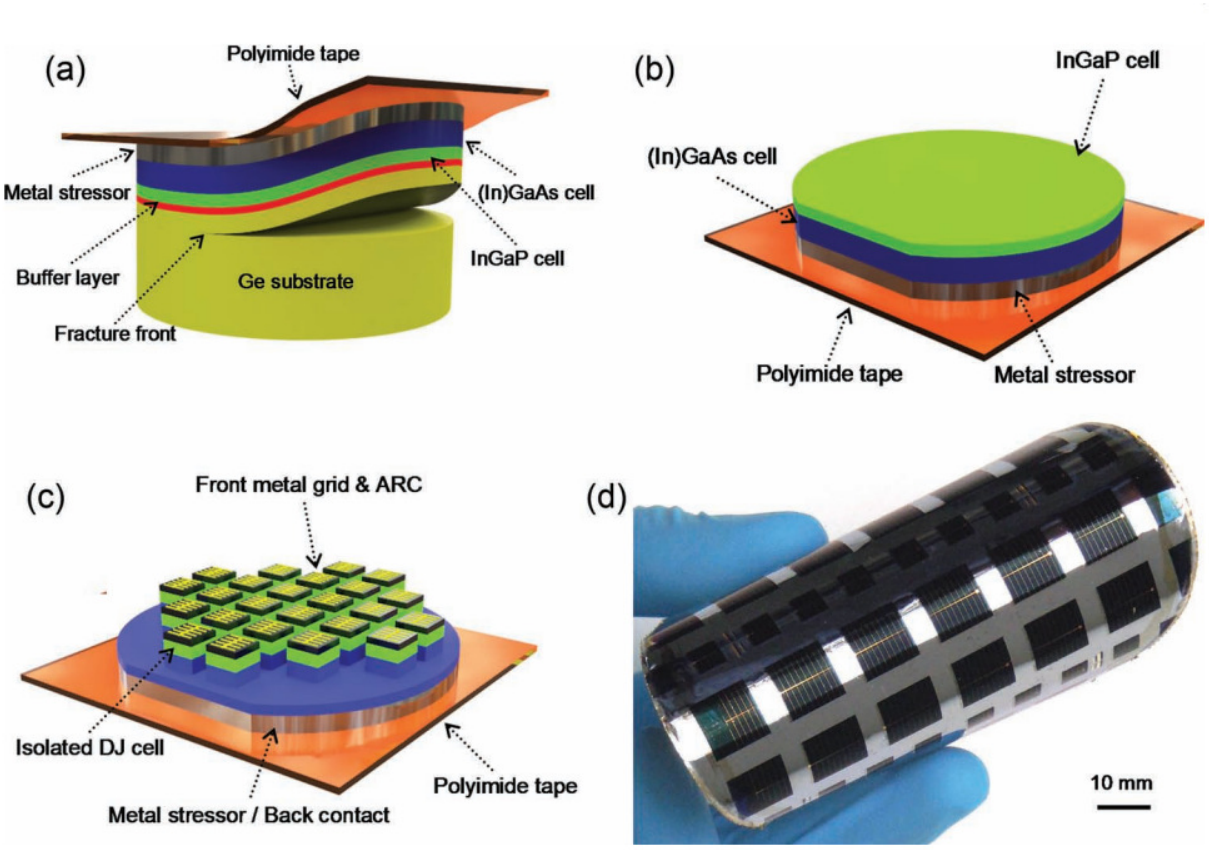


Fig. 2.33: Illustration of controlled spalling process and image of fabricated thin-film solar cells. (a) The schematic of structure used in controlled spalling process. (b) Schematic of lifted-off thin-film active layers bonded on polyimide tape. (c) Schematic of fabricated thin-film solar cells on flexible substrate. (d) Photograph of fabricated thin-film tandem solar cells on plastic substrate. Reproduced from ref. 78.

2.7.2 Exfoliation

Exfoliation is a mechanical lift-off process similar to controlled spalling. However, this process produces thin-film active layer separation by physically weakening the thin region using hydrogen ion implantation, then the weakened interface is cleaved (Fig. 2.34).[79] This process is called the Smart-Cut process that is intensively used for the preparation of Silicon on Insulator (SOI) wafers. For compound semiconductors, exfoliation is used to create an engineered substrate consisting of thin-film epitaxial templates on top of host substrate and thin-film solar cells such as Si or glass (Fig. 2.34).[5,80]

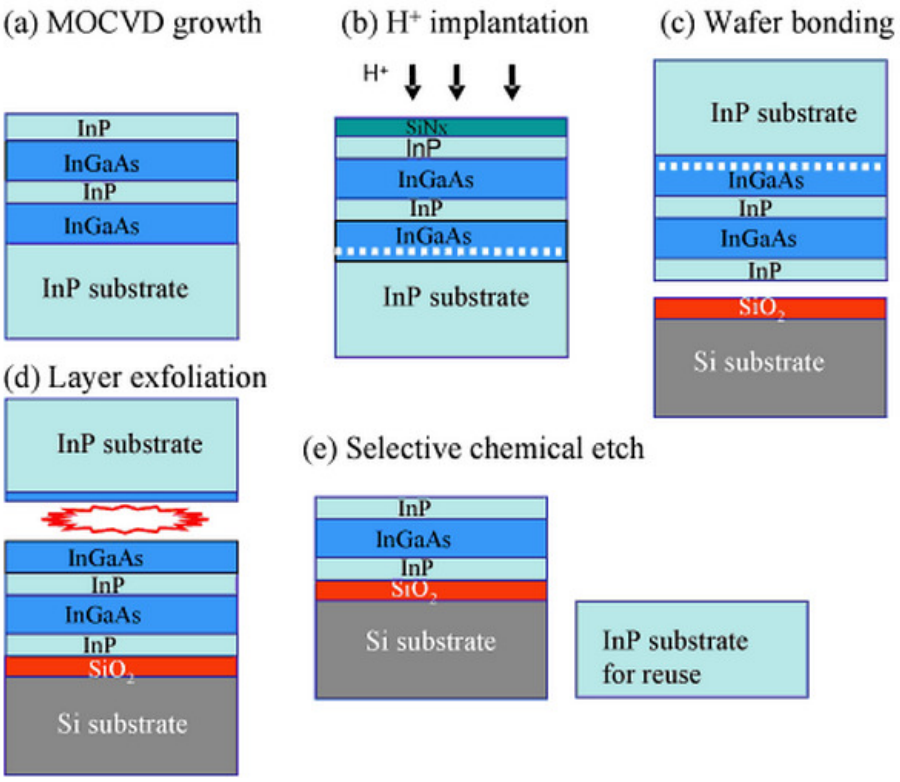


Fig. 2.34: Process flow chart for InP layer transfer via exfoliation process. (a) Heterostructure growth using MOCVD (b) Hydrogen ion implantation process (c) Wafer bonding process (d) Exfoliation process induced by thermal annealing (e) Selective chemical etching process of both samples. Reproduced from ref. 79.

Fabricated InGaAs solar cells (PCE = 13.6 %) on InP/Si[5] and InGaP/GaAs tandem solar cells (PCE = 15.5 %) on Ge/Si epitaxial templates[80] were demonstrated using the exfoliation process without significant performance degradation compared with the reference cell. However, this process is relatively expensive, mainly caused by the hydrogen implantation process.

2.7.3 Cleavage of lateral epitaxial films for transfer (CLEFT)

The CLEFT process was developed to produce multiple single crystalline thin-film layers from a single substrate using lateral vapor phase epitaxy (VPE) by McClelland et al.[4] Figure 2.35(a) shows a process flow chart. For the CLEFT process, a carbonized photoresist is first patterned on a (100) GaAs substrate with an appropriate spacing (e.g. 2.5 μm wide striped openings), then epitaxial growth is initiated within the patterned opening, followed by lateral growth over the mask. Once it reaches ~ 1 μm film thickness, it forms a continuous single crystalline film. After the growth, the sample is bonded to the host substrate and the thin-film layer is mechanically cleaved from the substrate using a cleaving wedge (Fig. 2.35(b)). Comparable film quality of the lateral epitaxial growth layer before and after lift-off is confirmed by Hall effect measurements. However, the CLEFT process requires epitaxy technique which allows for lateral growth, and the film quality of lateral epitaxy is poor compared to ane identical film grown on a crystalline substrate using conventional epitaxial growth.[4]

(a) (b)

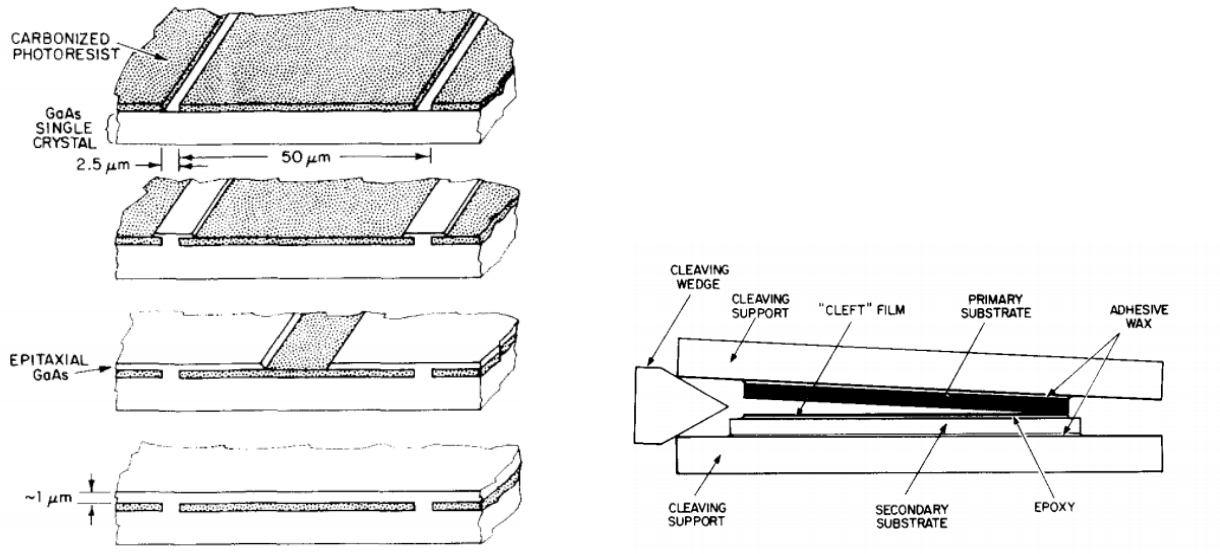


Fig. 2.35: Schematic illustration of cleavage of lateral epitaxial films for transfer (CLEFT) process. (a) Fabrication flow for CLEFT process. The photoresist is patterned on a GaAs substrate, then the GaAs layer is grown together laterally from the narrow slot to form a continuous single crystalline film. (b) Cross-sectional view of thin-film transferring process to a host substrate. A small force is applied to cleave the sample. Reproduced from ref. 4.

2.7.4 Modified ELO

Multiple layer release is an ELO process that produces multiple crystalline layers from a stack of layers on a single wafer.[8] This process was proposed by Konagai et al. when the ELO process was initially introduced. An identical process structure was also employed for a multiple release layer etch method to examine the lateral etch rate of the ELO process dependence on Al faction in the sacrificial layer. Recently, Yoon et al. demonstrated a multiple batch of photovoltaic cells, MESFETs and photodiodes from a single GaAs substrate using releasable multilayer epitaxial assemblies (Fig. 2.36). However, the long growth time with high doping concentration in the device contact layers leads to unwanted *p*-type Zn dopant diffusion to adjacent layers which

causes degradation of devices in the bottom of the stack compared with those on top. This issue was resolved by switching the Zn dopant to carbon[81] or changing the structure from n-on-p to p-on-n.[82] However, the demonstration of a multiple layer release process is still limited to sub-millimeter size devices (~500 µm).

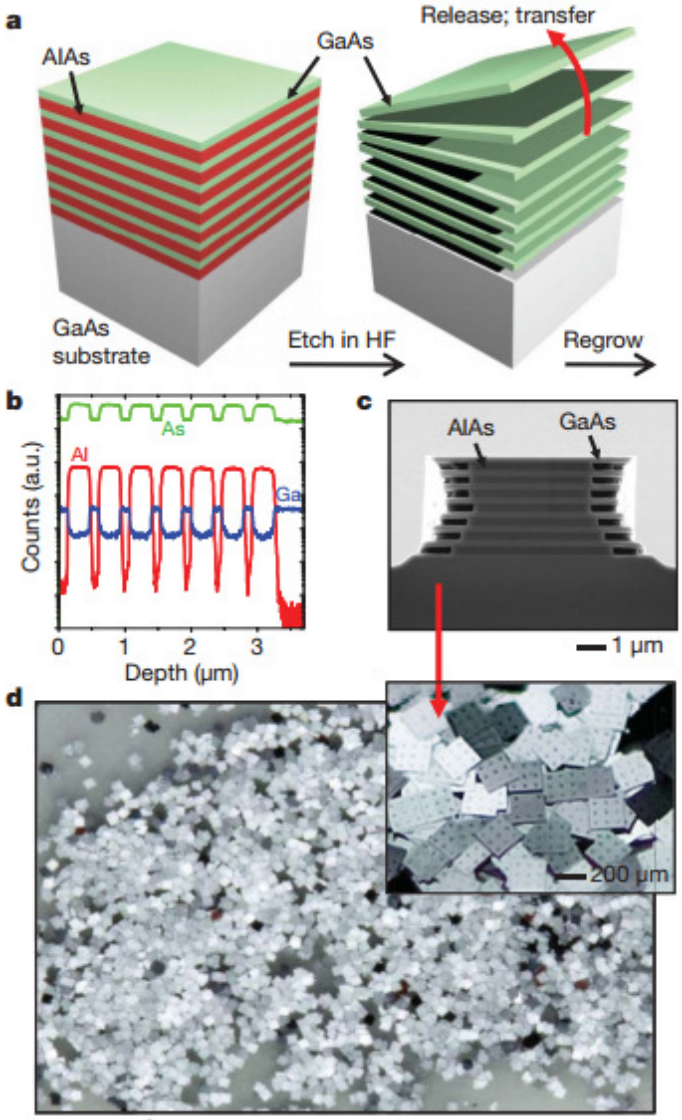


Fig. 2.36: The multiple layer release process. (a) Schematic of epi-layer structure and fabrication flow for the multiple layer release process. (b) SIMS profile and (c) SEM image of epitaxial structure. (d) Photograph of a collection of GaAs solar cells produced by a multiple layer release process. Reproduced from ref. 8.

Recently, the ELO process employing an AlInP sacrificial layer instead of AlAs combined with HCl-based etching was developed.[34] The HCl-based etchant provides a residue-free post-ELO surface which allows for substrate recycling without CMP. Furthermore, surface-tension was used to accelerate the ELO process by creating a wide opening at etch interface that assists in HF etchant diffusion (Fig. 2.37). However, this process requires encapsulation of an In-containing alloy in the device structure used for passivation or side-wall protection due their high etching rate in HCl. Therefore the demonstration using an HCl-based ELO process is limited only to In-free compound semiconductors.

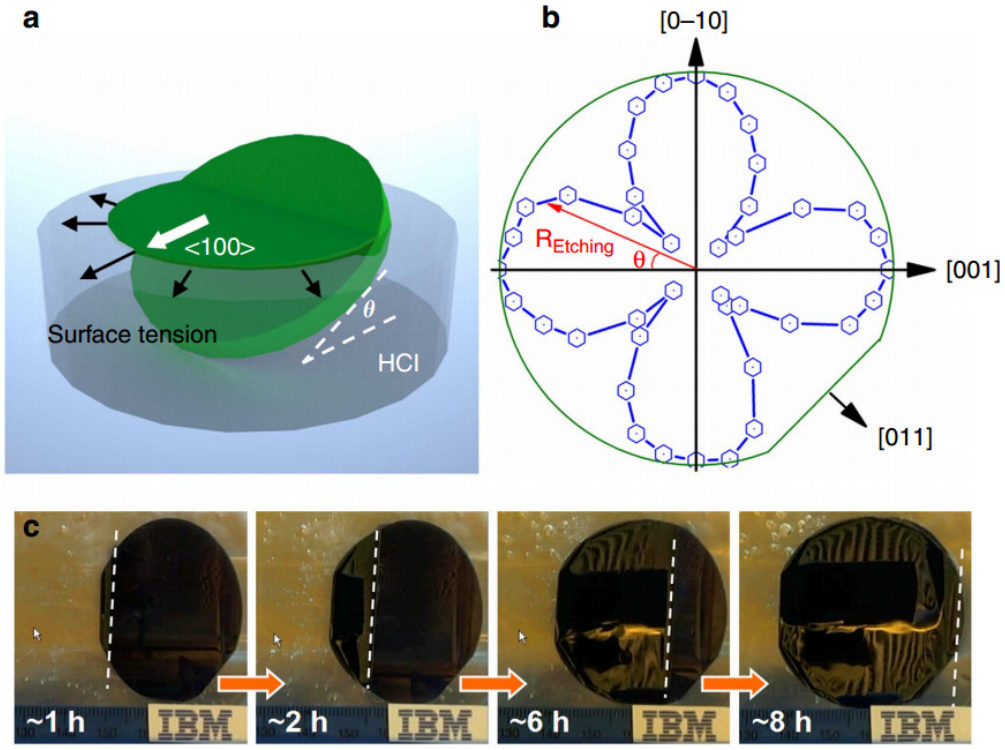


Fig. 2.37: Surface tension-assisted ELO process. (a) Schematic of surface tension-assisted ELO process. (b) Crystallographic direction dependent etch rate of AlInP in HCl. (c) Photographs of the surface tension-assisted ELO process. The average lateral etching rate of 5.9 mm/h is achieved. Reproduced from ref. 34.

2.8 Conclusion

Compound semiconductor based thin-film optoelectronic devices exhibit numerous benefits over bulky and rigid substrate-based devices including lightweight and flexibility, as well as superior performance enabled by light trapping and photon recycling. These advantages have driven the development of various lift-off technologies. Moreover, lift-off technologies provide a potential for substrate recycling after the process; thus, the device production cost can be dramatically reduced. However, most lift-off technologies are in their infancy mainly due to immature fabrication process development and high processing cost. To overcome the cost and technical barriers, considerable efforts have been focused on improving the ELO process, which is promising due to its simplicity and controllability. As a result, advanced processing concepts including ND-ELO, WI-ELO, surface tension-assisted ELO and multi-layer release processes have been derived from the original ELO process. These improved ELO processes allow high throughput, low-cost and simplified methods for advanced compound semiconductor-based thin-film optoelectronic device fabrication. The development of cost-efficient lift-off technologies for high quality thin-film compound semiconductor epitaxial layers is a critical step towards allowing high performance optoelectronic devices to be fabricated on conformal and flexible substrate for countless applications.

CHAPTER II

Bibliography

1. Konagai, M., Sugimoto, M. & Takahashi, K. High efficiency GaAs thin film solar cells by peeled film technology. *J. Cryst. Growth* **45,** 277–280 (1978).

2. Yablonovitch, E., Gmitter, T., Harbison, J. P. & Bhat, R. Extreme selectivity in the lift-off of epitaxial GaAs films. *Appl. Phys. Lett.* **51,** 2222 (1987).

3. Shahrjerdi, D. *et al.* High-efficiency thin-film InGaP/InGaAs/Ge tandem solar cells enabled by controlled spalling technology. *Appl. Phys. Lett.* **100,** 3 (2012).

4. McClelland, R. W., Bozler, C. O. & Fan, J. C. C. A technique for producing epitaxial films on reuseable substrates. *Appl. Phys. Lett.* **37,** 560 (1980).

5. Zahler, J. M. *et al.* High efficiency InGaAs solar cells on Si by InP layer transfer. *Appl. Phys. Lett.* **91,** 012108 (2007).

6. Lee, K., Zimmerman, J. D., Hughes, T. W. & Forrest, S. R. Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics. *Adv. Funct. Mater.* **24,** 4284–4291 (2014).

7. Voncken, M. M. A. . *et al.* Influence of radius of curvature on the lateral etch rate of the weight induced epitaxial lift-off process. *Mater. Sci. Eng. B* **95,** 242–248 (2002).

8. Yoon, J. *et al.* GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies. *Nature* **465,** 329–333 (2010).

9. Yablonovitch, E. Statistical ray optics. *J. Opt. Soc. Am.* **72,** 899 (1982).

10. Asbeck, P. Self-absorption effects on the radiative lifetime in GaAs-GaAlAs double heterostructures. *J. Appl. Phys.* **48,** 820 (1977).

11. Miller, O. D., Yablonovitch, E. & Kurtz, S. R. Strong Internal and External Luminescence as Solar Cells Approach the Shockley–Queisser Limit. *IEEE J. Photovoltaics* **2,** 303–311 (2012).

12. Voncken, M. M. A. J., Schermer, J. J., Bauhuis, G. J., Mulder, P. & Larsen, P. K. Multiple release layer study of the intrinsic lateral etch rate of the epitaxial lift-off process. *Appl. Phys. A* **79,** (2003).

13. Yablonovitch, E., Hwang, D. M., Gmitter, T. J., Florez, L. T. & Harbison, J. P. Van der Waals bonding of GaAs epitaxial liftoff films onto arbitrary substrates. *Appl. Phys. Lett.* **56,** 2419 (1990).

14. Bauhuis, G. J., Mulder, P., Haverkamp, E. J., Huijben, J. C. C. M. & Schermer, J. J. 26.1% thin-film GaAs solar cell using epitaxial lift-off. *Sol. Energy Mater. Sol. Cells* **93,** 1488–1491 (2009).

15. Kayes, B. M. *et al.* 27.6% Conversion efficiency, a new record for single-junction solar cells under 1 sun illumination. in *2011 37th IEEE Photovolt. Spec. Conf.* 000004–000008 (IEEE, 2011).

16. Shockley, W. & Queisser, H. J. Detailed Balance Limit of Efficiency of p-n Junction Solar Cells. *J. Appl. Phys.* **32,** 510 (1961).

17. Bauhuis, G. J. *et al.* Wafer reuse for repeated growth of III-V solar cells. *Prog. Photovoltaics Res. Appl.* **18,** 155–159 (2010).

18. Adams, J. *et al.* Demonstration of Multiple Substrate Reuses for Inverted Metamorphic Solar Cells. *IEEE J. Photovoltaics* **3,** 899–903 (2013).

19. Lee, K., Shiu, K.-T., Zimmerman, J. D., Renshaw, C. K. & Forrest, S. R. Multiple growths of epitaxial lift-off solar cells from a single InP substrate. *Appl. Phys. Lett.* **97,** 101107 (2010).

20. Van Niftrik, A. T. J. *et al.* HF Species and Dissolved Oxygen on the Epitaxial Lift-Off Process of GaAs Using AlAsP Release Layers. *J. Electrochem. Soc.* **155,** D35 (2008).

21. Voncken, M. M. A. J. *et al.* Etching AlAs with HF for Epitaxial Lift-Off Applications. *J. Electrochem. Soc.* **151,** G347 (2004).

22. Smeenk, N. J. *et al.* Arsenic Formation on GaAs during Etching in HF Solutions: Relevance for the Epitaxial Lift-Off Process. *ECS J. Solid State Sci. Technol.* **2,** P58–P65 (2012).

23. Voncken, M. M. A. J. *et al.* Etching AlAs with HF for epitaxial lift-off applications. *J. Electrochem. Soc.* **151,** G347–G352 (2004).

24. Voncken, M. M. A. J., Schermer, J. J., Bauhuis, G. J., Niftrik, A. T. J. van & Larsen, P. K. Strain-accelerated HF etching of AlAs for epitaxial lift-off. *J. Phys. Condens. Matter* **16,** 3585–3596 (2004).

25. Van Niftrik, A. T. J. *et al.* A Diffusion and Reaction Related Model of the Epitaxial Lift-Off Process. *J. Electrochem. Soc.* **154,** D629 (2007).

26. Schermer, J. J. *et al.* Photon confinement in high-efficiency, thin-film III–V solar cells obtained by epitaxial lift-off. *Thin Solid Films* **511-512,** 645–653 (2006).

27. Kim, C., Burrows, P. & Forrest, S. Micropatterning of organic electronic devices by cold-welding. *Science* **288,** 831–3 (2000).

28. Ferguson, G. S., Chaudhury, M. K., Sigal, G. B. & Whitesides, G. M. Contact adhesion of thin gold films on elastomeric supports: cold welding under ambient conditions. *Science* **253,** 776–778 (1991).

29. Haisma, J. & Spierings, G. A. C. M. Contact bonding, including direct-bonding in a historical and recent context of materials science and technology, physics and chemistry. *Mater. Sci. Eng. R Reports* **37,** 1–60 (2002).

30. Savage, G. *A concise history of bronzes.* Praeger, (1969).

31. Smith, J., Bozzolo, G., Banerjea, A. & Ferrante, J. Avalanche in adhesion. *Phys. Rev. Lett.* **63,** 1269–1272 (1989).

32. Meitl, M. A. *et al.* Transfer printing by kinetic control of adhesion to an elastomeric stamp. *Nat. Mater.* **5,** 33–38 (2005).

33. Lee, C. H. *et al.* Peel-and-stick: fabricating thin film solar cell on universal substrates. *Sci. Rep.* **2,** 1000 (2012).

34. Cheng, C.-W. *et al.* Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics. *Nat. Commun.* **4,** 1577 (2013).

35. Kelsall, R. W. Hybrid silicon lasers: Rubber stamp for silicon photonics. *Nat. Photonics* **6,** 577–579 (2012).

36. John St., A. E. Multiple internal reflection structure in a silicon detector which is obtained by sandblasting. (1968).

37. Redfield, D. Multiple-pass thin-film silicon solar cell. *Appl. Phys. Lett.* **25,** 647 (1974).

38. Steiner, M. A. *et al.* Optical enhancement of the open-circuit voltage in high quality GaAs solar cells. *J. Appl. Phys.* **113,** 123109 (2013).

39. Schnitzer, I., Yablonovitch, E., Caneau, C., Gmitter, T. J. & Scherer, A. 30% external quantum efficiency from surface textured, thin-film light-emitting diodes. *Appl. Phys. Lett.* **63,** 2174 (1993).

40. Hwang, C. Quantum Efficiency and Radiative Lifetime of the Band-to-Band Recombination in Heavily Doped n-Type GaAs. *Phys. Rev. B* **6,** 1355–1359 (1972).

41. Dumke, W. Spontaneous Radiative Recombination in Semiconductors. *Phys. Rev.* **105,** 139–144 (1957).

42. Stern, F. Photon recycling in semiconductor lasers. *J. Appl. Phys.* **45,** 3904 (1974).

43. Ahrenkiel, R. K. *et al.* Ultralong minority-carrier lifetime epitaxial GaAs by photon recycling. *Appl. Phys. Lett.* **55,** 1088 (1989).

44. Lush, G. & Lundstrom, M. Thin film approaches for high-efficiency III–V cells. *Sol. Cells* **30,** 337–344 (1991).

45. Lundstrom, M. S. *et al.* Radiative recombination and photon recycling in gallium arsenide solar cells. in *AIP Conf. Proc.* **268,** 298–303 (AIP, 1992).

46. Kosten, E. D., Kayes, B. M. & Atwater, H. A. Experimental demonstration of enhanced photon recycling in angle-restricted GaAs solar cells. *Energy Environ. Sci.* **7,** 1907 (2014).

47. Kosten, E. D., Atwater, J. H., Parsons, J., Polman, A. & Atwater, H. A. Highly efficient GaAs solar cells by limiting light emission angle. *Light Sci. Appl.* **2,** e45 (2013).

48. Sheng, X. *et al.* Device Architectures for Enhanced Photon Recycling in Thin-Film Multijunction Solar Cells. *Adv. Energy Mater.* n/a–n/a (2014). doi:10.1002/aenm.201400919

49. Lee, X. Y. *et al.* Thin film GaAs solar cells on glass substrates by epitaxial liftoff. in *Conf. Rec. Twenty Fifth IEEE Photovolt. Spec. Conf. - 1996* 53–55 (IEEE, 1996). doi:10.1109/PVSC.1996.563944

50. Hageman, P. R. *et al.* Large area, thin film epitaxial lift off III/V solar cells. in *Conf. Rec. Twenty Fifth IEEE Photovolt. Spec. Conf. - 1996* 57–60 (IEEE, 1996). doi:10.1109/PVSC.1996.563945

51. Green, M. A., Emery, K., Hishikawa, Y., Warta, W. & Dunlop, E. D. Solar cell efficiency tables (version 44). *Prog. Photovoltaics Res. Appl.* **22,** 701–710 (2014).

52. Tatavarti, R. *et al.* Lightweight, low cost InGaP/GaAs dual-junction solar cells on 100 mm epitaxial liftoff (ELO) wafers. in *2009 34th IEEE Photovolt. Spec. Conf.* 002065–002067 (IEEE, 2009). doi:10.1109/PVSC.2009.5411455

53. Tatavarti, R. *et al.* InGaP/GaAs/InGaAs inverted metamorphic (IMM) solar cells on 4″ epitaxial lifted off (ELO) wafers. in *2010 35th IEEE Photovolt. Spec. Conf.* 002125–002128 (IEEE, 2010). doi:10.1109/PVSC.2010.5616004

54. Sheng, X. *et al.* Printing-based assembly of quadruple-junction four-terminal microscale solar cells and their use in high-efficiency modules. *Nat. Mater.* **13,** 593–8 (2014).

55. Ganapati, V., Ho, C.-S. & Yablonovitch, E. Intermediate Mirrors to Reach Theoretical Efficiency Limits of Multi-Bandgap Solar Cells. (2014). at <http://arxiv.org/abs/1406.3126>

56. Schumacher, H. *et al.* High-speed InP/InGaAs photodiode on sapphire substrate prepared by epitaxial lift-off. *IEEE Trans. Electron Devices* **36,** 2625 (1989).

57. Yang, C.-D. *et al.* Investigation of epitaxial lift-off the InGaAs p–i–n photodiodes to the AlAs/GaAs distributed Bragg reflectors. *Solid. State. Electron.* **47,** 1763–1767 (2003).

58. Kobayashi, F. & Sekiguchi, Y. GaAs Schottky Photodiode Fabricated on Glass Substrate Using Epitaxial Lift-Off Technique. *Jpn. J. Appl. Phys.* **31,** L850–L852 (1992).

59. Windisch, R. *et al.* Light-emitting diodes with 31% external quantum efficiency by outcoupling of lateral waveguide modes. *Appl. Phys. Lett.* **74,** 2256 (1999).

60. Corbett, B., Considine, L., Walsh, S. & Kelly, W. M. Resonant cavity light emitting diode and detector using epitaxial liftoff. *IEEE Photonics Technol. Lett.* **5,** 1041–1043 (1993).

61. Yablonovitch, E., Kapon, E., Gmitter, T. J., Yun, C. P. & Bhat, R. Double heterostructure GaAs/AlGaAs thin film diode lasers on glass substrates. *IEEE Photonics Technol. Lett.* **1,** 41–42 (1989).

62. Pollentier, I., Buydens, L., Van Daele, P. & Demeester, P. Fabrication of a GaAs-AlGaAs GRIN-SCH SQW laser diode on silicon by epitaxial lift-off. *IEEE Photonics Technol. Lett.* **3,** 115–117 (1991).

63. Mi, Z. & Bianucci, P. When self-organized In(Ga)As/GaAs quantum dot heterostructures roll up: Emerging devices and applications. *Curr. Opin. Solid State Mater. Sci.* **16,** 52–58 (2012).

64. Shah, D. M. *et al.* Epitaxial lift-off GaAs HEMT's. *IEEE Trans. Electron Devices* **42,** 1877–1881 (1995).

65. Young, P. G., Alterovitz, S. A., Mena, R. A. & Smith, E. D. RF properties of epitaxial lift-off HEMT devices. *IEEE Trans. Electron Devices* **40,** 1905–1909 (1993).

66. Pollentier, I., Brys, C., Demeester, P., van Daele, P. & Martens, L. Transplantation of epitaxially lifted-off MESFETs fabricated by a commercial foundry: operation and reliability. *Electron. Lett.* **29,** 291 (1993).

67. Thomas Morf Charlotte, C. B. W. B. Effects Of Epitaxial Lift Off On The Dc, Rf And Thermal Properties Of Mesfets On Various Host Materials.

68. Fan, J. C., Lee, C. P., Hwang, J. A. & Hwang, J. H. AlGaAs/GaAs Heterojunction Bipolar Transistors on Si substrate using epitaxial lift-off. *IEEE Electron Device Lett.* **16,** 393–395 (1995).

69. Lee, K., Zimmerman, J. D., Xiao, X., Sun, K. & Forrest, S. R. Reuse of GaAs substrates for epitaxial lift-off by employing protection layers. *J. Appl. Phys.* **111,** 033527 (2012).

70. Notten, P. H. L., Meerakker, J. E. A. M. & Kelly, J. J. *Etching of III-V semiconductors: an electrochemical approach*. 349 (Elsevier Advanced Technology, 1991).

71. Campbell, S. A. & Lewerenz, H. J. *Semiconductor Micromachining, Fundamental Electrochemistry and Physics*. 332 (Wiley, 1998)

72. Costescu, R. M., Deneke, C., Thurmer, D. J. & Schmidt, O. G. Rolled-Up Nanotech: Illumination-Controlled Hydrofluoric Acid Etching of AlAs Sacrificial Layers. *Nanoscale Res. Lett.* **4,** 1463–8 (2009).

73. Heijna, M. C. R., Theelen, M. J., van Enckevort, W. J. P. & Vlieg, E. Spherulitic growth of hen egg-white lysozyme crystals. *J. Phys. Chem. B* **111,** 1567–73 (2007).

74. Dai, Q., Hu, J. & Salmeron, M. Adsorption of Water on NaCl (100) Surfaces: Role of Atomic Steps. *J. Phys. Chem. B* **101,** 1994–1998 (1997).

75. Woodhouse, M. & Goodrich, A. a manufacturing cost analysis relevant to single and dual junction photovoltaic cells fabricated with III-Vs and III-Vs grown on Czochralski Silicon. *NREL Rep. No. PR-6A20-60126* 92 (2014).

76. Shahrjerdi, D. *et al.* Ultralight High-Efficiency Flexible InGaP/(In)GaAs Tandem Solar Cells on Plastic. *Adv. Energy Mater.* **3,** 566–571 (2013).

77. Lauro, P. A. *et al.* Kerf-Less Removal of Si, Ge, and III-V Layers by Controlled Spalling to Enable Low-Cost PV Technologies. *IEEE J. Photovoltaics* **2,** 141–147 (2012).

78. Shahrjerdi, D. & Bedell, S. W. Extremely flexible nanoscale ultrathin body silicon integrated circuits on plastic. *Nano Lett.* **13,** 315–20 (2013).

79. Chen, P. Integration of III-V materials with silicon for optoelectronic integrated circuit applications. (2008).

80. Archer, M. J. *et al.* GaInP/GaAs dual junction solar cells on Ge/Si epitaxial templates. *Appl. Phys. Lett.* **92,** 103503 (2008).

81. Kang, D. *et al.* Carbon-doped GaAs single junction solar microcells grown in multilayer epitaxial assemblies. *Appl. Phys. Lett.* **102,** 253902 (2013).

82. Choi, W. *et al.* A Repeatable Epitaxial Lift-Off Process from a Single GaAs Substrate for Low-Cost and High-Efficiency III-V Solar Cells. *Adv. Energy Mater.* (2014). doi:10.1002/aenm.201400589

Chapter III

Cold-Welding and Epitaxial Protection Layers

In this chapter, we introduce two unique technologies that makes the non-destructive epitaxial lift-off (ND-ELO) process possible: bonding and wafer recycling. Cold-welding directly bonds the epi-layer onto the host substrate. Cold-welding is an adhesive-free solid-state welding method between two similar and smooth metal surfaces that only requires pressure under ambient conditions. This process simplifies the conventional ELO by eliminating additional transfer processes. The second technology is the use of epitaxial protection layers. The combination of multiple lattice-matched epitaxial layers inserted in between the wafer and sacrificial layer can preserve the substrate surface during the ELO process and the layers can be simply removed by wet-etching to recover the epi-ready surface quality comparable or even better than the original substrate. Hence, the use of protection layers enables the recycling of the parent wafer without degrading the quality of epi-layers grown multiple times on it. The combination of these two key technologies with conventional ELO provides an opportunity to overcome the cost barrier for the various compound semiconductor-based thin-film optoelectronic devices.

3.1 Introduction

Unlike the standard thin-film fabrication processes based on solution and deposition techniques such as chemical vapor deposition (CVD), sputtering, and evaporation that grow an active region directly on the host substrate, epitaxial lift-off (ELO) requires a bonding process to transfer the thin active region from the parent wafer to the handle or the flexible host substrate.[1,2] In conventional ELO, the lifted-off layers are typically attached to flexible secondary handles using adhesives such as thermal releasing tape, wax, or glue.[2,3] These adhesives can be bulky, heavy, brittle, and subject to degradation, while they require an additional transfer following the separation of the epitaxy onto an intermediate "handle". To eliminate the need for adhesives and the intermediate handle transfer, we attach the epitaxial surface directly to the final flexible substrate by using a cold-weld bond by applying pressure across the two surfaces to be bonded.[4,5] Furthermore, we develop a thermally-assisted cold-welding process that applies heat in addition to pressure under vacuum and thus, the pressure generally required for cold-weld bonding is dramatically reduced from 50 MPa to 4 MPa.[6]

Furthermore, transferring the device active region from the original wafer to a host substrate via ELO provides a potential to reuse the parent substrate and enables the fabrication of optoelectronic devices on the flexible substrate. To avoid the use of chemo-mechanical polishing (CMP) that consumes tens of micrometers of material from the top surface of the wafer[7,8], we employ lattice-matched protection layers that protect the wafer surface from the dilute HF during the ELO process.[6,9] Here we demonstrate the protection layers schemes for both InP and GaAs substrates to preserve their surface qualities during ELO. Combination of the cold-weld bonding and protection layers is hereafter used for non-destructive ELO (ND-ELO) as a bonding and wafer recycling process described in the following chapters of this thesis.

3.2 Cold-weld bonding process

Cold-weld bonding is a particularly promising direct-attachment technique for attaching metal layers associated with an ELO process. Figure 3.1(a) shows a schematic illustration of cold-weld bonding process that can be performed under the ambient conditions by only the application of pressure. Figure 3.1(b) shows a tool (Alliance RT/100, MTS) used for cold-weld bonding in this work.

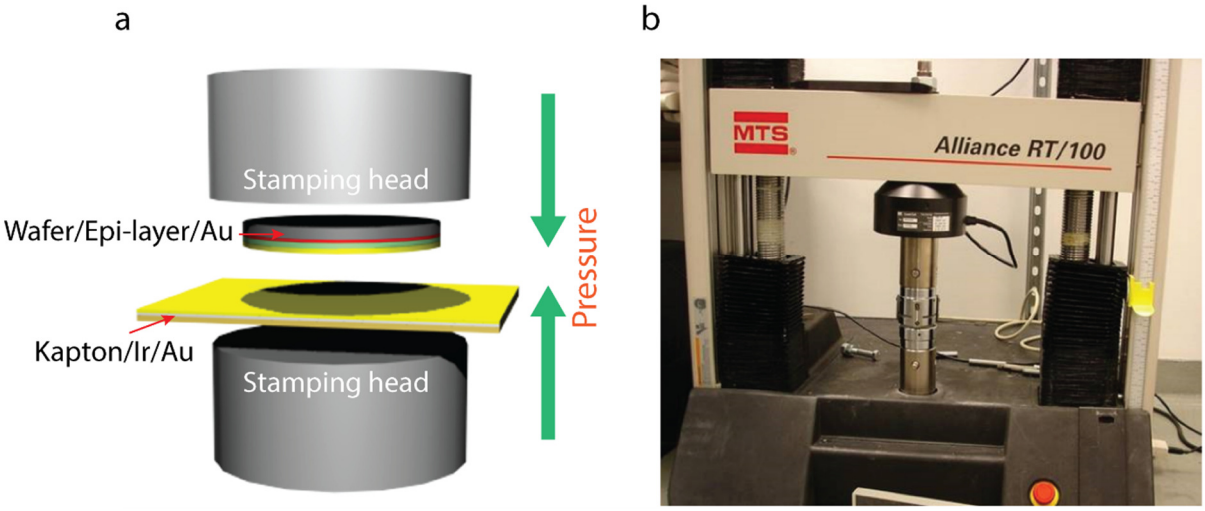


Fig. 3.1: Cold-welding process (a) Schematic illustration of cold-welding process to bond the between Au coated wafer and flexible substrate under the ambient condition (b) Photograph of a bonding tool (Alliance RT/100, MTS).

Conventional cold-welding is simple compared with the fusion-based techniques since it only requires a pressure for bonding between two similar metal surfaces. However, a major disadvantage of cold-welding at room temperature is that it requires relatively high pressure to form a uniformly bonded interface[5,10]. Therefore, the sample can be easily damaged by a non-

uniform pressing force or defects on the sample surface (dusts, point defects, dislocations etc.) which reduces device fabrication yield and prevents wafer reuse.

Thermocompression bonding can be an alternative metal-metal bonding, requiring a much lower pressure, but at a temperature higher than the metal re-crystallization temperature.[11,12] Application of this technique to plastic-based flexible electronics is limited due to its high processing temperature, since plastic substrates have a lower glass-transition or melting temperature than the metal re-crystallization temperature. Also, due to the mismatch of coefficients of thermal expansion between the plastic and semiconductor materials, a high amount of stress can be induced during the bonding process. Therefore, thermocompression is not appropriate for bonding semiconductors to plastic handles.

We developed a method to bond a semiconductor wafer to plastic substrates that uses a much lower pressure compared to cold-welding, as well as lower temperature and shorter bonding duration than thermocompression bonding. This technique takes advantage of plastic deformation of gold which requires a temperature below the re-crystallization temperature.[13] In addition, the relatively low elastic modulus of the plastic substrate facilitates the boding process and is further reduced by heat[14] that helps to bond Au-Au interfaces at a much lower pressure.[15] Running the process under vacuum assists the bonding process.[16,17] Table 3.1 compares the process parameters of cold-welding, thermally-assisted cold-welding and thermocompression bonding processes.

Table 3.1 Comparison between cold-welding, thermally-assisted cold-welding and thermocompression bonding

	Pressure	**Time**	**Temperature**	**Base Pressure**
Cold-welding	**50 MPa**	1 min	Room temp.	Atmosphere
Thermally-assisted cold-welding	**4 MPa**	3 min	175 ℃	~10^{-5}
Thermocompression bonding	**~2 MPa**	20~45 mins	Above 260 ℃	-

The Au-Au metallic bonding for ELO by cold-welding or thermally-assisted cold-welding is advantageous for several reasons. First, Au is chemically robust to HF so that it can form a chemically robust bond between the thin film layers and the handle substrate during the ELO. Second, Au conveniently acts as a back contact if deposited directly on a highly doped *n* or *p* type semiconductor layer or is combined with the appropriate metal at the interface by forming a metal alloy (e.g. Pd/Ge/Au for ohmic contact with n-type GaAs at low temperature). Third, Au, has a high reflectance in the near IR wavelength region, and hence can act as a rear side mirror to increase photon trapping.[18,19] Fourth, Au can be combined with the strained materials, such as Ir, Ni, and NiFe, to expedite the ELO process. Lastly, it is insensitive to oxidation that can increase the pressure needed to form the cold-weld bond.

To perform the cold-weld bonding, the surface of both a rigid wafer and a flexible substrate are pre-coated with similar noble metals. In this work, a 10 nm-thick Ir adhesion layer is sputtered on a Kapton® sheet. The Ir layer provides tensile strain to the substrate that significantly reduces the wafer and substrate separation time (~5 hrs) by more than 90% and 35 % when compared with the ELO process without the Ir layer (~2 days) and the surface tension-assisted ELO process (~8 hrs)[20], respectively. Next, a 350 nm-thick Au layer is simultaneously

deposited on both sample surfaces to produce the cold-weld bonding interface. Cold-weld bonding is performed under vacuum (~10^{-5} Torr) with an applied force of 4 MPa at a stage temperature of 175 ℃. The process allows for a ~92% reduction in bonding pressure in comparison to conventional room temperature cold-welding under ambient conditions. Figure 3.2 shows a photograph of lifted-off GaAs thin film layers from fresh and reused substrates which are cold-weld bonded onto a Kapton® substrate.

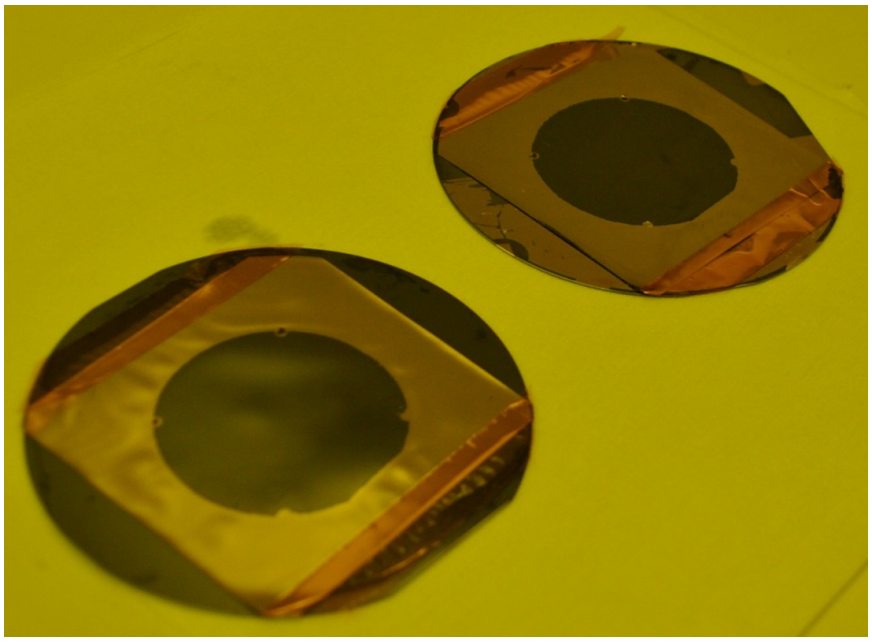


Fig. 3.2: ELO processed 2 inch diameter GaAs thin-film after bonded onto plastic substrate via thermally-assisted cold-weld bonding under vacuum. (Lifted-off from fresh wafer (left) and reused-wafer (right))

Figure 3.3(a) shows detailed procedures for thermally-assisted cold-weld bonding. The process combined with vacuum, heat and a soft graphite pad allows for a significantly lower pressure (4 MPa) than conventional cold-welding (50 MPa for the same area bonding). Additionally, it requires a lower temperature and shorter duration than conventional thermo-

compression bonding (above 260 ℃/ 20~45min). Figure 3.3(b) shows a bonding tool (EAG 520) used for thermally-assisted cold-weld bonding process in this work.

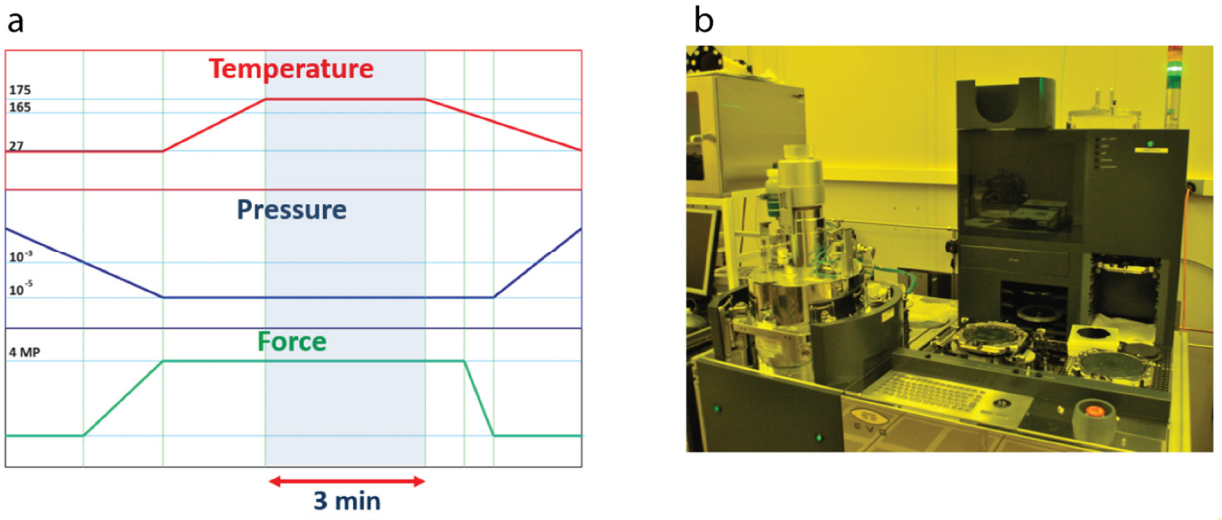


Fig. 3.3: Thermally-assisted cold-welding process (a) Detailed bonding procedure including stage temperature, chamber pressure and applied force vs. time. (b) Photograph of bonding tool (EAG 520) used in this work.

3.3 Epitaxial protection layer

The ELO process is a promising method to create a thin-film device by transferring the device active region from the wafer to lightweight and flexible host substrate. After the ELO process, it is essential to recycle the parent substrate in subsequent epitaxial growths to reduce the device production cost. However, prior attempts to recycle the parent substrate have either resulted in reduced device efficiency or it required a CMP process of the wafer by removing the top several micrometers of material.[7]

To allow for reuse of the wafer while avoiding loss of material, we developed a layer scheme for both InP and GaAs substrates to protect the wafer surface from dilute HF during the

ELO etch process. The protection layers include the growth buffer, etch-stop, and protection layers in between the substrate and the AlAs sacrificial layer. The protection layers generally comprise lattice matched epitaxial layers to minimize defect generation. Each comprising layer has high etching selectivity with adjacent epi-layers so that it can be easily removed by wet-etching that halts at the interface with the next layer in the stack. Figure 3.4(a) and (b) show protection layer structures for both InP and GaAs substrates. The primary function of the top layer is to provide an etch stop against the ELO etch. The etch stop layer underneath the top protection layer should allow for an abrupt smooth etch stop when removed for regrowth on top of it. A second aspect of etch stop layer is that it helps remove debris from the surface that may remain after the attempted removal of top protection layer.

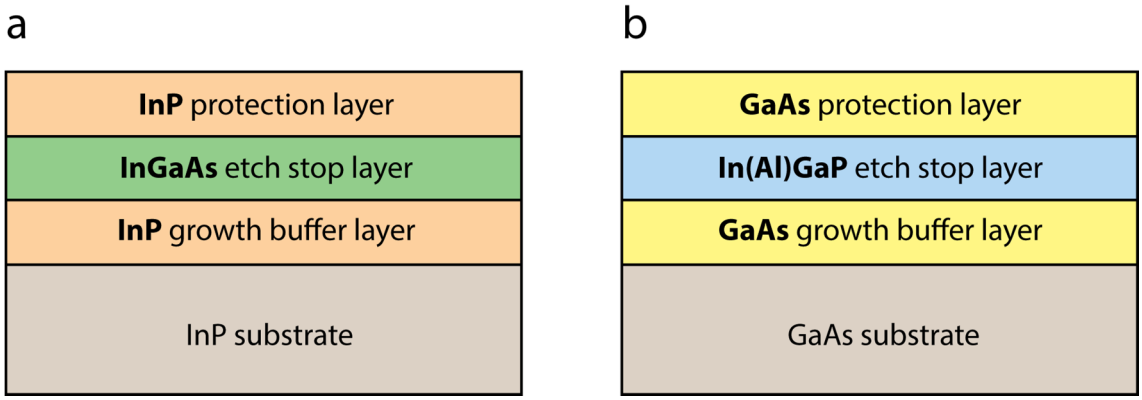


Fig. 3.4: Epitaxial protection layers schemes. (a) InGaAs/InP and (b) In(Al)GaP/GaAs protection layers employed for non-destructive ELO process to preserve the InP and GaAs wafer surface quality, respectively, from the dilute HF.

As briefly described above, the major reason for employing double protection layers is to provide a clean epi-ready surface, since the selectivity between AlAs sacrificial layer and other III-V compounds materials to HF is finite.[21] Therefore, the protection layer may react with HF, creating residues and other damage that are very difficult to completely remove; additional

protection layers can be added to separately remove the residues and allow for the proper etch chemistries, and place the optimal material adjacent to the AlAs lift off layer, providing the best surface fidelity. It should be noted that the protection layer scheme is not only limited to the bi-layer structure, but can be a relatively thick single layer or triple layers etc. with various material combinations. Table 3.2 shows a summary of protection layers and selective etchants employed for ND-ELO process. Etch stop layers provide very high etching selectivity with substrate to provide high quality surface after their removal.

Table 3.2 Summary of protection layers and selective etchant

	On InP wafer		**On GaAs wafer**	
	Epi-layer	Etchant	Epi-layer	Etchant
Protection layer	InP	H_3PO_4:HCl (1:3)	GaAs	H_3PO_4:H_2O_2:H_2O (3:1:25)
Etch stop layer	InGaAs	H_2SO_4:H_2O_2:H_2O (1:1:10) : Selectivity ~80[22] + Citric acid: H_2O_2 (20:1) : Selectivity ~470[22]	GaInP (AlGaInP)	HCl:H_2O (1:1) : Selectivity >10^6 [23]

Lattice mismatched epi-layers can also be employed as a protection layers. While lifting off the InP layers, it was found that the InP surface is exposed to the HF etchant for over a week without degradation[5]; however, GaAs exposed to HF for as short as two days can develop a residue or surface contamination, making it very difficult to recover the original surface quality, rendering wafer reuse almost impossible. We expect that by placing a thin layer of strained InP

adjacent to the AlAs sacrificial layer can improve the robustness of the ELO process. The InP layer can be thinner than the strain relaxation thickness (~1.7 nm)[24] or it may be thicker, as we have been able to use ~10 nm of strained AlAs on InP (the same strain value, but opposite sign as for this situation) for liftoff of InP-based devices (see Chapters 4 and 5) without noticeable degradation to the surrounding device layers.

Detailed methods and characterizations for wafer recycling using epitaxial protection layers are discussed for InP and GaAs substrates in Chapter 4 and 6, respectively. In addition, the effectiveness of these structures is experimentally confirmed by demonstrating multiple thin-film optoelectronic devices lifted-off from a single InP or GaAs wafer without systematic performance degradation.

3.4 Conclusion

In summary, we introduced cold-welding and epitaxial protection layer concepts to bond the wafer onto a flexible thin foil and to preserve the wafer surface quality during ELO process, respectively. The cold-welding of active device regions directly onto permanent host substrates eliminates the need for complicated transfer processes. The use of protective epitaxial layers in between the sacrificial layer and the wafer results in a chemically and morphologically preserved wafer surface, allowing for its continuous recycling without the need for costly CMP process. Hence, these two key technologies contribute to simplified and potentially low cost fabrication of multiple compound semiconductor-based thin-film optoelectronic devices from a continuously reused wafer, while maintaining the consistent performance across the devices.

CHAPTER III

Bibliography

1. Konagai, M., Sugimoto, M. & Takahashi, K. High efficiency GaAs thin film solar cells by peeled film technology. *J. Cryst. Growth* **45,** 277–280 (1978).

2. Yablonovitch, E., Gmitter, T., Harbison, J. P. & Bhat, R. Extreme selectivity in the lift-off of epitaxial GaAs films. *Appl. Phys. Lett.* **51,** 2222 (1987).

3. Cheng, C.-W. *et al.* Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics. *Nat. Commun.* **4,** 1577 (2013).

4. Kim, C., Burrows, P. & Forrest, S. Micropatterning of organic electronic devices by cold-welding. *Science* **288,** 831–3 (2000).

5. Lee, K., Shiu, K.-T., Zimmerman, J. D., Renshaw, C. K. & Forrest, S. R. Multiple growths of epitaxial lift-off solar cells from a single InP substrate. *Appl. Phys. Lett.* **97,** 101107 (2010).

6. Lee, K., Zimmerman, J. D., Hughes, T. W. & Forrest, S. R. Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics. *Adv. Funct. Mater.* **24,** 4284–4291 (2014).

7. Bauhuis, G. J. *et al.* Wafer reuse for repeated growth of III-V solar cells. *Prog. Photovoltaics Res. Appl.* **18,** 155–159 (2010).

8. Adams, J. *et al.* Demonstration of Multiple Substrate Reuses for Inverted Metamorphic Solar Cells. *IEEE J. Photovoltaics* **3,** 899–903 (2013).

9. Lee, K., Zimmerman, J. D., Xiao, X., Sun, K. & Forrest, S. R. Reuse of GaAs substrates for epitaxial lift-off by employing protection layers. *J. Appl. Phys.* **111,** 033527 (2012).

10. Shiu, K.-T., Zimmerman, J., Wang, H. & Forrest, S. R. Ultrathin film, high specific power InP solar cells on flexible plastic substrates. *Appl. Phys. Lett.* **95,** 223503 (2009).

11. Froemel, J. *et al.* Investigations of thermocompression bonding with thin metal layers. *2011 16th Int. Solid-State Sensors, Actuators Microsystems Conf.* 990–993 (2011). doi:10.1109/TRANSDUCERS.2011.5969495

12. Antle, W. Friction Technique for Optimum Thermocompression Bonds. *IEEE Trans. Compon. Parts* **11,** (1964).

13. Bellosi, A., Kosmac, T. & Tomsia, A. P. *Interfacial Science in Ceramic Joining*. (1997).

14. Davidson, M., Bastian, S. & Markley, F. Measurement of the Elastic Modulus of Kapton Perpendicular to the Plane of the Film at Room and Cryogenic Temperatures. in *Fourth Annu. IISSC Conf. New Orleans, LA, March 4-6, 1992* (1992).

15. Ferguson, G. S., Chaudhury, M. K., Sigal, G. B. & Whitesides, G. M. Contact adhesion of thin gold films on elastomeric supports: cold welding under ambient conditions. *Science* **253,** 776–778 (1991).

16. Tabor, D., Pashley, M. D. & Pethica, J. B. Adhesion and micromechanical properties of metal surfaces. *Wear* **100,** 7–31 (1984).

17. Tabor, D. Friction - The present state of our understanding. *J. Lubr. Technol.* **103,** 169–179 (1981).

18. Miller, O. D., Yablonovitch, E. & Kurtz, S. R. Strong Internal and External Luminescence as Solar Cells Approach the Shockley–Queisser Limit. *IEEE J. Photovoltaics* **2,** 303–311 (2012).

19. Bauhuis, G. J., Mulder, P., Haverkamp, E. J., Huijben, J. C. C. M. & Schermer, J. J. 26.1% thin-film GaAs solar cell using epitaxial lift-off. *Sol. Energy Mater. Sol. Cells* **93,** 1488–1491 (2009).

20. Cheng, C.-W. *et al.* Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics. *Nat. Commun.* **4,** 1577 (2013).

21. Smeenk, N. J. *et al.* Arsenic Formation on GaAs during Etching in HF Solutions: Relevance for the Epitaxial Lift-Off Process. *ECS J. Solid State Sci. Technol.* **2,** P58–P65 (2012).

22. DeSalvo, G. C. Etch Rates and Selectivities of Citric Acid/Hydrogen Peroxide on GaAs, $Al_{0.3}Ga_{0.7}As$, $In_{0.2}Ga_{0.8}As$, $In_{0.53}Ga_{0.47}As$, $In_{0.52}Al_{0.48}As$, and InP. *J. Electrochem. Soc.* **139,** 831 (1992).

23. Hjort, K. Sacrificial etching of III - V compounds for micromechanical devices. *J. Micromechanics Microengineering* **6,** 370–375 (1996).

24. Matthews, J. Defects in epitaxial multilayers I. Misfit dislocations. *J. Cryst. Growth* **27,** 118–125 (1974).

Chapter IV

Thin-Film InP Solar Cells and Wafer Reuse

In this chapter, we demonstrate multiple growths of flexible, thin-film indium tin oxide-InP Schottky-barrier solar cells on a single InP wafer via epitaxial lift-off (ELO). Layers that protect the InP parent wafer surface during the ELO process are subsequently removed by selective wet-chemical etching, with the active solar cell layers transferred to a thin, flexible plastic host substrate by cold welding at room temperature. The first- and second-growth solar cells exhibit no performance degradation under simulated AM 1.5G illumination, and have power conversion efficiencies of η_p=14.4±0.4% and η_p=14.8±0.2%, respectively. The current-voltage characteristics for the solar cells and atomic force microscope images of the substrate indicate that the parent wafer is undamaged, and is suitable for reuse after ELO and protection-layer removal processes. X-ray photoelectron spectroscopy, reflection high-energy electron diffraction observation and 3D surface profiling show a comparable or improved surface following ELO. Wafer reuse over multiple cycles suggests that high-efficiency, single-crystal thin-film solar cells may provide a practical path to low-cost solar-to-electrical energy conversion.

4.1 Introduction

Epitaxial lift-off (ELO), in which the active region of an electronic device structure is separated from its parent substrate and then transferred to a different host substrate, is attractive for cost reduction of III-V thin film solar cells by re-using the original, and costly substrate[1,2,3,4,5,6]. However, wafer reuse has been limited by the increased wafer surface roughness caused by wet-chemical etching during ELO. Although chemo-mechanical polishing is a reliable method to restore the surface smoothness[7,8], the procedure removes some of the substrate material and has the potential for damaging its edges; consequently, the number of substrate re-uses and the concomitant reduction in production cost is limited. Here, we employ epitaxial protection layers for both the substrate and the lifted-off thin film to provide a high quality regrowth surface without polishing. By combining ELO with cold welding to transfer the epitaxial solar cells to a thin, flexible plastic sheet[5,9,10,11,12], we demonstrate re-use of the original substrate for fabricating efficient indium tin oxide (ITO)-InP Schottky-barrier thin-film solar cells[13] without loss of device performance. Power conversion efficiencies approaching η_p=15% are achieved.

4.2 Background

The Schottky-barrier diode is a device based on rectifying metal-semiconductor contacts and is widely employed for solar cells, photodetectors, and the gate electrode of MESFETs, etc. The Schottky-barrier for current rectification is formed at the interface between metal and semiconductor when the metal is directly in contact with the semiconductor. The Schottky-barrier height (ϕ_B) is determined by the band alignment between the work function of the metal (ϕ_m), and the Fermi level of the semiconductor (ϕ_F). For an ideal contact case, the barrier height is mainly

governed by the difference between the work function of metal and the electron affinity (χ) of the semiconductor. This ideal case is never realized in practice, however, mostly due to the presence of an interface layer and defect states.

The interface states are a property of the semiconductor surface and independent of the metal. Especially for III-V compound semiconductors, Schottky-barrier formation is mostly affected by the metal deposition process which generates defects near the interface; therefore, the surface Fermi-level positions are pinned at an energy independent of the metal work function. The dependence of ϕ_B on ϕ_m can be described by the index of interface behavior, S=$d\emptyset_B/dX_M$, where X_M is the electronegativity of the metal. Hence, ϕ_B is expressed as[14]:

$$\phi_B = S(\phi_m - \chi) + (1-S)(E_g - \phi_0) \qquad (4.1)$$

where χ and E_g represent the electron affinity and the bandgap of the bulk semiconductor, respectively. In general, silicon and III-V semiconductors have S < 0.1 which indicates a weak dependence of barrier height with the metal work function, while ionic semiconductors such as II-VI compound semiconductors have S > 0.5.[14]

Schottky-barrier solar cells consist of transparent or semi-transparent metal contacts to a bulk semiconductor. The photocurrent is generated in both depletion and neutral regions, and the current-voltage characteristics of Schottky-barrier cells under illumination are given by[14],

$$I = I_S\left(e^{qV/k_BT} - 1\right) - I_{ph} \qquad (4.2)$$

and

$$I_S = A^{**}T^2 exp\left(-q\,\phi_B/k_BT\right) \qquad (4.3)$$

where n is the ideality factor, A^{**} is the effective Richardson constant, and $q\phi_B$ is the barrier height. Conventional Schottky-barrier solar cells show relatively low performance compared with *p/n* junction solar cells due to limited built-in voltage at the junction. For example, the Schottky-barrier GaAs-based solar cells show PCE < 10 % which is significantly lower than *p/n* junction GaAs solar cells (~28.8 %)[15]. However, ITO-InP Schottky-barrier solar cells show comparable *PCE* (~19 %)[16] with *p-n* junction InP solar cells (~22 %)[17] under 1 sun illumination due to their advantageous Fermi level pining position leading to a higher barrier. A sputtering process for ITO contact formation on top of the *p*-type InP epi-layer inverts the surface doping type into an *n*+ InP layer, therefore it enhances the barrier height which results in a correspondingly high open circuit voltage. This is confirmed by Hall measurements which indicate the existence of an unintentionally doped n^+ layer at the *p*-type InP surface.[18] Furthermore, ITO/InP Schottky-barrier solar cells provide the advantage of a simple fabrication process which only requires metallization to form the ohmic and Schottky-barrier contacts.

4.3 Result and Discussion

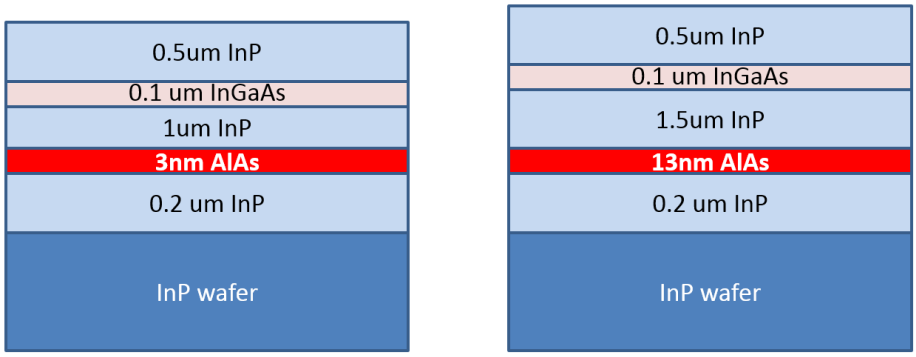
4.3.1 Epitaxial growth

The epitaxial layers were grown, starting with a 0.2 μm thick InP buffer layer, on an S-doped (100) InP substrate by gas source molecular beam epitaxy (GSMBE). Then, a 0.1 μm thick lattice-matched $In_{0.53}Ga_{0.47}As$ etch stop layer, followed by a 1.5 μm thick InP protection layer are grown. At this point, a 10 nm thick AlAs sacrificial layer is grown which is later etched away to separate the active layers from the parent wafer. Next, a second 1.5 μm thick InP protection layer is grown, followed by a 0.1μm thick lattice-matched $In_{0.53}Ga_{0.47}As$ etching stop layer, and then the

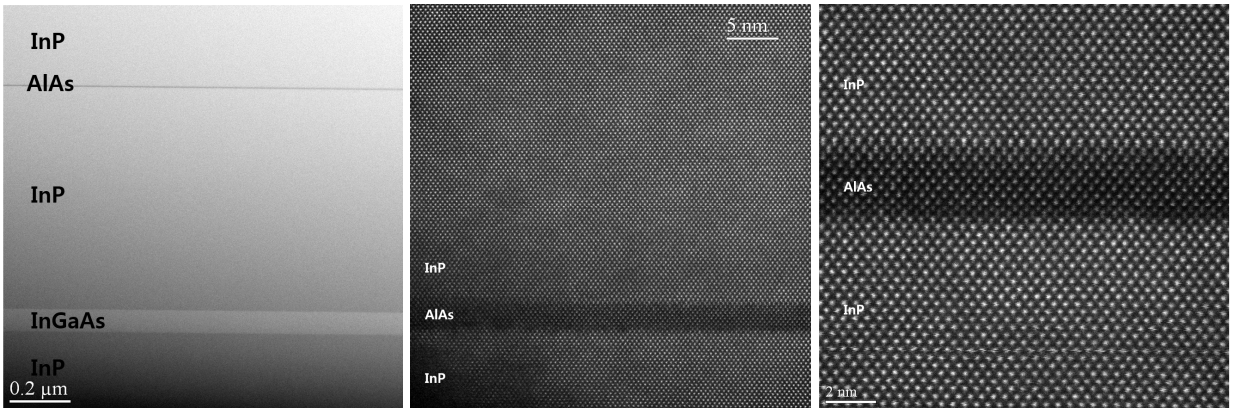
active region consisting of a 3.0 μm thick lightly Be-doped (3×10^{16} cm^{-3}) InP base layer with 0.1 μm thick Be-doped (3×10^{18} cm^{-3}) InP Ohmic contact layer is grown. For the second growth, the InP buffer layer thickness was increased from 0.2 μm to 2 μm to smooth the surface. In all other respects, the first- and second-growth epitaxial structures were identical.

The AlAs (lattice constant of 0.587 nm) that is generally employed as a sacrificial layer for ELO process is known to be lattice-mismatched with the InP (lattice constant of 0.566 nm) which is employed as an active device layer. However, *pseudomorphic* growth of the InP/AlAs heterostructure over the critical thickness of AlAs already has been demonstrated for the resonant tunneling diodes[19] and the tunnel junction for semiconductor laser[20]. To confirm the growth quality of lattice mismatched InP on an AlAs layer, we grew two test structures with 3 nm and 12 nm thick AlAs lattice mismatched layers on an InP substrate (Fig 4.1 (a)). Figure 4.1 (b) and (c) show the cross-sectional, high angle annular dark field images of an InP/AlAs/InP layers at the interface under various resolutions. The cross-sectional, atomic resolution scanning tunneling electron microscope (STEM) images show the nearly perfect crystalline growth without any apparent defects for both samples.

(a)



(b)



(c)

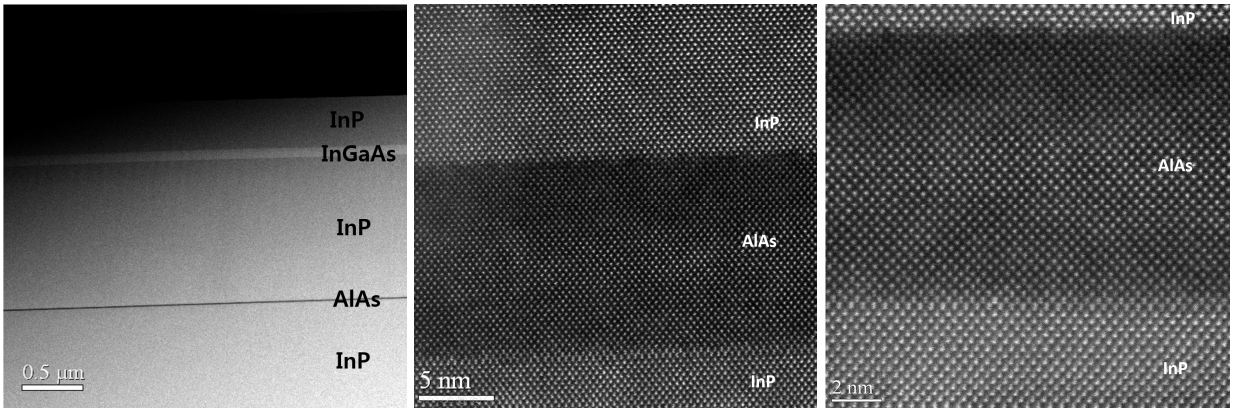


Fig. 4.1: Growth quality of lattice mismatched InP on AlAs layer (a) Test growth structure for InP/AlAs hetrostructure (b) Atomic resolution cross-sectional transmission electron microscope images of the growth interface between the InP and (b) 3 nm thick and (c) 12 nm thick AlAs sacrificial layer with various resolution.

4.3.2 Thin-film InP solar cell fabrication

Immediately following growth, a 100 Å thick Cr adhesion layer followed by a 600 Å Au contact layer were sputtered onto a 50 µm thick Kapton® sheet, and a 600 Å of Au layer was deposited on the highly *p*-doped InP epitaxial layers by electron-beam evaporation.

After metal deposition, the wafer is mounted Au-side down on the plastic sheet and a cold-weld bond[9] is formed by applying a pressure of 10 MPa for 60 s using an MTS Alliance RT/100 Testing system. Then, the Kapton® sheet is affixed to a rotatable, 7.5 cm diameter Teflon rod with Kapton® tape, and immersed into an etching solution of HF:H_2O (1:10). To expedite the ELO process, a 13 g weight is mounted on the plastic substrate, and the Teflon rod is rotated to maintain an external force on the wafer while increasing the gap between the epitaxial layers and substrate as the etching proceeds (Fig.4.2). This ensures that the epilayer/substrate interface will constantly be exposed to fresh etchant throughout the process.

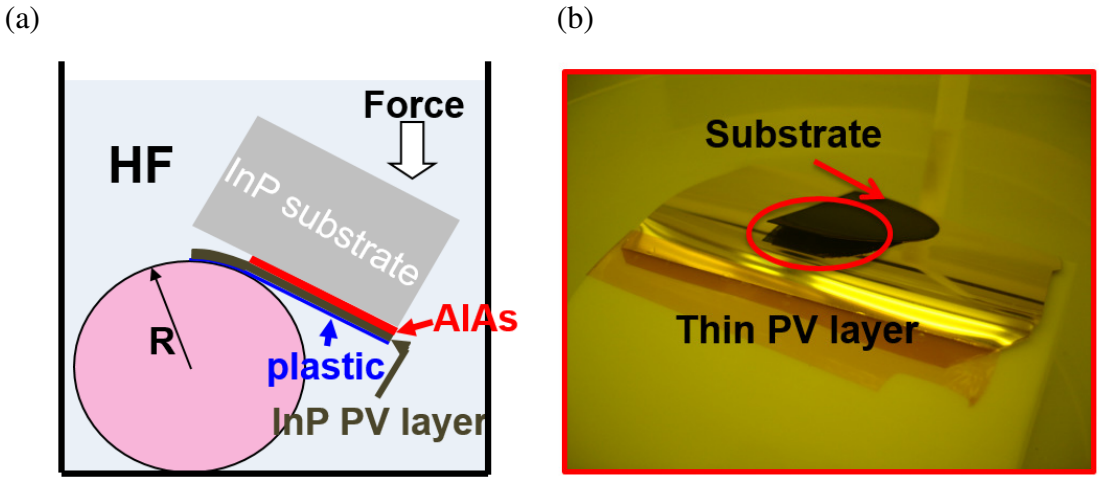


Fig. 4.2: (a) Schematic of weight-induced ELO set-up (b) Image of ELO process for half 2-inch-diameter epitaxial layer.

After completing ELO, the Au residue on the original InP substrate is removed by etching (etchant type TFA, Transene Co.). The InP protection and $In_{0.53}Ga_{0.47}As$ etch-stop layers on both the substrate and solar cell are then selectively removed by etching in H_3PO_4: HCl (1:3) and H_2SO_4: H_2O_2: H_2O (1:1:10), respectively. Subsequently, citric acid:H_2O_2 (20:1) is used to fully remove the remaining $In_{0.53}Ga_{0.47}As$. The freshly exposed InP substrate surface is then degreased by sequential dipping in heated trichloroethylene, acetone, and heated iso-propanol, followed by the intentional growth of an oxide by exposure to UV/ozone for 10 min. The substrate is then loaded back into the GSMBE chamber and degassed. The second photovoltaic cell is then grown on the original parent substrate using the identical procedure described above, followed by a second round of cold welding and ELO.

To fabricate the ITO/InP Schottky junction, exposure to UV/ozone for 7 min removed the surface contaminants and forms a thin, passivating native-oxide.[21] The ITO is sputter-deposited at a rate of 0.3 Å/s through a shadow mask with an array of 1 mm diameter openings. A control, thin-film ITO/InP solar cell cold-welded onto the Kapton® sheet with the same epitaxial structure was fabricated via complete substrate removal, as described previously.[9] Solar cell characterization was carried out under simulated AM1.5G illumination.

4.3.3 Parent substrate cleaning

Selective removal of the protection and etch-stop layers must result in a pristine wafer surface to allow for repetitive use of the parent substrate. Sulfuric acid based solutions have a high etch rate (0.22 μm/min), with a selectivity between $In_{0.53}Ga_{0.47}As$ and InP of 80:1[22]. This etchant results in a 0.17 nm root-mean square (RMS) roughness of the InP substrate after $In_{0.53}Ga_{0.47}As$ removal. In contrast, the citric acid:peroxide etch has higher selectivity (470:1)[22], but nanometer-scale spikes remain after the etching. To minimize the InP surface damage and roughness, and to

eliminate residual $In_{0.53}Ga_{0.47}As$, the sulfuric acid etch was used to remove the majority of $In_{0.53}Ga_{0.47}As$, followed by sonicating in the citric acid etch. The same procedure was employed for $In_{0.53}Ga_{0.47}As$ layer removal from the solar cell epitaxial surface, with 1 min longer exposure to the citric acid solution and without sonication.

Atomic force microscope images (Fig. 4.3 (a)) show that the RMS roughness of the InP surface after $In_{0.53}Ga_{0.47}As$ layer removal following both the first and the second growths (0.16 ± 0.01 nm) is less than that of the epi-ready original InP substrate (0.30 ± 0.02 nm), and the ELO wafer that lacked a protection layer (0.41 ± 0.02 nm).

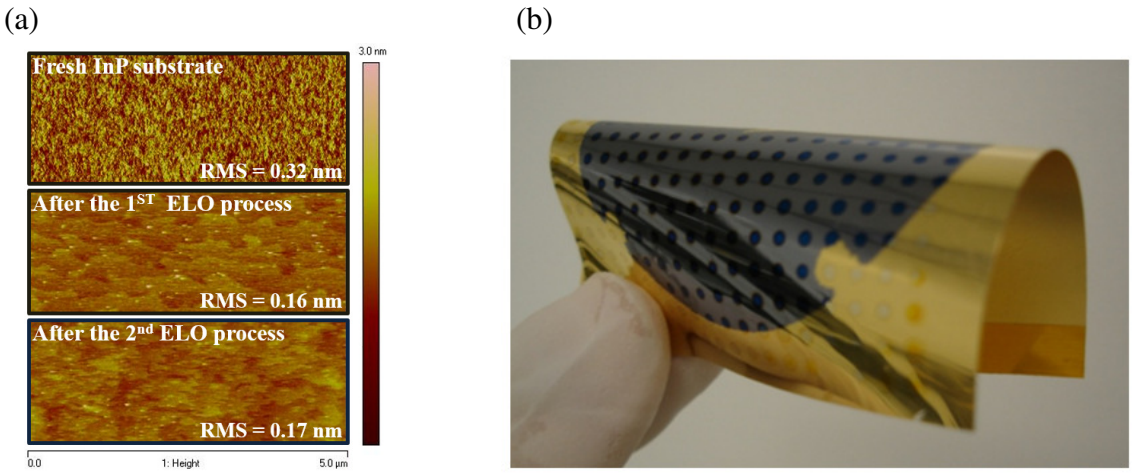


Fig. 4.3: (a) Atomic force microscope images of the surfaces of the original epi-ready InP substrate, recovered InP substrate surface after the first and second epitaxial lift off (ELO) processes following the removal of the protection and etch stop layers, and an ELO surface without the protection layer. (b) Image of lifted-off 2-inch-diameter epitaxial layer containing an array of ITO/InP thin film solar cells fabricated by a combination of ELO and cold-weld bonding to a 50 μm thick Kapton® sheet.

An image of the completed, 2" diameter epilayer with an array of ITO/InP solar cells bonded to the Kapton® substrate is shown in Fig. 4.3 (b). These cells can withstand considerable bending stress without cracking or a degradation in performance.[9]

4.3.4 Characterization of wafer surface quality for wafer recycling

Figure 4.4 shows the X-ray photoelectron spectra that compare the surface elemental compositions of the fresh and ELO-processed substrates following protection layer removal. Both substrates show almost identical In and P peak intensities at the same binding energies, indicating that the surface after ELO has not changed from that of the original, epi-ready InP substrate.

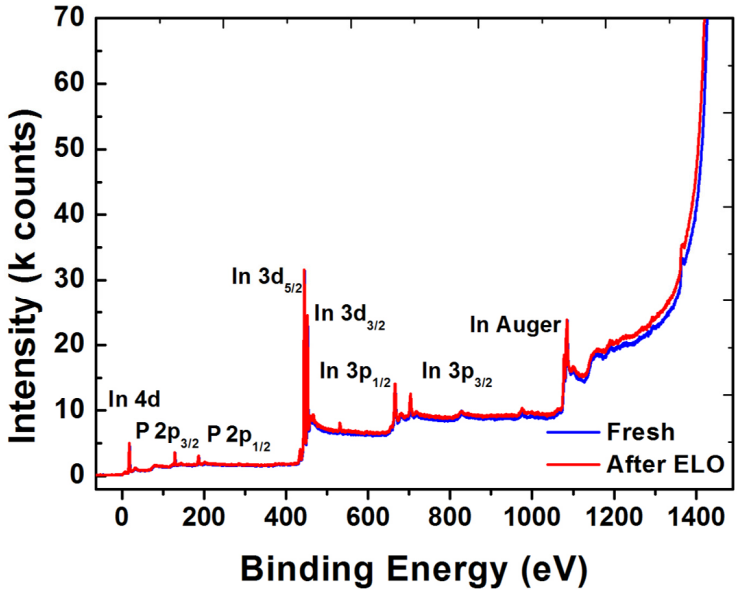


Fig. 4.4: X-ray photoelectron spectra from the fresh and the ELO processed substrate surfaces.

Furthermore, the reflection high-energy electron diffraction patterns obtained from the wafer surface after eliminating the native oxide exhibits the same 2×4 reconstructions as the original wafer (Fig 4.5.). The streaky pattern also indicates that the roughness has not increased on epitaxial layer removal.

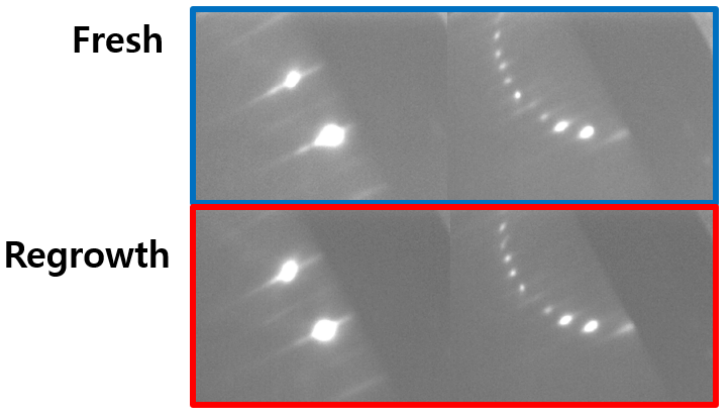


Fig. 4.5: The 2x and 4x surface reconstruction patterns obtained by reflection high-energy electron diffraction for the fresh and the ELO-processed substrate after eliminating oxide layer.

Orange-peel-like roughness was observed on the surface exposed to the ELO etching process in the absence of a protection layer. This is apparent from the 3D surface profiles in Fig. 4.6 that compare the millimeter-scale surface morphology between ELO processed substrate with and without the protection layer. The surface images confirm the necessity of employing the protection layer to ensure that the regrowth surface is flat on both the macro- and nano-scales.

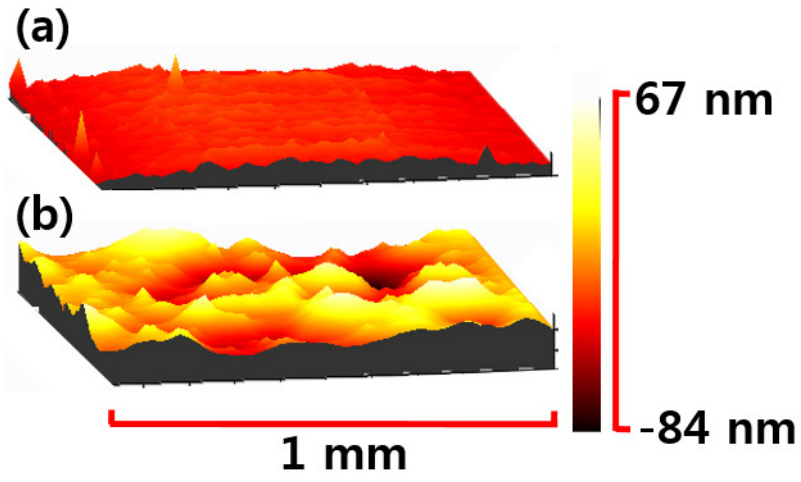


Fig. 4.6: Surface morphology of the original substrate (a) after ELO and protection layer removal and (b) after the ELO without the protection layer.

4.3.5 Comparison of device performance

The fourth quadrant current density-voltage (*J-V*) characteristics of the first and the second ELO processed photovoltaic cells, and the control device measured under simulated AM1.5G illumination at 1 sun (100 mW/cm^2) intensity are compared in Fig. 4.7. The characteristics are nearly identical for all devices (see Table 4.1). The reverse-bias dark current density (J_D) at -1 V for the control cell is lower than that of either of the ELO cells, as also listed in Table 4.1. However, there is not a systematic increase in dark current with the number of ELO steps employed, indicating that these differences are due to run-to-run variations in the ITO/InP Schottky barrier formation process rather than from systematic differences in the epitaxial layer quality. This is confirmed by the minor differences in the forward characteristics that are apparent in Fig. 4.7.

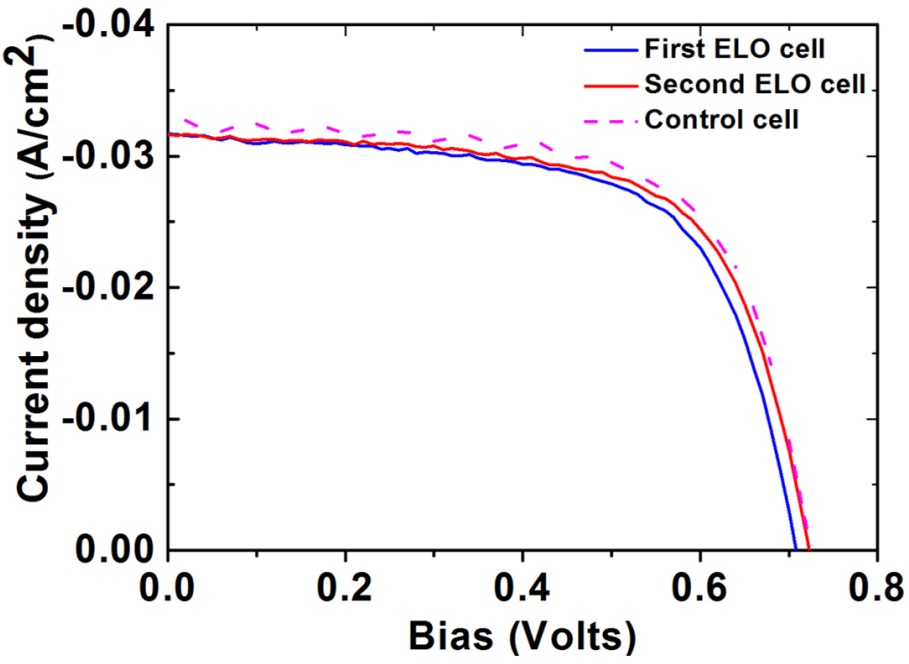


Fig. 4.7: Current density versus voltage characteristics of the first and the second ELO processed ITO/InP and the control solar cells bonded to a Kapton® sheet, all measured under 1 sun, AM1.5G simulated solar illumination.

Slight variations in Schottky barrier height and J_D are observed for different ITO sputtering depositions and for different positions on the sample holder. The ideality factors (n) and specific series resistances (R_S) are extracted using the Shockley equation modified to include R_S,

$$J = J_0(e^{\frac{q(V-IR_S)}{nk_BT}} - 1) + \frac{V - JR_S}{R_P} \qquad (4.4)$$

where J_0 is the reverse bias saturation current, q is the electron charge, V is applied voltage, k_B is the Boltzmann constant, T is temperature and R_P is specific parallel resistance.[14] The first- and the second-growth solar cells exhibit no systematic performance loss under 1 sun intensity, with η_p=14.4% and 14.8%, respectively. A compilation of J_D, n, R_S, J_{sc}, V_{oc}, FF, and η_p is provided in Table 4.1.

Table 4.1: Comparison of device performances under AM1.5G simulated solar spectrum, and the dark current at -1V (J_D), ideality factor (n) and specific series resistance (R_s) in the dark.

	J_D (μA/cm^2)	n	R_s (Ω-cm^2)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	η_p (%)
Previous work[a]	1.6	1.14	5.4	29.6±2.9	0.62	55	10.2±1.0
Control cell	0.6	1.66	0.7	31.2±1.0	0.71	64.3±2.0	14.6±0.3
1st ELO cell	128	1.87	0.5	31.8±0.1	0.70	64.4±1.9	14.4±0.4
2nd ELO cell	17	1.71	0.7	31.3±0.3	0.71	66.1±0.3	14.8±0.2

[a] Ref. 9

The significant improvement in device performance compared with previous reports of InP solar cells prepared by total substrate removal[12] primarily results from the increased V_{oc} and FF due to the improved ITO/InP interface. To reduce the contact surface damage, a higher ITO sputtering power has been combined with the UV/ozone treatment to form a thin oxide passivation and surface protection layer. The increased sputtering power also leads to an increase in ITO conductivity.

4.4 Conclusion

In summary, we have demonstrated the fabrication of ITO/InP thin-film solar cells sequentially grown multiple times on a single InP parent substrate. After each growth, the epilayers were removed by ELO, and then cold-weld bonded at room temperature to a thin, flexible plastic sheet. The performance of the first- and second-growth and control epitaxial cells were characterized and compared. The optimized fabrication processes lead to similar performance for both ELO processed and control cells, with η_p=14.4±0.4%, 14.8±0.2% and 14.6±0.3%, respectively. Furthermore, including protective epitaxial layers reduces the RMS surface roughness of the parent wafer, while resulting in a chemically equivalent surface, allowing for its continued re-use without the need for potentially damaging mechanical polishing. Hence, this work demonstrates a reduced-cost fabrication method for ITO/InP thin-film solar cells based on continuous reuse of a single substrate without the loss of device performance.

CHAPTER IV

Bibliography

1. Yablonovitch, E., Gmitter, T., Harbison, J. P. & Bhat, R. Extreme selectivity in the lift-off of epitaxial GaAs films. *Appl. Phys. Lett.* **51,** 2222 (1987).

2. Bauhuis, G. J., Mulder, P., Haverkamp, E. J., Huijben, J. C. C. M. & Schermer, J. J. 26.1% thin-film GaAs solar cell using epitaxial lift-off. *Sol. Energy Mater. Sol. Cells* **93,** 1488–1491 (2009).

3. Yoon, J. *et al.* GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies. *Nature* **465,** 329–333 (2010).

4. Demeester, P., Pollentier, I., Dobbelaere, P. De, Brys, C. & Daele, P. Van. Epitaxial lift-off and its applications. *Semicond. Sci. Technol.* **8,** 1124–1135 (1993).

5. Lee, K., Zimmerman, J. D., Hughes, T. W. & Forrest, S. R. Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics. *Adv. Funct. Mater.* **24,** 4284–4291 (2014).

6. Smeenk, N. J. *et al.* Arsenic Formation on GaAs during Etching in HF Solutions: Relevance for the Epitaxial Lift-Off Process. *ECS J. Solid State Sci. Technol.* **2,** P58–P65 (2012).

7. Bauhuis, G. J. *et al.* Wafer reuse for repeated growth of III-V solar cells. *Prog. Photovoltaics Res. Appl.* **18,** 155–159 (2010).

8. Adams, J. *et al.* Demonstration of Multiple Substrate Reuses for Inverted Metamorphic Solar Cells. *IEEE J. Photovoltaics* **3,** 899–903 (2013).

9. Shiu, K.-T., Zimmerman, J., Wang, H. & Forrest, S. R. Ultrathin film, high specific power InP solar cells on flexible plastic substrates. *Appl. Phys. Lett.* **95,** 223503 (2009).

10. Kim, C., Burrows, P. & Forrest, S. Micropatterning of organic electronic devices by cold-welding. *Science* **288,** 831–3 (2000).

11. Ferguson, G. S., Chaudhury, M. K., Sigal, G. B. & Whitesides, G. M. Contact adhesion of thin gold films on elastomeric supports: cold welding under ambient conditions. *Science* **253,** 776–778 (1991).

12. Plößl, A. Wafer direct bonding: tailoring adhesion between brittle materials. *Mater. Sci. Eng. R Reports* **25,** 1–88 (1999).

13. Li, X., Wanlass, M. W., Gessert, T. A., Emery, K. A. & Coutts, T. J. High-efficiency indium tin oxide/indium phosphide solar cells. *Appl. Phys. Lett.* **54,** 2674 (1989).

14. Sze, S. M. & Ng, K. K. in *Phys. Semicond. Devices, 3rd Ed. John Wiley Sons, Inc.; NJ* 164, 682 (2007). doi:10.1002/9780470068328.fmatter

15. Green, M. A., Emery, K., Hishikawa, Y., Warta, W. & Dunlop, E. D. Solar cell efficiency tables (version 44). *Prog. Photovoltaics Res. Appl.* **22,** 701–710 (2014).

16. Coutts, T. J. & Naseem, S. High efficiency indium tin oxide/indium phosphide solar cells. *Appl. Phys. Lett.* **46,** 164 (1985).

17. Keavney, C. J., Haven, V. E. & Vernon, S. M. Emitter structures in MOCVD InP solar cells. in *IEEE Conf. Photovolt. Spec.* 141–144 (IEEE, 1990). doi:10.1109/PVSC.1990.111606

18. Tsai, M.-J., Fahrenbruch, A. L. & Bube, R. H. Sputtered oxide/indium phosphide junctions and indium phosphide surfaces. *J. Appl. Phys.* **51,** 2696 (1980).

19. Sugiyama, H. *et al.* InP-based strained In/sub 0.8/Ga/sub 0.2/As/AlAs resonant tunneling diodes with high peak-current density and large peak-to-valley current ratio grown by metal-organic vapor-phase epitaxy. in *Int. Conf. onIndium Phosphide Relat. Mater. 2003.* 211–214 (IEEE, 2003).

20. Sekiguchi, S., Miyamoto, T., Kimura, T., Koyama, F. & Iga, K. Self-aligned current confinement structure using AlAs/InP tunnel junction in GaInAsP/InP semiconductor lasers. *Appl. Phys. Lett.* **75,** 1512 (1999).

21. Raring, J. W., Skogen, E. J., Denbaars, S. P. & Coldren, L. A. A study of regrowth interface and material quality for a novel InP-based architecture. *J. Cryst. Growth* **273,** 26–37 (2004).

22. DeSalvo, G. C. Etch Rates and Selectivities of Citric Acid/Hydrogen Peroxide on GaAs, $Al_{0.3}Ga_{0.7}As$, $In_{0.2}Ga_{0.8}As$, $In_{0.53}Ga_{0.47}As$, $In_{0.52}Al_{0.48}As$, and InP. *J. Electrochem. Soc.* **139,** 831 (1992).

Chapter V

Conformal thin-film *p-i-n* InGaAs photodiode array with external quantum efficiency approaching 100%

Compound semiconductor based photodiodes provide extremely high performance over elemental semiconductors due to their intrinsically superior material properties; however, their applications have been mostly limited onto planar substrates due to the difficulties of crystal growth and device fabrication on a conformal structure. Here, we develop a method to transfer thin-film InGaAs *p-i-n* photodiode arrays from a rigid and bulky substrate onto a flexible and lightweight plastic sheet via epitaxial lift-off (ELO) and cold-welding technology. The ELO processed 10 × 10 pixel photodiode array shows approximately 100 % external quantum efficiency (EQE) at 1300 nm wavelength using a light trapping structure with 100 % fabrication yield. The unique feature of extremely high performance photodiode arrays integrated on a flexible or conformal substrate provides a practical path to meet countless imaging applications.

5.1 Introduction

InGaAs photodiodes offer high sensitivity and speed with low noise over a spectral range from ~900 nm to ~1700nm which is ideal for optical communication and near infrared (NIR) detection. Among their wide variety of applications, *p-i-n* InGaAs focal plane arrays (FPA)

provide excellent performance as a NIR and shortwave IR (SWIR) range imager which makes them widely employed in night vision and thermal inspection applications. However, these high performance SWIR imagers have been limited to the planar structures, which provide a limited field-of-view (FOV) smaller than 40 degree solid angle. To extend the FOV of the imager, photodiode arrays formed on a conformal structures such as a hemisphere is a possible solution.[1,2]

In this work, we employed the epitaxial lift-off (ELO) process and cold-weld bonding to fabricate a *p-i-n* thin-film InGaAs photodiode array on a flexible substrate. The ELO process enables the production of thin-film optoelectronic devices by separating the active device region from the substrate.[3,4] The lifted-off and transferred thin-film photodiode array onto a flexible substrate can be transformed into a conformal shape to expand the FOV, which is difficult to achieve with a planar photodiode array. Furthermore, very high external quantum efficiency (EQE) can be achieved with a relatively thin active device region by using an integrated rear-side metal reflector to form a light trapping structure.

The EQE at -1V of a thin-film *p-i-n* InGaAs photodiode fabricated on a flexible substrate shows as high as 82%, 99%, 99%, and 88% at 980nm, 1300nm, 1480nm, and 1550nm wavelength, respectively. These results confirm a comparable or even better performance of thin-film InGaAs photodiode arrays under the small reverse bias compared to conventional bulky substrate-based InGaAs photodiode arrays with identical device structures. Moreover, the previously demonstrated non-destructive ELO (ND-ELO) process provides a potential for significant device production cost reduction by recycling the parent InP substrate multiple times.[4,5] The above combination of merits makes thin-film flexible photodiode arrays highly promising in low-cost, high performance, large-FOV imaging applications, which is far beyond current state of art.

5.2 Result and discussion

5.2.1 Epitaxial growth

The epitaxial structure and fabrication flow of an ELO processed thin-film *p-i-n* InGaAs photodiode array is illustrated in Figure 5.1(a)-(d). The epitaxial structure consists of the sequential growth of sacrificial and active device layers in inverted order. A 200 nm InP buffer layer is grown by gas source molecular beam epitaxy (GSMBE) on a 2 inch diameter 350 μm thick (100) InP wafer followed by 4 nm thick AlAs sacrificial layer. Since the lattice mismatch between AlAs epi-layer and InP substrate creates ~3.5% strain, the critical thickness of pseudomorphically growing AlAs on an InP substrate is only ~2 nm.[6] Hence, the AlAs layer needs to be grown as thin as possible to reduce defects generated by the mismatched epi-layer growth in the following active device layers. However, an AlAs sacrificial layer thinner than 4 nm exhibits a dramatic decrease in etch rate, which prohibits the completion of the ELO process. Consequently, we employed a 4 nm thick AlAs sacrificial layer in this work. Next, a 200 nm thick degenerately Zn doped p^+-InP window layer is grown, followed by a 2.1 μm thick unintentionally doped *i*-InGaAs active absorption layer and a 100 nm thick Si-doped n^+-InGaAs contact layer growth. The active device region is grown in inverted order such that after bonding to the host substrate and lifted off from the parent InP substrate, devices can be fabricated into conventional *p-i-n* top illumination photodiode structure.

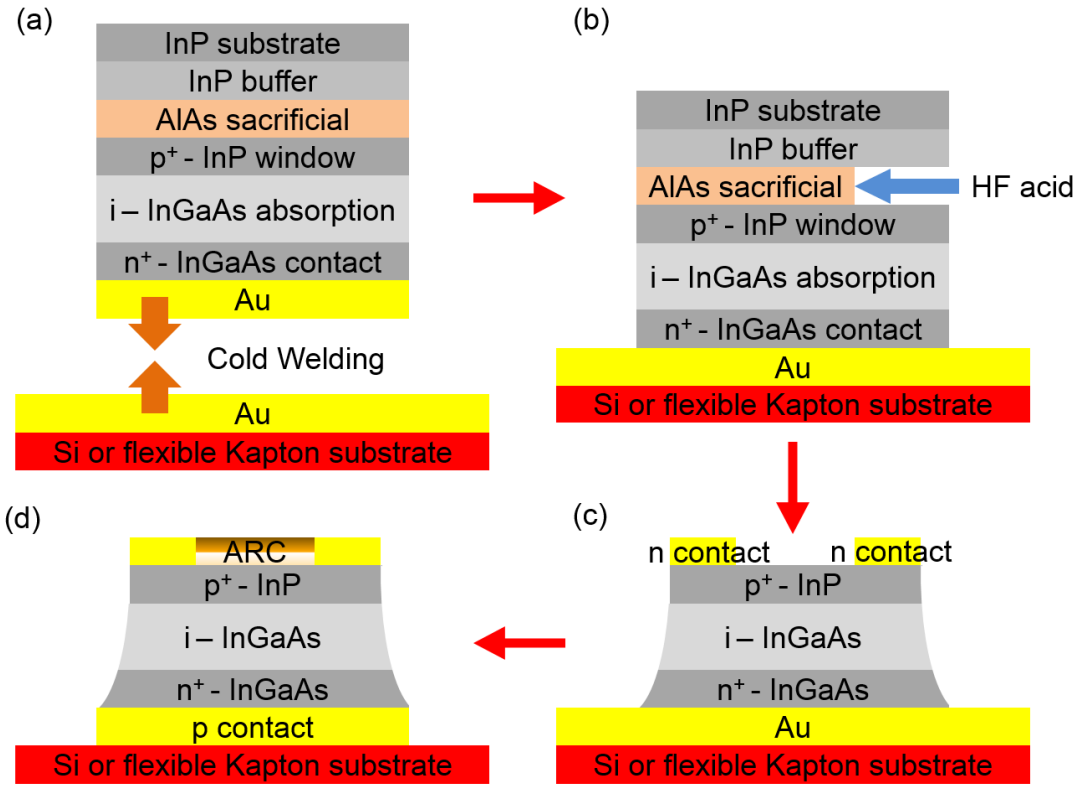


Fig. 5.1: Schematic of fabrication flow of p-i-n thin-film photodiode, showing that **(a)** the device epi-growth structure and the cold-welding process to bond the epi-sample onto a host substrate; **(b)** the epitaxial lift-off process to separate the active device region from the parent InP substrate, transferring the thin-film photodiode epi-layers to the host substrate; **(c)** the front contact patterning and mesa defining process to make *p-i-n* InGaAs photodiode mesas on the host substrate; and **(d)** the back contact patterning and top bi-layer anti-reflection coating (ARC) deposition process to finish the fabrication.

5.2.2 Cold-weld bonding and epitaxial lift-off

After growth, the epi-wafer is diced into 4mm × 4mm squares using an ADT 7100 dicing saw. Subsequently, the surface native oxide of epi-samples is removed by dipping them into buffered HF for 1 minute and rinsing in DI water for 10 seconds. Immediately after the surface oxide removal, 0.5 nm Ir followed by 300 nm Au are deposited on both epi-samples and a host

substrate using e-beam evaporation. Then, Au films on the epi-samples and host substrate are cold-weld bonded using an EVG 510 wafer bonder with the application of heat and pressure immediately after Au deposition. The bonding is performed under ~10^{-5} torr vacuum with an applied pressure of 20 MPa and the stage temperature of 240 °C for 8 minutes. To ensure uniform force is applied over the sample, a soft graphite sheet is inserted between the sample and the metal press head of the bonder. Once the InP substrate is bonded to the host substrate, the epitaxial thin-film active device region is separated from the parent InP substrate through ELO process. The entire sample is immersed into 16% HF acid that is maintained at 45 °C, and stirred at a speed of 400 rpm using a magnetic stir bar. Due to the high etch selectivity between AlAs and the active device layers, dilute HF only removes the AlAs sacrificial layer without damaging the adjacent epitaxial thin-film active device region and InP substrate. The thin-film active device region can be lifted off within 1.5 hours with 4 nm thick AlAs sacrificial layer.

5.2.3 Photodiode array fabrication

A scanning electron microscope (SEM) image of a linearly connected 10×10 photodiode array fabricated on a Kapton substrate is shown in Fig.5.2. The fabrication process is as follows. The front circular contact pad attached to a ring contact is photolithographically patterned using an LOR 3A and S1827 (MicroChem) bi-layer photoresist process. A Ti(20 nm)/ Pt(30 nm)/Au(200 nm) front contact is deposited using e-beam evaporation. The diameter of the circular contact pad is 60 μm. The inner diameter of a ring contact is 100 μm for a single photodiode mesa, defining the top light detection area. The width of the ring contact is 5 μm. After the front contact lift-off, photodiode mesas are defined at the position of the front ring contacts and circular contact pads using plasma etching using Cl_2 (16 sccm) and H_2 (12 sccm) gases with a base pressure of 12 mTorr and an inductively coupled plasma (ICP) power of 600 W. During the plasma etch process, a

forward power of 100 W is applied and the stage temperature is maintained at 0 ℃ with liquid nitrogen. The active device epi-layers are etched at a rate of 500 nm/min. The back Au contact is patterned by wet-etching for 3 minutes using TFA gold etchant. The photodiode mesas are then annealed for 1 minute at 270 °C for ohmic contact formation. Bi-layer anti-reflection coating (ARC) was deposited using e-beam evaporation as a last step of the fabrication process. The target thickness of ARC simulated using a transfer matrix method[7] to maximize the EQE is 40 nm for MgF_2 and 123 nm for TiO_2, and the actual ARC thickness measured by a Woollam M-2000 Ellipsometer is found to be 37 nm for MgF_2 and 127 nm for TiO_2, resulting in 100% transmissivity and 99.9% EQE at 1300 nm light at -1V.

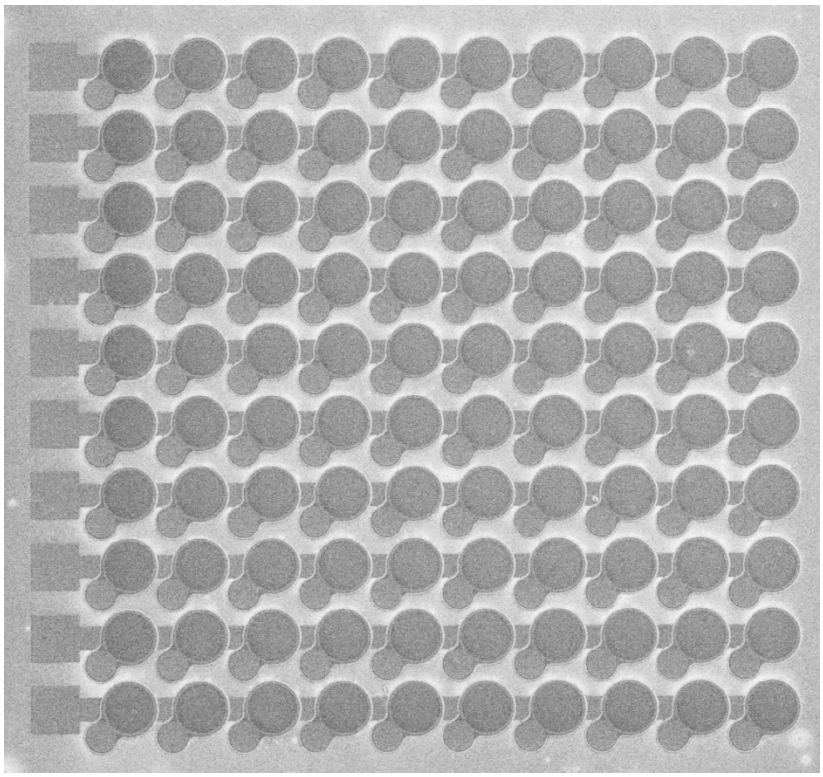


Fig. 5.2: SEM image of linearly connected 10×10 photodiode array fabricated on the lifted-off epi-layers on Kapton host substrate.

5.2.4 Enhanced external quantum efficiency (EQE) via light trapping structure

The external quantum efficiency (EQE), is given by the equation

$$\eta_{ext}(\lambda) = \Theta(\lambda)(1 - e^{-\alpha(\lambda)W}) \tag{5.1}$$

where $\Theta(\lambda)$ is the transmission of light through anti-reflection coating, $\alpha(\lambda)$ is the absorption coefficient of the InGaAs active layer, and W is the absorption path length. The rear-side contact of the ELO-processed photodiode acts as a highly reflective mirror; therefore, the lifted-off thin-film device absorbs additional light reflected back from the rear-side metal reflector compared with a conventional substrate device. With the same InGaAs active layer thickness, the thin-film device doubles the absorption light path, assuming that the rear-side reflector provides a 100% reflectivity. The large index contrast among semiconductor, anti-reflection coating (ARC) and air limits the escape cone of trapped light. Therefore, the solid angle of the escape cone from the semiconductor surface enhances light absorption path even longer than twice the absorption layer thickness by trapping the light inside the active device region. A schematic of light absorption in thin-film devices and substrate devices with and without light trapping is shown in Fig. 5.3.

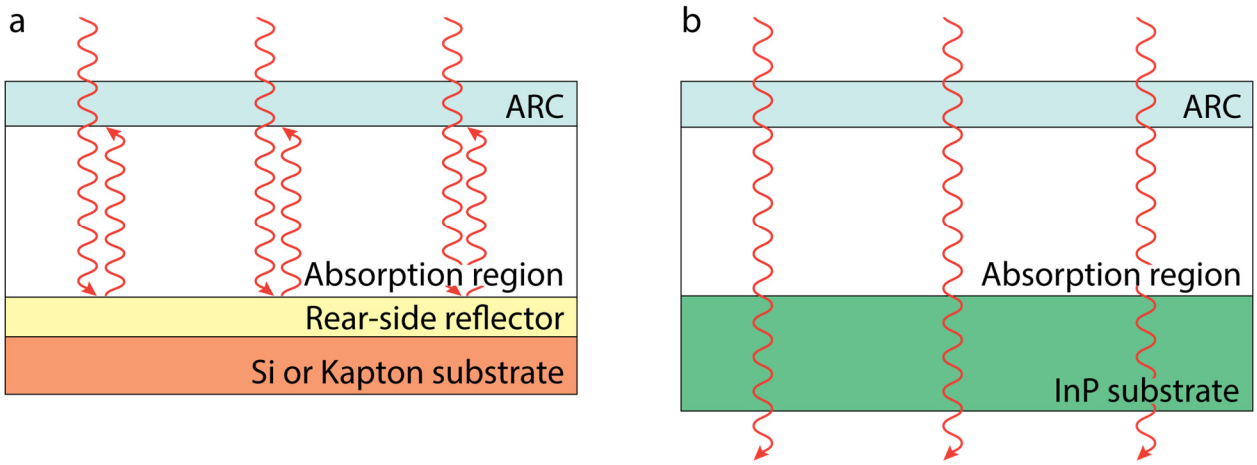


Fig. 5.3: Schematic demonstration of light absorption in (a) thin-film devices and (b) substrate devices with and without light trapping mechanism.

Furthermore, a Fabry-Perot cavity along the light incidence direction, is created within the device due to the rear-side metal reflector. By controlling the bi-layer ARC and InGaAs absorption layer thicknesses, the cavity length can be adjusted to enhance the Fabry-Perot effect and provide $\Theta(\lambda) = 100\ \%$ for λ between 980 nm and 1650 nm. In this work, we demonstrated an anti-reflection coating design which maximizes the response at 1300 nm wavelength, while maintaining $\Theta(\lambda) > 85\ \%$ between λ = 980 nm and 1650 nm. As a result, very high external quantum efficiency (EQE) is achieved over a very wide spectral range. Fig. 5.4 (a) and (b) shows the simulated absorption intensity distribution within a thin-film device (2.1 µm and 0.65 µm thick, respectively), compared with that within a substrate device using transfer matrix method. Comparison of the color contrast at the InGaAs absorption layers of both devices confirms the improved light absorption in the thin-film device. For device with a relatively thin InGaAs active layer (0.7µm), a huge improvement of light absorption in thin-film device is seen from the strong color contrast over the entire simulated wavelength region. For devices with a thicker InGaAs active layer (2.1µm), the absorption at short wavelength region is similar for both thin-film and

substrate-base device; while at long wavelength region, the thin-film device has a stronger absorption due to the Fabry-Perot effect, which overcomes the limitation of the low absorption coefficient at wavelength around band edge.

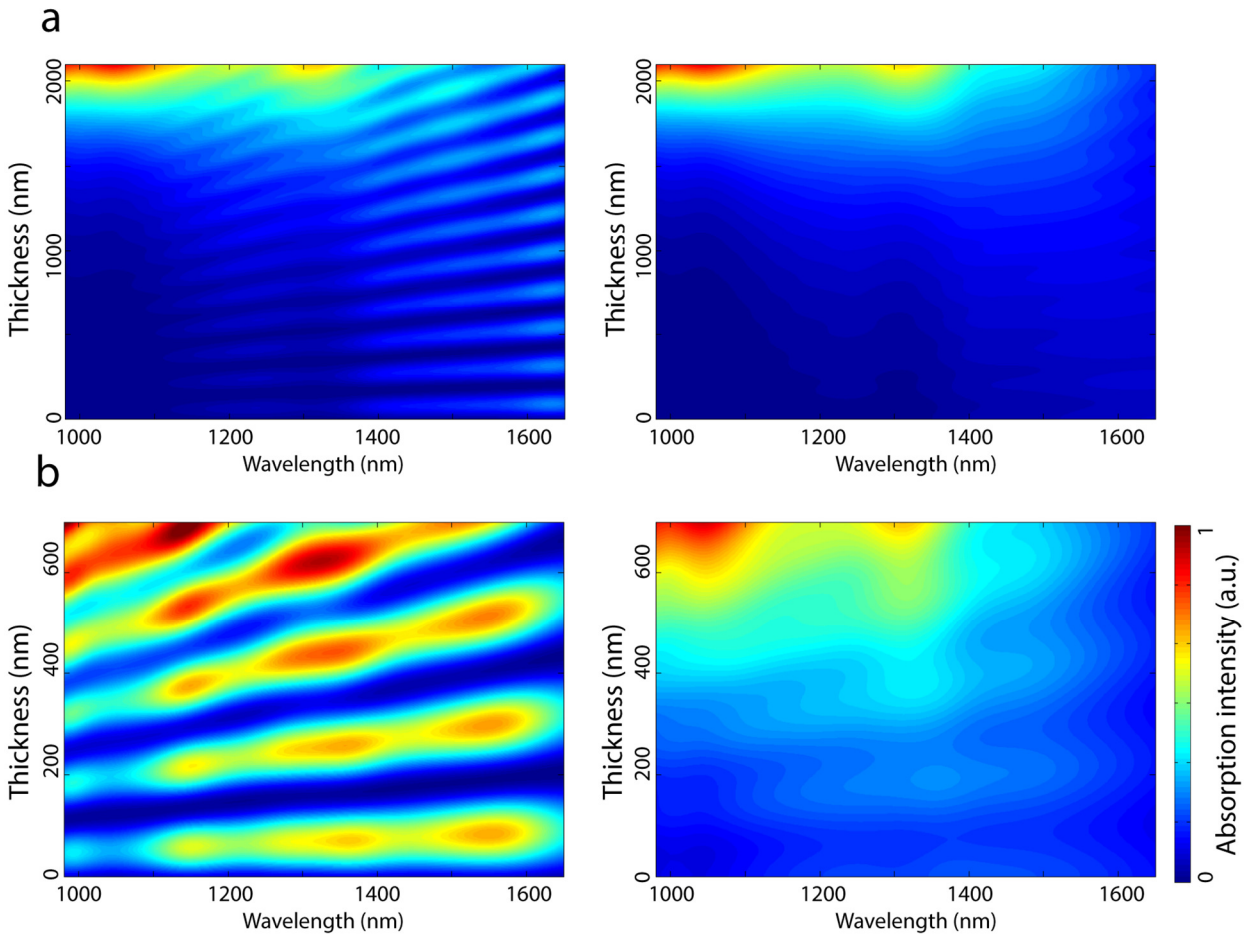


Fig. 5.4: (a) The simulated absorption intensity distribution within a thin-film device (L), compared with that within a substrate device (R). The InGaAs absorption layer thickness is 2.1 μm. (b) The simulated absorption intensity distributions for an absorption layer thickness of 0.7 μm. The bi-layer ARC of MgF_2 (37 nm) and TiO_2 (127 nm) is employed for all simulated structures.

The improvement in EQE performance at -1V bias and 1550 nm wavelength of thin-film devices over substrate devices with different InGaAs absorption layer thicknesses is shown in Fig 5.5.

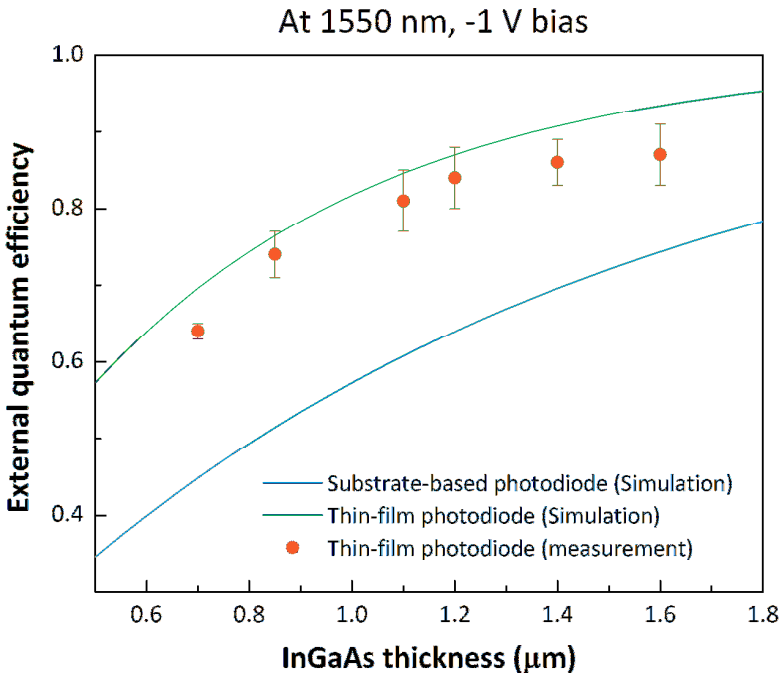


Fig. 5.5: Comparison of simulated and measured EQE performance at -1V bias and 1550 nm wavelength between thin-film devices (green line) and substrate devices (blue line) with different InGaAs absorption layer thicknesses, together with the measured EQE performance of fabricated photodiode devices with different InGaAs absorption layer thickness (orange dots)

In this work, a double layer ARC is employed to enhance light absorption. Given that the refractive index of the top *p*-type InP layer is 3.2 at 1300 nm, the transmissivity of 1300 nm light at normal incidence is only 67% without ARC. To improve the transmissivity, the transfer matrix method is used to design a double layer ARC. According to optical simulation results, 100% transmissivity can be achieved by employing a 40 nm thick MgF_2 layer followed by a 123 nm thick TiO_2 layer at 1300 nm wavelength (Fig. 5.6).

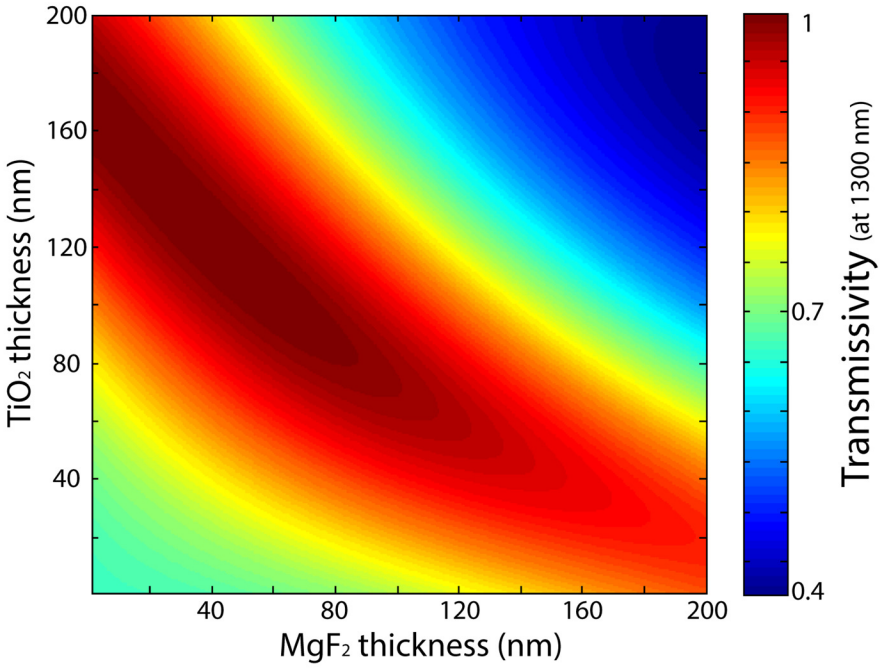


Fig. 5.6: Simulated transmission contour plot of 1300 nm light in-coupled into the photodiode by employing MgF_2 and TiO_2 bi-layer ARC structure with different layer thicknesses. 100% transmission is achieved when 40 nm thick MgF_2 followed by 123 nm thick TiO_2 are employed. 37 nm thick MgF_2 followed by 127 nm thick TiO_2 are measured on actual devices, providing a theoretical value of 99.996% light transmission.

5.2.5 Characterization of thin-film photodiodes

The dark current and EQE at 1550 nm and -1V bias for a photodiode array fabricated on Si and Kapton substrates are demonstrated. The illumination source was a 100 μW 1550 nm laser. As shown in Fig. 5.7(a), the dark currents at -1V bias are 3 nA (current density of 10.6 μA/cm^2) and 4 nA (current density of 14.1 μA/cm^2), and the EQE at -1V bias for 100 μW 1550 nm light illumination is measured to be 88% and 86% for photodiodes fabricated on Si and Kapton substrates, respectively. The simulated EQE spectrum from 980 nm to 1650 nm is shown by the green line in Fig. 5.7(b) together with the measured EQE spectrum at this wavelength regime shown in orange dots. Full spectrum EQE from 980nm to 1650 nm is measured under the

monochromated illumination, which is chopped at 200 Hz and coupled into a SMF-28 optical fiber. The fiber is mechanically guided by a Cascade Microtech Lightwave Probe to achieve normal incidence onto the detection region of the photodiode. The photocurrent generated by the photodiode is amplified by a gain of 10^5 V/A using Keithley 428 Current Amplifier under -1V bias condition. The output signal is then collected by a SR830 Lock-in Amplifier. The light illumination power is calibrated by a Newport 818-IG/DB InGaAs photodetector. As shown in Fig. 5.7(b), the measured EQE values are 82 %, 99 %, and 88 % at 980 nm, 1300 nm, and 1550 nm wavelengths, respectively, which are well matched with the simulated result.

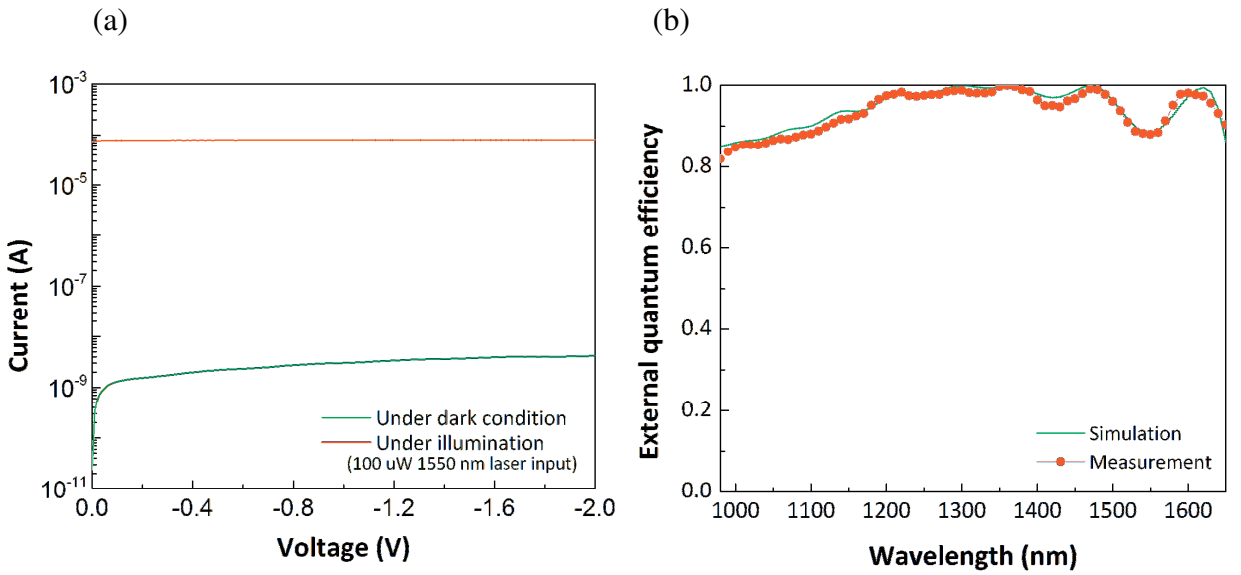


Fig. 5.7: Characterization of thin-film photodiode (a) The I-V characteristic of photodiode under dark (green line) and 100 μW 1550 nm light illumination (orange line) conditions. At -1V bias, the dark current is measured to be 3 nA (current density of 10.6 μA/cm^2), and the EQE for 100 μW 1550 nm light illumination is measured to be 88 % for photodiodes fabricated on a Si substrate. (b) The simulated EQE spectrum (green line) of the photodiode from 980 nm to 1650 nm, together with the measured EQE spectrum at this wavelength regime (orange dots). The measured EQE values are 82 %, 99 %, and 88 % at 980 nm, 1300 nm, and 1550 nm wavelengths, respectively.

The performance of 10×10 photodiode arrays fabricated on both Si and Kapton substrates are shown by mapping the EQE and dark current of all individual photodiodes as shown in Fig. 5.8(a) and (b). The EQE and dark current are measured at -1 V bias with and without 60 μW 1550 nm laser illumination, respectively. The device fabrication yield is 99% for devices fabricated on Si substrate and 100% for devices fabricated on Kapton substrate. The one malfunctioning device on the Si substrate (indicated in white blank at (3,1) in Fig. 5.8(a)) is shorted. Excluding the malfunctioning device, the average EQE at -1V bias and $\lambda = 1550$ nm are 88% and 86% for devices fabricated on Si and Kapton substrate, respectively.

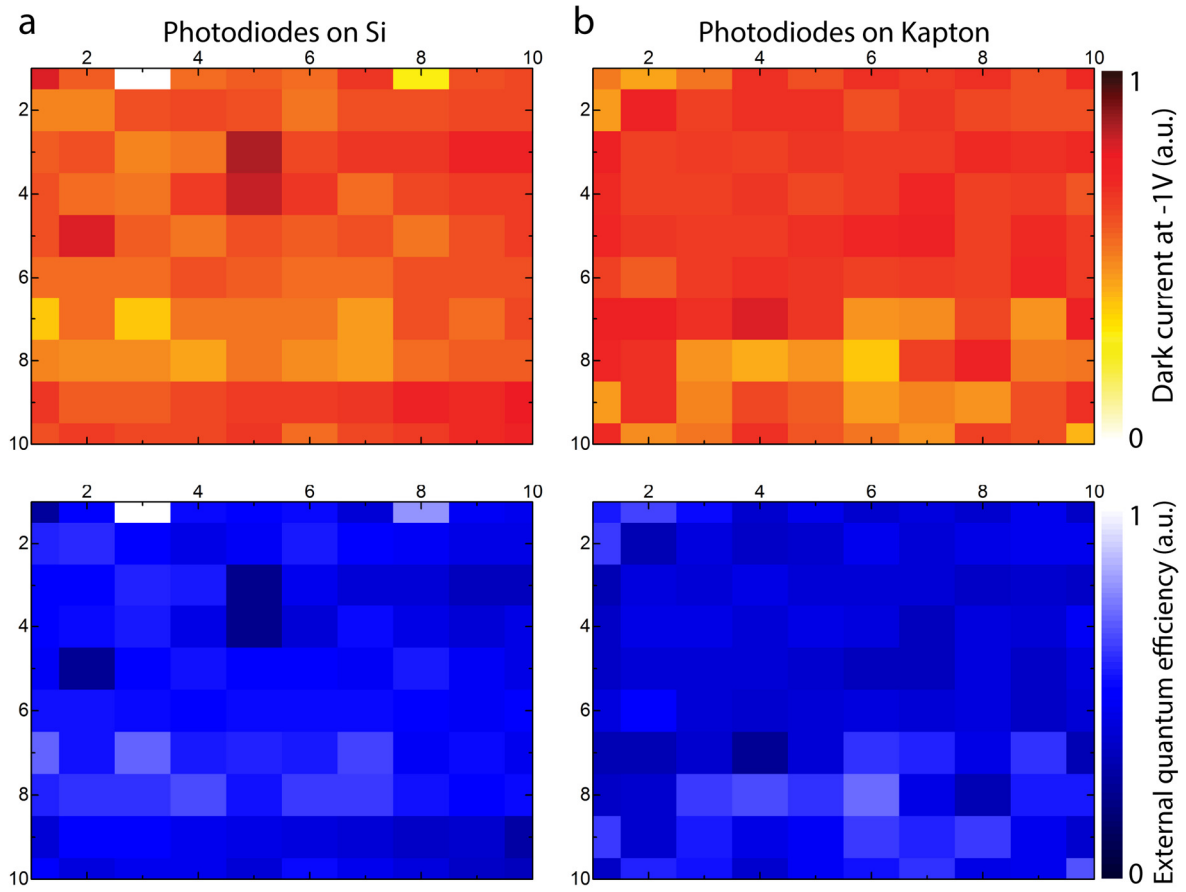


Fig. 5.8: Thin-film device fabrication yield. Dark current (top) and EQE (bottom) mapping of all individual photodiodes showing the fabrication yield of 10×10 thin-film InGaAs photodiode array on (a) Si substrate and (b) Kapton substrate.

Table 5.1 gives a performance comparison between devices fabricated on Si and Kapton substrates at -1 V bias. The dark current, EQE, and yield of devices fabricated on these two substrates are almost identical, showing that the device performance is independent of whether Si or Kapton substrates are used as the host substrate for ELO in the fabrication.

Table 5.1 Device performance comparison between photodiodes fabricated on Si and Kapton substrates under -1 V bias condition.

Host substrate	Dark Current	Dark Current Density	EQE @ 1550nm	Yield
Si	3 ± 0.4 nA	10.6 ± 1.4 μA/cm^2	88%	99%
Kapton	4 ± 0.8 nA	14.1 ± 2.8 μA/cm^2	86%	100%

5.3 Conclusion

In summary, we demonstrate ELO processed *p-i-n* thin-film InGaAs photodiode arrays fabricated on both Si and Kapton substrates. In particular, photodiode arrays fabricated on flexible Kapton substrates that can be conformally shaped to achieve an expanded field of view, overcoming the huge FOV limitation of the conventional substrate-based photodiode array. Thin-film flexible InGaAs photodiodes, employing a rear-side reflector, dramatically enhances the light absorption with a much thinner InGaAs absorption layer, achieving comparable or even better EQE performance compared to a substrate-based InGaAs photodiodes over a wide spectral range. This work represents a technological step providing a practical path for countless imaging applications.

CHAPTER V

Bibliography

1. Xu, X., Davanco, M., Qi, X. & Forrest, S. R. Direct transfer patterning on three dimensionally deformed surfaces at micrometer resolutions and its application to hemispherical focal plane detector arrays. *Org. Electron.* **9,** 1122–1127 (2008).

2. Song, Y. M. *et al.* Digital cameras with designs inspired by the arthropod eye. *Nature* **497,** 95–9 (2013).

3. Konagai, M., Sugimoto, M. & Takahashi, K. High efficiency GaAs thin film solar cells by peeled film technology. *J. Cryst. Growth* **45,** 277–280 (1978).

4. Lee, K., Shiu, K.-T., Zimmerman, J. D., Renshaw, C. K. & Forrest, S. R. Multiple growths of epitaxial lift-off solar cells from a single InP substrate. *Appl. Phys. Lett.* **97,** 101107 (2010).

5. Lee, K., Zimmerman, J. D., Hughes, T. W. & Forrest, S. R. Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics. *Adv. Funct. Mater.* **24,** 4284–4291 (2014).

6. Matthews, J. Defects in epitaxial multilayers I. Misfit dislocations. *J. Cryst. Growth* **27,** 118–125 (1974).

7. Peumans, P., Yakimov, A. & Forrest, S. R. Small molecular weight organic thin-film photodetectors and solar cells. *J. Appl. Phys.* **93,** 3693 (2003).

Chapter VI

Non-Destructive Epitaxial Lift-Off for III-V Thin-Film Optoelectronics

Compound semiconductors are the basis for many of the highest performance optical and electronic devices in use today. Their widespread commercial application has, however, been limited due to the high cost of substrates. Device costs can, therefore, be significantly reduced if the substrate can be reused in a simple, totally non-destructive and rapid process. Here, we demonstrate a method that allows for the indefinite reuse and recycling of wafers, employing a combination of epitaxial "protection layers", plasma cleaning techniques that return the wafers to their original, pristine and epi-ready condition following epitaxial layer removal and adhesive-free bonding to a secondary plastic substrate. We demonstrate the generality of this process by fabricating high performance GaAs-based photovoltaic cells, light emitting diodes, and metal-semiconductor field effect transistors that are transferred, without loss of performance, onto flexible and lightweight plastic substrates, and then the parent wafer is recycled for subsequent growth of additional device layers. Our process leads to a transformative change in, device cost, arising from the inevitable consumption of the wafer that accompanies conventional epitaxial liftoff followed by chemo-mechanical polishing.

6.1. Introduction

Compared to elemental semiconductors such as Si or Ge, compound semiconductors often have superior material properties useful in high performance optoelectronic devices, including high carrier mobilities, direct and indirect band-gap tuning, ability to form heterojunctions that confine optical fields and charge, etc.[1-2]. However, wafers on which compound semiconductor active device regions are epitaxially grown are costly (e.g. GaAs costs ~$20k/m^2), limiting their viability for use in the production of large area devices such as displays and solar cells. Epitaxial lift-off (ELO) was introduced to reduce costs of GaAs/AlGaAs devices by enabling the separation of single crystal active epitaxial layers from fragile and bulky substrates using hydrofluoric acid to selectively remove an AlAs sacrificial layer grown between the substrate and the device layers[3]. The ELO process is also advantageous in that it yields a flexible and lightweight thin film. Unfortunately, the promise of wafer reuse has not been fully realized, since the removal of the sacrificial layer results in residual surface damage, and leaves debris on the parent wafer surface. The most common method for preparing that surface for subsequent growth, therefore, has been by post lift-off chemo-mechanical polishing that reduces wafer thickness and ultimately inflicts additional damage, limiting reuse to only a very few growth and cleaning cycles[4,5].

Recently, ELO using hydrochloric acid as a selective etchant for an AlInP sacrificial layer was introduced for wafer reuse without repolishing[6]. In this case, the process requires a pre-processing step, such as passivation or protection of In-containing layers due their high etching rate in HCl. This complication is required to allow for compatibility with many devices such as high-efficiency multijuction solar cells with InGa(Al)P wide bandgap absorbers, window layers, back-surface field layers, and InGa(Al)P-based light emitting diodes (LEDs). Especially, many of high efficiency GaAs solar cells employed InGa(Al)P based window and back-surface field layers

instead of AlGaAs layer[7]. To ameliorate this issue, we choose to use the HF chemistry-based ELO process, and employ surface protecting layers that can be removed using chemically selective etchants[7,8]. These protection layers comprise alternating lattice-matched arsenide-based and phosphide-based materials that enable recovery of the "epi-ready" wafer surface for regrowth on the original wafer without any observable degradation in surface quality or device performance. In this thesis proposal, we significantly simplify and improve previously reported protection layer schemes, which were previously studied using a simulated ELO process whereby the epitaxial cell was removed and a further device grown on the original substrate. We find here that the number of protection layers can be reduced from three to two by introducing a simple, rapid and potentially low cost two-step surface cleaning procedure[8]. The simplified scheme of non-destructive epitaxial lift-off (ND-ELO) eliminates an interface between materials with different group-V species, whose addition requires temperature changes during growth that increases both the growth time and amount of material used. We find that this scheme of lattice-matched protection layers combined with totally non-destructive surface cleaning is adaptable to a wide range of GaAs and InGa(Al)P-based devices, including photovoltaic cells, transistors, LEDs, and photodetectors, without material composition limitations or the need for damage-inducing wafer polishing commonly used in ELO processes. In this work, we develop a complete technique for non-destructive wafer recycling and thin-film optoelectronic device fabrication. Especially, we focus on characterizing various devices, and comparing their performance to validate the method.

6.2. Experiments

6.2.1 General Structure

The ELO process and a *generalized* epitaxial structure used in non-destructive wafer recycling are illustrated in Figure 6.1. The epitaxial structure consists of the sequential growth of protection, sacrificial and active device layers. The InGaP (50 nm) and GaAs (100 nm) protection and buffer layers are grown by gas source molecular beam epitaxy (GSMBE) on a 2 inch diameter (100) GaAs parent wafer, although this process is fully compatible to growth by other common techniques. An AlAs sacrificial release layer is then grown onto the protection layer stack. Next, the active device region is grown in *inverted* order such that, after bonding to the secondary plastic substrate, devices can be fabricated in their conventional orientation, thereby eliminating a second transfer step often employed in ELO device processing. For photovoltaic cells, a rear surface mirror allows for a thinner absorber layer than bulky substrate-based solar cells, saving growth time and reducing the use of costly materials while allowing for increased efficiency via "photon recycling"[9]. For LEDs, the rear surface mirror improves external quantum efficiency by allowing photons to be reflected back to the emitting surface instead of being absorbed in the wafer bulk[10].

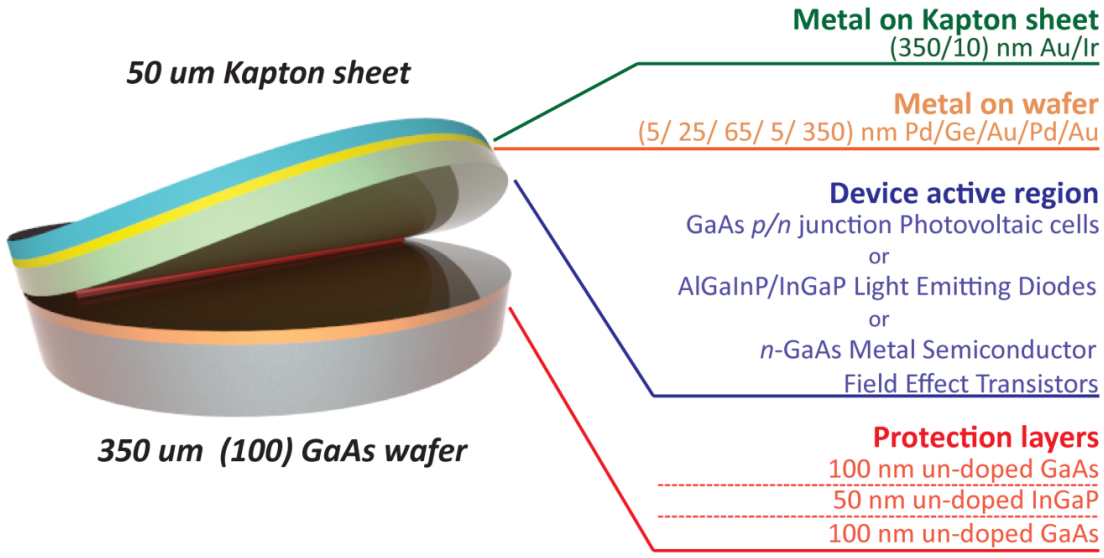


Figure 6.1: Schematic illustration of a generalized wafer structure used in non-destructive epitaxial lift-off (ND-ELO). The active thin film device region is lifted-off by selectively etching the AlAs sacrificial layer using dilute hydrofluoric acid. Details of the epitaxial layers, including the alternating GaAs-InGaP protection layers and the AlAs sacrificial layer are shown along with the metal layer used in cold-welding to the plastic substrate. The active region structure is varied according to the application requirements, e.g. a photovoltaic cell, light emitting diode, or metal semiconductor field effect transistor.

6.2.2 Epitaxial Growth

In advance of epitaxial growth, both fresh and reused parent wafers are thermally cleaned in the loading chamber attached to the growth chamber at 280 ℃ and at $< 5 \times 10^{-7}$ torr base pressure for 1 hr. The surface is then outgassed in the growth chamber at 620 ℃ for 5 min under an As over-pressure. Elemental solid Ga, In and Al, and AsH_3/PH_3 gas are used as source materials. The cracker for the gaseous sources is kept at 950 ℃ during the growth, and 3 SCCM of AsH_3 and 4 SCCM of PH_3 gas are introduced to the chamber through mass flow controller during the GaAs and InGaP/AlGaInP growths, respectively. The cracking efficiency is above 95% for both AsH_3

and PH_3 gas according to quadrapole mass spectroscopy measurements using a residual gas analyzer (RGA). For the GaAs/InGaP heterostructure growth, the substrate temperature of the initial GaAs growth is 600 ℃. Then the Ga shutter is closed, and the substrate temperature is ramped to 515 ℃ under an AsH_3 flux, followed by a further decrease to 480 ℃ without AsH_3 to change the surface from As-saturated to As-stable. Then the PH_3 flow is turned on for 3 s, and In and Ga shutters are opened for InGaP growth. After the growth of the InGaP layer, the GaAs and AlAs layers are grown at 600 ℃ and 630 ℃, respectively. Growth rates for GaAs, AlAs and $Al_{0.20}In_{0.49}Ga_{0.31}P$/ $In_{0.49}Ga_{0.51}P$ are 1 μm/hr, 0.6 μm/hr and 0.8 μm/hr, respectively. The *n/p*-type doping concentration is calibrated by Hall effect and secondary ion mass spectrometry (SIMS) measurements. Lattice matching of InGaP and AlInGaP to GaAs substrate is determined by X-ray diffraction.

For the protection layer, the growth starts with GaAs (0.1 μm)/ $In_{0.49}Ga_{0.51}P$ (0.05 μm)/ GaAs (0.1 μm) layers followed by a 20 nm thick AlAs sacrificial layer. Next, an inverted active device region is grown as follows: For the photovoltaic cells we grow a 0.1 μm thick, 5×10^{18} cm^{-3} Be-doped GaAs contact layer, 0.025 μm thick, 2×10^{18} cm^{-3} Be-doped $Al_{0.20}In_{0.49}Ga_{0.31}P$ window layer, 0.15 μm thick, 1×10^{18} cm^{-3} Be-doped p-GaAs emitter layer, 3.0 μm thick, 2×10^{17} cm^{-3} Si-doped n-GaAs base layer, 0.05 μm thick, 6×10^{17} cm^{-3} Si-doped $In_{0.49}Ga_{0.51}P$ back surface field (BSF) layer, and 0.1 μm thick, 5×10^{18} cm^{-3} Si-doped n-GaAs contact layer. For the light emitting diodes (LEDs) we grow a 0.1 μm thick, 5×10^{18} cm^{-3} Be-doped GaAs contact layer, 0.8 μm thick, 2×10^{18} cm^{-3} Be-doped $Al_{0.20}In_{0.49}Ga_{0.31}P$ layer, 0.1 μm thick un-doped $In_{0.49}Ga_{0.51}P$ layer, 0.8 μm thick, 2×10^{18} cm^{-3} Si-doped $Al_{0.20}In_{0.49}Ga_{0.31}P$ layer, 0.1 μm thick, 5×10^{18} cm^{-3} Si-doped n-GaAs contact layer. For the metal semiconductor field effect transistors

(MESFETs) we grow a 0.05 μm thick, 5×10^{18} cm^{-3} Si-doped GaAs contact layer, 0.16 μm thick, 4×10^{17} cm^{-3} Si-doped GaAs channel layer, 1 μm thick un-doped GaAs layer.

6.2.3 Cold Weld Bonding

In conventional ELO, lifted-off layers are typically attached to flexible secondary handles using adhesives such as thermal releasing tape, wax, or glue[3-6]. These adhesives can be bulky, heavy, brittle and subject to degradation while also requiring an additional transfer following the separation of the epitaxy onto an intermediate "handle" [3-5]. To eliminate all use of adhesives and the necessity of an intermediate handle transfer, we attach the epitaxial surface directly to the final flexible substrate following layer growth using a thermally-assisted cold-weld bond by applying pressure across the two surfaces to be bonded. To make the bond, the surfaces are pre-coated with layers of a similar noble metal.

Figure 6.2 shows details procedure for thermally assisted cold weld bonding. To prepare for cold-weld bonding; a 10 nm thick Ir adhesion layer is sputtered on a Kapton® sheet. Next, Pd (5 nm)/ Ge (25 nm)/ Au (65 nm)/ Pd (5 nm) layers are deposited onto the substrate using e-beam evaporation to form an ohmic contact with the 5×10^{18} cm^{-3} Si-doped n-type GaAs layer[11]. Then, a 350 nm thick Au layer is simultaneously deposited on both sample surfaces to complete the cold-welding bonding surfaces. Two freshly deposited Au films on opposing surfaces are bonded together with the application of pressure. Thus, the GaAs wafer with epitaxial layer is bonded to the Kapton® sheet using an EVG 520 wafer bonder under ~10^{-5} torr vacuum immediately following Au deposition by e-beam evaporation. For a 2 inch-diameter substrate, 4 MPa of pressure is applied to establish a bond between the two gold films with a 80 N/sec ramping rate. Then the thermally assisted cold-weld bonding process is carried out by ramping the temperature at 25 ℃/min to 175 ℃, and holding at the peak temperature for 3 min. The substrate temperature

is subsequently reduced using active stage cooling. To apply a uniform force over the sample area, a reusable, soft graphite sheet is inserted between the sample and the press head. The process combined with vacuum, heat and a soft graphite pad allows for a significantly lower pressure (4 MPa) than conventional cold-welding (50 MPa for the same area bonding)[12]. Additionally, it requires a lower temperature and shorter duration than conventional thermo-compression bonding (above 300 ℃/ 20~45min).

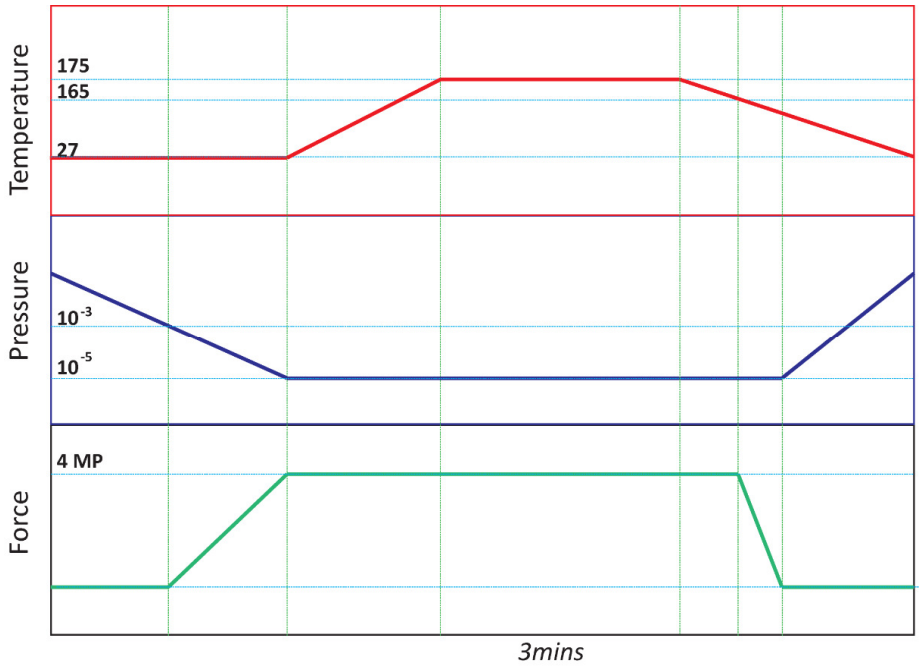


Figure 6.2: Thermally assisted cold-weld bonding Detailed bonding procedure including stage temperature, chamber pressure and applied force vs. time.

We note that Au also conveniently acts as a back contact and mirror while being undamaged by exposure to HF used in the ELO process. Further, it is insensitive to oxidation that can increase the pressure needed to effect the cold-weld bond.

6.2.4 Epitaxial Lift-Off

Once the GaAs substrate is bonded to the Kapton® sheet, the thin active device region is removed from its parent substrate through the non-destructive epitaxial lift-off (ND-ELO) process. The entire sample is immersed in a 20% HF solution maintained at 60 ℃. The HF solution is agitated with a stir bar at 400 rpm. Due to the high etch selectivity between AlAs and the active compound semiconductor layers, dilute HF removes the 20 nm thick AlAs sacrificial layer between the wafer and active device region without attacking the adjacent protection layers. The total lift-off time for a 2 inch GaAs substrate is approximately 5 hr. Here, the sample is fully submerged and relaxed in dilute HF and assisted solely by tensile stress introduced by the Ir. Therefore, the etching process is initiated from all directions similar to prior ELO process demonstrations[7]. The Ir layer provides tensile strain to the substrate, which is confirmed by observing curvature of the flexible secondary substrate following Ir deposition. The tensile-strained Ir layer significantly reduces the wafer and substrate separation time (~5 hrs) by more than 90% compared with the ELO process without Ir layer (~36 to 48 hours). This process acceleration was confirmed by comparison with a sample with the same structure and ELO process conditions but without the addition of the Ir film. The tensile stress from the film assists in creating a gap between the epitaxial layers and the substrate at the sacrificial layer etch interface allowing for the rapid ingress of etchant, analogous to that observed for compressively stressed layers. The induced curvature by tensile stress is kept below the tolerance of GaAs thin film, and the sacrificial layer is etched faster from the two curved sides and etched slowly from the other side which eliminates the damage of film caused by concentrated stress to the small area. Then, the separated epitaxial films are fabricated into photovoltaic cells, LEDs and MESFETs. The device

performance variations are negligible depending on the position of device on the film which indicates the integrity of the film.

Although ELO is an effective means to separate the substrate and active regions to create a thin film device, it also results in roughening of the parent wafer surface, as well as the accumulation of contaminants, notably As_2O_3[8,13]. Figure 6.3 shows these particles as observed by SEM. The rough, particle-covered surface prevents the subsequent growth of layers of the same quality as on the original surface, and eventually results in the degradation of regrown photovoltaic device performance. There is no evidence for etching of the GaAs layer adjacent to the sacrificial layer.

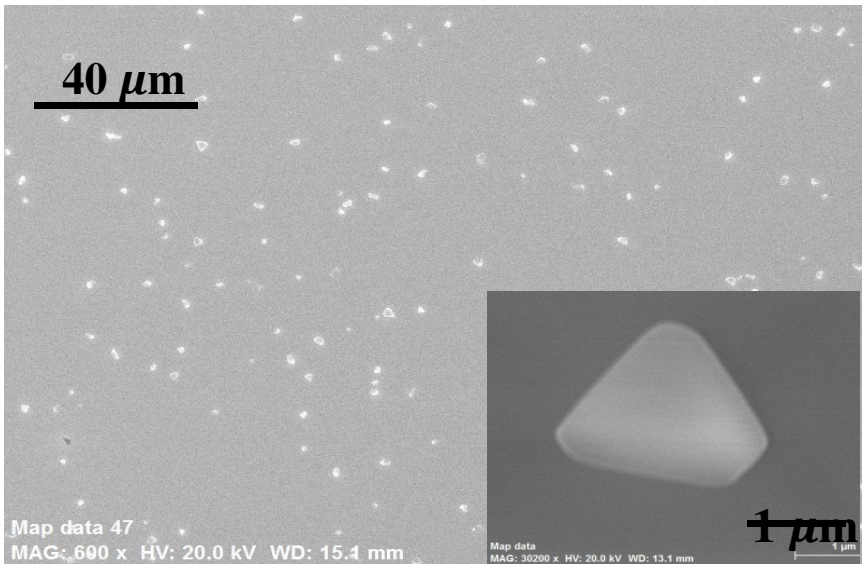


Figure 6.3: Scanning Electron Microscopic (SEM) image of an HF exposed wafer surface without protection layers.

The surface roughening is shown in the atomic force microscope (AFM) image of Figure 6.4. This morphological degradation significantly and negatively impacts device performance in subsequently regrown layers, e.g. 20~40% performance loss in solar cell power conversion efficiency (*PCE*)[4].

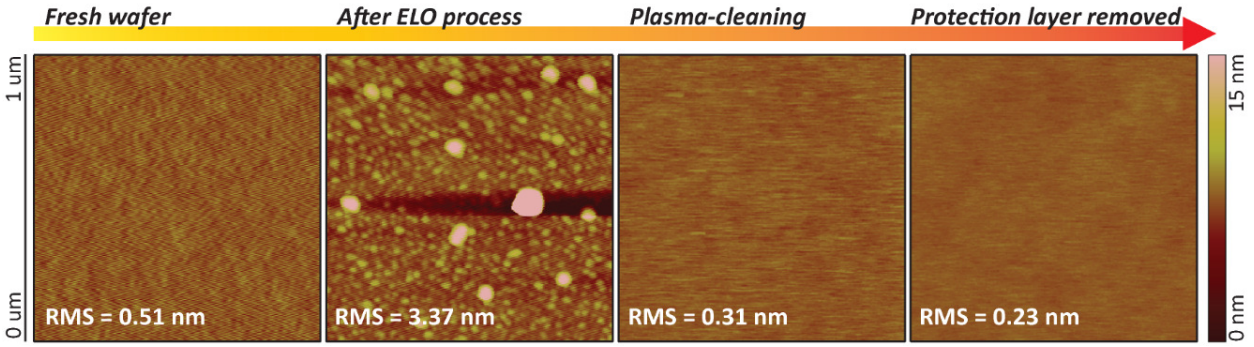


Figure 6.4: Comparison of wafer surface morphology before and after ELO. Atomic force microscope (AFM) images of the GaAs parent wafer substrate surface showing the root-mean-square (RMS) surface roughness (indicated by color bar) after each step. The growth starts with sub-nanometer surface roughness. However, immediately following ELO by etching the sacrificial layer, the roughness increases by an order of magnitude. Plasma cleaning reduces surface roughness by removing particulates while minor physical damage is incurred by the underlying GaAs protection layer. Wet chemical cleaning is used to remove the remaining InGaP protection layer, recovering the same surface morphology as the original wafer.

6.2.5 Surface Cleaning & Protection Layers Removal

To recover original surface quality, we have developed a completely non-destructive two-step cleaning procedure. The surface is pre-cleaned by an inductively coupled plasma using 50 SCCM of C_4F_8, a chemical etch gas to remove the oxides, mixed with 50 SCCM of Ar+ for 10s under 10 mTorr of base pressure at a substrate RF bias power of 110 W and a transformer coupled

plasma RF power of 500 W. Figure 6.5(a) provides 3 dimensional laser microscopy images of the wafer surface before and after plasma cleaning, respectively. The image indicates that most of the contamination is apparently removed during the cleaning process, leaving a roughened surface. This cleaning procedure can be applied to the lifted-off film as well as the substrate, which are similarly contaminated following the ELO process (Figure 6.5(b)). While eliminating the ELO process residuals, this process also physically/chemically damages the protection layer surface. Hence, InGaP and GaAs protection layers are grown on both the epi-side and the substrate-side (each in reverse order to the other starting with GaAs on the substrate) to address this problem. The roughened top GaAs protection layer is then removed using a phosphoric acid-based etchant (H_3PO_4:H_2O_2:H_2O (3:1:25)) until the etching stops at the InGaP layer. Next, the InGaP layer is removed through etching in diluted HCl acid (HCl:H_2O (1:1)), which provides complete etching selectivity with the GaAs growth buffer layer. The dilute HCl etch is well-known for preparing epi-ready surfaces through the removal of native oxides, allowing this last step of surface cleaning to provide a high quality regrowth interface[6, 14, 15.] The root mean square (RMS) surface roughness after each step is shown in Figure 6.4, confirming the recovery of the original surface morphology after cleaning.

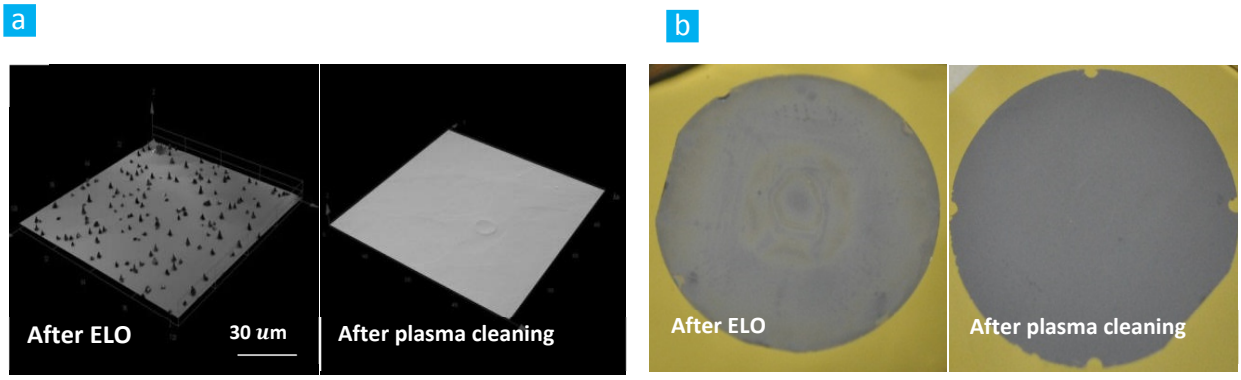


Figure 6.5: Comparison of wafer surface morphology before and after ELO. (a) Three dimensional laser microscope image of the surface immediately following ELO (left), and after plasma cleaning (right). (b) The thin-film surface following ELO (left), and after plasma cleaning (right).

To compare the surface chemistry and effectiveness of protection layers on exposure to etchants with that of the as-grown surface, EDS data for the surfaces of fresh, unprotected, and protected wafers were obtained. Figure 6.6 shows EDS maps of O, Ga and As for the surfaces of the three different samples. Original and surface-protected wafers show nearly identical chemical compositions, whereas surfaces exposed to HF while lacking a protection layer exhibit locally concentrated oxygen with a corresponding deficiency of elemental Ga. The shape of the oxidized feature is consistent with the presence of a micron-scale particle as shown in Figure 6.3, inset. This suggests the formation of As_2O_5 on the surface during the etch process.

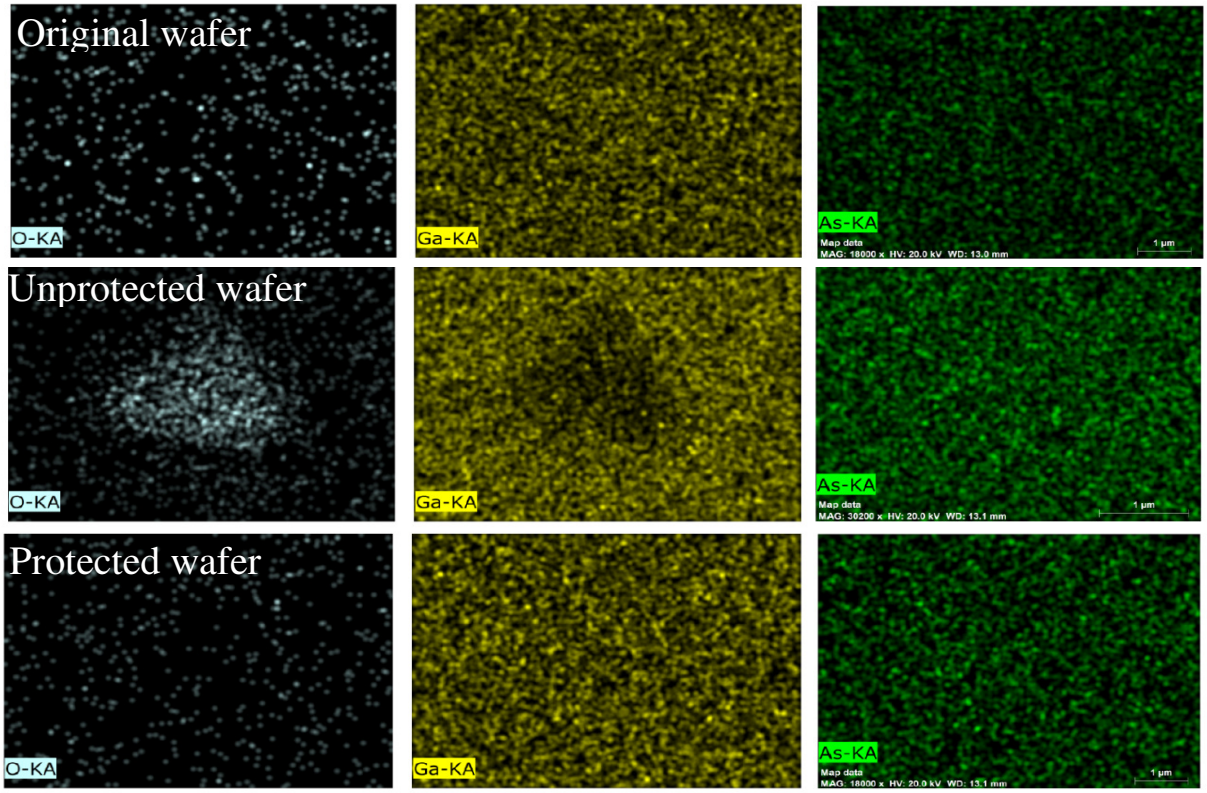


Figure 6.6: Hybrid mapping of elemental oxygen, gallium, arsenic near the surface of original, surface protected, and unprotected wafers after the protection layers were removed. The elemental compositions are shown in each image.

Figure 6.7 shows the EDS data for of the same samples as in Figure 6.3. The concentrations of O extracted from the spectra for the original, protected and unprotected wafers over the surface were 2.2%, 0.7% and 25.6%, respectively. Also, the atomic ratios of Ga to As were 48.3%:49.5%, 49.5%:50.3% and 33.2%:41.2% with $\pm$ 0.4% error, respectively. The fresh and protected samples show similar Ga:As ratios with low oxygen concentration.

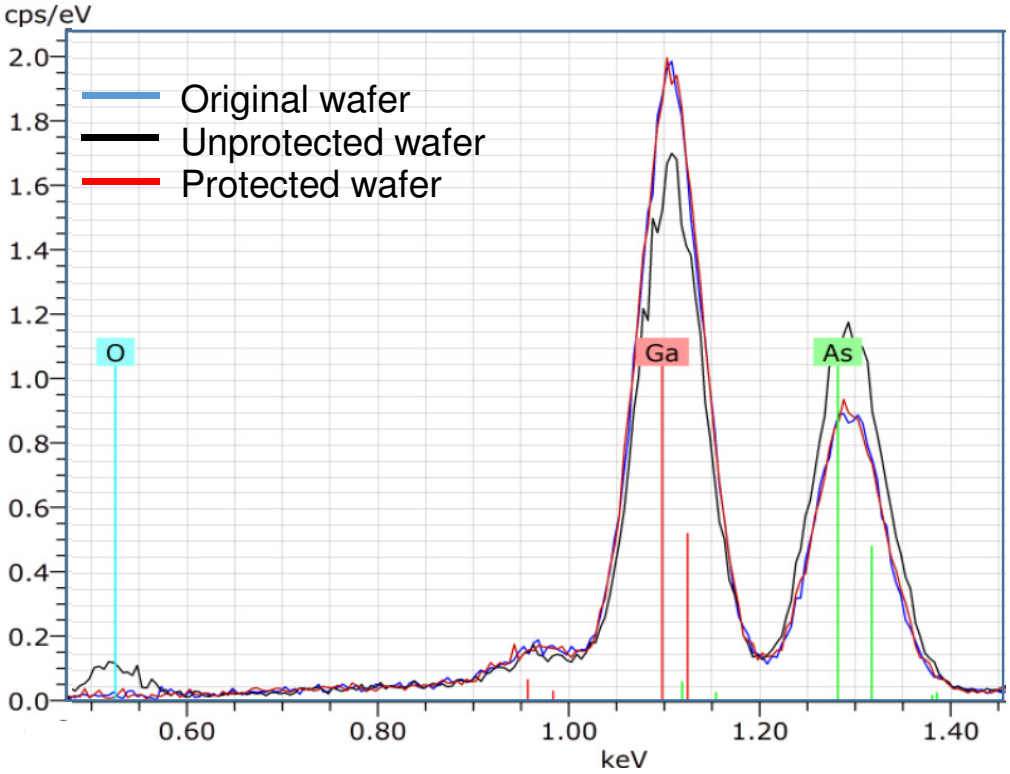


Figure 6.7: Energy dispersive spectra of wafers in Figure 6.3.

This conclusion is supported by the XPS data in Figure 6.8. Original and protected wafer surfaces exhibit nearly identical As and As_2O_5 peak intensities, however, the unprotected surface shows a weak As and strong As_2O_5 peak intensity. Moreover, the XPS measurements (not shown) indicate a negligible difference between original and regrown wafer surfaces following protection layer removal without the appearance of additional peaks, indicative of a chemically unchanged surface before and after protection layer removal and regrowth.

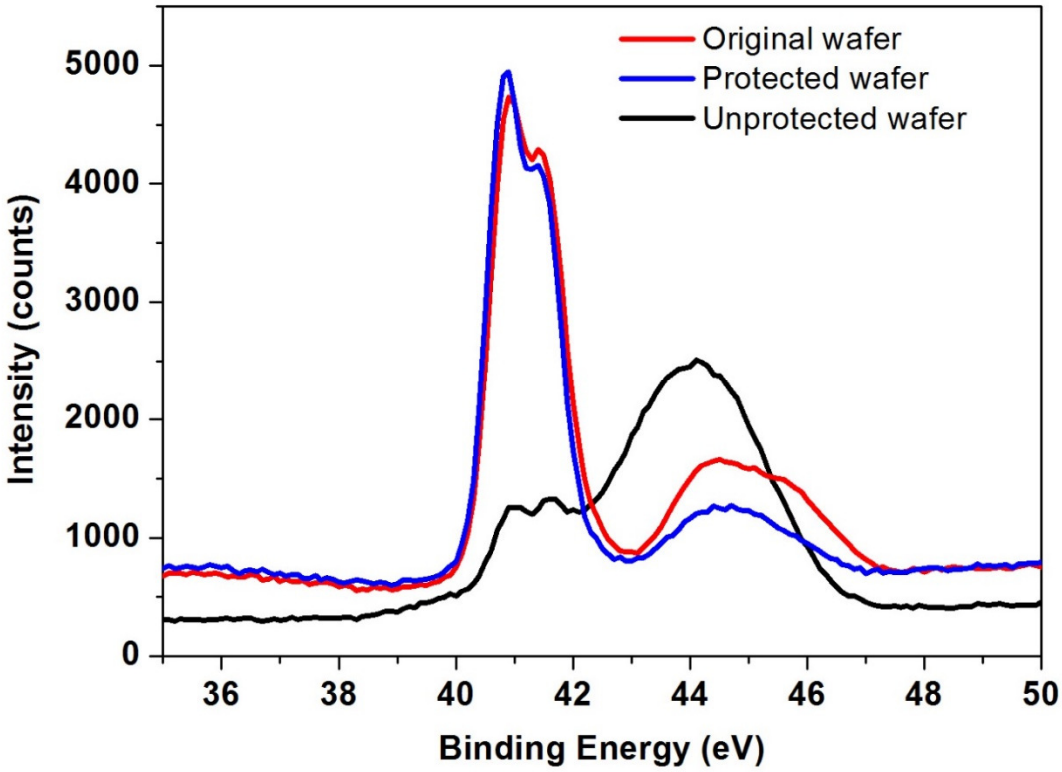


Figure 6.8: X-ray photoelectron emission spectra of the samples in Fig. 2 measured using energy dispersive spectrometery (EDS).

6.2.6 Characterizations of Regrown Epi-layer

Figure 6.9 shows cross-sectional, high angle annular dark field images of an undoped GaAs layer at the growth interface. The reference epitaxial layer was grown on the original, epi-ready wafer, and identical structures were grown on protected and etched wafer surfaces that have been exposed to this cycle twice, with the surface protection layers removed following each growth sequence. The cross-sectional, atomic resolution STEM image shows the nearly perfect crystalline growth without any apparent defects for all samples. This indicates that the quality at the growth interface after protection layer removal is unchanged from that of the original wafer.

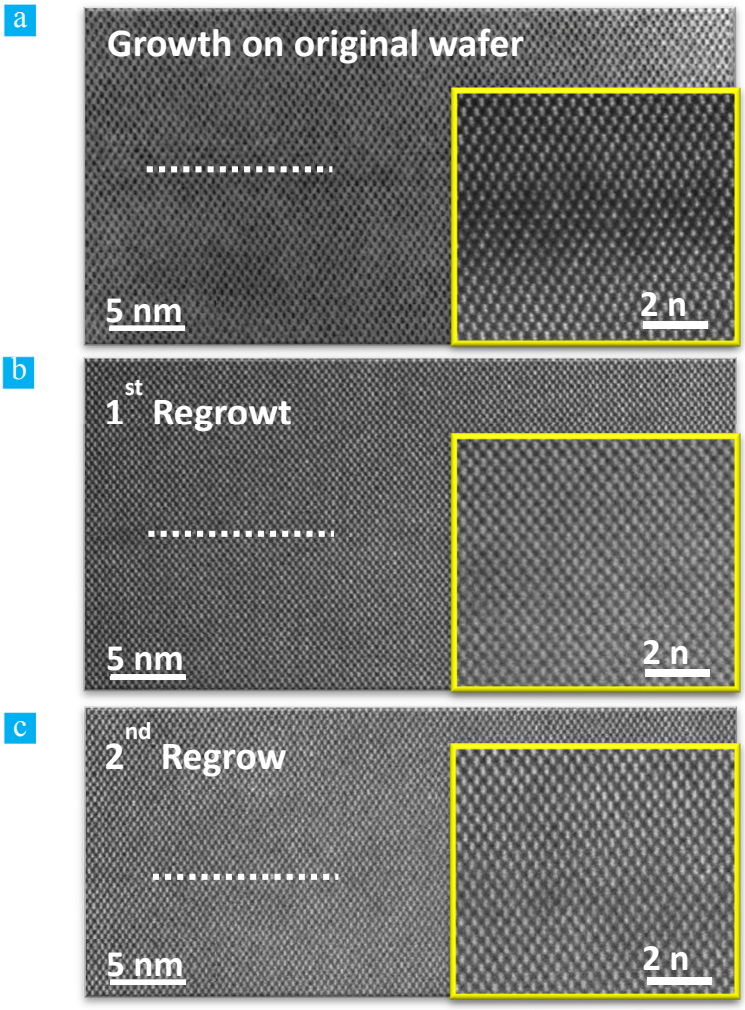


Figure 6.9: Atomic resolution cross-sectional transmission electron microscope images of the growth interface between the wafer and epitaxial GaAs layer grown on (a) original, (b) first epitaxial and (c) second epitaxial growth steps. Dotted lines indicate the starting growth interfaces. Insets show details of the growth interfaces.

Photoluminescence (PL) spectra of the samples were compared using a 20 mW, λ=473 nm wavelength diode pump laser. Figure 6.10 shows the PL intensity between λ=820 nm and λ=900 nm for three samples consisting of a 0.1 µm thick undoped $Al_{0.7}Ga_{0.3}As$, a 1 µm thick

undoped GaAs, and a 0.1 μm thick undoped $Al_{0.7}Ga_{0.3}As$ double heterostructure grown on an original (reference), protected and non-protected wafer. The data indicate that losses due to non-radiative recombination are comparable between the layers grown on the fresh and used, protected wafer. However, the weak PL intensity of the structure grown on the unprotected substrate is further evidence of a degraded surface. The inset provides the reflection high energy electron diffraction (RHEED) patterns obtained from the wafer surface in the GSMBE chamber. The original wafer clearly exhibits a 2×4 reconstruction after 100 monolayers of buffer layer growth. The nearly identical streak pattern after ~100 monolayers of growth after epitaxial protection layer removal indicates that the surface roughness is unchanged from that of the reference. However, the RHEED patterns for the unprotected surface exhibits a spotty chevron-shaped pattern, once more indicative of a roughened surface.

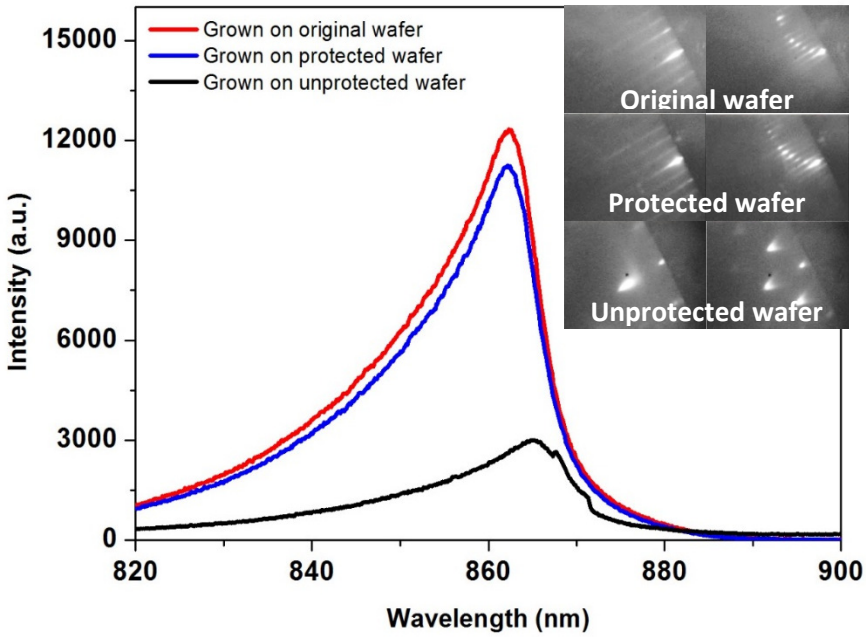


Figure 6.10: Photoluminescence spectra at room temperature (300K) from an $Al_{0.7}Ga_{0.3}As/GaAs/Al_{0.7}Ga_{0.3}As$ heterostructure on original and reused wafer. Insets: The 2 × and 4 × surface reconstruction patterns obtained by reflection high-energy electron diffraction for the original and etched substrate surfaces with and without a protection layers.

The Hall effect doping concentrations of the Si-doped, 1 μm thick GaAs layers of the original and regrown samples were $(1.62 \pm 0.05) \times 10^{18} cm^{-3}$ and $(1.66 \pm 0.12) \times 10^{18}$ cm^{-3}, respectively, and the Hall mobilities were 2030±80 cm^2/Vs and 2050±120 cm^2/Vs, respectively. The small differences between samples are due to run-to-run variations.

6.2.7 Characterizations of Thin-Film Optoelectronic Devices

To demonstrate the effectiveness of wafer recycling using the above methods, the cleaned parent wafer was re-loaded into the GSMBE chamber for subsequent growth, and the same procedure was repeated multiple times with solar cells, LEDs and MESFETs fabricated after each growth/ELO/cleaning cycle to ensure that no degradation of the original wafers was carried into the next cycle.

After lift-off, the thin-film active region and flexible plastic secondary substrate is fixed to a rigid handle for convenience throughout the remainder of the fabrication process. The front finger grid is photolithographically patterned using an LOR 3A and S-1813 (Microchem) bi-layer photoresist process, then a Pd(5 nm)/ Zn(20 nm)/ Pd(15 nm)/ Au(700 nm) metal contact is deposited by e-beam evaporation. The finger grid and bus bar widths are 25 μm and 80 μm, respectively, and the spacing between grid lines is 660 μm. The total coverage of the front contact is 5.8%. After the metal layer is lifted-off, and an array of 5 mm × 5 mm device mesas are defined by photolithography using S-1827 (Microchem) and chemical etching using H_3PO_4:H_2O_2: deionized H_2O (3:1:25) and the exposed, highly-doped 100 nm thick *p*+ GaAs contact layer is subsequently selectively removed using the same etchant. The thin-film solar cells are annealed for 1 hr at 200 °C for ohmic contact formation. Finally, to achieve a minimum surface reflection,

a bilayer anti-reflection coating (ARC) consisting of TiO_2 (49 nm) and MgF_2 (81 nm) is deposited by e-beam evaporation.

For example, three identical GaAs *p/n* junction thin film photovoltaic cells on plastic substrates were fabricated from a single parent wafer and processed using conventional methods into single junction solar cells (Figure 11(a) - (c)).

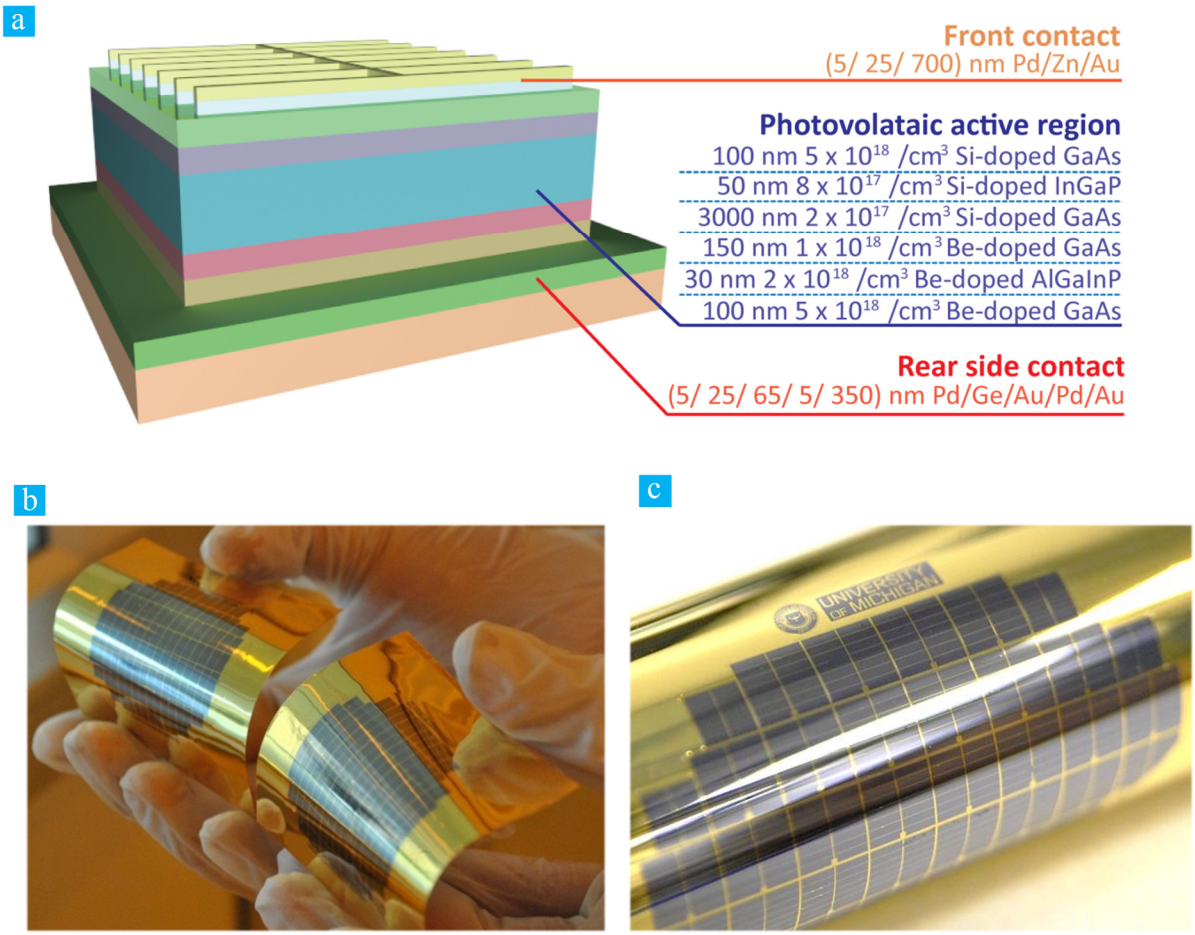


Figure 6.11: Thin-film GaAs single junction photovoltaic cells. (a) Device structure of the thin film GaAs *p-n* junction photovoltaic cells. (b) Fabricated GaAs thin film photovoltaic cells bonded by thermally assisted cold-welding to a plastic substrate following ND-ELO of 2 inch-diameter wafers. Both cell arrays are made from the same GaAs wafer using ND-ELO, wafer bonding, and parent wafer recycling. (c) Close-up image of the GaAs thin film photovoltaic cell array.

The current density-voltage (*J-V*) characteristics of the cells measured under simulated AM 1.5G illumination at 1 sun (100 mW/cm^2) after the first, second, and third ELO cycles are compared in Figure 6.12(a). An Oriel solar simulator (model: 91191) with Xe arc lamp and AM 1.5 Global filter is used for current density-voltage (*J-V*) measurements. Intensity is calibrated using a National Renewable Energy Laboratory (NREL) certified Si reference cell with diameter of 5 mm. Then, the *J-V* characteristics are obtained with an Agilent 4155B parameter analyzer. The external quantum efficiencies (*EQE*) are compared in Figure 6.12(b). A tungsten-halogen lamp combined with a monochrometer is used for measurement of the external quantum efficiency (*EQE*) spectrum. A band-pass filter is located at the output of the monochrometer to cut off higher wavelength harmonics. The monochoromatic light is then chopped at 200 Hz, focused and into an optical fiber. A lock-in amplifier is employed to measure the photovoltaic cell photocurrent. The illumination intensity is calibrated with a Newport 818-UV Si low-power photodetector. The *J-V* characteristics, short circuit current density (J_{SC}), open circuit voltage (V_{OC}), fill factor (*FF*) and *PCE* are nearly identical (with a standard deviation of 1.5% in *PCE*) for all devices without any apparent systematic degradation after a given cycle (see Table 6.1).

Table 6.1: Comparison of device performances under AM1.5G simulated solar spectrum.

	J_{SC} (mA/cm^2)	V_{OC} (V)	*FF* (%)	*PCE* (%)	J_{max} (mA/cm^2)	V_{max} (V)	*N*
First ELO	24.2 $\pm$ 0.1	0.98	76.4 $\pm$ 0.6	18.1 $\pm$ 0.1	22.4 $\pm$ 0.2	0.81	1.95
Second ELO	23.9 $\pm$ 0.1	0.97	77.9 $\pm$ 1.3	18.0 $\pm$ 0.3	21.7 $\pm$ 0.3	0.83	1.83
Third ELO	24.2 $\pm$ 0.1	0.98	77.7 $\pm$ 0.1	18.5 $\pm$ 0.1	23.2 $\pm$ 0.2	0.84	1.98

Integration of the *EQE* spectra assuming an incident AM 1.5G solar spectrum gives J_{SC} = $23.2 \pm 0.1 mA/cm^2$, 23.0 ± 0.1 mA/cm^2 and 23.2 ± 0.1 mA/cm^2 for the first, second, and third ELO cycle, respectively. The discrepancy between the integrated J_{SC} and that extracted from the *J-V* characteristics is primarily due to absorption at wavelengths λ<400 nm, which is not accounted for in the integration. Finally, we note that *PCE* = $18.1 \pm 0.1\%$, $18.0 \pm 0.3\%$, and $18.5 \pm 0.1\%$ were achieved for the three-cycle ND-ELO sequence. Normalized device performance parameters of the first, second and third cells are compared in Figure 12(c).

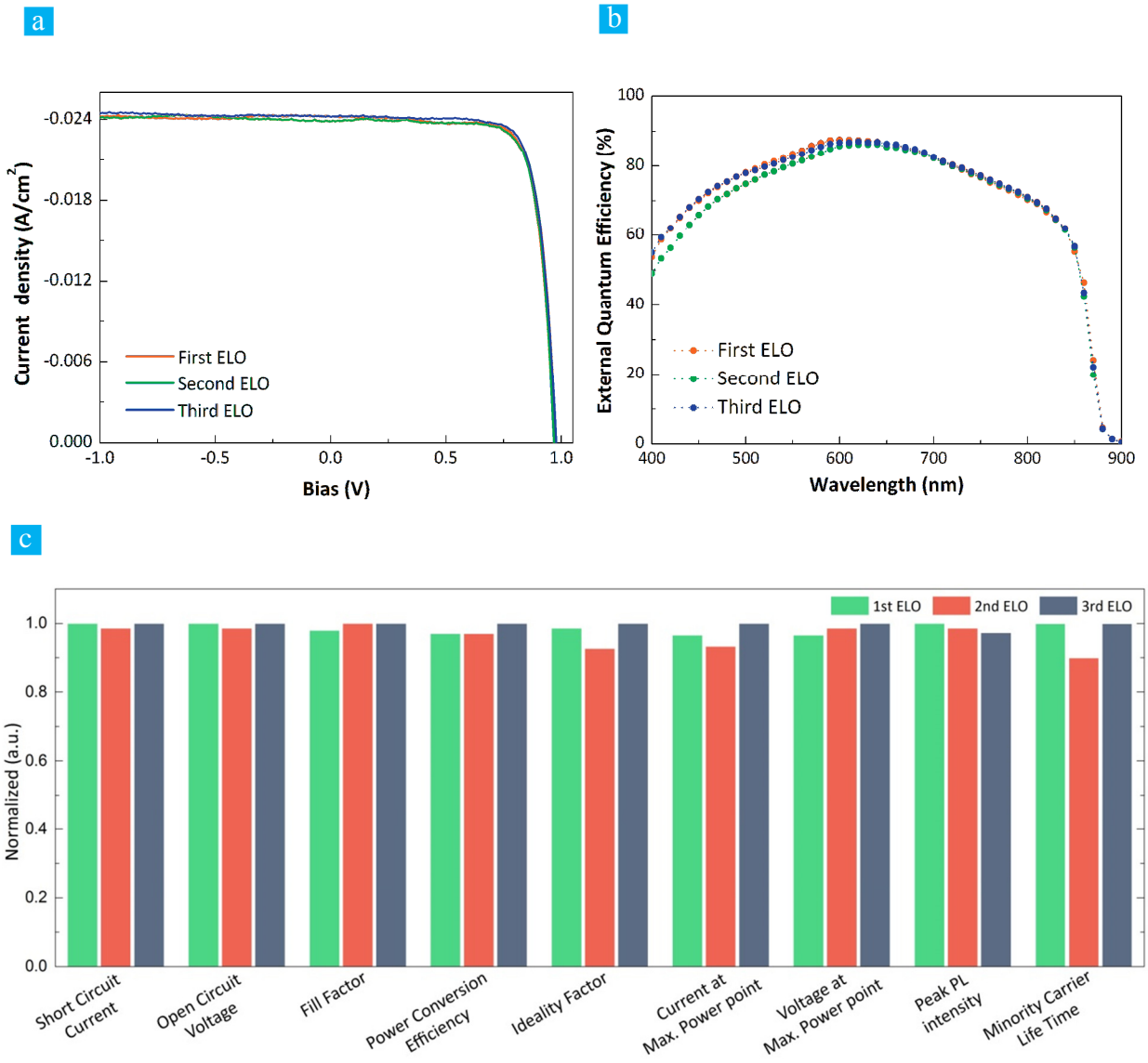


Figure 6.12: (a) Current density versus voltage (*J-V*) characteristics measured under 1 sun, AM1.5G simulated solar illumination, and (b) External quantum efficiency (EQE) measured from wavelengths between 400 nm and 900 nm after the first, second and third ND-ELO-processed photovoltaic cells originating from a single parent wafer. (c) Comparison of photovoltaic cell performance. These figures display statistically identical device performance without systematic degradation from growth to growth.

Figure 6.13 presents both the measured and fitted J-V characteristics assuming a Shockley ideal diode behavior modified to account for series resistance (R_S). The extracted R_S of the first, second and third ELO-processed photovoltaic cells are 4.2 Ω-cm^2, 4.5 Ω-cm^2 and 4.4 Ω-cm^2, respectively. The ideality factor is n = 1.9, 1.8 and 1.9, respectively.

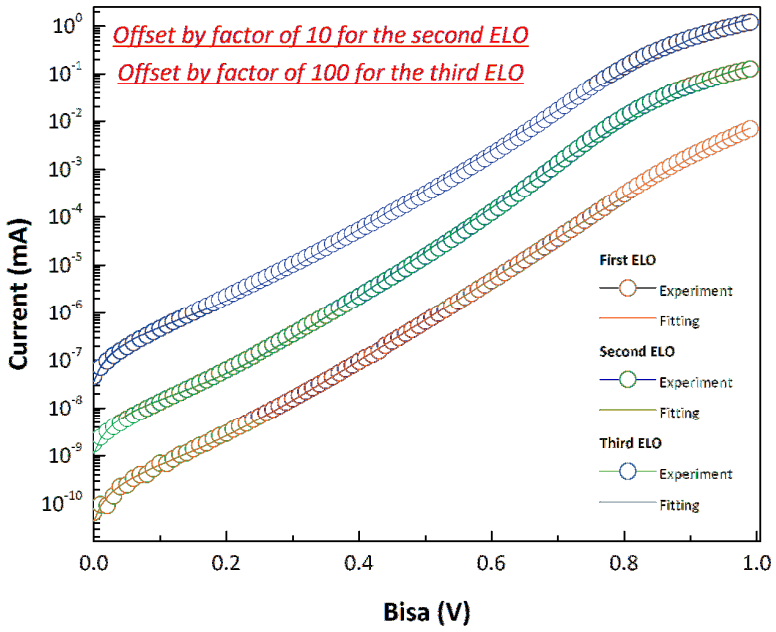


Figure 6.13. Current density-voltage (*J-V*) characteristics of photovoltaic cells in the dark. Measured and fitted *J-V* characteristic of the first, second and third ND-ELO processed solar cells. The second ELO is offset by a factor of ten and the third ELO by a factor of hundred for clarity.

The generated power as a function of forward voltage from photovoltaic cells after the first, second and third ND-ELO cycle is presented in Figure 6.14, indicating a nearly identical similar maximum power point at nearly identical voltage and current density of ~0.83 V and ~22 mA/cm^2, respectively. The output of each 5 mm × 5 mm thin-film cell at their maximum power points are 4.5 mW, 4.5 mW and 4.6 mW, respectively. These non-systematic, small deviations confirm the feasibility of wafer reuse via ND-ELO and surface-preserving buffer layers.

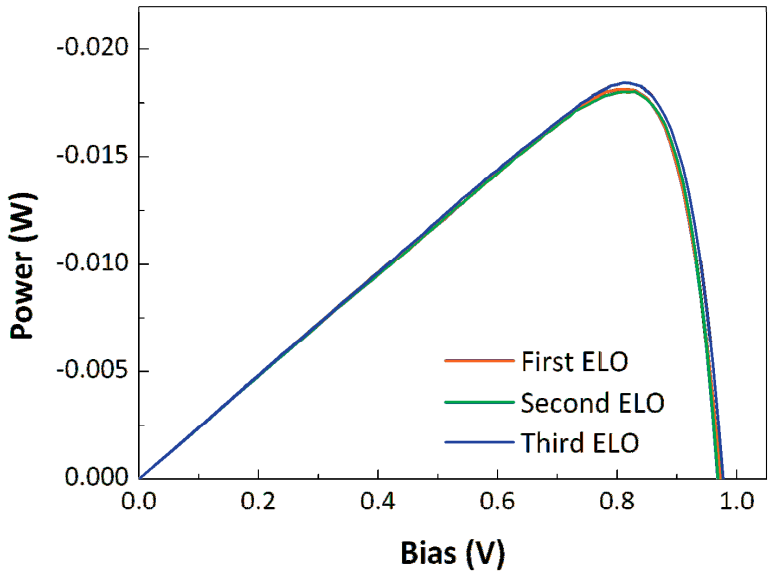
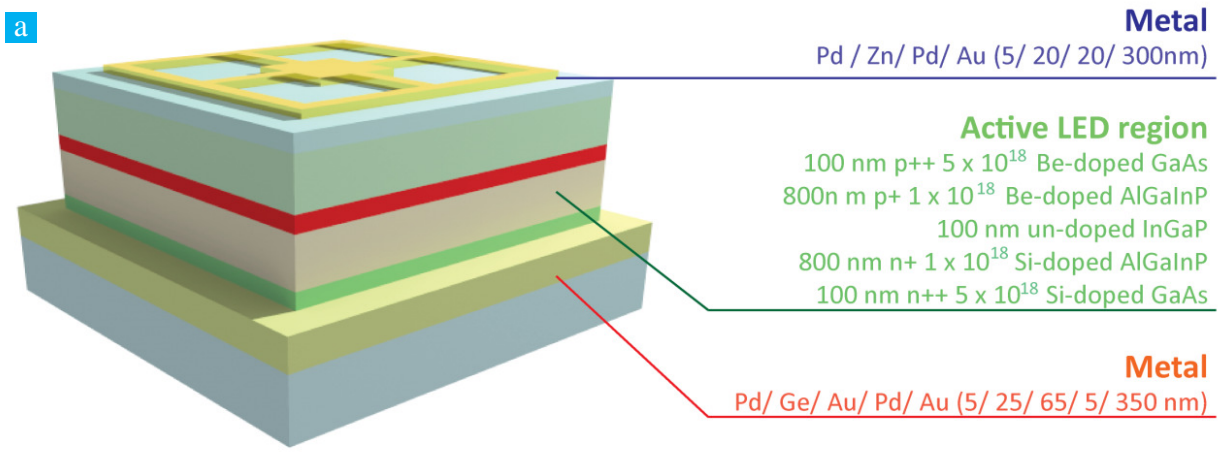


Figure 6.14. Power generation for photovoltaic cells. Comparison of the power output from each photovoltaic cell under forward voltage (*V*) under 1 sun intensity, AM1.5G illumination.

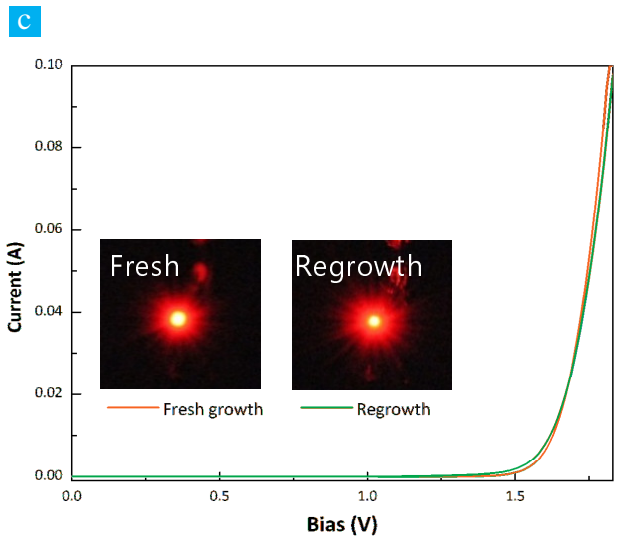
Multiple cylces of AlGaInP/ InGaP double heterojuction LEDs (Figure 6.15(a)) were also grown and fabricated to test the generality of our process approach. After the ND-ELO process, the thin-film active region and flexible plastic secondary substrate is fixed to a rigid substrate as in the case of the solar cell processing. The front finger grid is patterned by photolithography as in the case of the solar cells. Then, a Pd(5 nm)/ Zn(20 nm)/ Pd(15 nm)/ Au(300 nm) metal contact is

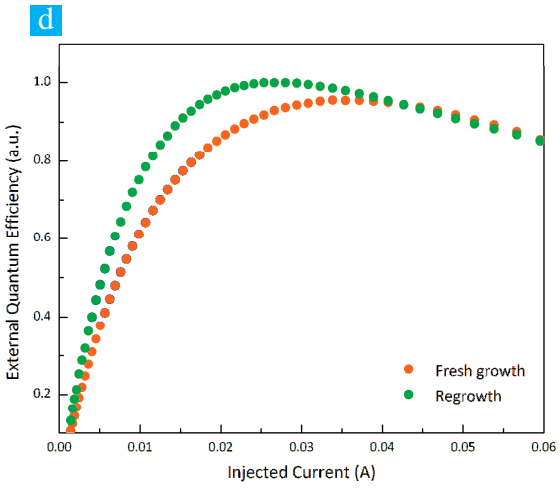
deposited by e-beam evaporation. The width of the front grid is 25 μm, and a 300 μm × 300 μm contact pad is patterned at the center of the grid. The total coverage of the front contact is 22.7%. After the metal layer is lifted off, 680 μm × 680 μm mesas are defined by photolithography using S-1827 (Microchem) and chemical etching using the same etchants as for the solar cells. The thin-film LEDs are annealed for 1 hr at 200 °C for ohmic contact formation.

Figure 6.15(b) shows images of the thin film LEDs with and without current injection (bent over a 1.2 cm radius without incurring damage or performance degradation), confirming device flexibility as in the case of the solar cells in Figure 6.11. The *J-V* and *EQE* characteristics of the first and second ELO-processed thin-film LEDs are compared in Figure 6.15(c) and (d), respectively. An HP 4156A semiconductor parameter analyzer and a Si *PIN* photodetector (Hamamatsu S3584-08) were used to measure the *J-V* and *EQE* of the LEDs. For electroluminescence (EL) measurements, the emitted light is focused onto an optical fiber, and the spectrum is measured by an Ocean Optics spectrometer. Turn-on voltage (1.66 $\pm$ 0.01 V and 1.67 $\pm$ 0.01 V, respectively) and peak *EQE* (4% variation) are extracted from the data for the first and second ELO cycles. Electroluminesence (EL) spectra for these same devices is provided in Figure 6.15(e).


a
Metal
Pd / Zn/ Pd/ Au (5/ 20/ 20/ 300nm)
Active LED region
100 nm p++ 5 x 10^18 Be-doped GaAs
800n m p+ 1 x 10^18 Be-doped AlGaInP
100 nm un-doped InGaP
800 nm n+ 1 x 10^18 Si-doped AlGaInP
100 nm n++ 5 x 10^18 Si-doped GaAs
Metal
Pd/ Ge/ Au/ Pd/ Au (5/ 25/ 65/ 5/ 350 nm)


b


c
Current (A)
Bias (V)
Fresh
Regrowth
Fresh growth
Regrowth


d
External Quantum Efficiency (a.u.)
Injected Current (A)
Fresh growth
Regrowth

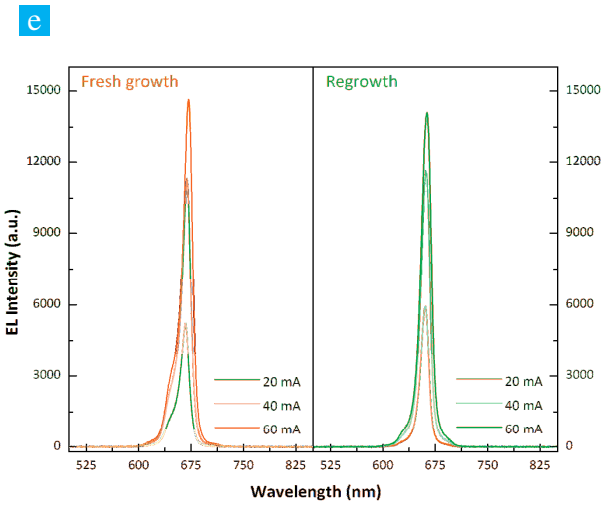

e
Fresh growth
Regrowth
EL Intensity (a.u.)
Wavelength (nm)
20 mA
40 mA
60 mA

Figure 6.15: Thin-film AlGaInP/InGaP double heterostucture LEDs. (a) Device structure of the thin film AlGaInP/InGaP LEDs. (b) Images of patterned LEDs in the shape of the University of Michigan logo bonded by thermally assisted cold-welding to a Kapton™ substrate (above), and the same device under operation (below). The images were taken for the plastic wrapped around a 1.2 cm radius cylinder. (c) Current density versus voltage (*J-V*) characteristics, (d) External quantum efficiency (EQE) measured from 400 nm to 900 nm and (e) Electroluminescence (EL) spectrum intensity comparisons for LEDs after the first and second ND-ELO removal from the same parent wafer. Similar peak EL intensities and full width half maxima (FWHM) indicate identical device performance without systematic degradation from the wafer recycling process.

The nearly identical performances of the first and second ELO processed thin film LEDs is confirmed by the measured full width half maxima of 16.5 nm and 16.6 nm, and peak EL intensities (3% variation) at an injection current of 60 mA. The current density vs. peak EL intensity (Figure 6.16) extracted from EL spectra in Figure 6.15(d) indicates comparable device performance without degradation following the ND-ELO process. Figure 6.17 shows an image of the LEDs before being bent around a cylinder.

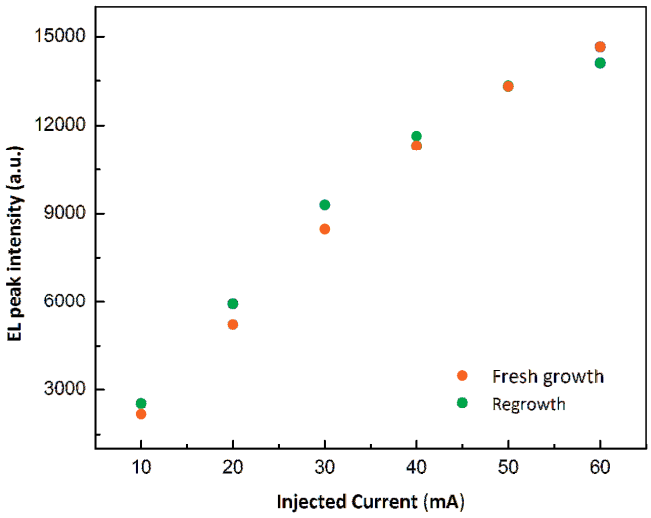


Figure 6.16. Comparison of LEDs performance. Comparison of peak intensity vs applied current density extracted from LED electroluminescence characteristics.

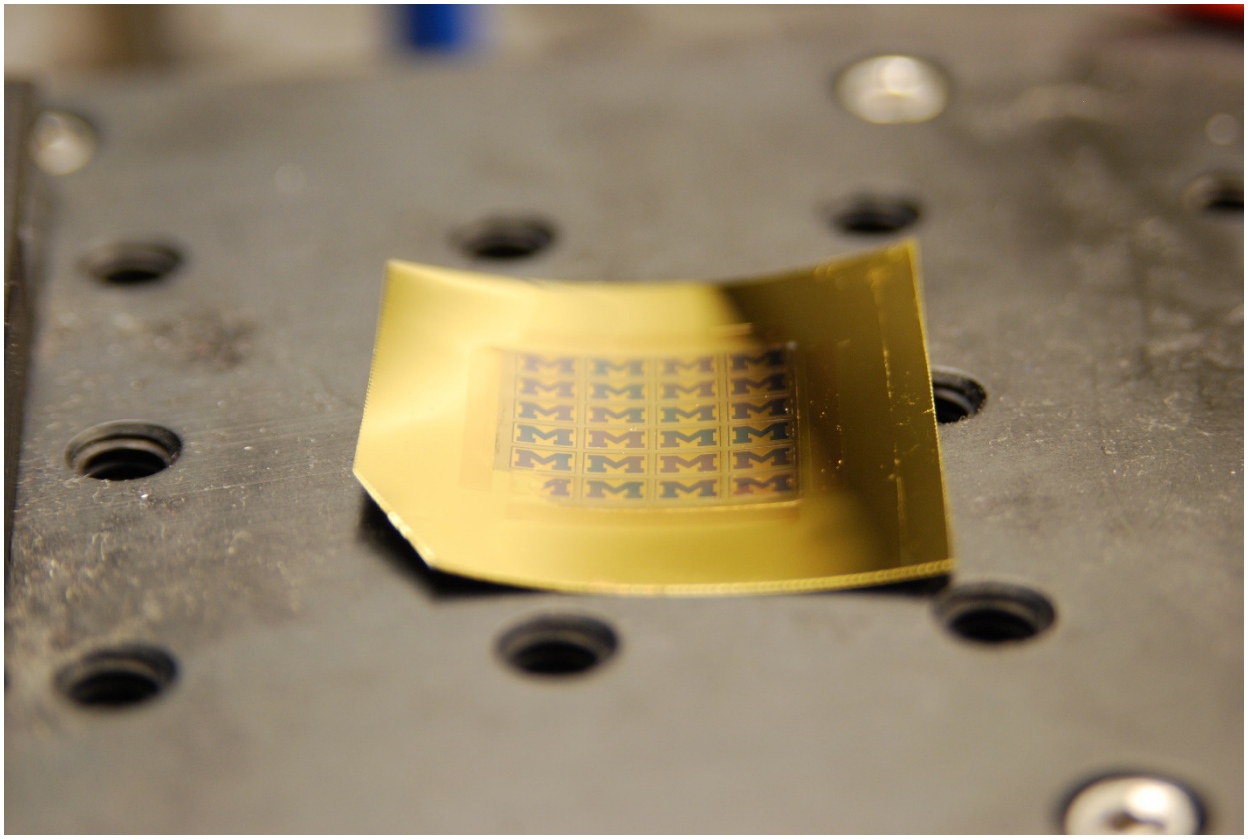
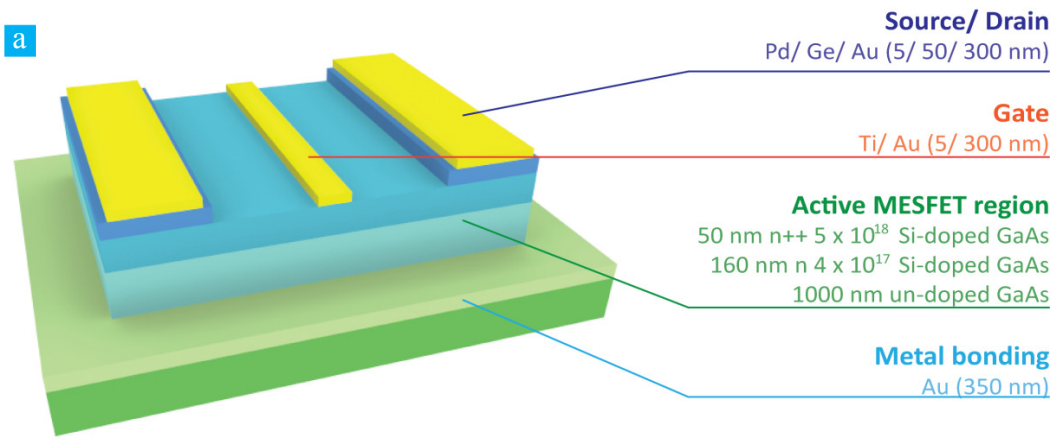


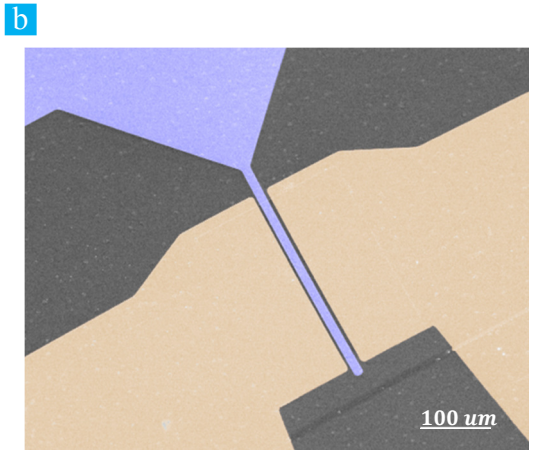
Fig. 6.17. Thin-film LEDs. Image of AlGaInP/ InGaP double heterostructure LEDs on a plastic substrate before the epitaxy is bent around a 1.2 cm radius.

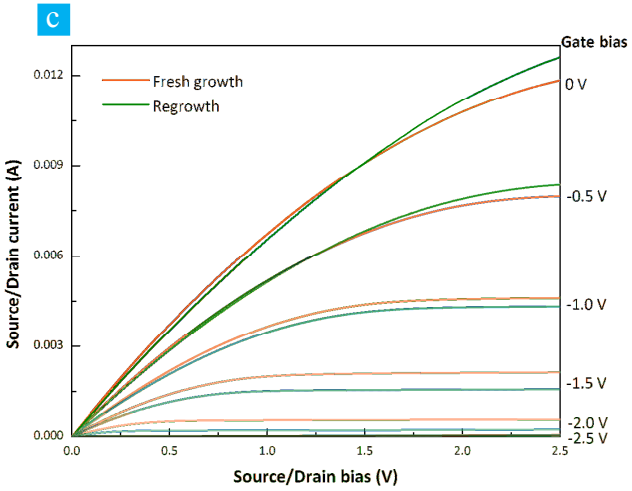
Finally, two iterations of *n*-GaAs MESFETs are fabricated from a single parent wafer and transferred to plastic, as shown in Figure 6.18(a). After lift-off, 225 μm × 250 μm mesas for ohmic contacts and channel layers are photolithographically defined as for solar cells. Then 210 μm deep mesas are etched with an inductively coupled plasma etching using a plasmalab system 100 (Oxford Instruments). For plasma etching, the sample was attached to a Si wafer carrier using thermal paste and Kapton® tape. During the etch process, the stage is actively cooled to 5 ℃ using LN_2. The source and drain contact is patterned using photolithography, and a Pd(5 nm)/ Ge(50

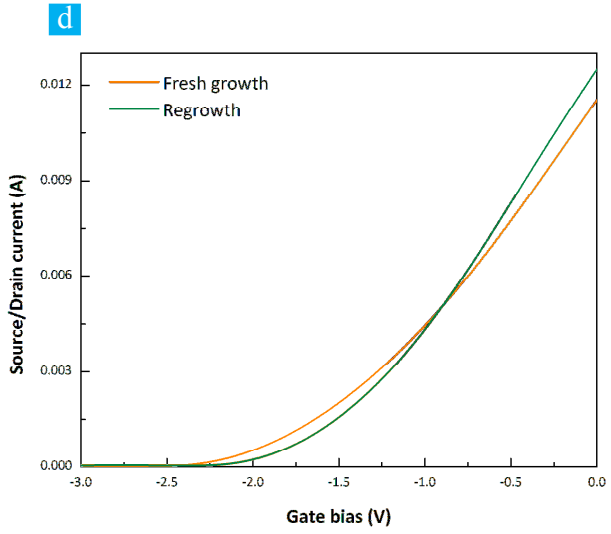
nm)/ Au(300 nm) metal contact is deposited by e-beam evaporation. The width and length of channel are 250 μm and 25 μm, repectively. After the metal layer is lifted-off, a 50 nm highly n-doped GaAs contact layer and the 10 nm thick channel layer are selectively removed by the inductively coupled plasma etching using the same procedure as above. The MESFETs are annealed for 1 hr at 240 °C for ohmic contact formation. Finally, the gate contact is patterned using photolithography, and a Ti(5 nm)/Au(300 nm) metal contact is deposited by e-beam evaporation. The patterned gate length is 11 μm measured by optical microscope.

The inverted MESFET structure is grown with the active channel layer closer to the growth interface compared with substrate-based device, therefore the device performance is very sensitive to the growth interface quality. Figure 6.18(b) shows a scanning electron microscope image of a fabricated MESFET, Figure 6.18(c) and (d) present source drain current-gate voltage (I_{DS}-V_G) and transfer curves after the first and second ELO cycles. To compare the performance of the MESFETs, I_{DS}-V_{DS} and I_{DS}-V_G characteristics are measured using a Keithley 4200-SCS semiconductor characterization system. Ohmic contact formation for the source and drain using low temperature annealing is confirmed by comparing the resistance between source and drain without a gate contact. We find the contact changes from slight Schottky-like to ohmic behavior following annealing. The transconductance characteristics of thin-film MEFETs are extracted from the transfer curve, and compared in Figure 6.18(e). The similar transconductances of 7.5 $\pm$ 0.5 mS and 8.5 $\pm$ 0.5 mS for the first and second ELO processed MESFETs, which is more than twice that of MESFETs fabricated with similar technology on glass substrates[16], shows that ND-ELO growth quality for these majority carrier electronic devices is not compromised by wafer recycling, epi-layer cleaning, and cold-weld bonding. Minor variations in device performance arise from variations in fabrication and growth from run-to-run.


a
Source/ Drain
Pd/ Ge/ Au (5/ 50/ 300 nm)
Gate
Ti/ Au (5/ 300 nm)
Active MESFET region
50 nm n++ 5 x 10^18 Si-doped GaAs
160 nm n 4 x 10^17 Si-doped GaAs
1000 nm un-doped GaAs
Metal bonding
Au (350 nm)


b
100 um


c
Fresh growth
Regrowth
Gate bias
0 V
-0.5 V
-1.0 V
-1.5 V
-2.0 V
-2.5 V
Source/Drain current (A)
Source/Drain bias (V)


d
Fresh growth
Regrowth
Source/Drain current (A)
Gate bias (V)

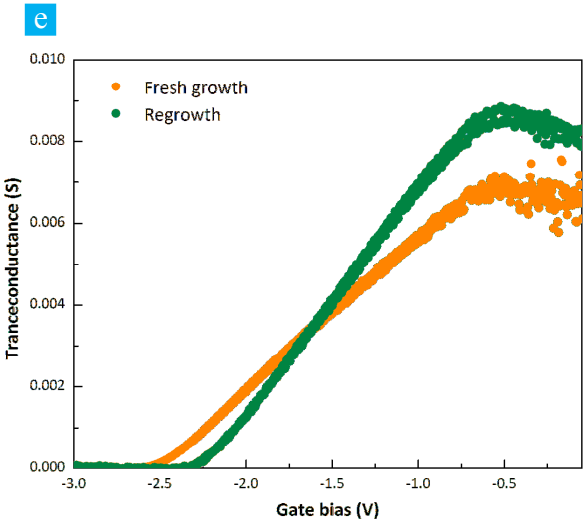

e
Fresh growth
Regrowth
Tranceconductance (S)
Gate bias (V)

Figure 6.18: Thin-film *n*-GaAs MESFETs. (a) Device structure of thin film *n*-GaAs MESFETs. (b) Microscope image of the MESFET after transfer and thermally assisted cold-weld bonding to the plastic substrate. (c) Source-drain current versus source-drain voltage (I_{DS}-V_{DS}) characteristics measured under various gate biases (V_G), (d) Source-drain current versus gate voltage (I_{DS}-V_G) transfer characteristics at V_{DS} = 3 V, and (e) Transconductance after the first and second ND-ELO-processed MESFETs from a single parent wafer. Differences in characteristics are due to variations in device processing from run to run.

6.3. Conclusion

The nearly identical performance of both minority (solar cells and LEDs) and majority (MESFETs) carrier devices that are grown and lifted-off from as-delivered and reused wafers confirms the feasibility of our ND-ELO wafer reuse process, as well as the generality of the fabrication methods using epitaxial protection layers and substrate cleaning combined with cold-weld bonding to a secondary substrate. The protection layers preserve the surface quality during the ELO process, as well as eliminate the wafer thinning issue caused by conventional polishing. Therefore, this method allows for potentially unlimited wafer recycling. Furthermore, all devices are directly fabricated on a flexible thin-film plastic substrate instead of rigid and bulky platforms such as glass or Si, thereby eliminating the need to transfer the fragile epitaxial active regions twice as is required in conventional ELO processing. In addition, the acceleration of the lift-off process via external strain makes this process compatible for use with large area substrates. The extreme flexibility of this approach makes it useful for deploying the mounted substrates on compact roles prior to unfurling for a particular application (i.e. area coverage by solar cells for terrestrial or space-borne purposes), as well as lending itself to simplified attachment of devices on conformal or pre-deformed substrate surfaces[17, 18].

In summary, we have demonstrated a universal method for creating a variety of very low cost GaAs-based single crystalline thin-film optoelectronic devices including photovoltaic cells, LEDs and MESFETs. The process involves a unique, non-destructive ELO process that allows for multiple growth and active epitaxial film removal cycles, thereby transforming the conventional high cost of materials associated with the substrate to a capital cost. We developed unique methods for substrate bonding, wafer protection and cleaning, and combined them with ND-ELO to avoid the typically wafer consuming repolishing step. A non-destructive substrate reuse method without performance degradation provides the potential for dramatic production cost reduction along with extending the application of high performance group III-V optoelectronic devices by moving from bulky, two dimensional substrate-based platforms to conformal, flexible and lightweight thin film devices. This technology is a critical step towards allowing III-V devices to overcome the cost barriers impeding their widespread acceptance in mainstream commercial applications.

CHAPTER VI

Bibliography

1. A. W. Bett, F. Dimroth, G. Stollwerck, O. V Sulima, *Appl. Phys. A Mater. Sci. Process.* **1999**, *69*, 119.

2. S. Mokkapati, C. Jagadish, *Mater. Today* **2009**, *12*, 22.

3. M. Konagai, M. Sugimoto, K. Takahashi, *J. Cryst. Growth* **1978**, *45*, 277.

4. G. J. Bauhuis, P. Mulder, E. J. Haverkamp, J. J. Schermer, E. Bongers, G. Oomen, W. Köstler, G. Strobl, *Prog. Photovoltaics Res. Appl.* **2010**, *18*, 155.

5. J. Adams, V. Elarde, A. Hains, C. Stender, F. Tuminello, C. Youtsey, A. Wibowo, M. Osowski, *IEEE J. Photovoltaics* **2013**, *3*, 899.

6. C.-W. Cheng, K.-T. Shiu, N. Li, S.-J. Han, L. Shi, D. K. Sadana, *Nat. Commun.* **2013**, *4*, 1577.

7. G. J. Bauhuis, P. Mulder, E. J. Haverkamp, J. C. C. M. Huijben, J. J. Schermer, *Sol. Energy Mater. Sol. Cells* **2009**, *93*, 1488.

8. K. Lee, K.-T. Shiu, J. D. Zimmerman, C. K. Renshaw, S. R. Forrest, *Appl. Phys. Lett.* **2010**, *97*, 101107.

9. K. Lee, J. D. Zimmerman, X. Xiao, K. Sun, S. R. Forrest, *J. Appl. Phys.* **2012**, *111*, 033527.

10. O. D. Miller, E. Yablonovitch, S. R. Kurtz, *IEEE J. Photovoltaics* **2012**, *2*, 303.

11. I. Schnitzer, E. Yablonovitch, C. Caneau, T. J. Gmitter, A. Scherer, *Appl. Phys. Lett.* **1993**, *63*, 2174.

12. L. C. Wang, P. H. Hao, B. J. Wu, *Appl. Phys. Lett.* **1995**, *67*, 509.

13. K.-T. Shiu, J. Zimmerman, H. Wang, S. R. Forrest, *Appl. Phys. Lett.* **2009**, *95*, 223503.

14. E. Yablonovitch, T. Gmitter, J. P. Harbison, R. Bhat, *Appl. Phys. Lett.* **1987**, *51*, 2222.

15. J. Yoon, S. Jo, I. S. Chun, I. Jung, H.-S. Kim, M. Meitl, E. Menard, X. Li, J. J. Coleman, U. Paik, J. A. Rogers, *Nature* **2010**, *465*, 329.

16. N. J. Smeenk, J. Engel, P. Mulder, G. J. Bauhuis, G. M. M. W. Bissels, J. J. Schermer, E. Vlieg, J. J. Kelly, *ECS J. Solid State Sci. Technol.* **2012**, *2*, P58.

17. S. Osakabe, S. Adachi, *Jpn. J. Appl. Phys.* **1997**, *36*, 7119.

18. Y. Ishikawa, *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.* **1994**, *12*, 2713.

19. Y. M. Song, Y. Xie, V. Malyarchuk, J. Xiao, I. Jung, K.-J. Choi, Z. Liu, H. Park, C. Lu, R.-H. Kim, R. Li, K. B. Crozier, Y. Huang, J. A. Rogers, *Nature* **2013**, *497*, 95.

20. X. Xu, M. Davanco, X. Qi, S. R. Forrest, *Org. Electron.* **2008**, *9*, 1122.

Chapter VII

Transforming the Cost of Solar-to-Electrical Energy Conversion:

Integrating Thin-Film GaAs Solar Cells with Non-Tracking Mini-Concentrators

Practical solar energy solutions must not only reduce the cost of the module, but also address the substantial balance of system costs. Here we demonstrate a counter-intuitive approach based on gallium arsenide (GaAs) solar cells that can achieve extremely low-cost solar energy conversion with an estimated cost of only 3% of conventional GaAs solar cells using an accelerated, non-destructive epitaxial lift-off (ND-ELO) wafer recycling process integrated with a lightweight, thermoformed plastic, truncated mini-compound parabolic concentrator (CPC) that avoids the need for active solar tracking. Using solar cell/CPC assemblies whose orientation is adjusted only a few times per year, the annual energy harvesting is increased by 2.8 times compared with planar solar cells without solar tracking. These results represent a potentially drastic cost reduction in both the module and balance of systems costs compared with heavy, rigid conventional modules and trackers that are subject to wind loading damage and high installation costs.

7.1. Introduction

Due to the nearly unlimited abundance of solar energy, photovoltaic cells that convert sunlight directly into electricity, represent the most promising alternative energy source. However, cost-efficient solar-to-electrical energy harvesting still remains a major hurdle that needs

to be fully surmounted if we are to expect its eventual widespread deployment. Considerable efforts in developing photovoltaics have therefore focused on achieving low cost while increasing their power conversion efficiency (*PCE*)[1]. One recent achievement has been the demonstration of thin-film GaAs solar cells approaching their thermodynamic efficiency limit[2,3,4,5]. However, the cost reduction long promised by the ELO process has primarily been limited by the inability to fully recover the original wafer surface quality after each growth leading to a limited number of times the substrate can be recycled due to accumulation of defects, and due to wafer thinning incurred by chemo-mechanical polishing[6,7,8,9,10]. Furthermore, high *PCE* alone does not necessarily translate into low cost solar energy production when expensive active materials and fabrication processes are used in their manufacture. As an alternative to simply improving the *PCE*, solar concentrators have been demonstrated as a means for reducing the use of costly active solar cell materials[11]. However, most concentrators suffer from a significant roll-off in efficiency at large light incident angles and can also result in high cell operating temperatures, thereby necessitating expensive active solar tracking and solar cell cooling systems[12].

Here we demonstrate that the integration of thin-film GaAs solar cells produced by an accelerated ND-ELO fabrication process, and integrated with simple, thermoformed mini-concentrators can lead to dramatic reductions in the cost of the production of electricity via solar energy harvesting. This approach reduces cell materials and fabrication costs to only 3% of that of analogous substrate-based GaAs cells, and only 11% of ELO-processed GaAs solar cells, while the optical system maximizes the annual energy output without requiring daily active solar tracking systems by using highly-truncated two dimensional mini-compound parabolic concentrators (CPCs). This low-profile concentrator provides a very thin and lightweight module with improved off-angle sunlight absorption compared to conventional concentrators both in direct, as well as

diffuse sunlight with only minor losses. Our approach, therefore eliminates the need for high concentration factor optics that require expensive and heavy solar tracking paraphernalia. Furthermore, the unique geometry of thin-film GaAs solar cells that are mounted on a heat-sinking metal layer enable operation at or near room temperature without active cooling, even for concentration factors approaching 4×, representing a reduction of over 40ºC when compared to substrate-based GaAs solar cells.

7.2. Experiments and results

7.2.1 Epitaxial growth

The solar cell epitaxial layer structures are grown by gas-source molecular beam epitaxy (GSMBE) on Zn-doped (100) p-GaAs substrates. The growth starts with a GaAs buffer layer (0.2 μm thick) followed by InGaP/GaAs (100 nm/100 nm) protection layers, and the AlAs (20 nm) sacrificial layer. Next, an inverted active device region is grown as follows: 5×10^{18} cm^{-3} Be-doped GaAs (0.15 μm) contact layer, 2×10^{18} cm^{-3} Be-doped $Al_{0.20}In_{0.49}Ga_{0.31}P$ (0.025 μm) window, 1×10^{18} cm^{-3} Be-doped p-GaAs (0.15 μm) emitter layer, 2×10^{17} cm^{-3} Si-doped n-GaAs (3.0 μm) base, 6×10^{17} cm^{-3} Si-doped $In_{0.49}Ga_{0.51}P$ (0.05 μm) back surface field (BSF) layer, and 5×10^{18} cm^{-3} Si-doped n-GaAs (0.1 μm) contact layer. The GaAs/AlAs layers are grown at 600 °C and $Al_{0.20}In_{0.49}Ga_{0.31}P$/ $In_{0.49}Ga_{0.51}P$ layers at 480 °C.

7.2.2 Accelerated ND-ELO

Figure 7.1(a) shows the fabrication sequence of the thin-film GaAs solar cells via the combination of rapid ND-ELO and cold-weld bonding[6]. The previously described ND-ELO method employs epitaxial protection layers grown between the sacrificial layer and the wafer that completely preserves the original wafer surface quality, even at the atomic scale, during the ELO

process[6,7]. Selective removal of protection layers using wet chemical etching eliminates the need for chemo-mechanical polishing used in conventional ELO. Therefore, ND-ELO allows for the nearly indefinite reuse of the GaAs substrates, converting their cost from a materials expense into a capital investment. To accelerate conventional ELO that takes several hours to separate the active epitaxy from even a small wafer, a 350 nm thick Au layer deposited onto the epitaxial layer surface is photolithographically patterned using a LOR 3A and S-1827 (Microchem) bi-layer photoresist to form a mask for the formation of an array of 2.5 mm × 6.5 mm mesas separated by 500 μm wide trenches by wet chemical etching using H_3PO_4:H_2O_2: deionized H_2O (3:1:25) and HCl: H_3PO_4 (3:1) for GaAs and InGaP, respectively that terminates at the active solar cell epitaxy/AlAs sacrificial layer interface. Immediately following mesa etch, the sample is cold-weld bonded to a Cr/Au (4 nm/ 350 nm) coated 25 μm-thick E-type Kapton® sheet by application of 4 MPa of pressure with a 80 N/sec ramp rate at a temperature of 230 ℃ for 8 mins using an EVG 520 wafer bonder at ~10^{-5} torr, where the patterned Au on the wafer is used for the bonding interface[6,13,14,15]. The substrate is then rapidly cooled. To apply uniform pressure, a soft graphite sheet is inserted between the sample and the press head. Once the GaAs substrate fully adheres to the Kapton® sheet, the thin active device region is removed from its parent substrate using ND-ELO[6]. The sample is immersed in a 20% HF:H_2O maintained at 60℃ while agitating the solution with a stir bar at 900 rpm. The total lift-off time is 30 min.

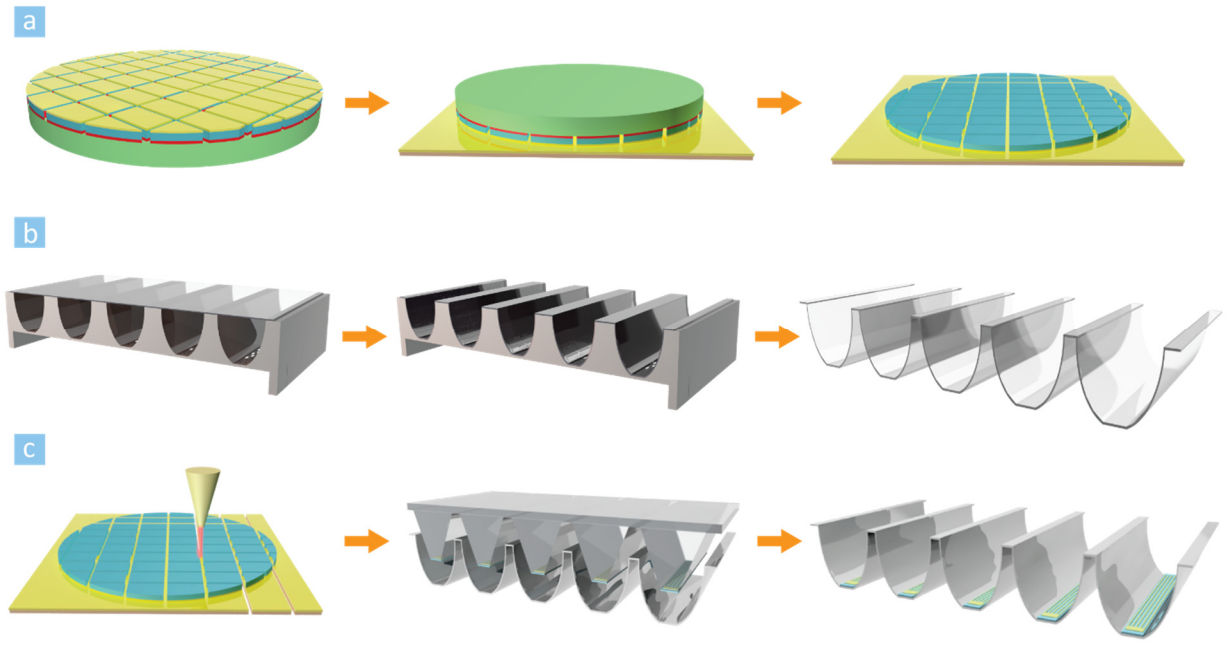


Fig. 7.1: Illustration of the fabrication steps for integration of compound parabolic concentrators (CPCs) with thin-film GaAs solar cells. (a) Proceeding left to right: Mesas are pre-patterned prior to non-destructive epitaxial lift-off (ND-ELO) by selective etching that stops at the AlAs sacrificial layer (red). The sample is then bonded onto the Au coated Kapton® sheet via cold-welding. The third step shows the sample following ND-ELO. (b) The PETG sheet is fixed on top of the metal mold, then the PETG is thermoformed into its final shape by applying heat and vacuum. Finally, the mini-CPCs are detached from the mold. (c) The solar cell-Kapton® sheet assembly is separated into individual bars using laser dicing. Then, each bar is transfer printed onto the mini-CPCs using a PDMS stamp via low-pressure cold-welding. The last schematic shows the integrated thin film solar cells and mini-CPC after reflective metal coating is deposited onto the CPC array surface.

7.2.3 Solar cell fabrication

Following lift-off, the thin-film active region and flexible plastic host is fixed to a rigid substrate using Kapton® tape. The front surface contact grid is photolithographically patterned using the LOR 3A and S-1827 (Microchem) bi-layer photoresist; then a Pd(5 nm)/Zn(20 nm)/ Pd(20 nm)/Au(700 nm) metal contact is deposited by e-beam evaporation. The widths of the grid

and bus bar are 20 μm and 150 μm, respectively, and the spacing between the grid fingers is 300 μm. The total coverage of the solar cell active area by the metallization is 4%. After the metal layer is lifted-off, the highly-doped 100 nm *p*++ GaAs contact layer is selectively removed by plasma etching. The thin-film solar cells are annealed in air for 1 hr at 200 °C to form ohmic contacts. An anti-reflection coating bilayer comprised of 49 nm thick TiO_2 and 81 nm thick MgF_2 is deposited by e-beam evaporation.

7.2.4 Laser dicing of thin-film GaAs solar cells on plastic sheet

A CO_2 laser engraving and cutting system (X-660 superspeed-600, Universal Laser Systems, Inc.) is used to dice the non-destructive epitaxial lift-off (ND-ELO) processed thin-film GaAs solar cells bonded to a Kapton® sheet. The solar cells on the plastic sheet are covered by a plastic film to protect them from debris generated during dicing. To confirm the feasibility of the laser dicing process, linear and zig-zag cut patterns, with 750 μm and 500 μm spacing between the active solar cell active areas, respectively, are demonstrated (Figure 7.2(a) and (b)). Improved material utilization by reducing the 300 μm kerf is possible. Figure 7.2(c) and (d) shows the area loss due to the cut geometry. For 6 inch wafers, the area loss is ~27% and 6.2% for single square and bar shaped cuts, respectively. Therefore, the wafer material utilization is improved by ~21% by increasing the cell packing density.

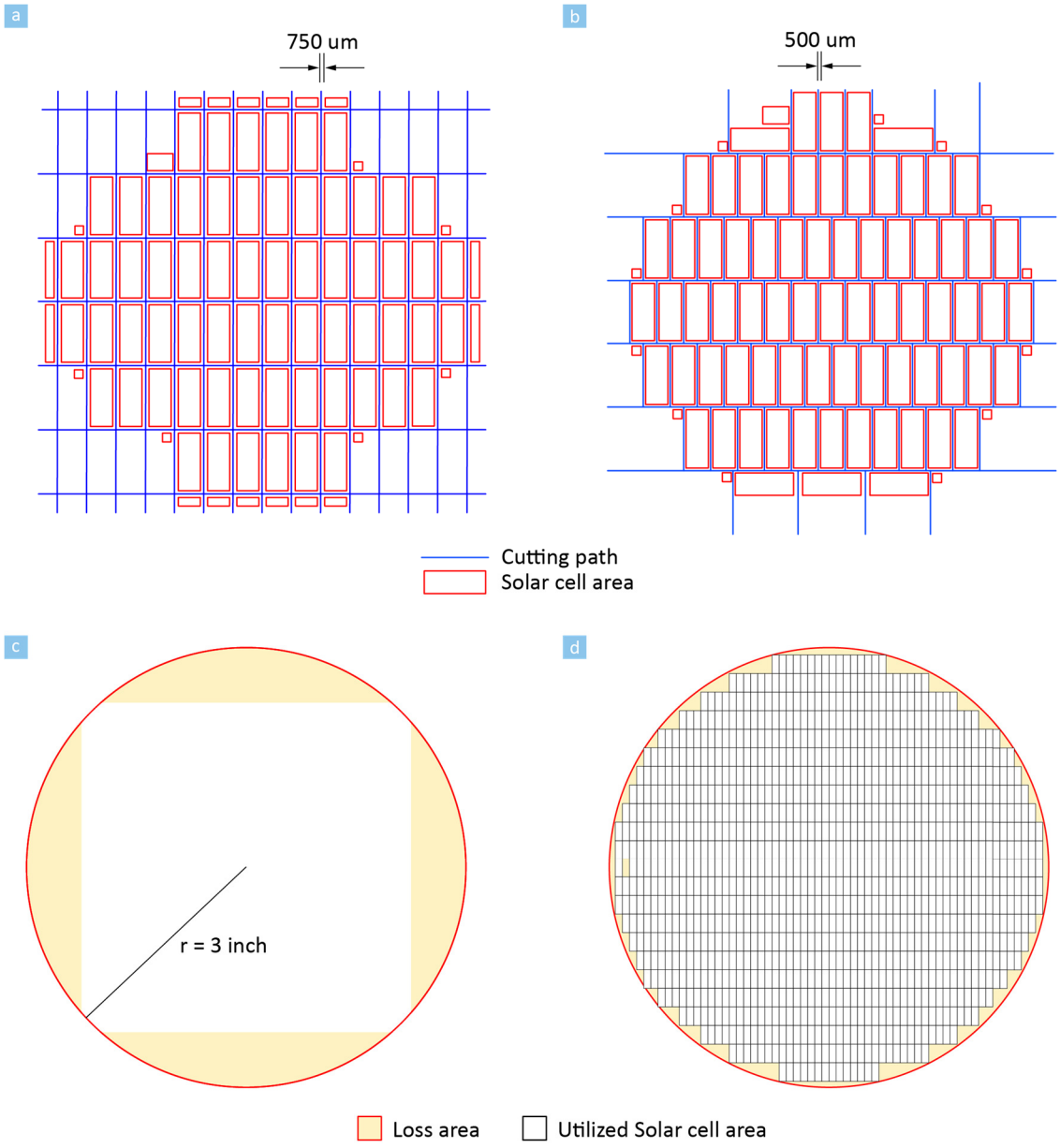


Fig. 7.2 Laser dicing of thin-film GaAs solar cells on plastic sheet (a) Linear cutting pattern with 750 µm spacings between solar cells. (b) Zig-zag cutting pattern with 500 µm spacing between solar cells. Schematic illustration of wafer utilization for (c) single square cut and (d) multiple small bar shape (2.5 mm × 6.5 mm) cut.

7.2.5 Thermoforming of plastic-CPC and adhesive-free transfer printing.

Figure 7.1(b) illustrates the thermoforming process used in fabricating the mini-CPCs. The process employs three molds: a metal mold in which to shape the thermoformed CPC, another

for making an elastomeric stamp to transfer the solar cells onto the substrate, and a third to assist in solar cell alignment.

The process for fabricating the CPCs and integration with the solar cells is as follows: A 0.75 mm thick polyethylene terephthalate glycol-modified (PETG) sheet is employed for the concentrators due to its low glass transition temperature (81°C), making it possible to shape by simultaneously applying heat and vacuum[16]. First, the PETG is fixed with Kapton® tape across the top of a metal mold containing holes at its base. While vacuum is applied through the holes, the assembly is placed in an oven at 60°C. The PETG is drawn into the mold as the oven temperature is raised to 96°C for ~15 min, forming the compound parabolic shape. The CPC is then cooled, after which CPC is detached from the metal mold. To transfer the diced, thin-film solar cells onto the thermoformed CPCs, an elastomeric PDMS stamp is prepared using an acrylonitrile butadiene styrene plastic mold (Fig. 7.1(c)) that is shaped using a 3D printer (Dimension Elite, Stratasys). Figure 7.3(a) shows the detailed dimensions and photographs of the mold for the PDMS stamp, which is designed to exactly fit into the CPC opening shown in Figure 7.3(b). An additional 3D printed mold is used to align the solar cell strips for pick-up by the PDMS stamp. The pyramid shape of the PDMS stamp prevents direct contact between the stamp and the side walls of the CPC so that pressure for bonding the solar cells is only applied onto the CPC base. Figure 7.3(c) is a schematic of the fit between the stamps and CPCs.

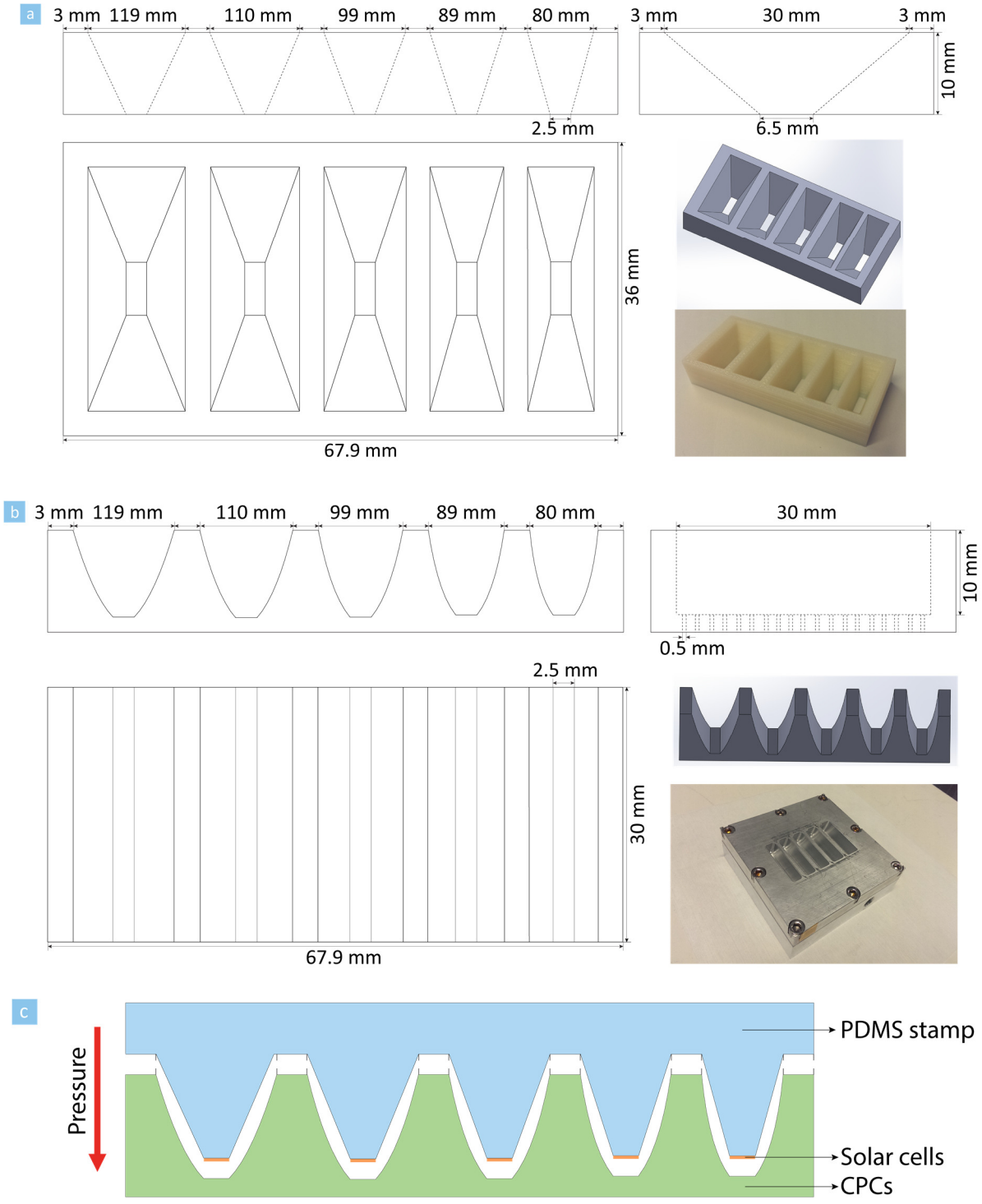


Fig. 7.3 Self-aligned transfer printing process (a) Mold design for the PDMS stamp. Image shows a 3D printed mold. (b) Mold design for the plastic CPCs. Image shows a mold made from a metal block. (c) Schematic illustration of the fit between the PDMS stamp and the plastic CPCs for solar cell transfer printing.

The CPC and Kapton® sheet beneath the solar cell strip are coated with Pd/Au (5 nm/100 nm) deposited through a shadow mask using electron beam evaporation. The solar cell strips are picked up by the PDMS stamp and transfer-printed onto the Au-coated plastic CPC via adhesive-free low-pressure cold-weld bonding[13] (Fig. 7.1(c)). A pyramid-shaped fixture is used to align the solar cell to the CPC without contacting its side walls (Figure 7.3(c)). Subsequently, the CPC is coated by a 500 nm thick reflecting Ag layer using vacuum thermal evaporation while screening the solar cell with a shadow mask. The metallic mirror coating can potentially enhance the CPC reliability under ambient and solar illumination conditions. Figure 7.4 shows images of the CPC and thin-film GaAs solar cells at several stages of fabrication.

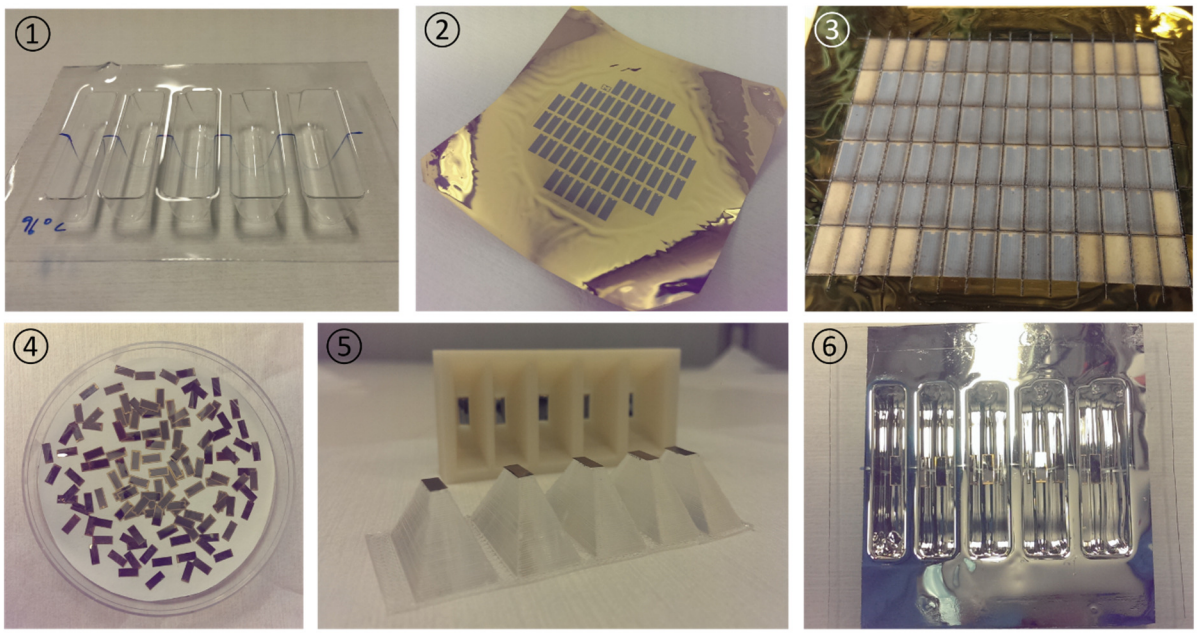


Fig. 7.4: Photographs of the fabrication steps for integration of compound parabolic concentrators (CPCs) with thin-film GaAs solar cells. ① PETG sheet after thermoforming into CPCs, ② Fabricated thin-film GaAs solar cells on a Kapton® sheet after mesa pre-patterning and ND-ELO, ③ Thin-film GaAs solar cells following dicing, ④ Separated and cleaned solar cell bars, ⑤ PDMS stamps and 3D printed mold used in transfer printing, and ⑥ Integrated thin-film GaAs solar cells integrated with plastic mini-CPCs.

7.2.6 Characterization of integrated CPC/thin-film GaAs solar cell assemblies

The CPC consists of two, rotated half parabolas joined together to achieve an acceptance angle that is determined by their tilt angle[17]. Previously, application of CPCs for solar energy generation has primarily focused on solar thermal energy conversion[18]. In fact, the combination of CPCs with photovoltaic cells has, up to this point been limited by their unwieldy, form factor, high aspect ratios and production costs compared with lens or mirror-based concentrators. To overcome this shortcoming, we employ the highly truncated (> 90%) design using low-cost plastic materials and fabrication processes. The combination of their high truncation ratios and half cylindrical symmetries enables concentration over a wide range of incident angles, thus completely eliminating the need for active tracking systems.

Figure 7.5(a) and (b) show schematics for a CPC comprised of two parabolas with tilted axes at an angle equal to its acceptance angle[17]. The plastic mini-CPCs are 2D, half cylinders to eliminate the need for solar tracking along its longitudinal axis. Figure 7.5(c) shows the effect of CPC truncation on the acceptance angle and concentration factor, *CF*. A non-truncated CPC shows the highest *CF* with no light collection outside of the acceptance angle. Although the *CF* is reduced with increased truncation, it is nevertheless able to collect light at much broader angles than the acceptance angle.

Ray tracing using Matlab software (MathWorks) was used to determine the *CF*. The geometry of the *CPC* is defined in Cartesian coordinates, and its four vertices are calculated using base width (defined by the dimensions of the GaAs solar cell), height, and acceptance angle. Note that the focal points of the two parabolas comprising the CPC form the base edges. We choose practical CPC heights (~8% of the untruncated *CPC*), where truncation alters the acceptance of input rays incident on the CPC, and hence the *CF*. We assume that the input rays are parallel.

Now, *CF* is the ratio of photons incident on the solar cell with CPC, to that without it. Due to the symmetry of the CPC about its central axis, only positive solar incident angles were considered, i.e., $0 < \theta_{sun} < \theta_{max}$, where θ_{sun} is the angle of the rays with respect to the central axis of CPC, and θ_{max} is the angle at which all incident rays are shadowed and thus, $CF \to 0$. Greater than 10,000 spatially distributed rays for each angle were used. When a ray is reflected by the CPC, its intensity is reduced by the reflectance of Ag, which was measured on PETG using a variable-angle spectroscopic ellipsometer (VASE, J.A. Woollam) and a UV/Vis/NIR Spectrophotometer (LAMBDA 1050, Perkin Elmer). The range of wavelengths and angles was 300 nm to 900 nm with 3 nm steps, and from 15^{o} to 85^{o} with 5^{o} steps. The values between those measured are interpolated. Then, the wavelength and incident angle dependent reflectance is weighted by the AM1.5G solar spectrum. Finally, *CF* vs. θ_{sun} and acceptance angle is calculated.

Figure 7.5(d) and (e) show contour plots of *CF* vs. incident angle calculated for various CPC shapes. Figure 7.5(d) shows the case of a non-truncated CPC where *CF* increases as the angle between each parabola axis (i.e. the acceptance angle) decreases. Figure 7.5(e) shows the case of CPCs with a fixed aspect ratio of 4 (CPC height/solar cell width) such that the truncation ratio depends on the acceptance angle. The truncation ratios of CPCs with narrow acceptance angles are higher than for wide acceptance angles.

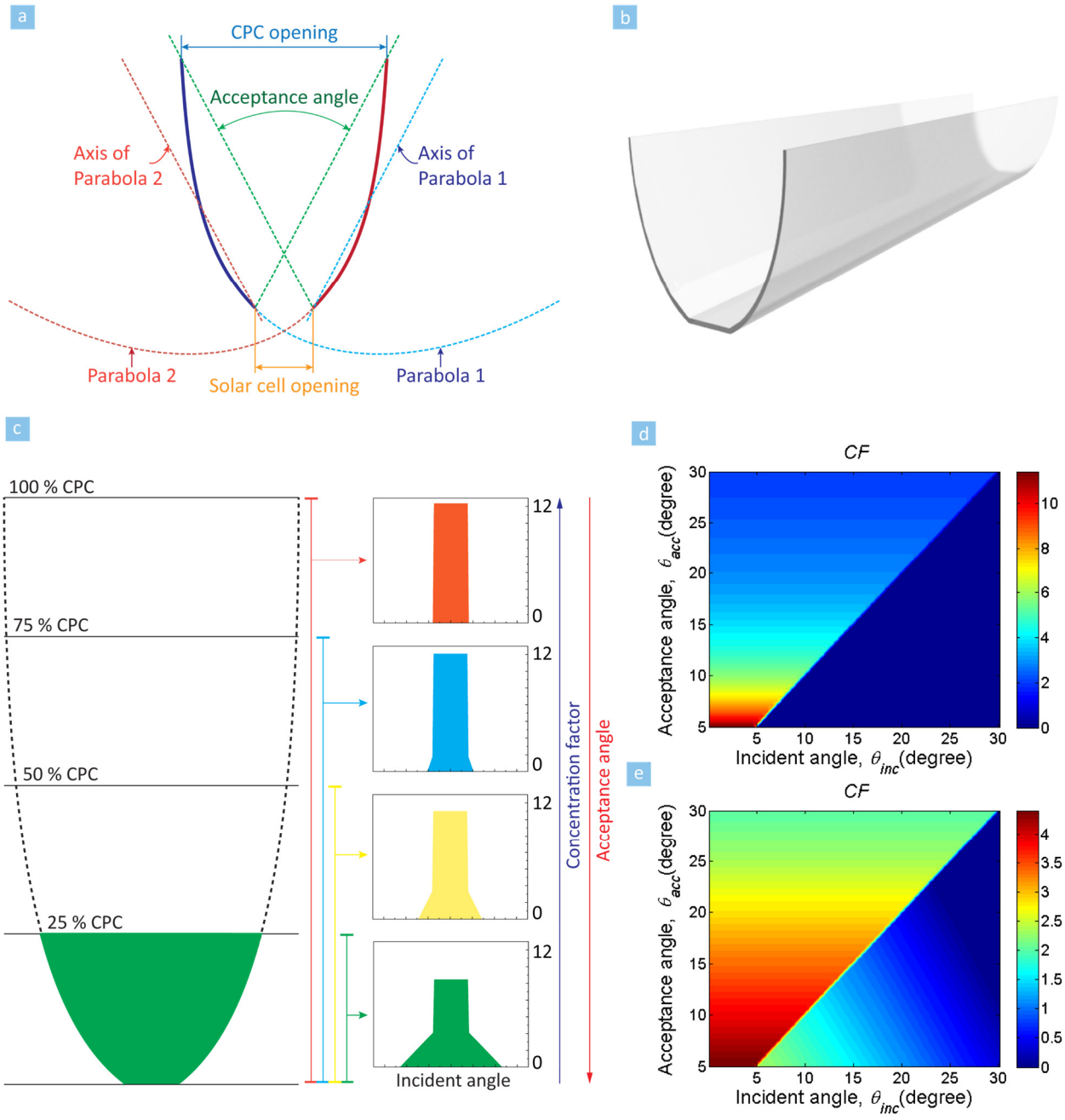


Fig. 7.5 Two dimensional mini-compound parabolic concentrator (CPC) design. Schematic illustration of the (a) CPC shape and (b) 2 dimensional CPCs. (c) Effect of CPC truncation on the acceptance angle and concentration factor. Contour plot of light incident angle dependent concentration factors for various shapes of (d) non-truncated, and (e) truncated CPCs.

Figure 7.6(a) shows the current-voltage (*I-V*) characteristics of the thin-film GaAs solar cells measured under simulated AM 1.5G illumination at 1 sun (100 mW/cm^2) intensity, both in a conventional planar configuration, and integrated with the variously shaped thermoformed CPCs with a fixed aspect ratio of 4 (corresponding to 2.5 mm wide solar cells with 10 mm high CPCs). The dependence of the concentration factor on the tilt angles of the axes of the parabolas, as inferred from the *I-V* characteristics along with the calculated values, are provided in Figure 7.6(b). A maximum concentration factor of 3.6 is achieved using a CPC with a 2.5^o axis tilt.

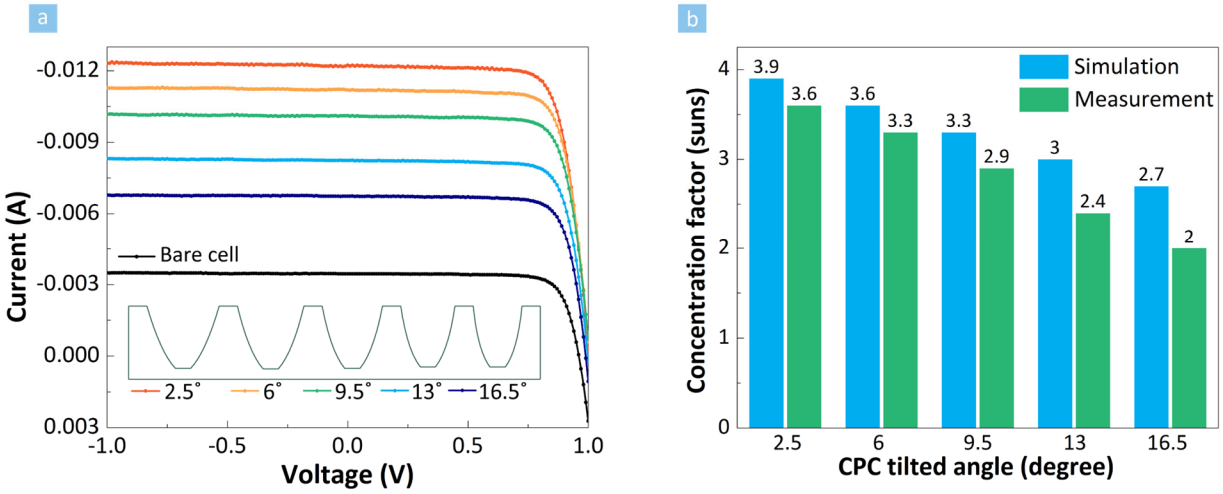


Fig. 7.6: Performance of thin-film GaAs solar cells and plastic mini-CPCs (a) Current versus voltage (*I-V*) characteristics of thin-film GaAs solar cells with and without various CPCs measured under 1 sun, AM1.5G simulated solar illumination. Inset shows the shape of each CPC along with their corresponding tilt angles. (b) Concentration factors depending on the tilt angle of the CPCs. Blue and green bars show simulated and measured concentration factors under AM 1.5G solar illumination, respectively.

The ND-ELO processed solar cell performance has a *PCE* = 18.4% and 17.9% with and without a 6^o tilted CPC, respectively. Figure 7.7(a)-(d) summarize the performance of the thin-film ND-ELO GaAs solar cells under various concentrated light conditions. The solar cells are integrated with the mini-CPCs and are measured using an Oriel solar simulator (model: 91191)

with a Xe arc lamp and AM 1.5 Global filter calibrated to 1 sun illumination (100 mW/cm^2). *I-V* characteristics are obtained with an Agilent 4155B parameter analyzer. The simulator intensity is calibrated using a National Renewable Energy Laboratory (NREL) certified Si reference cell with diameter of 5 mm. Short circuit current (J_{sc}), Open circuit voltage (V_{oc}), fill factor, and power conversion efficiency (*PCE*) are extracted from the *I-V* characteristics (Figure 7.6(a)). The measurement shows the power conversion efficiency of the cell integrated with a 6° tilted CPC with *CF* = 3.3 is slightly improved (~0.5%) compared to a non-concentrated device with one due to the increased open circuit voltage, V_{oc}, at higher intensities. The improved *PCE* using the concentrator is due to the increased open circuit voltage at higher light intensity.

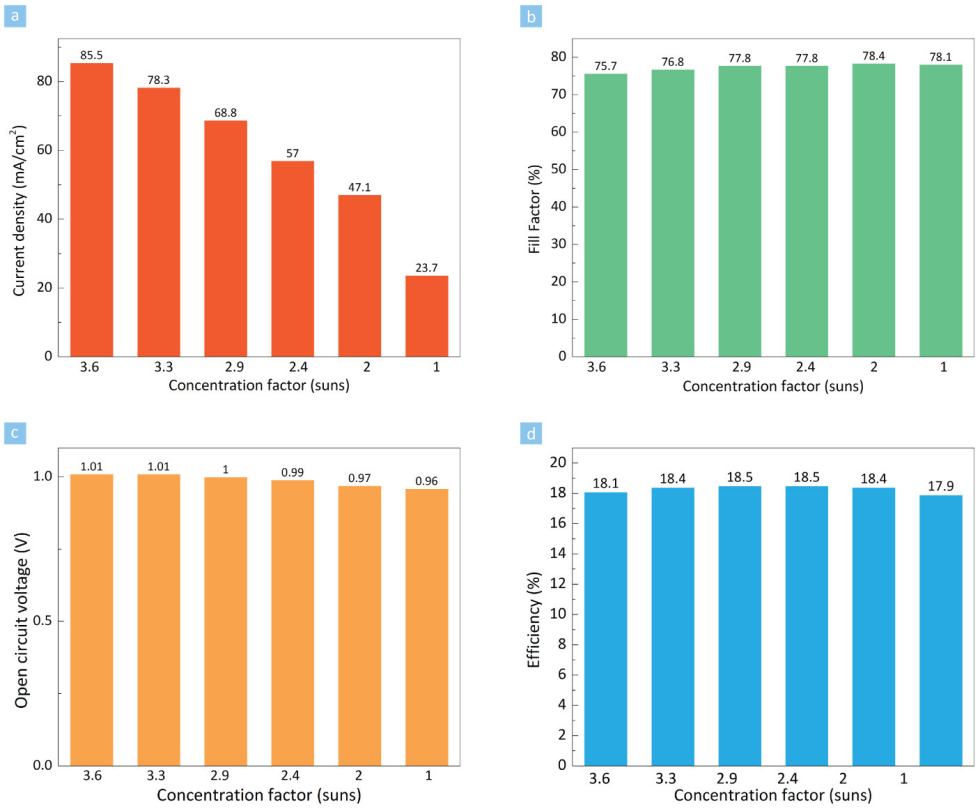


Fig. 7.7: Performance of the thin-film GaAs solar cells under the concentrated light (a) Short circuit current (b) open circuit voltage, (c) fill factor, and (d) power conversion efficiency of the thin-film GaAs solar cells under the various concentrated light conditions measured by their integration with the mini-CPCs.

Figure 7.8(a) shows both the measured and calculated values of the concentration factor as functions of the solar incidence angle for the 92% height-truncated, 6° tilted CPC under both direct and diffuse illumination. The measured peak concentration factor is 3.3, corresponding to 76% of the light incident on the concentrator aperture being directed onto the cell. The actual optical element also has an approximately 10° wider acceptance angle than calculated. Concentration losses are due to the rough light-scattering surfaces that result from the imperfect shape of the metal mold, and distortions created due to non-uniform thermal expansion of the PETG during thermoforming.

Light concentration vs. incidence angle was also characterized under diffuse illumination. The light incident angle is adjusted using an optical fiber and rotation stage (Newport, 481-A). The concentration factor under diffuse illumination (N-BK7 ground glass diffusers, 220 grit polish, Thorlab) is measured with an identical set-up. As a result of the wide collector acceptance angle, the measured concentration factor has a maximum of 3.2 suns, which is nearly identical with that obtained for specular illumination at normal incidence (Figure 7.8(a)). The reduced sensitivity of light concentration with solar position under diffuse, as well as direct sunlight confirms that the truncated CPC eliminates the need for active tracking.

The thermal performance of both substrate-based and thin film GaAs solar cells under 3.3 suns concentration is shown in Figure 7.8(b). The solar cell operating temperature is measured by a thermal imaging camera (A325, FLIR). Infrared images taken without heat sinking at an ambient temperature of 23.6℃ are shown in the inset. The thin-film cells are mounted onto a 700 nm thick Au film which is used for the contact, rear-side mirror, cold-weld bonding material, and heat-sink.

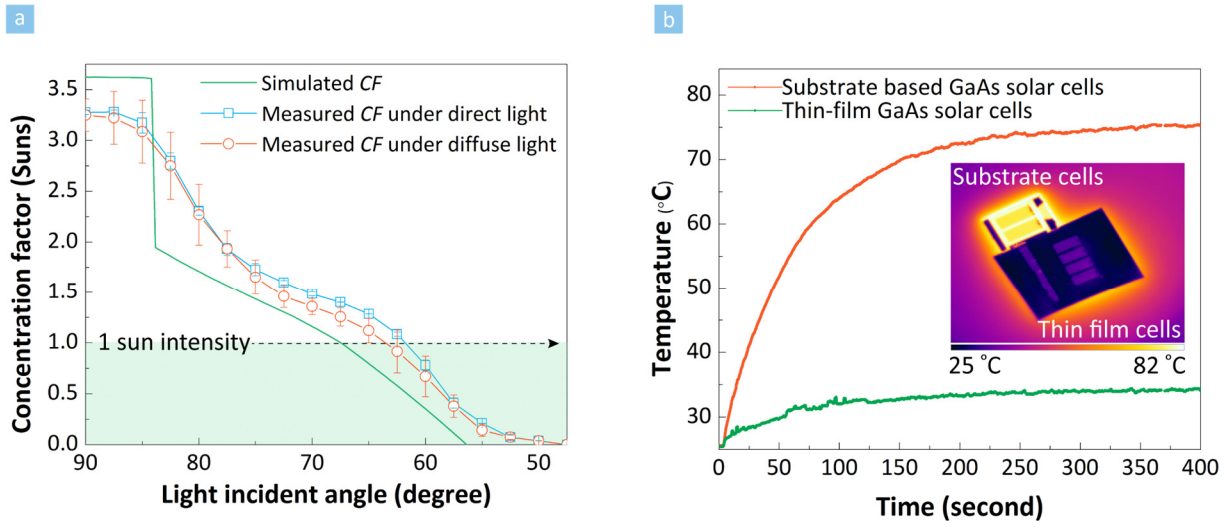


Fig. 7.8: Performance of thin-film GaAs solar cells and plastic mini-CPCs (a) Light incident angle dependent concentration factors for thin-film GaAs solar cells integrated with 6 ° tilted plastic mini-CPCs. The green solid line shows the simulated value. Blue and red dots with guide line show measured concentration factors under direct and diffuse illumination, respectively. (b) Operating temperatures of thin-film and substrate-based GaAs solar cells under AM1.5G simulated solar illumination at 3.3 suns concentration measured using an infrared (IR) camera. Inset shows the cell IR camera images.

The cells exhibit a 17ºC lower temperature under 1 sun illumination compared with analogous cells on a 350 µm thick GaAs substrate, and 41ºC lower operating temperature under 3 suns intensity. The near room temperature operation of thin-film solar cells is advantageous, since every 10ºC increase leads to decrease in *PCE* of ~0.7%[19]. Figure 7.9 shows the operating temperatures of thin-film and substrate-based GaAs solar cells under simulated AM 1.5G, 1 sun intensity (100mW/cm^2) illumination. After 250 s, the substrate-based GaAs solar cells operate around 45℃ as predicted[19], whereas the thin-film cells operate at 28℃.

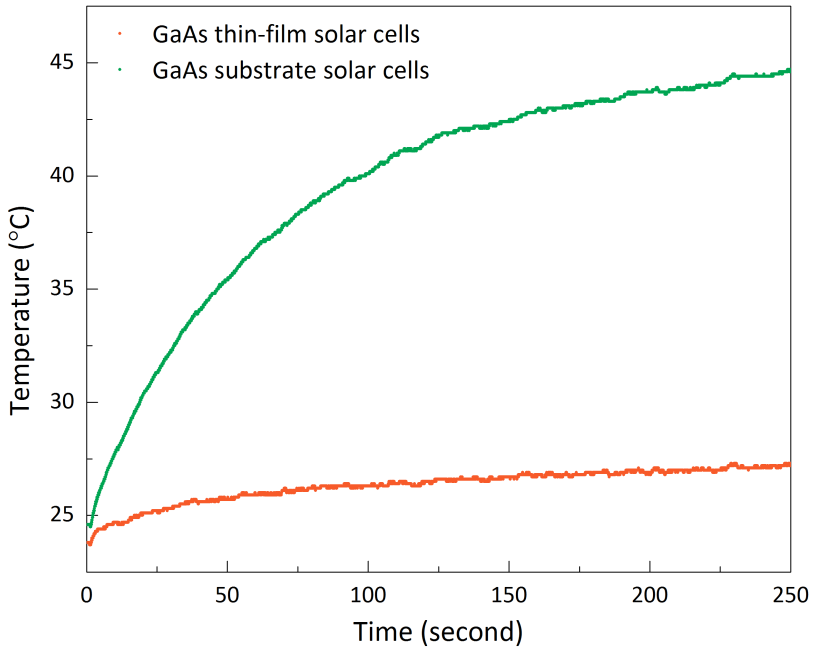


Fig. 7.9 Operating temperature of thin-film and substrate GaAs solar cells. Time dependent temperature measured by IR imaging under 1 sun illumination (100mW/cm^2).

7.2.7 Enhanced annual energy harvesting using CPC/thin-film GaAs solar cell assemblies

As noted, the mini-CPC is cylindrically symmetric, suggesting that it should be aligned along an east-west axis to provide the widest coverage of sunlight throughout the day simply by tilting its axis towards the zenith of solar declination path, with only occasional seasonal adjustments in tilt. Figure 7.10(a) and (b) shows east-west and north-south axis longitudinal CPC alignments. For north-south alignment, the CPC only collects light when the sun lies within the acceptance angle of the CPC; however, the east-west axis alignment provides a wide coverage of sunlight throughout the day by tilting it toward the solar declination path. The position of the CPC needs to be adjusted only 4 times per year for optimum energy harvesting since the acceptance angle of the CPC is sufficiently wide to cover the seasonal changes in the solar path.

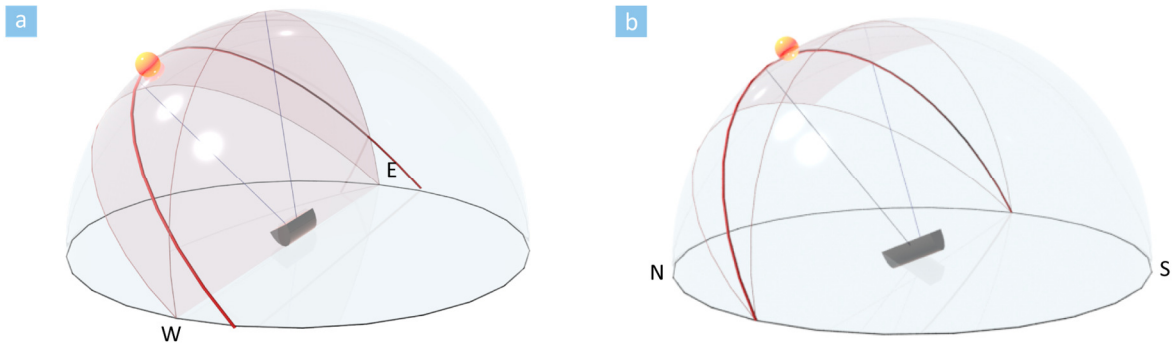
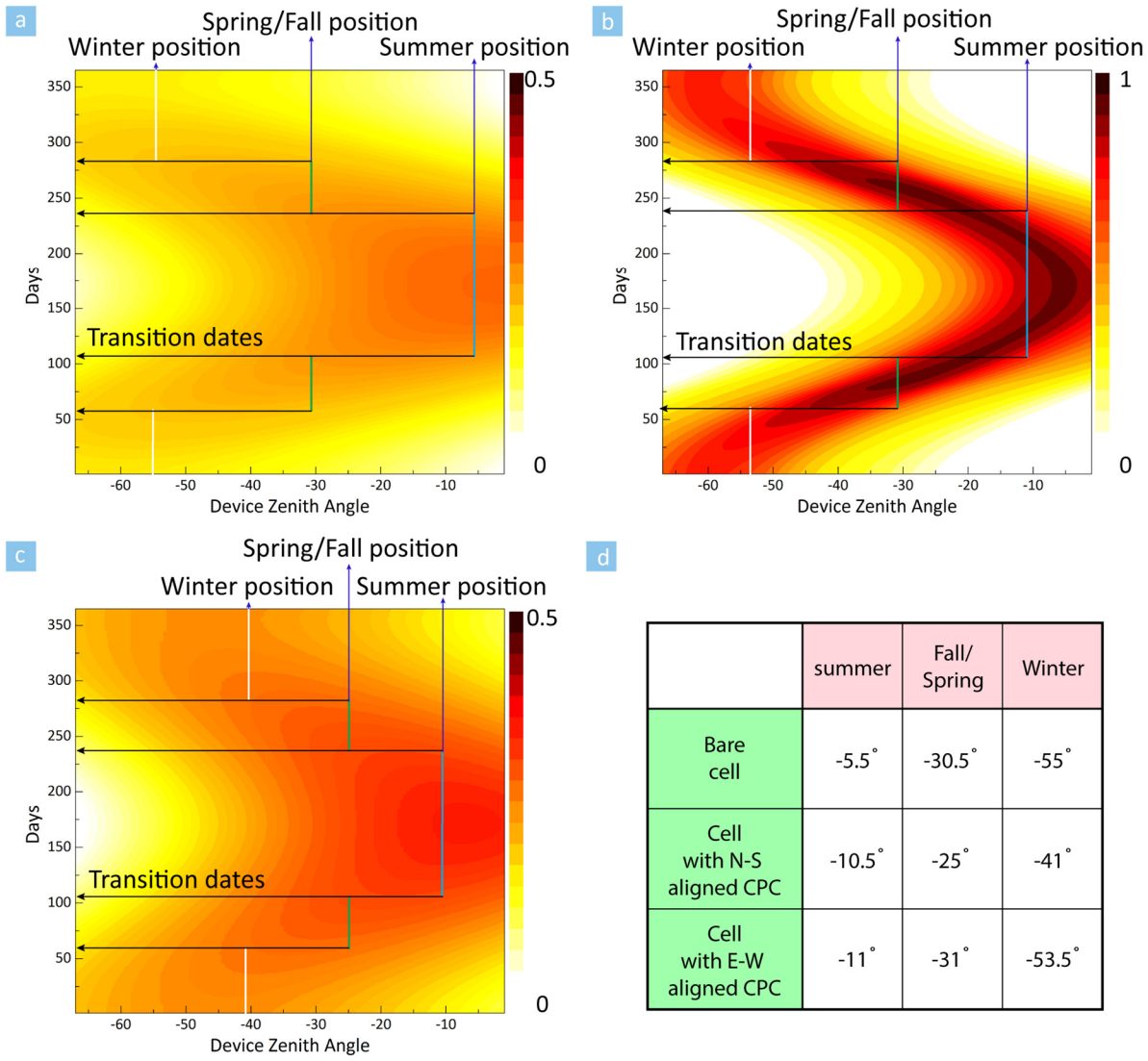


Fig. 7.10 Alignment of CPCs. Schematic of the CPC longitudinal axis aligned along an (a) east-west axis and (b) north-south axis.

To maximize the energy harvesting throughout the year, at Phoenix, AZ (33.4N, 112.1W), we first calculate the optimum seasonal alignment. Solar radiation intensity is then determined using time dependent zenith angles and air mass for each day of the year. Diffuse light is not considered for the calculation. The daily energy generation is then integrated over the entire year. The device tilt is iteratively changed, to generate a full contour mapping of the energy generation as both a function of southward tilt and day of the year.

Figure 7.11(a), (b) and (c) show the daily energy generated using the measured angle dependent *CF*s for a non-concentrated and a cell with 6° tilted a CPC aligned along north-south and east-west axes. Using the seasonal position shift of the solar path, we find the optimum CPC facing angle by maximizing the integrated energy generation with varying alignment angle. The optimum seasonal positions are summarized in Figure 7.11(d).



	summer	Fall/ Spring	Winter
Bare cell	-5.5°	-30.5°	-55°
Cell with N-S aligned CPC	-10.5°	-25°	-41°
Cell with E-W aligned CPC	-11°	-31°	-53.5°

Fig. 7.11 Optimum alignment of CPCs. Contour plot of energy harvesting for each day, depending on the CPC tilt angle of (a) non-concentrated cell, (b) east-west axis and (c) north-south aligned CPC. Solid lines indicate optimum seasonal CPC positions and transition dates for maximum yearly energy harvesting. (d) Summary of optimum seasonal facing angles for each case.

Fig. 7.12 shows the solar path at specific dates (Jan 1, April 1 and July 1) and the coverage of the 6º tilted CPC at seasonally adjusted tilt angles (i.e. adjusted to zenith angles of 11º / 31º / 53.5º only at the summer solstice, spring/fall equinoxes, and the winter solstice, respectively).

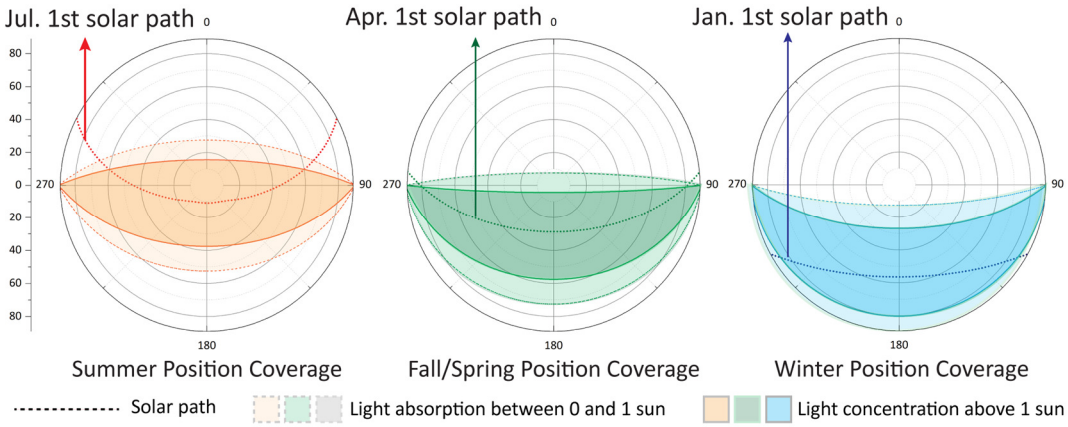


Fig. 7.12: **Optimum alignment of CPCs for maximum annual energy harvesting.** Polar plots showing coverage of CPC at its optimum seasonal positions.

To calculate the hourly, daily and yearly energy generation of thin-film GaAs solar cells with the plastic mini-CPCs, the air mass and zenith angle of the solar radiation are calculated at Phoenix, AZ. The solar position is calculated for every day of the year, and at 500 times during each day. The radiation incident on the device is calculated based on the air mass at that time. Figure 7.13(a) shows the hourly air mass and solar angles for two specific dates. Hourly and daily radiation intensity values, and the incident angle on the CPC are determined based on these calculations.

Figure 7.13(b)-(e) shows hourly and daily energy harvesting patterns of the thin-film GaAs solar cells with and without east-west aligned CPCs for four seasonal alignments per year. The CPC with a narrow acceptance angle shows high energy harvesting at specific dates but, is not able to completely cover the seasonal solar path. In contrast, CPCs with wider acceptance angles show almost full coverage of the solar path, although it shows a relatively low *CF*. The optimum design employs a 9.5° tilted CPC, although the 6° tilted CPC shows the best annual energy harvesting performance from the experimentally measured concentration factors due to an imperfect CPC shape and reflectance of the Ag film on PETG. Figure 7.13(f) shows the energy harvesting based on angle dependent *CF*s measured using a 6° tilted CPC.

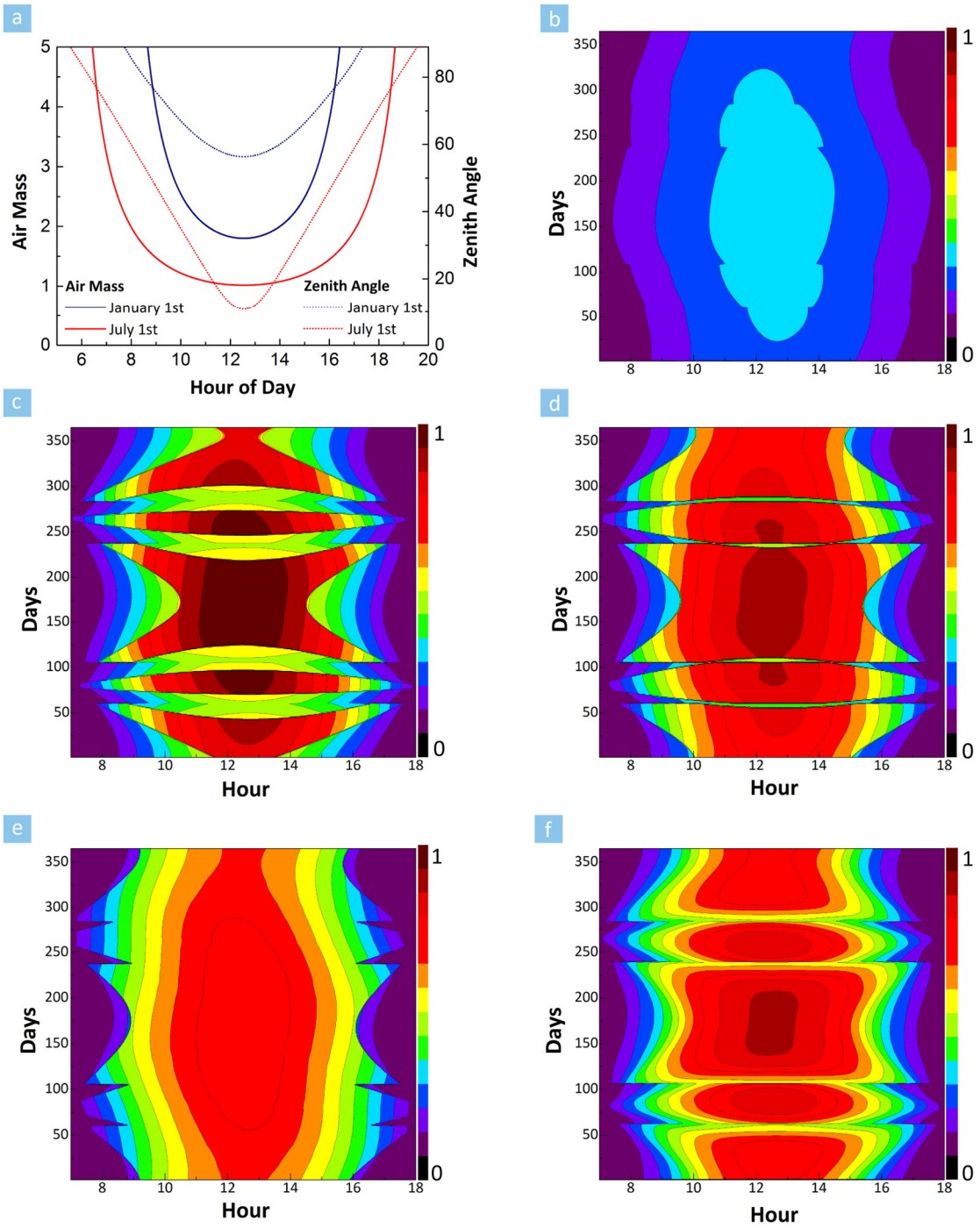


Fig. 7.13 Characterization of hourly, daily and yearly energy harvesting at Phoenix, AZ. (a) Air mass and zenith angle of sunlight calculated on Jan 1st and July 1st. (b) Simulated hourly and daily energy generation for (b) non-concentrated thin-film GaAs solar cells, and the thin-film GaAs solar cells with (c) 5°, (d) 9.5 ° and (e) 15 ° tilted CPC. (f) Hourly and daily energy harvesting based on measured angle-dependent concentration factors for the thin-film GaAs solar cells integrated with 6° tilted CPC.

Figure 7.14(a) and (b) show the energy harvesting on two specific dates during winter and summer, respectively, using a 6° tilted CPC. The wide acceptance angle enables the CPC to cover most of the useful daylight with low air mass. From the integration of hourly energy harvesting curves for thin-film GaAs solar cells with and without a CPC, we confirm that the ND-ELO processed solar cells integrated with a 6° tilted CPC shows 2.8 and 2.7 times higher energy harvesting compared with non-concentrated cells on January 1st and July 1st, respectively (Figure 7.14(c)). Figure 7.14(d) compares the non-concentrated, and the 2, 3 and 4 tilt positions per year.

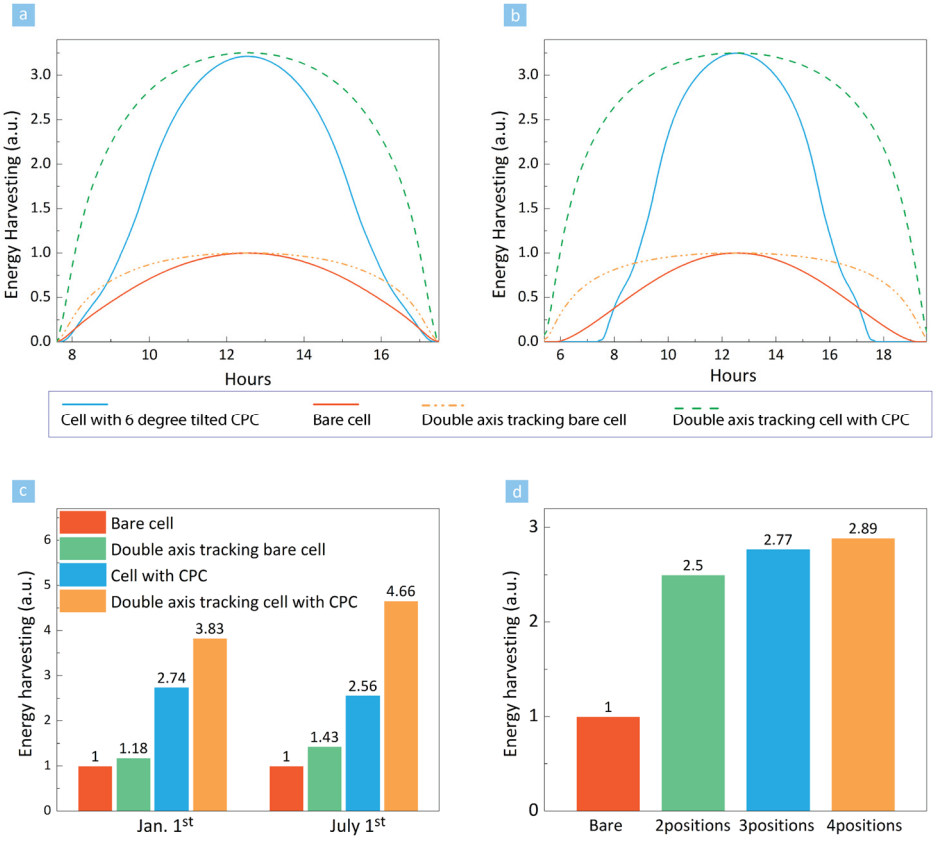


Fig. 7.14 Characterization of hourly and annual energy harvesting. Hourly energy generation using thin-film GaAs solar cells with and without a CPC for (a) January 1st and (b) July 1st at Phoenix, AZ. Dashed lines indicate the maximum energy harvesting case using a double axis tracking system. (c) Comparison of daily energy harvesting for January 1st and July 1st by integrating the curves in Fig. 7.14 (a) and (b). (d) Annual energy harvesting dependence on the number of CPC positions per year.

Figure 7.15(a) shows the daily and hourly trends of concentrated power generation using the 6° tilted CPC. The wide CPC acceptance angle allows for energy harvesting during the most useful hours of daylight straddling midday. Figure 7.15(b) shows the result of concentrated energy harvesting throughout the year using a thin-film GaAs solar cell with the 6° tilted CPC compared to conventional, non-concentrated cells. Both cases are calculated based on three seasonal positional adjustments each year. The inset of Fig. 7.15(b) compares the annual energy generation of concentrated and non-concentrated thin-film GaAs solar cells. We find that the total annual energy yield is 2.8× higher for the concentrated cells.

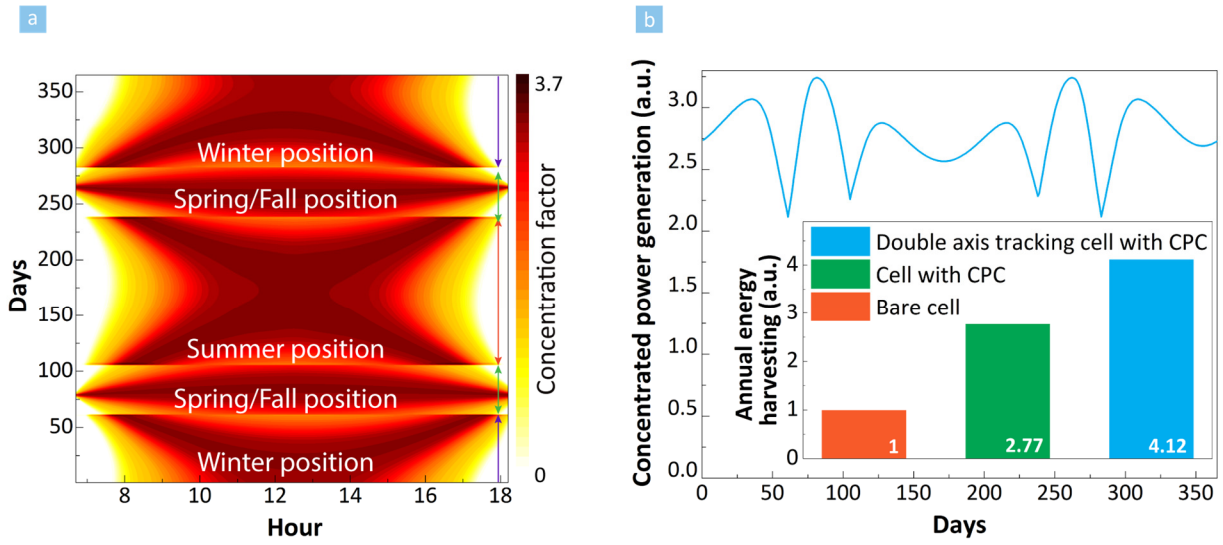


Fig. 7.15: **Optimum alignment of CPCs for maximum annual energy harvesting.** (a) Contour plot of daily and hourly concentration factors in Phoenix, AZ using a 6° tilted CPC. (b) Ratio of the daily concentrated energy harvesting factor for the thin-film GaAs solar cells with the 6° tilted CPC compared to a cell without concentration. Inset: Summary of annual power generation calculated from the integration of hourly and daily energy harvesting using thin-film GaAs solar cells with and without concentrators.

7.2.8 Production cost estimation

Ultimately, the most important figure of merit for any solar cell technology is the cost of energy generation. Hence, Fig. 7.16 shows estimated cost *reductions* using the combination of approaches demonstrated here, as compared with conventional GaAs-based methods[20,21]. Manufacturing costs of solar cells grown by metal organic vapor phase epitaxy (MOVPE) on 6 inch diameter round wafers are estimated based on the consideration of 24% cell efficiency, $150 per 6 inch wafer with a 27% area loss, 50 wafer reuses for both conventional ELO with wafer polishing and ND-ELO processing, 30% and 20% group III and V precursor utilization yields, 15 μm/hr growth rate, 70% CMP process yield, 9% margin, and miscellaneous expenditures (materials costs, labor, maintenance, utility and equipment depreciation)[21]. Module materials costs are estimated using the existing crystalline Si manufacturing costs without considering the expenses for module assembly (depreciation, labor, etc.)[20]. The loss of wafer area can be reduced by the increased packing density achieved by the bar shaped solar cells. Another significant cost is incurred in the chemo-mechanical polishing (CMP) process used in conventional ELO, which amounts to ~$8/repolishing at 70% yield[21]. This cost can be completely eliminated by the ND-ELO method which does not employ CMP[6]. Other assumptions for U.S. based manufacturing include[21]: 1) 0.25 labor cost per reactor and 1:0.35 direct:indirect labor ratio. Wages assumed are $12.05 /hr and $17.56 /hr with 55% benefits for unskilled and skilled workers. 2) 350 working days per year and 24 working hours per day (3 shifts). 3) $0.07 /kWh electricity price. 4) $500 /$m^2$ for class 1000 cleanroom cost. 6) 28% effective corporate tax rate.

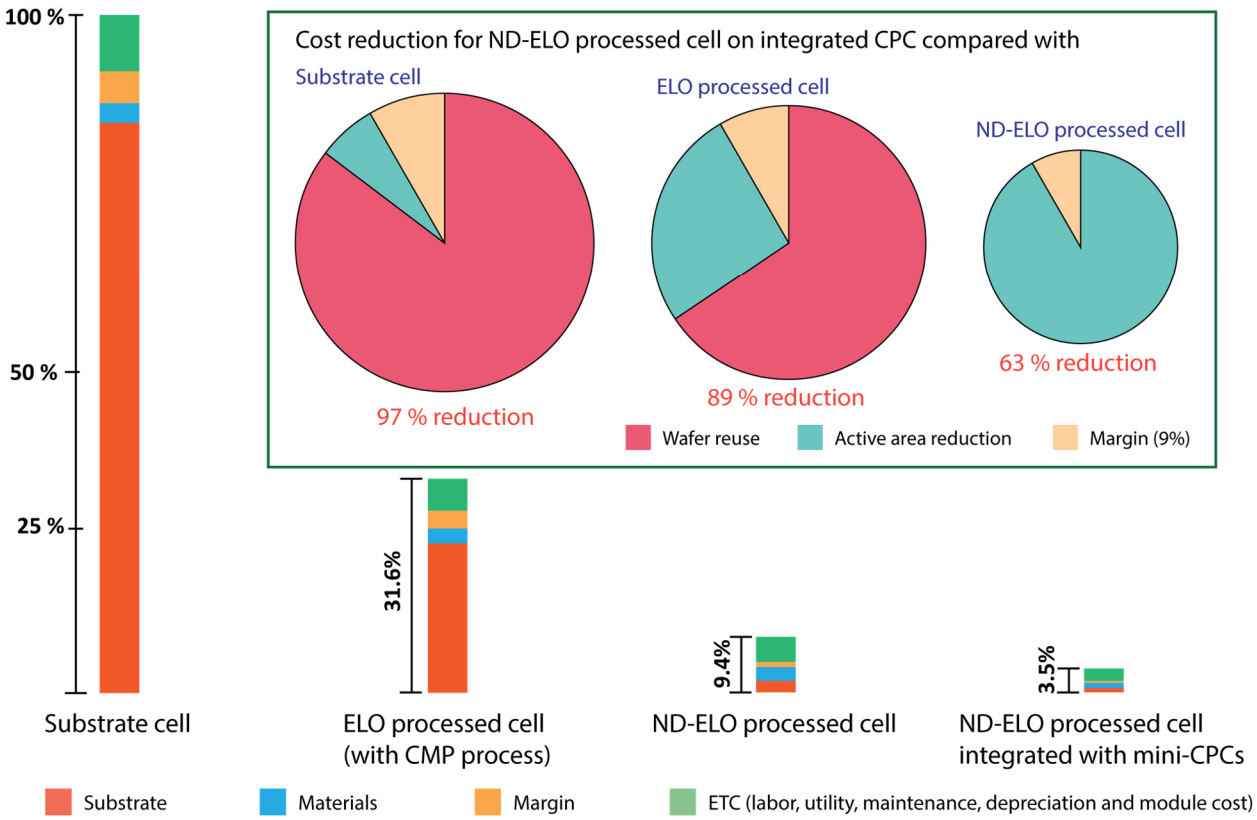


Fig. 7.16: Comparison of production cost using thin-film GaAs solar cells integrated with CPCs. Comparison of solar cell production cost for the substrate based, ELO processed and ND-ELO processed thin-film GaAs solar cell modules with and without the 6° tilted CPC. The percentages show the relative costs compared to a conventional non-lifted-off (substrate) cell lacking concentration. Inset shows the cost reduction for the major processes used in fabrication of ND-ELO processed thin-film GaAs solar cells integrated with CPCs, compared with a non-concentrated substrate based cell and a conventional ELO processed cell.

This analysis indicates an approximately 97% cost reduction using the ND-ELO thin-film GaAs solar cell integrated with a 6° tilted CPC compared with substrate-based cells, and a 89% reduction compared with conventional ELO-processed thin film solar cells. Here, 66% of the reduction is due to improved epitaxial-substrate utilization using ND-ELO, and 25% from the area reduction of 2.8× afforded by the mini-CPCs. The cost for CPC fabrication is estimated at < 1%

of the total module production cost. Table 7.1 shows the detailed costs used in comparing each technology approach.

Table 7.1 Production cost estimation. Cost estimation for substrate based, conventional ELO processed, and ND-ELO processed thin-film GaAs solar cells, and module employing integrated plastic mini-CPCs.

	Substrate cell	**ELO processed cell**	**ND-ELO processed cell**	**ND-ELO processed cell integrated with mini-CPCs**
wafer	\$47.1/W_p	\$12.37/ W_p†	\$0.94/ W_p	\$0.34/ W_p
Material	\$1.62/ W_p	\$1.25/ W_p	\$1.25/ W_p	\$0.45/ W_p
Depreciation	\$1.8/ W_p	\$1.8/ W_p	\$1.8/ W_p	\$0.64/ W_p
Module cost	\$0.1/ W_p	\$0.1/ W_p	\$0.1/ W_p	\$0.11/ W_p
Margin*	\$4.62/ W_p	\$1.46/ W_p	\$0.43/ W_p	\$0.16/ W_p
Etc (laber, utility, maintenance)	\$0.73/ W_p	\$0.73/ W_p	\$0.73/ W_p	\$0.26/ W_p
Total	\$55.97/ W_p	\$17.71/ W_p	\$5.25/ W_p	\$1.96/ W_p

* 9% fixed margin is assumed

† Fixed CMP cost of \$8/repolish with a 70 % process yield is assumed.

Ultimately, to estimate the long term cell production cost, we assume the reference case cost base of \$13.6 /W_p by assuming 20× substrate reuse, utilization of 30% for the III-source and 20 % for the V source precursors, 15 μm/hr GaAs growth rate, 70% CMP process yield and 25 % cell power conversion efficiency. 49 % of this cost originates from the CMP process and the cost of parent epi-substrate. Therefore, a dramatic cost reduction to \$4.6/W_p can be achieved simply by eliminating the CMP process via ND-ELO, and increasing the number of wafer reuses combined

with lower weighted average cost of capital (WACC, 9% to 7%) and improved *PCE* (27%). As shown in figure 7.17(a), this cost can be further reduced to \$0.5 /W_p by improving cell processing (enhanced material utilization, deposition rate and yield etc.), and developing manufacturing processes that lead to reduced material, labor, and depreciation expenses.

The \$0.6 /W_p module cost is estimated based on the production cost of 2.26 m^2 crystalline Si module. For our calculation, the thin-film GaAs solar cell efficiency of 29% is adjusted to 24%, which is the current record module efficiency for the equivalent cell[1]. Therefore, an additional cost of \$0.12 /W_p is incurred. The CPC fabrication cost is estimated at ~\$0.01/Wp based on the material cost (\$1.05 /m^2 for PETG and \$2.08 /m^2 for 300 nm thick Ag; therefore, ~\$0.003/Wp for PETG and ~\$0.007/Wp for Ag) which is comparable to a commercially available Ag-coated Mylar substrate with ~95% reflectance (DuPont Teijin Film). By applying an active GaAs solar cell area reduction using CPCs, the total cost for the completed module is reduced to \$0.34/Wp (Figure 7.17(b)), representing a potential cost reduction of 99.4%. Furthermore, the lightweight module impacts the balance of system cost by minimizing expenses incurred on installation and racking, thus making it adaptable for rooftop installations which may not be capable of supporting heavy, unwieldy modules and bulky, active solar tracking concentrator systems.

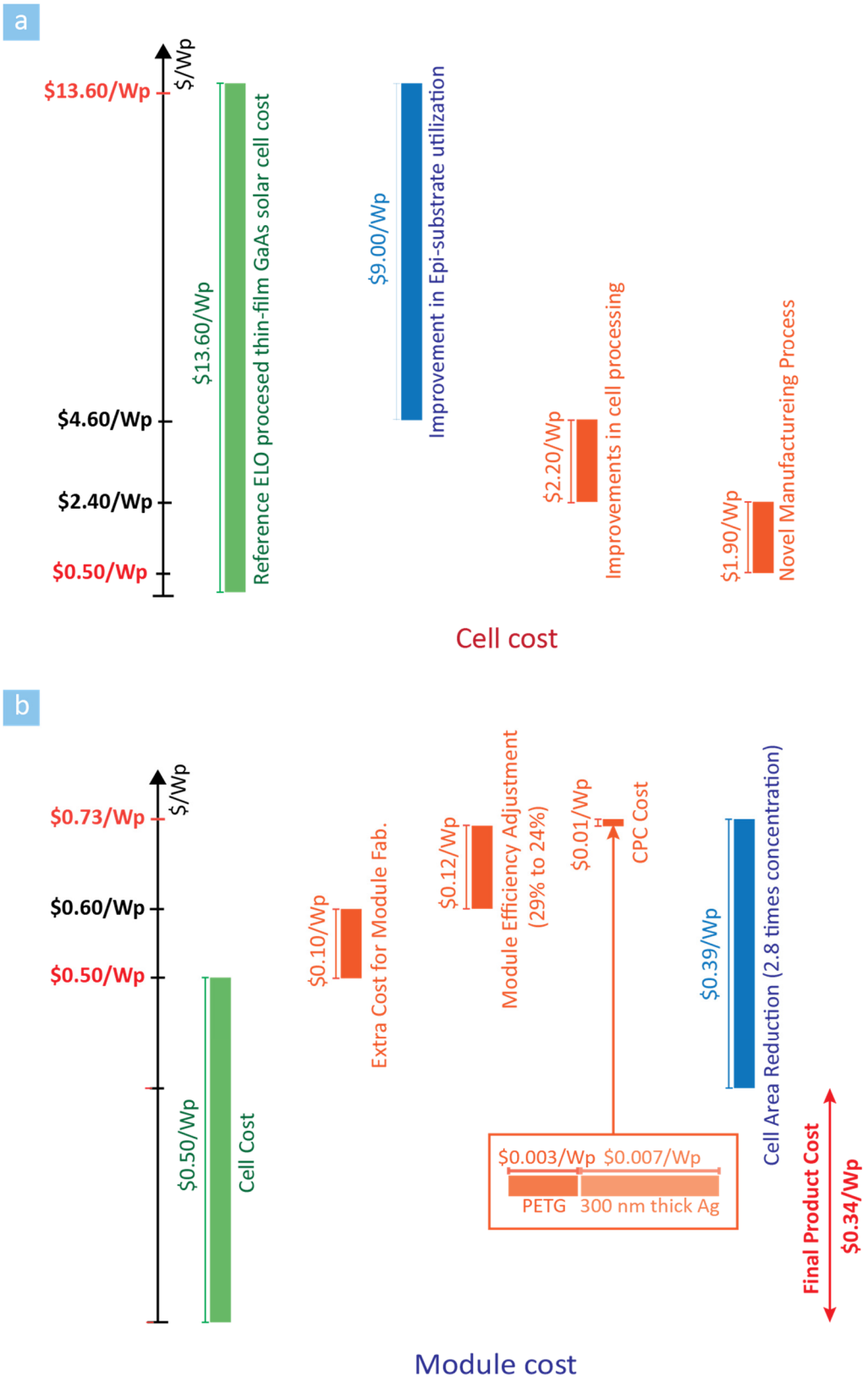


Fig. 7.17 Production cost estimation (a) Cost estimation for thin-film GaAs solar cells and (b) modules where the cells are integrated with plastic mini-CPCs.

7.3 Conclusion

In summary, we demonstrated thin-film GaAs solar cells integrated with low-cost, thermoformed, lightweight and wide acceptance angle mini-CPCs. The fabrication combines rapid ND-ELO thin film cells that are cold-welded to a foil substrate, and are subsequently attached to the CPCs in an adhesive-free transfer printing process. The combination of low-temperature operation of the thin-film solar cells along with the highly truncated low-profile plastic CPCs provides 2.8× enhanced energy harvesting throughout the year without the need for active solar tracking, while eliminating losses incurred at high operating temperatures characteristically encountered in concentration systems. Additionally, the combination of potentially low-cost fabrication and lightweight materials enables significant reductions in the balance of systems costs. This demonstration represents a significant step towards removing the cost barriers to the widespread deployment of lightweight and high performance thin-film GaAs solar cells in terrestrial and commercial solar electricity generation applications.

CHAPTER VII

Bibliography

1. Green, M. A., Emery, K., Hishikawa, Y., Warta, W. & Dunlop, E. D. Solar cell efficiency tables (version 44). *Prog. Photovoltaics Res. Appl.* **22,** 701–710 (2014).

2. Kayes, B. M. *et al.* 27.6% Conversion efficiency, a new record for single-junction solar cells under 1 sun illumination. in *2011 37th IEEE Photovolt. Spec. Conf.* 000004–000008 (IEEE, 2011). doi:10.1109/PVSC.2011.6185831

3. Miller, O. D., Yablonovitch, E. & Kurtz, S. R. Strong Internal and External Luminescence as Solar Cells Approach the Shockley–Queisser Limit. *IEEE J. Photovoltaics* **2,** 303–311 (2012).

4. Steiner, M. A. *et al.* Optical enhancement of the open-circuit voltage in high quality GaAs solar cells. *J. Appl. Phys.* **113,** 123109 (2013).

5. Shockley, W. & Queisser, H. J. Detailed Balance Limit of Efficiency of p-n Junction Solar Cells. *J. Appl. Phys.* **32,** 510 (1961).

6. Lee, K., Zimmerman, J. D., Hughes, T. W. & Forrest, S. R. Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics. *Adv. Funct. Mater.* **24,** 4284–4291 (2014).

7. Lee, K., Zimmerman, J. D., Xiao, X., Sun, K. & Forrest, S. R. Reuse of GaAs substrates for epitaxial lift-off by employing protection layers. *J. Appl. Phys.* **111,** 033527 (2012).

8. Cheng, C.-W. *et al.* Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics. *Nat. Commun.* **4,** 1577 (2013).

9. Bauhuis, G. J. *et al.* Wafer reuse for repeated growth of III-V solar cells. *Prog. Photovoltaics Res. Appl.* **18,** 155–159 (2010).

10. Yoon, J. *et al.* GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies. *Nature* **465,** 329–333 (2010).

11. Kurtz, S. R. Opportunities and challenges for development of a mature concentrating photovoltaic power industry. *NREL/TP-5200-43208* (2012).

12. Rabl, A. Comparison of solar concentrators. *Sol. Energy* **18,** 93–111 (1976).

13. Ferguson, G. S., Chaudhury, M. K., Sigal, G. B. & Whitesides, G. M. Contact adhesion of thin gold films on elastomeric supports: cold welding under ambient conditions. *Science* **253,** 776–778 (1991).

14. Kim, C., Burrows, P. & Forrest, S. Micropatterning of organic electronic devices by cold-welding. *Science* **288,** 831–3 (2000).

15. Lee, K., Shiu, K.-T., Zimmerman, J. D., Renshaw, C. K. & Forrest, S. R. Multiple growths of epitaxial lift-off solar cells from a single InP substrate. *Appl. Phys. Lett.* **97,** 101107 (2010).

16. Xu, X., Davanco, M., Qi, X. & Forrest, S. R. Direct transfer patterning on three dimensionally deformed surfaces at micrometer resolutions and its application to hemispherical focal plane detector arrays. *Org. Electron.* **9,** 1122–1127 (2008).

17. Rabl, A. Optical and thermal properties of compound parabolic concentrators. *Sol. Energy* **18,** 497–511 (1976).

18. Kalogirou, S. A. Solar thermal collectors and applications. *Prog. Energy Combust. Sci.* **30,** 231–295 (2004).

19. Fan, J. C. C. Theoretical temperature dependence of solar cell parameters. *Sol. Cells* **17,** 309–315 (1986).

20. Goodrich, A. *et al.* A wafer-based monocrystalline silicon photovoltaics road map: Utilizing known technology improvement opportunities for further reductions in manufacturing costs. *Sol. Energy Mater. Sol. Cells* **114,** 110–135 (2013).

21. Woodhouse, M. & Goodrich, A. a manufacturing cost analysis relevant to single and dual junction photovoltaic cells fabricated with III-Vs and III-Vs grown on Czochralski Silicon. *NREL Rep. No. PR-6A20-60126* 92 (2014).

Chapter VIII

Application of thin-film GaAs photovoltaic cells

In this chapter, we introduce the various applications of thin-film GaAs photovoltaic cells by taking advantage of their unique features of flexibility and light weight. First, we demonstrate the integration of a GaAs thin-film solar cell array with an ultra-high frequency (UHF) antenna and an RF choke on a flexible substrate using the epitaxial lift-off (ELO) process. In this setup, the thin-film solar cells, their contact metallization, and metallic interconnections function as both power source and radiation element. A resonant frequency at ~350 MHz is simulated and this value is confirmed with the voltage standing wave ratio (VSWR) measurement of the solar cell array. Furthermore, the multifunctional thin-film GaAs solar cell array works as both the power supply and communication antenna for an unmanned aerial vehicle (UAV) platform. Second, we introduce a new paradigm for solar tracking and concentration system based on thin-film GaAs solar cells using origami and kirigami processes. These flexible and lightweight thin-film solar tracking and concentrating systems enable the replacement of traditional bulky optical systems with cost-efficient and simple structures by using a simple cutting and folding process. Therefore, the balance of system (BoS) cost of a thin-film GaAs solar module can be significantly reduced compared with conventional solar tracking/concentration systems.

8.1 Introduction

Recently, demand has been increasing for lightweight and flexible electronics, making thin-film III-V solar cells a relevant technology for satellites to personal and terrestrial applications.[1,2] By integrating III-V solar cells onto the lightweight plastic substrates, the ELO process enables high specific power conversion (W/g), which is essential for reducing device weight.[3,4,5,6] The overall system mass can be further enhanced by adding additional functionalities to the solar cell modules.

In this chapter, we demonstrate two kinds of possible applications using the unique feature of thin-film GaAs solar cells. First, we describe the fabrication of GaAs thin-film solar cell array on flexible plastic substrates integrated with ultra-high frequency (UHF) antenna and RF choke, and the performance is investigated. The integration of solar cells and an antenna is promising as both components are exposed to the surface of the device.[7,8] Second, we demonstrate single axis tracking/concentrating thin-film GaAs solar cells using a kirigami architecture. The kirigami design enables the addition of a solar tracking/concentrating function by applying a simple cut and fold geometry to the thin-film platform. A lightweight and low-profile solar tracking and concentrating optical system can potentially reduce the balance of system cost of a solar module compared to conventional solar tracking systems.

8.2 Experiment and results

8.2.1 ELO processed solar cell array integrated with a flexible antenna

The epitaxial layer structures were grown by gas-source molecular beam epitaxy (GSMBE) on Zn-doped (100) *p*-GaAs substrates. The growth starts with a 0.2 μm-thick GaAs buffer layer

followed by the 0.1 μm-thick $Al_{0.25}Ga_{0.26}In_{0.49}P$/ 0.1 μm-thick GaAs/ 0.05 μm-thick $Al_{0.25}Ga_{0.26}In_{0.49}P$ protection layers. Then, a 0.025 μm-thick AlAs sacrificial layer is grown. A *p*-on-*n* GaAs solar cell active region is grown as follows: 0.1 μm-thick, 5×10^{18} cm^{-3} Be-doped GaAs contact layer, 0.025 μm-thick, 2×10^{18} cm^{-3} Be-doped $Al_{0.25}Ga_{0.26}In_{0.49}P$ window layer, 0.15 μm-thick, 1×10^{18} cm^{-3} Be-doped *p*-GaAs emitter layer, 3.5 μm-thick, 2×10^{17} cm^{-3} Si-doped *n*-GaAs base layer, 0.05 μm-thick, 4×10^{17} cm^{-3} Si-doped $In_{0.49}Ga_{0.51}P$ back surface field (BSF) layer, and a 0.1 μm-thick, 5×10^{18} cm^{-3} Si-doped *n*-GaAs contact layer.

After growth using GSMBE, a 5 nm-thick Ir layer is sputtered onto a 50 μm-thick Kapton® sheet as an adhesion layer. Ir is also utilized as a stressor layer to accelerate the ELO process. Then, 500 nm-thick -thick Au contact layer is deposited onto both the Ir coated Kapton® sheet and GaAs epitaxial layer by e-beam evaporation. The substrate and plastic sheet are bonded via cold-welding by applying 25 kN force application using an MTS alliance RT/100 stamping machine and then submerged into a heated solution of 20% HF for epitaxial lift-off. Immediately after the ELO process, the thin film and parent substrate are cleaned by plasma etching with BCl_3 and Ar gases. Then, the thin film is fabricated into a solar cell. The $Al_{0.25}Ga_{0.26}In_{0.49}P$ and GaAs protection layers are sequentially etched with $HCl:H_2O$ (1:1) and $H_3PO_4:H_2O_2:H_2O$ (3:1:25).

The lifted-off thin film is fabricated into solar cells starting with the front contact grid patterning using photolithography and deposition of Pd(5 nm)/ Zn(15 nm)/ Pd(15 nm)/ Au(800 nm) by e-beam evaporation. The device is annealed for 30 min at 180 °C to form Ohmic contacts. Mesas are defined using photolithography and wet etching, and the highly-doped GaAs Ohmic contact layer is removed between gridlines. Finally, a TiO_2 (52 nm)/ MgF_2(85 nm) bi-layer antireflective coating (ARC) is deposited by e-beam evaporation. The inset of Fig. 8.1 shows a fabricated GaAs thin-film solar cells from an ELO processed 2" GaAs wafer.

The fourth quadrant current density-voltage (*J-V*) characteristics of the ELO processed GaAs solar cell was measured under simulated Atmospheric Mass 1.5 Global (AM 1.5G) illumination at 100 mW/cm^2 intensity and is presented in Fig. 8.1. The optical power intensity was calibrated using a National Renewable Energy Laboratory traceable Si reference photovoltaic cell. The short circuit current density is 26 mA/cm^2 and the open circuit voltage is 0.99 V, the fill factor is 76.1 %, resulting in a power conversion efficiency of 19.8 %.

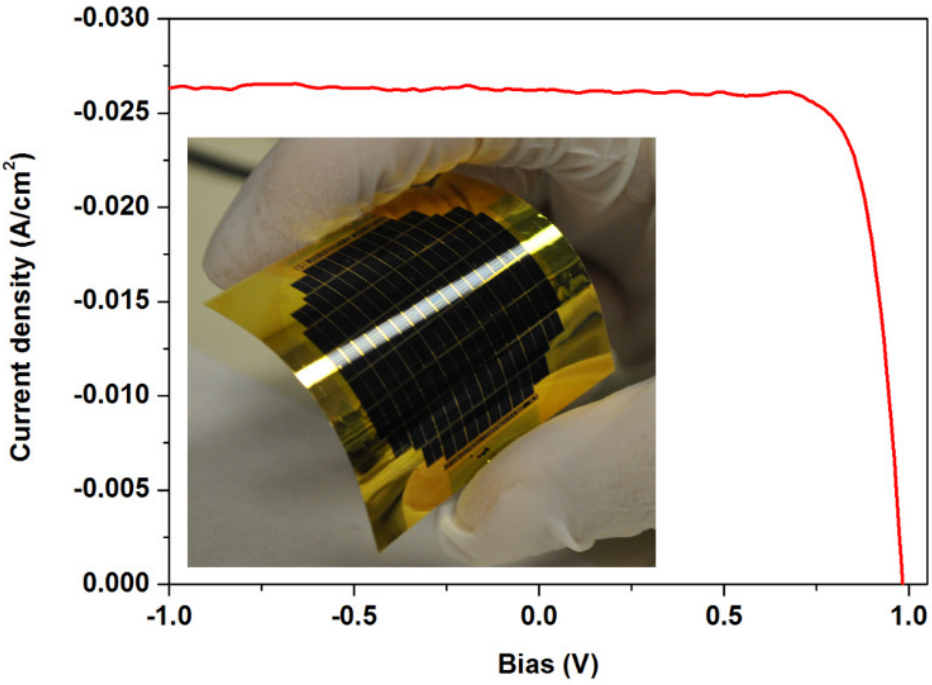


Fig. 8.1: The current density-voltage characteristics and (inset) image of flexible GaAs thin-film solar cells on a 50 μm-thick Kapton® sheet

For the solar cell array to function as an antenna, additional fabrication steps are required between mesa definition and ARC deposition. After mesa definition, Au is patterned using photolithography and wet-etching (TFA etchant, Transene CO), followed by an Ir inductive

coupled plasma etch using Cl_2 gas at 4 mTorr to pattern the rear-side of the metal array connection. To form a series connection of the solar cells, the sides of each solar cell are passivated using a 400 nm SiNx layer deposited by plasma enhanced chemical vapor deposition and patterned by photolithography and plasma etching. After a ZnS(43 nm)/MgF_2(102 nm) antireflective coating is deposited by e-beam evaporation, solar cells are connected using a 500 nm-thick Au layer sputtered through a shadow-mask.

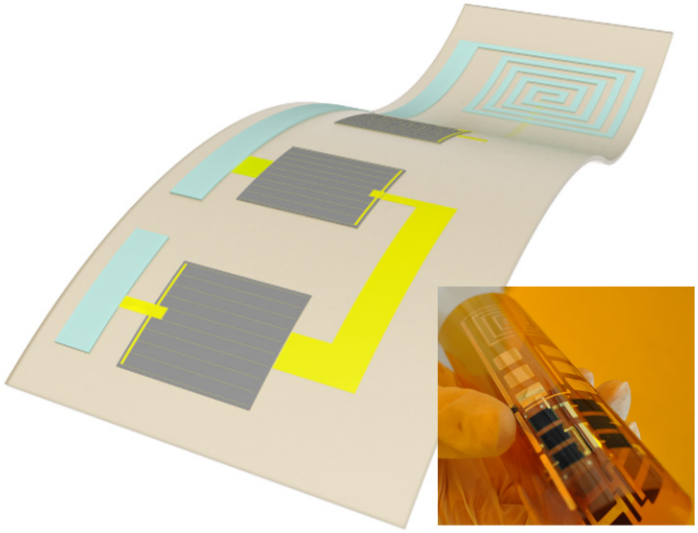


Fig. 8.2: The schematic of multifunctional solar cell array in series a spiral RF choke and (inset) image of fabricated GaAs thin-film solar cell array on a 50 μm-thick Kapton® sheet

After solar cell fabrication, a 15 μm-thick Al layer is deposited via e-beam evaporation through a shadow mask to enhance the antenna and RF choke. Then, the DC output metal connection is evaporated onto the reverse side of the Kapton® sheet and connected to both the center of the RF choke and the contact pad on the front side. Figure 8.2 shows the schematic of a solar cell array and interconnections integrated with antenna and the RF choke.

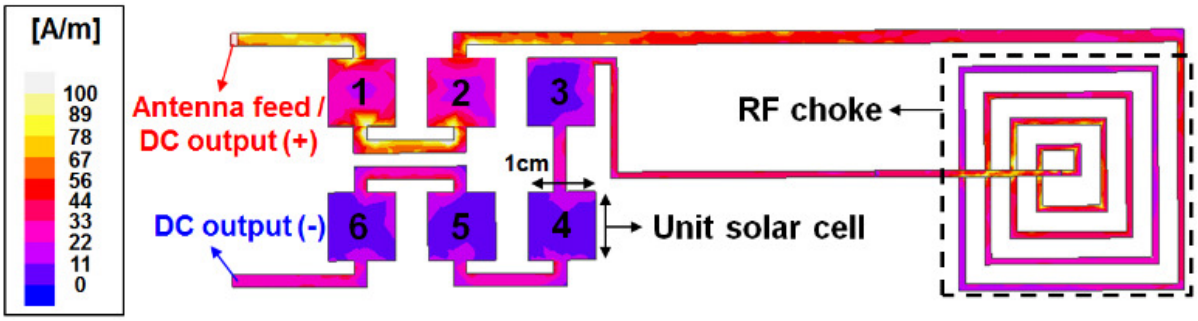


Fig. 8.3: Thin-film solar cells working as part of a UHF antenna, their current distribution at 350 MHz and the whole antenna topology integrated with a RF choke.

The fabricated thin-film solar cells have a large junction capacitance at microwave frequencies, and thus can be used as a part of or an entire efficient antenna. Figure 8.3 shows the topology and current distribution in a meander monopole UHF antenna employing thin-film solar cells as a part of the radiating elements. Except for the solar cells where the metal is part of the back contact (denoted by number 1~6), all of the traces are exposed metal. A RF current path excited by the antenna feed on the top left-hand corner in Fig. 8.3 is effectively disconnected by a RF choke. Therefore, while solar cells 1 and 2 operate as a transmission line of RF current as well as a DC power generator, solar cells 3, 4, 5 and 6 only operate as a DC power generator. This is shown in Fig. 8.3 where the RF current density on solar cells 1 and 2 is much higher than on solar cells 3, 4, 5 and 6.

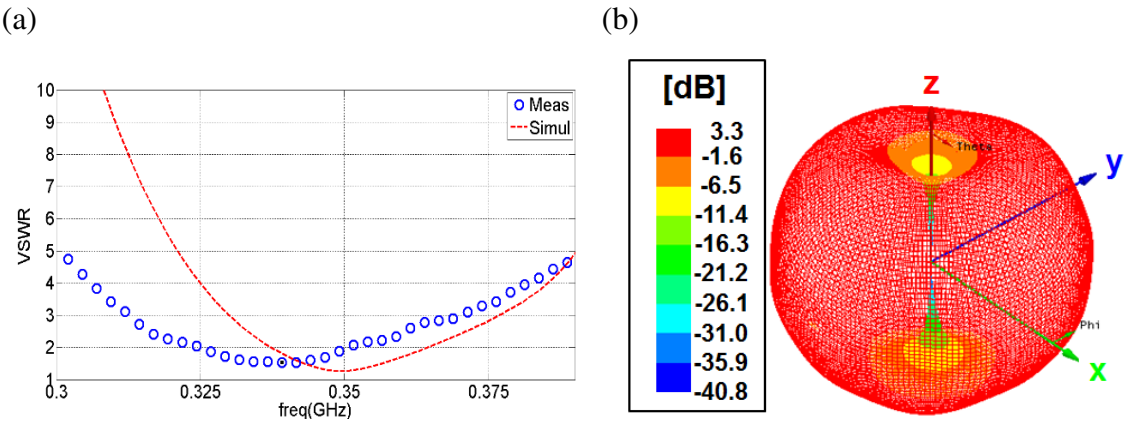


Fig 8.4: (a) Measured and simulated VSWR and (b) 3D radiation pattern (G_θ) of the solar antenna.

Figure 8.4(a) and (b) show the measured and simulated voltage standing wave ratio (VSWR) and 3D radiation pattern (G_θ) of a solar antenna integrated with a RF choke. The measured VSWR shows good agreement with the simulated VSWR and the value of antenna gain acquired by 3D radiation pattern validates high radiation efficiency of the integrated solar cells and antenna. Finally, the ELO processed solar cell array with patterned interconnection is mounted on the wing of an UAV platform, and the versatility of power supply and communication properties is confirmed.[8]

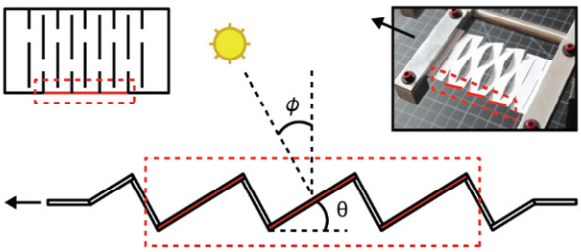
8.2.2 Thin-film photovoltaic cells integrated with Orgami & Kirigami based optical systems

To fabricate the thin-film GaAs solar cells on plastic substrate, epitaxial layers of *p-n* junction GaAs active material on an AlAs sacrificial layer were grown by gas-source molecular beam epitaxy (GSMBE) on a 2 inch-diameter (100) GaAs substrate. The sample was then coated with a 300 nm thick Au layer by e-beam evaporation, and bonded to a 50 μm-thick E-type Kapton® sheet (also coated in 300 nm Au layer) using cold-weld bonding by applying a pressure of 4 MPa for 8 mins at a temperature of 230 ℃. After bonding, the photovoltaic epitaxial active region and

Kapton® carrier were isolated from the bulk wafer using epitaxial lift-off (ELO) by selectively removing the AlAs sacrificial layer in dilute (15%) hydrofluoric acid (HF) solution at room temperature.

After ELO, a Pd(5 nm)/ Zn(20 nm)/ Au(700 nm) front metal contact was patterned using photolithography. Then, the device mesas were similarly defined using photolithography and subsequent chemical etching using H_3PO_4:H_2O_2:deionized H_2O (3:1:25). The exposed, highly-doped 150 nm thick *p*+ GaAs contact layer was selectively removed using plasma etching. After annealing the sample for 1 hr at 200 °C to facilitate ohmic contact formation, the sidewalls were passivated with a 1 μm-thick polyimide applied by spin coating. After curing the sample at 300 °C for 30 min, the polyimide was selectively removed by photolothograpy and plasma etching. The external contact pad was patterned with Ti (10 nm)/Au (500 nm). Finally, a bilayer anti-reflection coating consisting of TiO_2 (49 nm) and MgF_2 (81 nm) was deposited by e-beam evaporation. Then, to test the feasibility of the kirigami process as a single axis solar tracker, various cut geometry is formed on the Kapton® sheet. Figure 8.5(a) shows the schematic illustration of a solar tracking mechanism using a kirigami-based thin-film solar tracking structure. The Kapton® sheet is cut into various different dimensions to test the tracking performance: For $R_1 = R_2 = 3$, $L_C = 15$ mm, $L_U = 5$ mm, and $W_C = 5$ mm. For $R_1 = R_2 = 5$, $L_C = 15$ mm, $L_U = 3$ mm, and $W_C = 3$ mm (Fig 8.5 (b)).

(a)



(b)

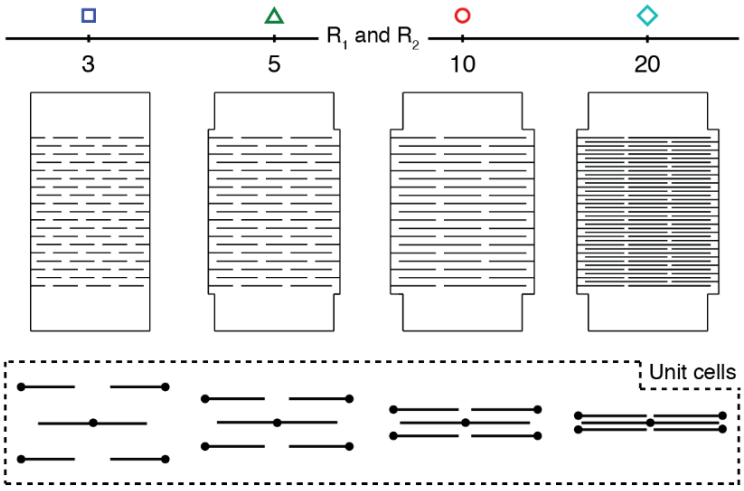


Fig. 8.5: (a) A kirigami tracking structure that, upon stretching, simultaneously changes the angle of the elements comprising the sheet. By incorporating thin film solar cells into this structure, it may be used as a low-profile alternative to conventional single-axis solar tracking mechanisms. (b) Schematics of four kirigami structures, where $R_1 = R_2 = 3$, 5, 10, and 20, along with their corresponding units cells. Figure courtesy of Aaron Lamoureux

Figure 8.6(a) shows photographs of thin-film GaAs photovoltaic cells comprised of kirigami cut geometry, where $R_1 = R_2 = 3$. The appropriate force is applied to strain each cell to track the simulated solar radiation. Then, the photovoltaic cells are measured by using light incident angle resolved measurement under the simulated AM1.5G light source (Oriel solar simulator, model 91191 with Xenon arc lamp and AM 1.5 global filter) calibrated by using Si

photodiode certified by NREL. The *J-V* characteristics were measured at each angle using a semiconductor parameter analyzer (SPA, Agilent 4155B), in increments of five degrees, from normal incidence ($\phi = 0°$) to $\phi = 90°$. The short circuit current density, J_{SC}, was determined at each angle, and subsequently normalized to J_{SC} at $\phi = 0°$. Figure 8.6(b) shows the normalized short circuit current density as a function of light incident angles for two different samples with cut geometry of $R_1 = R_2 = 3$ and $R_1 = R_2 = 5$ (closed symbols) with the simulated values for various of $R_1 = R_2$ (open symbols, solid lines). The larger R_1 and R_2 result in an enhanced solar tracking performance as expected due to the suppression of transverse strain at equivalent axial strain. The inset of Fig. 8.6(b) shows a schematic of measurement set-up.

Furthermore, the reliability test of a kirigami-processed system performed by repeating the straining/un-straining process over 350 cycles shows no systematic performance degradations before and after the test. Finally, the daily energy harvesting of thin-film GaAs solar cells with and without a kirigami-based tracking system are compared in Fig. 8.6(c). The zenith and air mass of the solar radiation is assumed to be at the equator during Equinox for the energy harvesting simulations for simplified comparison. As expected, the kirigami structures with larger R_1 and R_2 provide more close tracking performance to the conventional perfect single-axis tracking systems. The inset of Fig. 8.6(c) shows values for the integration of each curve in Fig. 8.6(c). The enhanced output energy density from thin-film GaAs solar cells (~1.78 times) indicates the effectiveness of the kirigami-based solar tracking systems.

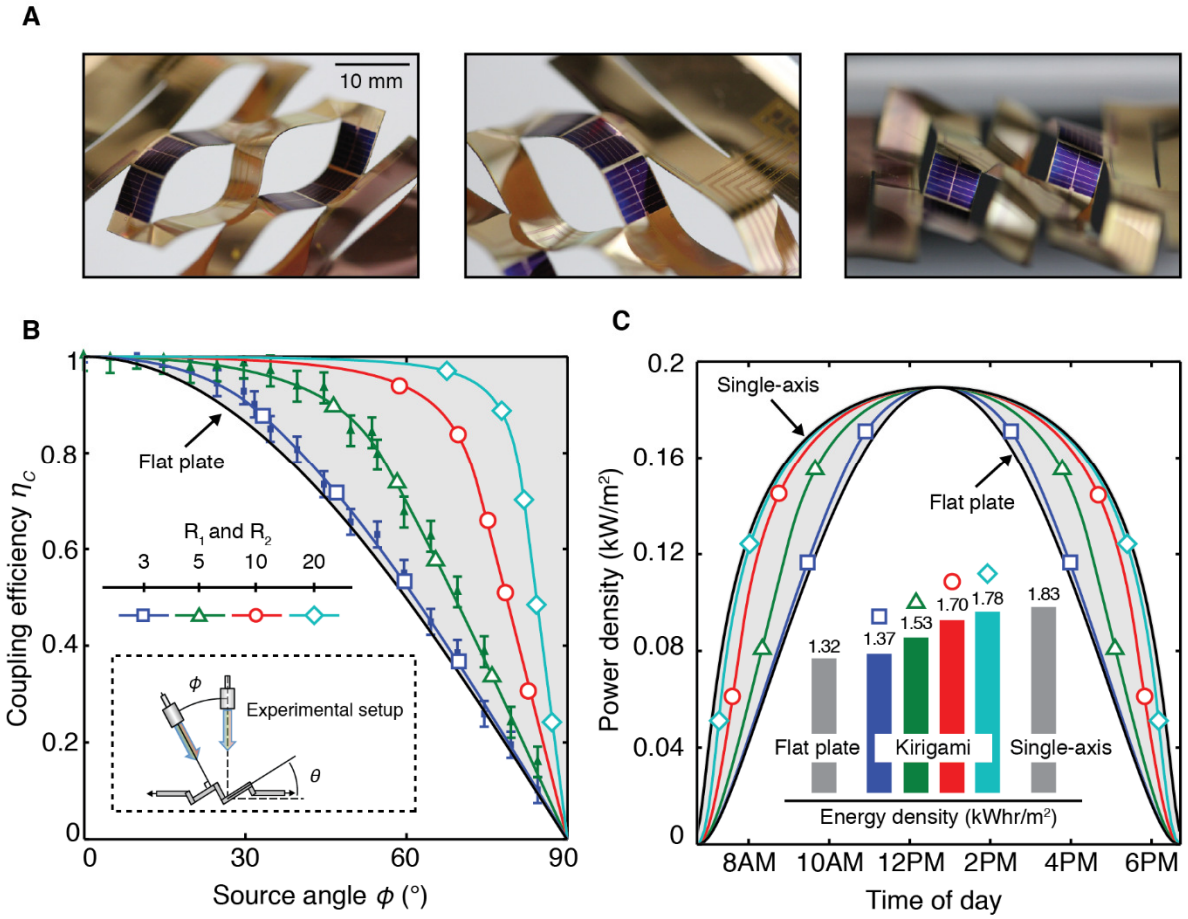


Fig. 8.6: (a) Photographs of integrated kirigami solar cells, comprised of linear cut epitaxial lift-off GaAs solar cells, mounted by cold weld bonding on the plastic carrier substrate. Here, L_C = 15 mm, L_U = 5 mm, and W_C = 5 mm (R_1 = R_2 = 3). (b) Normalized solar cell short circuit current density $J_{SC}(\phi)$ / $J_{SC}(\phi=0)$ for two samples, where R_1 = R_2 = 3 and R_1 = R_2 = 5 (closed symbols). Also shown are the simulated data for coupling efficiency, η_C, (solid lines, open symbols). The agreement between experimental and simulated results suggests that η_C is a direct measure of optical coupling, and that performance may be optimized by increasing R_1 and R_2. (c) Output electrical power density (per unit area of semiconductor) *vs.* time of day for several kirigami cut structures, stationary panel, and single-axis tracking systems. Integration of the curves yields the energy density per unit area of semiconductor, where kirigami-enabled tracking systems are capable of near single-axis performance (inset). Figure courtesy of Aaron Lamoureux

We also demonstrate the solar tracking/concentrating integrated system based on an origami process. Figure 8.7(a) and (b) shows a schematic illustration of the origami process to form parabolic solar concentrators and trackers. Polyethylene terephthalate (PET) is employed as a concentrator and tracker platform for the origami process. The planar figure of hexagonal parabolic concentrators are designed using Solidworks software, first. Then, the 125 μm thick PET substrate is cut and folded along the guidelines on it. The length of each bottom hexagonal side is 2 mm, and the opening area of concentrator is 9 times larger than the solar cell area. To form the reflector on top of the concentrator, a ~100 nm thick silver coating is applied using e-beam evaporation which is thick enough to limit the transmission through the thin-film metal layer to approximately 0.05 %. Figure 8.7(c) shows a schematic illustration of the solar tracking operation using concentrator/tracker assemblies. Flexible arch bridges which support the solar cells enable the rotation of solar cell/concentrator assembles to track the solar radiation by pushing the structure with a laterally moving stage. Figure 8.7(d) shows an image of an origami-processed concentrator/tracker assembles array.

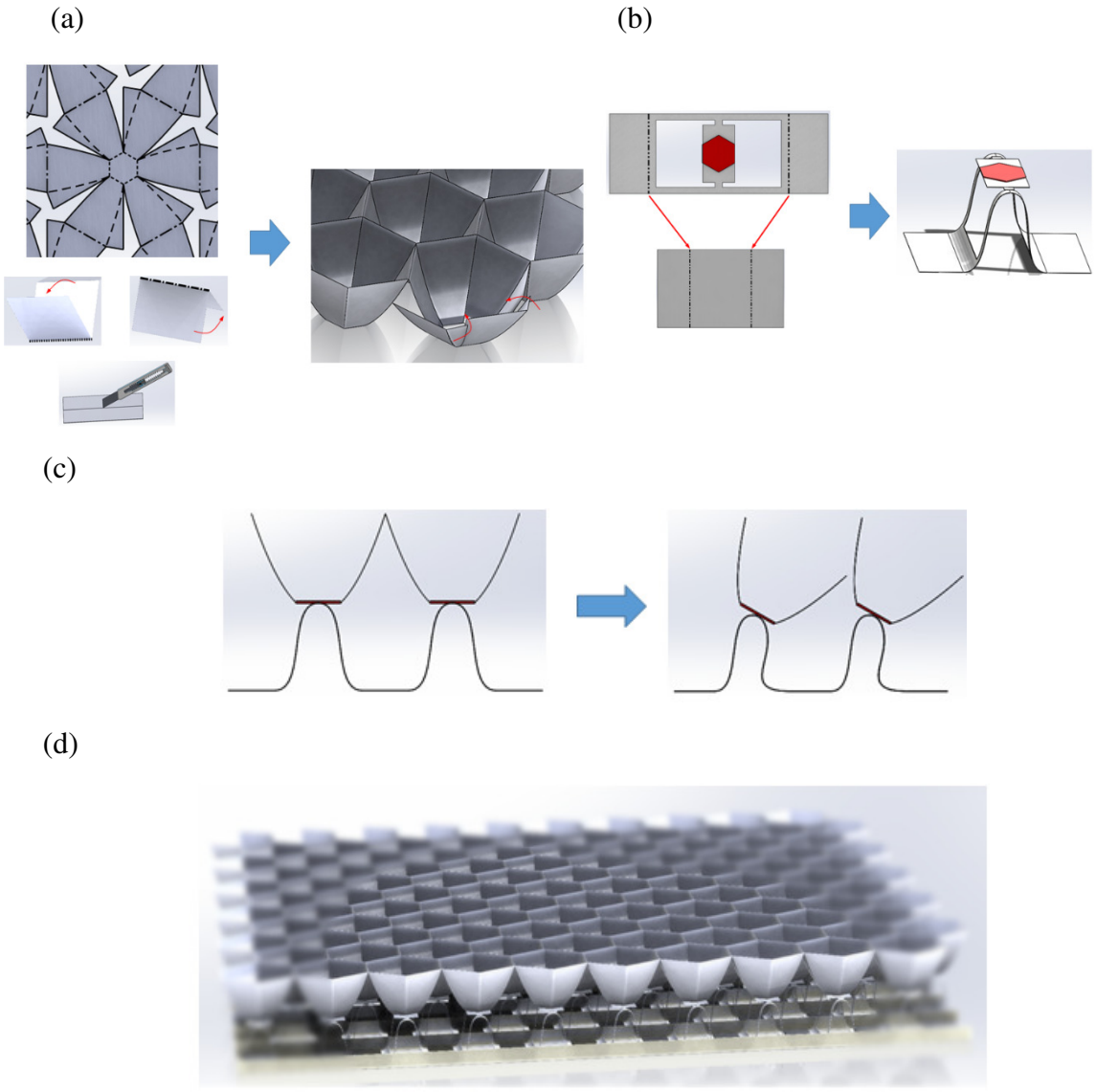


Fig. 8.7: Origami integrated PV system (a) Schematic illustration of origami process for concentrator fabrication: The dashed lines indicate the folding guide lines. (b) Schematic illustration of origami process for origami solar trackers: The patterned PET substrate is squeezed up and shaped into an arc structure. The red area shows the position of the solar cell. (c) The cross-section view of the origami PV system with and without the rotation of collectors. The bottom origami structure is the principal part to perform tracking of the concentrators. The net force applied on the bottom origami structure determines the rotation angle of the solar collectors. The figure shows that the net force on the bottom origami structure is toward the left and, thus, the solar concentrator is tilted toward right. (d) The schematic diagram of the origami integrated PV system. Figure courtesy of Chih-Wei Chien.

Figure 8.8(a) shows the current-voltage characteristics of a GaAs solar cell with and without the origami concentrator under normal angle illumination. The GaAs solar cell without concentrator shows a short-circuit current density (J_{sc}) of 23.07 mA/cm^2, open circuit voltage (V_{oc}) of 0.91 V, and fill factor of 73.3% under the simulated AM 15.G illumination at 1 sun intensity. The identical solar cells integrated with an origami-processed parabolic concentrator shows a 6.09 times higher J_{sc} compared with the reference case without concentrator. As a result, the power generation from the GaAs solar cells shows 6.14 times improvement compared with the same cell without concentrators due to increased J_{sc} as well as V_{oc}.

Figure 8.8(b) shows a characteristic of an GaAs solar cell with and without origami tracker/concentrators assemblies under various light incident angles. As expected, GaAs solar cells with an origami-processed single-axis solar tracking system provides enhanced energy harvesting under the off-angle light illumination. The effect of an origami tracking system is significant when combined with a concentration system. Parabolic concentrators generally provide very narrow acceptance angles. Therefore, the off-angle performance of a solar cell with a parabolic concentrator is relatively poor compared with the normal light incident angle case. However, the concentrator combined with a single-axis tracking system enabled by the origami process provides a significant improvement in terms of sensitivity to the light incident angle, which indicates a feasibility of the origami process for a solar concentrating/tracking system. Eventually, the integrated origami PV system provides potential to reduce the solar module production cost due to its low process cost.

(a) (b)

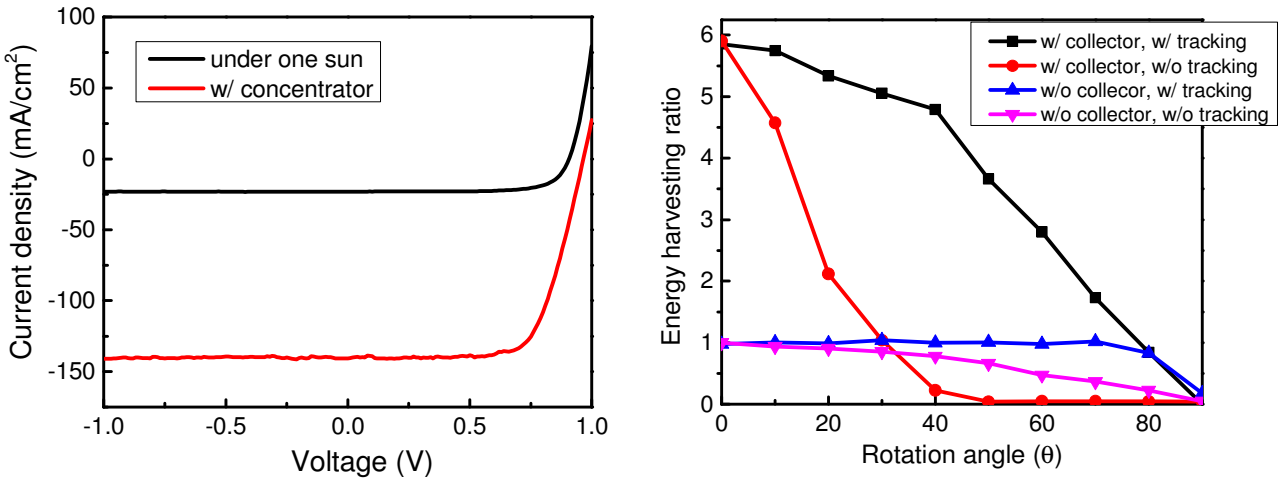


Fig. 8.8: Energy harvesting and GaAs solar cell characteristics. (a) *I-V* characteristics of GaAs solar cell with and without the Ag-coated origami collector. (b) Comparison of energy harvesting ratio with and without the trackers and collectors. Figure courtesy of Chih-Wei Chien.

8.3. Conclusion

In summary, we have demonstrated the fabrication of thin-film GaAs *p/n* junction solar cells on flexible plastic substrates with an efficiency of approximately 20% by combining ELO and cold welding. Moreover, patterned, ELO-processed GaAs thin-film solar cells and interconnections functioned as a UHF antenna and RF choke at the design frequency. The incorporation of ELO-processed GaAs solar cells with an UHF antenna presents an opportunity for a thin, flexible and lightweight power supply that also works as a radio communication antenna. Furthermore, we have demonstrated the solar tracking and concentrating structure via origami and kirigami processes to maximize energy harvesting of thin-film GaAs solar cells. The simple cut and folded geometry enables a low profile and lightweight solar tracking and concentrating system which leads to a significant cost reduction of balance of system. The combination of the previously

described non-destructive wafer recycling and versatility of ELO-processed GaAs thin-film solar cells provides the potential for cost effective, solar-to-electrical energy conversion with increased compactness of system by adding extra functionality.

CHAPTER VIII

Bibliography

1. Chin-Chin Tsai. Recent development in Flexible Electronics. 370–371 (2011).

2. Nathan, A. *et al.* Flexible Electronics: The Next Ubiquitous Platform. *Proc. IEEE* **100,** 1486–1517 (2012).

3. Konagai, M., Sugimoto, M. & Takahashi, K. High efficiency GaAs thin film solar cells by peeled film technology. *J. Cryst. Growth* **45,** 277–280 (1978).

4. Lee, K., Shiu, K.-T., Zimmerman, J. D., Renshaw, C. K. & Forrest, S. R. Multiple growths of epitaxial lift-off solar cells from a single InP substrate. *Appl. Phys. Lett.* **97,** 101107 (2010).

5. Lee, K., Zimmerman, J. D., Hughes, T. W. & Forrest, S. R. Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics. *Adv. Funct. Mater.* **24,** 4284–4291 (2014).

6. Kayes, B. M. *et al.* 27.6% Conversion efficiency, a new record for single-junction solar cells under 1 sun illumination. in *2011 37th IEEE Photovolt. Spec. Conf.* 000004–000008 (IEEE, 2011). doi:10.1109/PVSC.2011.6185831

7. Oh, J., Lee, K., Forrest, S. R. & Sarabandi, K. Conformal, structurally integrated antenna with a thin-film solar cell array for flapping-wing robots. in *2013 IEEE Antennas Propag. Soc. Int. Symp.* 1332–1333 (IEEE, 2013). doi:10.1109/APS.2013.6711326

8. Oh, J., Lee, K., Hughes, T., Forrest, S. & Sarabandi, K. Flexible Antenna Integrated With an Epitaxial Lift-Off Solar Cell Array for Flapping-Wing Robots. *IEEE Trans. Antennas Propag.* **62,** 4356–4361 (2014).

Chapter IX

Conclusions and Future Work

9.1 Conclusions

Thin-film optoelectronics attract considerable attention due to their unique features, such as light weight, flexibility and superior performance over substrate-based rigid and bulk devices. However, their deployment for commercial applications is still in its infancy due to immature fabrication process development and high production cost. In this thesis, we proposed universal and advanced fabrication methods to produce lightweight and flexible thin-film compound semiconductor optoelectronic devices including photovoltaic cells, photodetectors, LEDs, and MESFETs from both GaAs and InP substrates using non-destructive epitaxial lift-off (ND-ELO) process. Furthermore, substrate recycling for various optoelectronic devices using epitaxial protection layers is demonstrated without any systematic performance degradations. The multiple substrate recycling provides a potential for optoelectronic device production cost reduction by eliminating the cost of expensive wafers. The low cost and high performance thin-film based optoelectronics provide an opportunity to open a completely new domain of device applications by escaping from its planar and rigid geometry to a conformal one. In this chapter, we are proposing two promising applications by taking advantage of the unique features of thin-film photodiode and photovoltaic cells on a plastic substrate.

9.2 Conformal and multispectral photodetector array

Vision is one of the most crucial senses for humans when evaluating a scene. Current cameras use a flat focal plane arrays that require complex multi-element optics that flatten the Petzval field curvature of a simple lens. This adds weight and complexity, while limiting the field of view and f/number of the optics. By curving the focal plan array to match the field of curvature of a lens, analogous to the way a human eye is shaped, the imaging system can be made much lighter, smaller, and with minimal optical aberrations. In Chapters 5 and 6, we have demonstrated the fabrication and characterization of high performance thin-film photodiodes and field effect transistors. The thin-film based photodetector array on a conformal substrate has the potential to provide small, ultra-lightweight camera systems that have wide fields of view, function in very light-limited environments, and can operate across multiple spectral bands. For future work, we propose a multispectral hemispherical focal plane array (HFPA) imaging system with extremely low optical aberration, operating at wavelengths from the visible to the near infrared (i.e. 400 nm – 1700 nm) in both extremely low light levels and infrared rich environments.

Previously, Xu et al. demonstrated an organic photodetector array on a conformal substrate[1]; however, it lacked the passive or active pixel sensor transistor backplane and other features needed to realize a functioning, low-cost, high sensitivity, high dynamic range multispectral imaging system. The inorganic transistor backplane, along with extremely low dark current integrated inorganic and organic detectors ensures that the performance (dynamic range, field of view, f/number, light weight, video acquisition rates, spectral bandwidth) of the camera will surpass all known imaging systems available today. Multispectral HFPA imaging systems will enable visible and short wavelength infrared (SWIR) detection. The combination of organic and inorganic (InGaAs) detectors spans the wavelengths from λ=400 nm to λ=1650 nm, along with an InP-based

transistor active pixel sensor array to maximize sensitivity. High performance photodetectors and associated circuitry can be grown by molecular beam epitaxy and can be transferred to transparent hemispherical domes as in Fig. 9.1 using cold welding to metal pads pre-deposited on the substrates. Integrating organic detectors to extend the spectral bandwidth of the pixels is also not anticipated to lead to higher leakage or other performance degradation of the inorganic components since the deposition processes are completely non-destructive and occur near room temperature. Hence, leakage current introduced in heterogeneous integration schemes, where lattice mismatch and high temperature processing are common, are not a factor in this integration scheme.

(a) (b)

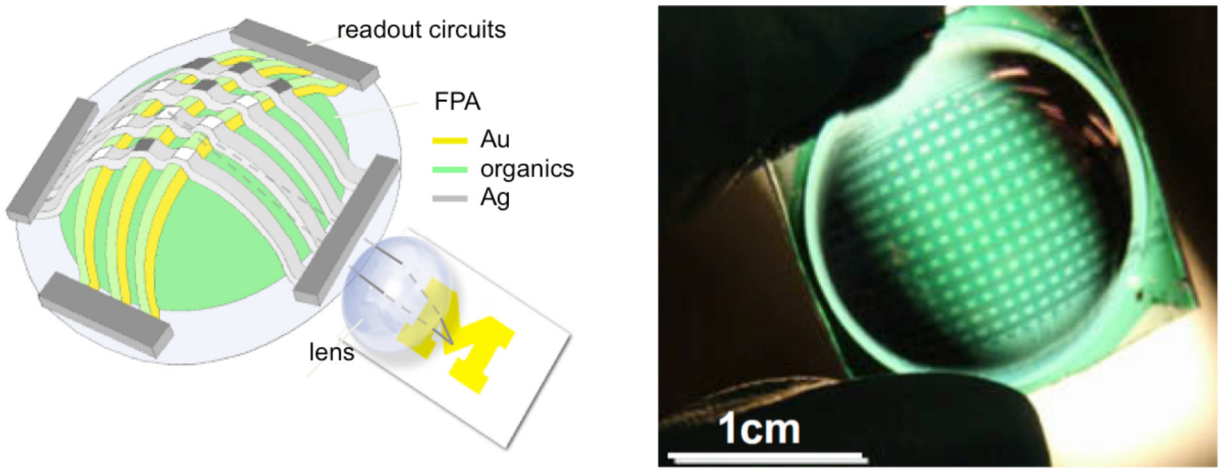


Fig. 9.1: The hemispherical focal plane array (HFPA) imaging systems (a) conceptual diagram of a HFPA. (b) an example 20x20 HFPA.

Mimicking the form factor of the human eye, imagers with spherical, or near-spherical focal planes greatly simplify the optics needed to create a high definition image. This approach, shown in Fig. 9.1, results in a low f/number (~1) for very low light level imaging, an exceptionally large field of view without need for optical correction, as well as lightweight, and inexpensive

optics. The achievement of such an imaging system remains a challenge. Demonstration of multispectral imaging systems that are capable of very low light level and thermal imaging, while being only 0.5-1 cm in radius and a few grams in weight, will allow for capturing thermal and other multispectral images.

Typical cameras have a field-of-view of $50^o \times 40^o$. The proposed camera with a hemispherical focal plane array will have a field-of-view of $140^o \times 140^o$ providing near complete vision in the direction forward of the FPA. As opposed to merely imaging, the backplane (retina) electronics could be designed to provide processing that would mimic retinal processing in the human eye. This would, among other advantages, enable noise suppression via averaging over receptive fields, optical flow sensing, light level adaptation that is variable across the retina, etc. A notable advantage of this curved imaging architecture is its rapid, high resolution, exceptional field-of-view, and night-vision data acquisition capability that make the platform highly capable for countless applications.

9.3 Thin-film GaAs solar cell technologies

9.3.1 50 times wafer recycling

Given the prohibitive cost of GaAs substrates, the parent wafers must be recycled at least 50X without the use of chemo-mechanical polishing (CMP) to make thin-film GaAs solar cells economically viable. In a recent NREL cost assessment of GaAs technology[2], the largest cost impact comes from wafer handling due to CMP. However, past demonstrations of ELO have all required CMP to remove defects following each growth iteration, introducing wafer damage and drastically limiting the number of cycles possible. By using the process of ND-ELO[3], a potentially

unlimited number of wafer reuses is possible, therefore transforming the wafer expense from a costly expendable material into a capital outlay.

However, continual regrowth on the same substrate can result in the accumulation of defects from previous growth cycles[4]. To achieve >50X wafer reuse, variants to the ND-ELO process are required to avoid this problem. Hence, the introduction of a superlattice (SL) within the protection or growth buffer layers provides a high quality regrowth interface on the parent wafer. Here, a 5 to 50 period $Al_{0.3}Ga_{0.7}As$/GaAs SL (each individual layer from 2 to 300 nm thick) followed by InGaP (Fig. 9.2) can be combined for wafer protection. Both the buffer and protection layers can be replaced by an $Al_{0.3}Ga_{0.7}As$/GaAs SL. The Al composition can be varied up to 100% for the upper protection layer and up to 40% for the growth buffer. This scheme will allow for the continual restoration of the original wafer surface after many repetitive ND-ELO cycles required since the process for removing SLs is identical to that used for removal of GaAs.

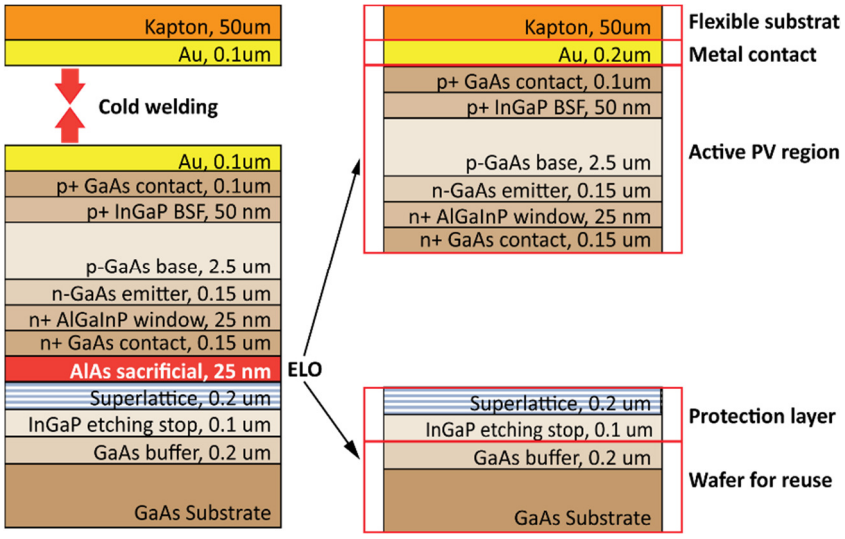


Fig. 9.2: Modified protection layer scheme where the top GaAs layer is replaced by a 5 period AlGaAs/GaAs superlattice (SL) that can bend defect propagation toward the wafer edges. AlAs is the sacrificial layer removed during ELO. The active solar cell epitaxial layers are grown on the SL protection layer surface.

The critical stress of dislocation threading in AlGaAs is larger than that of GaAs[5], and hence the SL results in bending dislocations and other defects toward the wafer edges, removing them along with the SL during the protection layer etch-off process[6,7]. On each growth cycle, the lower GaAs buffer (or SL buffer) thickness will increase. Hence, after approximately 20 growths, these layers will have a total thickness of ~10 μm. CMP can then be used to remove the accumulated GaAs or SL buffer layers together with any residual roughness and accumulated defects without causing thickness loss to the parent wafer, while leaving an epi-ready surface for wafer reuse.

9.3.2 Mini-concentrator arrays with exceeding 5× concentration

To decrease the cost of solar cells an additional 5×-10×, the devices can be attached to parabolic or compound parabolic mini-concentrators using the automated process flow described in Fig. 9.3. The mesas patterned prior to ND-ELO process can be used such that parallel trenches are etched into the epitaxial layers across the wafer surface down to the AlAs sacrificial layer to form narrow, raised mesas. Next, an elastomeric stamp (e.g. PDMS) is metallized and attached at very low pressure to the raised regions of the epitaxial layer and its metalized surface. In this geometry, the *n* and *p* layers of the cells in Fig. 9.2 are reversed. Then, the upper (*n*-type) surface of the solar cells is patterned and metalized to allow for illumination and contact via that surface. Next, the elastomer is stretched to approximately double its length and wrapped around a cylinder. The cylinder is used to press against an array of previously fabricated, molded and metalized cylindrical paraboloids that are planarized with a transparent (e.g. polymer) medium. The appropriate spacing between strips is adjusted by translating the substrate beneath the roller. Alternatively, a flat elastomer handle can be deformed out of plane toward the concentrator array during the placement of each strip. To prevent the degradation of concentrator performance due to

moisture and dust, a super-hydrophobic coating will be applied directly on its surface. For the applications where there is severe weather or environmentally adverse conditions, the array can be fully encapsulated by plasma-deposited SiO_2 with a super-hydrophobic coating.[8]

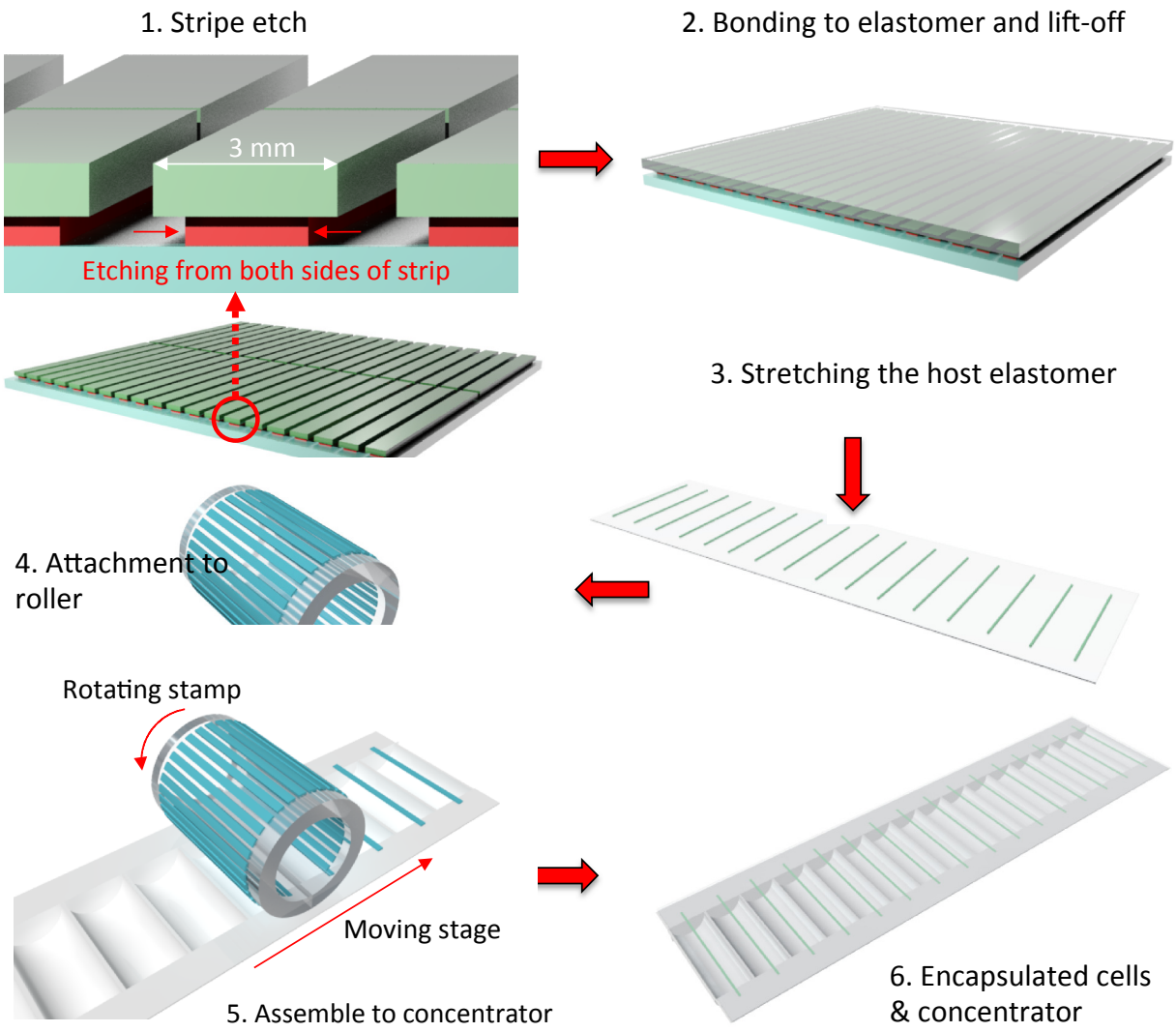


Fig. 9.3: Example process flow for fabricating integrated GaAs solar cell/mini-concentrator arrays. 1. Channels are patterned and etched to the sacrificial layer, defining the stripes. 2. Once patterned, the wafer is bonded epi-side to an elastomer and 3. Stretched over the surface of a 4. Roller. 5. The stripes are then cold-weld bonded to the mini-concentrator array (either the top or bottom side) to 6. Form the concentrator/solar cell arrays.

The concentrator can be fabricated via one of two processes. In the first, a glass master is patterned to form the CPC shape (Fig. 9.4). A polymer is then poured over the mold and cured by baking, forming the permanent CPC shape, after which it is removed from the mold. An alternative is to use a suitably shaped hollow mold with vacuum channels at its base.[1,9] A thin plastic sheet is placed over the mold opening, and vacuum is applied while the sheet is heated. The sheet is then pulled into the mold and cooled.

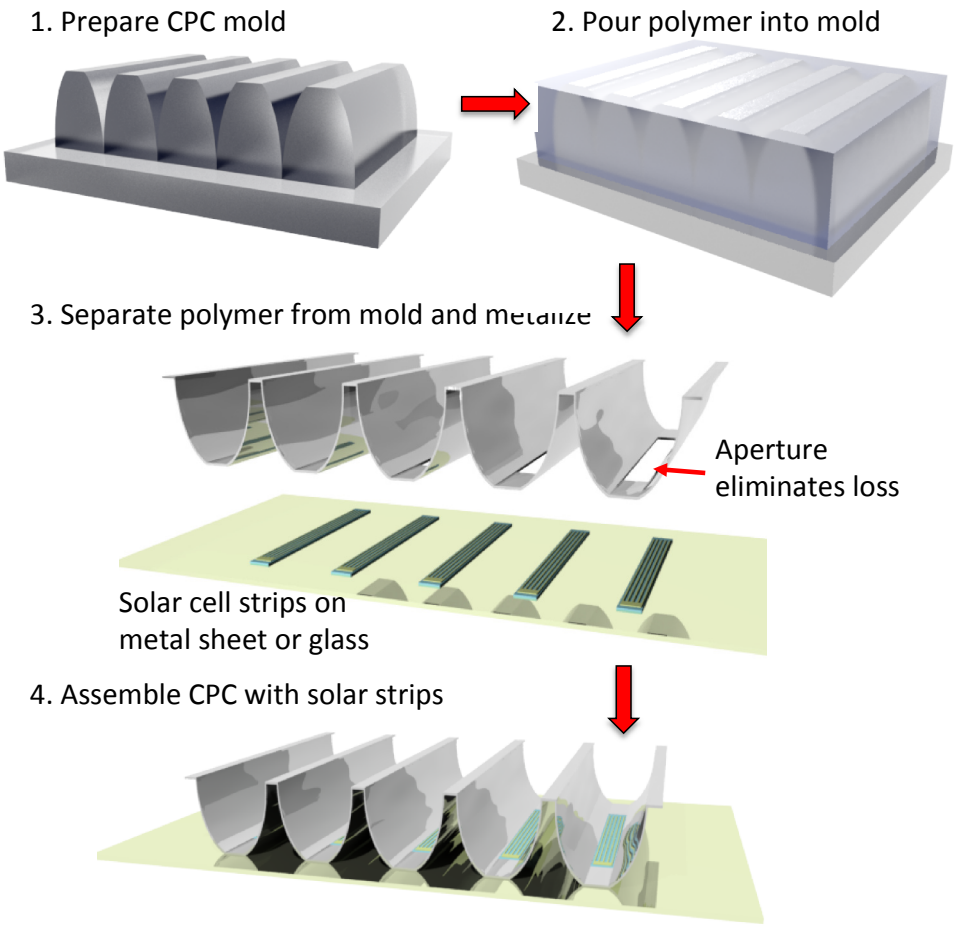


Fig. 9.4: One of two methods for fabricating and integrating compound parabolic concentrators (CPC). 1. Prepare a mold, for example by etching the appropriate pattern in glass using photolithographic patterning. 2. Pour polymer into mold to form concentrator shape. 3. Remove concentrator (along with window apertures) and metalize interior surface with Ag. 4. Attach solar cell array to CPC by cold weld bonding forming contact fan out.

Au pad is pre-deposited onto the bottom surface plane, which is cut open to form a window aperture to eliminate light loss incident on the cell. This pad forms a fan out contact, and also is the surface onto which the array of solar cells is cold-weld bonded. The entire molded array should be extremely lightweight and have limited flexibility since it is comprised only of plastic and thin metal films.

9.3.3 Increasing cell efficiency using back surface reflectors

One means to increase cell efficiency is to use a reflector on the back surface of the cell. Indeed, a significant advantage of thin ELO cells is that incident light not absorbed by the cell can be reflected for a second pass, whereas light that passes through cells supported by the original wafer is absorbed far from the *p-n* junction, and hence is lost.[10] This becomes particularly important at the near infrared absorption (NIR) edge of the GaAs cell (at a wavelength of 0.88 μm), where a photon that is absorbed at a shorter wavelength is re-emitted at the band edge, and is ultimately lost as radiation. However, by placing a high reflectivity distributed Bragg reflector (DBR) on the bottom cell surface, the weakly absorbed NIR radiation will experience multiple bounces.[11] This limits radiative cell losses, moving the cell efficiency much closer to its thermodynamic limit. Indeed, photon recycling has led to record high efficiencies of 28.8% in GaAs solar cells.[12]

In Fig. 9.5, we show a comparison between a conventional substrate/thin-film solar cell and a bi-facial GaAs cell bonded to the metallized (and hence reflecting) secondary substrate, whereby a dielectric (TiO_2/SiO_2) DBR is grown on the back cell surface. Minimizing the loss of photons from the cell is extremely important for photon recycling, which increases the open circuit voltage by cycling the internal emission and reabsorption process more than 50 times. Bi-facial GaAs cells differ from that described above, in that both top and bottom ohmic contact layers are

patterned. Hence, the absorption loss due to the bottom Ohmic contact layer is minimized, and reflection from the rear surface mirror is enhanced. Back-side patterning requires the use of a handle. The process flow is as follows: Following semiconductor growth, the DBR is grown on the epi surface, followed by patterning and deposition of the grid. Next, a temporary handle is attached, followed by ND-ELO. It may be necessary to protect the mirror edges during etching using a polyimide coating. A similar patterning and grid deposition process on the back surface then follows. The handle is used to apply pressure to the bi-facial cell and the Au-coated substrate to form the cold-weld bond. The substrate Au coating provides a high reflectance surface useful for reflecting shorter wavelength light is not absorbed in its first pass.

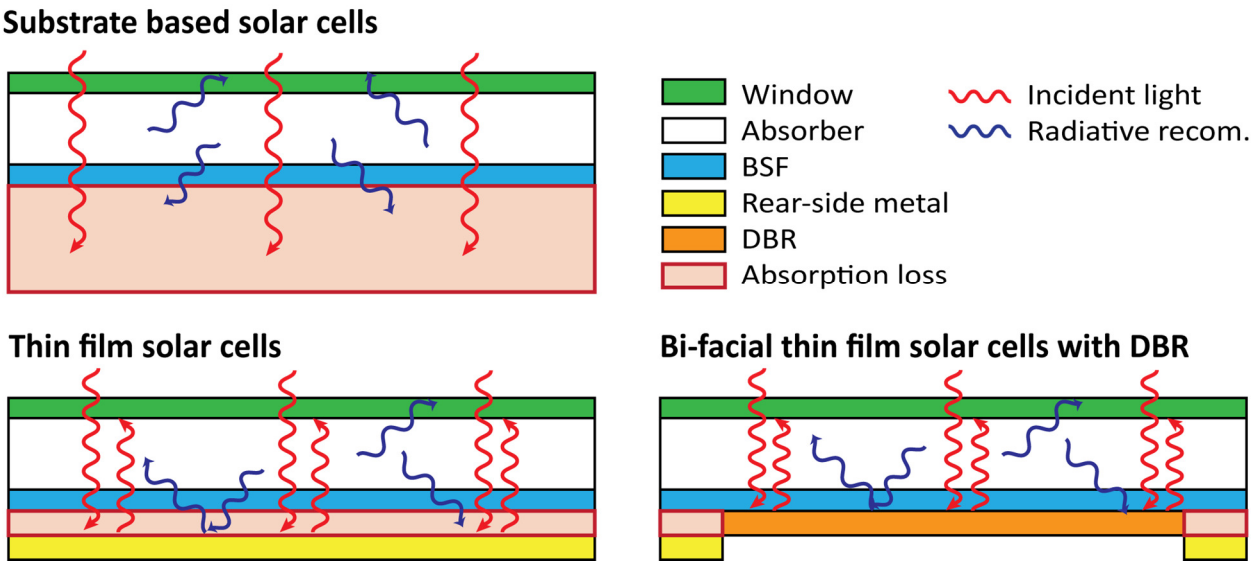


Fig. 9.5: Comparison of absorption processes between conventional substrate/thin film solar cells and bi-facial GaAs solar cells with rear NIR reflecting distributed Bragg reflecting mirrors. High reflectance of the DBR and minimum absorption losses by the patterned back ohmic contact layer enhance the photon recycling.

The sputtered DBR will consist of at least 10 periods to achieve >99% reflectivity in the NIR, designed for a pass band of 200 nm centered at 790 nm. The objective is to achieve an efficiency increase of approximately 2% in addition to the as-grown cell efficiency of approximately 23%. We note that a simple bilayer dielectric antireflection coating tuned to shorter wavelengths (<600 nm) will be grown on the top surface of the solar cell.

9.3.4 Monolithic integration of microinverters with thin-film solar cells

A photovoltaic cells generate a direct current (DC) output; therefore, the extra solar inverters are generally accompanied to convert the DC output into a utility frequency alternating current (AC) which can be fed into a commercial electrical grid or off-grid electrical systems. The inverter is an essential component in a photovoltaic panel, at the same time, it takes a considerable portion of balance of system (BOS) cost. Therefore, the integration of inverter with photovoltaic cells provide a potential to reduce the cost of photovoltaic system. Here, we are proposing a monolithic integration of microinverter with a thin-film III-V solar cells via epitaxial lift-off (ELO) process and cold-welding. The integrated microinverter on each solar cell allows the parallel connection of individual cells in a modular way; therefore, it provides an enhanced power generation especially under the shaded condition compared with the photovoltaic system using single inverter.

We have shown that ND-ELO can also be used to transfer GaAs field effect transistors to flexible substrates without degradation of their operating characteristics in Chap 5. Thin-film HEMT transistors can be integrated with a solar cell array and bonded to a Kapton foil to implement the H-bridge DC/AC inverter in Fig. 9.6. By switching G1/G4, on/off while switching G2/G3 off/on, DC/AC inversion is achieved using an external transformer. The transistor epi-layers are grown prior to the solar cell layers on the parent wafer. After bonding and ND-ELO, the

structure is inverted, leaving the transistor layers on top. The transistor mesa is then etched, and metal interconnects are deposited. Since transistor mesas are roughly 10^{-4} times smaller than the solar cells, the loss of active area is negligible.

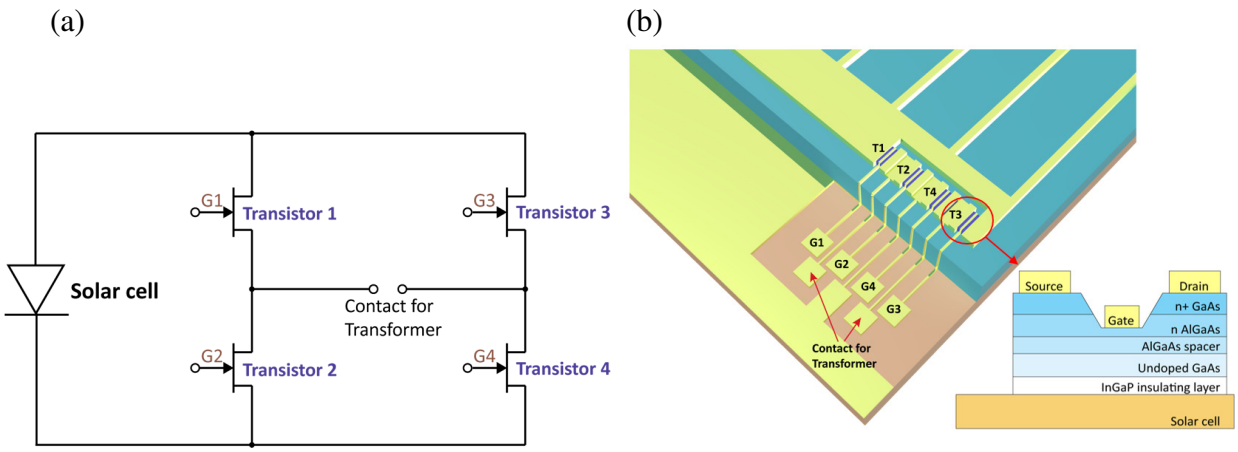


Fig. 9.6: (a) H-Inverter circuit plus solar cell array. (b) Monolithic integration scheme of a GaAs HEMT transistor plus solar cell cold-weld bonded to a flexible substrate.

The integrated microinverter on each solar cell allows the parallel connection of individual cells in a modular way; therefore, it provides an enhanced power generation especially under the shaded condition compared with the photovoltaic system using single inverter (Fig. 9.7 (a) and (b)). Furthermore, the microinverter embedded with power optimizer can provide a maximum power point tracking functionality by pinpointing individual cell's ideal voltage and producing at its maximum power.

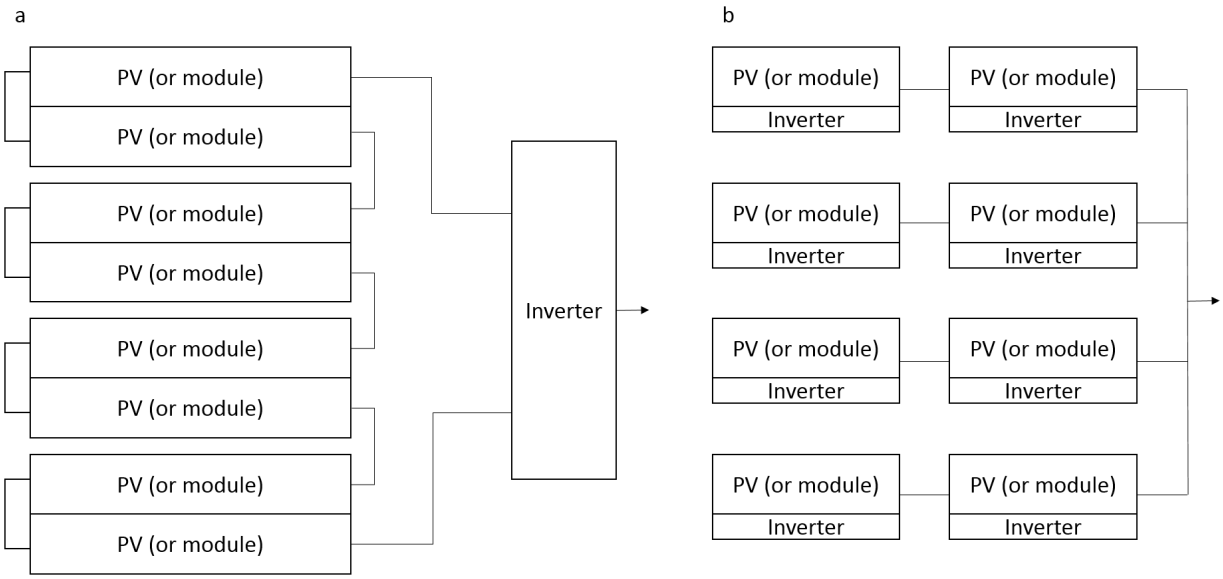


Fig. 9.7: Schematic illustration of solar power system (a) Large number of panels connected to a single inverter. (b) Each solar cell or module incorporates its own inverters (known as microinverter system).

The innovations demonstrated and envisioned are poised to revolutionize the cost structure and acceptance of high efficiency solar cells. This combination of technologies promises to make GaAs cost competitive with the most aggressive solar technologies deployed to date, while delivering flexibility and the highest specific power (i.e. power/weight) performance of any other known solar cell technology.

CHAPTER IX

Bibliography

1. Xu, X., Davanco, M., Qi, X. & Forrest, S. R. Direct transfer patterning on three dimensionally deformed surfaces at micrometer resolutions and its application to hemispherical focal plane detector arrays. *Org. Electron.* **9,** 1122–1127 (2008).

2. Woodhouse, M. & Goodrich, A. a manufacturing cost analysis relevant to single and dual junction photovoltaic cells fabricated with III-Vs and III-Vs grown on Czochralski Silicon. *NREL Rep. No. PR-6A20-60126* 92 (2014).

3. Lee, K., Zimmerman, J. D., Hughes, T. W. & Forrest, S. R. Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics. *Adv. Funct. Mater.* **24,** 4284–4291 (2014).

4. Horng, R.-H. *et al.* Thin Film Solar Cells Fabricated Using Cross-Shaped Pattern Epilayer Lift-Off Technology for Substrate Recycling Applications. *IEEE Trans. Electron Devices* **59,** 666–672 (2012).

5. Hayafuji, N. *et al.* Effectiveness of AlGaAs/GaAs superlattices in reducing dislocation density in GaAs on Si. *J. Cryst. Growth* **93,** 494–498 (1988).

6. Bedair, S. M. *et al.* Defect reduction in GaAs grown by molecular beam epitaxy using different superlattice structures. *Appl. Phys. Lett.* **49,** 942 (1986).

7. Petroff, P. M., Miller, R. C., Gossard, A. C. & Wiegmann, W. Impurity trapping, interface structure, and luminescence of GaAs quantum wells grown by molecular beam epitaxy. *Appl. Phys. Lett.* **44,** 217 (1984).

8. Nakajima, A., Hashimoto, K. & Watanabe, T. Recent Studies on Super-Hydrophobic Films. *Monatshefte fuer Chemie/Chemical Mon.* **132,** 31–41 (2001).

9. Pfeiffer, C., Grbic, A. & Forrest, S. R. Novel methods to analyze and fabricate electrically small antennas. in *2011 IEEE Int. Symp. Antennas Propag.* 761–764 (IEEE, 2011). doi:10.1109/APS.2011.5996824

10. Bauhuis, G. J., Mulder, P., Haverkamp, E. J., Huijben, J. C. C. M. & Schermer, J. J. 26.1% thin-film GaAs solar cell using epitaxial lift-off. *Sol. Energy Mater. Sol. Cells* **93,** 1488–1491 (2009).

11. Miller, O. D., Yablonovitch, E. & Kurtz, S. R. Strong Internal and External Luminescence as Solar Cells Approach the Shockley–Queisser Limit. *IEEE J. Photovoltaics* **2,** 303–311 (2012).

12. Green, M. A., Emery, K., Hishikawa, Y., Warta, W. & Dunlop, E. D. Solar cell efficiency tables (version 44). *Prog. Photovoltaics Res. Appl.* **22,** 701–710 (2014).