Optimization of Signal-to-Noise Ratio in Semiconductor Sensors via On-Chip Signal Amplification and Interface-Induced Noise Suppression

by

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To my beloved family

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Chapter 1. Introduction

Radiation detectors are now used in a large variety of fields in science and technology, including nuclear physics, elementary particle physics, optical and x-ray astronomy, medical devices, and materials testing – and the number of applications is growing continually. Detectors are used by both industry and academia in those instruments that utilize neutrons, electron and ion beams, and high-energy photons, whether x-rays or gamma-rays. Modern detection systems consist of two constituent parts: the detector and the instrumentation that provides the actual measured signal. Semiconductors and scintillators are two general classes of solid materials used as the active materials in radiation detectors. Scintillators requires a readout instrument that converts light emitted from the scintillating bulk into charge carriers. The photomutiplier tube (PMT) is the instrument that converts light into an electronic signal with low noise and high gain. Since the photomultiplier has inherent weaknesses; large volume, high bias voltage requirement, and susceptibility to magnetic fields, solid-state photomultipliers (SSPMs) are the best candidate to displace the bulky vacuum tube. For the semiconductor radiation detectors, we are investigating the performance enhancement of the detectors via the suppression of noise induced from the semiconductor interface.

Although the photomultiplier remains a unique and important optoelectronic component, silicon SSPMs already have been developed and demonstrated as viable alternatives to the traditional photomultiplier tube. However, recently developed advanced scintillators, which have the ability to distinguish gamma-ray interaction events from those that accompany neutron impact, require improved quantum efficiency in the blue or near UV region of the spectrum where Si SSPMs are lacking. We are therefore developing wide band-gap SSPMs which meets the optical responsivity requirements while delivering reduced dark noise, the latter enabling the deployment of larger sensing areas. $Al_{0.8}Ga_{0.2}As$ is adopted as a SSPM material based on its optical and electrical characteristics. We tested the electrical performance with design variations, focusing on the realization of consistent, uniform breakdown. Chapter 2 will discuss the development of the wide band-gap SSPMs.

Semiconductor detectors for nuclear radiation and particles have been in development for several decades. The semiconductor detectors have unique properties that cannot be replicated by other types of detectors. The advantages include: 1) precise position sensing with high readout speed, 2) the direct conversion into charge carriers, and 3) the possibility of integrating the detector and the interface circuit on a common substrate. Silicon is the most widely used semiconductor and popular in the semiconductor detector field as well due to its fast response and its crystalline properties, possessing a band structure that is neither totally conducting nor insulating. Its relatively low cost, its room temperature operation, and the availability of well-established processing technologies also make it a suitable material for semiconductor radiation detectors. Although the material's low atomic number and relatively high leakage currents limits its application to low-energy x-ray and charged-particle detection [1], high-resistivity Si with good charge carrier transport properties has been produced and has achieved success as a radiation detector material over the past few years. To increase the operational limit to increasingly small energy depositions, we have lowered the dark current.

Although thermal and shot noise both contribute to the noise in a semiconductor sensors, the 1/f noise can dominate the total noise for many wide band-gap detectors [2], [3]. In Chapter 3, we take a closer look at the properties of the phonon-based 1/f noise and how to quench the charge-mobility fluctuations via surface control. We evaluate acoustic reflectance at the semiconductor metal interface by calculating reflectance coefficient via the roaming phonon microgradient (RPMG) model. Si radiation detectors are fabricated and the hypotheses evaluated with different geometries and metal types.

Fundamental methods to reduce the semiconductor noise were therefore developed, but we also sought to increase the device signal so that the SNR could be maximized. In Chapter 4, we discuss an effort to deliver a breakthrough in particle-detection sensors, by integrating an amplifying junction as part of the detector topology. Focusing on energetic particle detection in the heliosphere, the resulting increase in the resolution with which the deposited charge is measured results in far more precise energy and position measurements, from which the certainty in the particle identification is increased. Silicon is chosen as the material upon which the avalanche particle detector (APaD) is developed because it possesses high stopping power for ions, low material cost, and an extensive microelectronic fabrication base.

During the research, we successfully demonstrated the feasibility of improving the energy resolution relative to those low-noise designs that don't possess on-chip amplification by modeling, fabricating, and characterizing proof-of-concept planar and partitioned detectors. We succeeded in making n/p breakdown junctions that breakdown near 40 V, and have multiplication gains up to 80 times. Our modelling has shown that a gain of ~8 is ideal if one is attempting to optimize the SNR, which is realized in the experimental detectors at an excess bias of 3 V. At that voltage, the energy resolution for 81 keV gamma-rays can be reduced from 2.12 % to 0.96 % (for a k = 0.2), the degree of improvement limited by the leakage current of the devices, and within a factor of 2 of the ultimate Fano limit (0.53 %). For the sensors developed, the result is limited by multiplication noise and leakage current, rather than the preamplifier noise, as desired.

Chapter 2. Wide band-gap solid-state photo multiplier

2.1 Introduction

Many nuclear detection methods are developed using physical phenomena known to produce electrical signals in response to energy deposition from ionizing radiation. One of the main detection methods is to use scintillation materials that luminesce upon their excitation. When an incident particle interacts with the scintillator, the material absorbs its energy through charge-excitation interactions and re-emits the absorbed energy in the form of light, upon the de-excitation of the charge carriers. A scintillation crystal is typically coupled to a photomultiplier tube, which absorbs the light emitted by the scintillator and reemits it in the form of electrons via the photoelectric effect and multiplies the charge number by roughly a million times through the multiple dynodes in the structure. The underlying gain mechanism of the PMT is that the photoelectron leaving the photocathode is accelerated in vacuum over some distance by an electric field. That primary electron then gains enough energy during its flight to strike a dynode and cause secondary electrons to be emitted toward subsequent dynodes. These electrons increase exponentially by passing through multiple dynodes until collected in an anode. The PMT's excellent performance, which includes high gain, low noise, and fast response makes it an essential tool in nuclear and particle physics, medical imaging, astronomy, as well as radiation detection. To date, PMTs have been widely deployed for many of the applications that require detection of low light levels. However, it also has multiple deficiencies that include: (1) low quantum efficiency

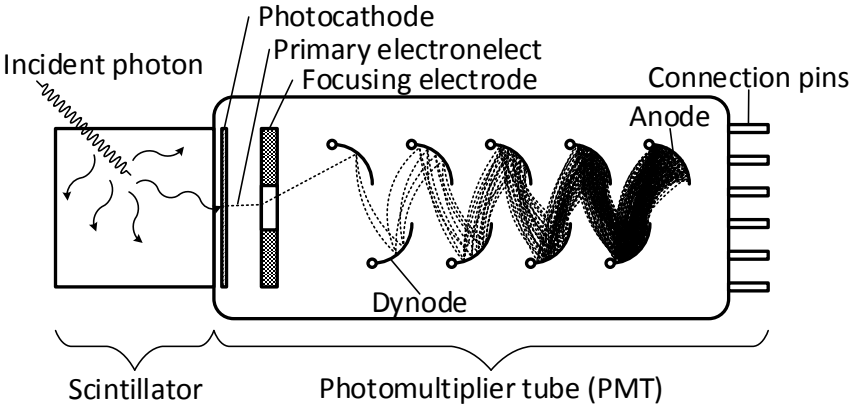


Fig. 2.1. Operating mechanism of scintillator and photomultiplier tube.

of the photocathode for UV light, (2) high voltage (~1000 V) requirements, (3) high cost, (4) gain and timing sensitivity to the presence of external magnetic fields, and (5) their vacuum tube structure inherently makes them bulky and delicate. A gain of 10^6 requires a high bias voltage of 1-2 kV, which increases the power consumption and requires costly high-voltage power supplies. Solid-state devices however have many practical advantages over the PMTs in which solid-state devices significantly reduce volume, consume less power, and are not as delicate as PMTs. Solid-state devices use the avalanche breakdown effect as a multiplication mechanism to achieve comparable gain values as PMTs and are usually called an avalanche photodiode.

2.2 Why wide-band-gap material?

Silicon solid-state photomultipliers (SSPMs) already have been developed and demonstrated as viable alternatives to the traditional photomultiplier tube for small area applications. However, many advanced scintillation materials, which provide improved neutron-gamma discrimination such as $Cs_2LiYCl_6 : Ce$ (CLYC), require a strong absorption response in the blue and near-UV region of the spectrum in order to minimize the statistical counting noise associated with the photon-to-electron creation process. Furthermore, the size of silicon SSPMs are inherently limited by the material's relatively low band-gap (1.12 eV), which governs the dark count rate.

In addition, recent advances in the development of scintillation detectors has produced materials that provide dual neutron and gamma-ray detection capabilities with improved isotope identification. Many of these advanced scintillators emit light in the blue or near UV region of the spectrum. To utilize the advanced scintillation detectors, such as CLYC, a robust, high-performance, low power, and mass-deployable photodetector technology is required. Both photomultiplier tubes (PMTs) and silicon photomultiplier exhibit limitations. For employment of a large UV-emitting scintillating panel, a wide band-gap semiconductor photodetector could be an ideal solution to replace PMTs and silicon based photodetectors.

One candidate semiconductor material is AlGaAs, which has a tunable band gap from 1.43 to 2.17 eV depending on the aluminum concentration, since it has large band gap energy, potentially high quantum efficiency in the near UV, and attenuated photon responsivity above 500

nm (for $Al_{0.8}Ga_{0.2}As$) , improving its solar-blind properties. The large band gap suppresses the dark current generated from thermally excited carriers. The absorption length of $Al_{0.8}Ga_{0.2}As$ at wavelengths between 300-500 nm is long compared with silicon (approximately 13 nm at 35 nm, 100 nm at 400nm [4]), which is a region of interest for using emerging scintillation materials, such as CLYC, that have a peak emission around 350-450 nm. A low-noise solid-state detector with high detection efficiency within the optical range of interest provides an ideal component for nuclear detectors, allowing for a large-area photodetector coupled to a large volume scintillation material for maximum sensitivity.

2.3 Design of Photodiode Element

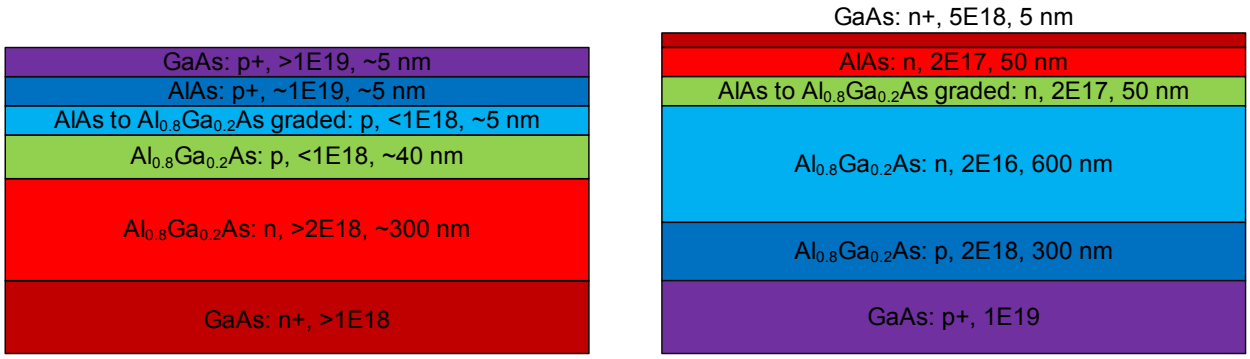
The starting wafers described in this work were obtained from two commercial vendors who were given the specifications illustrated in Table 1. The wafers were fabricated, and referred to as LandMark (LM) and El-Cat (EC) respectively (the two wafer vendors), at different times as numbered. The illustration shows the layer structure derived from commercially available metal-organic chemical vapor deposition (MOCVD) epi-layers. Each layer structure is developed based

Table 1. The general vertical structure of the avalanche photodiode element

1 LM PIN	2 EC PIN	3 LM PN+
GaAs: p+, as high as possible, > 10^{19} — As thin as possible	GaAs: p+, as high as possible, > 10^{19} — As thin as possible	GaAs: p+, as high as possible, > 10^{19} — As thin as possible
$Al_{0.8}Ga_{0.2}As$: p, < 1 x 10^{18} — ~300 nm	$Al_{0.8}Ga_{0.2}As$: p, ~ 5 x 10^{17} — ~300 nm	$Al_{0.8}Ga_{0.2}As$: p, < 1 x 10^{18} As low as possible — ~300 nm
$Al_{0.8}Ga_{0.2}As$: i, < 1 x 10^{17} — ~200 nm	$Al_{0.8}Ga_{0.2}As$: i, < 1 x 10^{16} — ~200 nm	
$Al_{0.8}Ga_{0.2}As$: n, ~ 2~3 x 10^{18} — ~200 nm	$Al_{0.8}Ga_{0.2}As$: n, ~ 5 x 10^{18} — ~200 nm	$Al_{0.8}Ga_{0.2}As$: n+, ~ 2~3 x 10^{18} — ~200 nm
GaAs n+ substrate (>10^{18})	GaAs n+ substrate (>10^{18})	GaAs n+ substrate (>10^{18})
4 EC PN+	**5 LM PN+**	**6 EC PN+**
GaAs: p+, as high as possible, > 10^{19} — As thin as possible	GaAs: p+, as high as possible, > 10^{19} — As thin as possible	GaAs: p+, as high as possible, > 10^{19} — As thin as possible
$Al_{0.8}Ga_{0.2}As$: p, < 1 x 10^{17} — ~300 nm	$Al_{0.8}Ga_{0.2}As$: p, 1 x 10^{18} — ~300 nm	$Al_{0.8}Ga_{0.2}As$: p, < 1 x 10^{17} — ~300 nm
$Al_{0.8}Ga_{0.2}As$: n+, ~ 5 x 10^{18} — ~200 nm	$Al_{0.8}Ga_{0.2}As$: n+, ~ 2~3 x 10^{18} — ~200 nm	$Al_{0.8}Ga_{0.2}As$: n+, ~ 5 x 10^{18} — ~200 nm
GaAs n+ substrate (>10^{18})	GaAs n+ substrate (>10^{18})	GaAs n+ substrate (>10^{18})

on breakdown characteristics of the fabricated devices. We will focus on the pn+ diode structures when discussing the results.

From the illustrated structure shown in Table 1, surface proximate recombination can reduce the quantum efficiency due to trapping centers and band bending at the surface. Since the shorter wavelength photons have a lower chance to penetrate deep inside the bulk material due to the larger absorption coefficient, photo-generated carriers have a higher probability of recombination at the surface dead layer. In order to remove such a dead layer, the AlAs layer which has longer absorption length is introduced to deepen the photo generated carriers location so that the carriers can be generated where the depletion region is formed and collected through their drift along the electric field toward the bounding electrodes. The new vertical structure of the AlGaAs photodiode elements includes the AlAs layer and the following grading region from AlAs to $Al_{0.8}Ga_{0.2}As$ that are expected to improve optical response of the device. When contemplating the design of the avalanche diode, we must first select the doping of the underlying substrate, which impacts the ease with which it is depleted as well as the direction of current flow. In GaAs, electrons drift over ten times as fast as holes (if below their saturated velocities), and they can therefore be accelerated to the energy needed to ionize secondary charges more easily that holes, an effect embodied in the ionization coefficient, one consequence of which is that the excess noise is smaller in avalanching configurations. Thus, one generally designs the diode such that electrons are drifted into the multiplying region. Specifically, the electron mobility, at 8500 $cm^2/V{\cdot}s$ is 20 times greater than the hole mobility (400 $cm^2/V{\cdot}s$), which is even worse than that of Si (450 $cm^2/V{\cdot}s$). We designed two different polarity structures as shown in Fig. 2.2.



(a) (b)

Fig. 2.2. The vertical structure of the new photodiode element with an additional AlAs layer.

In order to create a diode with uniformly distributed avalanche initiation, the diode's edge where the electric field is usually more concentrated should not break down before the central area of the diode. An earlier study showed that the sloped sidewall reduces the electric field at the surface by increasing the effective depletion width at the surface [5]. A beveling structure is adopted for our diode elements due to its edge breakdown reducing capability. However, the corners of a rectangle diode produce intense electric fields so that the corners can easily initiate the breakdown as shown in Fig. 2.3 for a silicon diode. With increasing bias, the diode breaks down first at its corners, then at its edges.

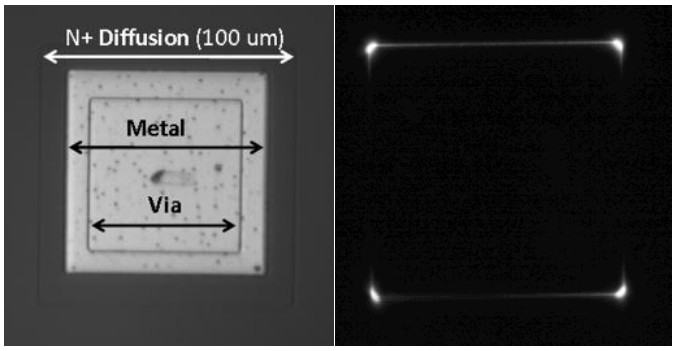


Fig. 2.3. Electroluminescence image (right) of a single –diffusion square diode operated above breakdown, as imaged by a CMOS camera on a probe station microscope [6].

Diodes are designed with different geometric shapes to test the corner breakdown. The shape changes gradually from square to circle with varying corner curvature as illustrated in Fig. 2.4. The breakdown voltage and dark current of the square diodes, which can be affected by edge or corner effects that would compromise the device performance, were compared to those of the circular diodes. The square diodes are more vulnerable to corner breakdown, but are preferred in array designs due to the increased optical detection efficiency that accompanies high fill factors. Circular diodes, in contrast, are more robust to breakdown since they do not have corners, but the overall fill factor has to be sacrificed. Thus, the square diodes without corner breakdown are the most desirable design.

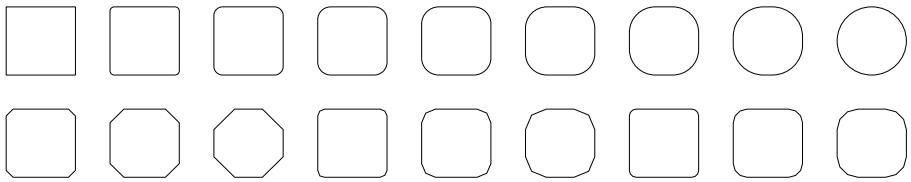


Fig. 2.4. Design of diodes with shape variation with different corner curvature.

2.3.1 Device simulation

Device simulations for the electric field exhibit how the depletion region forms and develops as the bias voltage is varied for the p+ substrate device shown in Fig. 2.2b. The result, as illustrated in Fig. 2.5, shows that the depletion region is generated at the n-type/p-type AlGaAs interface and starts to grow toward the n-type AlGaAs layer since the n-type AlGaAs has two orders of magnitude lower doping concentration than the p-type AlGaAs. At 7 V bias, the depletion region reaches the AlAs-to-AlGaAs grading region and the expansion rate nearly stops even with a higher bias voltage because of the high doping of the region.

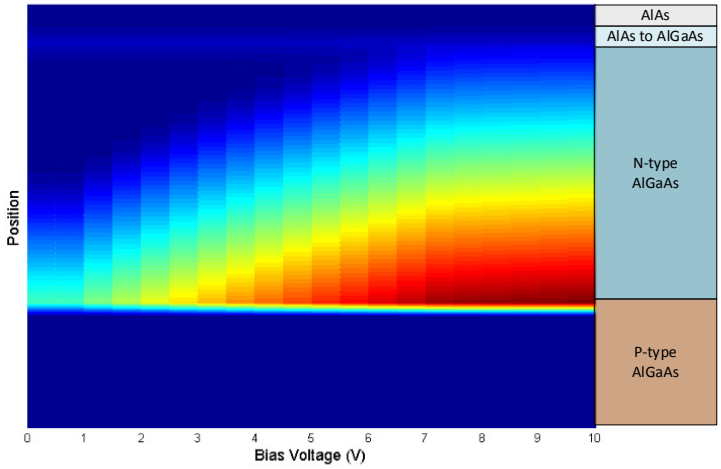


Fig. 2.5. Electric field development for the p+ GaAs substrate device, Fig. 2.2b, as bias voltage increase. Depletion region develops at the interface of the p/n AlGaAs interface toward the n-type AlGaAs. The region stops growing until it is fully depleted at 7 V bias.

The electric field result above indicates that the quantum efficiency will improve as the depletion region is expanded to the surface because the photo-generated carriers are mostly located near surface especially for the short wavelength photons. We simulated the external quantum

efficiency (EQE) of the AlGaAs photodiode element with wavelength from 250 nm to 650 nm, and with multiple bias voltages, varying from 0 V to 7 V. With a bias voltage of 0 V, the maximum EQE is 52 % at 470 nm and the response at the range of 300 nm to 400 nm is less than 40 %. However, as the bias increases, the EQE at the 300 nm – 400 nm range increases rapidly and the peak location gradually move towards 350 nm as shown in Fig. 2.6. At 0 V bias, most of the photo-generated carriers from the 300 nm – 400 nm wavelength photons have a lower chance to diffuse into the depletion region, located in close proximity to the n/p AlGaAs interface, and this therefore, lowers the EQE. Once the bias voltage is increased and the device is fully depleted at 7 V, the EQE reaches to almost 100 % as indicated in Fig. 2.6.

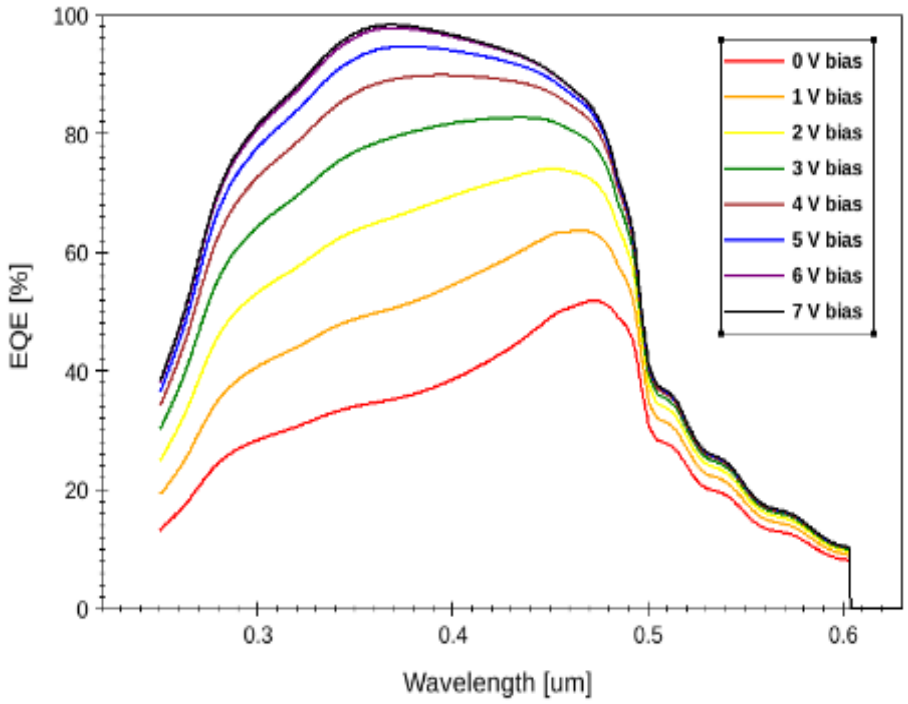


Fig. 2.6. Simulated external quantum efficiency as a function of wavelength with various bias voltages from 0 V to 7 V, which fully depletes the device.

In order to increase the external quantum efficiency further, an anti-reflective coating layer is designed to minimize the reflected light in the wavelength range of interest; specifically in the range from 380 nm to 420 nm where the peaks of the advanced scintillator CLYC and standard scintillator NaI(Tl) reside. Since the nitride layer is already deposited as a passivation layer, which will be discussed in Chapter. 2.4, it can also work as an anti-reflective coating if the thickness is

controlled accordingly. We targeted minimum reflectance from 300 to 500 nm wavelengths and simulation indicated approximately a thickness of 40 nm of the nitride layer results in low reflectance at the given range of the wavelengths as illustrated in Fig. 2.7. The thickness of the layer has to be carefully controlled when the device is fabricated, because a small variation in the thickness of the nitride layer greatly alters the valley point of the simulated reflectance curves. The simulation result is based solely on the epitaxial structure without the GaAs substrate; thus, beginning from 460 nm, the absorption rate starts decreasing rapidly and the transmittance rate starts increasing at higher wavelengths. The simulations suggest that the EQE should nearly match the internal quantum efficiency near 400 nm, as desired.

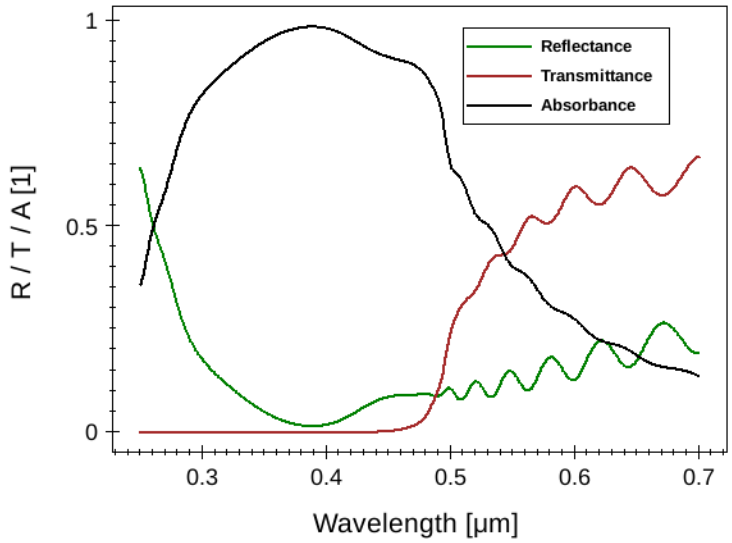
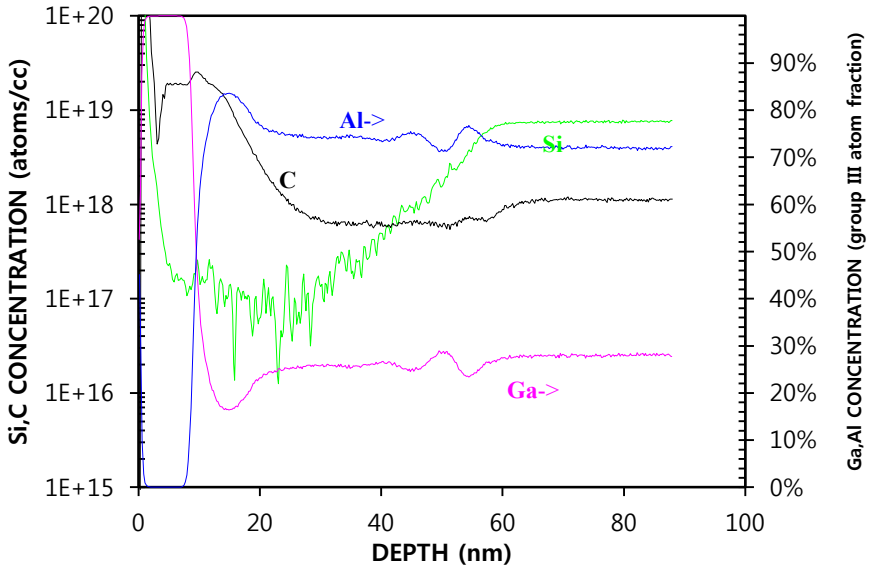


Fig. 2.7. Reflectance, transmittance, absorption rate from the epitaxial layer structure when the anti-reflective coating is consist of 40 nm of a nitride layer.

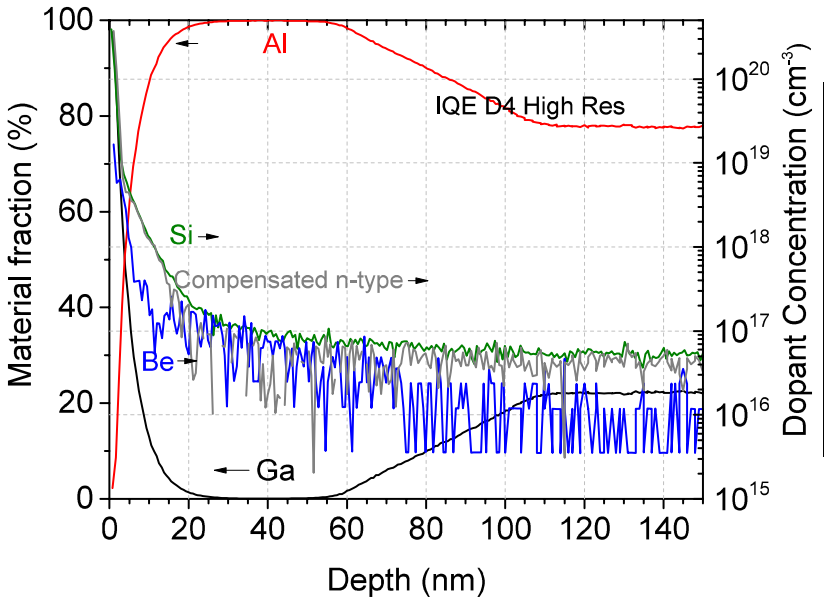
2.4 Secondary ion mass spectrometry (SIMS) analysis

Secondary ion mass spectrometry (SIMS) analyses have been performed for an in-depth understanding of the doping profiles of the delivered wafers. As suggested by its name, the atomic constituents in various near-surface layers can be determined as a function of depth by selectively sputtering the solid and using a mass spectrometer to isolate the backscattered ion stream that results. In all of the wafers, silicon serves as the n-type dopant for AlGaAs, but the p-type dopant varies depending on the MOCVD vendor. In the Landmark epi-layer structure of Fig. 2.8a, carbon

is the p-type dopant, and in Fig. 2.8b, the vendor IQE uses beryllium to compensate the doping in an attempt to make a very low-concentration p-type region.



(a)



(b)

Fig. 2.8. Secondary ion mass spectrometry measurement of the layer structure given in (a) Fig. 2.2a, (b) Fig. 2.2b. The results show the undesired grading layer from the top GaAs layer to the next AlAs layer which absorbs most of the short wavelength light.

The experimental result illustrated in Fig. 2.8 shows a couple of discrepancies between our requested design and the fabricated wafers. One of the main mismatches is observed at the interface between GaAs and AlAs where no transitional graded layer should be. Such a transitional layer changing from GaAs to AlAs is observed through a depth of approximately 20 nm, particularly shown in Fig. 2.8b. Since $Al_xGa_{1-x}As$ with low Al mole fraction has a smaller band gap, many of the short wavelength photons are absorbed at the surface of the window where the graded region is located, as shown in Fig. 2.9, which is derived from a Sentaurus simulation result. This absorption, in turn, lowers the chance that the photo-generated carriers are collected before recombination. This problem is verified with the TCAD simulation, the result from which shows that the limited quantum efficiency due to the undesired grading layer can be improved if the graded layer is removed. The maximum quantum efficiency is 80 % at 370 nm but it is improved to 100 % once the graded layer is etched out, which makes a recessed window, as illustrated in Fig. 2.10. Based on the simulation results, the recessed window design is adopted for our device fabrication to improve the optical response.

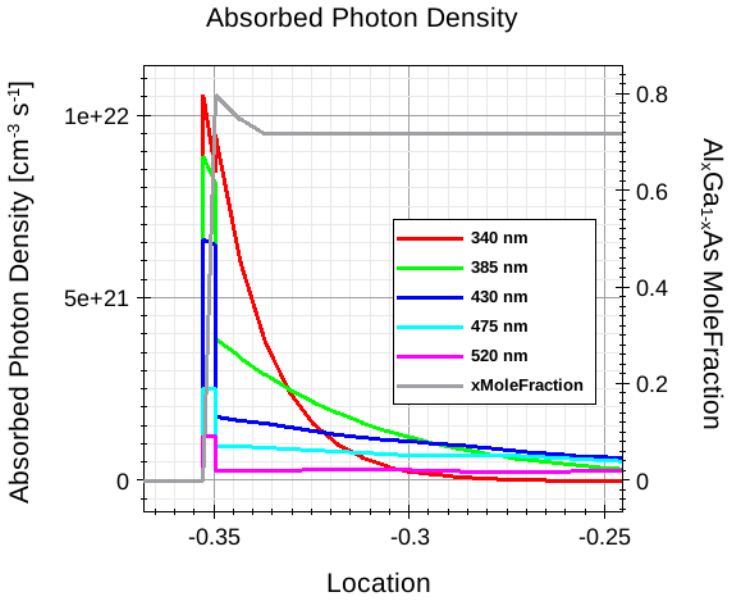


Fig. 2.9. Simulated absorbed photon density with the undesired grading layer (GaAs to AlAs) based on the Fig. 2.8a structure. Grey line indicates Al mole fraction in the layer structure based on SIMS analysis result. The other lines indicate the density of the absorbed photons at certain wavelength as indicated in a legend. Up to 30 % of the photons are absorbed at the grading layer.

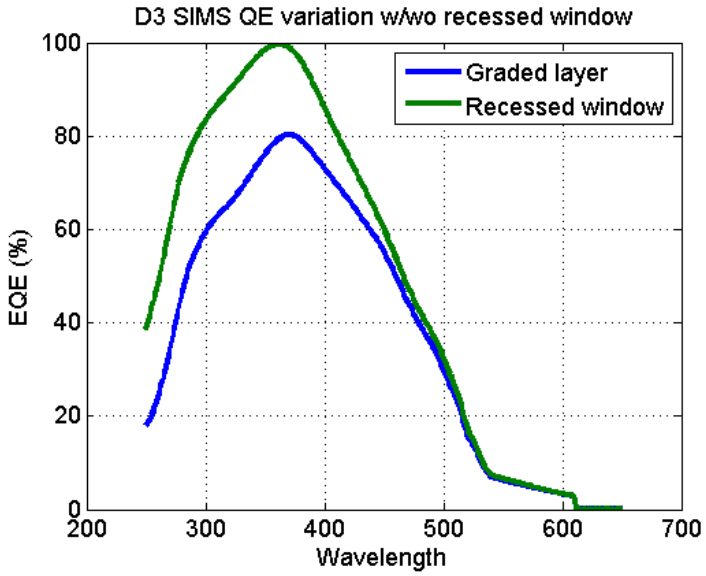


Fig. 2.10. EQE simulation with the graded layer and without the layer. If the window is recessed, the grading layer is etched out, EQE improves around 20 %.

2.5 Fabrication of diode elements

We purchased GaAs wafers with epitaxial grown AlGaAs layers through metal-organic chemical vapor deposition. The fabrication process starts from cleaning the epitaxial grown wafers in which the wafer is dipped in hot trichloroethylene (TCE), acetone, and isopropyl alcohol (IPA) for 10 minutes in turn.

We patterned with a diode defining mask via a photolithography process to define the diode area. Once patterning is done, we etched out areas that are not part of the diodes with either wet etching or dry etching. After the diode definition etching (Fig. 2.11b), we patterned for the window area in which the top GaAs layer (top thin blue layer in Fig. 2.11) is removed because of its high light absorption. The GaAs layer is selectively wet-etched in which the AlGaAs layer serves as an etch stop (Fig. 2.11c). The patterned sample is dipped in citric acid and hydrogen peroxide solution (4:1) for one minute.

One might argue that the beveled edge arrangement would lead to a significant thermally generated dark current because of the large density lattice defects at the beveled edge. Therefore, passivation is necessary to prevent surface recombination and high dark current. Two steps of passivation are included: the first step is sulfur passivation used to tie off the surface dangling bonds, and the second step is a silicon nitride (SiN_x) deposition via plasma-enhanced chemical vapor deposition (PECVD), which is used to cap the sulfide layer and electrically isolate the diode from the metallic interconnects. Sulfur passivation is accomplished using trioctylphosphine sulfide (TOP:S), which is synthesized by combining equimolar amounts of sulfur powder and trioctylphosphine and stirring the mixture while applying gentle heat (50-60 °C) for 12 - 24 hours until the sulfur powders melt [7]. Each device, which contains mesa-etched diode elements, is soaked in TOP:S for 12 hours. After the sulfur passivation, the samples are rinsed with acetone

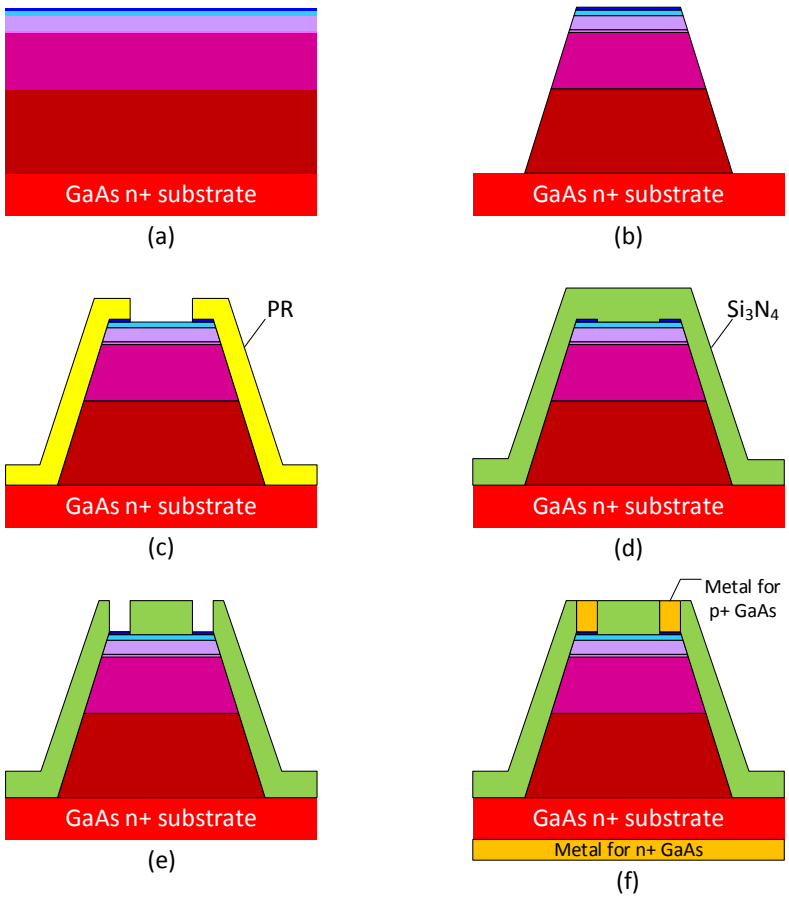


Fig. 2.11. Avalanche photodiode device fabrication process chart.

and IPA to remove all but the mono-layer of sulfur passivation. To enhance the optical response, the window area is etched with citric acid as mentioned above. A silicon nitride layer is deposited with a thickness of 400 Å (Fig. 2.11d) which functions as a passivation layer and an anti-reflective coating layer. Following passivation, ohmic contact to the p+ GaAs is made with an opaque metal stack (Pd/Zn/Pd/Au (5/20/20/300) nm thick), and n+ GaAs contact is made with a Ni/Ge/Au/Ti/Au stack (5/32.5/65/20/300 nm thickness) (Fig. 2.11f). For the ohmic contact to the p-type GaAs, Pd serves as interstitial adhesion layers, Zn serves the role of the p-type dopant, diffusing into the GaAs surface, and Au is used to make electrical contact. For the ohmic contact to the n-type GaAs, Ni is an adhesion layer, Ge is the n-type dopant, Ti is a diffusion stop layer, and Au is for making external contact.

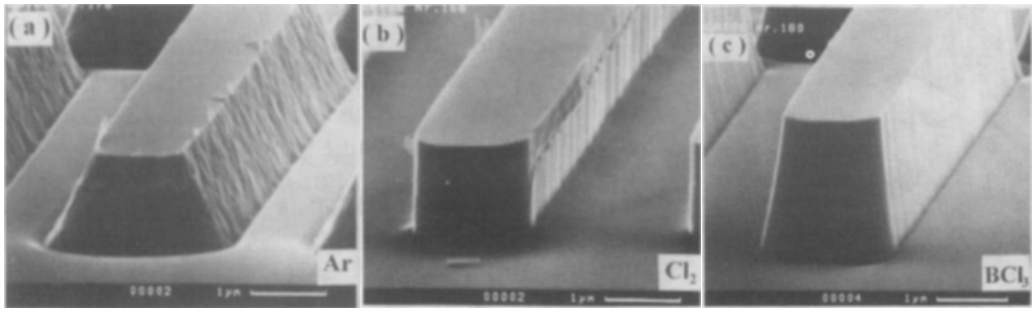
2.5.1 Dry etching for Bevel Edge

Since wet etching is isotropic, it more readily forms a mesa structure compared with anisotropic dry etching, because the top-most layer etches more than the lower layers exposed later in the etch. However, it was hard to control the etch rate and uniformity from the wet etching. We therefore focused our efforts on making bevel-angled sidewall structures via dry etching by using the LAM 9400 facility in the Lurie Nanofabriation Facility (LNF). According to the previous research, bevel angled sidewall structures were achieved with gas variation [8]. From the literature survey, we found that Ar, BCl_3, and Cl_2 gases are commonly used for GaAs etching. Fig. 2.12 shows the influence of the etch gases on etch profiles of GaAs wafer [9]. Etching with Ar ions alone (Fig. 2.12a) produced facets with very rough surfaces and poor anisotropy. The use of Cl_2 and Ar ion beams (Fig. 2.12b) produced relatively good anisotropy but rough surfaces. The BCl_3 and Ar ion-beam (Fig. 2.12c) produced smooth surfaces but with substantial anisotropy. Since non-vertical beveled angles are targeted, Cl_2 gas is ruled out for a mixture that produces a higher degree of bevel etching. We tried to reproduce the results, but were unable to achieve the same results. Experiments have been executed to have similar results by changing the tool parameters as shown in Table 2. The LAM 9400 is a high-density plasma etch tool that uses two different kind of RF power sources; one is a transformer coupled plasma (TCP) inductive RF plasma source that impacts most notably the plasma density, and the other source is a bias RF power source that

controls the ion bombardment energy. With Ar gas only, the etch rate is limited because Ar ions mostly etch out the surface with physical bombardment rather than chemical reactive etching. In the case in which the etch rate is too low, the etching time is extended and the photoresist is hardened severely so that it was hard to remove PR with either solvents or plasma ashing. To increase the etch rate, the plasma density has to be increased in which the TCP power should be increased and the chamber pressure should be decreased [10].

Table 2. Various recipes for each run

	TCP power	Bias power	Chamber Pressure	Ar gas	BCl_3 gas
Recipe 1	500 W	36 W	5.0 mTorr	50 sccm	5 sccm
Recipe 2	500 W	100 W	5.0 mTorr	50 sccm	5 sccm
Recipe 3	300 W	36 W	2.0 mTorr	12 sccm	3 sccm
Recipe 4	800 W	36 W	1.5 mTorr	40 sccm	3 sccm
Recipe 5	800 W	100 W	1.5 mTorr	40 sccm	3 sccm
Recipe 6	800 W	100 W	1.5 mTorr	50 sccm	0 sccm



(a) (b) (c)

Fig. 2.12. SEM micrographs of etched GaAs samples showing variations in surface morphology for different gases [9].

From the original recipe which has 15 sccm (standard cubic centimeters per minutes) of Ar gas and same amount of BCl_3 result in vertical side wall, the gas proportion is changed to mainly Ar gas and small portion of BCl_3 in the recipe 1, expecting angled sidewalls. However, the first recipe resulted in very rough surface and almost vertical sidewalls. Since the bottom substrate surface is not clearly etched out, pillar shapes are found in the middle of the substrate (Fig. 2.13a). In the recipe 2, the bias power was increased from the first recipe and results in a smoother surface (Fig. 2.13b). Although exactly the same recipe was run twice to etch deeper into the layers, the

upper step is smoother than the lower step, and the side-wall is highly vertical. The third sample used an existing GaAs etching recipe as a control group. Both the TCP power and bias power is much lower than previous recipes, but the chamber pressure was set lower which only helps to increase the plasma density. As a result, not only does the sidewall become very rough but so does the substrate surface (Fig. 2.13c). The etch rate is significantly lower than any other recipe because of the lower gas flow and the lower plasma energy. The fourth recipe focused on increasing the plasma density and the Ar gas flow was also increased. The result showed the best bevel angle of around 48°, but the sidewall and the surface is very rough (Fig. 2.13 d). For the fifth recipe, the bias power is increased from the fourth recipe to yield stronger ion bombardment that resulted in a smoother surface. The fifth sample has a bevel angle of around 12° which is less than the fourth recipe, but the smoothness of the surface is much better (Fig. 2.13e). In the sixth recipe, BCl_3 gas is removed and Ar gas is increased even further up to 50 sccm. As a result, the sidewall becomes rougher than sample 5, but the angle is increased to around 25°. The sidewall roughness and the bevel angle are inversely related and therefore must be traded-off. The higher the bias power (36 W vs 100 W normally), the smoother becomes the substrate surface (Recipe 1 vs 2, and Recipe 4 vs 5). From this study, we are able to draw the conclusion that dry-etched bevels can be achieved with lower chamber pressure and/or higher bias powers by increasing plasma density.

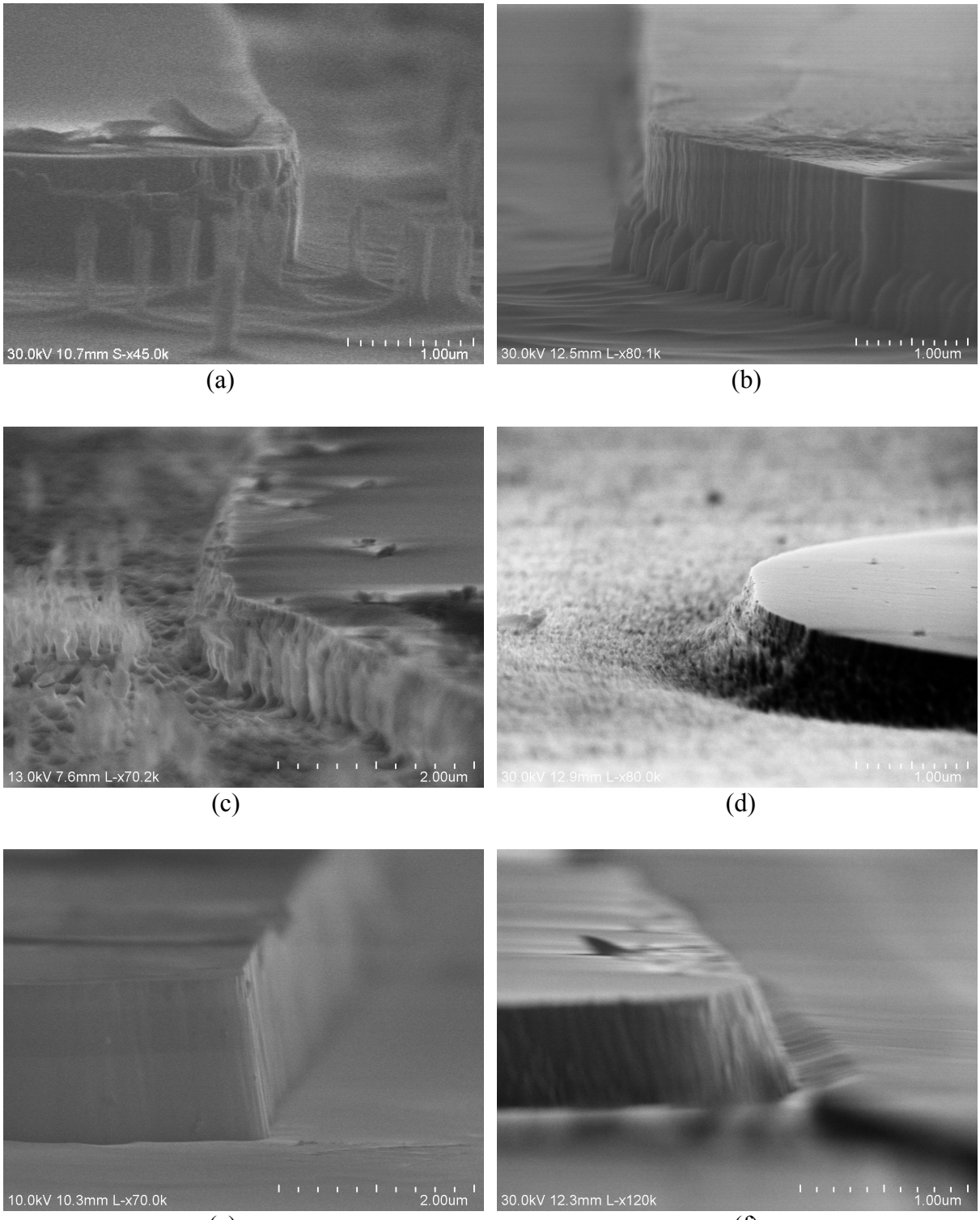
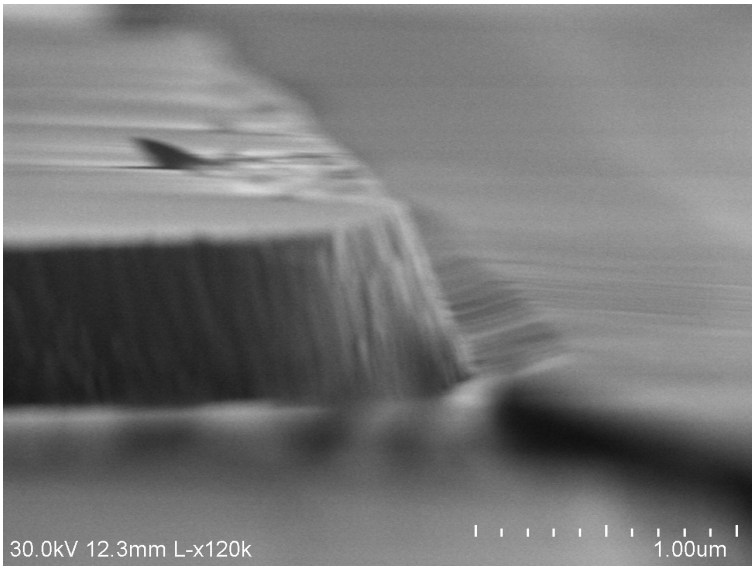


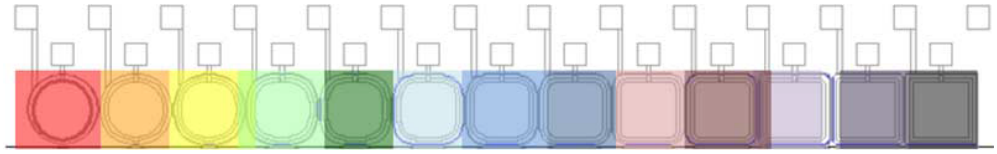
Fig. 2.13. SEM images of the samples from the recipes in Table 2.

2.6 IV characterization of design variations

After fabricating the structures, the IV curves are measured to quantify the diode characteristics, such as the saturation current and reverse bias breakdown voltage. The doping and layer thicknesses of the pn+ structure was designed such that breakdown occurs at low operating voltages (less than 40V) for ease of implementation with standard power supplies. In particular, the pn+ diodes breakdown below 30V, as shown in Fig. 2.14, in which the variation in the reverse bias current-voltage (IV) characteristic is compared for various corner shape. For all of the IV curves shown in figures, an external 220 kΩ series resistance is included which governs the saturated current value above breakdown.



(a)



(b)

Fig. 2.14. IV characteristic as the diode shape is varied, as coded with the shades shown in (a), where the corner radius varies from 120 μm (the round element) on the left, to the square element on the right, but steps of 10 μm.

For array implementations, one would prefer a photodiode shape that is conducive to close-packed geometries, such as square or hexagons, rather than the circles that are commonly found in avalanche photodiodes. As shown in Fig. 2.14a, diodes with curvatures varying between fully circular and fully square were studied, and no substantial difference in either dark count response or the IV characteristic were observed, the latter reflected in Fig. 2.14b, in which the diode-to-diode process variation exceeds any effect due to geometric changes. In particular, the breakdown voltage and dark current of the square diodes, which can be affected by edge or corner effects that would compromise the device performance, were comparable to those of the round diodes. Thus, the electrical performance is preserved for high fill factor (FF) diode geometries.

One would also prefer high FF contact geometries, in which small contact areas replace the border contacts used in the Fig. 2.14 devices. As indicated in Fig. 2.15, finger contact devices—in which only the tip must be opaque—produce equivalent IV characteristic to those measured using border contacts.

The IV variations thus indicate that $Al_{0.8}Ga_{0.2}As$ diodes conducive to SSPM implementations are realizable. The curves also reveal that the operational range of the processed diodes is narrow compared with silicon APDs as the current rises to saturation within a volt of its onset, even in the presence of various quench resistors. The Geiger-region of a silicon Geiger Photodiode (GPD: avalanche photodiodes working in Geiger mode) has a voltage range that typically extends 10% - 20% beyond the breakdown voltage. For instance, the silicon APDs

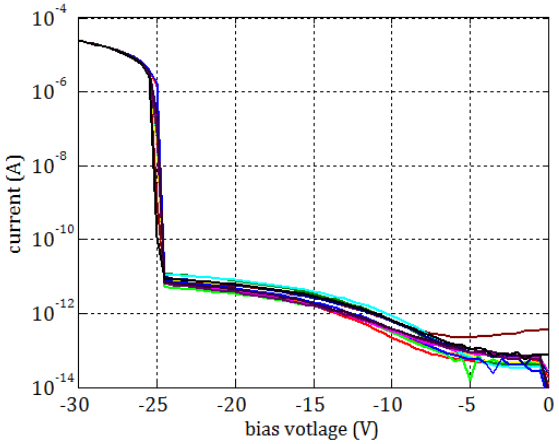


Fig. 2.15. Four finger-contact diodes of side length 240 μm, the IV characteristics for various corner curvatures.

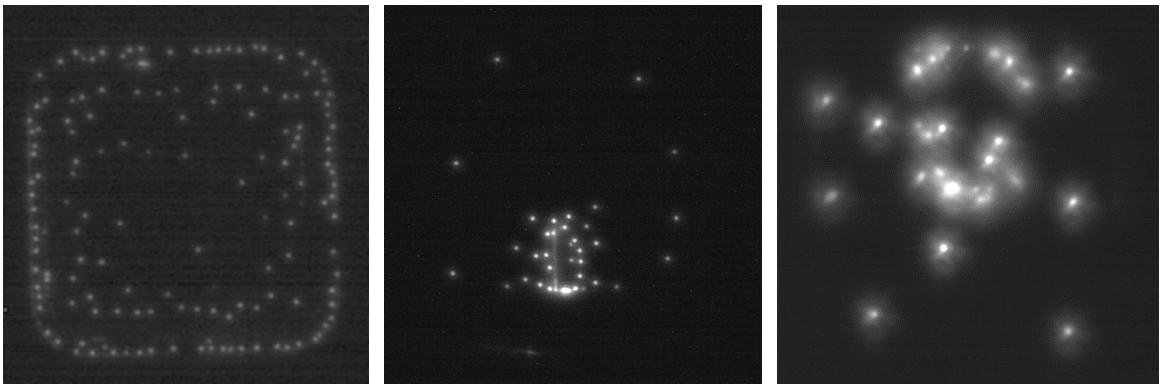
fabricated in [11] have a breakdown voltage of 31 V and effective operational range up to 38 V reverse bias before the quenching mechanism becomes less effective and the dark count rate quickly rises to saturation.

Ideally, one world prefer a wider operational voltage range and a more deliberate rise in the post-breakdown current so that power-supply voltage fluctuations and fabrication-induced variations in the breakdown voltage from pixel-to-pixel do not result in a large variance in the dark count rate (DCR) across the SSPM array. In practice, if a small subset of pixels does dominate the DCR, then they can be disconnected from the grid at the cost of FF or one can conceivably employ control circuitry to compensate for variations in the onset of breakdown.

2.7 Electroluminescence Experiments

Charges flowing through the device structure can result in carrier excitation and subsequent relaxation, which, at high currents, yields an observable photon flux. Those regions with higher current concentrations will be more emissive, and they can therefore serve as an indication of non-uniformity in the device, either due to E-field non-uniformities of thickness variations, for instance. The goal is to have a uniform electric field across the face of the diode with no premature edge, corner, or contact breakdown, which manifests itself as a uniform glow across the area of the structure. Unfortunately, we don't see that, but instead have indications that point defects result in high E-field regions. For instance, in the electroluminescence (EL) image in Fig. 2.16a, the expected electric field is more concentrated near the border contact, and this is indicated in by a higher density of point defects; however, one would prefer that the glow be uniform about the contact.

Note that the PIN results indicate that even if the edge fields are dropped below that formed in the central region, then the point-defect structure will remain, as indicated in EL images derived from finger contacts (Fig. 2.16b). For instance, Fig. 2.16b and 16c show that the distribution of high-current regions is greatest nearest the higher field about the contact, and not governed by an edge effect. In general however, the field density is highest near the edges.



(a) (b) (c)

Fig. 2.16. Electroluminescent images for diodes from El-Cat pin AlGaAs.

Some of the El-Cat pn+ results show this point-defect structure (as in Fig. 2.17); however, there are many diodes for which the edge does glow bright, which may be edge breakdown, although the breakdown voltage doesn't vary substantially for various edge conditions, based on the IV curves. We expect the ionization integral region to be well-buried and the hot-carrier photonic emissions will not penetrate the top layers to make it to the camera in as great of an

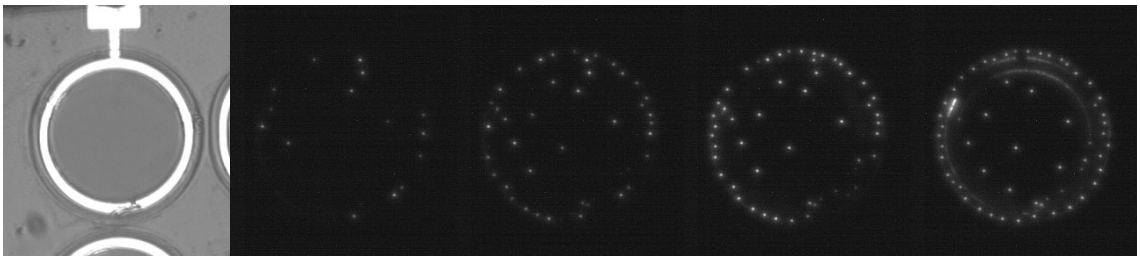


Fig. 2.17. LandMark PIN diode shows spotted illumination concentrated more around electrode. The bright spot appears after breakdown and the number of spots increases by applying higher voltage. The bright spots seem to be defect-induced electric field concentration.

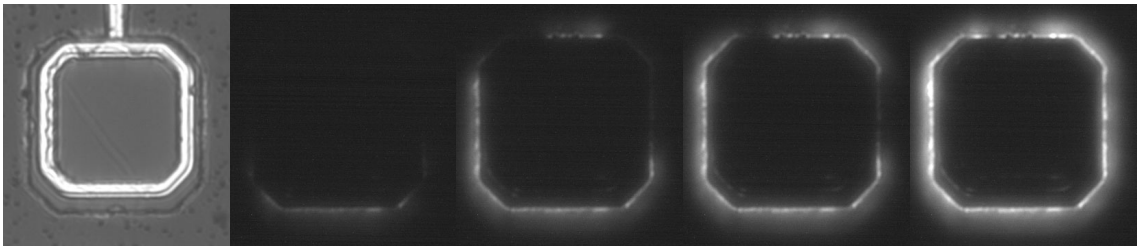


Fig. 2.18. El-Cat PN+ diode shows glowing edge of diodes. This could be corner breakdown due to edge effect.

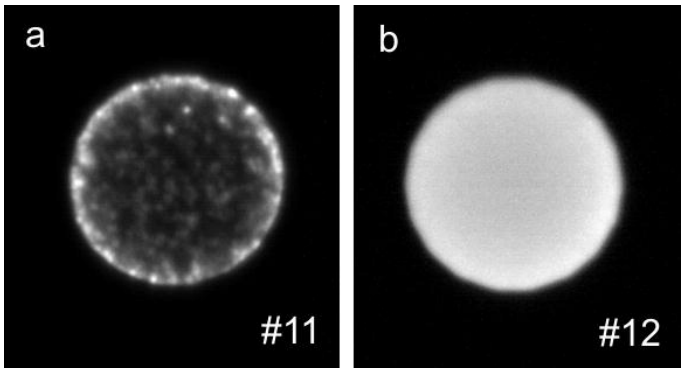


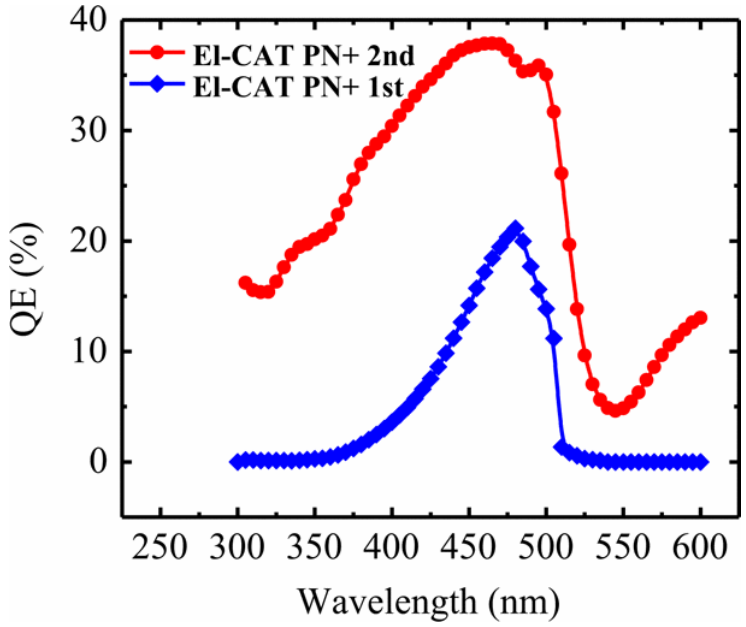
Fig. 2.19. For prime silicon (1-10 Ωcm), gettering lowers the leakage current and makes the current-distribution far more uniform.

intensity as the exposed junction; however, one can see that the inner edge of the border contact glows prior to the interior and E-field non-uniformities are evident.

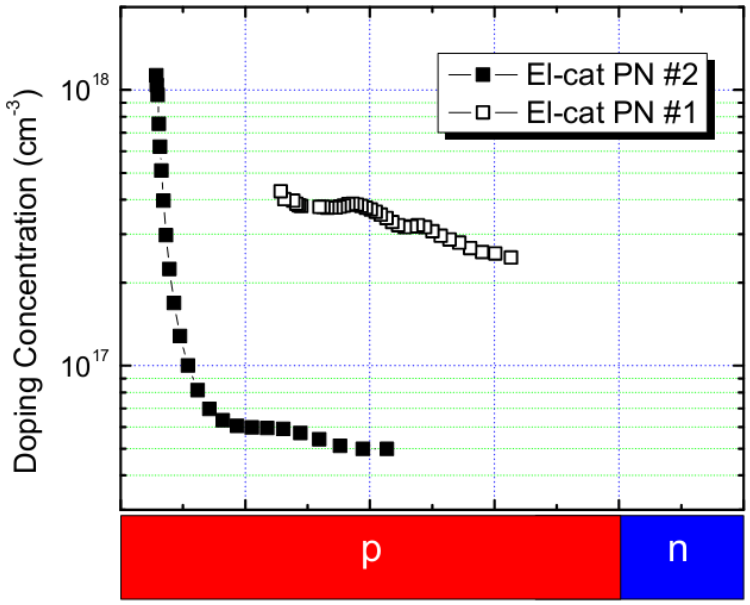
The spotted EL images do explain the DCR variation with area, as well as the lack of a similar photonic response. It may also help explain why dry etching BCl_3 produces lower leakage than wet-etchants. In fact, if the material has an unacceptably high defect density inherent to the epitaxy, then gettering may be the breakthrough. From P. Barton's study [57], a non-uniform spatial distribution was seen in GPD elements derived from silicon, as shown in Fig. 2.19, and gettering can perhaps improve matters in a similar fashion in AlGaAs.

2.8 Quantum Efficiency Measurement

The high defect density can therefore impact the rapidness of the growth of the breakdown and the uniformity of the electrical field across the diode. One would also expect that the defects would provide sites into which photocarriers can trap and therefore reduce the quantum efficiency. The following therefore represents an external quantum efficiency measurement for the diodes comprised fully of AlGaAs, without the front-side window layer, which is designed to bury the junction away from the surface. Specifically, the efficiency measurements were taken for AlGaAs pn-junction EC 4 (vendor El-Cat, design 4) and EC 6 as shown in Table 1.



(a)



(b)

Fig. 2.20. (a) Quantum efficiency as a function of wavelength for two AlGaAs pn+ photodiode structures fabricated from two different epi-wafers. The top curve shows the results from the newer batch of wafers. The significant difference between the optical responses are due to doping concentration difference for the AlGaAs epi-layers. Both are reverse biased to -5 V. (b) For two different epitaxial pn+ diodes, the doping concentration as measured via the CV curve.

The performance of the fabricated structures as photodiodes are characterized by measuring the quantum efficiency as a function of wavelength. Quantum Efficiency (QE) measurements were performed on the pn+ structure at the University of Virginia. A Stanford Research SR-850 lock-in amplifier, a monochromator, an optical signal chopper, and a 1 kW Xenon lamp UV light source were used to measure QE. Specifically, the UV was filtered through the monochromator and subsequently chopped and focused onto the structures using an optical fiber. The incident power on the device is calibrated using a silicon detector from UDT Sensors Inc. The photocurrent is measured and compared to the calibrated result and the QE is then extracted from the 300 - 600 nm range.

Plotted in Fig. 2.20a is the QE response of the two pn+ structures. The two curves shown in the figure were derived from two different epi-wafers, the lower curve measured from an earlier iteration in the pn+ design. One should note that there are no QE enhancement treatments- such as anti-reflective coating, surface diffusion or texturing- done on these structures. The improvement in QE response for the newer structure suggests that there are variations in AlGaAs epi-layer doping concentrations, which was confirmed by capacitance voltage measurements, as shown in Fig. 2.20b, which shows that the doping concentration in the p-AlGaAs layer in the newer structure is lower, which resulted in a larger charge collection region in the device active area.

The QE results presented here show good optical sensitivity in the blue and shallow UV region without any optical enhancements. This is critical in achieving high detection efficiency for optical readout of emerging scintillation materials.

The QE in Fig. 2.20a is superior to the typical QE's of PMTs, which is promising particularly since no anti-reflection coating was included which typically increases the QE by 10 – 15 %. We wished to see if we can retain that QE or increase its value while burying the junction deeper within the bulk of the epitaxy, as a means to reduce the defect-induced noise upon biases to breakdown voltages. Thus, the AlAs window/AlGaAs junction structures of Fig. 2.2 is fabricated and tested.

Radiation Monitoring Device (RMD) Inc., one of our collaborators, acquired a high intensity, broad spectrum light source, the LDLS EQ-99 from Energetiq. The EQ-99 is a laser-driven source that produces an almost flat spectral radiance response across UV-visible spectrum (200 nm to 800 nm). The light power is at least an order of magnitude larger than the halogen lamp

for UV light below 400 nm. The first measurement is executed after calibrating and finalizing the setup of the light source with their monochromator connected to a computer to scan the wavelength and measure current. The result for the first-generation design for a wafer grown by Landmark, with SIMS profile shown in Fig. 2.8a, is shown in Fig. 2.21.

Although the design simulations predict a QE of ~100 %, even at 0 V bias, the measured results peak at roughly 25 %. The difference of the two curves (blue and green) is a slight variation in the bias. One should note that there are no QE enhancement treatments—such as an anti-reflective coating, surface diffusion or texturing—included on these structures.

One possible mechanism that lowers the efficiency is the uneven window area surface. When the window area is etched, citric acid is used for selective etching of GaAs over AlAs. However, after the etching, the window area showed uneven surface due to the undesired graded layer as explained in Chapter 2.4 and unexpected Al_2O_3 formation from the oxidation of Al. Even though a uniform layer of Al_2O_3 does not affect the optical penetration into the underlying layers, the issue lies with the non-uniform formation of native Al_2O_3 at the surface that causes surface roughness, which can scatter the light and deteriorate the light absorption. Non-uniform Al_2O_3

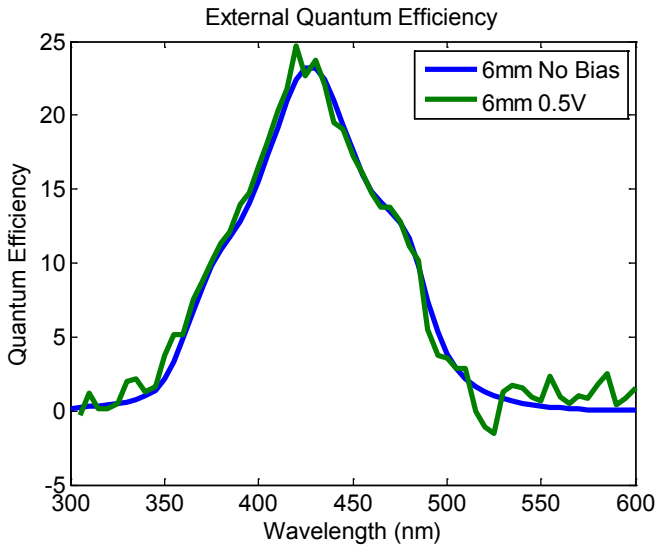


Fig. 2.21. Plot of the quantum efficiency from a 6 mm diameter diode, which consists of 200 nm of low doped p-type AlGaAs. The blue curve is measured without bias voltage on the device and the green curve is with 0.5 V reverse bias voltage. Note that the small difference between with bias and no bias is because the 0.5 V reverse bias is not enough to trigger the avalanche breakdown.

formation at the AlAs surface is a likely detriment to achieving higher QE. To further improve the QE, the window area etching scheme is changed to plasma etching which does not have selectivity but the etch rate can be carefully controlled; thus, the graded AlAs and the non-uniform Al_2O_3 can be eliminated at a same time.

Our quantum efficiency measurement set up consists of a Cary 5000 UV-VIS-NIR spectrophotometer as a light source and Keithley picoammeter for the photo-current measurement. In order to measure the intensity of the light source, a calibrated Si photodiode is used as control, which has active area of 13 mm^2 and wavelength response range of 350 – 1100 nm, as illustrated in Fig. 2.22. Test diodes are designed in a circular shape with 3 and 4 mm diameters, with recessed window radii of 0.95 and 1.5 m,m respectively as shown in Fig. 2.23.

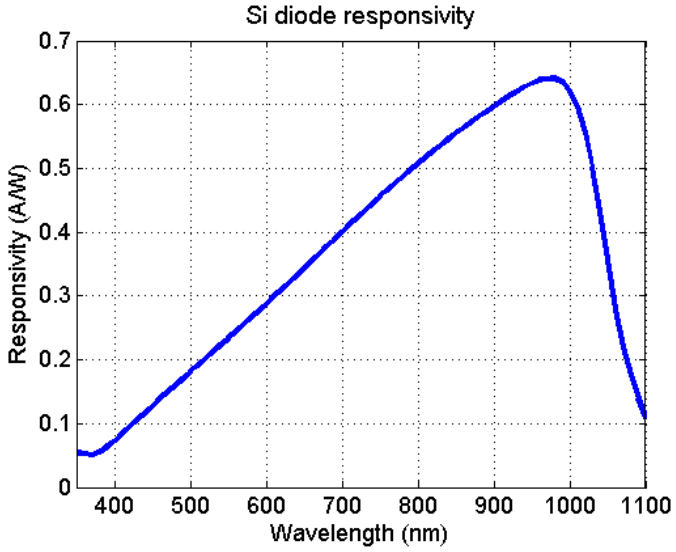


Fig. 2.22. Responsivity of a calibrated Si diode in 350 – 1100 nm range.

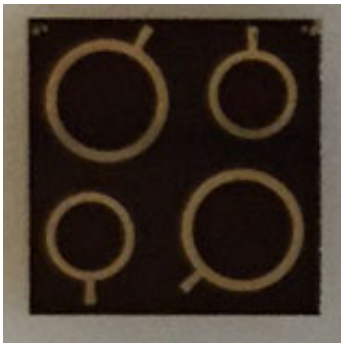


Fig. 2.23. Diodes for the quantum efficiency measurement. The metal part protruding from the circle is the pad for the device probing.

As we have seen from the simulation in Fig. 2.6, the quantum efficiency is increased with higher bias but such a saturation effect is not observed. Fig. 2.24 shows the quantum efficiency plot measured from a wet-etched window diode which has an uneven surface at the window area, as explained above.

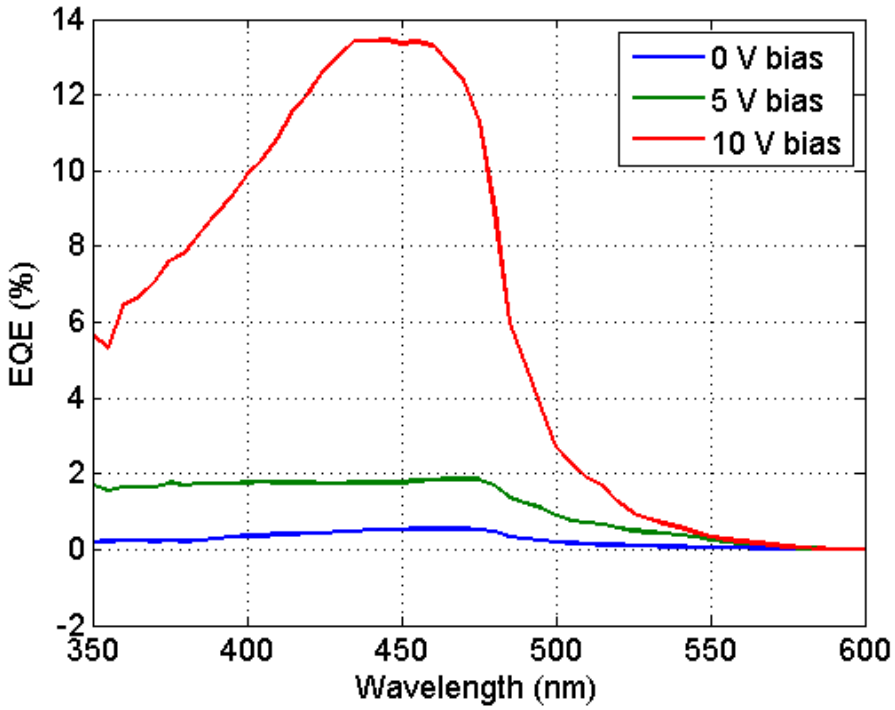


Fig. 2.24. Plot of the external quantum efficiency measured from the diode with a wet etched window. With the wet etching, the rough surface restrains the high EQE

The maximum quantum efficiency is around 13 % in the case in which only the top-layer of GaAs is removed, but the entire AlAs window and graded layers are retained. However, if the window area is recessed 32 nm into the AlAs transition layers via dry etching, the maximum quantum efficiency is increased up to 50 % as illustrated in Fig. 2.25. Compared with the simulation result, the peak location shifts only slight toward shorter wavelength (from ~470 nm at 2.5 V to ~450 nm at 10 V), but it doesn't show the obvious shift to 380 nm shown in Fig. 2.6. This lack of a shift implies that the shorter wavelength photons are not participating as strongly in the experimental QE measurements as in the simulation. We hypothesized that the carrier lifetime in the AlAs is shorter than that value assumed in the Sentaurus simulations, the effect of which is that

the diffusion from near-surface absorption into the depletion region is substantially reduced in the real device. This hypothesis is confirmed because when the carrier lifetime was reduced from the default 1 microsecond to 20 ns, an experimental value for the lifetime, the QE plots showed roughly the same shape as that shown in Fig. 2.25.

From the simulation, we can also observe that the quantum efficiency saturates once the device is fully depleted (at around 7 V bias); however, the measured device is not saturated at 7 V but rather quickly increases from 5 – 10 V and saturates at ~15 V. Since some of the diodes can't withstand the high bias voltage and broke-down in some cases, the bias voltage is carefully increased and limited by 10 V in most cases.

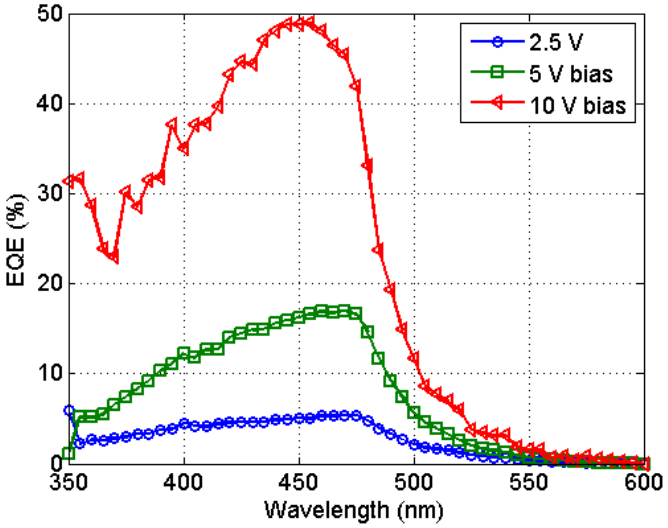


Fig. 2.25. Plot of external quantum efficiency measured from the diode with a dry etched window which can eliminate the deterrent to make a clean and uniform surface.

In order to confirm the saturation effect, we found one which is more stable at the higher bias voltage and tested up to 15 V bias as depicted in Fig. 2.26. The incremental increase in the QE from 0 and 5 V is much smaller than that rapid rise from 5 to 12 V, which implies that the quantum efficiency is significantly affected by the depletion region inside the diode. The maximum EQE increase rate gradually declines above 12 V. Specifically, the percentage increase from 10 to 12 V is 6.8 % while the variation from 13 to 15 V is 3.4 %, indicating that the depletion region growth diminishes.

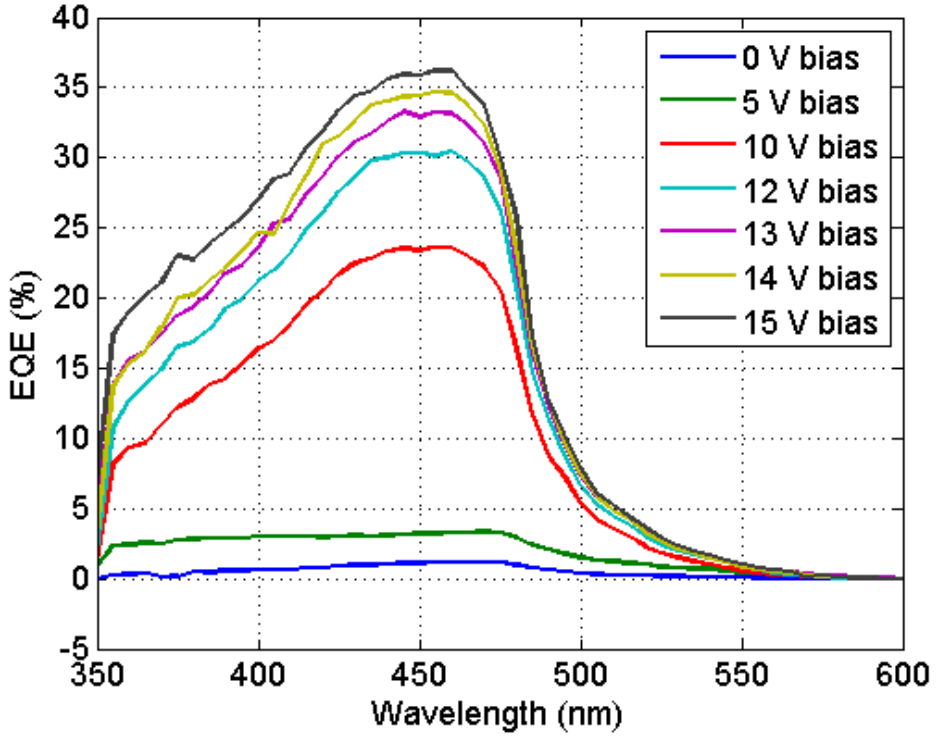


Fig. 2.26. Plot of external quantum efficiency in various bias voltage.

Although the anti-reflective coating targeted a minimum reflection at 390 nm wavelength as shown in Fig. 2.7, the measured results show the maximum peak is located at ~ 450 nm. Since the reflectivity is highly sensitive to the thickness of the anti-reflective coating layer, we measured the reflectivity from the fabricated devices to verify that the thickness of the layer is fabricated as we designed. As indicated in Fig. 2.27, the measured reflectivity data matches with the simulated higher data (cf. Fig. 2.7). Although the minimum reflection point at approximately 420 nm is than from the simulation (390 nm), the entire reflectivity remains less than 20 % at the range of 375 – 450 nm. We can confirm that the anti-reflective coating is fabricated as designed and worked as expected from the simulation. In consideration of the reflectivity at the quantum efficiency peak location, 450 nm, the maximum quantum efficiency can be increased by 10 % - 20 % if the anti-reflective coating thickness is increased to match the optimum responsivity wavelength, resulting

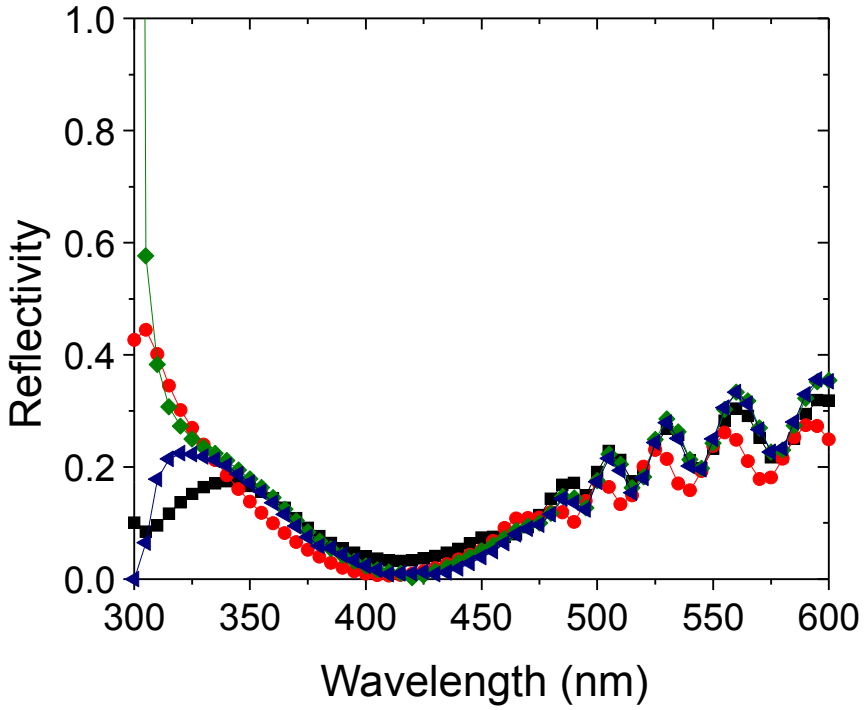
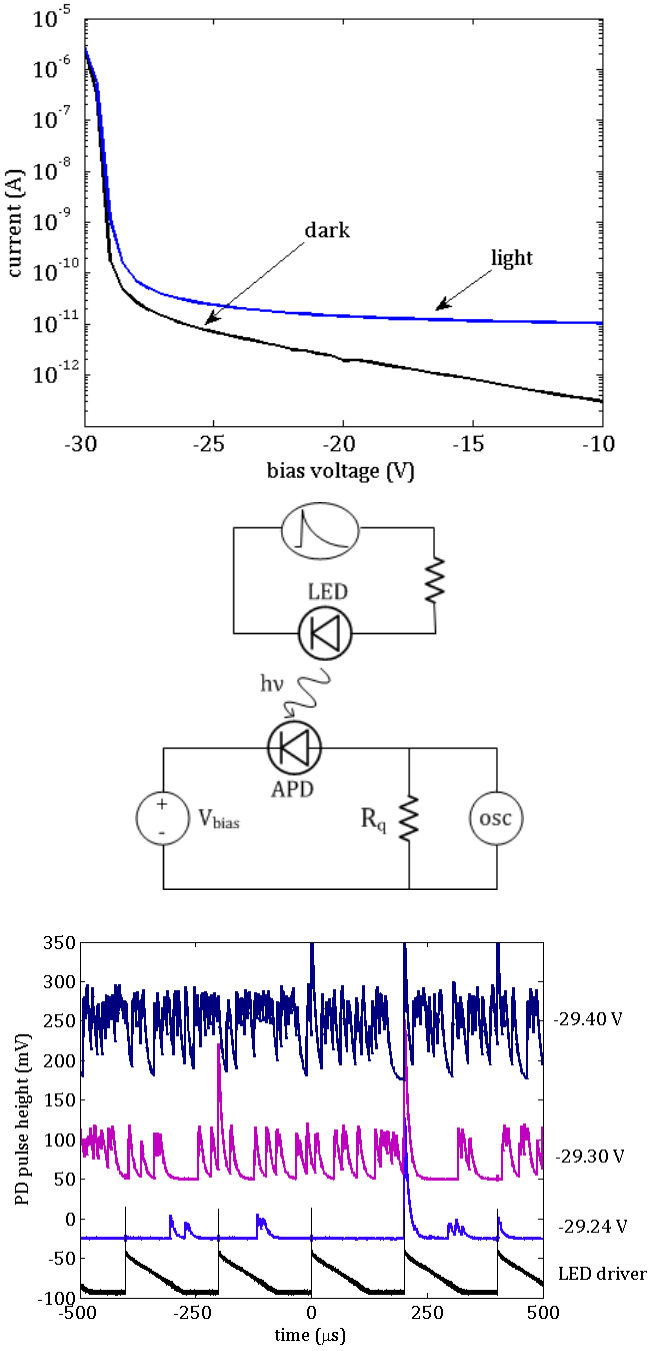


Fig. 2.27. Reflectivity measured from the photodiode with a 40 nm nitride anti-reflective coating.

in 60 – 70 % QE. We were therefore able to achieve our aim of retaining a high QE, but only by the removal of some 75 % of the AlAs window thickness.

2.9 Breakdown Pulse Formation

Finally, we examine the operation of the device near and above the reverse-bias breakdown voltage, that is, in Geiger-mode as a Geiger photodiode. The characterization of the dark and light Geiger pulses is discussed next. Consider a pn+ square GPD with 60-μm-wide sides with a breakdown at -28.5 V, as shown in Fig. 2.28a. Dark pulses, passively quenched with an external 50 kΩ resistor, initiate at -29.18 V and grow in size and frequency until they overlap and become indistinguishable at -29.45 V, as shown in Fig. 2.28c.



(a)

(b)

(c)

Fig. 2.28. (a) IV characteristics for 5:1 pn+ diode passivated with TOP:S and PECVD nitride. (b) Schematic of experimental setup, in which the LED and APD are separated by 2 cm, and the LED light is directed parallel to the diode (90 ^{0} from direct incidence). (c) Transimpedance (G = 1 MV/A) photodiode pulse heights, offset for clarity, for blue (λ_{peak} = 465 nm) light. The bottom LED-driver trace, which has a peak amplitude of 9V, is overlaid for timing comparisons.

Geiger pulses can also be photon-induced, their frequency increasing as the intensity of the light increases. As shown in Fig. 2.28, the (blue LED) light-induced pulse formation is stochastic and the temporal characteristics (rise time and fall time) are consistent with the dark counts, although the pulse height is larger. This variation between dark and light pulse heights can also be observed in silicon GPDs, but we have not yet studied the underlying source of the difference in detail. Note that the scale for the LED driver is different from the photodiode (PD) response curves and the light is emitted during the narrow pulse at the onset of the tail pulse.

As discussed toward the end of Chapter 2.6, one would prefer that the pulse evolution shown in Fig. 2.28c occurs over a wider voltage range, so that the GPD's behavior in array designs would be highly robust to slight variations in the process conditions across the wafer. Furthermore, if the wide band-gap of AlGaAs is to be optimally used to suppress the dark count rate, then the deleterious effects of active interband states that accompany defects must be mitigated. One method to sequester defects in inactive regions is through gettering, which is the process by which on diffuses unwanted impurities away from the active area. We investigated whether the introduction of backside damage to the GaAs substrate, and the subsequent annealing of the device can suppress the noise. For the introduction of damage, we used 30 μm lapping paper on the backside of the device to introduce a high dislocation density within a few micrometers of the GaAs surface. We do not expect that the backside damage to the conductive substrate should substantially degrade the diode's leakage current, the magnitude of which is governed by front-side surface leakage. This expectation realized with comparison between the pre-breakdown leakage current for before and after damage.

As shown in Fig. 2.29, furnace annealing of an intentionally damaged pn+ 480 μm square structure at 500 °C in forming gas (5% H_2) results in stability of the onset of breakdown, and most notably, the leakage current is substantially diminished by the annealing process.

The annealed devices exhibit greater dark-pulse height variation than the non-annealed devices of Fig. 2.29, and the junction gain, as measured in the dark pulse height is diminished by over an order of magnitude, both indicating that the anneal impacted the junction geometry (cf. Fig. 2.30). Furthermore, a comparison of Fig. 2.29 and Fig. 2.30 shows that the pulse-height distribution exhibits greater variance upon annealing, an effect we attribute to the non-uniform diffusion of the dopants across the lateral junction.

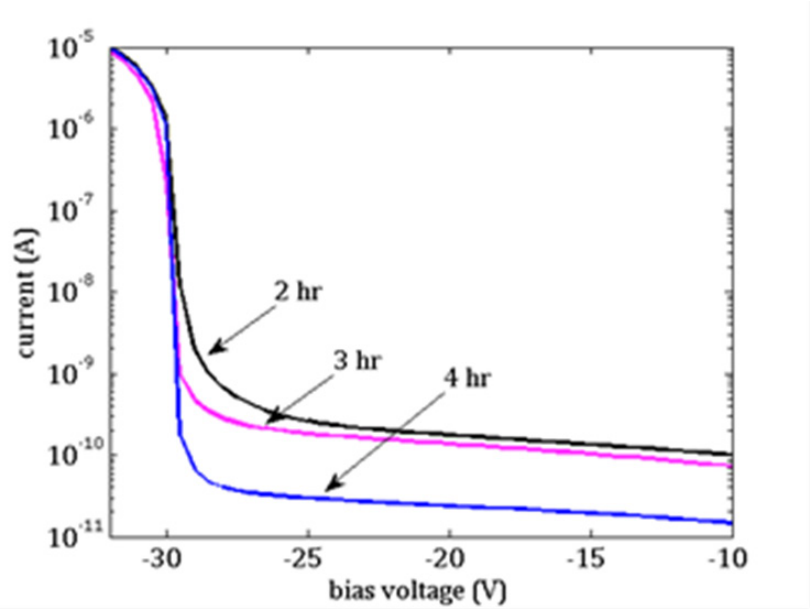


Fig. 2.29. For the pn+ diode design, which is damaged and annealed in forming gas at 500 °C, the IV curve variation as the annealing time (2, 3, 4 hr) is varied.

As qualitatively shown in Fig. 2.30, the APDs nevertheless exhibit similar optical sensitivity, with a response scaling with the LED's optical fluences—the strongest response to UV (λ_{peak} = 402 nm) and blue light and increasingly weak response to green (λ_{peak} = 570 nm) and yellow photons, successively, the direct-UV and direct-green comparison are made in the top two traces of Fig. 2.30, noting that the LED pulse is also accompanied by a sharp RF coupling glitch pulse, whose appearance doesn't change even as the diode bias is varied.

The middle three traces of Fig. 2.30 show that as the intensity of the UV light is diminished, the light-induced pulses no longer occur for every light pulse, the timing for which is reflected in the bottom trace, the narrow tail pulse used to drive the LED. This is clearly seen in the UV 90 ° trace of Fig. 2.30. Rotating the LED away from direct incidence to a 90 ° orientation reduces the intensity of the light by a factor of 89 times, as measured by the pre-breakdown photocurrent. At 90 ° incidence, the average number of UV photons per pulse is 1.62. Given the frequency of GPD triggering (20%) and that the QE at 405 nm is 50% if an simple quarter-wavelength dielectric anti-reflection coating is added as was true for these measurements, this implies that the Geiger discharge probability at a slight ~ 1% excess bias for a single photon is approximately 6%, a

number which scales up at higher applied bias. Avalanche pulses can thus be induced with blue and near-UV wavelength optical pulses relevant to scintillator light emission.

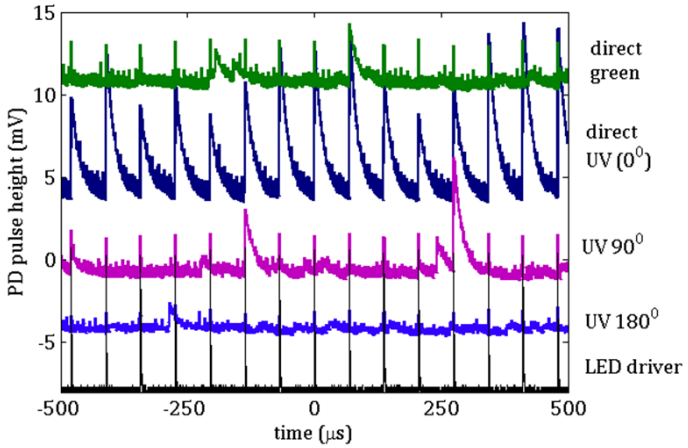


Fig. 2.30. For the pn+ diode design, which is damaged and annealed in forming gas at 500 °C, the transim-pedance (G = 1 MV/A) pulse heights, offset for clarigy, of the diode current for green (λpeak = 570 nm) and UV (λpeak = 402 nm) LED light incident upon the diode. The UV 90° PD trace is measured when the diode is rotated 90° from direct incidence and the UV 80° trace is for light directed away from the sensor. The LED driver, a BH-1 tail pulse generator (rise time = 0.02 μs, fall time = 1μs) has a peak amplitude of 9 V. The APD has a bias voltage of -29.26 V.

Chapter 3. Suppression of Interface-Induced Noise

3.1 Introduction

In order to effectively interdict nuclear and radiological materials that may be secreted and shielded, existing radiation detector materials are inadequate because of either: (a) low efficiency, (b) moderate energy resolution, (c) high unit cost, or (d) ineffective signal generation. A substantial amount of research and development effort is required to develop a high-performance semiconductor substrate from new materials, but the performance as delivered after crystal growth or colloidal synthesis can be compromised during the formation of the contact because of the material's exposure to chemical, mechanical, and thermal load during processing. Furthermore, effective surface control beyond the contact is needed if the favorable radiation-detection properties of the bulk properties are to be preserved.

Although thermal and shot noise both contribute to the current fluctuation in semiconductor sensors, for many wide band-gap detectors, the $1/f^{\alpha}$ noise can dominate the total noise [2], [3]. In noise research, in which agreement between theory and experiment is common, the microscopic origin of 1/f noise is, surprisingly, still debated even though it has been studied for over 80 years, in which the main point of dispute is whether the 1/f spectrum is due to fluctuations in the carrier number or the mobility. In 1937, Bernamont showed that a 1/f spectrum can be obtained from a superposition of Lorentzian distributions [12], which in turn, requires the existence of a distribution of relaxation times ($D(\tau) \sim 1/\tau$) [13]. The generality of the underlying mathematics explains the presence of 1/f noise in many natural systems, including geological, physiological, and musical phenomena [14].

For condensed matter and for semiconductors in particular, McWhorter initially proposed a microscopic model in which the noise was attributed to the tunneling of carriers into surface (oxide-induced) states, and therefore amounted to a charge-number fluctuation model in which the contribution of the surface was paramount [15]. The generation-recombination (g-r) mechanism for the production of 1/f noise is the main framework still used today to try to reduce the semiconductor noise, in which the avoidance of near-surface and bulk traps is the goal of the device engineer. For instance, Farmakis *et al*. used an interface generation-recombination model to extract

the surface state density from noise spectra at the interface of a TiN_x / n-Si Schottky diode [16]. Furthermore, the data indicated that models based on mobility and diffusivity fluctuations within the space-charge region or to the spatial fluctuations of the Schottky barrier height were inappropriate, and the interface trap density was shown to decrease as the internal stress decreased [16]. As another example, Ouacha *et al*. used an interface state density noise model to discern that the formation of a Pt silicide at the interface to a p-type $Si_{1-x}Ge_x$ substrate reduced the noise relative to that formed via metallic Pt contact alone [17].

The trap density model can be useful in not only providing phenomenological guidance in understanding the current densities derived from the devices, but it can be used to make the connection between the process steps used in the device fabrication and the noise properties observed during operation. Nevertheless, the model cannot be used to effectively describe the noise in metals and more pertinently, it fails to account for variations between devices that have undergone nominally identical processing.

There have been many attempts to explain the variations of 1/f noise behavior and its level, particularly as observed during experimental studies which use the same materials and similar devices. In particular, the Hooge parameter temperature behavior depends on many parameters, such as the concentration and distribution of impurities, bulk and surface structural defects, lattice mismatches, surface conditions, and phonons relaxation times, and there exist many models attempting to describe the mechanisms of those dependences [18]. However, the absence of a uniform theory fully describing the mechanism of the origin of 1/f noise despite the multitudinous experimental data has resulted in a reconsideration of the theoretical approaches, For instance, in [19]–[21] the influence of the electron-phonon interactions on the level of the $1/f^{\alpha}$ noise, resulting in the roaming phonon microgradient model (RPMG), has implied that if one can regulate the surface temperature and interface phonon exchange, then the semiconductor may experience far lower 1/f noise. In this chapter, we test the hypothesis that one can use the geometric and material design of the interface to a solid to suppress the phonon distribution and concomitantly, the electron distribution via phonon-phonon and phonon-electron scattering, as a means to substantially reduce the noise in semiconductor-based devices.

3.2 Background

3.2.1 Evidence of Phonon-Based 1/f Noise

The participation of lattice vibrations in the generation of 1/f noise has been recognized for some time (cf. [22]), but the precise manner in which the phonon population participates in the fluctuation in the electron mobility remains an open research question. Nevertheless, several empirical reports have shown that both bulk and surface phonons participate in the generation of 1/f noise and in fact, the current noise from a device can potentially be used to probe the underlying lattice vibrational modes of the sample [23].

Recall that the noise parameter, γ, is defined by Hooge's formula [18]:

$$\frac{S_v(f)N}{V^2} = \frac{\gamma}{f^\alpha} \qquad (1)$$

Where N is the total number of free charge carriers, f is the frequency, α is an empirical constant, V is the voltage, and S_v is the power spectral density of the voltage fluctuations. In low-dimensional systems, for which the participation of phonon collisions can be quenched, the noise parameter, γ, can be made quite large. For instance, γ values on the order of 10^{-8} were found by Schmidt *et al*. [24] in near ballistic n+nn+ GaAs submicrometer diodes. More direct evidence of the participation of phonons has been found in the fine structure of the noise as various experimental parameters are varied. In particular, in [25] Mihaila showed that the peaks in the statistical distribution of γ versus base current for a batch of bipolar transistors corresponded to the phonon energies in silicon.

For metals as well as semiconductors, the mobility fluctuation 1/f noise parameter exhibits inflection points and peaks which correspond to fundamental vibration modes or to two-phonon and even three-phonon combinations. For instance, in [26], the authors map the dependence of the noise parameter on temperature for an 80 nm Cu film on a sapphire substrate, in which the kinks and peaks in the mapping are directly correlated with particular phonon modes, as confirmed with neutron inelastic scattering.

Once the phonon-mechanism is recognized, then the behavior of the noise in other systems can be explicated. For instance, in n-type silicon, it was found that the noise parameter exhibited a clear maximum at 210 K, for which the corresponding energy (18.1 meV) can be correlated to the energy of TA mode phonons (18.3 meV) in silicon [27]. In [28], in which the noise spectral density from an 8 nm platinum film was studies as a function of temperature, the data revealed a fine structure with features corresponding to surface phonon energies, with values verified using inelastic scattering techniques, results indicating that a phonon-assisted mechanism is involved in the 1/f noise generation in discontinuous metal films, which is relevant to radiation detectors with pixelated or strip-line electrodes.

The empirical data therefore suggests that the microscopic source of $1/f^{\alpha}$ noise is carrier-phonon interactions, whether sourced at the surface or in the bulk, and if one relates the size of the noise density to the phonon density of states, then large 1/f noise is expected in materials with strong electron-phonon coupling. One of the aims of this work is to experimentally verify this supposition and to provide guidance by which the electron distribution can be quenched via proper control of the phonon population.

3.2.2 Quenching of Charge-Mobility Fluctuations via Surface Control

The first step is to more fully develop the theories that have been proposed, in which the processes of reflection and refraction of both electrons and phonons from the near-surface are used to relax the longer-wavelength electron distribution. From the experimental data, one expects that the noise parameter to be related to the Eliashberg function, which characterizes the strength and spectrum of the electron-phonon coupling [29]. Furthermore, the random scattering between phonons results in fluctuations in the phononic energy and momentum distributions. For long-wave (acoustic) phonons, these stochastic perturbations can couple to the conduction electrons, which can, in turn, result in relaxation of the energy and momentum equilibrium states for different coupling conditions to the environment.

In [20], Melkonyan modeled an ideal semiconductor with mirror reflecting surfaces, in which the scattering processes were caused exclusively by phonon-phonon and electron-phonon scattering, and impurity and point defects mechanisms were ignored. The phonon modes that were

consistent with the boundary conditions and the phonon refraction laws were found, and the refraction points, which correspond to those phonons which permit energy relaxation to the surrounding environment, were quantified. The energy and momentum positions of those refraction points are strongly dependent on the phonon velocities and semiconductor dimensions, so areas with even minor changes in the phonon velocities—such as due to interdiffusion layers near the surface or doped regions—can serve as environments to which the phonon energy can couple.

This general picture suggests that by manipulation of the so-called phonon refraction points at the hetero-interface, the volume current fluctuations can be reduced by the relaxation of longer-wavelength electron distribution.

An initial attempt to consider different contacting media on the 1/f noise level in nondegenerate n-type silicon with aluminum (Al) and silver (Ag) contacts layers was presented in [30]. The experiment compared the difference between Ag and Al, showing that Ag contacts produced roughly four orders of magnitude lower 1/f noise, which was attributed to the phonon effect. This connection is difficult to make definitively because of material differences (work function, interface stress, etc.), but the second observation was that if one removed Ag from the surrounding area (thus lowering the area through which phonons could leak), then the noise increased by two orders of magnitude, an effect that is more difficult to dismiss. After all, one would expect the removal of Ag to increase the surface resistance and therefore reduce the noise, not increase it. The predicted effect therefore, was that the removal of a high phonon refracting material has a much more marked effect on the noise properties. We tested the materials and their geometries as explained in Chapter 3.3 and 3.4.

3.2.3 Evaluation of Acoustic Reflectance at Metal-Semiconductor Interface

The electron-phonon coupling model may therefore be an effective framework by which one can derive general solutions for quenching the noise across many different semiconductor systems. As mentioned above, one must also account for trap-based scattering, the precise mitigation of which is material specific; however, we have previously achieved some control over

those contributors to the noise in both silicon and CdZnTe and aim to quench the remaining noise by gaining a greater understanding of its fundamental character.

As a first step, one can derive the acoustic wave equations within the semiconductor and quantify the ease with which the phonons leak into various interfaces. As shown in (2), the reflection coefficient for longitudinal acoustic wave from a semiconductor (S) to a metal (M) depends on the densities (ρ) of the materials as well as their acoustic velocities (v) [31].

$$R = \frac{2}{\pi}\int_0^{2\pi}\left(\frac{\rho_M v_M cos\theta - \rho_S\sqrt{v_S^2 - v_M^2 sin^2\theta}}{\rho_M v_M cos\theta + \rho_S\sqrt{v_S^2 - v_M^2 sin^2\theta}}\right) \quad (2)$$

The reflectance coefficient plot for silicon is shown in Fig. 3.1. The RPMG model would suggest that a high degree of phonon communication, from both semiconductor-to-metal and metal-to-semiconductor [27], is conducive to the quenching of the elctron distribution, which implies that the reflectance should be as low as possible, or equivalently, the probability of phonon refraction (and transmission) is high. Thus, all else being equal, bounding materials with low R_{SM} should produce lower noise.

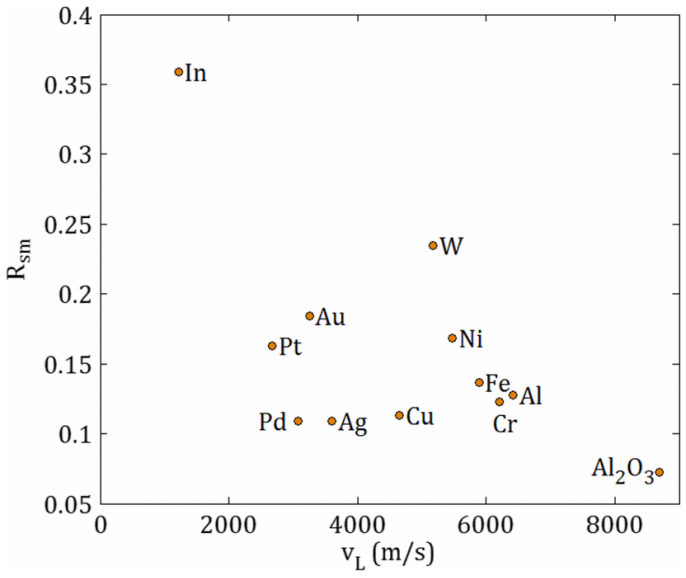


Fig. 3.1. Reflectance coefficient for various materials bounding silicon.

For instance, Pd and Au have roughly equal work functions (5.1 eV). The RPMG model predicts that the noise due to charge mobility fluctuations should be substantially less for Pd than for Au. Note that typically, one doesn't contact Au directly to silicon because of poor adhesion; instead, a thin layer of Cr is added to facilitate strong adhesion. Fortuitously, the Cr is also predicted to have high phonon leakage which may explain, in part, the excellent noise characteristics of Cr/Au contacts.

As outlined in [27] and detailed in the reference therein (cf. [21]), for those device designs and operating temperatures at which phonon boundary scattering is predicted to substantially contribute to the 1/f noise, optimizing the noise design must take into account more than the semiconductor-metal reflectance. In addition, the metal-semiconductor phonon communication and the geometry impact the degree to which the electron and acoustic phonon distribution functions are predicted to be quenched. Prior to this optimization however, our goal was to determine if a significant effect was present at all, as detailed in Chapter 3.3 and 3.4.

3.3 Detector Fabrication and Measurement Setup

3.3.1 Fabrication of the Silicon Detectors

We investigated many different material systems (Si Schottky-barrier detectors with gettering, Si pin detectors with or without gettering [32], [33], CdTe, AlGaAs photodiodes [34], nanocrystalline PbSe, CdTe [28] contacted by an array of different metals, but if one wishes to isolate the phonon effect, then one would prefer to avoid Schottky contacts because the diffusion barrier of the contact will dominate the noise properties. One can use Schottky devices for geometric studies, but in evaluating the differences between bounding metals, we buried the junction using a pin configuration, such as that shown in Fig. 3.2. There still exists a junction between the metal and the p+ layer, but the current is constrained by the diffusion barrier at the p+/n interface.

High resistivity (10 kohm-cm) 4" n-type phosphorus doped <100> Si wafer is used for the pin diode fabrication process. The first step is a poly Si deposition on the bottom layer as shown in Fig. 3.2b and phosphorus is diffused for 20 min and annealed for an hour. This process is one

of the most important processes in the Si pin diode fabrication. Annealing is not only used for the drive-in phosphorus but also for the gettering process. Impurities are diffused toward the bottom side of the wafer and trapped by grain boundaries of poly-Si. From the gettering process, the leakage current is suppressed by sequestering mobile impurities in an inactive region of the device. An oxide layer with a thickness of around 5000 Å is introduced on both the top and bottom of the wafer during the annealing process as indicated in Fig. 3.2c. Boron diffusion is used to make p+ a doped region on selectively defined diode area. Oxide windows are etched out in BHF (Buffered HF) solution after the photoresist (PR)) patterning. The remaining oxide layer works as a mask for the boron diffusion process. The boron diffusion process is executed under a temperature of 1000 °C for 45 min and a 10 min dilution time. The whole oxide layer is etched out after the boron diffusion process and another 5000 Å oxide layer is grown. The following step is to pattern the area for metallization, and deposit metal with E-beam evaporator. A lift-off process will remove all the deposited metal except the patterned area. The bottom metal deposition is the last fabrication process to measure the devices. However, the passivation layer is required for the prevention of device performance deterioration since the device leakage current increased as time goes on from the previously fabricated device. A passivation layer deposited from PECVD tool consists of 2000 Å of oxide layer and 3000 Å of nitride layer at 200 °C as depicted in Fig. 3.2f. We controlled the other sources of noise with optimized surface passivation and gettering recipes, the effectiveness of which is demonstrated in [32], [33]. The low surface-leakage detectors are fabricated which then serve as an effective platform to compare the effect of modifying the interface of the semiconductor to the environment.

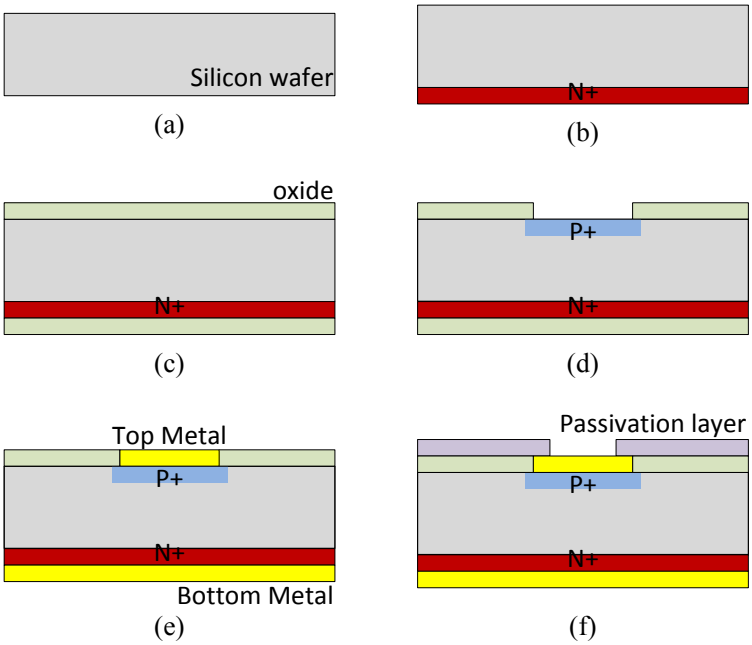


Fig. 3.2. Schematic of important aspects of the fabrication processes for the pin type Si detector.

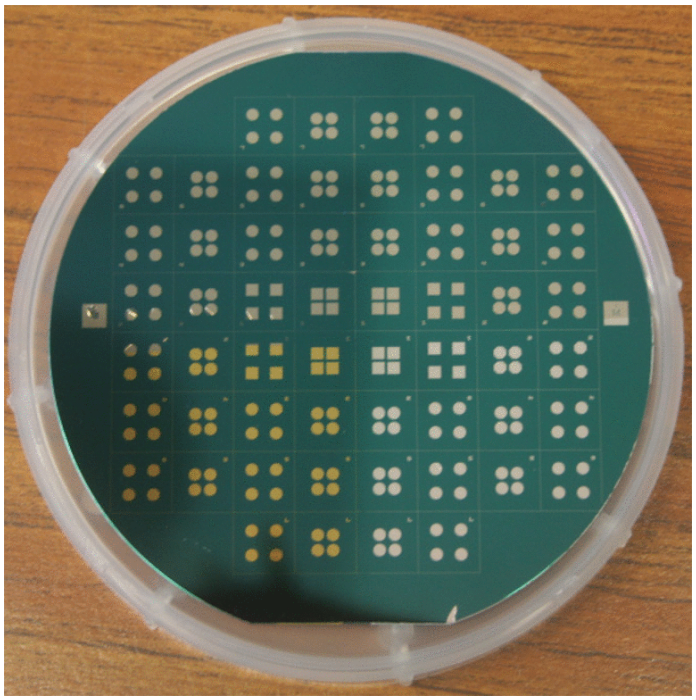


Fig. 3.3. Picture of the fabricated silicon pin-type radiation detectors for the 1/f noise measurements. The four quarters of the 4″ wafer are composed of contact of Au (lower left), Pd (upper left), Al (lower right) and Pt (upper right) on top side, and the botton n+ layer is contacted with Al.

One of the mask designs used in the testing is shown in Fig. 3.3. All diodes have 2 mm lateral extent (e.g. 2 × 2 mm^2 square diodes) and different shapes with corner angles of: 90° (4sides), 45° (8 sides), 30° (12 sides), 22.5° (16 sides), 19° (20 sides), 18° (24 sides) and circle. As a practical matter, the shapes are square, octagon, and 5 different degrees of circle. The sample die also have different gap sizes (2 mm and 0.5 mm gaps), in order to assess if the diode spread impacts the noise. The p+ contact is made with various metals, including gold (Au), palladium (Pd), aluminum (Al), and platinum (Pt). The back-side contact is made of aluminum to make an ohmic contact to the n+ layer.

3.3.2 Electronic Readout Chain

In Chapter 3.4, we compare the relative device noise through: (a) current-voltage (IV) curves, which integrate the current noise across all frequency bands, (b) the fast Fourier transform (FFT) of the signal output from the charge-sensitive preamplifier (eV-5903 from Endicott Interconnect Technologies, Inc.), and (c) the width of gamma-ray peaks derived from ^{133}Ba gamma-rays impinging upon the detectors.

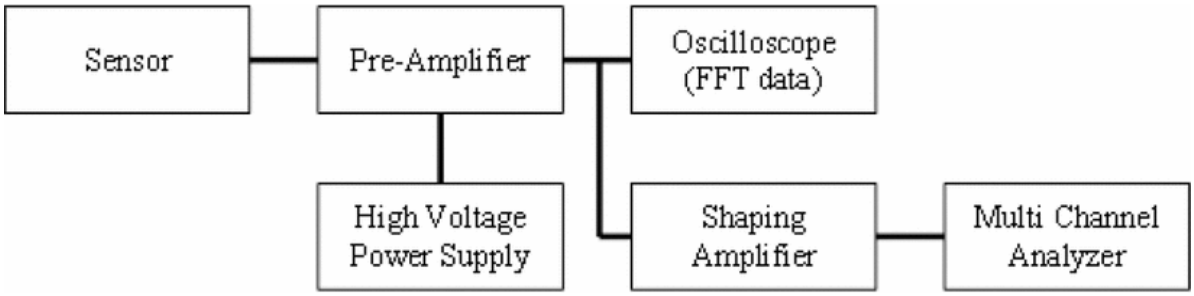


Fig. 3.4. Schematic of electronic readout chain.

The IV curves are measured directly from the detector via a probe station connected to a semiconductor parameter analyzer (Keithley 4200-SCS). For the other measures, the general setup is shown in Fig. 3.4. The shaping amplifier (Ortec 572A) and multi-channel analyzer (MCA) are included to derive the gamma-ray energy spectra.

For the noise power spectra, the preamplified signal is digitally sampled and transformed with an oscilloscope (Lecroy Waverunner 204Xi with 2 GHz bandwidth and 10 GSa/s sampling rate). The FFT signal is represented as a power spectrum that has a unit of dBm.

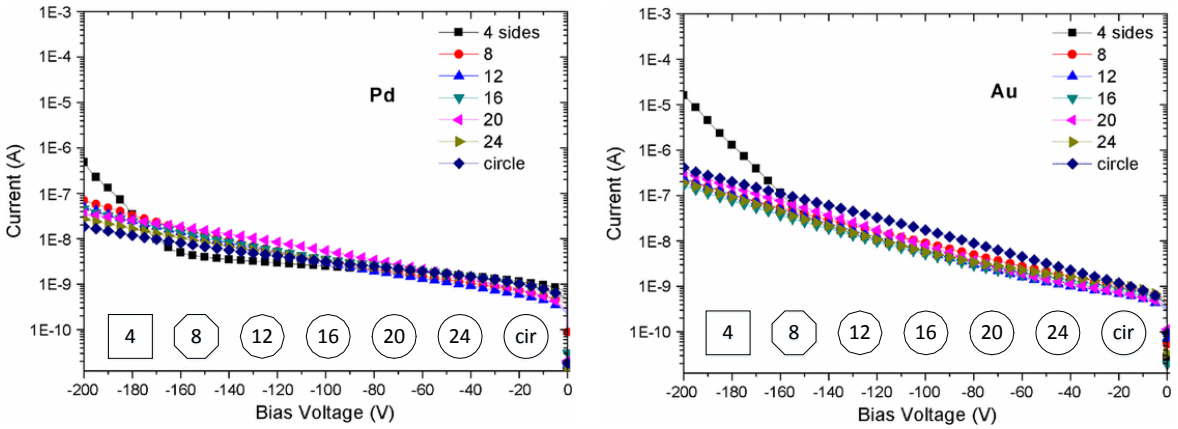
$$dBm\ Power\ Spectrum = 10 \times log_{10}\left(\frac{M_n^2}{M_{ref}^2}\right) \quad (3)$$

where M_n is the nth voltage magnitude and M_{ref} = 0.316 V. That is, 0 dBm is defined as a sine wave with a 0.316 V peak or 0.224 V_{rms}, delivering 1.0 mW into 50 Ω. The dBm power density spectrum, measured in units of V^2/Hz is the power spectrum divided by the equivalent noise bandwidth of the filter, in Hertz. The equivalent noise bandwidth (ENBW) is that of a rectangular filter which would collect the white noise signal in each frequency bin with the same gain at the center frequency. We utilized a rectangular window with an ENBW of 1.0 bins and the frequency step (Δf) used was 477 Hz.

3.4 Noise Measurements and Effect on Radiation Response

3.4.1 Experimental Effect of Changing the Contact Material

Fig. 3.5 shows the current-voltage characteristics for the pin devices of various side multiplicity, with either Pd or Au metals on the (top side) p+ contact. The diodes contain neither guard rings nor metal-field plate structures (cf. [33]) and the square diodes, with the sharpest corner curvature, thus start to breakdown below 200 $V_{reverse}$, with a post-breakdown shape that is consistent with avalanche breakdown over different ionization integrals that depend on the diode geometry. For the 1/f noise study, we are concerned with the pre-breakdown leakage current, and the IV curves show that the Pd-bounded pin devices have lower noise than the Au contacted structures.



(a) (b)

Fig. 3.5. The IV characteristics of the pin-type Si radiation detectors that have either Au or Pd contacting the p+ contact. The numbers in the legend define the number of sides on the diode.

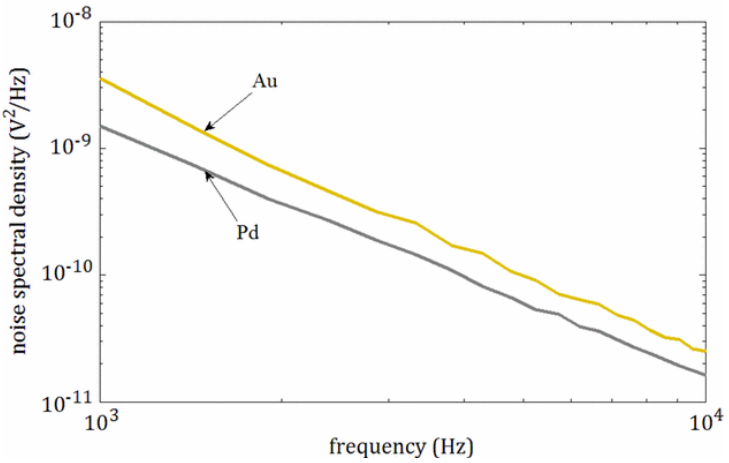


Fig. 3.6. FFT of low-noise Si pin detector signal for either Au or Pd contacting the p+ region. The botton n+ metal contact is Al. The detector was biased to 50 $V_{reverse}$.

Fig. 3.6 shows the FFT of the detector's digitized signal as derived from the charge-sensitive preamplifier output. The first point to note is that the noise spectral density falls across the measured frequency range with a roughly constant slope. Thus, those sources governing the variation at low frequencies are relevant at the higher frequencies where radiation pulse shapes reside.

Upon comparing the relative response from the various materials, we find that Pd and Pt have approximately the same noise spectral density, while the Au-contacted detectors have noise that is 3-5 dB higher, the latter corresponding to 3 times more noise.

The noise spectral density measurements, in general, were consistent with the phonon leakage model although one must take care when comparing different metals and assigning the variation to one physical mechanism. Nevertheless, the 3-5 dB variation between the Pd and Au test case is rather large and significant for nuclear measurements.

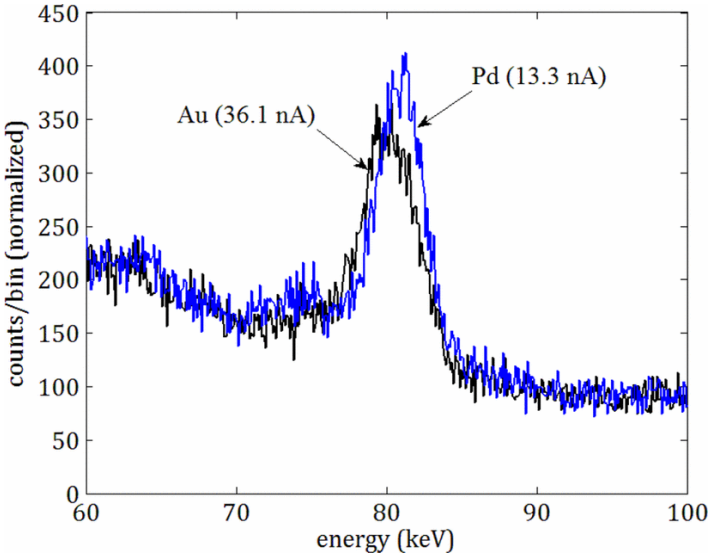


Fig. 3.7. ^{133}Ba gamma-ray spectra derived from Pd-bounded and Au-bounded Si pin detectors operated at 120 $V_{reverse}$, in which a standard pulse-processing chain (charge-sensitive preamp, shaping amp, MCA) was sused to collect the distributions.

Specifically, Fig. 3.7 shows the gamma-ray spectra derived from ^{133}Ba gamma-rays impinging upon single typical detectors of each contact type, recalling that multiple gammas are emitted by the isotope (356 keV, 383 keV, 302 keV, 81 keV) with various yields. If one focuses on the 81 keV peak (Fig. 3.7), then one can see that the peak resolution is moderately better for the Pd device (4.6% (3.71 ± 0.03 keV) vs. 4.9% (3.94 ± 0.03 keV) for Au), and the leakage current is approximately three times less (36 nA vs. 13 nA at 100 $V_{reverse}$). The standard deviation in the resolution (0.03 keV for both spectra) is small because approximately 10,000 net counts contribute to each peak; thus, the fractional standard deviations in the resolutions are much smaller than the observed difference between the diode cases.

More interestingly, as the leakage current is increased—achieved by simply increasing the bias voltage—such that the intrinsic detector noise dominates the noise response, the variance between the Pd and Au responses becomes great, as indicated in Fig. 3.8, in which the IV curves

are compared. In fact, one can bias the device such that the peak resolution for Au completely degrades while the Pd devices continue to resolve the spectral features.

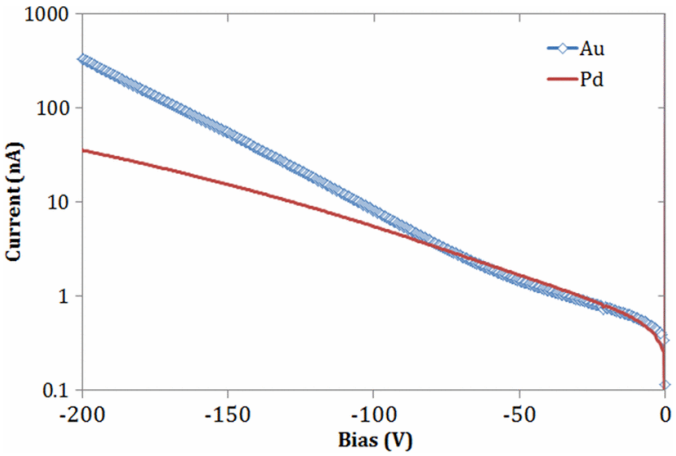


Fig. 3.8. IV characteristics derived from Pd-bounded and Au-bounded Si pin detectors.

One might hypothesize that the resolution improvement in the Pd-bounded device may be due, in part, to the lower atomic number and density of the contact relative to Au, the effect of which is greater charge creation in the semiconductor bulk and therefore lower Fano-noise for those events that are initiated in the contact. However, most of the gamma-ray interactions occur in the silicon substrate (~97% the Pd devices and ~85% for the Au-bounded pin structures) and for those that do not, roughly 98% of the secondary electron energy-loss is in the silicon substrate because the range is 10's of micrometers, based on Monte Carlo simulations [35]. Thus, one doesn't expect a contact-effect nor is one observed; for instance, in energy peaks that are at lower channel number for the Au devices compared to Pd devices.

Thus, with our best noise control environment—that of an optimized Si pin process recipe—we see variations that are consistent with mobility fluctuations derived from phonon-electron interactions. However, the data did not yet convince us of the RPMG picture because one can't definitely eliminate other sources of variation. To do that, we sought to make identical diodes and to compare their noise properties as the interfacial geometry away from the depleted structure was varied, as will be explained next.

3.4.2 Experimental Effect of Changing the Metallized Area

As indicated in Fig. 3.9, for the Si pin devices, the FFT measurement indicated that for completely identical 1×1 cm^2 die (each of which contains four diodes with 2 mm lateral extent as shown in Fig. 3.3), the diode-to-diode noise variation was less than 1 dB, a 30% variation that is typical when low-noise devices (~100 s of pA to nA leakage currents) are being processed. Fig. 3.9 shows one example in which the die aren't identical because the diode shape and spacing vary; nevertheless, the noise response is highly consistent. We therefore seek effects in which 3 dB or 5 dB differences are consistently measured so that process-induced stochastic variations can be eliminated.

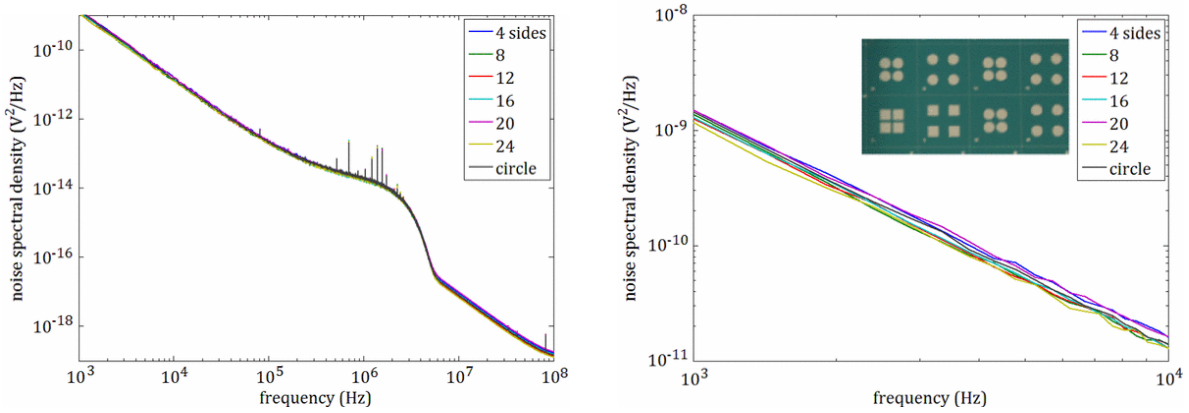
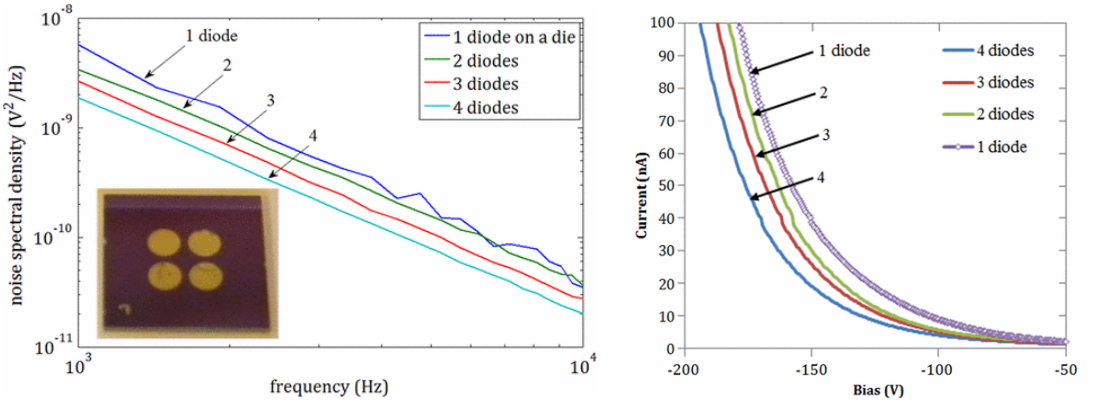


Fig. 3.9. FFT variation across the entire wafer (for a given metal contact, Pt in this case) as the shape is alone changed. The Si pin diodes are biased to 50 $V_{reverse}$ and the gap between the diodes is 2 mm. The full frequency spectrum is shown in the top figure and the 1 kHz-10 kHz region is expanded on the bottom for clarity.

If one measures the noise properties from Au-covered circular diodes, then based on the vertical device design, one expects equivalent noise responses. In addition, if one varies the amount of metal that covers the surface peripheral to the device, then we don't expect that to have an effect as long as the intervening oxide suppresses surface currents, as it does for our Si pin structures. However, if the roaming phonon effect is substantial, then the area through which phonons may leak is decreased as the metallized area decreases, and the noise should increase. Put simply, more metal is predicted to result in lower noise. Interestingly, this is what is observed if we vary the number of Au-covered diodes on a die, such as that shown in Fig. 3.10.



(a) (b)

Fig. 3.10. (a) FFT variation as the number of Au-covered circular diodes is varied. Note that this low-frequency measurement is consistent across the range all of the way up to 0.1 GHz. The inset shows a die with all four diodes covered with Au. (b) IV curve comparison of the diodes as the number of peripherally covered diodes is varied.

Specifically, four circular diodes are processed on each die, but for the experiment, we varied the number of diodes that were covered with gold, all other processes being equivalent. As shown in either the FFTs (Fig. 3.10a) or the IV curves (Fig. 3.10b), the noise is lowest for those die with four diodes covered, next lowest for three Au-covered diodes, and so forth such that the die with the least Au-covered area (the one-diode case) had the highest noise. Furthermore, if one examines the FFTs, we see that the variation between diodes was a sizable and significant 5 dB. This variation was consistent across multiple runs and therefore reproducible. Fig. 3.11 further indicates that the noise variance has spectral consequence with increasing effect as the detector noise becomes more dominant.

Fig. 3.10b shows the IV curve in linear form, which clarifies that the absolute noise value becomes large as the bias is increased beyond 100 $V_{reverse}$. Nevertheless, even at 100 $V_{reverse}$, in which the leakage currents for the 4 diode, 2 diode, and 1 diode cases are 4, 5, and 9 nA, respectively, the effect on the ^{133}Ba spectrum is apparent, as shown in Fig. 3.11. Quantitatively, for the 4, 2, and 1 diode cases, the resolutions of the 81 keV peaks are 3.3% (2.67 ± 0.01 keV), 3.6% (2.92 ± 0.01 keV), and 5.1% (4.1 keV ± 0.02 keV), respectively. As discussed above, the fractional

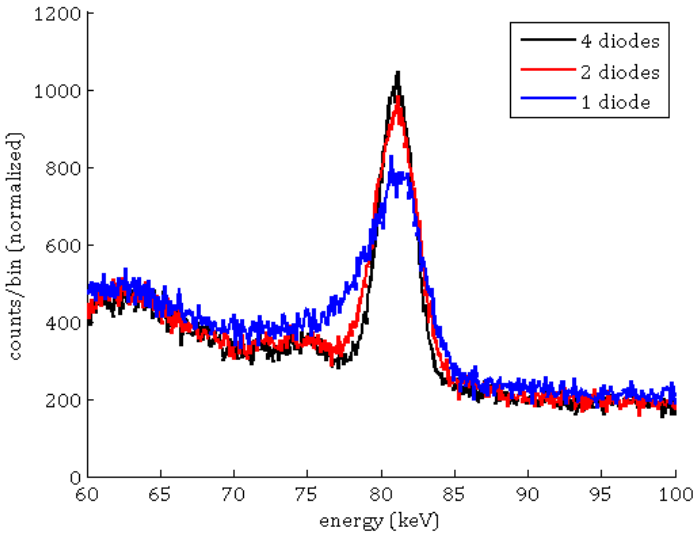


Fig. 3.11. ^{133}Ba gamma-ray spectra, focusing on the 81 keV spectral line, derived from Au-bounded circular diodes Si pin detectors operated at 100 $V_{reverse}$ in which the number of diodes on the die is varied.

standard deviations in the resolutions are much smaller than the observed difference between the 4, 2, and 1 diode cases because more than 20,000 net counts contribute to each peak. If the reverse bias is increased to 150 $V_{reverse}$, then the features are indistinguishable for the 1 diode case, but they remain resolvable for the four-diode case. The measurements therefore suggest that phonon surface leakage can impact the noise markedly, and one should therefore maximize the areal coverage of the peripheral metallization, all else being equal.

In order to further test this observation, we processed die with lateral metallic coverage greater than that used above, but with each die consisting of same dimensions (1 × 1 cm^2) analyzed above, although the individual diode diameters are reduced by a factor of 2 (to 1 mm). For instance, Fig. 3.12 shows die with a 1 mm diameter circular diode, and 3 × 3, 5 × 5, and 7 × 7 arrays of 1 mm diameter diodes, all using a high phonon leakage contact (Ag). In all of the experiments, the peripheral diodes were unconnected and unbiased. The silicon substrate and vertical junction design remains identical, only the metal and mask pattern are varied; most notably, the bottom n+ contact is still covered with Al.

As in Fig. 3.10a, the noise in Fig. 3.12 scales with the areal coverage, the greatest metallic coverage resulting in noise spectral density near that measured without the detector connected ("control" in Fig. 3.12). For the 7 × 7 array shown in Fig. 3.13 the lateral area of the top-side

metallization is four times greater in this case (37.7 mm^2 vs. 9.4 mm^2) compared with the geometric design shown in Fig. 3.10a.

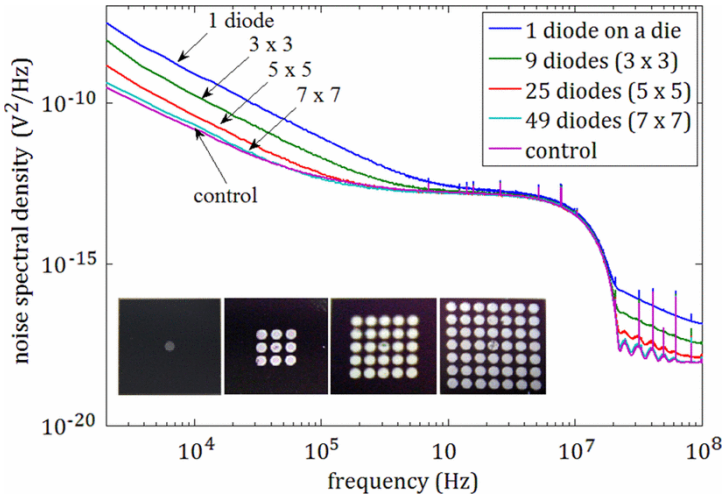


Fig. 3.12. FFT variation of the central diode as the number of Ag-covered 1 mm diameter circular diodes is varied. Note that the noise from the preamp dominates the noise in the 1 MHz – 10 MHz range. The inset shows the various die designs.

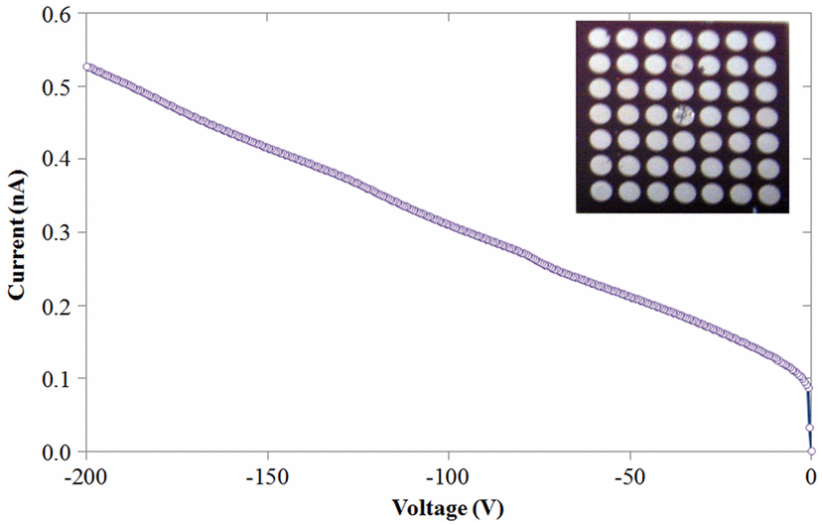


Fig. 3.13. For the central 1 mm diameter Ag diode shown in the inset picture, the IV curve under reverse bias. The total die dimensions are 1 × 1 cm^2 and all of the neighboring diodes are covered with Ag.

As shown in the IV curve in the figure, the leakage current, at 311 pA at 100 $V_{reverse}$, is suppressed by two orders of magnitude relative to previous measurements, approaching the leakage current density that we can achieve only if highly engineered guard rings and metal-field

plates are employed (cf. [32] and [33]). Note that the noise is quenched by an order of magnitude more than one would expect from the ~4 times diminishment in the diode's top-metal contact area (from 3.1 mm^2 to 0.79 mm^2), a reduction that mitigates the bulk-induced leakage current and the capacitance, the latter reducing the FET-noise on the preamp. This lends credence to the supposition that the phonon-leakage characteristics of the interface impact the electronic noise. Nevertheless, one should recognize that the extended diode arrays of Fig. 3.10a or Fig. 3.12 may be acting, in part, as a guard ring structure and thus contributing to the diminishment. We therefore evaluated the magnitude of this effect by processing detectors with Pd central diodes but with different metal on the peripheral diodes.

Consider the extended diode arrays shown in Fig. 3.14, in which a central 2 mm diameter Pd-covered Si pin diode is surrounded by identical pin structures bounded by different metals. Specifically, the left-most die includes a central Pd diode embedded in a 5 × 5 array of Pd-covered diodes. The right-most die consists of the central Pd diode surrounded by Au-covered structure, and the central die consists of a central Pd diode embedded in a 3 × 3 Pd array, that is ultimately surrounded by Au in the outer ring.

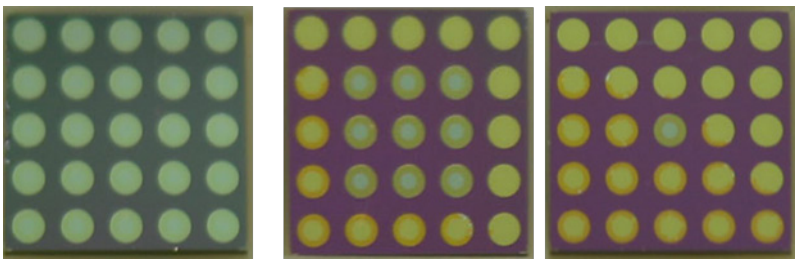


Fig. 3.14. Pd-covered 2 mm diameter circular Si pin central diodes embedded, from left-to-right, in: a 5 × 5 array of Pd-covered diodes, a 3 × 3 of Pd array with an outer ring of Au, and a 5 × 5 array of Au covered diodes, respectively.

One possible direct effect of adding metallization to the die is shown in Fig. 3.15, in which the electric field lines are shown for a central conductor with charge 4σ adjacent to a smaller σ conductor. As bias is applied to the central diodes of Fig. 3.14, charge can migrate over the surface to the neighboring contacts, thus reducing the electric-field gradient at the surface. This is standard practice when guard-rings are allowed to float. The broken guard ring structures of Fig. 3.14 may not perform as effectively as a complete ring; however, the charge-migration process can still result in a reduction of the charge flow through the readout circuit.

A second possible direct electrical mechanism through which the current noise can be reduced is by a diminishment in the volume that is electrically exposed to the central guard ring, as suggested in Fig. 3.15. Neighboring contacts can divert field-lines that would have contacted the central diode in their absence and therefore reduce the flow of thermally-induced charge to the central anode.

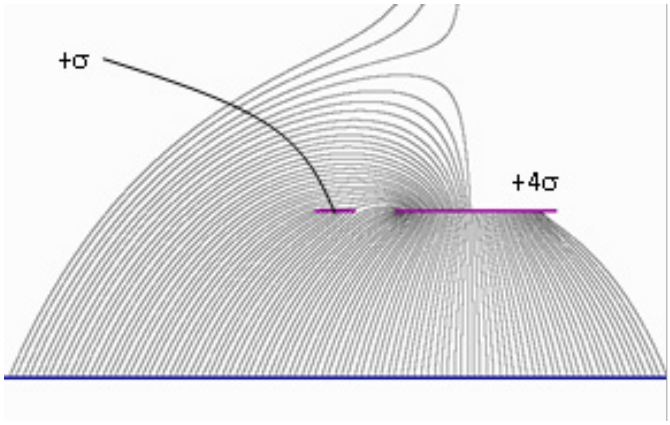


Fig. 3.15. Theoretically derived electric field lines for the charge distribution shown.

If either of these direct electrical mechanisms results in the noise reduction observed previously, then we expect that the degree of noise reduction will be the same, whether the surrounding diodes are contacted with Au or Pd. However, if the surrounding metals have an indirect effect on the electrical noise; specifically, if the surrounding metals increase the degree of phonon percolation out of the semiconductor, then the Pd covered diodes should decrease the noise to a greater degree than the Au-covered diodes. The direct hypotheses were tested first using the 3 × 3 arrays shown in Fig. 3.16.

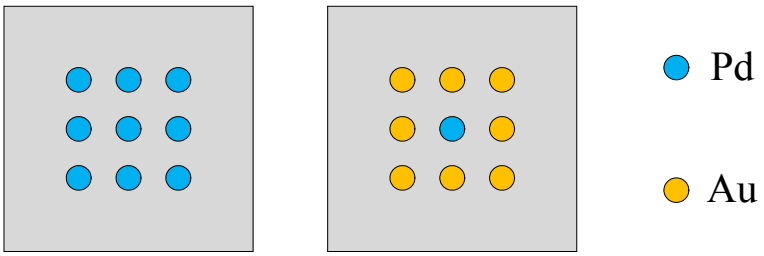


Fig. 3.16. Pd-covered 2 mm diameter circular Si pin central diodes embedded, from left-to-right, in: a 3 × 3 array of Pd-covered diodes and a 3 × 3 array of Au covered diodes, respectively.

The IV curves for the central Pd diodes of Fig. 3.16 are compared with each other and a single Pd diode, in Fig. 3.17. First note that the single Pd diode (in blue) has higher leakage current than either of the metal-surrounded diodes, buttressing the earlier measurements that indicated that more peripheral metallization results in lower noise. In order to clarify the source of the reduction, the red and black curves compare the difference in leakage current when the peripheral metal type is changed. As shown in the figure, the variation matches the predictions of the roaming phonon micrograd ient (RPMG) model, because the Pd-surrounded diode results in lower noise than the Au-surrounded Pd test diode.

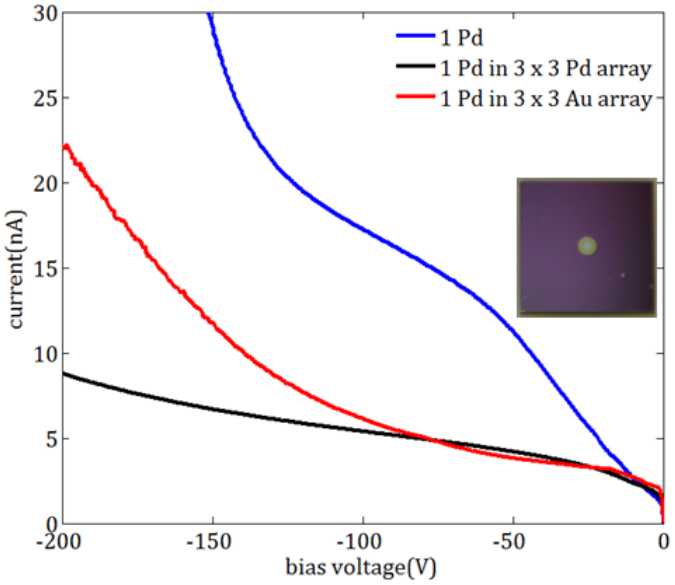


Fig. 3.17. IV curve comparison of the diodes as the number of peripherally covered diodes is varied, from 1 diode (in blue) to a 3 × 3 array (in red or black). The red curve corresponds to the Au-surrounded array and the black curve was derived from the fully Pd array.

Note that the leakage current density shown in Fig. 3.17 at 100 $V_{reverse}$ (~150 nA/cm^2) is not the best that we can achieve, which is approximately an order of magnitude better, when optimized guard rings are employed on bigger devices. One of the goals of our current effort is to maximize the degree to which the noise can be reduced via this indirect phonon effect. As shown in Fig. 3.18 and Fig. 3.19, the difference in behavior due to the peripheral metallization can, nevertheless, be large and important for radiation spectroscopy.

At our typical reverse bias voltage, 100 V, Fig. 3.18 shows that the 81 keV peak resolution reduced from 8.3 % (6.7 keV) to 3.7 % (3.0 keV) when the surrounding Au contacts were replaced by surrounding Pd contacts, which is the much more transparent to phonons. The degree to which this phonon effect becomes important increases as the detector noise increases, controlled most simply through either the detector size or the bias. In fact, we chose 2 mm wide diodes because they provide a balance between maximizing the diode size and maximizing the number of device iteration that can be fit on a 4″ wafer.

If the central diode is biased beyond 100 V to 150 V reverse bias, then one expects from the IV curve of Fig. 3.17 that the noise from the Au-surrounded case will substantially degrade while the Pd-surrounded diode will remain low noise. As confirmed in Fig. 3.19, this is precisely what is observed, even to the point where we start to loss the 81 keV peak because of thermal noise competition

The 3 × 3 arrays comparing the effects of Pd and Au are thus consistent with the phonon -reduction mechanism, rather than the guard-ring mechanisms. This measurement can be further buttressed by experiments with arrays of different size, such as the 5 × 5 arrays shown above in Fig. 3.14.

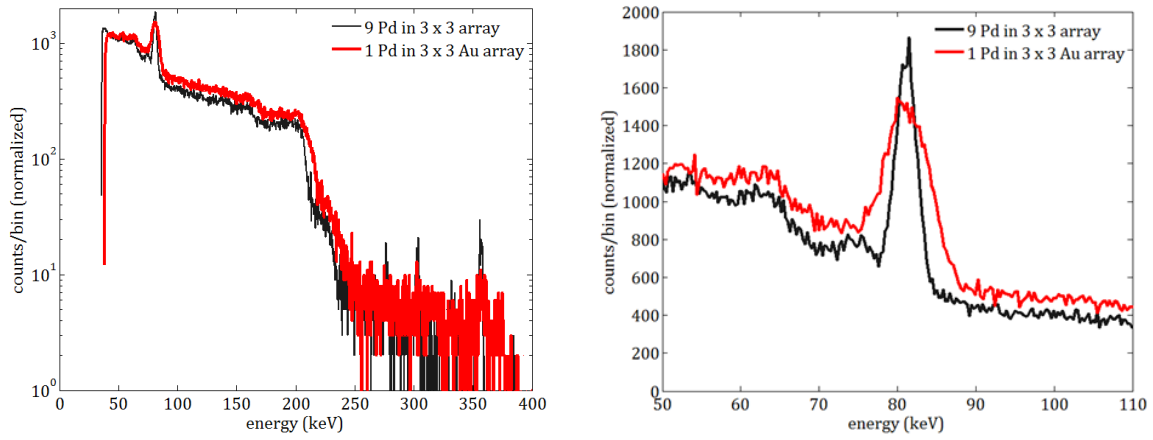


Fig. 3.18. ^{133}Ba gamma-ray spectra, focusing on the 81 keV spectral line, derived from Pd-bounded circular diode Si pin detectors operated at 100 $V_{reverse}$ in which the type of metallization is varied from Pd (black) to Au (red). The spectra, derived from a ~1 mCi 133Ba source, were measured for 1 hour.

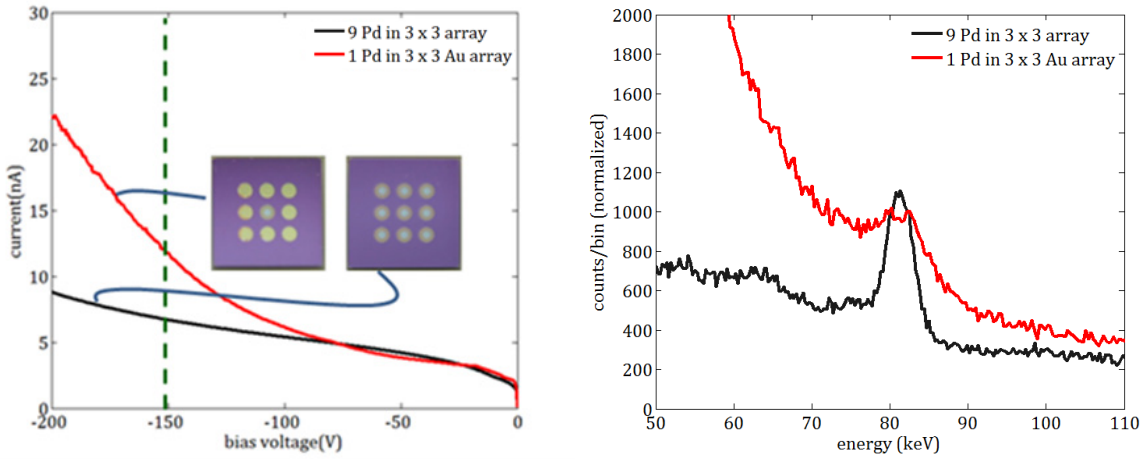


Fig. 3.19. IV curves and ^{133}Ba gamma-ray spectra, focusing on the 81 keV spectral line, derived from Pd-bounded circular diode Si pin detectors operated at 150 $V_{reverse}$ in which the type of metallization is varied from Pd (black) to Au (red). The spectra, derived from a ~1 mCi 133Ba source, were measured for 1 hour.

Specifically, Fig. 3.20 shows the spectral comparison between Pd-covered 2 mm diameter circular Si pin central diodes embedded in: a 5 × 5 array of Pd-covered diodes (blue), a 3 × 3 of Pd array with an outer ring of Au (black), and a 5 × 5 array of Au covered diodes (red). Note that changing from a fully Au peripheral metallization to various degrees of Pd has a marked effect of the peak resolution, decreasing from 3.71 % (3.0 keV) to 3.09 % (2.5 keV) for the 9 Pd case and 2.95 % (2.4 keV) for the 25 Pd case. The difference between the 9 Pd case and the 25 Pd case is not substantial in the peak resolution, but one can observe the lower noise in the lower background in the blue trace of Fig. 3.20. As in the 3 × 3 case, the 5 × 5 case therefore provides more evidence that the phonon-modulation effect exists and its effect is substantial.

The next step is to therefore optimize the degree to which the noise can be quenched by mitigating the extent of that portion of the phonon population that participates most strongly in electron-phonon scattering. One systematic methodology for monitoring the effect of the boundary on the bulk phonon-population is to derive the phonon density of states (PDOS) from the underlying dynamics of the atoms in the solid. The use of molecular dynamics simulations to monitor the motion of Si or Ge atoms when bounded by different contacts is discussed next.

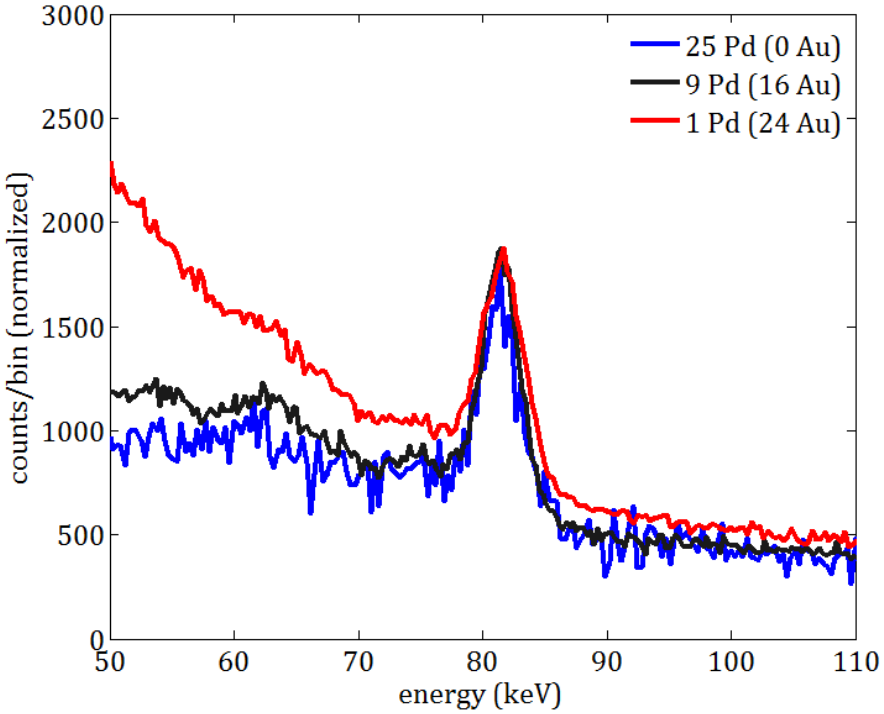


Fig. 3.20. ^{133}Ba gamma-ray spectra, focusing on the 81 keV spectral line, derived from Pd-bounded circular diode Si pin detectors operated at 100 $V_{reverse}$ in which the type of metallization is varied from fully Pd (blue), to 9 × 9 Pd inside Au ring (black), to fully Au (red).

3.5 Phonon Density of States Derived from Molecular Dynamics Simulation

One of the advantages of using silicon as a test-bed upon which one can investigate the physics of phonon-induced current quenching is that the material has been extensively studied by theoretically and experimentally. For instance, there are over thirty different forms of the interatomic potential that governs the Si-Si interaction, optimized for various material investigations, but many based on the Stillinger-Weber (SW) potential [36], [37]. A more recent potential, the so-called Environment-Dependent Interatomic Potential (EDIP), is more rooted in *Ab Initio* quantum mechanical calculations that lend a physical basis to many of the features of the potential [38]. Regardless of the precise form, the potential is used in molecular dynamics (MD) simulations to increment the motion of each atom in the solid, when acted upon by all of the other constituent atoms [39], [40]. That motion can then be used to observe the variation in the microstructure for various external stimuli (stress, strain, temperature change).

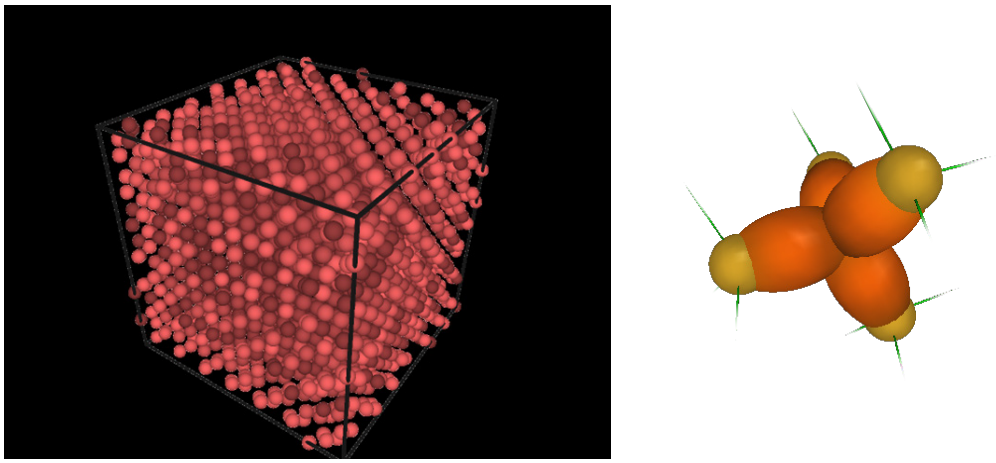


Fig. 3.21. 7 × 7 × 7 unit cell lattice of 2744 silicon atoms, each in the tetrahedral configuration shown on the right.

Our interest is to observe the degree to which the PDOS is modified by the surface, and more particularly, to find those boundary conditions that shift the lattice energy away from those modes that participate in electron-phonon scattering and towards those transverse optical modes for which the scattering integral is small [41]. In order to calculate the PDOS, one typically evaluates the velocity-velocity autocorrelation function from the trajectory of each atom in a molecular dynamics simulation, whose Fourier transformation gives the phonon density of states (PDOS) [42]. For the PDOS shown below, we instead constructed the dynamical matrix by observing the displacements of atoms during molecular dynamics simulation, making use of the fluctuation-dissipation theory [43], [44]. Using this method, the PDOS for bulk silicon was simulated using a 7 × 7 × 7 unit cell, each unit cell containing 8 silicon atoms in a diamond-cubic lattice, as shown in Fig. 3.21.

For simulating bulk properties, one employs periodic boundary conditions, in which the atoms on opposite faces of the cell interact with each other. This is an appropriate assumption because the forces acting on the atoms are assumed to be short-range with well-defined cutoffs. For instance, Fig. 3.24 shows the results of our simulation using a Stillinger-Weber (SW) potential compared with some distributions from the literature [36], [45].

The two-body SW potential is shown in Fig. 3.22 compared with potentials derived from the Environment-Dependent Interatomic Potential [38]. In general, when choosing an appropriate potential, a curve shape such as that shown in Fig. 3.22 is employed and then fit such that the

simulation produces appropriate behavior, compared with measured bulk properties. For the SW potential, whose form has found wide-spread use, the fit parameters used for the presented simulations are shown in Fig. 3.23. As shown in the figure, for diamond-cubic lattices, one must employ a three-body term as well as a two-body term in order to ensure valence saturation as well as bond-angle compliance with the known tetrahedral form, as shown in Fig. 3.21.

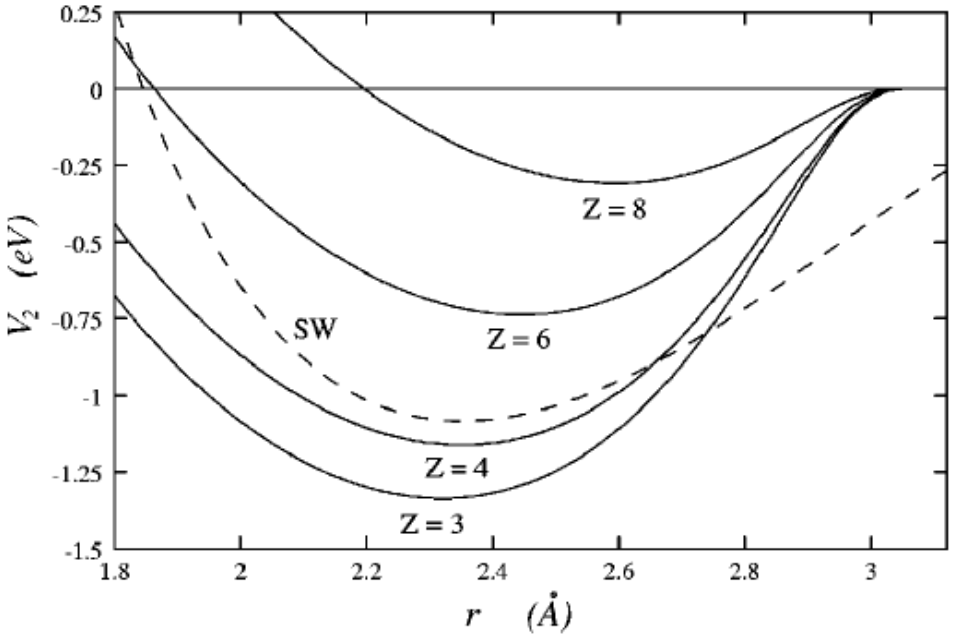


Fig. 3.22. Radial variation in the two-body form of the SW potential compared with the EDIP potential for various coordination number, Z [38].

$$f_2(r) = \begin{cases} A(Br^{-p} - r^{-q})\exp[(r-a)^{-1}], & r < a \\ 0, & r \geq a \end{cases}$$

$$f_3(r_i, r_j, r_k) = h(r_{ij}, r_{ik}, \theta_{jik}) + h(r_{ji}, r_{jk}, \theta_{jik}) + h(r_{ki}, r_{kj}, \theta_{ikj}),$$

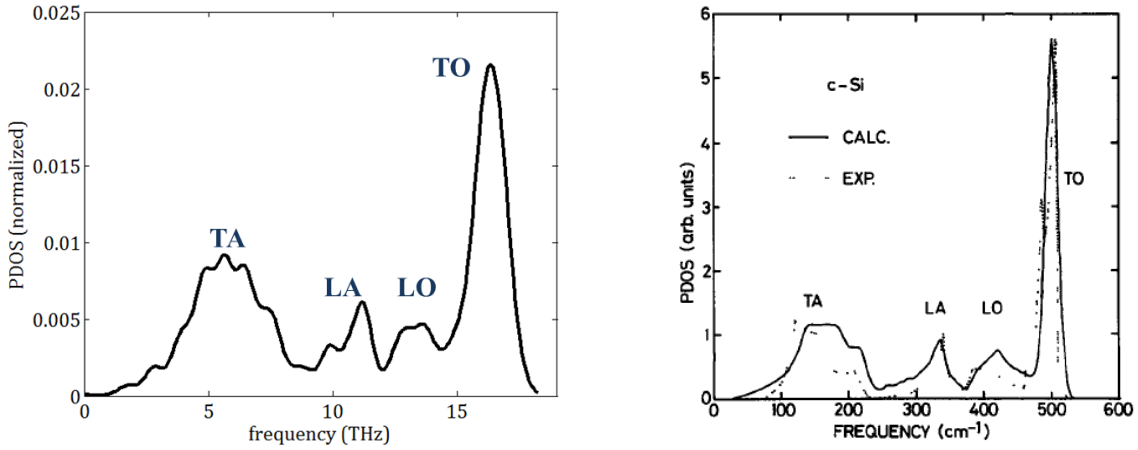
$$h(r_{ij}, r_{ik}, \theta_{jik}) = \lambda \exp\left[\gamma(r_{ij} - a)^{-1} + \gamma(r_{ik} - a)^{-1}\right] \times (cos\theta_{jik} + {}^1/_3)^2$$

$A = 7.049\,556\,277$, $B = 0.602\,224\,558\,4$,

$p = 4$, $q = 0$, $a = 1.80$,

$\lambda = 21.0$, $\gamma = 1.20$.

Fig. 3.23. Two-body Si-Si potential (f_2) and three body Si-Si-Si potential (f_3) as well as the fit parameters, in which θ is the angle between the three atoms in the solid [36].



(a) (b)

Fig. 3.24. (a) 7 × 7 × 7 unit cell lattice PDOS compared with (b) bulk theoretical calculation and experimental measurement from [45]

If one wishes to quench the electronic noise via a phonon mechanism, then the phonon modes of interest are the lower frequency longitudinal acoustic (LA) and transverse modes. Recall that for *N-processes*, LA modes dominate electron-phonon scattering, but U-processes can result in electron-phonon scattering of the transverse modes [41]. Furthermore, the longitudinal optical (LO) and transverse optical (TO) modes can also participate in scattering in Si and Ge because of its diamond cubic structure [41]. Nevertheless, we are primarily interested in modifying the LA modes that dominate the scattering integral. Colloquially, we therefore seek to either shift the modal frequencies to higher frequencies using a more tightly bound structure, or we attempt to change the boundary pattern such that transverse oscillations are preferred rather than longitudinal modes.

An example modal shifting is shown in Fig. 3.25, in which a thin-film of Si is simulated using a 5 × 5 × 5 unit cell. This thin-film is realized by using a free-boundary condition (BC) on the top and bottom faces of the lattice and periodic BC's on the lateral dimensions which results in removal of the bonding energy on top and bottom atoms. As shown in the figure, relaxing the BC's results in lower frequency modes, as expected, because the weaker surface bonding. Pd and Au have similar lattice constants and are therefore bonded to the silicon substrate in a similar matrix; however, the Pd makes stronger bonds with the surface to a greater degree, which may explain the experimental observation of lower noise.

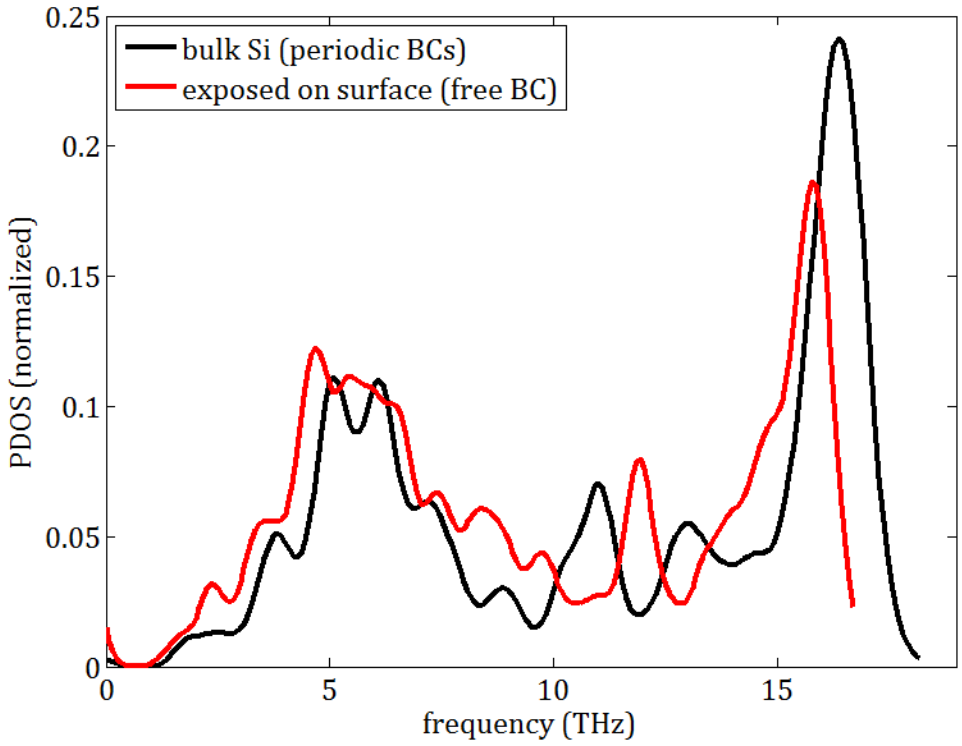


Fig. 3.25. 5 × 5 × 5 unit cell lattice bulk PDOS (black) compared with thin film PDOS (red).

Two of the drawbacks of the MD approach are that the result can be sensitive to the size of the ensemble simulated, and the atom-by-atom calculations, one femtosecond at a time, can be time-consuming. Regarding the former, note that the 5× 5 × 5 unit cell bulk case in Fig. 3.25 (in black) differs slightly shift from the equivalent 7 × 7 × 7 distribution in Fig. 3.24. In particular, the acoustic modes slightly shift between the two cases. In order to remove these size-dependent variations, one would prefer to use larger ensembles, such as the 35 × 35 × 35 unit cell ensemble in Fig. 3.26. Unfortunately, the simulation takes very long time for every ns of simulation time, multiple nanoseconds being needed to measure the lowest frequency phonon modes.

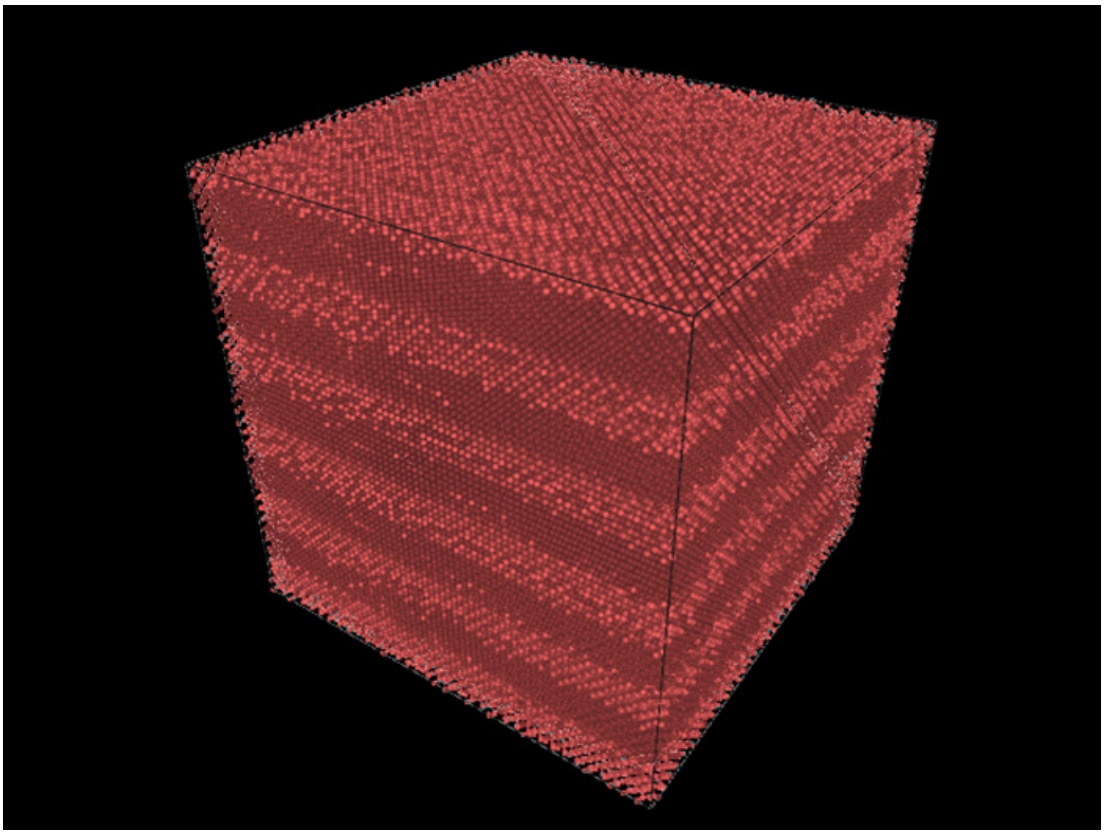


Fig. 3.26. 35 × 35 × 35 unit cell lattice of 343,000 silicon atoms.

These MD simulations are focusing on Si and Ge, for which there exists a more extensive literature of interatomic potentials than for other technologically relevant materials, such as CZT or TlBr, recalling that one needs validated potentials not only for the substrate atoms but also for the contact material cross-terms (e.g. Au-Si, Pd-Ge). Furthermore, “cooling” Si and high purity Germanium (HPGe) through non-active means could set a technological precedent for various sensing devices. We therefore are also engaging in the microelectronic fabrication of germanium-based detectors.

Chapter 4. Particle Sensors with Integrated Amplification

4.1 Introduction

For solid-state radiation detectors that convert energy directly into charge carriers, the noise floor is typically dominated by the thermally-generated current fluctuations in the detector and the preamplifier electronics. The detector's surface-leakage current can be mitigated by guard rings and surface passivation [33], [46 - 47]. The bulk leakage current can be quenched by either gettering the mobile impurities [48] or by employing fabrication techniques that reduce the frequency of the phonon-electron scattering as described in Chapter 3.

Upon the successful quenching of the detector's noise, the noise floor is not typically set by the statistical counting limit associated with the stochastic charge-creation process during a radiation interaction as desired, but rather by the gate noise of the preamplifier. For instance, Fig. 4.1 shows the ^{133}Ba gamma-ray spectrum for a small silicon PIN diode, the fabrication of which is described in [33]. If one calculates the Fano noise that results from the deposition of 81 keV in

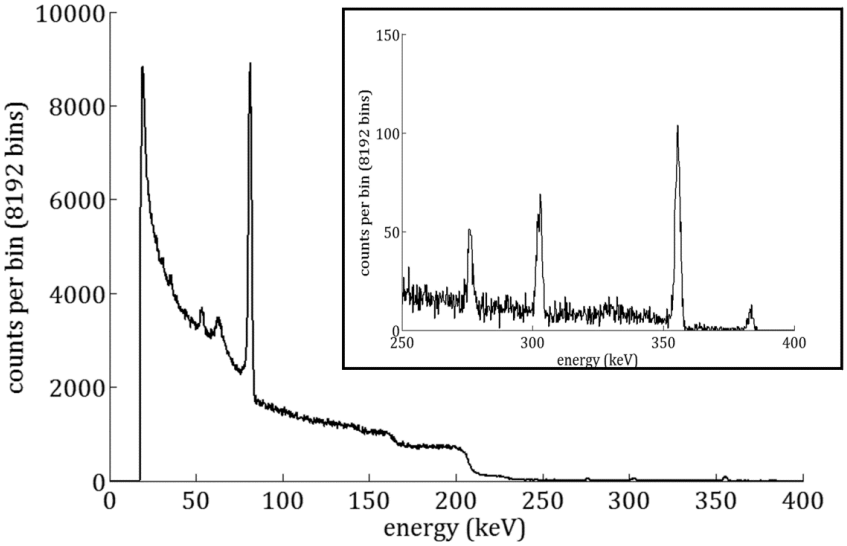


Fig. 4.1. ^{133}Ba gamma-ray spectra, derived from Ag-bounded circular diodes Si PIN detectors operated at 100 $V_{reverse}$ in which the number of 1 mm diameter circular diodes on the 1 × 1 cm^2 die is maximized. The inset shows an expanded view of the 250 – 400 keV region, where most of the photopeaks reside. The peak resolution is 2.12 % (1.72 keV) at 81 keV and 0.48 % (1.71 keV) at 356 keV' in fact, the noise is sufficiently low that the charge-sensitive readout noise characteristics dominate the peak width.

silicon (using a Fano factor of 0.115) then the energy uncertainty is 0.53% (0.432 keV), compared with a measured uncertainty of 2.1 % (1.7 keV). One can cool the front-end amplifier and develop advanced amplification methods to reduce the noise contribution of the preamp; however, if one can increase the signal size from the detector itself, then a higher preamp noise can be tolerated.

In optical photon devices, avalanche multiplication is used to produce internal device gain and enhance signal-to-noise ratio (SNR) in the form of avalanche photodiodes (APDs), but on-chip avalanching isn't typically employed in a direct-conversion nuclear radiation detector for two reasons. First, an avalanche particle detectors (APaDs) requires that the multiplication junction be developed across a relatively small voltage (< 1 V typically) because the depletion junction width of a nuclear detector may be hundreds of micrometers to a centimeter thick in order to efficiently stop a high-energy or incident neutral particle, compared with the few micrometers needed to highly attenuate optical photon flux. The consequence on the fabrication is that highly doped junctions must be formed to realize a high enough field to produce impact ionization near the surface. Second and more importantly, the signal size associated with a nuclear radiation event is orders-of-magnitude larger per quanta compared with optical-photon events, thus reducing the relative influence of the fixed noise source provided by the preamplifier. Instead, the multiplication noise associated with the stochastic process can become dominant. The range of energy depositions over which avalanche multiplication improves the SNR is presented in Chapter 4.2, in which we quantify the degree of improvement in the energy resolution for various multiplication factors and excess noise factors depending on carrier injection condition.

We designed the avalanche particle sensor configuration analytically and validated the design with numerical process and device simulations. The modeling indicates that effective multiplication junctions composed of thin n+/p+ layers can be confined to the central part of the diode if a junction termination extension (JTE) configuration is employed.

Finally, we tested the numerical design by fabricating and testing diagnostic sensors, the results from which are summarized in Chapter 4.3. The high-speed, high-resolution particle sensor consists of a high-resistivity p-type silicon substrate, in which electrons are injected into an n+/p+ multiplying junction, in which a drift field is created across the bulk of the detector and an amplifying field is created at the n+/p+ interface, the gradient and width of which governed the gain of the device. This configuration can enhance the direction and energy measurements of ions,

electrons, and low-energy photons, and is therefore applicable to detailed studies of the heliosphere, the Earth's magnetosphere, rare-isotope beams, as well as general particle sensors that require improved energy resolution.

4.2 Device Breakdown and Modeling of the Avalanche Gain

We first used solid-state physics to analytically design a diode-sensor that contained a thick stopping layer for incident particles (electrons, ions, photons), and an avalanche junction that amplifies the number of charge-carriers as they drift toward the collecting electrode. The difference between an avalanche photodiode (APD) and an avalanche particle diode (APaD) is that the latter has a much larger depletion region (0.5 mm – 2 mm thick, compared with a few micrometers), the result of which is that only a few volts or even a fraction of a volt drops across the amplifying junction. That is, one biases the sensor such that the physical thickness of the silicon substrate is fully depleted and no more, because higher bias can result in higher leakage current noise. For high-resistivity ($\rho > 10$ kΩ·cm) silicon, only 70 V is required to deplete 550 μm, which distributes uniformly in depth.

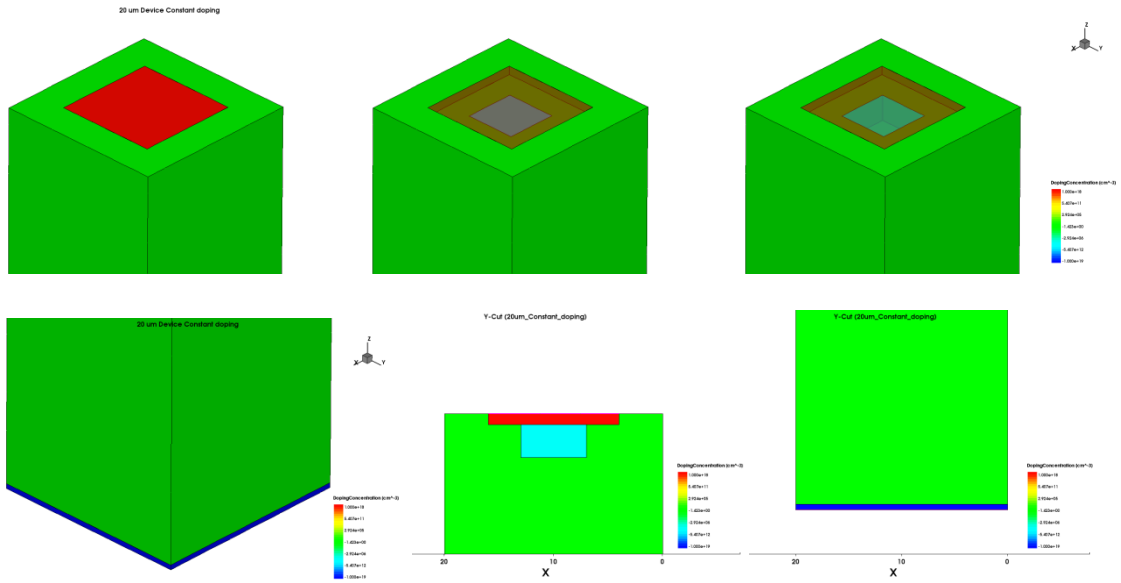


Fig. 4.2. Doping profile of the device simulation geometry with constant doping shown in 3-D view and the Y-cut view at the center.

As an example, consider a 500 μm square diode with the doping profile (12 μm wide and 1 μm thick n+ layer and 6 μm wide and 5 μm thick p+ region) shown in Fig. 4.2. Even though the field concentrates at the n+/p+ boundary, as shown in Fig. 4.3, the electrostatic potential falls uniformly across the depth of the overall sensor, so that the silicon must be highly doped such that a few volts generate enough electric field to induce avalanche multiplication.

From this study, we analytically, numerically, and experimentally found the doping necessary to induce this multiplication. Recall that float-zone (FZ) silicon wafers have resistivity of > 10 kΩ·cm, which corresponds to a boron doping of 1.3×10^{12} cm^{-3}. Unfortunately, one cannot simply deposit an n+ layer upon the FZ Si and hope to make an avalanching junction at low operational voltages, because the electrons diffuse too easily into the low-resistivity substrate in order to compensate for any applied bias voltages, thus resulting in a very moderate electric field.

For instance, as shown in Fig. 4.4, 32 kV is needed to breakdown the n/p junction (at 3×10^5 V/cm) if the lower doped side of the junction is held at FZ concentrations. We desire a breakdown voltage near the voltage needed to fully deplete the wafer (~ 100 V), which implies that the lower junction doping should be in the 10^{15} cm^{-3} range, if 100 V is developed across the junction. However, for thick (0.5 – 2mm) stopping detectors, the junction may only be $1/100^{th}$ of the detector thickness, which implies that only a few volts are developed across the junction. In that case, the plot of Fig. 4.4 shows that the junction doping concentration should be in the 10^{16} –

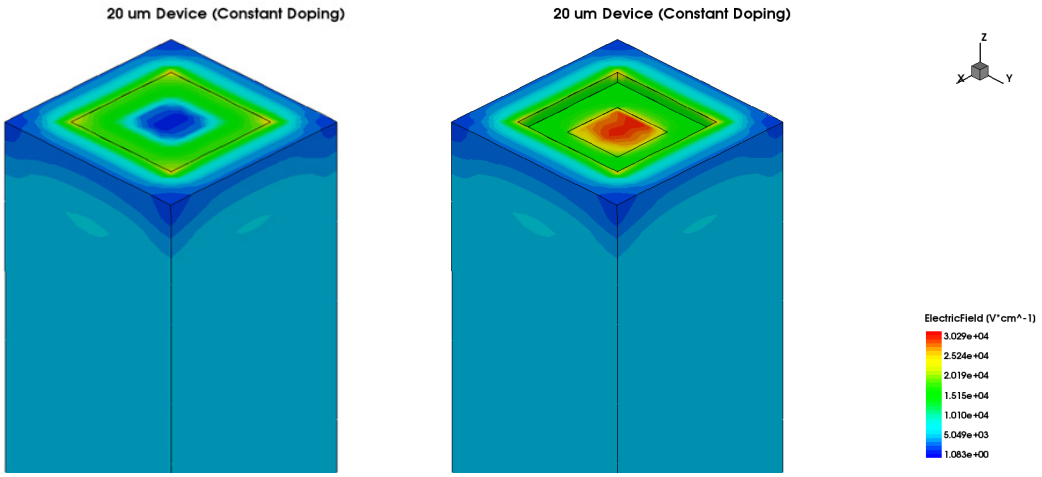


Fig. 4.3. Sentaurus simulation of n+ junction extension beyond an underlying p+ layer, showing the successful confinement of the high field region to the interior of the design.

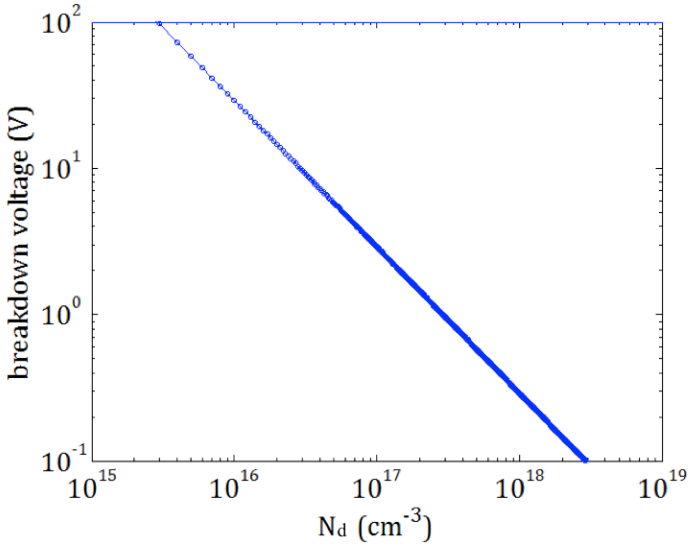


Fig. 4.4. Variation in the doping concentration as the doping for the lower side of the junction is varied, assuming a one-sided step junction and a critical field of 3×10^5 V/cm.

10^{17} cm^{-3} range. Thus, the general structure of APads should consist of a π wafer bounded by an n+/p+ junction.

It isn't enough to simply deliver a breakdown field in the diode structure; rather, the breakdown field region must be thick enough that substantial gain is developed in the devices. One of our initial goals was to predict the multiplication gain needed to maximize the signal-to-noise ratio (SNR) delivered from the device, across a range of energy depositions, given the broadly distributed energy spectrum delivered by space particles and plasmas. That multiplication information then provides guidance on the operational parameters of the device; namely, the lower limit on the thickness of the junction and the operational voltage needed to deliver the multiplication desired.

If we put aside the details of the device design and assume that some effective multiplication structure is implemented on a particle sensor, we can assess the conditions under which on-chip amplification improves the energy resolution. From Eq. (4) and (5), the improvement in the device SNR does not simply scale linearly with multiplication, M, because the stochastic avalanche process at the heart of on-chip amplification contributes its own noise, as

embodied in the excess noise F factor, included in the noise term (N) shown below, where σ_{pre}, σ_{leak}, σ_{Fano} are the preamp noise, leakage current, and Fano noise respectively.

$$N = \sqrt{\sigma_{pre}^2 + (\sigma_{leak}^2 + \sigma_{Fano}^2)M^2F} \qquad (4)$$

with a signal, S, Given by:

$$S = \frac{ME_\gamma}{w} \qquad (5)$$

where E_γ is the energy deposited by the impinging particle and w is the energy expended by charge-pair created, one can observe that if the preamp noise dominates, then the SNR does improve linearly with the multiplication. However, if the leakage current and Fano noise dominate, then the SNR is diminished relative to the M = 1 case by a factor of $F^{-1/2}$. By comparing the SNR at multiplication M with that at M = 1, we can determine the optimal M for our noise studies as well as find the limits beyond which avalanche multiplication is detrimental to the measurement. The normalized SNR is shown in Fig. 4.5.

As shown in the figure, if only a few eV of 10's of eV energy fluctuations are studied, then the degree of improvement in the SNR can exceed two orders of magnitude, and the optimal M is a device gain of several hundred. However, one can observe why avalanche photodiodes are

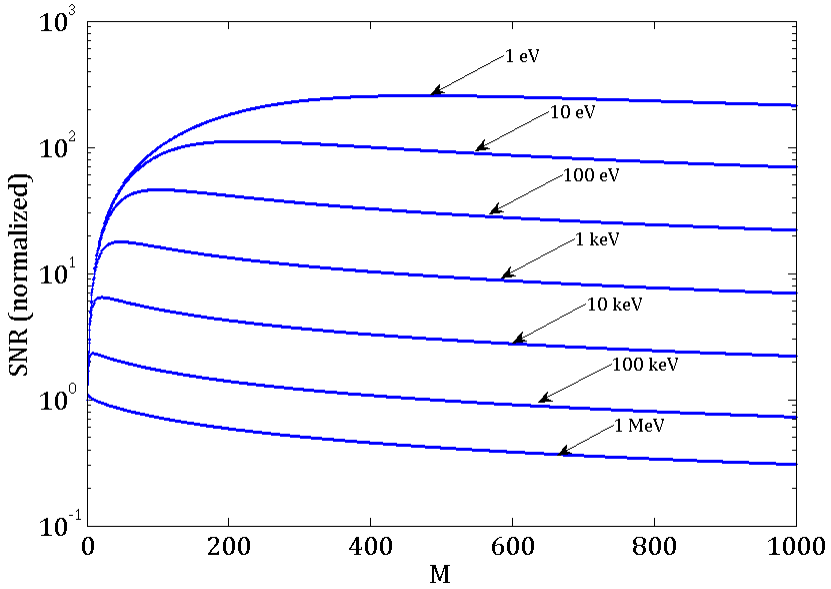


Fig. 4.5. SNR at multiplication M relative to that at M = 1 for various energy depositions, assuming electron injection with ionization coefficient k = 0.02.

common but avalanche particle sensors are largely non-existent. Specifically, if the energy deposition exceeds 1 MeV, then the SNR can actually diminish relative to the device absent on-chip amplification. Most pertinent to our low-energy gamma-ray studies, we expect an improvement of ~ 2.6 times at 81 keV, if the gain M is equal to 10, as shown in Fig. 4.5, and if 14 keV gamma-rays are employed (from Co-57 for instance), then one can achieve an improvement in the SNR of roughly 6 times (cf. Fig. 4.6).

The predictions embodied in Fig. 4.3 - Fig**.** 4.5 are anchored in experiments, in which room-temperature empirical values of the preamplifier noise and leakage current are utilized in the calculations. If the preamp noise can be quenched, through either advanced design or in preamplifier cooling on a spacecraft platform, then greater degree of SNR improvement are possible across all ranges of energy depositions.

As shown in Fig. 4.5, if the multiplication exceeds several hundred, then the SNR diminishes across all energy depositions because of greater multiplication noise. In our designs, we generally designed the structures to maximize the SNR in the 10 – 100 keV range for ease of feasibility probing, and therefore target an M of 10 or 20, values at which the SNR is improved across all energy ranges, and is about an order of magnitude better for the 1 – 100 eV region.

If the avalanche diode can thus be simply fabricated, then there can be a substantial improvement in our ability to characterize the particle flux if on-chip amplification is utilized.

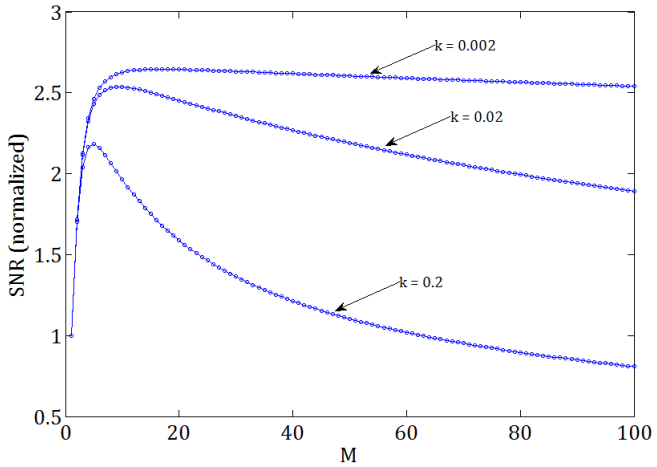


Fig. 4.6. For an energy deposition of 81 keV, the variation in the SNR at multiplication M relative to that at M = 1 for various excess noise factors k, assuming electron injection into the multiplication junction.

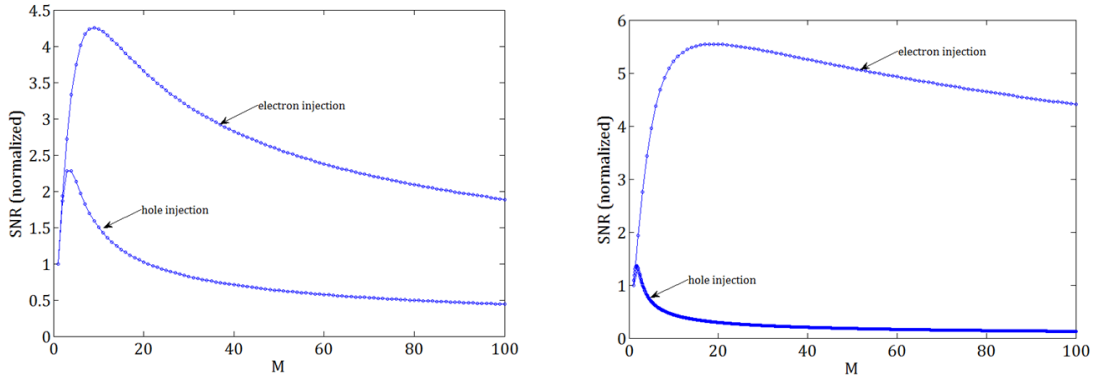


Fig. 4.7. For a 14 keV energy deposition, the sensitivity of the SNR improvement to the polarity of the charge that drifts into the multiplying junction for an excess noise factor k of (a) 0.2 and (b) 0.02

When contemplating the design of the APaD, we must first select the doping of the underlying substrate, which impacts the ease with which it is depleted as well as the direction of current flow. In silicon, electrons drift about three times as fast as holes (if below their saturated velocities), and they can therefore be accelerated to the energy needed to ionize secondary charge more easily that holes, an effect embodied in the ionization coefficient. Thus, one generally designs the diode such that electrons are drifted into the multiplying region. The marked effect of the injection polarity on the degree of SNR improvement is shown in Fig. 4.7b, particularly if the diode is designed with low k. We therefore choose a p- substrate, with as high of a resistivity as possible, in which electrons are drifted into an n+ junction.

4.3 Detector Modeling and Fabrication

4.3.1 Device simulation

Fig. 4.8 shows the results of a calculation for the electric field for various doping concentrations (on the low part of the junction) as the bias is applied. For our design, we wish to achieve breakdown just above the voltage needed to fully deplete the underlying high-resistivity wafer, which occurs from 70 – 100 V, because higher applied voltage merely increase the leakage current in the device. As indicated in Fig. 4.8, the doping concentration needed to have a breakdown field of 100 V is 3×10^{15} cm^{-3} if the underlying depletion region is thin or comparable

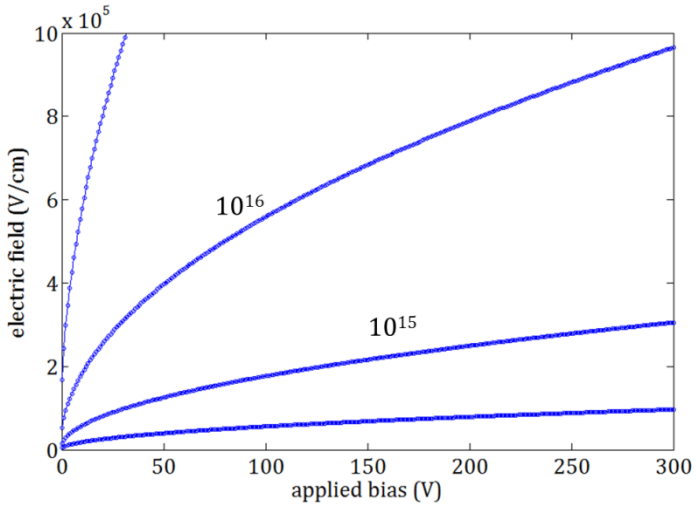


Fig. 4.8. Variation in the electric field at the junction as the bias is varied, for various boron (p) doping concentrations, assuming an n-doping (phosphorous) of 10^{19} cm^{-3}.

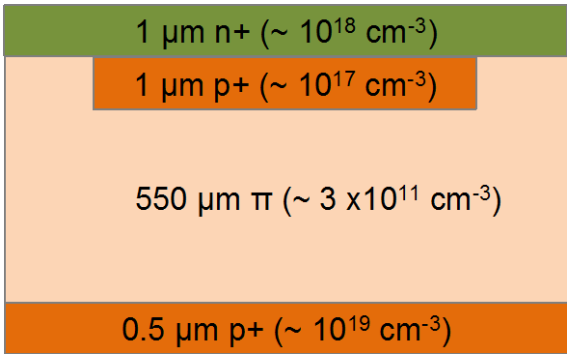


Fig. 4.9. Analytical layer design for avalanche radiation diode.

to the junction thickness. If the wafer is 550 μm thick, then the p+ concentration should be 1×10^{17} cm^{-3}. Such calculations result in the baseline design of Fig. 4.9, from which numerical simulation can validate the design.

Note in Fig. 4.9 that the bottom p+ layer has two purposes, first as an ohmic contact layer for the bottom metal (Cr/Au) electrode, and second, we make the p+ layer polycrystalline in order to serve as a sequestration layer during ionic-impurity gettering. The n+ layer is also extended beyond the p+ layer in order to realize a junction termination extension (JTE) design, recalling that the field at the n+/p- interface is much lower than that at the n+/p+ layer, thus confining the highest field region to the interior of the n+/p+ junction. This analytical n/p junction design analysis can

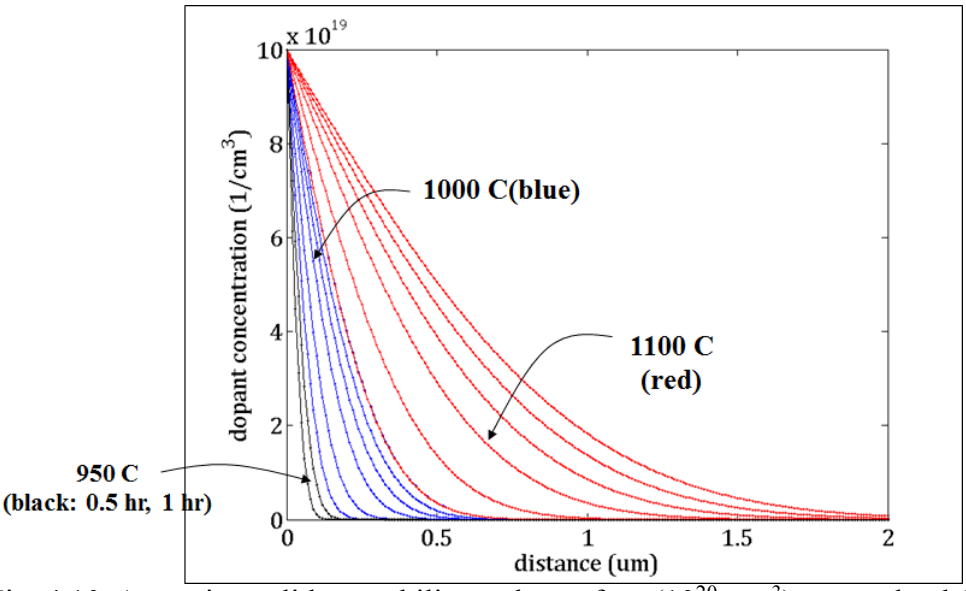


Fig. 4.10. Assuming solid saturability at the surface (10^{20} cm^{-3}), as can be delivered by a solid-target source, the boron diffusion profile after a diffusion of 0.5, 1, 2, 3, 4, and 5 hours for three different temperatures.

be buttressed by numerical simulations, which can provide guidance on the corner behavior and the process recipe needed to realize the JTE design.

One can predict the process sequence needed to make a particular design analytically. For instance, if we wish to make a thin p+ layer that minimizes dead-space losses, then diffusion calculations such as that shown in Fig. 4.10 can be employed to tell us the time and temperature needed to realize a particular profile. However, numerical simulations provide direct guidance on the three-dimensional behavior of the device upon changing various design parameters. For instance, Fig. 4.3 shows that the junction termination extension design of Fig. 4.9 does produce the highest fields at the p+/n+ interface (right figure), as desired, rather than at the n+/p- corners (left figure). As shown in the left figure, the field is higher at the corners and edges than the middle, but it is highest at the buried junction, across which breakdown can occur.

We conducted semiconductor fabrication process simulations using the Sentaurus Process Simulation Toolkit in order to estimate the key parameters for the real device fabrication. In order to create the doping profile of interest, one can implement a) gas or vapor deposition and diffusion, b) implantation, and c) implantation followed by the diffusion process. We used the simulations to predict the proper parameters for the implantation/diffusion processes.

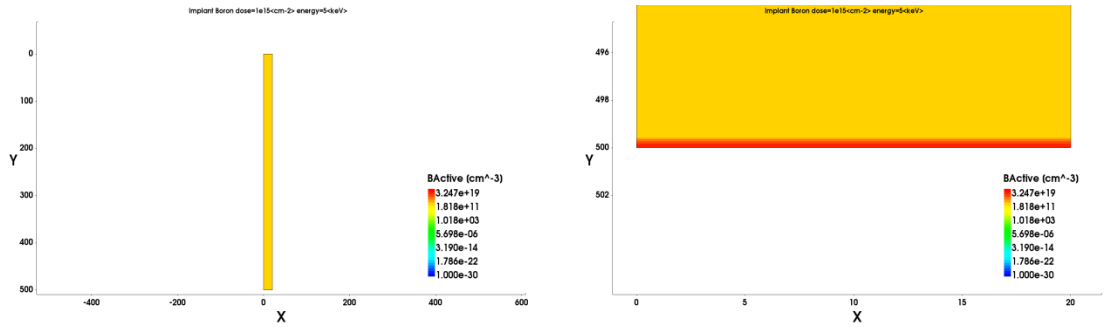
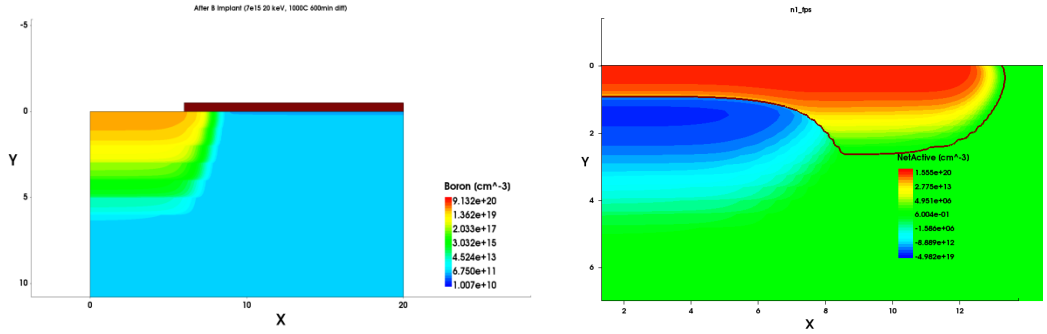


Fig. 4.11. Sentaurus process simulation result of boron implantation and diffusion on the back side of the p-type wafer.



(a) **(b)**

Fig. 4.12. Sentaurus process simulation result showing (a) boron implantation and diffusion and (b) phosphorus implantation and diffusion process on the front side of the p-type wafer.

We implemented fabrication parameters for the backside p+ region, which extends ~0.5 µm into the p-type wafer. After varying several parameters for the implantation and the follow-up diffusion, we found, as shown in Fig. 4.11, that a boron dose of 10^{15}/cm^2 with 5 keV energy followed by a 300 minute diffusion process at 800 ºC will create ~0.5 µm-deep p+layer on the surface.

Fig. 4.12a shows the deposition and diffusion of p+ boron on the front side of the wafer. We used 7×10^{15}/cm^2 dose of 20 keV boron to implant the boron layer and had it diffused at 1000 ºC for 600 minutes. The brown region on the top of the simulation area is oxide to mask the doping region. In this simulation, boron was doped in the area between the 0 and 6 µm, and phosphorus was doped in the area between 0 and 12 µm region to form the n+ layer. Fig. 4.12b shows the simulation result after phosphorus doping, achieved by the implantation of a 1×10^{16}/cm^2 dose of 14 keV P, followed by 120 min diffusion at 1000 ºC. Note that the phosphorus layer slightly flows

over the boron layer when the substrate is reprocessed with the phosphorus doping, which is modeled in the device simulation. The dark line in Fig. 4.12b shows the junction boundary.

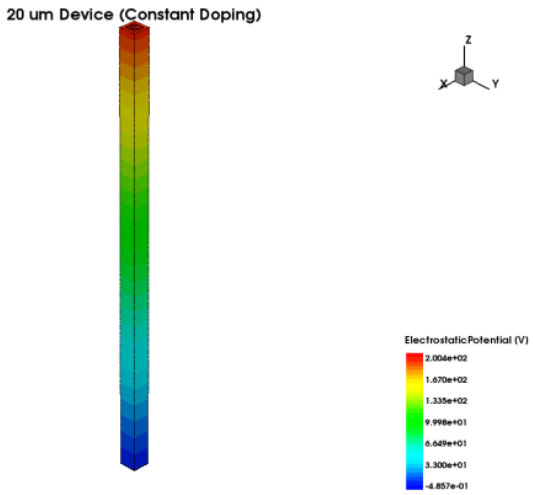


Fig. 4.13. Electrostatic potential distribution on the device when 2300 V bias is applied.

Based on the prototype design for the silicon sensor with multiplication, we performed the semiconductor device simulation using the Sentaurus Device Toolkit. We first modeled the analytical design, in which each n+ and p+ layer was assumed to have a constant doping profile, and the device size was assumed to be 20 × 20 μm to reduce the computation time. Note that this lateral size restriction does not negatively impact the evaluation because the edge and central field evaluations are relevant for a larger sensor as well (1 × 1 cm for instance). The depth of the device was assumed to be 500 μm, modeling a typical silicon wafer. The doping profile of the simulation is shown in Fig. 4.2. It shows the 3D view of the doping configuration and the y-cut view at the center of the device, in which a 6 μm wide p+ layer exists up to 5 μm depth, which is topped by 12 μm wide n+ region, reaching down to 1 μm depth. The backside of the wafer was also deposited with a p+ layer, which is illustrated as a bottom region of the device. The shape of the device was assumed as a square, a good shape for close-packing of diodes but a challenge for electric field concentration.

Using the simulation geometry shown in Fig. 4.2, we calculated the electric field profile, the electrostatic potential configuration, and the electron current density distribution in the device. Fig. 4.2 shows the electrostatic potential configuration in the device when the top contact is applied with 200 V bias. The gradient of electrostatic potential is uniformly distributed along the z-axis, as desired, induces charge drift toward the multiplication junction, the fields about which are shown in Fig. 4.3, repeated from Fig. 4.12 above, showing that the highest fields are confined to the n+/p+ interface and slightly less at the corners, implying that even for square structures, the JTE design can be effective.

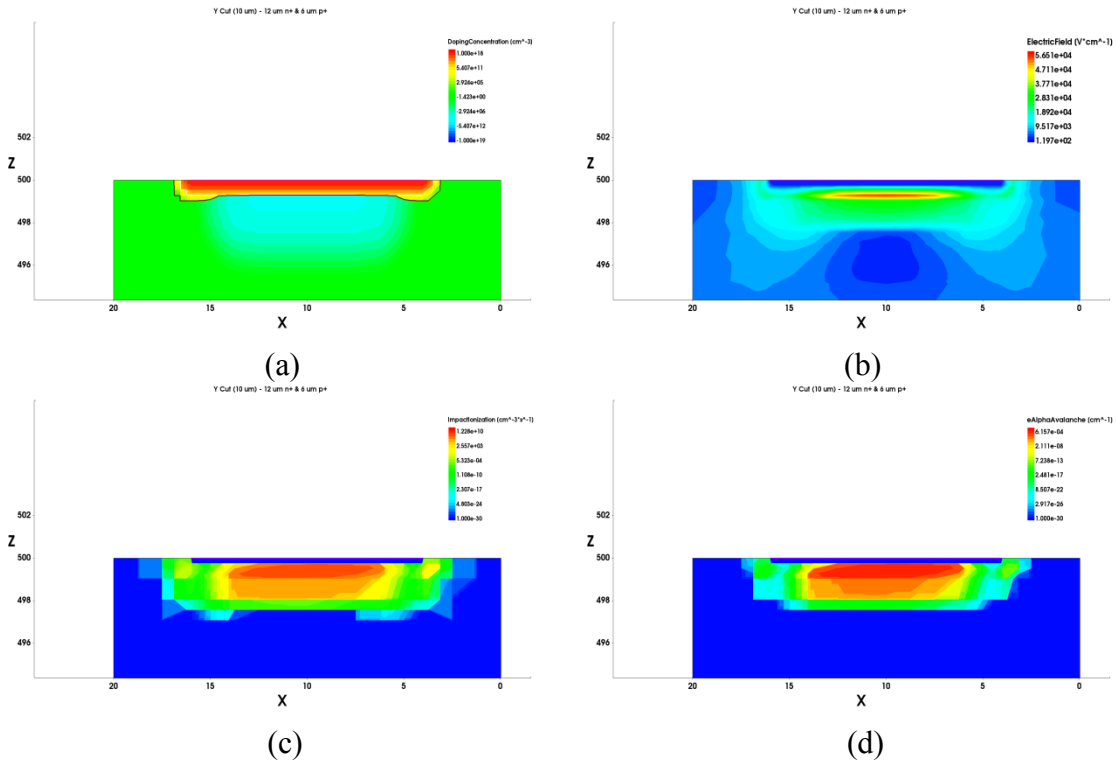


Fig. 4.14. For the 12 µm n+ layer/ 6 µm p+ layer square shape device at the center of the device, the cross-sectional view of the: (a) doping concentration, (b) electric field, (c) impact ionization rate, (d) electron avalanche coefficient profile with the bias voltage of 200 V.

In order to more realistically model the device, we used a Gaussian doping profile on each n+ and p+ layer, but the shape of the device was maintained as a square and the size of each layer was the same, inorder to solely see the effect of the Gaussian doping profile. The 3D profile is dissected at the center of the device, as shown in Fig. 4.14a. The figure shows the configuration at the junction between the n+ layer and p+ layer, which will act as the multiplication region in this device. The brown line in the figures shows the contour of the 3×10^{11} cm^{-3} region boundary, which we defined as a junction in the simulation. Note that the extended n+ region shown in process simulation is also considered in the simulation. Fig. 4.14b shows the electric field profile for an applied bias of 200 V. One can observe a higher electric fields at the n+ layer boundary region, and at the junction between the n+ layer and the p+ layer in the multiplication region. The maximum value of the electric field was 5.66×10^4 V/cm developed at the central junction area; however, the electric field of ~3×10^4 V/cm at the n+ layer boundary region was not negligible.

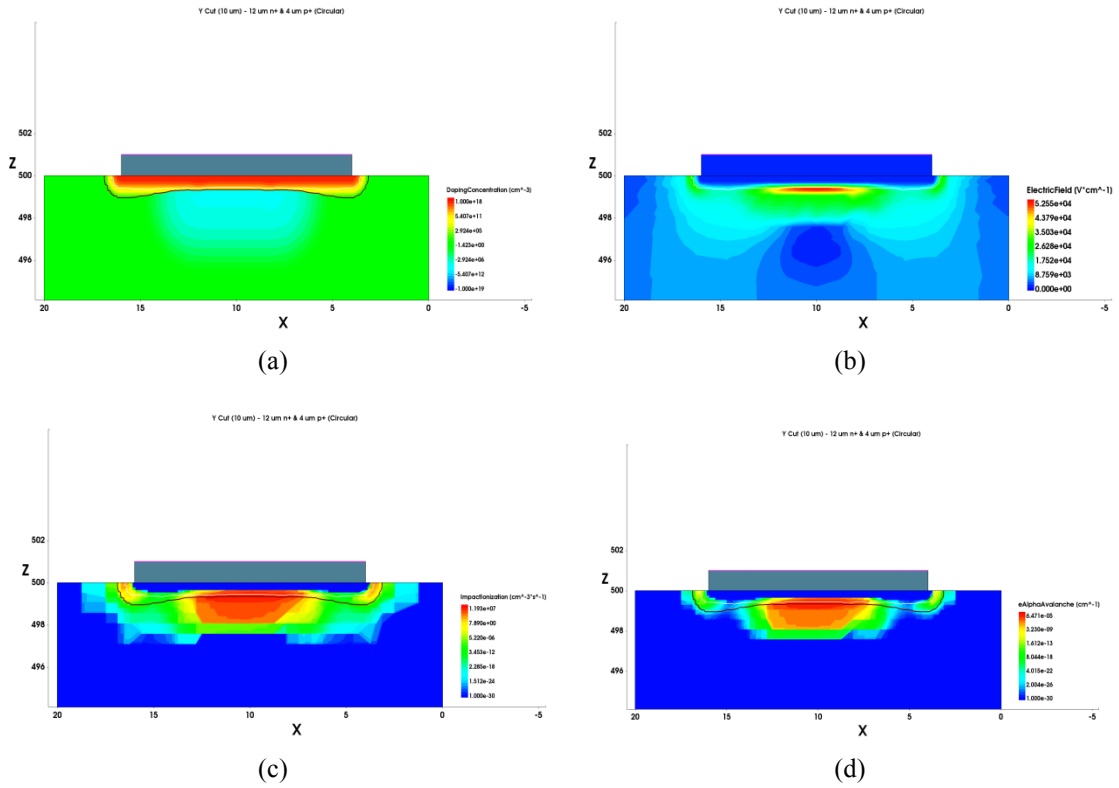


Fig. 4.15. For the 12 μm n+ layer/ 6 μm p+ layer circular shape device at the center of the device, the cross-sectional view of the: (a) doping concentration, (b) electric field, (c) impact ionization rate, (d) electron avalanche coefficient profile with the bias voltage of 200 V.

The simulation result confirms that a high electric field region can be developed even at junctions between gradual doping profiles. The impact ionization rate and the avalanche coefficient for electrons are displayed in Fig. 4.14c and Fig. 4.14d. One can observe a high impact ionization rate at the multiplication region which is many orders of magnitude greater than that developed at the corners of the diode.

From the simulation above, the devices suffered from high impact ionization rates at the corners of the square devices which can deteriorate the SNR of the device by increasing leakage current. We therefore sought to mitigate the high impact ionization (or avalanche) rate at the corner regions, while maintain a high multiplication effect at the n+/p+ boundary. After the change of the diode geometry into the circular shape, we examined circular multiplication regions, which exhibit much smoother doping profiles at the boundary, as shown in Fig. 4.15. The diameter of n+ layer was maintained as 12 μm and the diameter for the p+ region was defined as 4 μm. The results from

the electric field calculation at 200 V bias are shown in Fig. 4.15b. A high electric field of 5.26×10^4 V/cm was developed at the junction between the n+/p+ layers in the multiplication region, and $\sim 3 \times 10^4$ V/cm at the n+ layer boundary region. High electric fields at the corner regions are slightly mitigated, as one can tell from the impact ionization rate calculation shown in Fig. 4.15c. There is certainly lower impact ionization at the n+ layer boundary, compared with the center of the multiplication region between n+ and p+ layers. The effect of less relative impact ionization at the boundary region stands out more clearly in the avalanche coefficient calculation. Fig. 4.15d shows the result from the electron avalanche calculation. Compared with the square shaped devices, one can observe clearly less electron avalanche from the boundary region compared with the n+/p+ junction, which implies that if one is not tiling the devices, and thus concerned about fill factor, then the circular geometry is preferred.

4.3.2 Device fabrication

The nuclear-radiation sensors are fabricated with a PIN structure on a substrate of high-resistivity (> 10 kΩ·cm) double side polished <100> p-type boron doped 550 μm-thick 4" wafers, by using conventional microelectronic fabrication processes, which include oxidation, furnace doping, photolithography, dry/wet etching and sputtering. We chose p-type wafers since the electron mobility is almost three times faster than the holes in the material and therefore are more easily ionized.

The diagnostic diodes, shown in Fig. 4.16, consisted of 5 mm diameter n+ circles as the top layer, but the underlying p+ layer has 4 different sizes over the entire wafer. The largest p+ layer has 90% of the n+ top layer's diameter and the next largest one has 80%, 60%, and 40% in turn as shown in the figure.

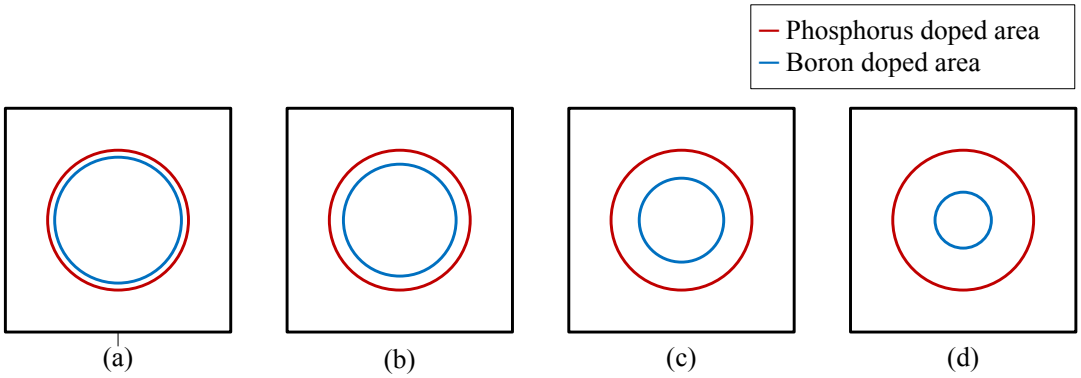


Fig. 4.16. Various diode designs with different boron doped area that covers: (a) 81 %, (b) 64 %, (c) 36 %, (d) 16 % of the phosphorus doped area respectively

The first process step is the deposition of a 500 nm polycrystalline Si layer on the bottom layer and boron is diffused and annealed for 45 min at 1000 ºC. Annealing is not only used for the drive-in but also for the gettering process. Impurities are diffused toward the bottom side of the wafer and trapped by the grain boundaries of the poly-Si., thus reducing interband carrier transition and concomitantly, the leakage current.

Four wafers were initially processed identically except for the top n+ and p+ layers, as shown in Table 3. Since it is a challenge to control the junction depth and the concentration of the buried P+ layer, two different doping techniques—the ion implantation method and the gas diffusion methods—were adopted to assess which one can make the most controlled p+ layer.

In detail, each wafer is processed differently, as shown in Table 3, although all were intended to produce the desired doping densities at the n+/p+ interface. Boron implantation is executed on wafer number 1 for the p+ buried layer and the following phosphorus implantation following phosphorus implantation forms

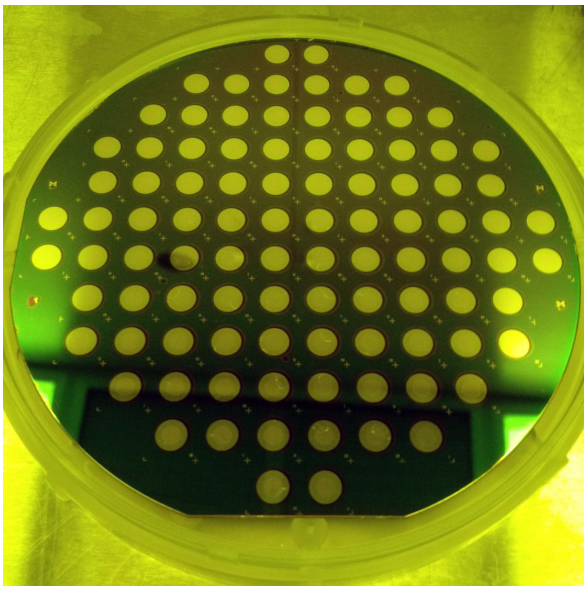
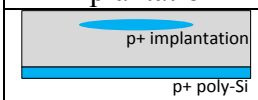
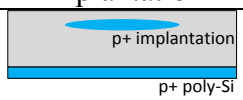
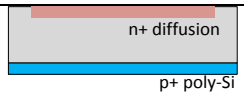
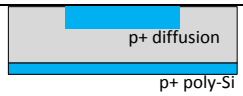
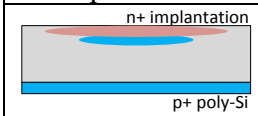
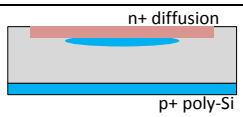
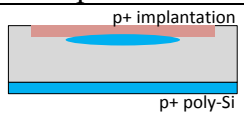
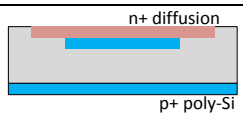


Fig. 4.17. Process finished wafer

Table 3. Example process variation chart for the top n+ and p+ layers

	Wafer #1	Wafer #2	Wafer #3	Wafer #4
1st doping	Boron Implantation	Boron Implantation	Phosphorus Diffusion	Boron Diffusion
				
2nd doping	Phosphorus Implantation	Phosphorus Diffusion	Boron Implantation	Phosphorus Diffusion
				

the n+ layer at the near surface. The boron implantation process as the first step is the same as that on wafer number 2, but the second n+ layer doping is performed by phosphorus gas diffusion. In contrast to other wafer processes, the top n+ doping is done prior to the p+ layer on the wafer number 3 by phosphorus gas diffusion. The p+ layer boron doping is implemented by an implantation technique through the already doped n+ top layer. Wafer number 4 is processed only with diffusion processes. The buried p+ layer doping is deposited via a boron diffusion process with a longer time in order to produce a deep junction depth. However, the phosphorus diffused n+ layer takes relatively short times to produce a shallow junction depth. After the top two layer doping process, all the wafers experience identical metallization processes. After the patterning with photoresist (PR), 3000 Å of Al is deposited with the electron beam evaporator on the n+ layer, and 50 Å of Cr and 3000 Å of Au is deposited on the bottom side. The completed wafers are shown in Fig. 4.17.

4.4 Device performance testing

From the fabricated device, we observed alpha particle signals and distribution with a ^{241}Am source to test the nature of the device behavior. The main peak corresponding to the ^{241}Am 5.5 MeV alpha particle energy deposition underneath the center part of the diode is shown in Fig. 4.18 at various low bias voltages. The slight shift in the peak is due to the increasing reach of the depletion region toward the surface, which decreases the dead layer as well as the diode capacitance, both of which result in a larger pulse amplitude, because the voltage, V, is equal to the integrated charge, Q, divided by the system capacitance, C, which includes the detector capacitance, the preamp feedback capacitance and any parasitic capacitance. The minor shift shows that the depletion region extends into the p- bulk beyond the range of the alpha particle (~28 μm in Si).

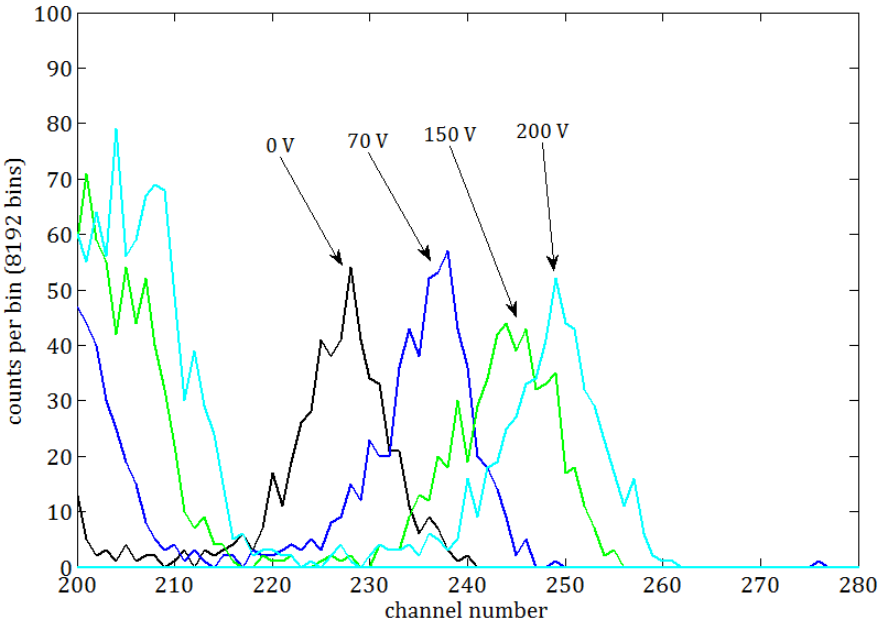


Fig. 4.18. For the detector shown in Fig. 4.17, the shift in the central-diode ^{241}Am (5.5 MeV) alpha-induced peak as the reverse bias voltage is varied as indicated by the arrows.

As is apparent from the peak shifts, the nature of the gain doesn't increase in a manner consistent with avalanche breakdown until the voltage is increase to above 800 V, as shown in Fig. 4.19. Specifically, the alpha particle deposition produces the shape similar to that shown in black, corresponding to 0 V in Fig. 4.18, all the way to 800 V. Note that the lower amplitude bulk distribution is due to edge energy-depositions, for which the charge transit is slower due to lower edge field. What is important is that at 1500 V, the edge pulse increase in amplitude such that a distributional shape change occurs and the amplitude begins to shift to the rightward with greater device gain. For instance, Fig. 4.20 shows the difference in the peak pulse amplitude between the 70 V case (silicon fully depleted) and the 3000 V case (avalanche gain apparent); specifically, the preamp pulse amplitude, which is a direct measure of the integrated charge, increases from 141 mV to 235 mV. The onset of avalanche gain is also apparent in Fig. 4.21, in which the alpha-peak channel number is plotted, normalized by the peak channel position measured at 0 V. From that plot, the increase in the relative peak height is gradual and consistent with dead layer thinning below 1500 V, and it then increases in a large fashion consistent with avalanche multiplication above 1500 V.

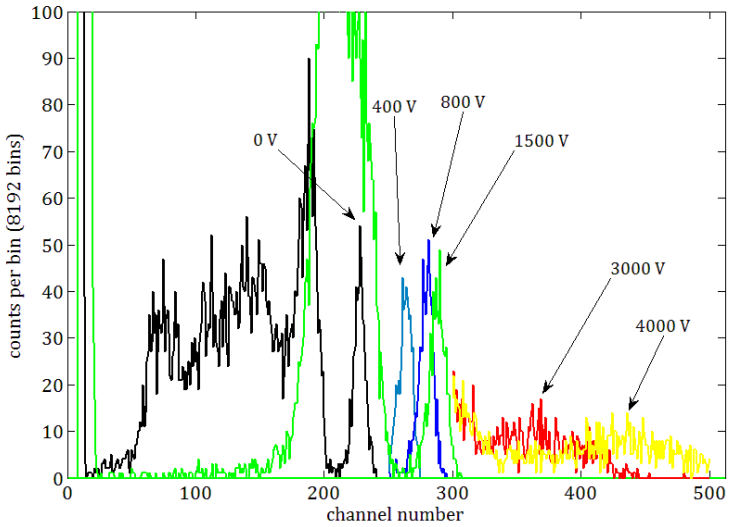


Fig. 4.19. For the detector shown in Fig. 4.18, the shift in the central-diode 241Am (5.5 MeV) alpha-induced peak as the reverse bias voltage is varied as indicated by the arrows. For the 400V, 800 V, 3000 V, and 4000 V cases, only the maximum alpha feature is shown, for the sake of clarity.

As mentioned above, this is positive for the APad development because the sensor is acting as predicted, when low ion implantation densities are deposited. One can now safely step the ion implantation density up until the breakdown occurs to somewhere near or below ~100 V and expect that energy-depositions can still be measured. Note that the 3×10^{15} cm^{-3} density was realized in only 28 sec of implantation time and therefore reaching the desired 10^{17} cm^{-3} level is not problematic.

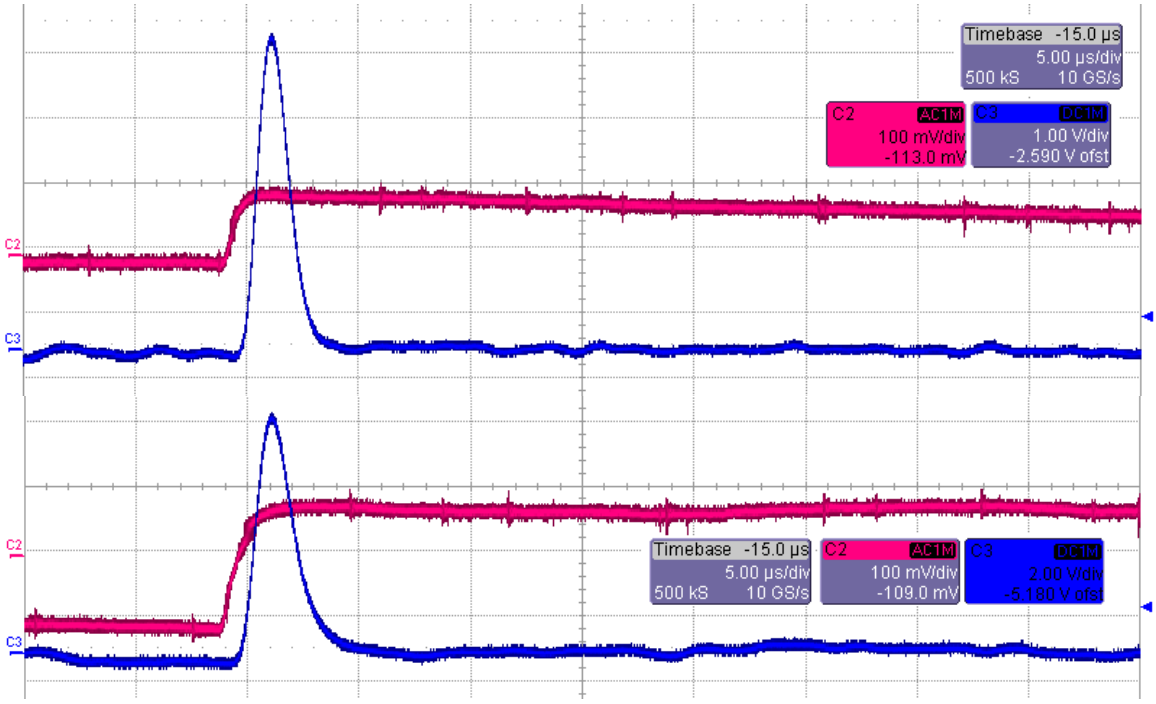


Fig. 4.20. Charge-sensitive preamplifier (in pink) pulses and shaped amplifier (in blue) pulses derived from n+/p+/p-/p+ detector biased to 70 V (top) and 3000 V (bottom). Note that the top preamp pulses is 141 mV while that at 3000 V is 235 mV, indicating that appreciable gain is produced at voltages above 1500 V.

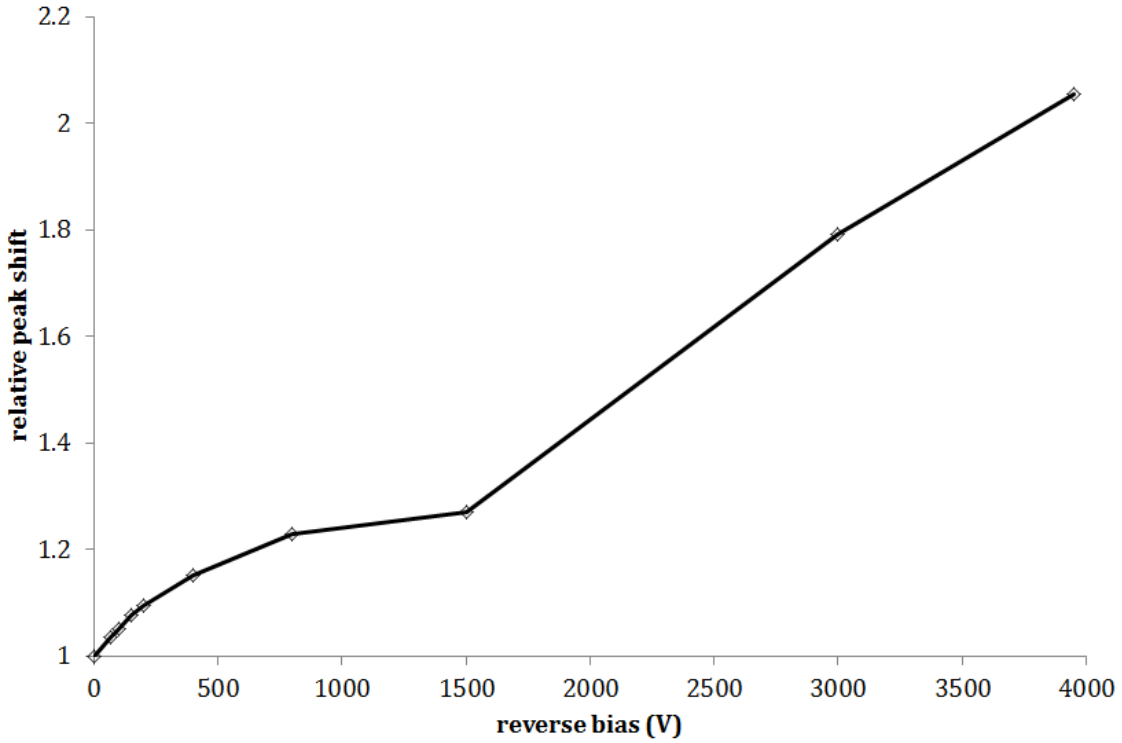


Fig. 4.21. When normalized by the alpha peak height at 0 V, the shift in the normalized peak height as a function of bias voltage. The nature of the increase changes from a change consistent with dead-layer thinning below 1500 V to avalanche gain above 1500 V.

Results such as these, generated from the first batch of the process, provided an experimental connection to the device modeling and the theoretical predictions; however, the challenge is to realize high doping in thin layers in order to realize higher amplitude gain at lower voltages. Furthermore, we are always focused on developing process solutions that do not compromise the low-energy sensing capabilities of the detector; that is, we desire dead layers that are as thin as possible. We used spreading resistance profiling to measure the effect of various doping recipes, such as that shown in Fig. 4.22, which shows the typical profile delivered by our phosphorous diffusion furnace.

As shown in the figure, the n+ diffusion extends over 0.5 μm, which is thin but for ion sensing, one would prefer the even thinner layers that result from ion implantation or metallic contacts. For instance, the range of a 10 keV proton or alpha particle in silicon are 0.13 μm or 0.11 μm, respectively. Extending the sensing range to 1 keV requires dead layers much smaller than 10's of nm, which is challenging given the intrinsic oxidation of the surface. Thus, one has to employ delta doping layers or thin metallic layers to electronically serve as the doped layers in the electric field profile. We demonstrated both techniques, building 0.1 μm Al/0.1 μm p+/p detectors as well as thin ion implanted layers.

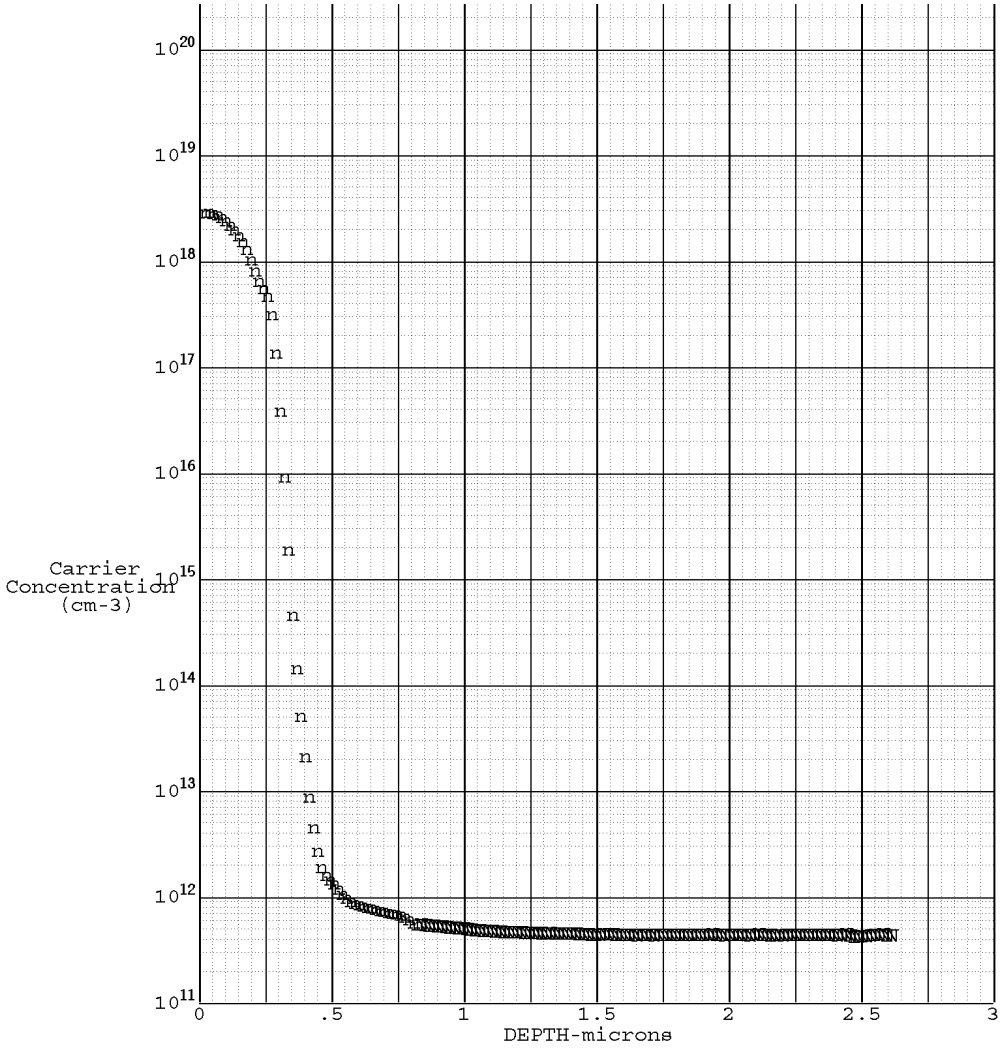
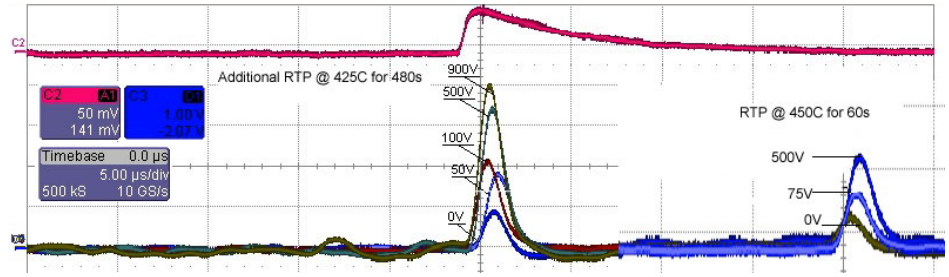
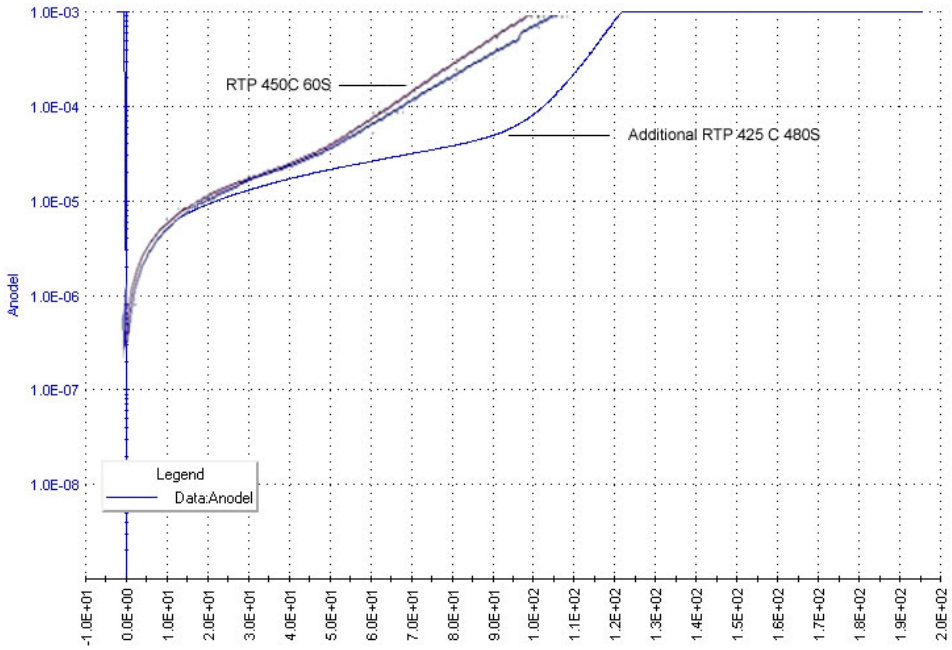


Fig. 4.22. Phosphorus doping profile as obtained using spreading resistance analysis (performed by Solecon Labs). Although the boron was implanted at this stage, because of lack of activation, the carrier concentration plot does not reflect its presence.

The first experimental challenge is to implant or deposit enough dose to realize high device gain. We used the Ion Beam Laboratory at the University of Michigan as well as a commercial ion implantation source, finding that the latter was less expensive and better characterized. Once the implantation does is delivered, one must then optimize the recipe to electrically activate the dopants in the silicon matrix, an annealing process that also reduces the damage that is incurred during implantation. Fig. 4.23 shows the general trend that accompanies annealing (rapid thermal



(a)



(b)

Fig. 4.23. (a) the increase in the gain, as reflected in the shaping amplifier pulse size as induced by 4.0 MeV alpha particle, as the annealing time is increased. (b) The reduction in the noise and sharpening of the electric field transition, as reflected in the current, as the annealing time is increased. The FZ p-type silicon detector has a n+ diffused and p+ implanted contact on a 550 µm substrate.

annealing or RTP in the figure). Specifically, the shaped pulses in Fig. 4.23a show the general trend as the bias is increased, as indicated in the figure, from 0 V to 500 V and beyond. Note for instance that additional annealing (leftmost collection of pulse) results in a greater gain from 0V to 50 V, then that exhibited from 0 V to 75 V (rightmost pulses), by the sensor prior to only 8 minutes of low-temperature annealing. Furthermore, as shown in the IV curves of Fig. 4.23b, even short-term, low-temperature annealing can impact the noise and electric field configuration.

Finally, one can control the onset of the breakdown by utilizing the high doping of diffused layers, but using the energy level of the bounding metal as a stand-in source of charge carriers. For instance, an aluminum contact on a p+ diffusion can be realized to deliver high fields and avalanche breakdown at lower voltages than the 1500 V shown in Fig. 4.21 above.

For instance, Fig. 4.24 shows the IV curve from an APaD (550 μm thick) that breaks down at 170 V and has relatively low noise. As shown in the multiplication gain (M) curve of Fig. 4.25, high device gains can be realized, but more important for our design, in which we desire an M of roughly 20 rather than 1000, the voltage shift near the desired excess bias shifts only gradually, allowing one to control to breakdown gain. On the downside, the pre-breakdown dark noise is

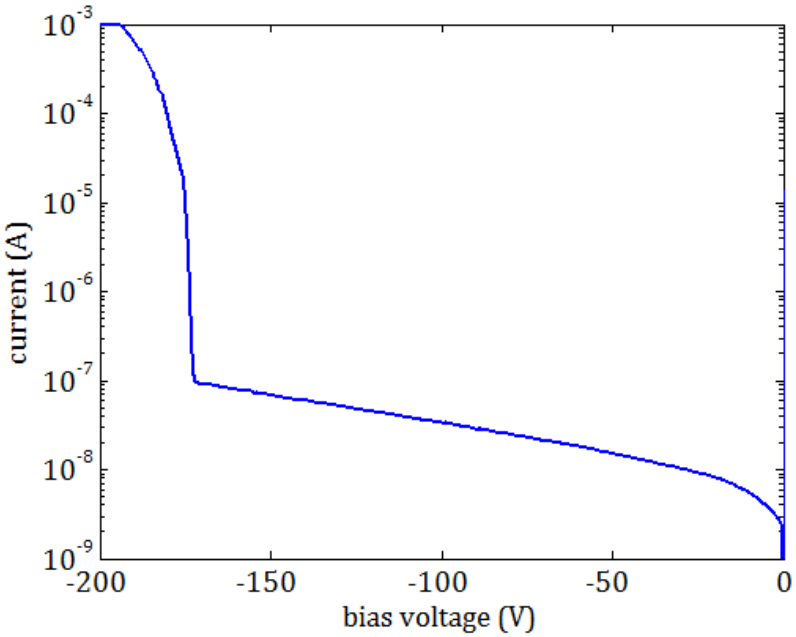


Fig. 4.24. Reverse bias current-voltage (IV) characteristic for thin Schottky/p+/p- junction devices (diffused boron) 550 μm-thick high-resistivity that are then annealed in forming gas at 600 ºC for 10 min, exhibiting relatively low noise and avalanche breakdown near 170 V.

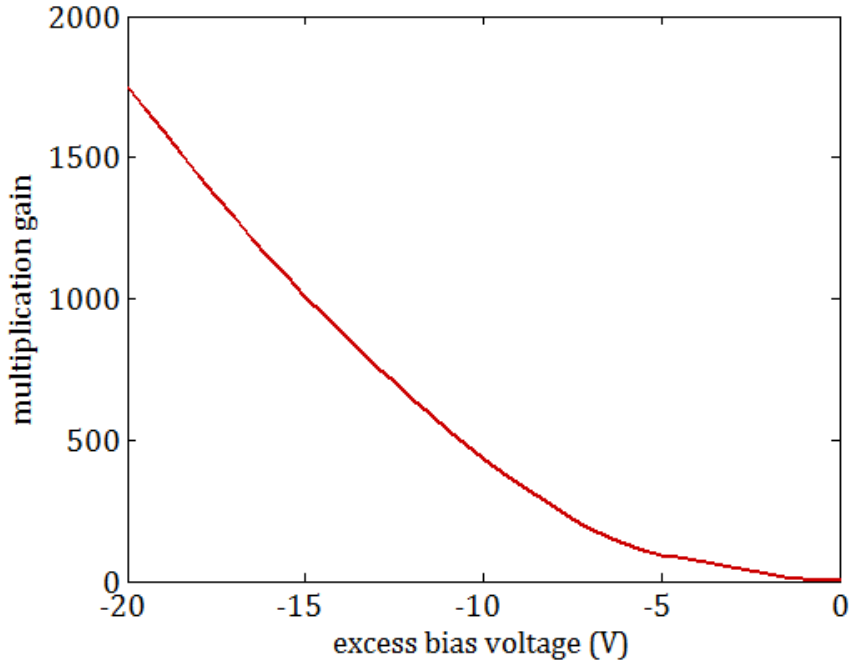


Fig. 4.25. Multiplication gain as a function of excess bias above breakdown (173 $V_{reverse}$)

below that which hampers the spectral measurement of high-energy ions (> ~10 μA introduce substantial noise), but the 100 nA can make low-energy photon detection imprecise, such that gamma-ray peaks are not discerned. We therefore desire lower noise as well as lower breakdown bias, so that the leakage current is minimized.

In order to establish the recipe that delivers the desired doping profile, we endeavored to solve one problem at a time, by using a substrate with a fixed relatively-high doping concentration. Specifically, instead of a high-resistivity (> 10 kΩ·cm) p-type substrate, we purchased low-resistivity (1-10 Ω) 200 μm thick p-type silicon, which yields a substrate boron doping of 10^{15} – 10^{16} cm^{-3}. Upon that substrate, we deposited a metalized n+ layer, which was deposited via either diffusion of implantation. The resulting devices exhibited avalanche breakdown near 40 V, as desired, as shown in the IV curve of Fig. 4.26 and the multiplication gain curve of Fig. 4.27.

As shown in the multiple trace of Fig. 4.26, the breakdown was reproducible, and the gradual rise in the current results in a multiplication gain that is easily controlled through the excess bias, as shown in Fig. 4.27. Specifically, for our targeted internal gain of 10 – 20, the excess bias must be raised to roughly 3 V. In Fig. 4.26, the pre-breakdown leakage current is high because of

the low substrate resistivity; however, if an equivalent amplification field can be applied on a high resistivity substrate, then low noise and gain can be produced.

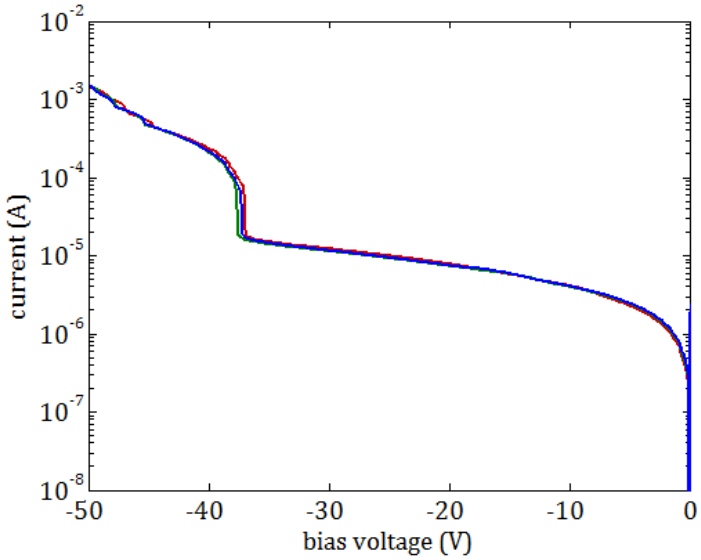


Fig. 4.26. Reverse bias current-voltage (IV) characteristic for np-junction devices (10^{20} P/cm^3 on n side, ~5 × 10^{15} B/cm^3 on p side), exhibiting avalanche breakdown near 40 V, as expected. The multiple traces are for repeated, reproducible measurements of the curve from the same die.

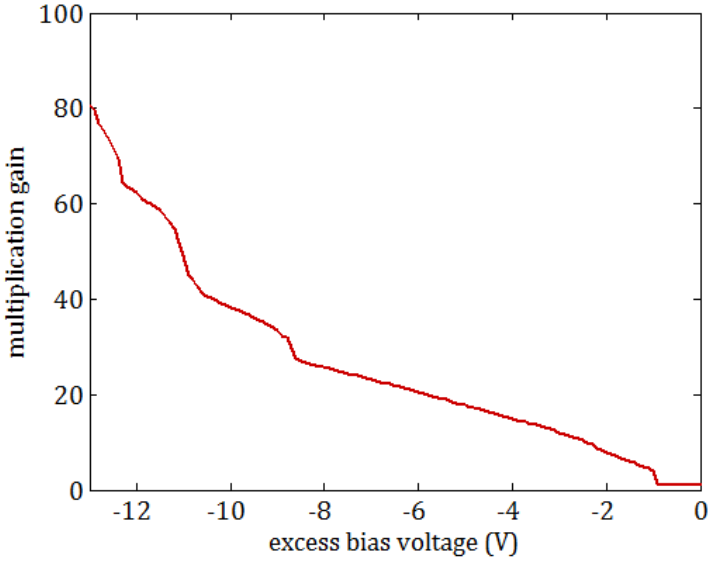


Fig. 4.27. Multiplication gain as a function of excess bias above breakdown (36 $V_{reverse}$), for np-junction devices (10^{20} P/cm^3 on n side, ~5 × 10^{15} B/cm^3 on p side).

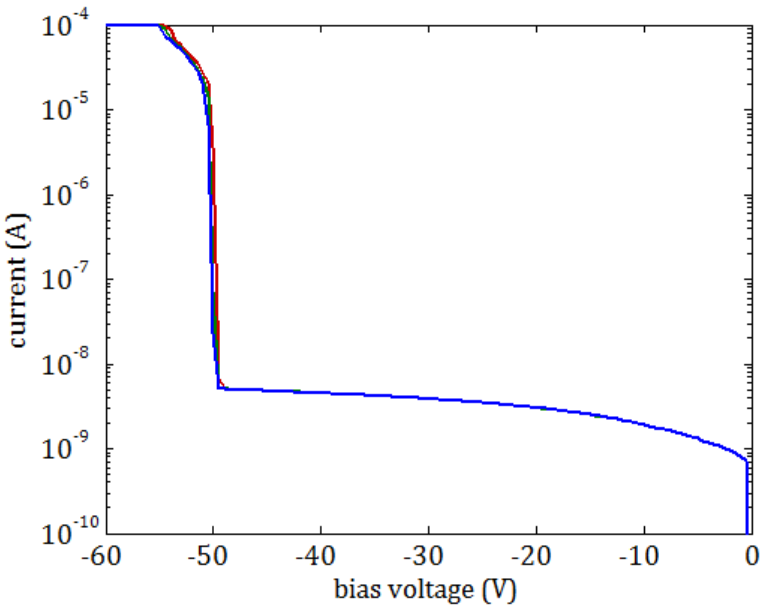


Fig. 4.28. Reverse bias current-voltage (IV) characteristic for Schottky/p+-junction 550 µm-thick high-resistivity device (diffused boron), exhibiting low noise and avalanche breakdown near 50 V. The multiple traces are for repeated, reproducible measurements of the curve from the same die.

Fig. 4.28 shows a resulting example, derived from one of the high-resistivity detectors, in which the aluminum contact served as the effective n-type layer upon a doped p+ region. As shown in the curves derived from repeated measurements, the pre-breakdown noise is less than 10 nA, and the multi-decade rise above breakdown results in high M-values as shown in Fig. 4.29. A leakage current of less than 10 nA results in high detector energy resolution, for which the preamplifier noise is a substantial contributor to the noise.

Using the experimental multiplication curve of Fig. 4.29, the spectra from the low-noise devices, and the results of the device simulation, we can demonstrate the effect that biasing the device above breakdown has on the spectral characteristics. In particular, Fig. 4.30 shows the81 keV peak from ^{133}Ba imaged at various excess bias. The black curve shows the spectral width when operated below breakdown, at 36 V. If the reverse bias is increased to 39 V, 3V above the breakdown voltage, then the blue curve results, showing a SNR improvement of 2.2 times, since the k of the diode is 0.2.

We would prefer a lower k value in order to minimize the excess noise factor and maximize the SNR gains that can be accrued, but the optimization of k and the excess noise factor

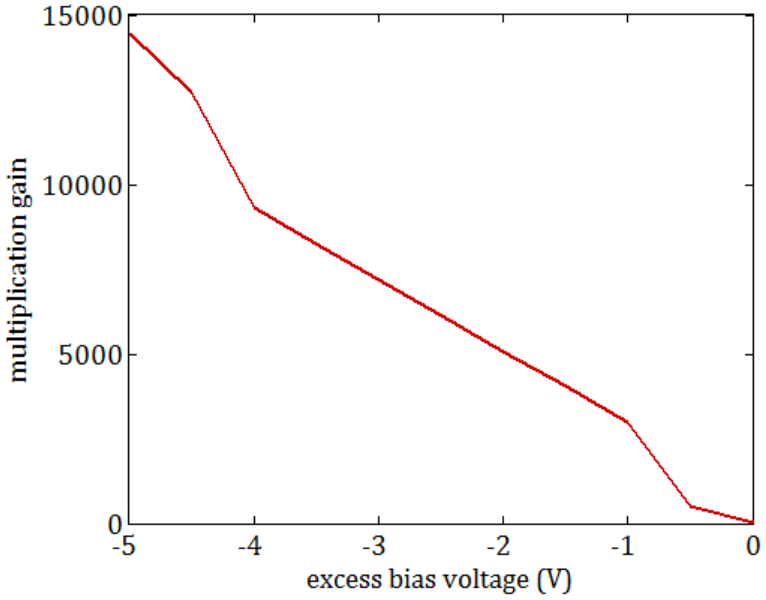


Fig. 4.29. Multiplication gain as a function of excess bias above breakdown (50 $V_{reverse}$)

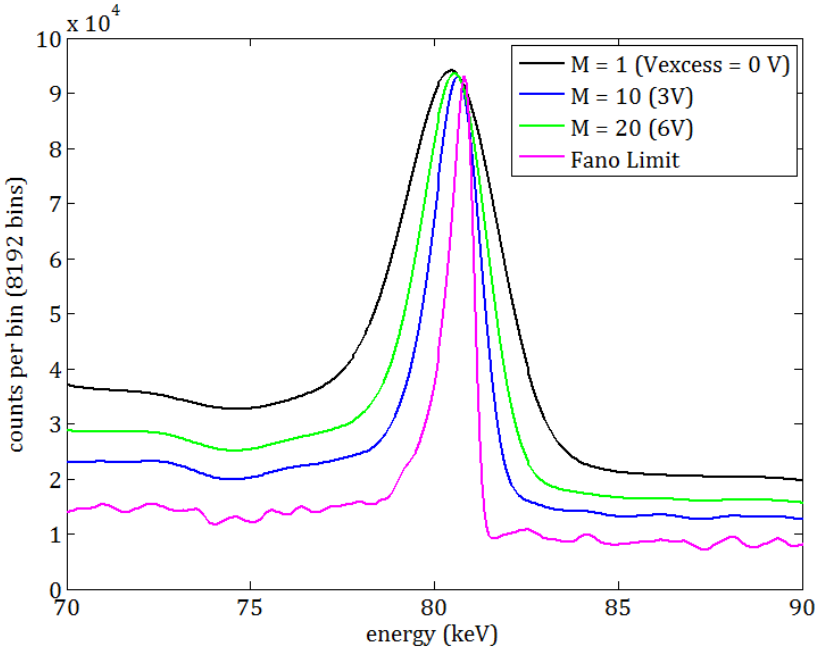


Fig. 4.30. Focusing on the 81 keV gamma-ray line of the ^{133}Ba gamma-ray spectra, derived from Au-bounded circular diodes Si PIN detectors, the variation in the peak shape as the applied bias is varied from 36 V (Vexcess = 0V), shown in black to 3V above breakdown (blue), to 6 V above breakdown (light green). The MCNP simulated ^{133}Ba gamma-ray spectrum is shown in pink, in which the peak is broadened by the Fano noise.

will be conducted on follow-up research. Our main focus was to show that a multiplying junction can be fabricated, which can result in device gain and improved SNR. Further increases in the bias result in lower SNR because the multiplication noise is substantial; hence the green trace at 6 V excess-bias is broader than the 3 V curve.

The ultimate theoretical limit of the resolution is shown in the last magenta curve of Fig. 4.30. The trace is derived from MCNP simulations of ^{133}Ba gamma-rays impacting a 550 μm thick silicon detector, broadened by the statistical counting noise that accompanies charge creation in a silicon substrate, assuming a Fano factor of 0.115 and a w value of 3.62 eV. In all of the spectral peaks, note that they tail slightly to lower energies because of secondary electron escape, an asymmetry diminished by using thicker detectors.

Chapter 5. Conclusions and Future work

5.1 Solid-state Photomultiplier

The active area of a silicon-based solid-state photomultiplier is dark-count limited, as governed by the material's relatively low band-gap (1.12 eV). Furthermore, the optical sensitivity of the material to the blue and near-UV wavelength bands is limited by the material's short absorption lengths and the accompanying near-surface carrier absorption.

We have shown that wide band-gap AlGaAs is responsive to blue and near UV in both linear and breakdown modes. Furthermore, the electrical characteristics, which include the leakage current and the onset of breakdown, are robust against geometric alterations in the diode design.

We investigated annealing as a means to extend the range of excess-biases over which breakdown pulses can be clearly recorded, but found only that the dark current is reduced by the process.

We also designed the anti-reflective coating with thickness control of the existing passivation layer and succeeded in minimizing the reflection at the range of interest (300 nm – 500 nm). Through the recessed window, we can eliminate the surface dead layer (the graded AlAs layer) and deleterious surface oxides and, therefore, improved the external quantum efficiency up to 50 % and internal quantum efficiency greater than 60 %, in the range between 400 nm and 470 nm. If we modify the anti-reflective coating, we can further increase the quantum efficiency.

For the continued development of the APD in an AlGaAs-based SSPM, what remains is to optimize the Geiger probability by adjustment of the layer structure. Currently we are studying the AlAs layer's effect on the optical response and the electrical noise.

5.2 Suppression of surface-induced noise

Although there exists a substantial body of literature demonstrating that the electronic noise in thin-film semiconductors, metals, and nanoparticles is connected to the lattice-vibrational modes of the solid, there has been only one published experiment [30] that took the next step, in which, for a given operating temperature (e.g. room temperature), one attempts to use the

geometric and material design of the interface to suppress the phonon distribution and concomitantly, the electron distribution via phonon-phonon and phonon-electron scattering. Furthermore, that experiment wasn't conducted with a material suitable for nuclear radiation detection nor was it well controlled against influences other than the phonon-leaking effect.

During this work, we established, first, that the current fluctuations in Si and other semiconductor devices are governed by a consistent variation out beyond 100 MHz; thus any mechanism that can suppress the flicker noise in the solid can improve the signal-to-noise ratio (SNR) of the radiation detector operating in either current mode or pulse mode.

Second, the data—derived from either material or area variation studies—was consistent with the prediction that the interface can be used as a sink for phonon-energy from which the charges' mobility fluctuations could be suppressed.

Finally, the degree to which the current noise could be reduced was found to be substantial, varying by several times to over an order of magnitude, depending on the nature of the contact variation. After all, even if the phonon-leakage mechanism was operational, if the leakage current was only reduced by 10% for instance, then it wouldn't be of particular interest to those wishing to transform the capabilities of radiation-sensing devices.

5.2.1 Molecular Dynamic Simulations with Metal Interface

For more clustered molecular dynamics simulation, we are currently investigating the degree to which modern parallel network using high performance computing (HPC) resources at the University of Michigan. We expect a speed improvement of one-thousand to ten thousand times compared with the serial-based desktop approach, with a goal of making large enough ensembles that one can project the performance to macroscopic detector configurations. For more applicable results to empirical data, interatomic potentials for the contact material cross-terms (e.g. Au-Si, Pd-Si) will be surveyed and applied to MD simulation.

5.2.2 Quenching the Thermally Generated Noise in HPGe via the Contact

Recall that as a first-order calculation of the effect of the contact on the noise, one can calculate the acoustic reflection coefficient, R_{sm}, from the semiconductor to the metal, and find those contacting materials that minimize the reflection. For germanium detectors, R_{sm} is shown in Fig. 5.1. Of particular note is a comparison between Cr and Ti, which have similar work functions (~4.4 eV) and therefore similar electrical junctions, but have disparate phonon-reflection properties, Cr producing the most effective communication with the environment.

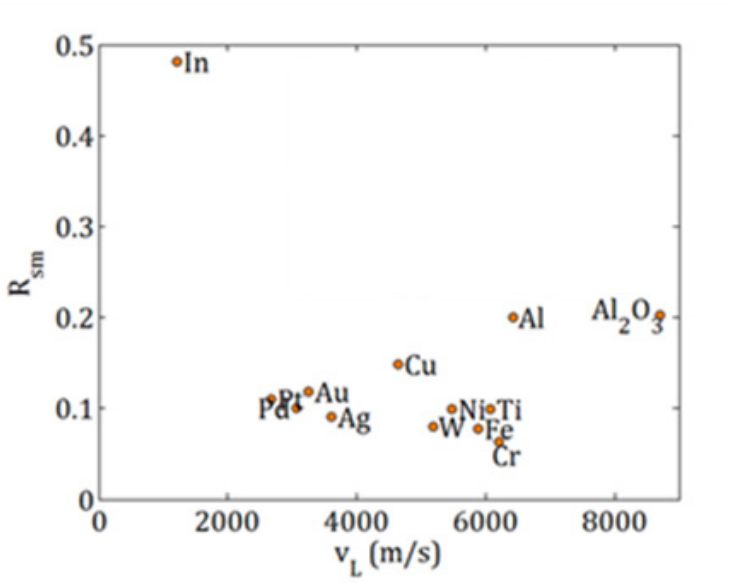


Fig. 5.1. Reflectance coefficient for various materials bounding Germanium. V_L is the longitudinal acoustic velocity of the material.

5.3 Particle sensor with on-chip amplification

In this research, we investigate whether enhanced energy resolution can be accrued via on-chip amplification for the > 10 keV energy depositions associated with nuclear radiation. Effective multiplication junction devices were designed, using semiconductor modeling and simulation software. We established that junction termination extension (JTE) designs can be employed to ensure that the avalanche field is confined to the broad middle of the detector. Finally, prototype devices were fabricated with thermal diffusion and implantation process and the

performance of the devices were investigated. In order to fully realize a particle-sensing prototype, the low-noise recipes and the avalanching detection platform must be optimized when coupled together, through design, fabrication, and test iterations, which we expect to conduct through the continuing research.

Appendix A. Silicon radiation detector fabrication process

For the silicon radiation detector, we used 4" high resistive (10 kΩ·cm) n-type double side polished wafers. Once a new wafer box is opened, all wafers are numbered with a tungsten-carbide (WC) scriber. Since all the wafers are not processed at the same time, an LPCVD oxide layer is deposited on both sides of the Si wafers to prevent contamination from any impurities in which the target thickness of the oxide layer is 5000 Å as illustrated in Fig. A.1b. At this step, the thickness of the oxide layer does not have to be exactly 5000 Å, but the following step can be affected by the oxide thickness—if the thickness is too thin, the oxide layer can't work as a mask from dopant diffusion process and if too thick, the undercut from wet etching process becomes significant and small features would not survive. Since 5000 Å is a compromise value for either of these faults in the process, we chose the thickness. Photoresist (SPR220 3.0) is spin-coated for the N-stop layer patterning which prevents the diverging electric field and terminates the junction at the edges of the detectors. After the patterning, the patterned oxide on the top and the whole bottom oxide is etched through BHF wet etching for 10 min. Through the exposed Si, phosphorous

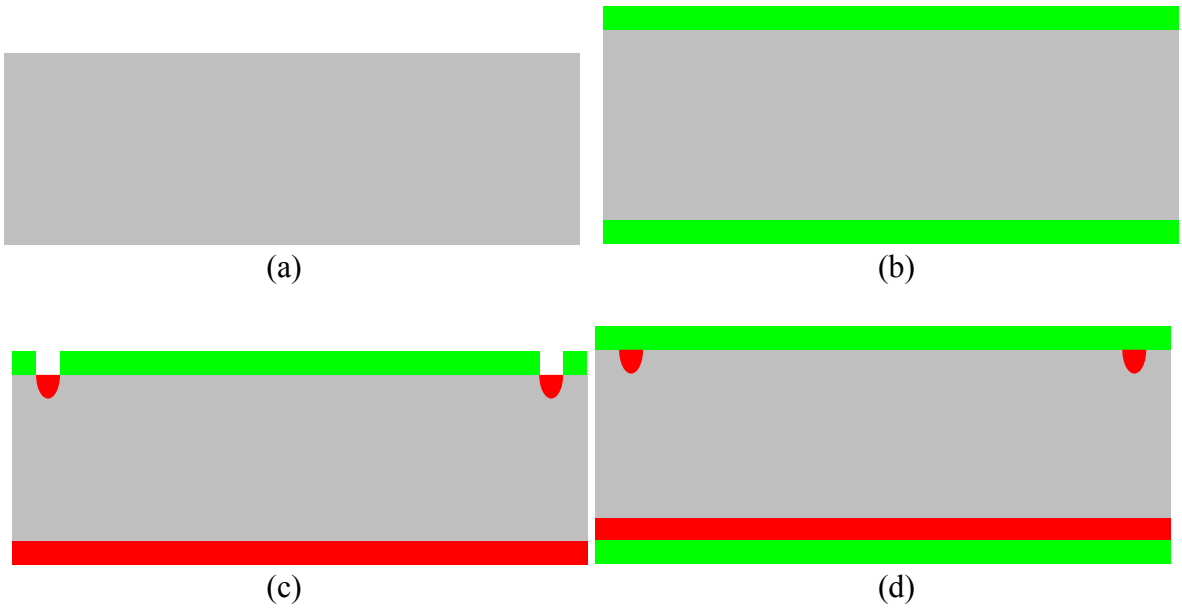


Fig. A.1. Silicon radiation detector processing chart. (a) High resistive N-type wafers. (b) Thermally grown oxide layer is deposited. (c) B^+ implantation after the selective oxide removal. (d) New oxide layer is grown.

is diffused for N-type doping at 950 ºC for 25 min as in Fig. A.1c. Once the doping process is finished, all the oxide is removed with BHF wet etching and another thermally grown oxide is deposited as depicted in Fig. A.1d, with thickness of 5000 Å, which is used as a mask for the following processes.

The next step is to spin coat photoresist, S1813. For the proper photoresist use, a thicker photoresist is selected for a larger pattern and thinner resist is used for smaller patterns because thinner layers, and therefore shorter diffraction wavelengths, reduced aspect ratios and a reduced minimum feature sizes are permitted. PR coated wafers are exposed with the guard ring mask which prevents the concentration of electric field lines at the edge of the detectors. B^+ is implanted with 40 keV of energy and 1×10^{15} of dose and activated through a following annealing for 60 min at 1100 ºC as indicated in Fig. A.2a. After the guard ring doping, the wafers are patterned with an active region mask. Active region is doped with BF_2 implantation with 50 keV of energy and 1×10^{15} of dose as illustrated in Fig. A.2b. Although the BF_2 implantation uses higher energy than the B^+ guard ring implantation, the doping profile shows a shallow junction depth because $^{49}BF_2$ is 4.46 times heavier than ^{11}B and the range implanted of boron in BF_2 is shorter than that of B.

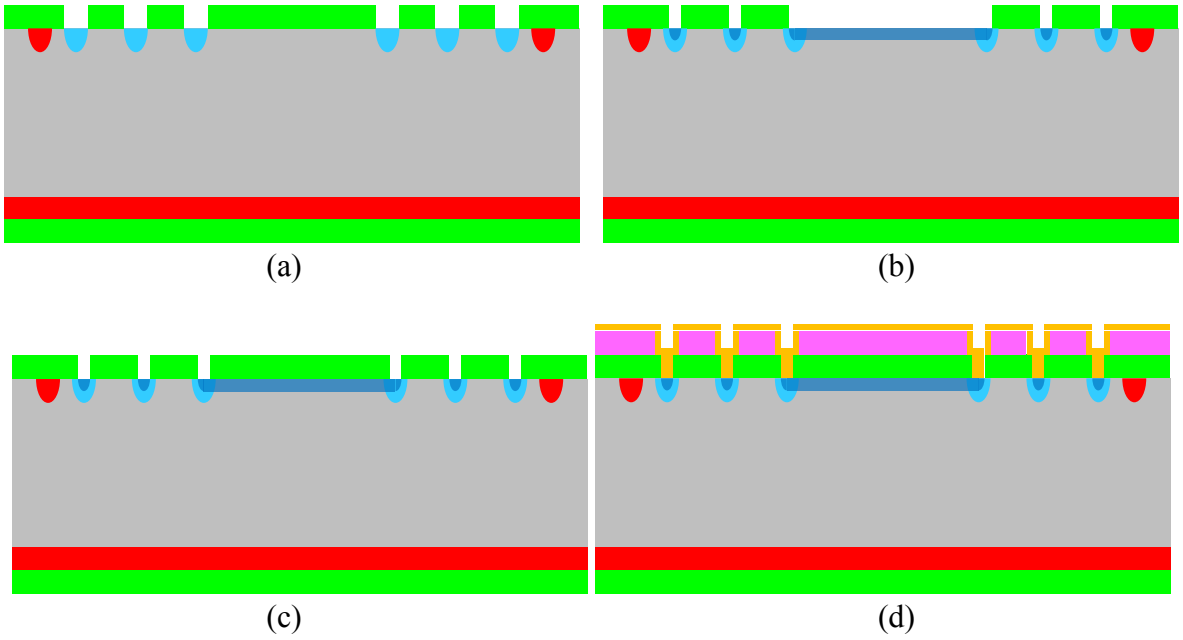


Fig. A.2. Silicon radiation detector processing chart. (a) Guard ring implantation with B+. (b) Active region implantation with BF2. (c) Contact hole etching after LPCVD LTO growth. (d) Metallization patterning with PR and metal deposition with TiW / Al / TiW.

Boron activation is executed by 900 ºC annealing for 30 min after the 5000 Å of LPCVD low temperature oxide (LTO) is deposited. Contact holes are patterned with photo resist (S1813) and they are etched out via the BHF wet etching process as in Fig. A.2c. Once the oxide in contact hole area is etched out, the wafers are patterned again for the metallization. The metal consist of TiW/ Al/ TiW for 2000 Å/ 6000 Å/ 700 Å is deposited with a sputter tool as shown in Fig. A.2d and which is patterned through a lift-off process. During the lift-off process, we can significantly reduce the time with heated acetone (which starts boiling if it is heated above 56 ºC) and ultrasonic agitation. PECVD oxide and nitride layers with 3000 Å of thickness each are deposited as a passivation layer which prevents further oxidation and contamination. The contact hole has to be etched from the passivation layer as shown in Fig. A.3c to probe the metal after the whole fabrication process step. The back side oxide layer is etched out by soaking into BHF, protecting the front side with a spin-coated PR layer. For the back side metallization, 7000 Å of Al is deposited with physical vapor deposition (PVD) method as illustrated in Fig. A.3d. After the PR

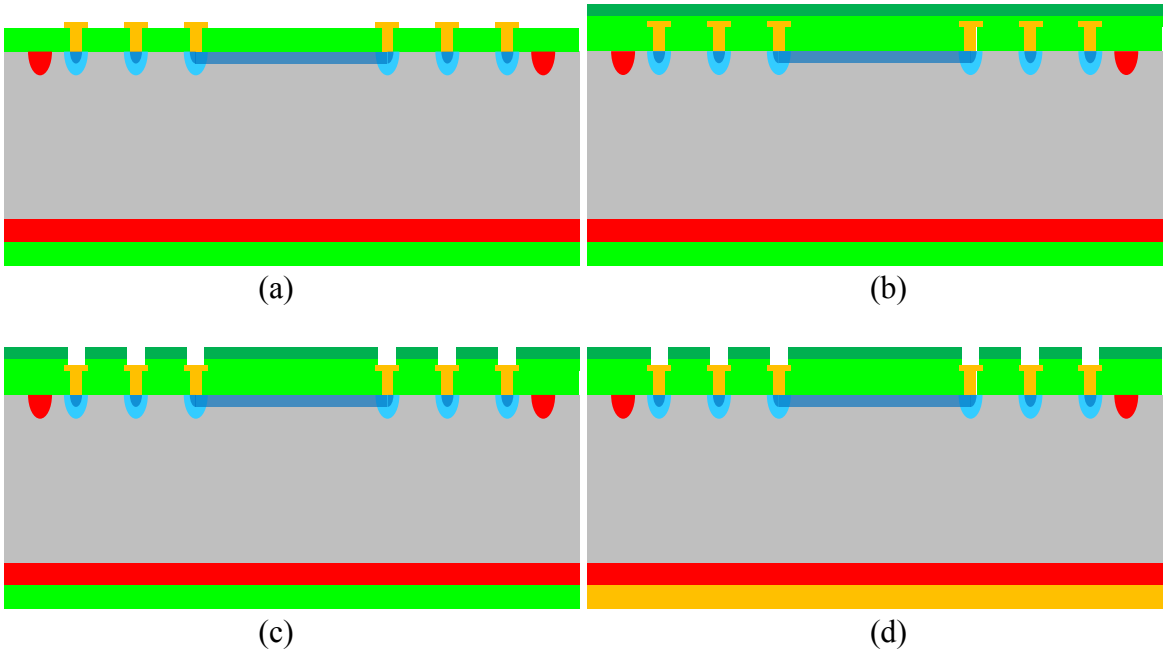


Fig. A.3. Silicon radiation detector processing chart. (a) After the lift-off process for the metal patterning. (b) Passivation layer deposition. (c) Contact hole is etched out for metal probing. (d) Back side metallization after the oxide removal.

removal which is used as a protection layer, the wafer should be annealed for 30 min at 400 ºC which can either alloy with the semiconductor or reduces the unintentional barrier at the interface.

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