IF-Sampling Digital Beamforming with Bit-Stream Processing

by

Jaehun Jeong

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Doctoral Committee:

Professor Michael P. Flynn, Chair
Professor Jerome P. Lynch
Associate Professor David D. Wentzloff
Associate Professor Zhengya Zhang

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LIST OF ABBREVIATIONS

ABF	Analog beamforming
ADC	Analog-to-digital converter
BiCMOS	Bipolar complementary metal-oxide-semiconductor
BSP	Bit-stream processing
CMOS	Complementary metal-oxide-semiconductor
CT	Continuous time
CTBPDSM	Continuous-time band-pass delta-sigma modulator
CWM	Complex weight multiplication
DAC	Digital-to-analog converter
DBF	Digital beamforming
DDC	Digital down conversion
DDS	Direct digital synthesizer
DSP	Digital signal processing
DT	Discrete time
dB	Decibel
ENOB	Effective number of bit
FoM	Figure of merit
FPGA	Field programmable gate array
HZ	Half-clock-delayed return-to-zero

IC	Integrated circuit
IF	Intermediate frequency
IMD	Intermodulation distortion
LO	Local oscillator
LPF	Low-pass filter
MIMO	Multiple input and multiple output
MUX	Multiplexer
NMOS	N-type metal-oxide-semiconductor
NTF	Noise transfer function
PCB	Printed circuit board
PMOS	P-type metal-oxide-semiconductor
PSD	Power spectral density
RF	Radio frequency
RZ	Return-to-zero
SiGe	Silicon Germanium
SNDR	Signal-to-noise-plus-distortion ratio
SNR	Signal-to-noise ratio
STF	Signal transfer function
VGA	Variable-gain amplifier

ABSTRACT

Beamforming in receivers improves signal-to-noise ratio (SNR), and enables spatial filtering of incoming signals, which helps reject interferers. However, power consumption, area, and routing complexity needed with an increasing number of elements have been a bottleneck to implementing efficient beamforming systems. Especially, digital beamforming (DBF), despite its versatility, has not been attractive for low-cost on-chip implementation due to its high power consumption and large die area for multiple high-performance analog-to-digital converters (ADCs) and an intensive digital signal processing (DSP) unit.

This thesis presents a new DBF receiver architecture with direct intermediate frequency (IF) sampling. By adopting IF sampling in DBF, a digital-intensive beamforming receiver, which provides highly flexible and accurate beamforming, is achieved. The IF-sampling DBF receiver architecture is efficiently implemented with continuous-time band-pass $\Delta\Sigma$ modulators (CTBPDSMs) and bit-stream processing (BSP). They have been separately investigated, and have not been considered for DBF until now. The unique combination of CTBPDSMs and BSP enables low-power and area-efficient DBF by removing the need for digital multipliers and multiple decimators.

Two prototype digital beamformers (prototype I and prototype II) are fabricated in 65 nm complementary metal-oxide-semiconductor (CMOS) technology. The prototype I forms a single beam from four 265 MHz IF inputs, and an array signal-to-noise-plus-

distortion ratio (SNDR) of 56.6 dB is achieved over a 10 MHz bandwidth. The prototype I consumes 67.2 mW, and occupies 0.16 mm^2. The prototype II forms two simultaneous beams from eight 260 MHz IF inputs, and an array SNDR of 63.3 dB is achieved over a 10 MHz bandwidth. The prototype II consumes 123.7 mW, and occupies 0.28 mm^2. The two prototypes are the first on-chip implementation of IF-sampling DBF.

CHAPTER 1 Introduction

1.1 Beamforming and Its Applications

Beamforming is an array processing technique to focus energy along a specific direction in multiple antenna systems. Beamforming in receivers performs spatial filtering of incoming signals. This spatial filtering separates a desired signal from interferers from different locations, and is especially useful when the interferer frequency is close to the desired signal frequency since frequency domain filtering is not helpful [1]. In addition, beamforming improves the SNR of the received signal by 3 dB for each doubling the number of antenna elements.

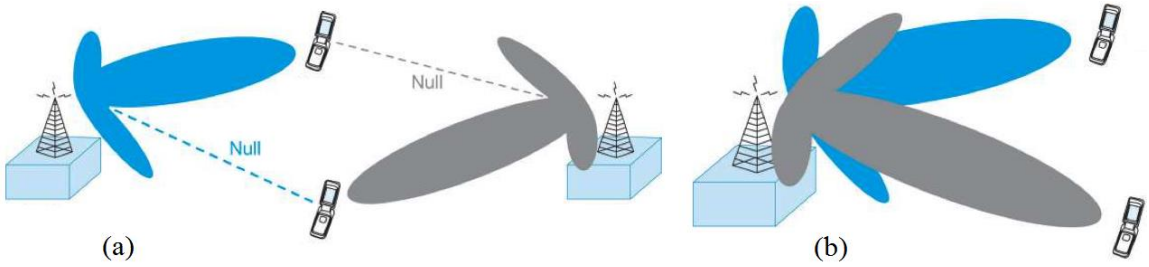
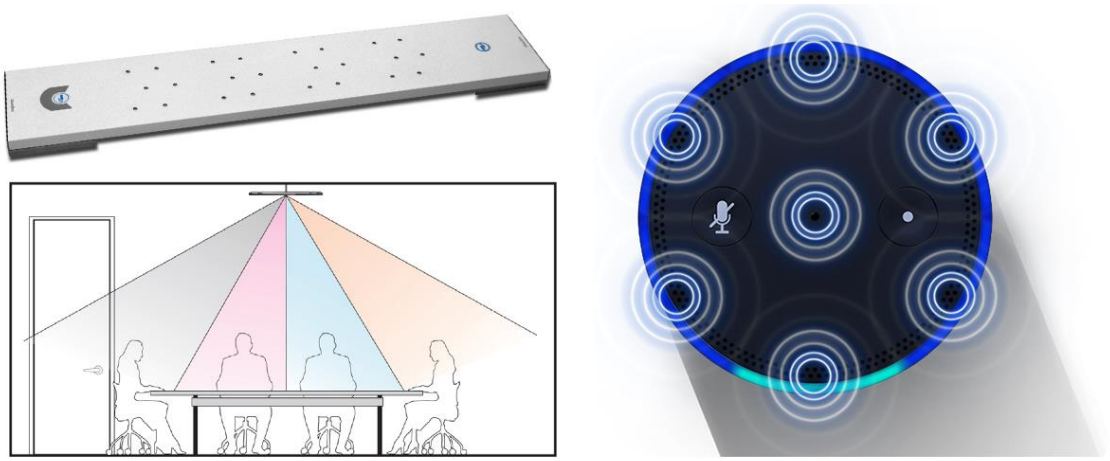


Figure 1.1 Improvement on (a) cell edge performance and (b) cell capacity [2]

Traditionally, beamforming is used in military systems to suppress jamming signals. Now, beamforming is widely used in many different applications as radar, sonar, astronomy, acoustics, and wireless communications. Especially in modern wireless communications such as the IEEE 802.16e (WiMAX) and the 3rd generation partnership project (3GPP), beamforming plays an essential role to support higher data rate, and improves link quality, capacity, and reliability. Figure 1.1 shows the advantages of

beamforming in a modern cellular wireless system: cell edge performance improvement (Figure 1.1(a)) and cell capacity improvement (Figure 1.1(b)) [2].

Beamforming techniques are applied to several commercial products. A 24-element beamforming microphone array shown in Figure 1.2(a) provides spatial selectivity in a conference. With beamforming, pickup patterns are created toward participants while unwanted noise is rejected. A bluetooth speaker with voice recognition shown in Figure 1.2(b) has seven microphones, and performs beamforming to improve far-field voice recognition.



(a) (b)

Figure 1.2 (a) Beamforming microphone array [3] (b) Amazon echo [4]

1.2 Narrowband and Wideband Beamforming

Beamforming can be classified into two categories depending on the signal bandwidth: narrowband beamforming and wideband beamforming.

In narrowband beamforming (phase-shift beamforming), a time delay associated with each antenna path is approximated with a constant phase shift (usually with respect to the center frequency) over the entire bandwidth of interest. Narrowband beamforming has been widely used in wireless applications where the signal bandwidth is narrow enough,

since phase shifters can be implemented with relatively low cost compared to time delays. However, the narrowband approximation does not hold with wideband signals, and as a result, the beam direction deviates as a function of frequency. This phenomenon is called *beam squint* [5].

In wideband beamforming (time-delay beamforming), adjustable time delays are implemented in each antenna path. This technique is not limited to narrowband signals, but the implementation of time delays is relatively bulky and costly [6]. Wideband beamforming has been studied in various areas, particularly in microphone arrays since human voice and sound are wideband signals. Recently, with the increased bandwidth in modern wireless systems, the importance of wideband beamforming has increased.

1.3 Beamforming in Receivers

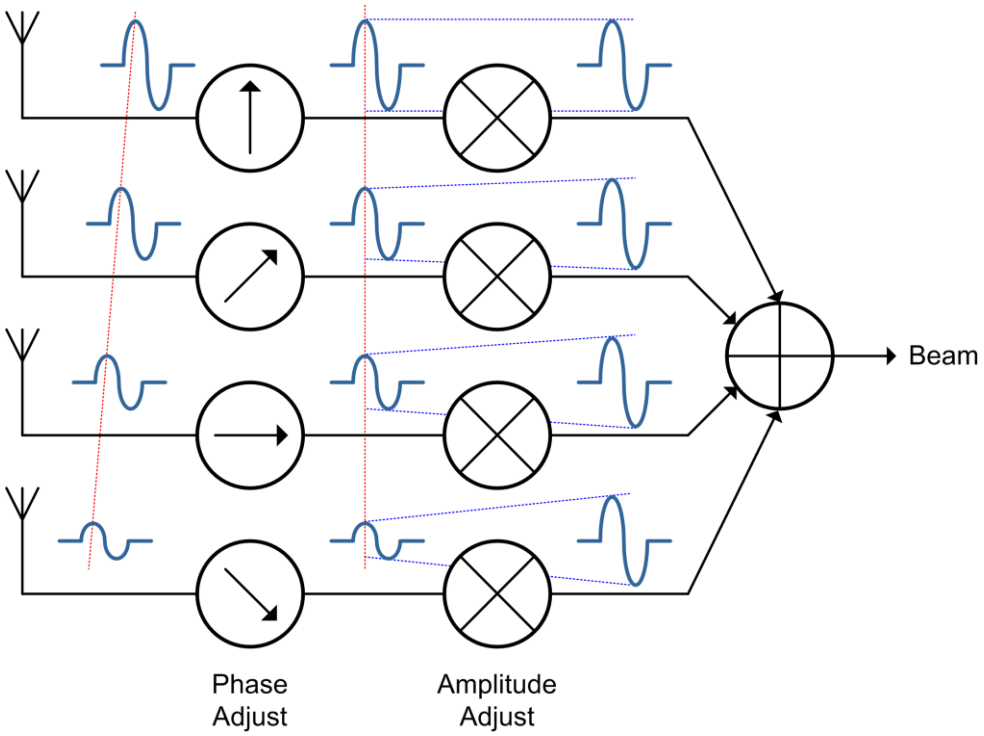


Figure 1.3 Four-element beamforming receiver

Beamforming has been adopted in receivers to enhance SNR and spatially reject interferers. Figure 1.3 shows a beamforming receiver with a uniformly spaced four-element linear antenna array. In the beamforming receiver, the phase and amplitude of each antenna element are adjusted to create beams, and to steer nulls. Mathematically, the phase (θ) and amplitude (A) adjustments in each antenna path can be represented as a complex weight ($Ae^{j\theta}$). In the far field, the received amplitude in each antenna element is approximately the same, and therefore only phase adjustment is sufficient.

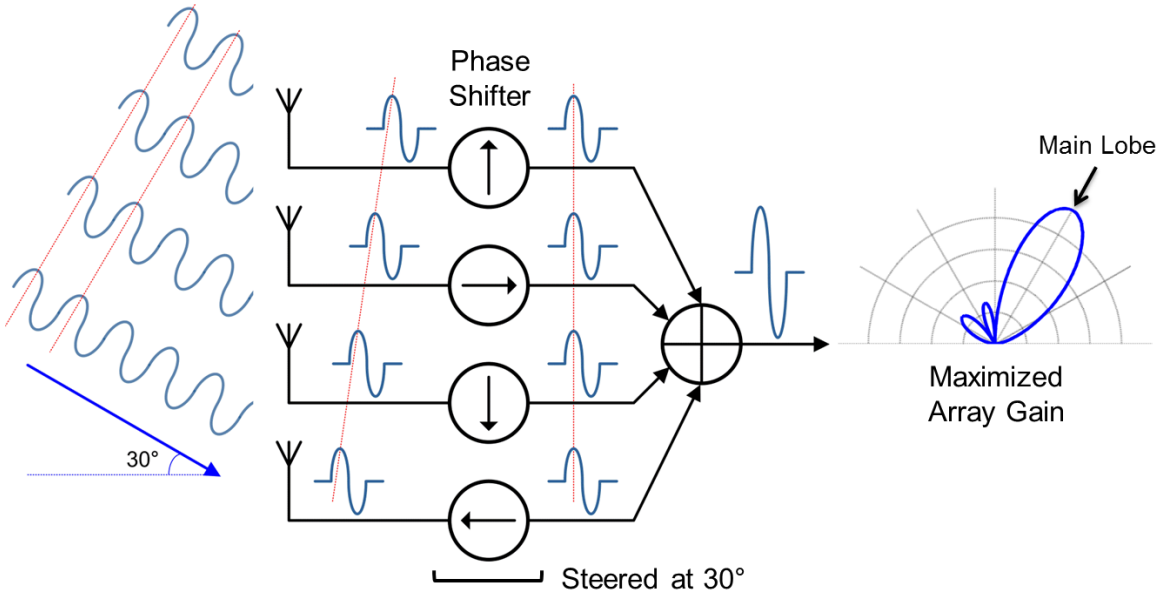


Figure 1.4 Constructive combination to create a main lobe

When a plane wave with an incidence angle of 30° is received by a four-element linear antenna array with λ/2 spacing as shown in Figure 1.4, there is a phase difference of 90° between adjacent element signals. To maximize the array gain for the incidence angle of 30°, the phase difference is compensated by phase shifters, resulting in coherent signals at the outputs of the phase shifters. The coherent signals are constructively combined, and the array gain is maximized (i.e. 12 dB) for the incidence angle of 30° to create a main lobe.

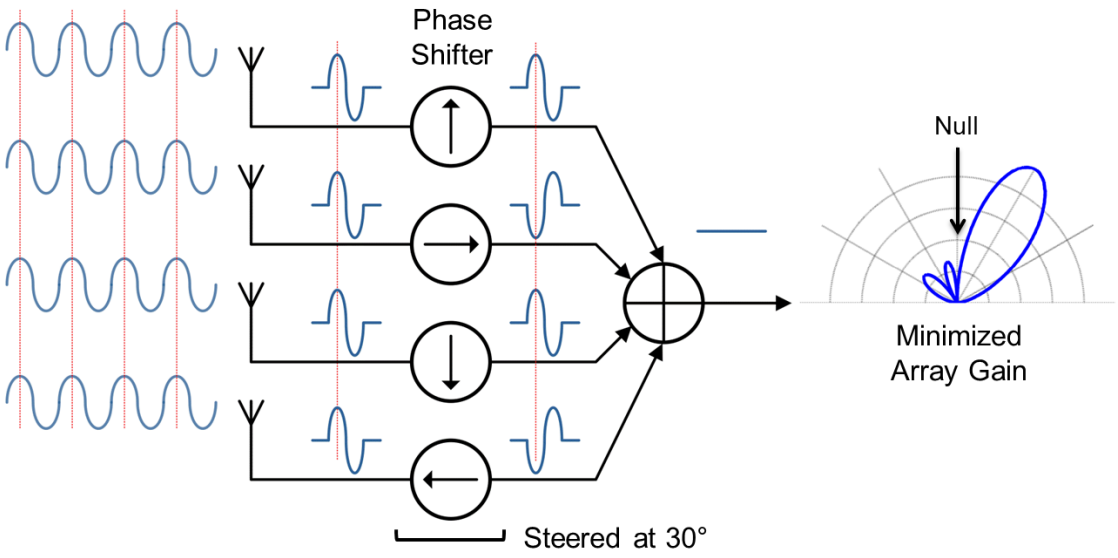


Figure 1.5 Destructive combination to create a null

When a plane wave with an incidence angle of 0° is received by the same antenna array with the same phase shifter configuration as shown in Figure 1.5, signals at the outputs of phase shifters are out of phase. Therefore, these signals are destructively combined, and canceled out, resulting in an array gain of zero.

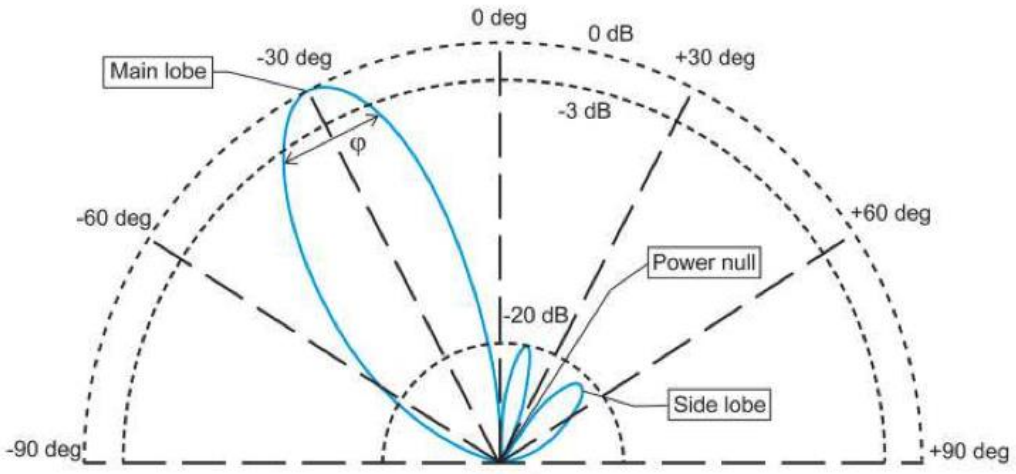


Figure 1.6 Beam pattern of a four-element linear array with λ/2 spacing [2]

The array gains for different incidence angles are usually plotted in a polar diagram, and the plot is called a beam pattern. Figure 1.6 shows a beam pattern of a four-element

linear array with λ/2 spacing [2]. The lobe which contains the maximum power is defined as a main lobe, and the other lobes are called as side lobes. The beamwidth (φ) is the angle between half-power (-3 dB) points in the main lobe. As the number of antenna elements increases, the beamwidth decreases, and the side lobes become smaller as shown in Figure 1.7.

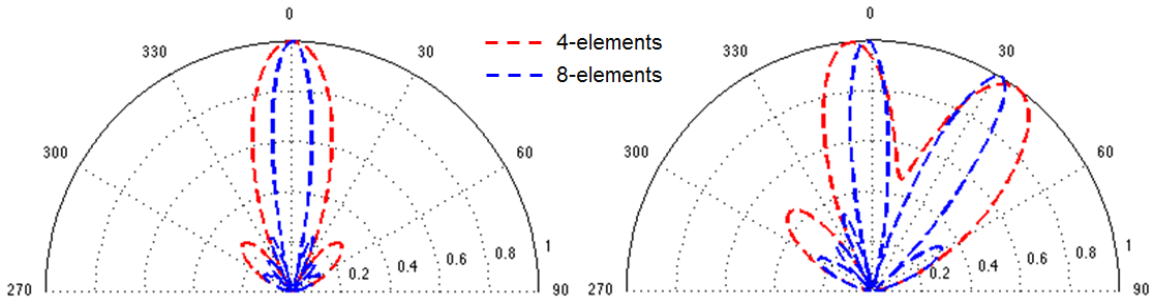


Figure 1.7 Beam patterns of four- and eight-element antenna arrays

1.4 Beamforming Receiver Architectures

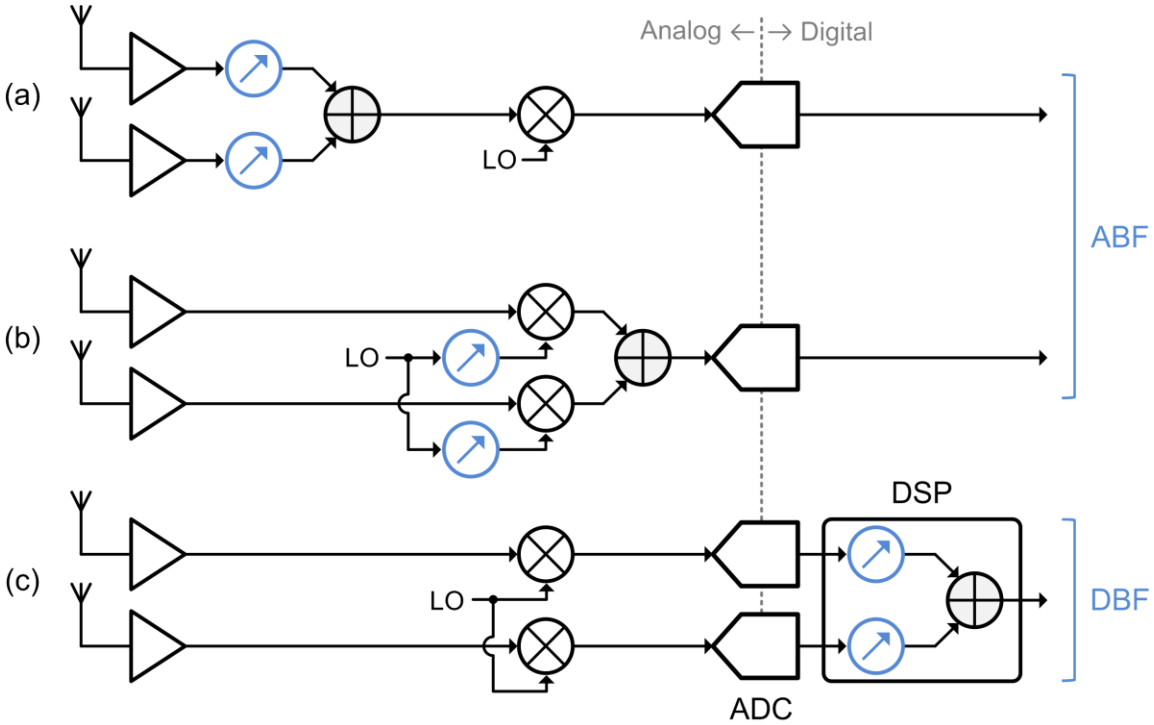


Figure 1.8 (a) ABF in the RF signal path (b) ABF in the LO path (c) DBF

For narrowband signals, beamforming is often implemented with phase shifters in a receiver. A receiver which performs beamforming with phase shifters is called a phased-array receiver. In the phased-array receiver, beamforming can be categorized into analog beamforming (ABF) and digital beamforming (DBF) depending on the domain where phase shifting is implemented as shown in Figure 1.8.

1.4.1 Analog Beamforming

In analog beamforming, phase shifters can be implemented in the RF signal path (Figure 1.8(a)) or in the LO path (Figure 1.8(b)). Traditionally, phase shifting in the RF signal path has been dominant. With the RF-path phase shifting, multiple signal paths are combined at the very early stage of the receiver, and therefore the number of subsequent hardware including down converters and ADCs can be minimized. The early combination of element signals also relaxes the linearity and dynamic range requirements of the down converters and ADCs, because interferers can be suppressed before reaching these components. However, due to the early combination, the information carried by each received element signal is lost before reaching the baseband digital signal processing (DSP). This limits flexibility and the ability to form multiple simultaneous beams. In the LO-path beamforming, phase shifting is implemented in the LO distribution network. Since phase shifters are not placed in the signal path, LO-path beamforming has less impact on SNR [7]. However, LO-path beamforming requires multiple analog mixers and a large LO distribution network, increasing system complexity and area.

Table 1.1 summarizes recent IC implementation of analog phased-array receivers with RF-path beamforming [8−12] and LO-path beamforming [13−15]. In [12], reflection-type passive phase shifters are used in the RF signal path. Passive phase shifters occupy a

large area, so they are feasible only at high frequencies (i.e. tens of GHz) [7]. In addition, the insertion loss of passive phase shifters depends on the amount of phase shift. Therefore, the passive phase shifter is sometimes followed by a variable-gain amplifier (VGA) to compensate the variation of insertion loss [12]. Active phase shifting in the RF signal path with vector modulation is more popular for on-chip implementation [8−11]. The active phase shifting is based on VGAs, and they occupy smaller area than passive shifters. However, due to the need for multiple high-resolution RF VGAs, the active approach is more power-hungry than the passive approach [12]. Vector modulation is also popular in LO-path beamforming. In [13], phase-oversampling vector modulation is presented to achieve fine phase-shift resolution. Vector modulation is also implemented with switched capacitors [14, 15].

Table 1.1 Fully-integrated analog phased-array receivers

Type	Ref.	Frequency [GHz]	# of Elements	Power [mW]	Area [mm^2]	Technology
RF	[8]	5	4	140	4.1	90 nm CMOS
	[9]	6−18	8	330−660	5.4	0.18 μm SiGe BiCMOS
	[10]	24	4	115	3.0	0.13 μm CMOS
	[11]	60	4	178	3.4	65 nm CMOS
	[12]	60	16	1800	37.7	0.12 μm SiGe BiCMOS
LO	[13]	4	4	166	1.9	90 nm CMOS
	[14]	1−4	4	308	1.1	65 nm CMOS
	[15]	1.5−5.0	4	65−168	0.7	65 nm CMOS

1.4.2 Digital Beamforming

In digital beamforming (Figure 1.8(c)), incoming signals received by an antenna array are down-converted to baseband I/Q signals, and digitized by ADCs. By digitally

controlling the phase of each down-converted signal (x_k) at the k-th element with DSP, element signals are constructively or destructively combined. To achieve a phase shift of θ, the baseband I/Q signals are scaled, and combined to generate phase-shifted I′/Q′ outputs as follows:

$$I' = \cos(\theta)\, I + \sin(\theta)\, Q, \tag{1.1}$$

$$Q' = -\sin(\theta)\, I + \cos(\theta)\, Q. \tag{1.2}$$

When the I/Q signals are represented as a complex signal, the above operations are equivalent to multiplication by $e^{j\theta}$. For this reason, this technique is called complex weight multiplication (CWM). For a uniformly spaced eight-element linear antenna array, a complex weight of $e^{j(k\theta)}$ adjusts the delay at the k-th element, and then all signal paths are combined to create a beam ($= \sum_{k=0}^{7} x_k e^{j(k\theta)}$).

Since phase shifting with CWM is performed in the digital domain, DBF achieves the highest accuracy and flexibility. In addition, DSP algorithms can be easily applied in DBF for advanced functions including adaptive beamforming and array calibration. Furthermore, multiple simultaneous beams can be formed because the digitized and down-converted I/Q signals for all antenna elements are available. Multiple beamforming is an integral part of beyond-3G mobile communication systems, and more advanced beamforming algorithms are expected to support adaptive beamforming in upcoming standards. DBF is essential for these emerging applications. However, DBF requires multiple down converters, high-performance ADCs, and an intensive DSP unit, resulting in high power consumption and large die area. Therefore, DBF has not been attractive for low-cost on-chip implementation. Instead, DBF is largely confined to base station applications, and implemented on FPGAs [16, 17] or in software [18].

1.5 Finite Complex Weight Resolution Effect on Phase Shifting

As discussed in Chapter 1.4.2, CWM is often used in DBF to implement phase shifting. Phase shifting with CWM is illustrated in Figure 1.9. To achieve a phase shift of θ, baseband I/Q vectors are multiplied by weighting factors of $\cos\theta$ and $\sin\theta$, and then combined to create phase-shifted I′/Q′ vectors.

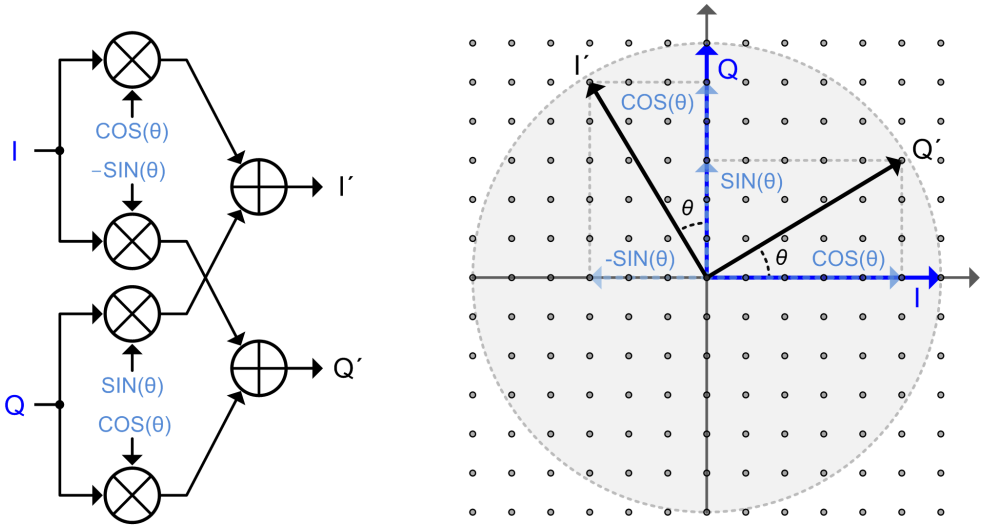


Figure 1.9 Phase shifting with CWM

With 3 bit resolution weighting factors, a total of 49 $(= (2^3 - 1)^2)$ vectors can be generated by CWM as shown in Figure 1.10(a). However, to maintain a near constant amplitude, only 24 vectors are used (shown as blue dots in Figure 1.10(a)). Due to the finite resolution of weighting factors, a desired vector with a phase shift of θ (shown as v in Figure 1.10(a)) is not always available. Instead, the closest available vector (shown as v' in Figure 1.10(a)) replaces the desired vector, resulting in amplitude and phase errors. Figure 1.11(a) shows the amplitude and phase errors with the 3 bit resolution. The amplitude error range is from -5.7% to +20.2% with a variation of 25.9%. The phase error range is from -10.7° to +10.7° with a variation of 21.4°. The amplitude and phase errors decrease as the weighting factor resolution increases. With a 6 bit resolution

(Figure 1.10(b)), the amplitude variation is 3.7%, and the phase variation is 2.5° as shown in Figure 1.11(b).

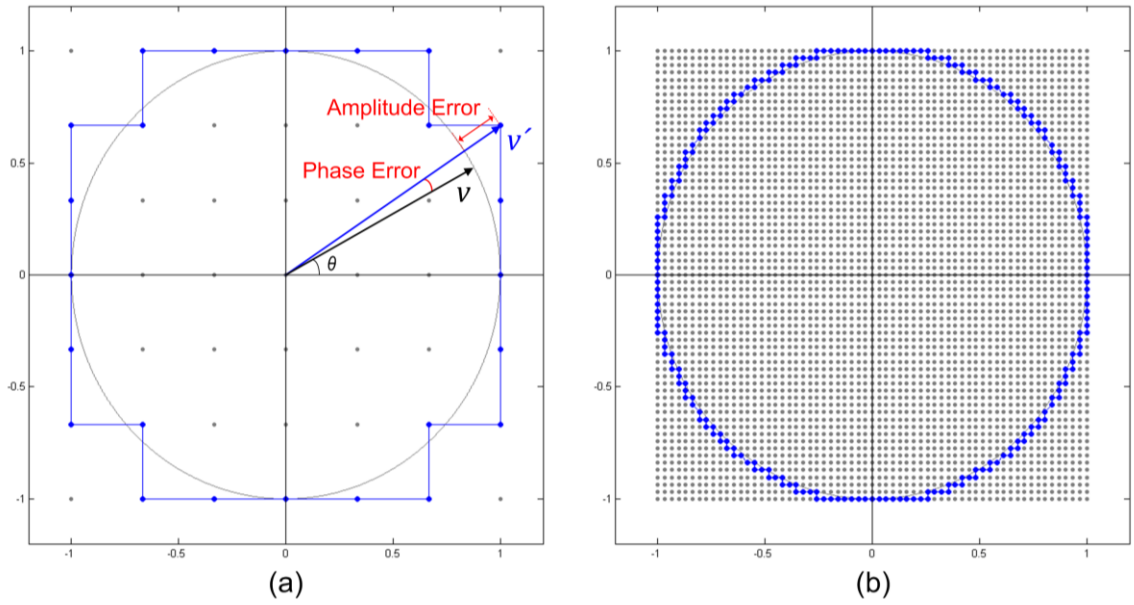


Figure 1.10 CWM with (a) 3 and (b) 6 bit weighting factors

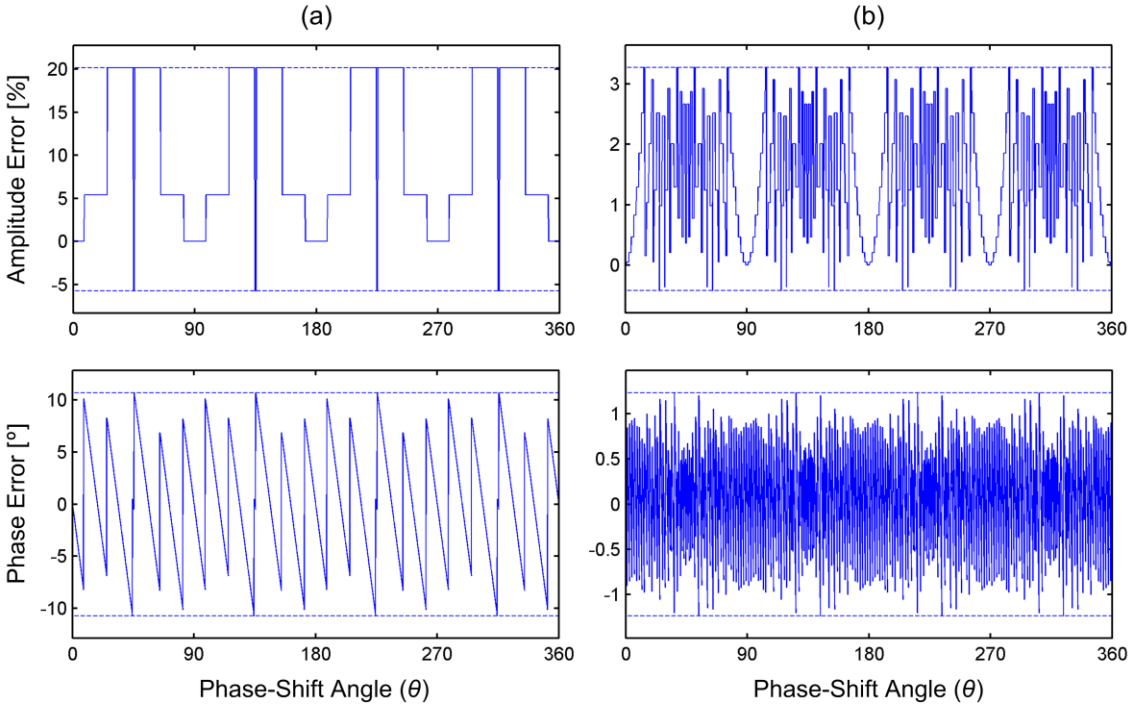


Figure 1.11 Amplitude and phase errors with (a) 3 and (b) 6 bit weighting factors

Table 1.2 Finite complex weight resolution effect

Weighting factor resolution [bit]	3	4	5	6	7
Total phase-shift steps	24	56	120	240	496
Amplitude variation [%]	25.9	15.2	8.4	3.7	1.9
Phase variation [º]	21.4	9.2	4.8	2.5	1.2
Average phase-shift step size [º]	15	6.4	3.0	1.5	0.7

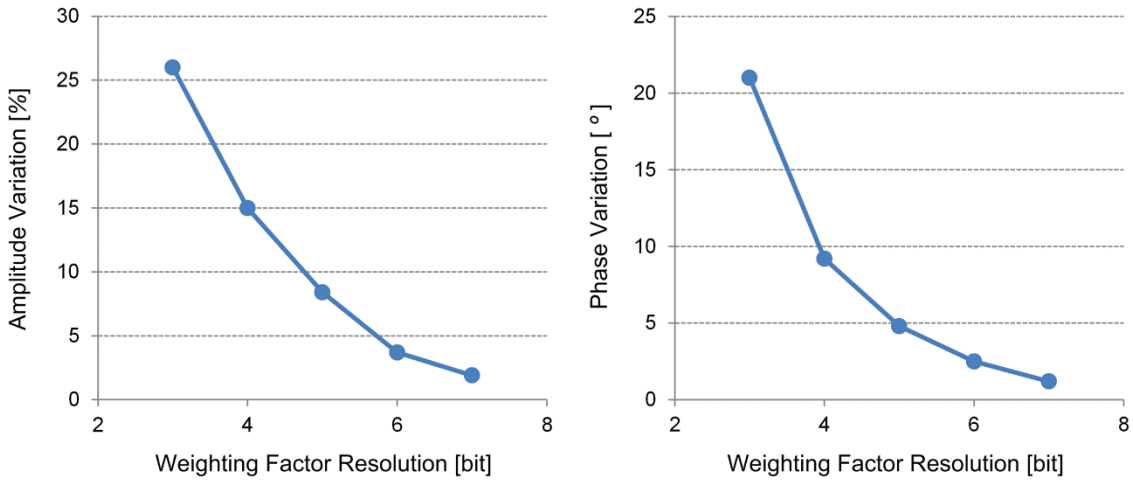


Figure 1.12 Amplitude and phase variations versus weighting factor resolution

Table 1.2 summarizes the effect of five different weighting factor resolutions on phase shifting. The amplitude and phase variations versus weighting factor resolution are plotted in Figure 1.12.

1.6 Thesis Overview

As discussed in Chapter 1.4.2, DBF is essential for emerging applications to support multiple simultaneous beams and advanced algorithms. However, DBF is not preferred for on-chip implementation due to its high power consumption and large die area for multiple high-performance ADCs and an intensive DSP unit. In addition, DBF has been performed with baseband sampling, and direct IF sampling has not been considered for

DBF until now. In Chapter 2, a new DBF receiver architecture with direct IF sampling is proposed. To enable efficient implementation of the architecture, an ADC-digital co-design approach which combines an array of continuous-time band-pass $\Delta\Sigma$ modulators (CTBPDSMs) and bit-stream processing (BSP) is also presented. In addition, two prototype beamformers and their detailed implementation are described. This research also focuses on the power- and area-efficient design of the CTBPDSM. Since the DBF architecture requires multiple CTBPDSMs, the power consumption and area of the CTBPDSM have a large bearing on the power consumption and area of the entire system. Chapter 3 details the architecture and circuit implementation of the CTBPDSM. Chapter 4 provides measurements of the two prototype beamformers. Future work is suggested in Chapter 5, and key contributions of this research are summarized in Chapter 6.

CHAPTER 2 IF-Sampling DBF with CTBPDSMs and BSP

To enable efficient implementation of DBF, we propose a new DBF architecture based on continuous-time band-pass ΔΣ modulators (CTBPDSMs) and bit-stream processing (BSP). Although both CTBPDSMs and BSP have been separately investigated, until now these techniques have not been considered for DBF. The emergence of new circuit techniques and the improvement in CMOS technology have made the combination compelling.

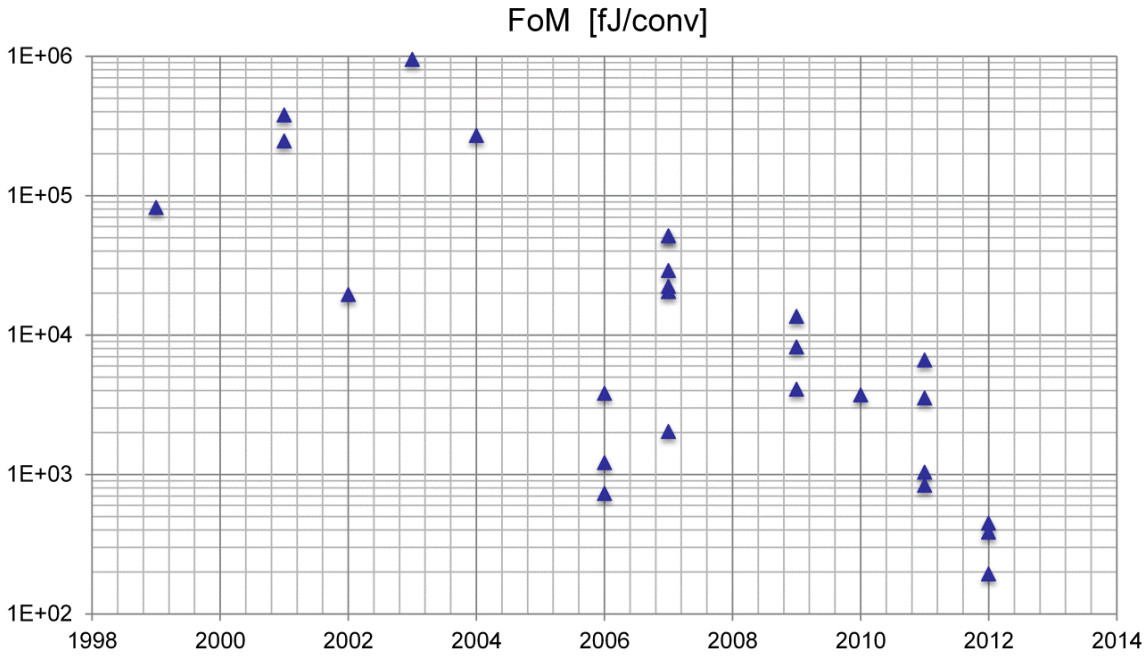


Figure 2.1 Band-pass ADC Walden FoM versus year

Figure 2.1 illustrates the dramatic improvement in the energy efficiency of band-pass ΔΣ modulators seen in published devices. An improvement of more than two orders of magnitude is seen in the Walden figure of merit (FoM) over the last decade.

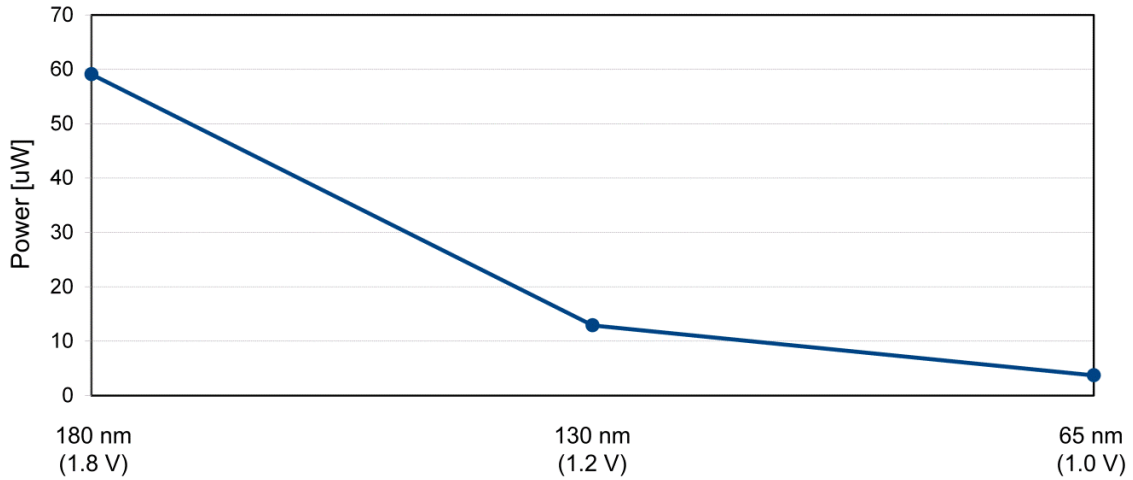


Figure 2.2 Power consumption of a 1 GHz bit-stream multiplier

Improvements in CMOS technology are also making BSP compelling. In BSP, single-bit (or low-resolution) signals are processed to take advantage of the low word width. As a result, the number of logic gates and routing complexity are reduced [19]. In addition, as we will see in Chapter 2.2, a bit-stream can be multiplied with a simple multiplexer (MUX). Figure 2.2 shows the power consumption of a 1 GHz bit-stream multiplier (implemented with a MUX) over three generations of CMOS technology: 180 nm, 130 nm, and 65 nm CMOS. The improvement in the energy efficiency is more than an order of magnitude. BSP is an attractive choice for DBF because of its simplicity and efficiency. As shown in Figure 2.1 and Figure 2.2, both CTBPDSMs and BSP scale very well with CMOS technology.

In the new DBF architecture with CTBPDSMs and BSP, IF signals are digitized by an array of CTBPDSMs to take advantage of direct IF sampling. By directly processing the un-decimated CTBPDSM digital outputs with BSP, digital down conversion (DDC) and phase shifting are implemented with only MUXs. Moreover, directly processing the CTBPDSM outputs avoids the need for multiple decimators for DBF. As a result, the

architecture achieves low-power and area-efficient IF-sampling DBF. Two prototype digital beamforming ICs are fabricated in 65 nm CMOS. The first prototype (prototype I) forms a single beam from four 265 MHz IF inputs. The second prototype (prototype II) forms two simultaneous beams from eight 260 MHz IF inputs. The two prototypes are the first IC implementation of IF-sampling DBF.

2.1 DBF with Direct IF Sampling

The concept of direct IF (or RF) sampling has arisen to enable digital-intensive receivers. By digitizing higher frequencies (i.e. IF or RF), most of the signal processing chain including down conversion and filtering is carried out in the digital domain. This enables perfectly matched digital I/Q down conversion as well as high-performance channel selection filtering. In addition, with a digital-intensive architecture, the receiver can be highly reconfigurable to support multiple standards, and benefits more from CMOS scaling. Furthermore, with direct IF sampling, the receiver is immune to flicker noise and DC offset.

CTBPDSMs [20 − 26] are capable of digitizing relatively high frequencies, and are attractive for direct sampling receivers. Compared to a discrete-time (DT) ΔΣ modulator, a continuous-time (CT) modulator is more suitable for high-speed operation due to the relaxed op-amp bandwidth requirements. In addition, a CT ΔΣ modulator presents a resistive input, which is relatively easy to drive in a system. Furthermore, a CT modulator provides implicit anti-alias filtering, which relaxes the receiver front-end filtering requirements. The sample rate of the CTBPDSM is often chosen to be four times the input IF (or RF). With this sample rate, the sampled LO sequence for DDC has only three values of -1, 0, and +1, simplifying DDC in the receiver.

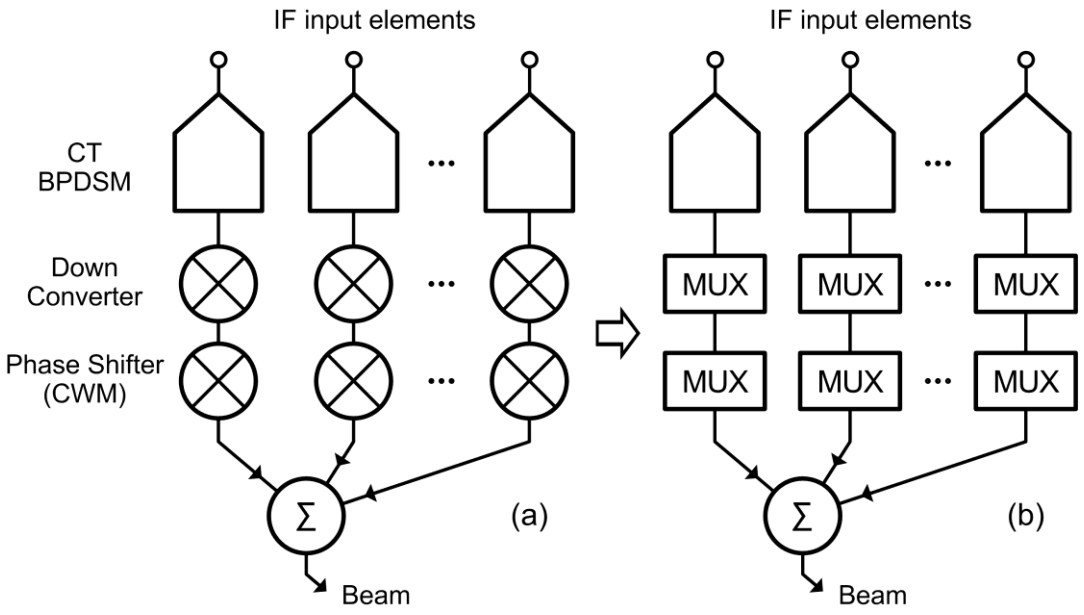


Figure 2.3 (a) IF-sampling DBF and (b) its MUX-based implementation

We implement IF-sampling DBF with an array of CTBPDSMs as shown in Figure 2.3(a). IF input signals are directly digitized by CTBPDSMs, and digitally down-converted to form baseband I/Q signals. The baseband I/Q signals are phase-shifted with CWM, and summed to create a beam. The IF-sampling DBF architecture normally requires several digital multipliers for DDC and CWM. However, thanks to the ΔΣ modulated low-resolution CTBPDSM digital outputs, the architecture is implemented very efficiently with MUXs as shown in Figure 2.3(b). As we will see next, multipliers are replaced with MUXs in BSP. As a result, both DDC and CWM are implemented with simple MUXs.

2.2 Bit-Stream Processing DBF with ΔΣ Modulator Outputs

In ΔΣ modulation, the combination of oversampling and noise shaping enables a high SNR modulator output with a single-bit (or low-resolution) quantizer. Conventionally, the low-resolution digital output of the ΔΣ modulator is low-pass filtered and decimated

before further DSP (Figure 2.4(a)). In the conventional approach, DSP is performed at a lower clock rate after decimation but at the cost of an increased word width. In BSP, on the other hand, the bit-stream modulator output is directly processed before decimation (Figure 2.4(b)) to take advantage of the low word width. This approach was first proposed in [27] to realize a multiplier-less digital filter with a single-bit Δ modulator output.

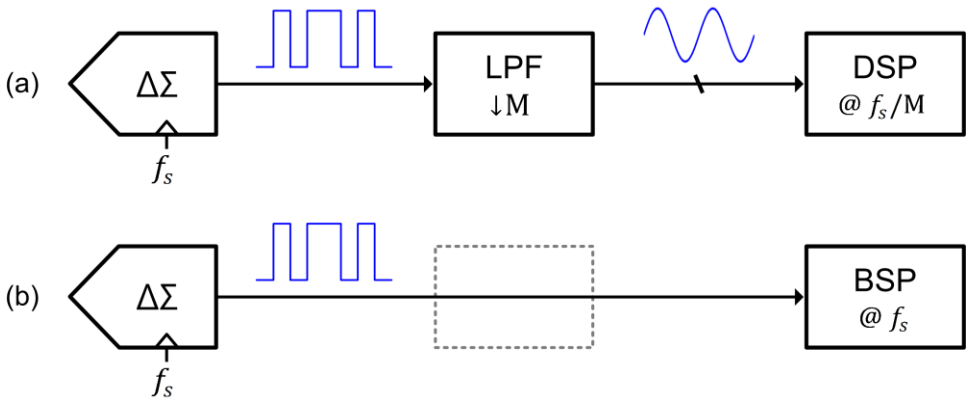


Figure 2.4 (a) DSP after decimation (b) BSP

A significant advantage of BSP is that it replaces bulky multipliers with simple MUXs. MUX-based multiplication with a bit-stream is described in Figure 2.5. The bit-stream controls a 2:1 MUX to multiply the input bit-stream by a multi-bit coefficient, W, which is stored in a register. Depending on the value of the bit-stream, the 2:1 MUX output is selected to be either 0 or W. In this way, the 2:1 MUX output represents the result of multiplication of the bit-stream by W. MUX-based multiplication can be extended to a five-level stream (Figure 2.6) [28]. Compared to a bit-stream, the five-level stream contains the additional levels of -2, -1, and +2. To handle these additional levels, two trivial operations are added to the multiplexing: sign inversion and 1 bit left shift (shown as $\ll 1$ in Figure 2.6). When the value of the five-level stream is -1, the sign of W is

inverted to implement multiplication by -1. When the value of the five-level stream is +2, W is left-shifted by 1 bit to implement multiplication by +2. When the value of the five-level stream is -2, both sign inversion and 1 bit left shift are performed to implement multiplication by -2. In this way, a 5:1 MUX performs multiplication with sign inversion and 1 bit left shift as shown in Figure 2.6. To exploit this simple MUX-based multiplication for DBF, the sample rate of the CTBPDSM is chosen to be four times the IF, and the CTBPDSM quantizer resolution is chosen to be five levels. These enable a MUX-based implementation of both DDC and CWM (Figure 2.3(b)), greatly reducing circuit complexity.

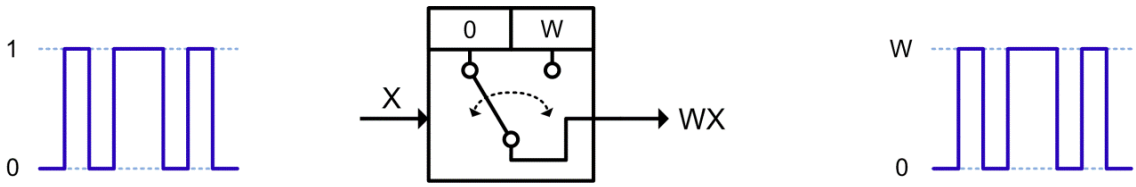


Figure 2.5 Bit-Stream multiplication with a 2:1 MUX

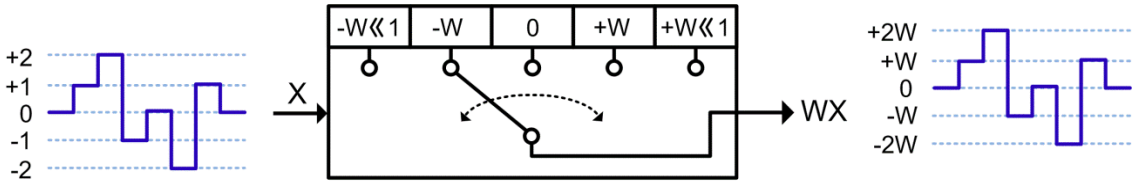


Figure 2.6 Five-level stream multiplication with a 5:1 MUX

Another advantage of directly processing the CTBPDSM outputs in a multiple-input single-output system (e.g. beamformer) is that it reduces the number of decimators to just one. For multiple inputs and multiple ΔΣ modulators in conventional DSP (Figure 2.7 (a)), there is a decimator for each modulator. Because of this, the cost of decimation (by M) increases linearly with the number of inputs. In BSP, on the other hand, decimation is performed only once after all the digital signal paths are combined (Figure 2.7(b)). Since

decimation consumes a lot of power and requires a large area, the single decimation helps significantly reduce the power consumption and area of the entire system.

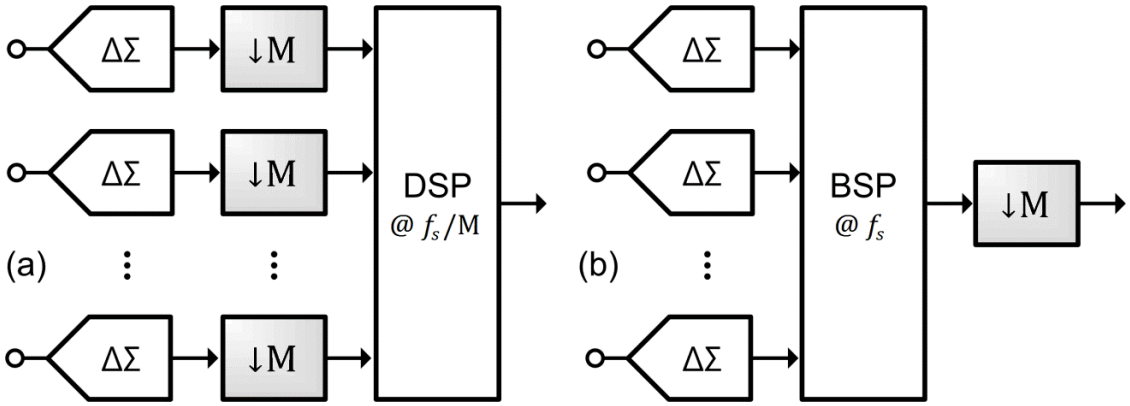


Figure 2.7 (a) DSP with multiple decimators (b) BSP with a single decimator

2.3 Mathematical Expressions of DBF with Band-Pass ADCs

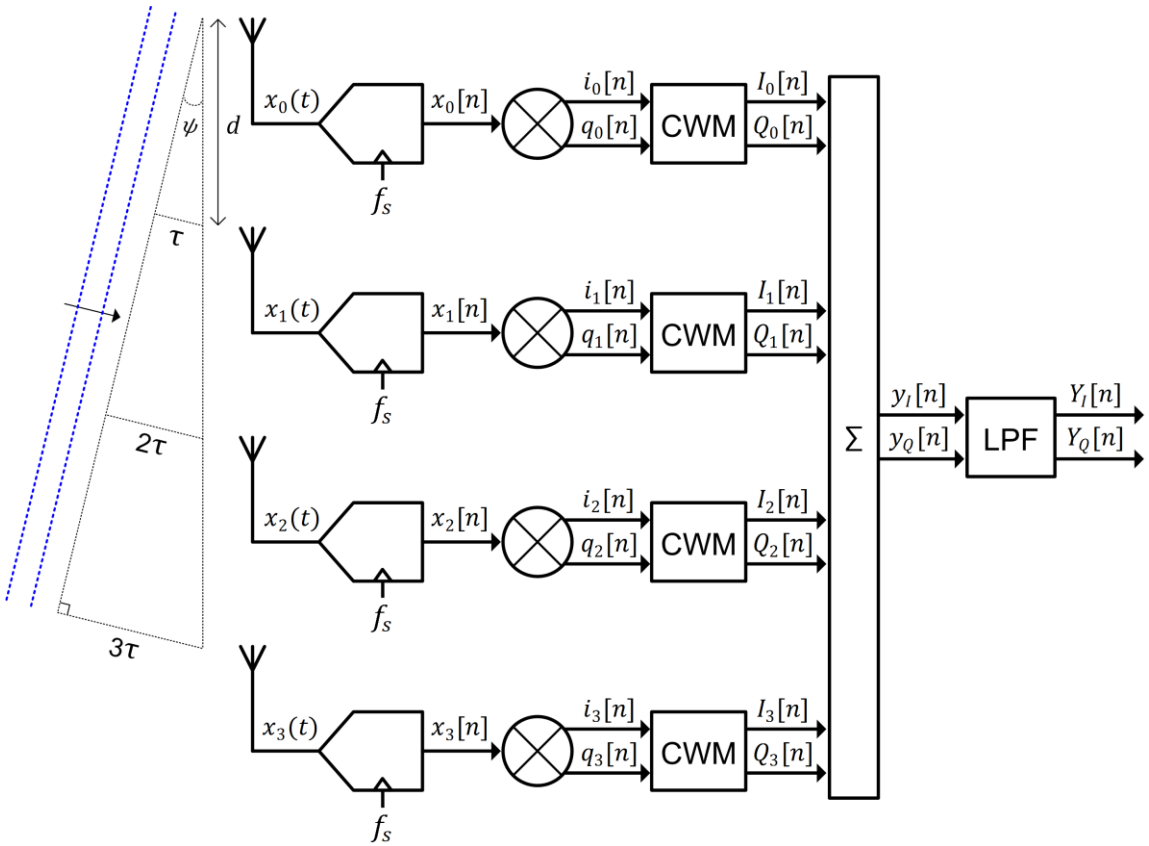


Figure 2.8 Four-element digital beamformer with band-pass ADCs

2.3.1 Beamforming with Single-Tone Inputs

Consider a plane wave with an incident angle of ψ, received by a linear antenna array of N elements with a spacing of d shown in Figure 2.8. Assuming that the incident plane wave is a narrowband signal around a center frequency of f_c, the frequency of the incident wave (f_{in}) can be represented by:

$$f_{in} = f_c + \Delta f. \tag{2.1}$$

Then, the received signal at k-th antenna element can be represented as:

$$x_k(t) = \cos(2\pi f_{in}(t - k\tau) + \varphi), \tag{2.2}$$

where $\tau = \frac{dsin\psi}{c}$ (c is the speed of light) and φ is the initial phase of the incident wave. In narrowband beamforming, the time delay associated with each antenna element (τ) is approximated with a constant phase shift of θ by the following equation.

$$2\pi f_{in}\tau \approx 2\pi f_c\tau = \theta. \tag{2.3}$$

With the narrowband approximation, equation (2.2) is expressed as:

$$x_k(t) = \cos(2\pi f_{in}t + \varphi - k\theta). \tag{2.4}$$

The received signals ($x_k(t)$) are sampled at f_s by band-pass ADCs, and the sample rate (f_s) is chosen to be four times the center frequency ($f_s = 1/T_s = 4f_c$) to simplify digital down conversion. Then, sampled signals are represented as:

$$x_k(t = nT_s) = x_k[n] = \cos\left[\frac{n\pi}{2}(1 + 4T_s\Delta f) + \varphi - k\theta\right]. \tag{2.5}$$

The sampled signals are fed to a digital I/Q down converter, and the outputs of the down converter ($i_k[n]$ and $q_k[n]$) are given by:

$$i_k[n] = \cos[2\pi f_c nT_s]\, x_k[n] = \cos\left[\frac{n\pi}{2}\right] x_k[n], \tag{2.6}$$

$$q_k[n] = -\sin[2\pi f_c n T_s]\ x_k[n] = -\sin\left[\frac{n\pi}{2}\right] x_k[n]. \tag{2.7}$$

Using equation (2.5), equation (2.6) and (2.7) can be rewritten as:

$$i_k[n] = \frac{1}{2}(\cos[2\pi\Delta f n T_s + \varphi - k\theta] + \cos[2\pi\Delta f n T_s + n\pi + \varphi - k\theta]), \tag{2.8}$$

$$q_k[n] = \frac{1}{2}(\sin[2\pi\Delta f n T_s + \varphi - k\theta] - \sin[2\pi\Delta f n T_s + n\pi + \varphi - k\theta]). \tag{2.9}$$

In the above two equations, θ-dependent terms needs to be removed to make the phases of all received signals the same. For this, complex weight multiplication (CWM) is used, and the required operations are given by:

$$I_k[n] = \cos(k\theta)\, i_k[n] - \sin(k\theta)\, q_k[n], \tag{2.10}$$

$$Q_k[n] = \sin(k\theta)\, i_k[n] + \cos(k\theta)\, q_k[n], \tag{2.11}$$

where $I_k[n]$ and $Q_k[n]$ denote signals after CWM. Equation (2.10) and (2.11) can be rewritten, using equation (2.8) and (2.9), as followings:

$$I_k[n] = \frac{1}{2}(\cos[2\pi\Delta f n T_s + \varphi] + \cos[2\pi\Delta f n T_s + n\pi + \varphi - 2k\theta]), \tag{2.12}$$

$$Q_k[n] = \frac{1}{2}(\sin[2\pi\Delta f n T_s + \varphi] + \sin[2\pi\Delta f n T_s + n\pi + \varphi - 2k\theta]). \tag{2.13}$$

After the phases of all element signals are adjusted by CWM, they are summed to create I/Q beam outputs ($y_I[n]$ and $y_Q[n]$), which are given by:

$$y_I[n] = \sum_{k=0}^{N-1} I_k[n]\ = \frac{N}{2}\cos[2\pi\Delta f n T_s + \varphi] + \alpha_{II} + \alpha_{IQ}, \tag{2.14}$$

$$y_Q[n] = \sum_{k=0}^{N-1} Q_k[n]\ = \frac{N}{2}\sin[2\pi\Delta f n T_s + \varphi] + \alpha_{QQ} - \alpha_{QI}, \tag{2.15}$$

where α_{II}, α_{IQ}, α_{QQ}, and α_{QI} are high-frequency components described by:

$$\alpha_{II} = \frac{\sum_{k=0}^{N-1} cos(2k\theta)}{2}\cos[2\pi\Delta f n T_s + n\pi + \varphi], \tag{2.16}$$

$$\alpha_{IQ} = \frac{\sum_{k=1}^{N-1} sin(2k\theta)}{2}\sin[2\pi\Delta f n T_s + n\pi + \varphi], \tag{2.17}$$

$$\alpha_{QQ} = \frac{\sum_{k=0}^{N-1} cos(2k\theta)}{2} \sin[2\pi\Delta f n T_s + n\pi + \varphi], \tag{2.18}$$

$$\alpha_{QI} = \frac{\sum_{k=1}^{N-1} sin(2k\theta)}{2} \cos[2\pi\Delta f n T_s + n\pi + \varphi]. \tag{2.19}$$

The high frequency components can be removed by low-pass filtering. Then, the final outputs ($Y_I[n]$ and $Y_Q[n]$) are given by:

$$Y_I[n] = \frac{N}{2} \cos[2\pi\Delta f n T_s + \varphi], \tag{2.20}$$

$$Y_Q[n] = \frac{N}{2} \sin[2\pi\Delta f n T_s + \varphi]. \tag{2.21}$$

2.3.2 Beamforming with Amplitude-Modulated Inputs

Consider an amplitude-modulated plane wave with an incident angle of ψ, received by a linear antenna array of N elements with a spacing of d. A message signal $m(t)$ is amplitude-modulated by a carrier frequency of f_c, and the bandwidth of $m(t)$ is assumed to be much smaller than f_c. Then, the received signal at k-th antenna element is represented as:

$$x_k(t) = m(t - k\tau)\cos(2\pi f_c(t - k\tau) + \varphi), \tag{2.22}$$

where $\tau = \frac{dsin\psi}{c}$ (c is the speed of light) and φ is the initial phase of the incident wave. With the narrowband assumption, $m(t - k\tau)$ is approximated with $m(t)$, and as a result, equation (2.22) is expressed as:

$$x_k(t) = m(t)\cos(2\pi f_c t + \varphi - k\theta), \tag{2.23}$$

where $\theta = 2\pi f_c \tau$.

The received signals ($x_k(t)$) are sampled at f_s by band-pass ADCs, and the sample rate is chosen to be four times the center frequency (f_c). Then, sampled signals are represented as:

$$x_k(t = nT_s) = x_k[n] = m[n]\cos\left[\frac{n\pi}{2} + \varphi - k\theta\right]. \quad (2.24)$$

The sampled signals are fed to a digital I/Q down converter, and the I/Q outputs of the down converter ($i_k[n]$ and $q_k[n]$) are given by:

$$i_k[n] = \cos[2\pi f_c nT_s]\, x_k[n] = \cos\left[\frac{n\pi}{2}\right] x_k[n], \quad (2.25)$$

$$q_k[n] = -\sin[2\pi f_c nT_s]\; x_k[n] = -\sin\left[\frac{n\pi}{2}\right] x_k[n]. \quad (2.26)$$

Using equation (2.24), equation (2.25) and (2.26) can be rewritten as:

$$i_k[n] = \frac{m[n]}{2}(\cos[\varphi - k\theta] + \cos[n\pi + \varphi - k\theta]), \quad (2.27)$$

$$q_k[n] = \frac{m[n]}{2}(\sin[\varphi - k\theta] - \sin[n\pi + \varphi - k\theta]). \quad (2.28)$$

After CWM, equation (2.27) and (2.28) are expressed as:

$$I_k[n] = \frac{m[n]}{2}(\cos[\varphi] + \cos[n\pi + \varphi - 2k\theta]), \quad (2.29)$$

$$Q_k[n] = \frac{m[n]}{2}(\sin[\varphi] - \sin[n\pi + \varphi - 2k\theta]). \quad (2.30)$$

After the phases of all element signals are adjusted by CWM, they are summed to create I/Q beam outputs ($y_I[n]$ and $y_Q[n]$), which are given by:

$$y_I[n] = \sum_{k=0}^{N-1} I_k[n] \; = \frac{N}{2} m[n]\cos[\varphi] + \alpha_{II} + \alpha_{IQ}, \quad (2.31)$$

$$y_Q[n] = \sum_{k=0}^{N-1} Q_k[n] \; = \frac{N}{2} m[n]\sin[2\pi\Delta f nT_s + \varphi] + \alpha_{QQ} - \alpha_{QI}, \quad (2.32)$$

where α_{II}, α_{IQ}, α_{QQ}, and α_{QI} are high-frequency components described by:

$$\alpha_{II} = \frac{\sum_{k=0}^{N-1} cos(2k\theta)}{2} m[n]\cos[n\pi + \varphi], \quad (2.33)$$

$$\alpha_{IQ} = \frac{\sum_{k=1}^{N-1} sin(2k\theta)}{2} m[n]\sin[n\pi + \varphi], \quad (2.34)$$

$$\alpha_{QQ} = \frac{\sum_{k=0}^{N-1} cos(2k\theta)}{2} m[n]\sin[n\pi + \varphi], \quad (2.35)$$

$$\alpha_{QI} = \frac{\sum_{k=1}^{N-1} sin(2k\theta)}{2} m[n]\cos[n\pi + \varphi]\,, \tag{2.36}$$

After low-pass filtering, the final outputs ($Y_I[n]$ and $Y_Q[n]$) are given by:

$$Y_I[n] = \frac{N\cos[\varphi]}{2} m[n], \tag{2.37}$$

$$Y_Q[n] = \frac{N\sin[\varphi]}{2} m[n]. \tag{2.38}$$

Note that $|m[n]| = \sqrt{{Y_I}^2 + {Y_Q}^2}$ and $\varphi = \tan^{-1}\left(\frac{Y_Q}{Y_I}\right)$.

2.4 Prototype BSP Beamformers

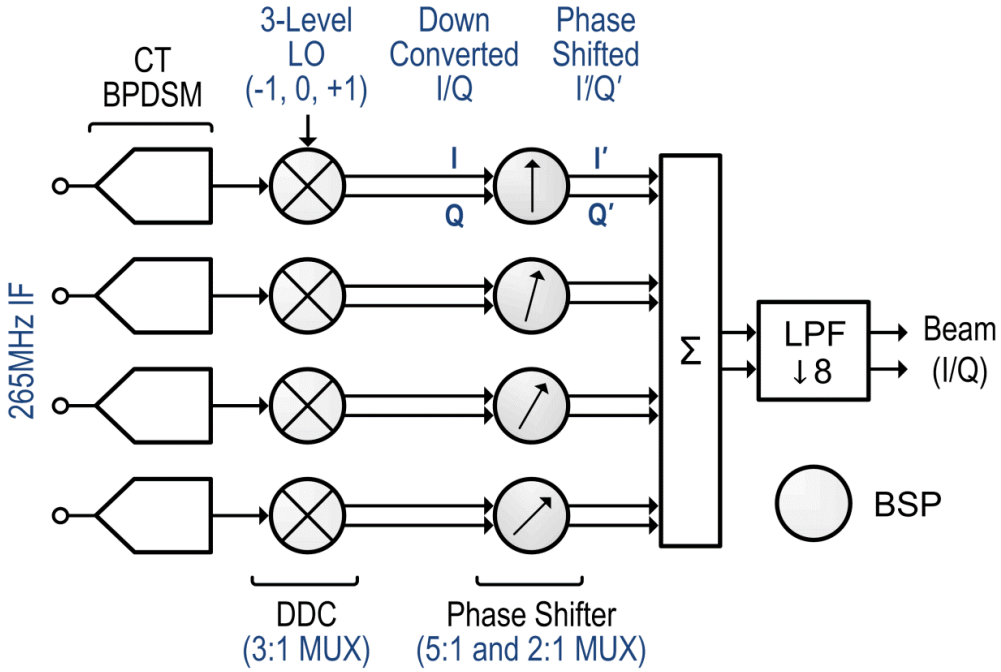


Figure 2.9 System overview of the prototype I beamformer

A block diagram of the prototype I digital beamforming IC is shown in Figure 2.9. Four 265 MHz IF signals are directly sampled at 1.06 GS/s by four CTBPDSMs. The CTBPDSM center frequency of $f_s/4$ (i.e. 265 MHz) and the five-level quantizer resolution are chosen to facilitate multiplier-less BSP. The five-level outputs of the

CTBPDSMs are down-converted to form baseband I/Q streams, and phase-shifted by 14 bit programmable complex weights, which provide a total of 496 phase-shift steps. After phase shifting, four I′/Q′ element signals are summed to create 1.06 GS/s 10 bit I/Q beam outputs. Finally, the 1.06 GS/s 10 bit I/Q beam outputs are low-pass filtered and decimated by eight to produce the overall 132.5 MS/s 13 bit I/Q beam outputs.

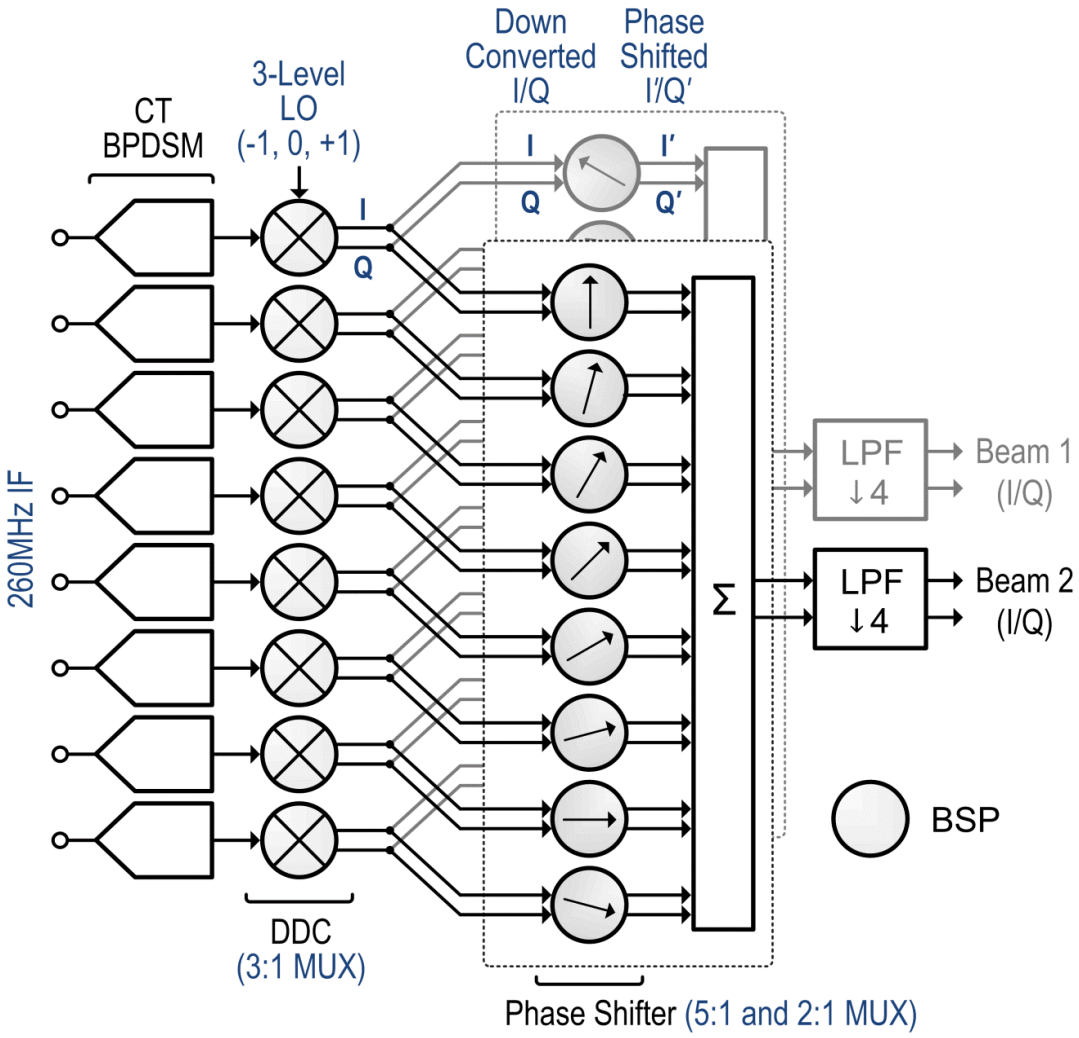


Figure 2.10 System overview of the prototype II beamformer

A block diagram of the prototype II digital beamforming IC [29] is shown Figure 2.10. Eight CTBPDSMs digitize eight 260 MHz IF input signals over a 20 MHz bandwidth to create 1.04 GS/s five-level digital outputs. To facilitate MUX-based in the following

DDC and phase shifting stages, the sample rate of the CTBPDSM (i.e. 1.04 GS/s) is chosen to be four times the 260 MHz IF, and the CTBPDSM output resolution is chosen to be five levels. After DDC, baseband I/Q streams are fed to two sets of phase shifters. Each phase shifter provides a total of 240 phase-shift steps through a 12 bit programmable complex weight. After phase shifting, eight I′/Q′ element signals are summed to create 1.04 GS/s 10 bit I/Q beam outputs. The beam outputs are finally decimated by four to produce 260 MS/s 13 bit I/Q beam outputs. The prototype II forms two simultaneous beams, and each beam can be independently configured.

2.4.1 MUX-based DDC and Phase Shifting

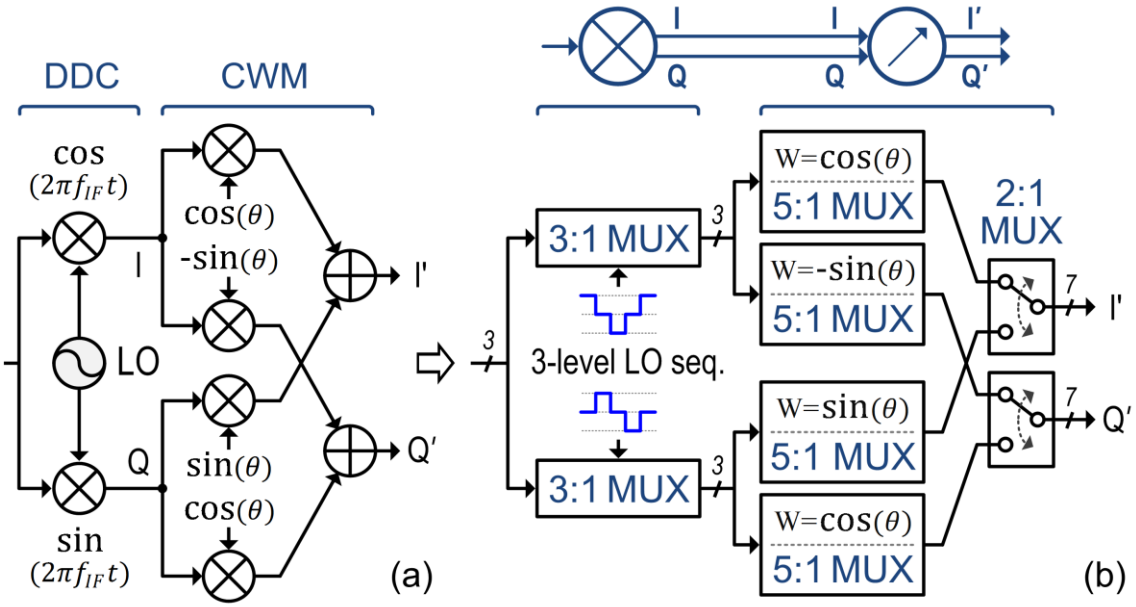


Figure 2.11 (a) DDC/CWM operations and (b) their MUX-based implementation

Figure 2.11(a) shows the operations of DDC and CWM, which normally require six multipliers and two adders. By exploiting MUX-based BSP on the five-level CTBPDSM digital outputs, the implementation of DDC and phase shifting is achieved with eight MUXs as shown in Figure 2.11(b).

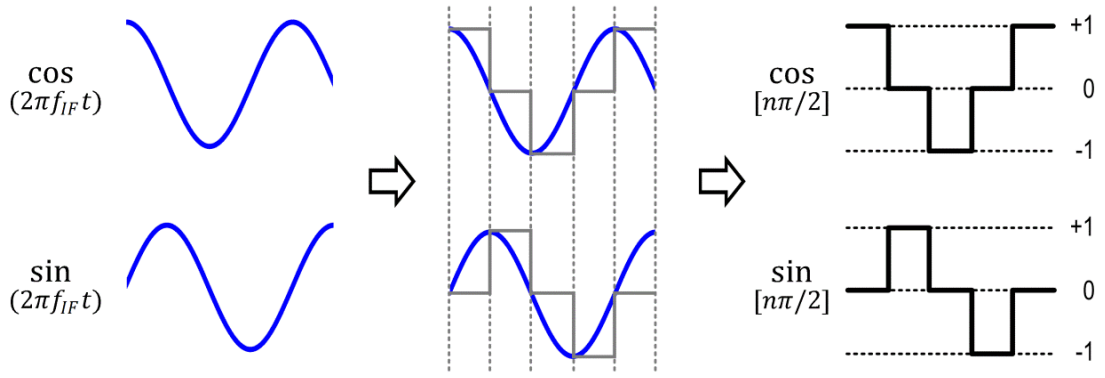


Figure 2.12 Three-level I/Q LO sequences

For DDC, the CTBPDSM digital output is multiplied by I/Q LO signals, $\cos(2\pi f_{IF}t)$ and $\sin(2\pi f_{IF}t)$, to create baseband I/Q streams as shown in Figure 2.11(a). Because the sample rate ($f_s = 1/Ts$) of the CTBPDSM is four times the input IF (f_{IF}), the required I/Q LO signals for DDC, $\cos[2\pi f_{IF}(nTs)]$ and $\sin[2\pi f_{IF}(nTs)]$, are simplified to $\cos[n\pi/2]$ and $\sin[n\pi/2]$, which are represented by only three values of -1, 0, and +1 as shown in Figure 2.12.

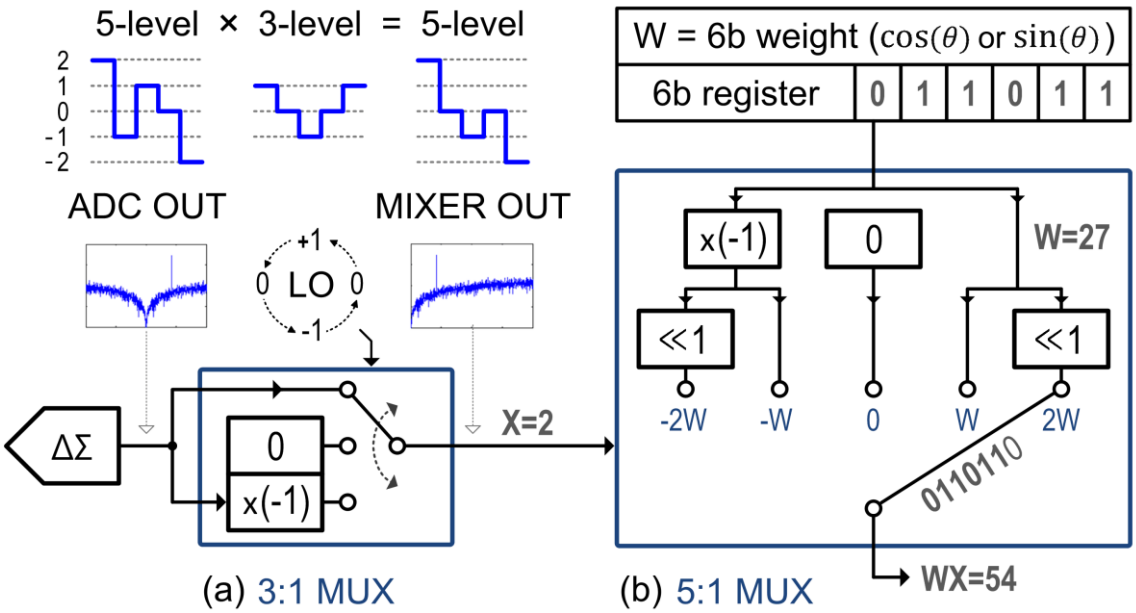


Figure 2.13 (a) DDC with a 3:1 MUX (b) Multiplication in CWM with a 5:1 MUX

As a result, a 3:1 MUX performs multiplication by three-level LO sequence as shown in Figure 2.13(a). Depending on the value of the three-level LO sequence, the five-level CTBPDSM output is passed through, zeroed, or its sign is inverted. Furthermore, since multiplication by ±1 does not change the magnitude of the signal, the down-converted I/Q streams are still represented by five levels (±2, ±1, and 0). This enables to implement multiplication with a 5:1 MUX in the following phase shifting stage.

After DDC, the five-level down-converted I/Q streams are fed to phase shifters. To achieve a phase shift of θ, each baseband I/Q stream is multiplied by weighting factors ($\cos\theta$ and $\sin\theta$), and combined to create phase-shifted I′/Q′ streams. The resolution of the weighting factor is chosen to be 7 bit for the prototype I, and 6 bit for the prototype II. In our BSP implementation, the two required operations for phase shifting (i.e. multiplication and combination) are realized by 5:1 MUXs and 2:1 MUXs as shown in Figure 2.11(b).

Figure 2.13(b) shows how a 5:1 MUX multiplies the baseband I or Q stream by a 6 bit weighting factor with a 5:1 MUX. Depending on the value of the five-level I or Q stream, the 6 bit weighting factor is zeroed, 1 bit left-shifted ($\ll 1$), or its sign is inverted. For example, when the down converter output (X) is 2 and the 6 bit weighting factor stored in the register (W) is 27, then the weighting factor is left-shifted by 1 bit, and the resulting 7 bit output of the 5:1 MUX (WX) is 54.

After the down-converted I/Q streams are multiplied by the weighting factors, they are added to create phase-shifted I′/Q′ streams. Although addition normally requires an adder, here, because the three-level LO sequences, $\cos[n\pi/2]$ and $\sin[n\pi/2]$, are alternately zero, only either the I or the Q down converter output is non-zero at any time, and

therefore this addition can be implemented with a 2:1 MUX (Figure 2.11(b)). The two 2:1 MUX outputs represent phase-shifted I′/Q′ streams, which are the result of multiplication of the baseband I/Q streams by a 12 bit complex weight of $e^{j\theta}$ ($= \cos\theta + \mathrm{j}\sin\theta$).

2.4.2 Summation

Phase-shifted I′/Q′ signals are summed to create a beam output. In the prototype I, each phase shifter I′/Q′ output is a 8 bit signal. After all four phase shifter outputs are summed, the resulting I or Q beam output is a 1.06 GS/s 10 bit signal. In the prototype II, each phase shifter I′/Q′ output is a 7 bit signal, and after summing all eight phase shifter outputs, the resulting I or Q beam output is a 1.04 GS/s 10 bit signal. The summation is performed with a conventional multi-bit adder, and followed by decimation.

2.4.3 Decimation

Decimation (or down sampling) is the process of reducing the sample rate of a signal. The outputs of oversampling ADCs are often decimated to reduce the power consumption of the following digital signal processing. Decimation requires low-pass filtering to avoid aliasing, and the low-pass filtering can be realized by a cascaded *sinc* filter. The output of the *sinc* filter is a moving average of *M* input samples, and the transfer function of the *sinc* filter ($H_{\mathrm{sinc}}(z)$) is given by:

$$H_{\mathrm{sinc}}(z) = \frac{1}{M}\sum_{0}^{M-1} z^{-1} = \frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}. \tag{2.39}$$

To decimate the output of an n-th order ΔΣ modulator, $(n+1)$ *sinc* filters need to be cascaded so that the roll-off of the cascaded filter is steeper than the slope of the shaped noise of the ΔΣ modulator. The transfer function of the cascade of *L sinc* filters is expressed as:

$$H_{\mathrm{sinc}}{}^{L}(z) = \left(\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right)^{L} = \frac{1}{M^{L}}\left(\frac{1}{1-z^{-1}}\right)^{L}(1-z^{-M})^{L}. \tag{2.40}$$

Equation (2.40) shows that the cascaded *sinc* filter can be realized by a cascade of L integrators and L differentiators. The implementation of the decimation filter is shown in Figure 2.14. In this implementation, down sampling by M is performed after the low-pass filtering.

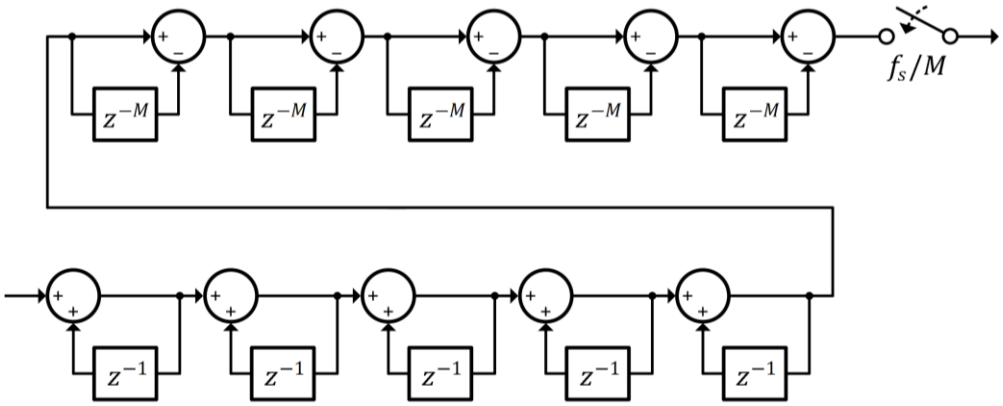


Figure 2.14 Direct implementation of the decimation filter ($L = 5$)

The decimation filter can be implemented more efficiently by separating integrators and differentiators with the down samplers as shown in Figure 2.15 [30]. In this implementation, z^{-M} is replaced with z^{-1}, and therefore differentiators can operate at a lower frequency (i.e. f_s/M).

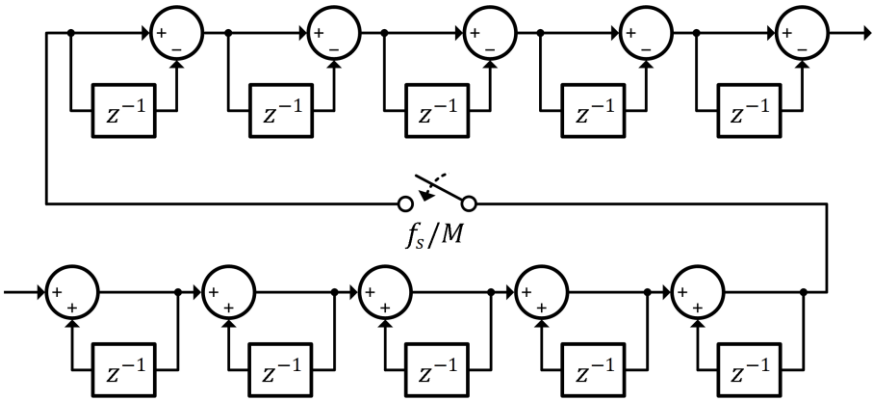


Figure 2.15 More efficient implementation of the decimation filter ($L = 5$)

The architecture shown in Figure 2.15 is used for decimation filtering in the prototype I and II beamformers. Table 2.1 summarizes the decimation filters.

Table 2.1 Summary of decimation filters used in the prototype beamformers

	Prototype I	Prototype II
Filter order (L)	5	5
Decimation ratio (M)	8	4
Input data rate [GS/s]	1.06	1.04
Output data rate [MS/s]	132.5	260
Number of input bits	10	10
Number of output bits	13	13

2.5 Comparison between DSP and BSP

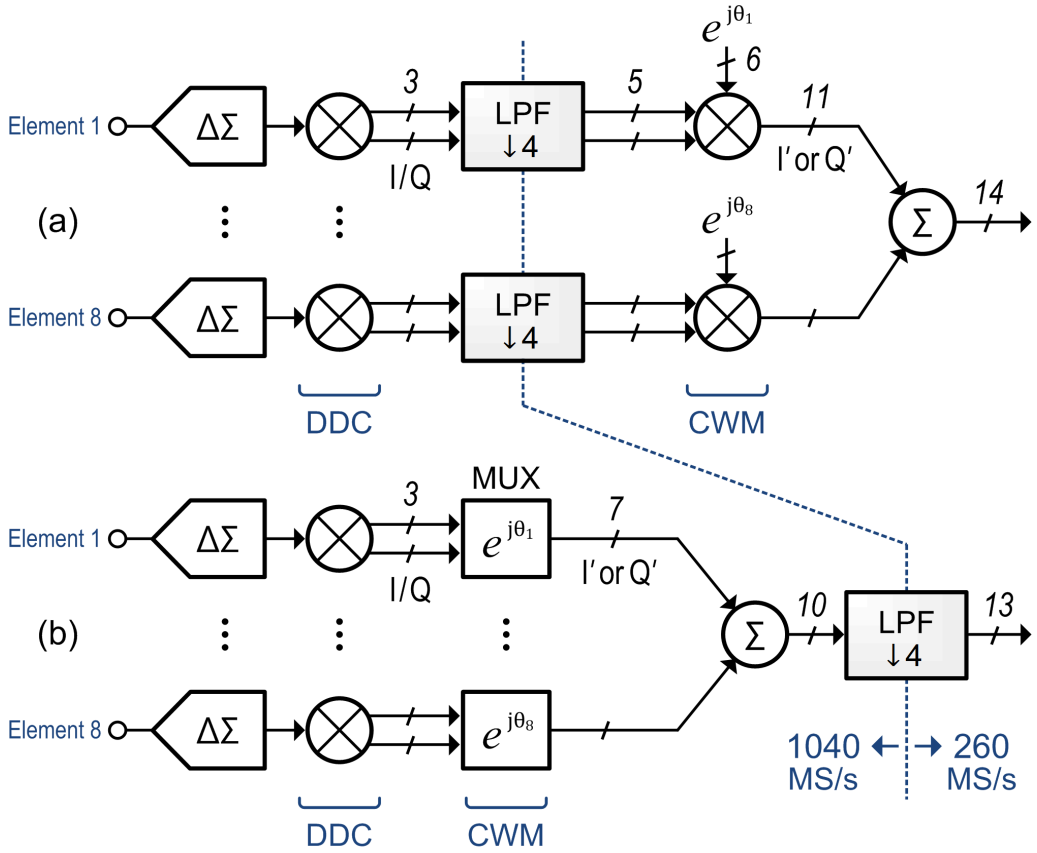


Figure 2.16 (a) DSP and (b) BSP implementations of eight-element DBF

To demonstrate the efficiency of BSP for eight-element DBF with CTBPDSMs, a BSP implementation with a single decimator (Figure 2.16(b)) is compared to a conventional DSP implementation with multiple decimators (Figure 2.16(a)). In the comparison, each implementation is synthesized with 65 nm CMOS digital standard cells, and simulated at transistor-level.

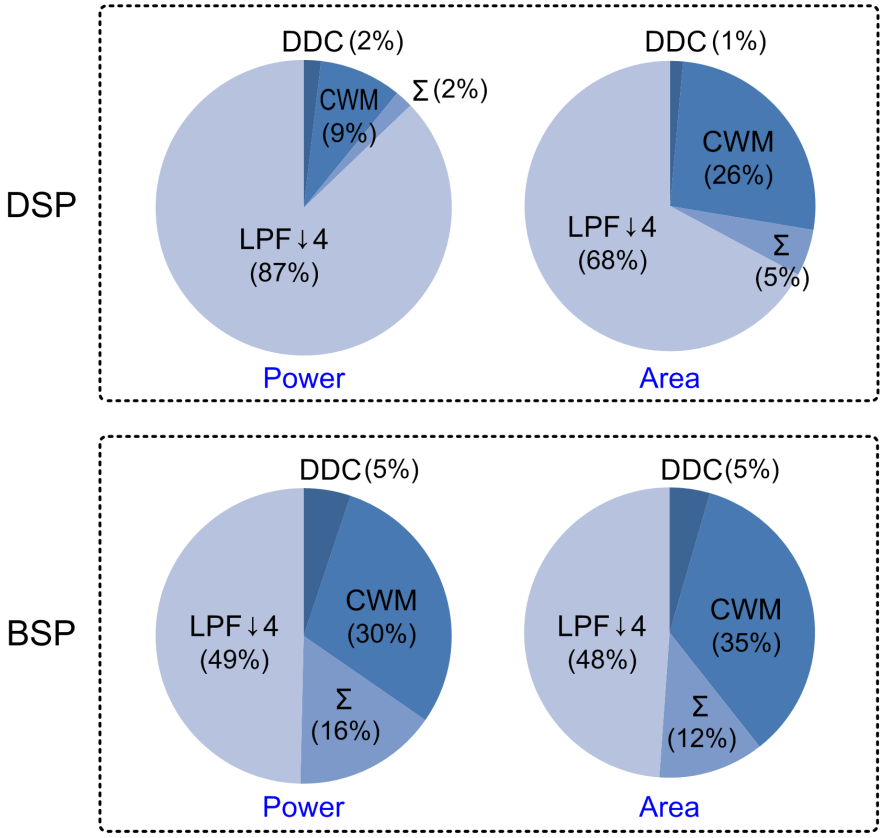


Figure 2.17 Power and area breakdown of the DSP/BSP implementations

In conventional DSP with oversampling ADCs (Figure 2.16(a)), the oversampled digital ADC outputs are low-pass filtered and decimated before further digital signal processing so that backend digital circuits operate at a lower clock rate, but with an increased word width. However, in a weighted-sum system (e.g. digital beamformer) with multiple inputs and a single output, the cost of decimation filtering increases linearly

with the number of inputs. Therefore, decimation filtering becomes a bottleneck to implementing low-power and area-efficient implementation of DBF as shown in Figure 2.17. In BSP (Figure 2.16(b)), decimation filtering, a high-cost operation, is performed only once for the final output. This, however, requires CWM for phase shifting to operate at a higher clock rate, but with a lower word width. The penalty of the higher clock rate in BSP is overcome by replacing bulky multipliers with simple MUXs. As a result, despite the higher clock rate, MUX-based weighting achieves comparable power consumption to conventional multiplier-based weighting, and greatly reduces area.

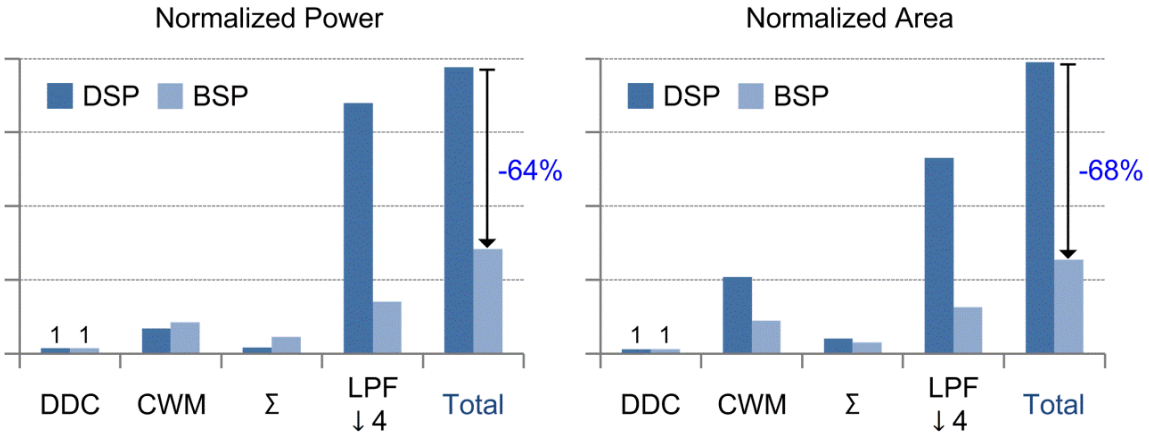


Figure 2.18 Power and area comparison between the DSP/BSP implementations

As shown in Figure 2.18, the area of the BSP implementation is only 32% of that of the conventional DSP implementation due to simple MUX-based CWM and single decimation. The power consumption of the BSP implementation is only 36% of that of the DSP implementation.

CHAPTER 3 Continuous-Time Band-Pass ΔΣ Modulator

Digital beamformer requires a large number of ADCs, and therefore the power consumption and area of the ADC have a large bearing on the power consumption and area of the entire beamformer. To achieve an area-efficient implementation, the prototype 4th order CTBPDSM is based on single op-amp resonators [26] instead of bulky LC-tank resonators. The feedback structure is also modified to save power and area.

3.1 Architecture

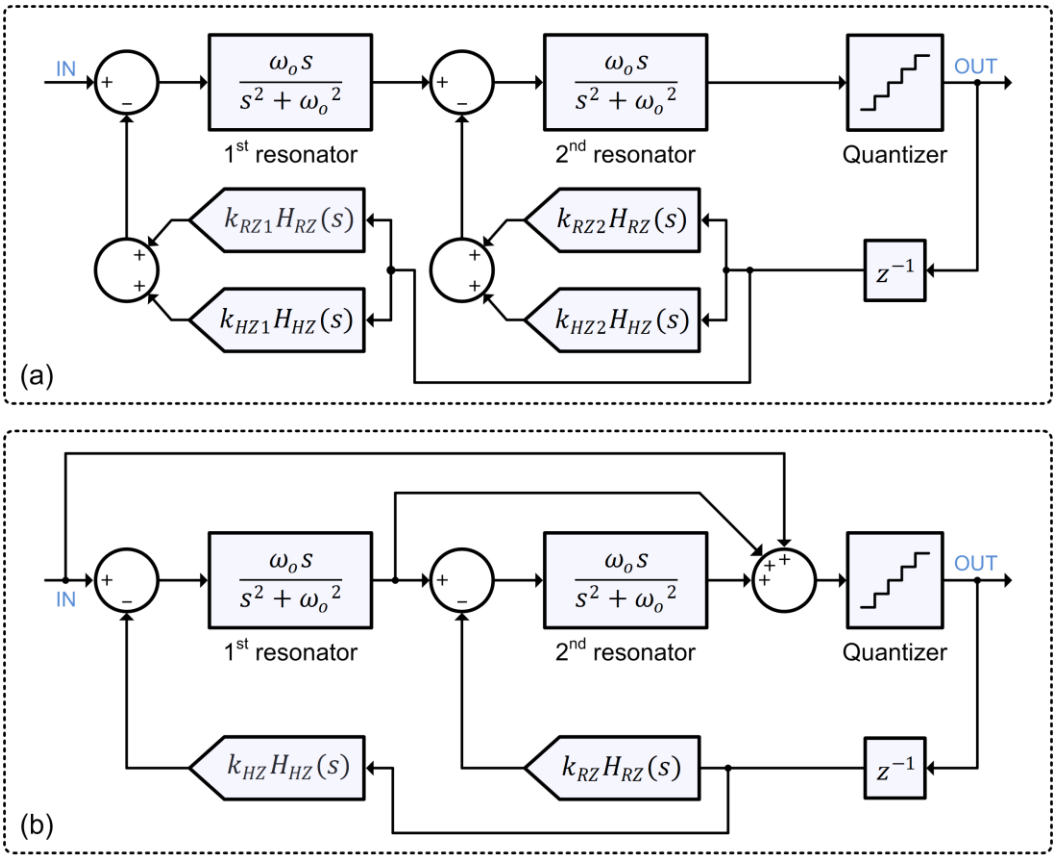


Figure 3.1 (a) CTBPDSM in [31] (b) CTBPDSM in [26]

A conventional 4th order CTBPDSM architecture [31] is shown in in Figure 3.1(a). This architecture requires a pair of feedback DACs, consisting of a return-to-zero (RZ) DAC and a half-clock-delayed return-to-zero (HZ) DAC per each resonator. This multi-path feedback architecture perfectly transforms a DT band-pass ΔΣ modulator into a CT counterpart with LC-tank resonators. However, this architecture requires bulky inductors, and two feedback DACs per each resonator. These increase power consumption and area.

A low-power and area-efficient architecture is proposed in [26]. In the architecture, single op-amp resonators replace LC-tank resonators, and two feed-forward paths are introduced to reduce the number of feedback DACs (Figure 3.1(b)). The feed-forward paths also reduce the output swings of the resonators. However, adding feed-forward path degrades the anti-alias filtering of the modulator.

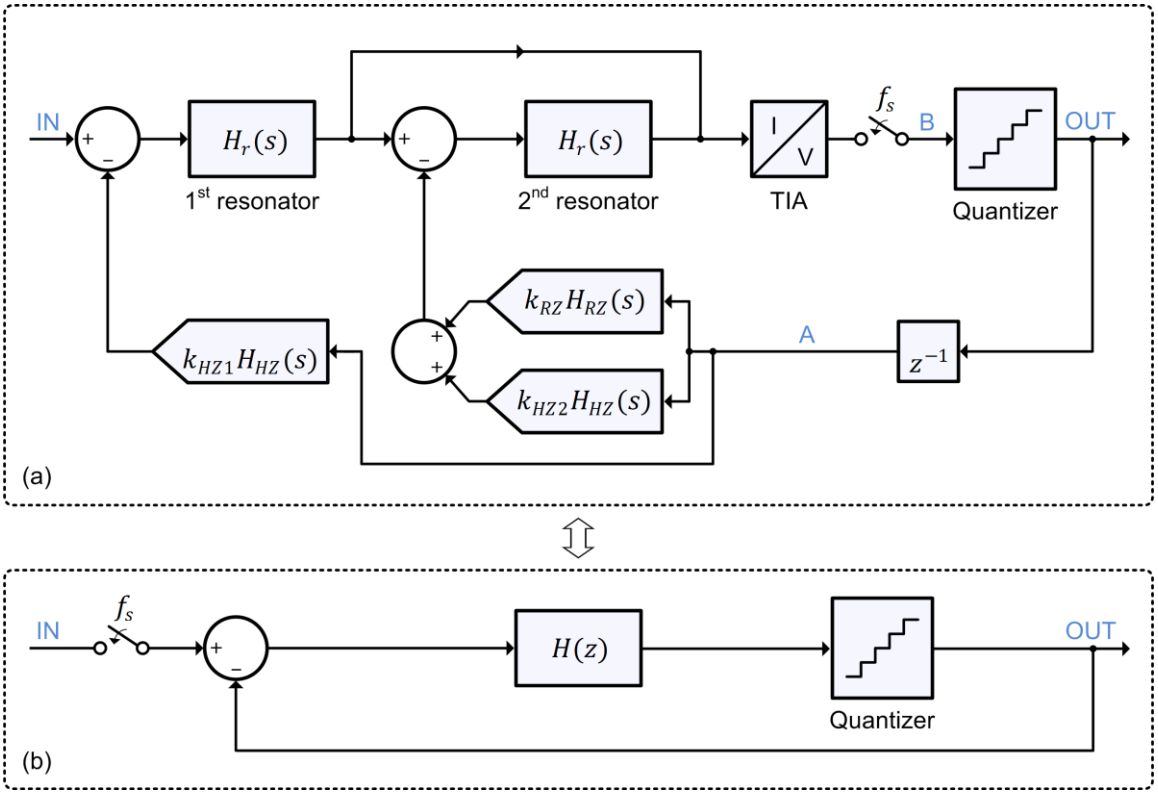


Figure 3.2 (a) Prototype CTBPDSM architecture and (b) its equivalent DT model

The prototype 4th order CTBPDSM architecture is shown in Figure 3.2(a). In the architecture, a single feed-forward path around the 2nd resonator is used. The feed-forward path removes the need for the RZ DAC to the 1st resonator input, which directly contributes to the input-referred noise of the modulator. The feed-forward path also reduces the output swing of the 2nd resonator, achieving lower power consumption and better linearity. Since there is no feed-forward path around the 1st resonator, the anti-alias filtering from the 1st resonator is fully retained without degradation. The current through the feed-forward path is combined with the output current from the 2nd resonator, and then converted to a voltage by a transimpedance amplifier (TIA). A five-level quantizer digitizes this voltage, and the sample rate is chosen to be four times the input IF.

The loop filter transfer function ($H(z)$) of the equivalent DT modulator shown in Figure 3.2(b) can be found by the impulse-invariant transformation. For the CT-to-DT equivalency, the loop impulse response of the CT modulator at the sampling time (nT_s) needs to be the same as the loop impulse response of the DT modulator as:

$$\mathcal{Z}^{-1}\{-zH(z)\} = \mathcal{L}^{-1}\{L_{AB}(s)\}\big|_{t=nT_s}, \tag{3.1}$$

where $L_{AB}(s)$ is a loop transfer function from A to B in Figure 3.2(a), and the pulse shaping functions of a RZ DAC ($H_{RZ}(s)$) and a HZ DAC ($H_{HZ}(s)$) are given by:

$$H_{RZ}(s) = \frac{1-e^{-sT_S/2}}{s}, \tag{3.2}$$

$$H_{HZ}(s) = e^{-sT_S/2}\frac{1-e^{-sT_S/2}}{s}. \tag{3.3}$$

The loop transfer function from A to B ($L_{AB}(s)$) is expressed as:

$$L_{AB}(s) = \big(L_1(s) + L_2(s)\big)\,R_{TIA}, \tag{3.4}$$

where R_{TIA} is the gain of the transimpedance amplifier (TIA),

$$L_1(s) = -k_{HZ1}H_{HZ}(s)\,H_r(s)\,\big(1 + H_r(s)\big), \tag{3.5}$$

$$L_2(s) = -\big(k_{HZ2}H_{HZ}(s) + k_{RZ}H_{RZ}(s)\big)\,H_r(s). \tag{3.6}$$

The transfer function of the resonator ($H_r(s)$) is given by equation (3.12). With k_{RZ} = 2×10^{-4}, k_{HZ1} = -2×10^{-4}, k_{HZ2} = -3×10^{-4}, and R_{TIA} = 2×10^{3}, the modulator is stabilized, and the SNR is maximized. Figure 3.3 shows the simulated PSD of the modulator output, and the SNR is 60 dB over a 20 MHz bandwidth around $f_s/4$ (i.e. 250 MHz).

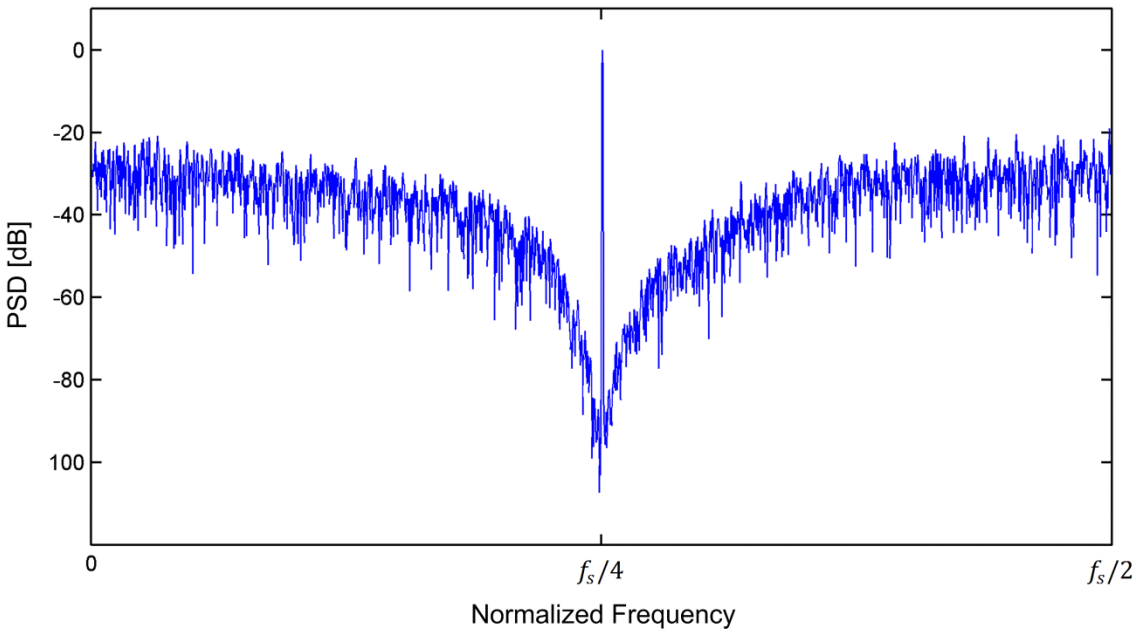


Figure 3.3 Simulated PSD in Matlab (f_s =1 GHz and f_{in} = 250.24 MHz)

The $H(z)$ of the designed modulator is expressed as:

$$H(z) \approx \frac{-0.32\left(z^2-0.01+0.65\right)}{(z^2+0.98)^2}. \tag{3.7}$$

The signal transfer function (STF) and noise transfer function (NTF) of the modulator are given by:

$$\mathrm{STF}(z) = \frac{H(z)}{1+H(z)}, \tag{3.8}$$

$$\mathrm{NTF}(z) = \frac{1}{1+H(z)}. \tag{3.9}$$

The pole-zero maps of the STF and NTF are shown in Figure 3.4.

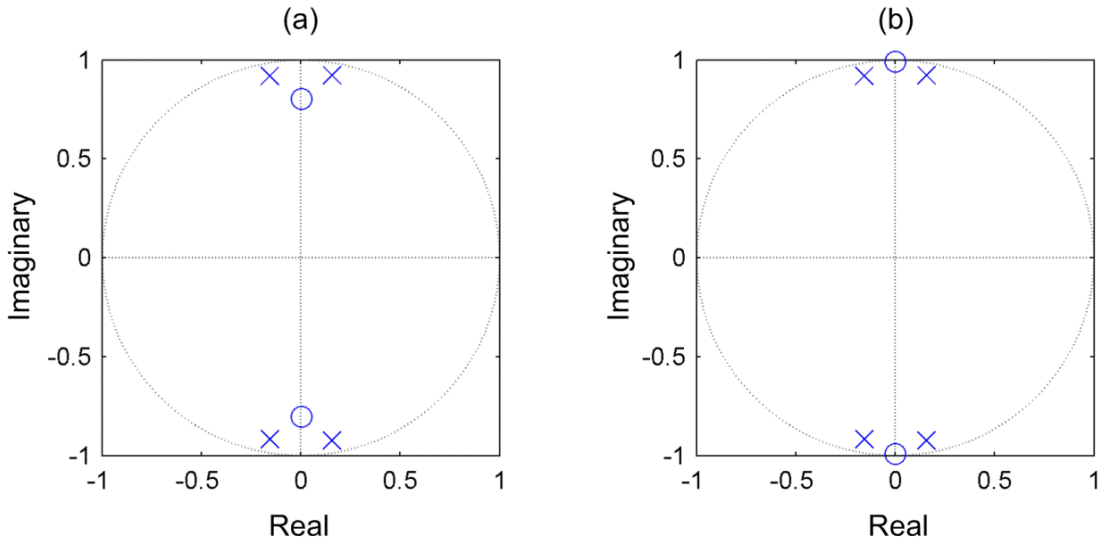


Figure 3.4 Pole-zero maps of the (a) STF and (b) NTF

3.2 Circuit Implementation

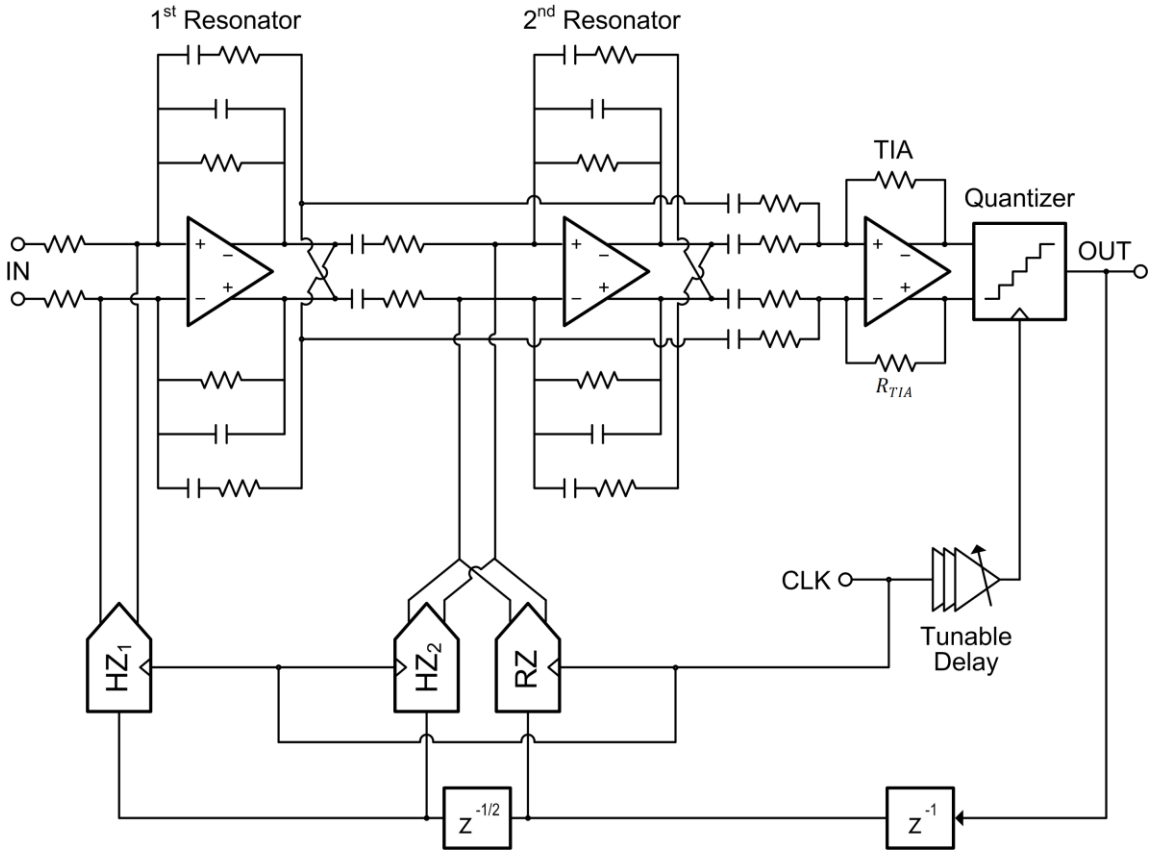


Figure 3.5 Circuit implementation of the 4th order CTBPDSM

Figure 3.5 shows the circuit implementation of the 4th order prototype CTBPDSM. In the modulator, single op-amp resonators [26] are much smaller than conventional LC-tank resonators, enabling a compact (0.03 mm^2) implementation of the CTBPDSM. The five-level quantizer is implemented with a flash ADC with four comparators. Any excessive loop delay in the feedback path is corrected by a 3 bit tunable delay, which aligns the quantizer sampling time and the time when the DAC current is fed back to the resonator input.

3.2.1 Single Op-Amp Resonator

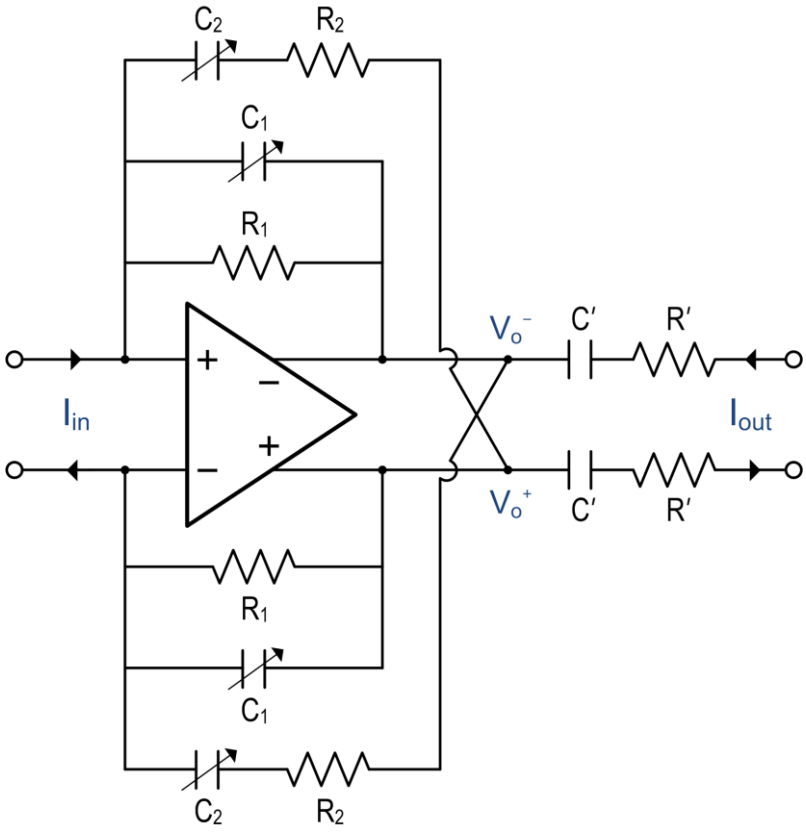


Figure 3.6 Single op-amp resonator [26]

A schematic of the single op-amp resonator is shown in Figure 3.6, and the transfer function of the resonator ($H_r(s)$) is expressed as:

$$H_r(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{R_1}{R'} \frac{1+\tau_2 s}{1+\tau' s} \frac{\tau' s}{1+(\tau_1+\tau_2-R_1C_2)s+\tau_1\tau_2 s^2}, \quad (3.10)$$

where $\tau_1 = R_1C_1$, $\tau_2 = R_2C_2$, and $\tau' = R'C'$. To derive equation (3.10), we assume that the op-amp is ideal and the inputs are virtual grounds. In addition, the outputs of the resonator are also assumed to be connected to virtual grounds since they are connected to the inputs of the next resonator (or the TIA) in the CTBPDSM, which are virtual grounds. When $\tau_1 = \tau_2 = \tau' = \tau$, equation (3.10) is simplified as:

$$H_r(s) = \frac{R_1}{R'} \frac{\omega_o s}{s^2+(\omega_o/Q)s+{\omega_o}^2}, \quad (3.11)$$

where $\omega_o = 1/\tau$ and $Q = \tau/(2\tau - R_1C_2)$. Choosing $R_1 = R$, $C_1 = C$, $R_2 = R/2$, $C_2 = 2C$, $R' = 2R$, $C' = C/2$ gives $\tau = RC$ and $Q = \infty$. As a result, equation (3.11) is expressed as:

$$H_r(s) = \frac{0.5\ \omega_o s}{s^2+{\omega_o}^2}. \quad (3.12)$$

The center frequency (ω_o) is designed to be 265 MHz for the prototype I, and 260 MHz for the prototype II. Process variation and mismatch of resistors and capacitors can result in a center frequency shift, and a finite Q factor. To adjust the center frequency and to maximize the Q factor, C_1 and C_2 are implemented as tunable capacitors with a 4 bit resolution.

Although the 1st resonator in the prototype CTBPDSM has two output branches due to the feed-forward path, the transfer function from the resonator input to each output branch is still represented by equation (3.12). When the resonator has two identical output branches as shown in Figure 3.7, resistors (R') and capacitors (C') in the branches can be merged for analysis, resulting in an equivalent single branch with halved resistance and doubled capacitance. The time constant of the equivalent single branch is

still $R'C'$, which is the same as the time constant when there is no feed-forward branch. With the same time constant, the transfer function of the resonator with the two identical output branches ($H_r'(s)$) is two times of $H_r(s)$ in equation (3.12) because R' in equation (3.11) is replaced with $0.5R'$. As a result, the transfer function ($H_r'(s)$) is given by:

$$H_r'(s) = \frac{I_{out}'(s)}{I_{in}(s)} = \frac{\omega_o s}{s^2 + {\omega_o}^2}. \tag{3.13}$$

The output current of the resonator ($I_{out}'(s)$) is equally divided to each output branch. Therefore, the transfer function from I_{in} to I_{out1} (or I_{out2}) is half of $H_r'(s)$ in equation (3.13), which is the same as $H_r(s)$ in equation (3.12) as follows:

$$\frac{I_{out1}(s)}{I_{in}(s)} = \frac{I_{out2}(s)}{I_{in}(s)} = \frac{0.5\,\omega_o s}{s^2 + {\omega_o}^2}. \tag{3.14}$$

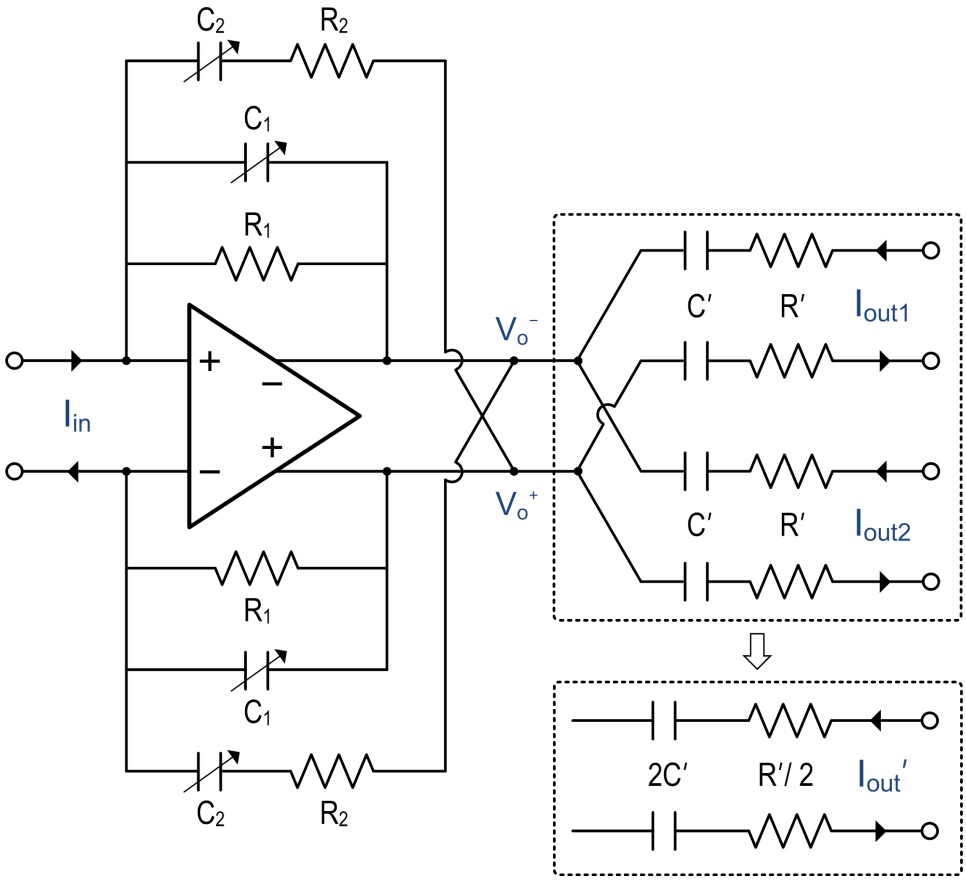


Figure 3.7 Single op-amp resonator with two identical output branches

3.2.2 Quantizer

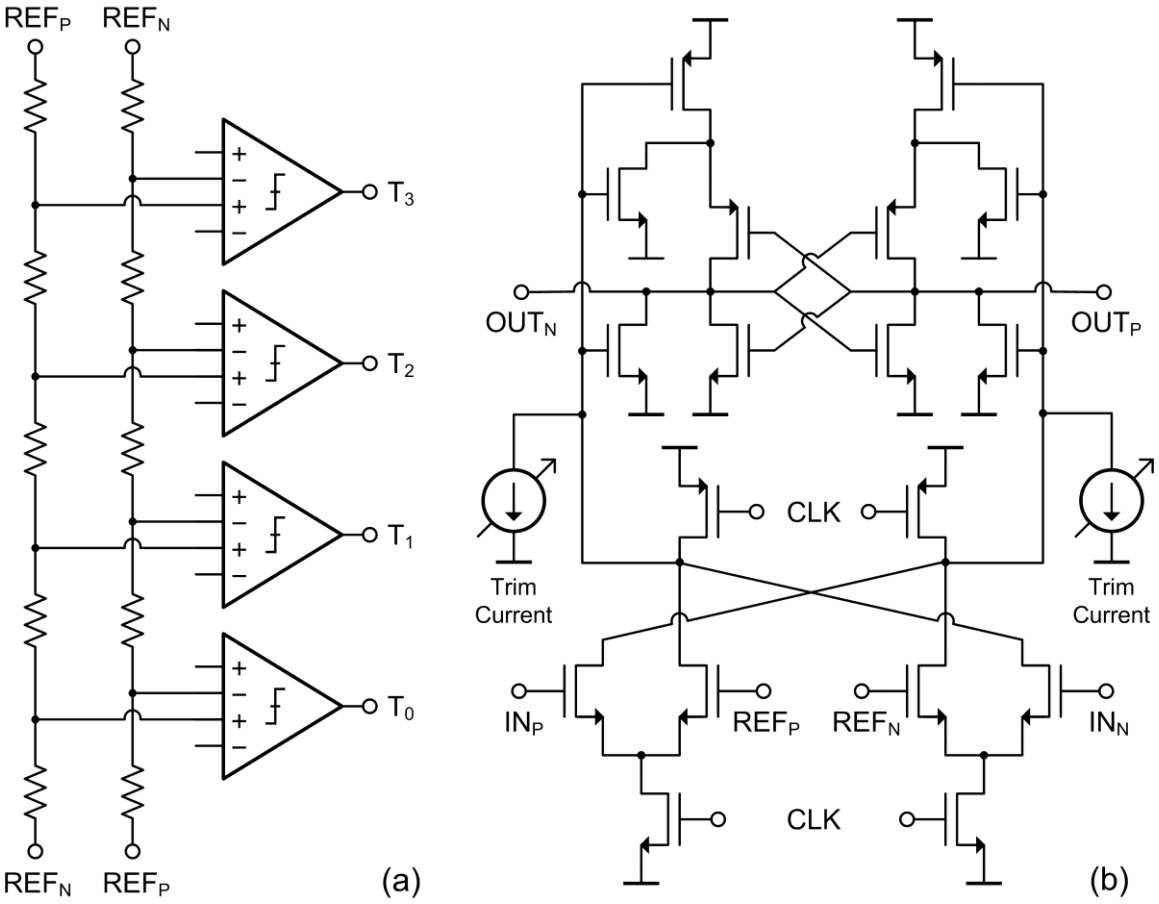


Figure 3.8 (a) Five-level quantizer (b) Double-tail dynamic comparator

Figure 3.8(a) shows the five-level quantizer (flash ADC) which consists of four comparators and two resistor ladders. With the double-tail dynamic comparator [32] shown in Figure 3.8(b), the input devices can be sized small to minimize input capacitance while the tail current of the output latch is large for fast regeneration. Comparator offsets are calibrated by two 4 bit trim currents [33]. The comparators are followed by SR latches to hold the output for an entire clock period. The output thermometer code (i.e. T_3, T_2, T_1, and T_0) directly drives current steering DACs. A summer converts the thermometer code to a 3 bit binary value [34].

3.2.3 Current Steering DAC

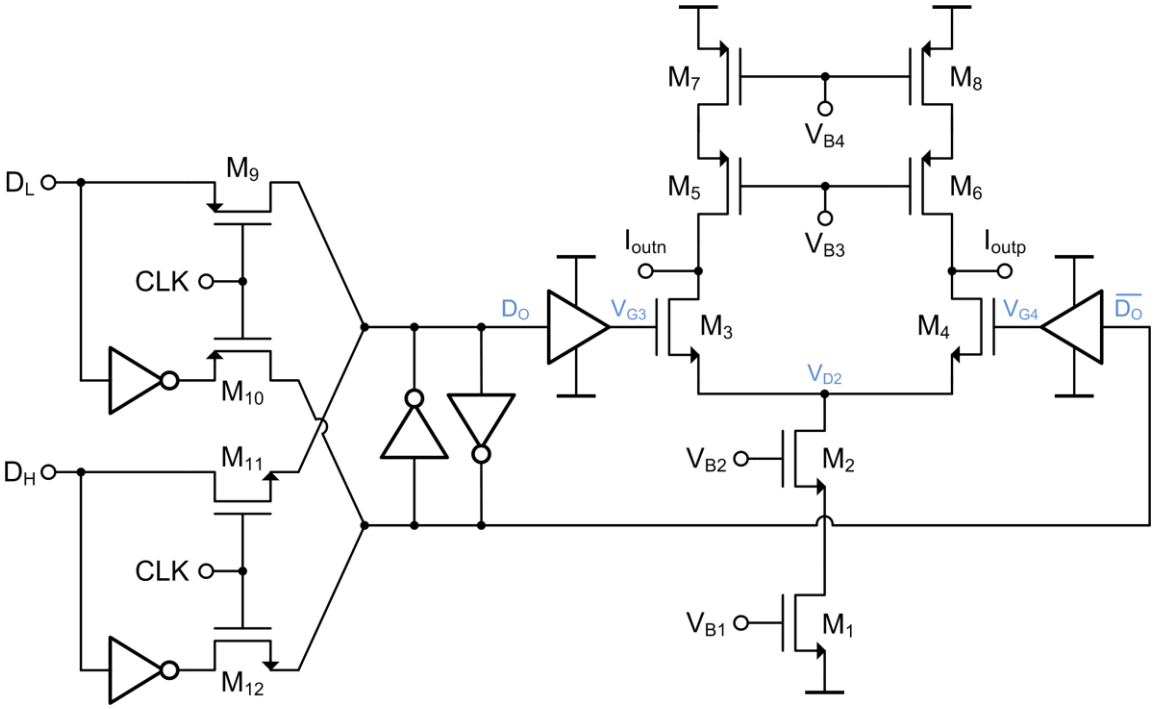


Figure 3.9 Unit current cell of the DAC

The current steering DAC consists of four unit current (I_{LSB}) cells driven by the 4 bit thermometer code from the quantizer. As shown in Figure 3.9, each unit current cell is composed of current source devices (M_1, M_7, and M_8), cascode devices (M_2, M_5, and M_6), switch devices (M_3 and M_4), and a latch. The unit current (I_{LSB}) through M_1 is steered to one of the DAC outputs. M_7 and M_8 inject a fixed current of half of the unit current to each DAC output. This injected current through M_7 and M_8 ensures a net DC current of zero from the DAC to the input of the resonator.

The current source devices (M_1, M_7, and M_8) are biased with high overdrive voltages to reduce thermal noise. The high overdrive voltage of M_1 also reduces mismatch of the unit current, and therefore improves the linearity of the DAC. The noise and linearity performances are especially important for the DAC connected to the 1st resonator input.

The cascode devices (M_2, M_5, and M_6) increase the output impedance of the DAC, and the linearity of the DAC is improved with the increased output impedance. In addition, M_2 isolates the large drain capacitance of M_1 from switch devices to achieve a fast settling time of the output current.

The latch has two digital inputs (D_L and D_H), and provides complementary outputs (D_O and $\overline{D_O}$) to drive the switch devices (M_3 and M_4). When the clock (CLK) is low, M_9 and M_{10} are turned on, and D_L and $\overline{D_L}$ are transferred to the outputs. When the clock is high, M_{11} and M_{12} are turned on, and D_H and $\overline{D_H}$ are transferred to the outputs. Since one of the two digital inputs (D_L and D_H) and its complementary signal are transferred to the outputs depending on the clock, both RZ and HZ operations can be realized with the latch. Depending on the DAC configuration (RZ or HZ), one of the two digital inputs are connected to the thermometer code from the quantizer, and the other is tied to the supply or ground. When the switch devices are driven by the complementary outputs, the gate voltages of the switch devices (V_{G3} and V_{G4}) cross each other at a high voltage (close to the supply voltage) so that at least one of the switch devices is always conducting current. The high-crossing gate voltages avoid a large voltage drop at the drain of the cascode device (V_{D2}), achieving a fast settling time of the output current.

CHAPTER 4 Measurements

4.1 Prototype I

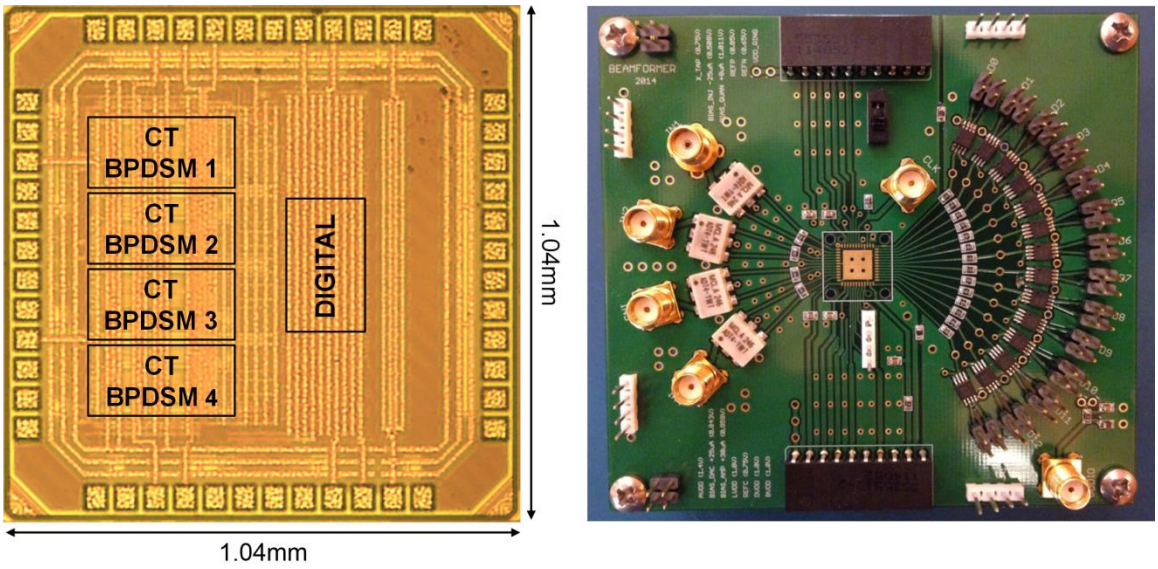


Figure 4.1 Die micrograph of the prototype I and PCB for measurements

The four-element prototype I digital beamforming IC is fabricated in 65 nm CMOS, and occupies a core area of 0.16mm^2 including 0.04mm^2 for the synthesized digital implementation of the BSP beamforming. A die micrograph and a PCB for measurements are shown in Figure 4.1. The prototype I consumes 67.1 mW from 1.0 V (digital) and 1.4 V (analog) supplies.

The prototype I beamformer contains four CTBPDSMs. Each CTBPDSM consumes 12 mW, and occupies 0.03 mm^2. The PSD of a single CTBPDSM is shown in Figure 4.2. The measured SNDR of a single CTBPDSM for a 265.06 MHz sinusoid over a 20 MHz bandwidth is 52.5 dB.

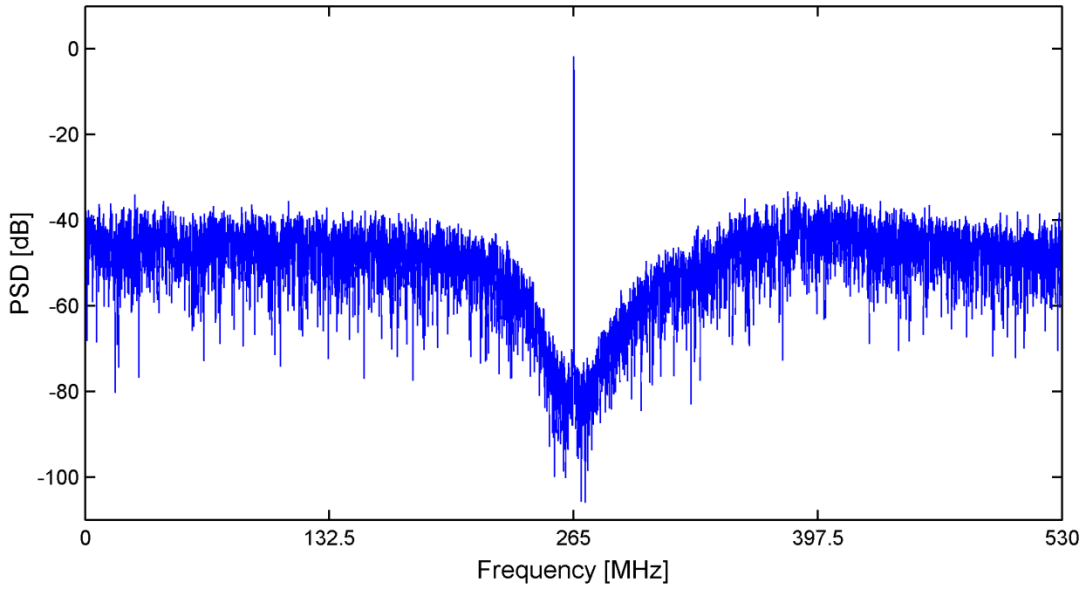


Figure 4.2 PSD of the CTBPDSM output (f_{in} = 265.06 MHz)

Each CTBPDSM output is down-converted to baseband. Figure 4.3 shows the PSD of the down-converted single element signal. As shown in Figure 4.3, a 270.89 MHz sinusoidal input is down-converted to 5.89 MHz, and the measured SNDR is 50.9 dB on average over a 10 MHz bandwidth.

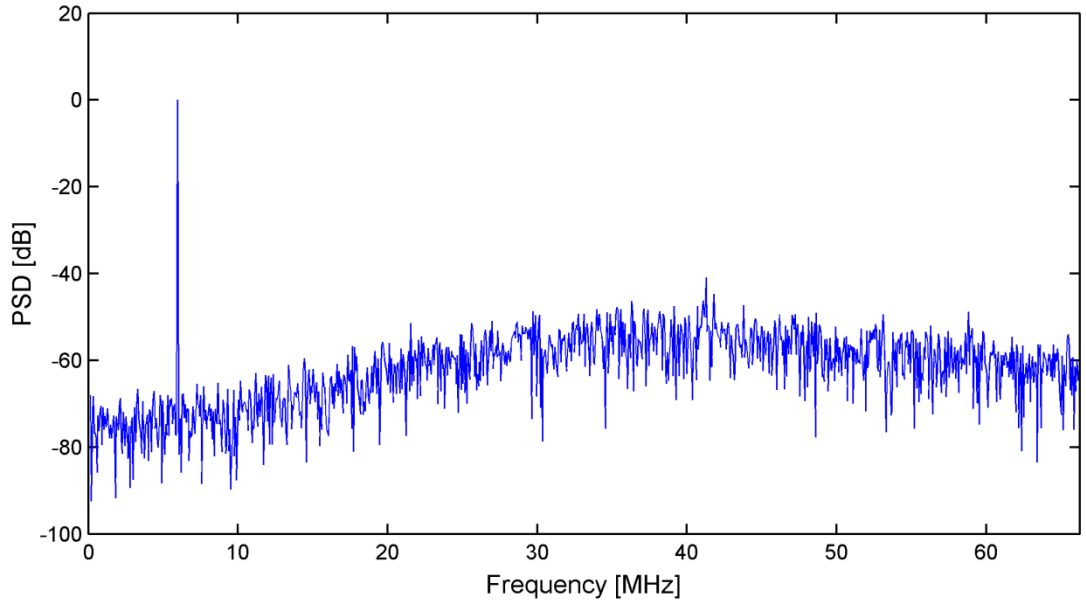


Figure 4.3 PSD of the down-converted single element signal (f_{in} = 270.89 MHz)

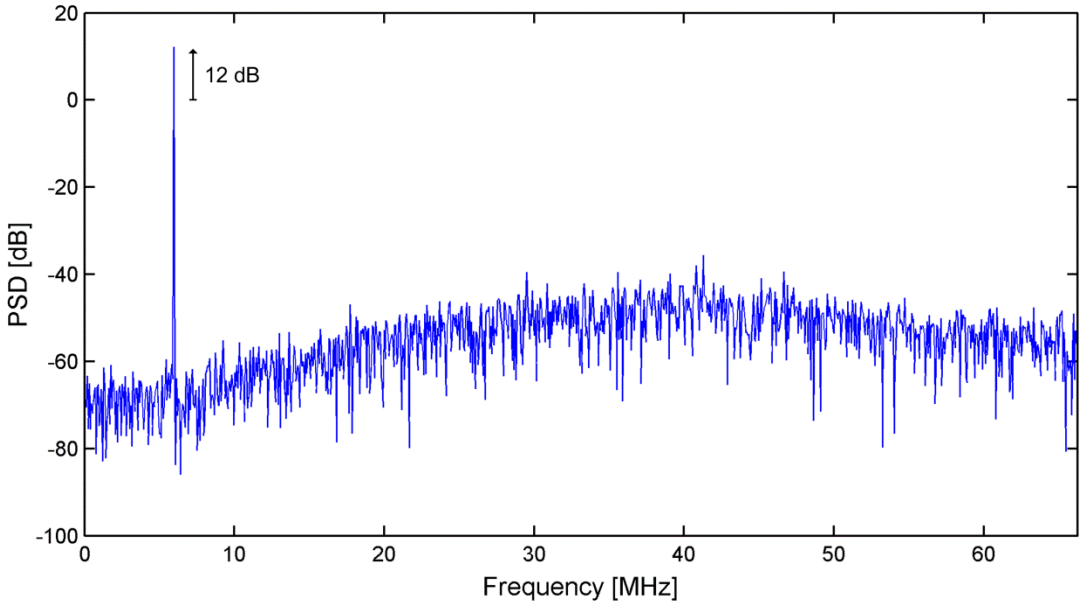


Figure 4.4 PSD of the beam with constructive combination (f_{in} = 270.89 MHz)

When the four down-converted 5.89 MHz element signals are constructively combined after phase shifting, the fundamental tone increases by 12 dB while the channel noise is uncorrelated, resulting in an overall SNDR of 56.6 dB with an 5.7 dB improvement over a 10 MHz bandwidth (Figure 4.4).

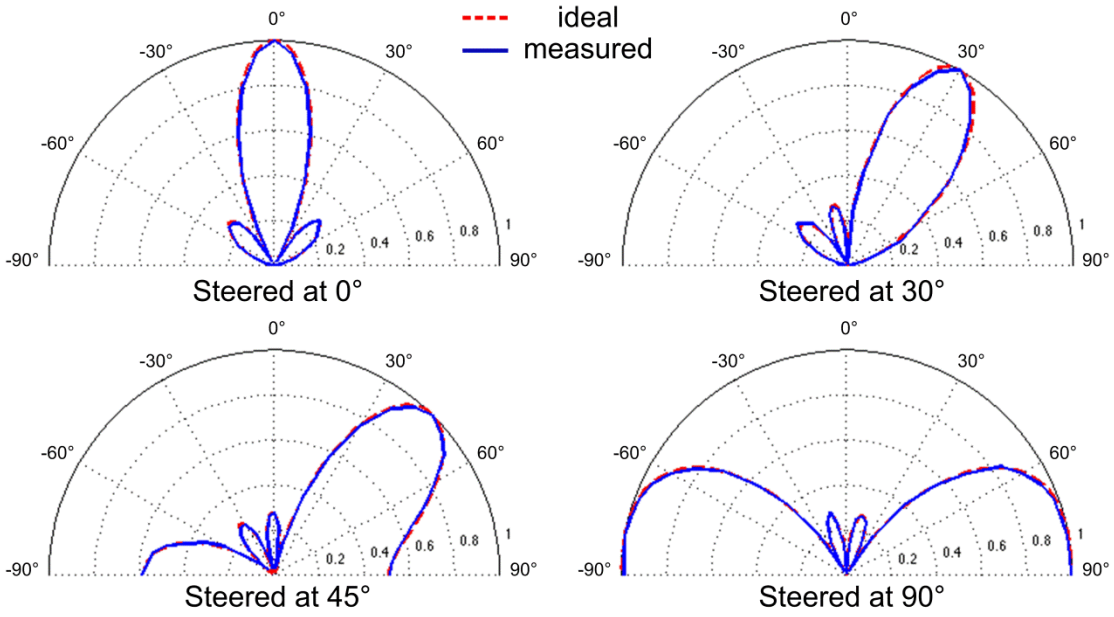


Figure 4.5 Ideal and measured beam patterns

The ideal and measured beam patterns for four different steering angles are plotted in Figure 4.5. For the measurements, four direct digital synthesizers (DDSs) generate four poly-phase 270.89 MHz sinusoidal inputs to mimic the received signals from an antenna array with λ/2 spacing.

The performance of the prototype I is summarized in Table 4.1.

Table 4.1 Performance summary of the prototype I beamformer

<table>
<tr><td colspan="2">Number of elements</td><td colspan="2">4</td></tr>
<tr><td colspan="2">Number of beams</td><td colspan="2">1</td></tr>
<tr><td colspan="2">Input IF [MHz]</td><td colspan="2">265</td></tr>
<tr><td colspan="2">IF bandwidth [MHz]</td><td colspan="2">20</td></tr>
<tr><td colspan="2">Sample rate [GS/s]</td><td colspan="2">1.06</td></tr>
<tr><td colspan="2">Overall array SNDR [dB]</td><td colspan="2">56.6</td></tr>
<tr><td colspan="2">SNDR improvement [dB]</td><td colspan="2">5.7</td></tr>
<tr><td colspan="2">Technology</td><td colspan="2">65 nm CMOS</td></tr>
<tr><td rowspan="2">Power [mW]</td><td>CTBPDSMs</td><td>$12 \times 4 = 48$</td><td rowspan="2">67.2</td></tr>
<tr><td>DBF core</td><td>19.2</td></tr>
<tr><td rowspan="2">Core area [mm^2]</td><td>CTBPDSMs</td><td>$0.03 \times 4 = 0.12$</td><td rowspan="2">0.16</td></tr>
<tr><td>DBF core</td><td>0.04</td></tr>
</table>

4.2 Prototype II

The eight-element two-beam prototype II digital beamforming IC [29] is fabricated in 65 nm CMOS. A die micrograph and a PCB for measurements are shown in Figure 4.6. The prototype II consumes 123.7 mW, and occupies 0.28 mm^2. The prototype II beamformer contains eight CTBPDSMs. Each modulator consumes 13.1 mW from a 1.4 V supply, and occupies 0.03 mm^2, which is almost an order of magnitude smaller than the CTBPDSM in [26]. The outputs of the eight CTBPDSMs are fed to the Verilog

synthesized DBF core, which consumes 18.9 mW (15% of the total power consumption) from a 0.9 V supply, and occupies 0.04 mm^2 (14% of the total area).

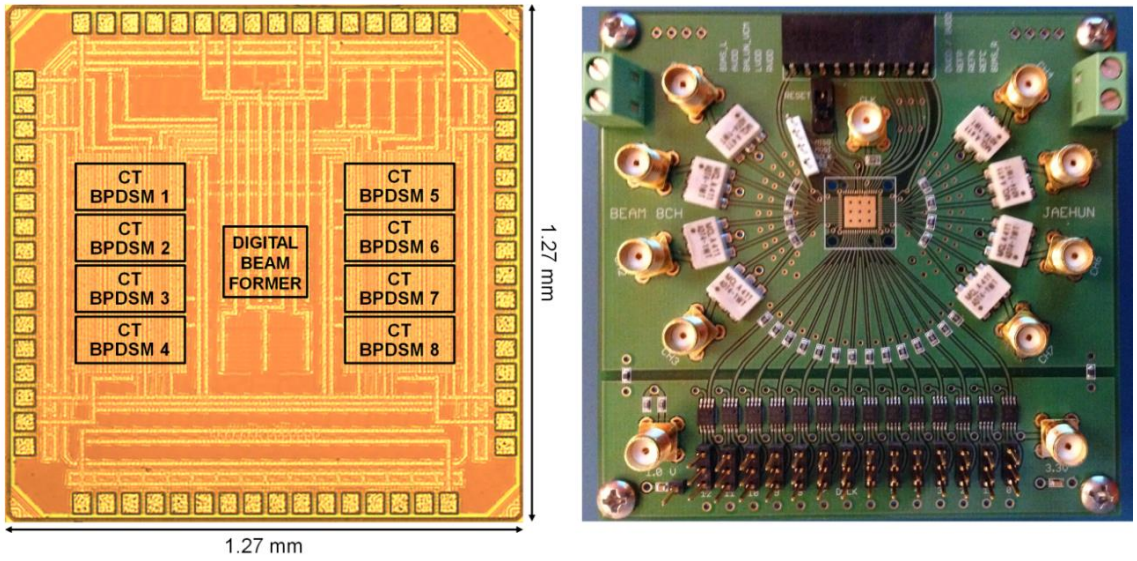


Figure 4.6 Die micrograph of the prototype II and PCB for measurements

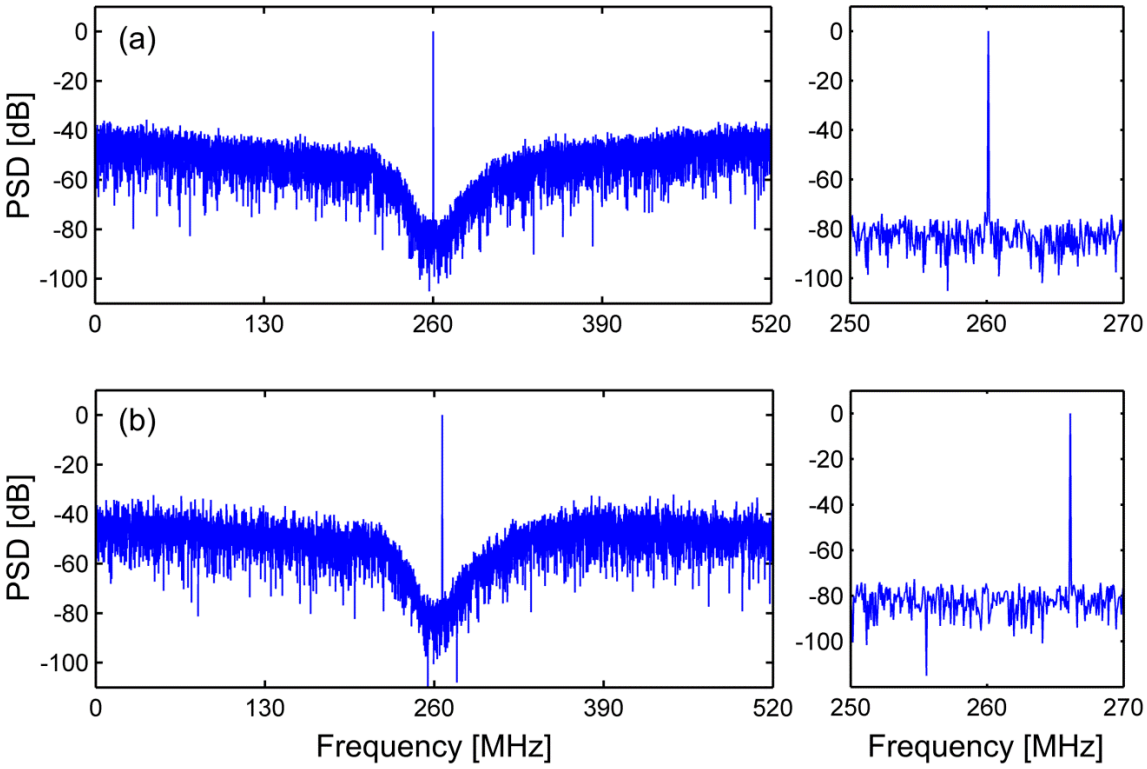


Figure 4.7 PSD of the CTBPDSM output for (a) 260 and (b) 266 MHz inputs

The measured PSD of the CTBPDSM output is shown in Figure 4.7 for 260 and 266 MHz sinusoidal inputs. The measured SNDR is 56 dB for both input frequencies over a 20 MHz bandwidth.

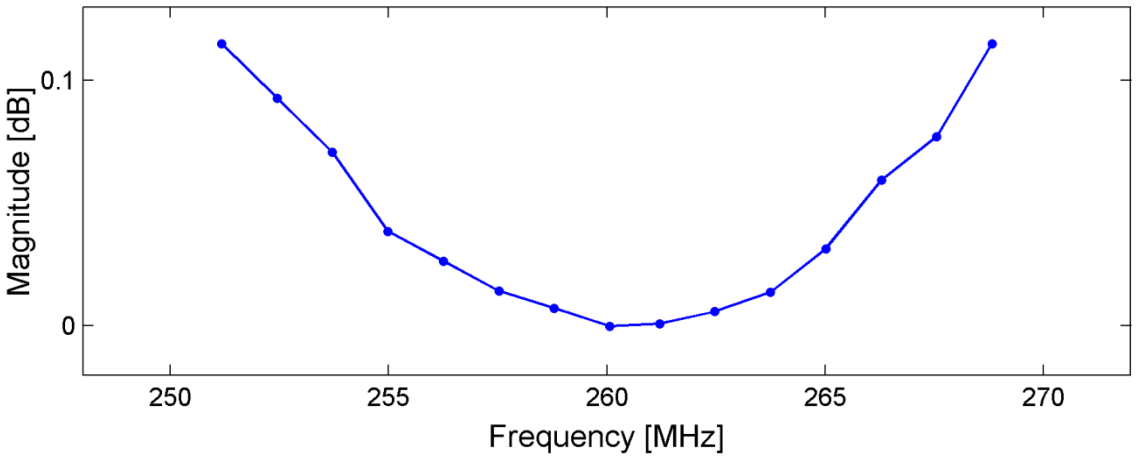


Figure 4.8 Measured in-band STF of the CTBPDSM

Figure 4.8 shows the measured in-band signal transfer function (STF) of the CTBPDSM. The slight peaking in the STF plot is due to the feed-forward path in the CTBPDSM. The maximum peaking is about 0.1 dB.

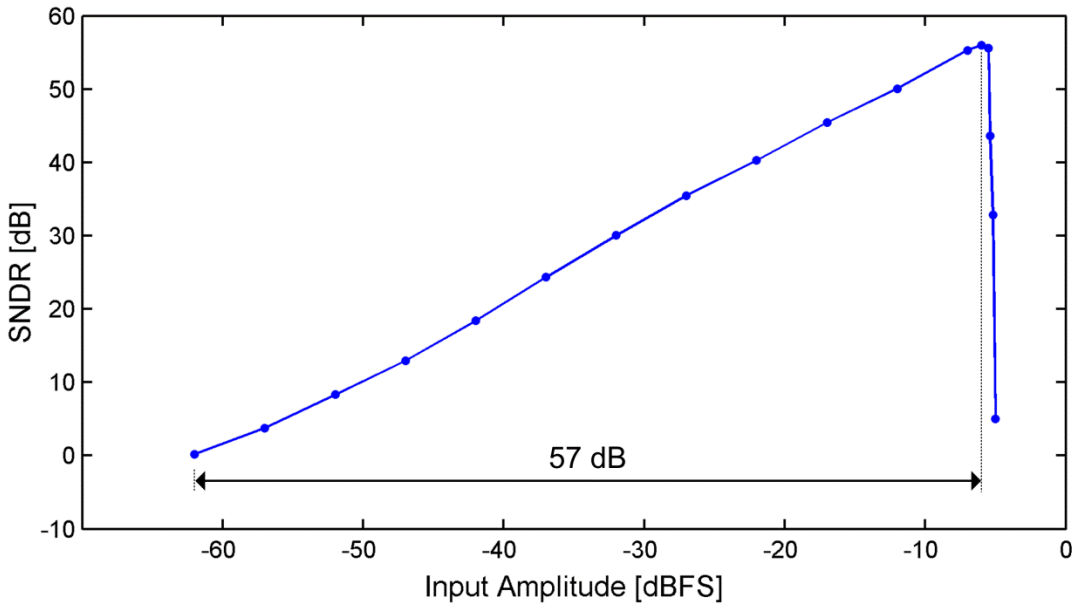


Figure 4.9 SNDR versus input amplitude

Figure 4.9 plots the measured SNDR versus input amplitude for a 260 MHz sinusoid. From the plot, the dynamic range of the CTBPDSM is 57 dB.

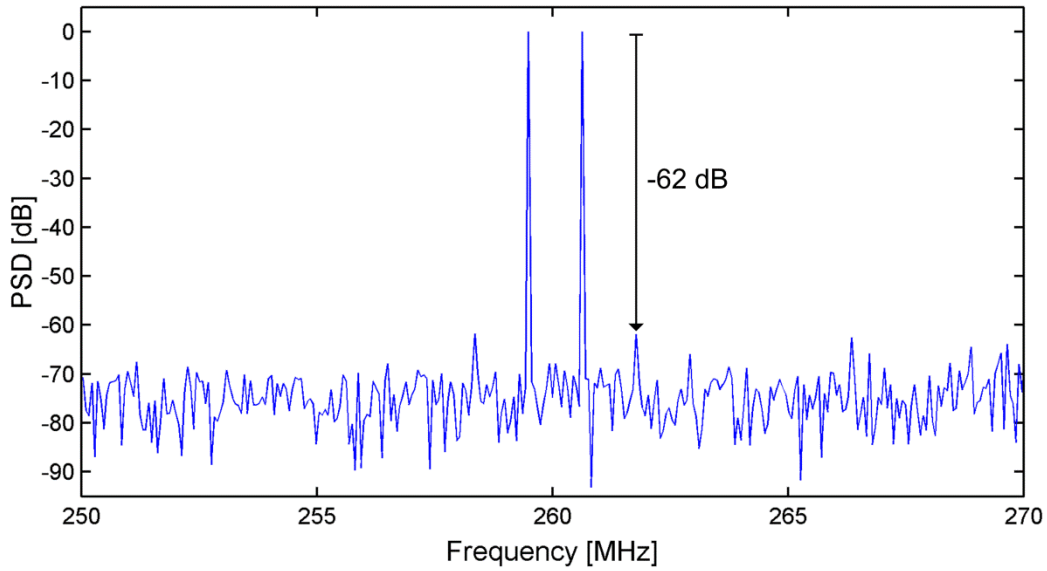


Figure 4.10 PSD with two tones 1.1 MHz apart

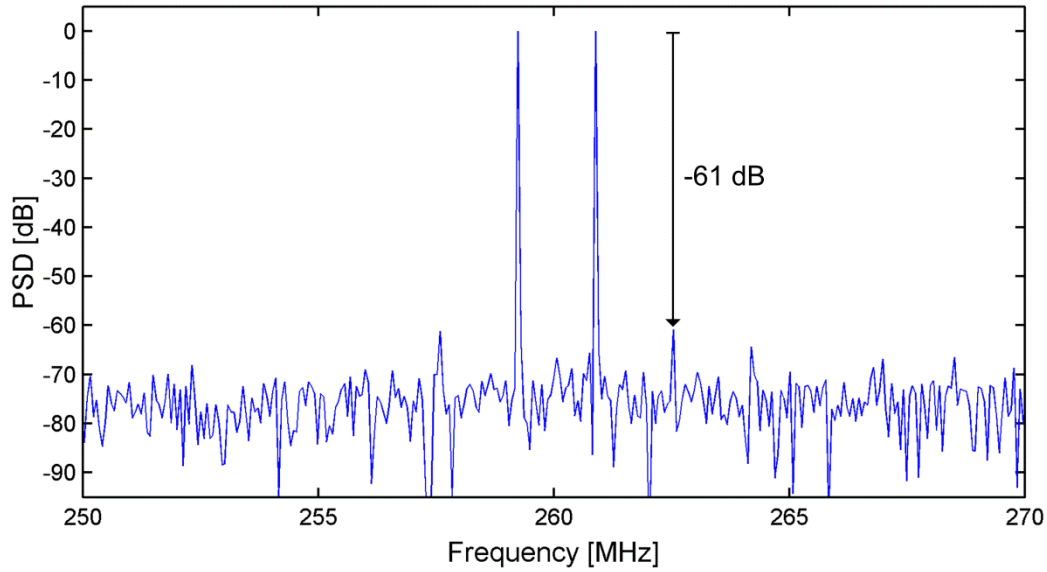


Figure 4.11 PSD with two tones 1.7 MHz apart

Two-tone test results are shown in Figure 4.10 and Figure 4.11. With two tones 1.1 MHz apart (Figure 4.10), the measured 3rd order intermodulation distortion (IMD_3) is -62 dB. With two tones 1.7 MHz apart (Figure 4.11), the measured IMD_3 is -61 dB.

To access the power efficiency of the CTBPDSM, a figure of merit for a band-pass modulator (FoM_{BP}), proposed in [35], is used. FoM_{BP} is defined as:

$$FoM_{BP} = \frac{Power}{2^{ENOB}\, 2BW(1+6\, f_{IF}/f_s)}. \tag{4.1}$$

The FoM_{BP} of the prototype II CTBPDSM is 0.25 pJ/conv. Figure 4.12 plots the FoM_{BP} versus area of the prototype II CTBPDSM as well as recently published CTBPDSMs fabricated in CMOS. The plot shows that the prototype II CTBPDSM has good power and area efficiency.

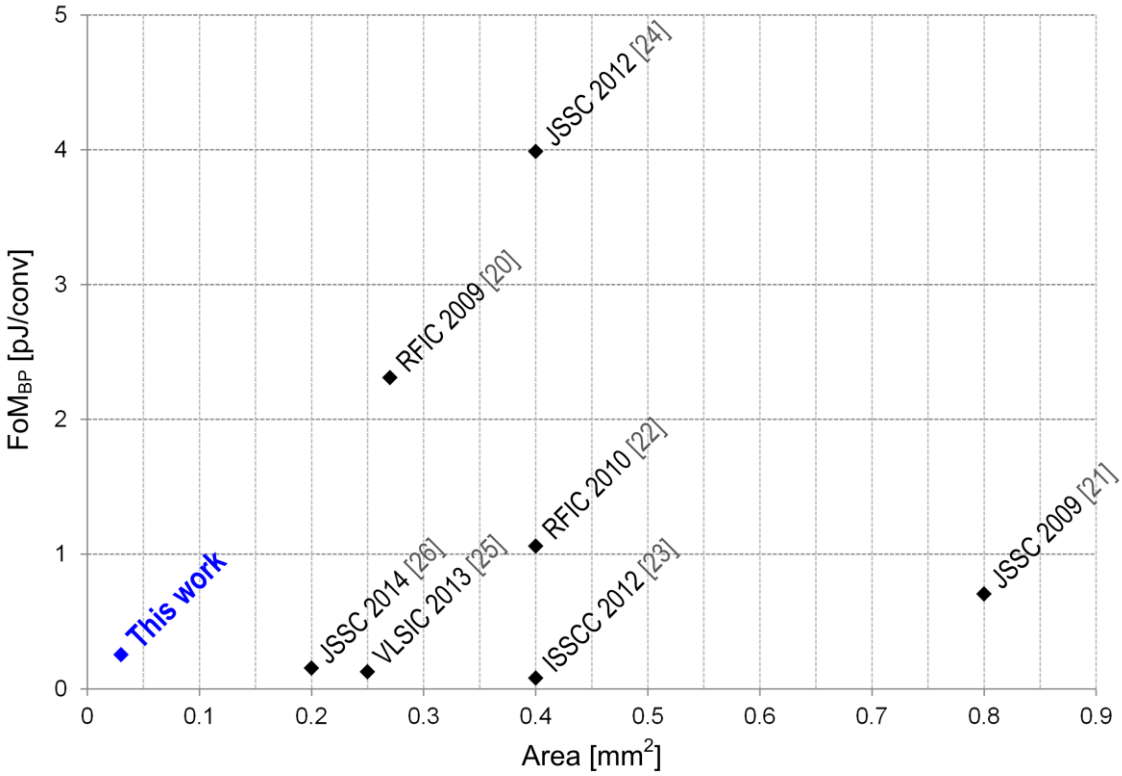


Figure 4.12 FoM_{BP} versus area of CTBPDSMs fabricated in CMOS

To measure beam patterns, eight 266 MHz poly-phase sinusoidal inputs are generated by eight synchronized DDSs to mimic the received signals from a uniformly spaced eight-element linear antenna array with λ/2 spacing. Eight CTBPDSMs digitize the eight 266 MHz signals at 1.04 GS/s, and the CTBPDSM digital outputs are fed to the

synthesized DBF core, which forms two simultaneous beams. As discussed in Chapter 1.4.2, a set of complex weights of $e^{j(k\theta)}$ adjusts the delay of the received and down-converted signal (x_k) at the k-th element to create a beam ($= \sum_{k=0}^{7} x_k e^{j(k\theta)}$) with one main lobe. When eight CTBPDSM digital outputs (having a measured SNDR of 54.4 dB on average) are constructively combined, the fundamental tone linearly increases by 18 dB while the channel noise is uncorrelated, resulting in an overall SNDR of 63.3 dB with an 8.9 dB improvement over a 10 MHz bandwidth as shown in Figure 4.13. This 8.9 dB SNDR improvement is very close to a theoretical limit of 9 dB.

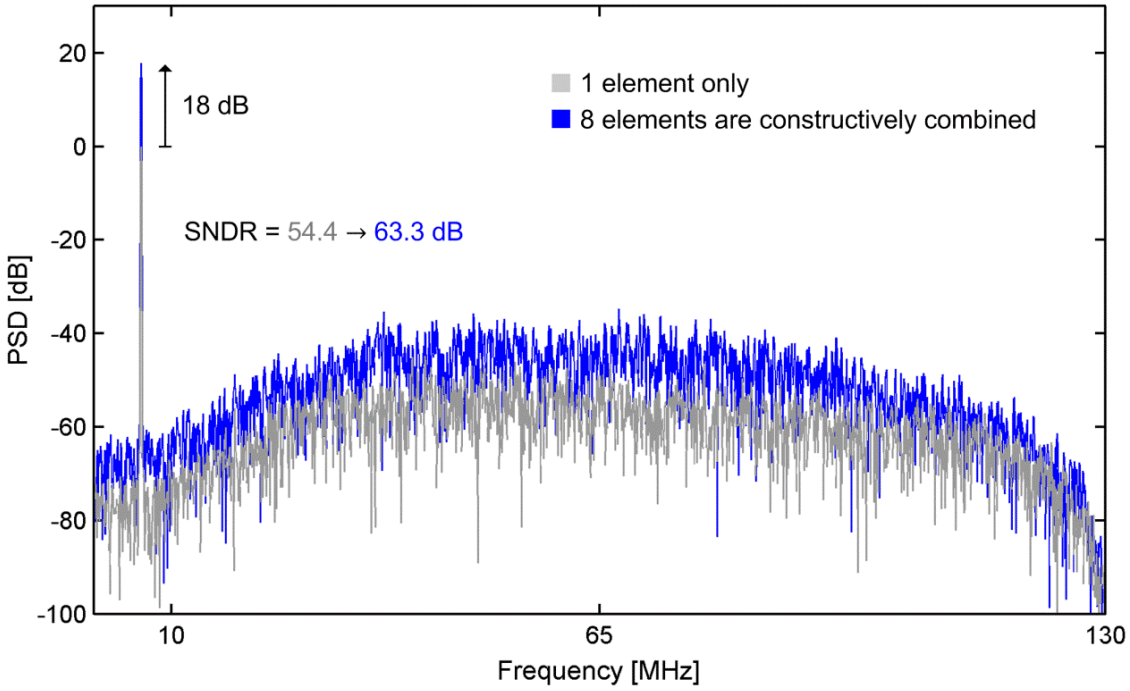


Figure 4.13 PSD of the beam with constructive combination (f_{in} = 266 MHz)

Figure 4.14 shows the measured single main-lobe beam patterns overlaid on ideal beam patterns for six different steering angles. The beam pattern is plotted for incidence angles from -90° to +90° and a measurement step size of 2.5°.

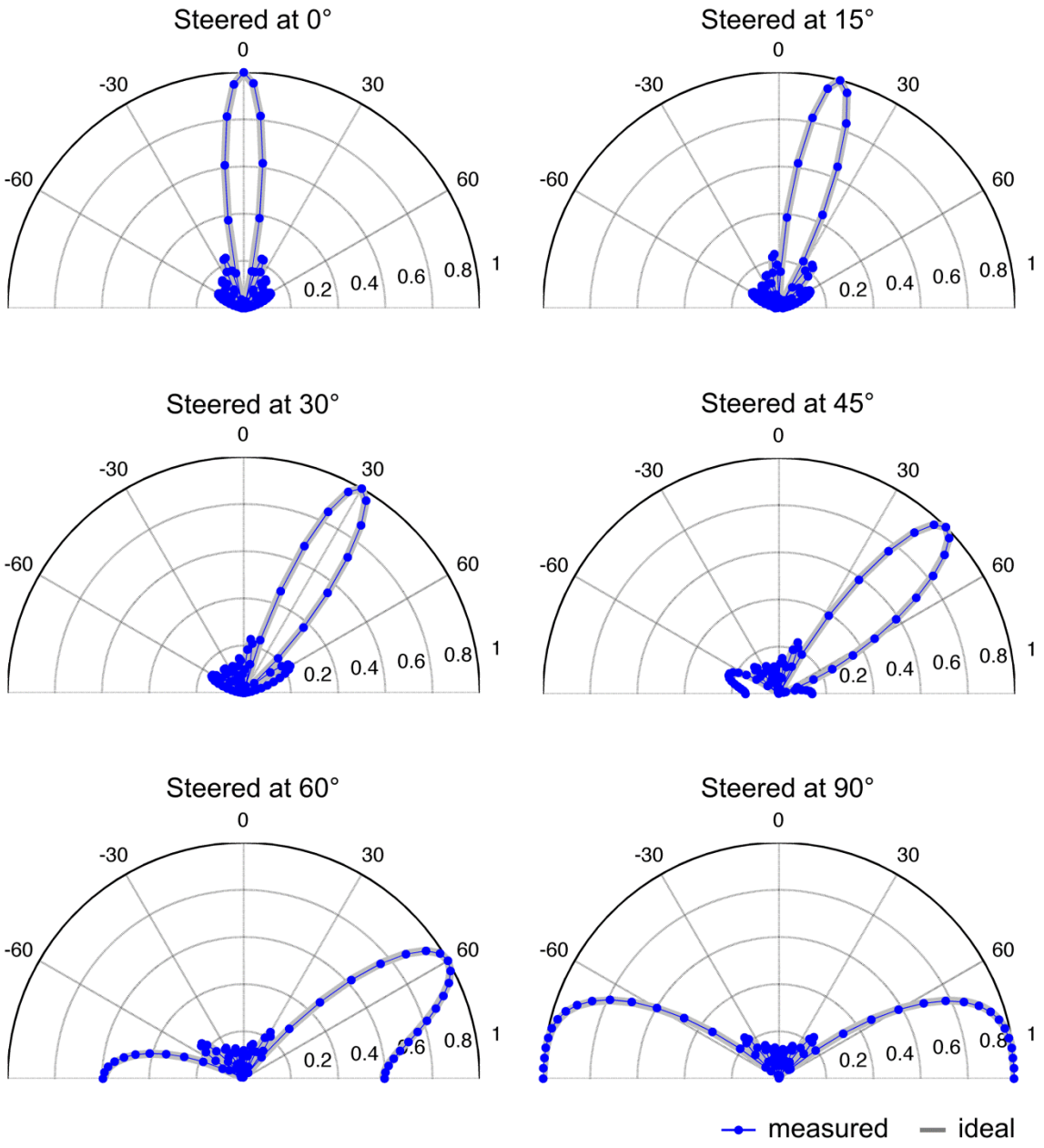


Figure 4.14 Ideal and measured beam patterns with one main lobe

Combining two single main-lobe responses creates a single beam with two main lobes ($= \sum_{k=0}^{7} x_k(e^{j(k\theta_1)} + e^{j(k\theta_2)})/2$) as shown in Figure 4.15. This can be easily done in the digital domain by using combined complex weights of $(e^{j(k\theta_1)} + e^{j(k\theta_2)})/2$ instead of $e^{j(k\theta)}$ at the cost of a 6 dB reduced array gain.

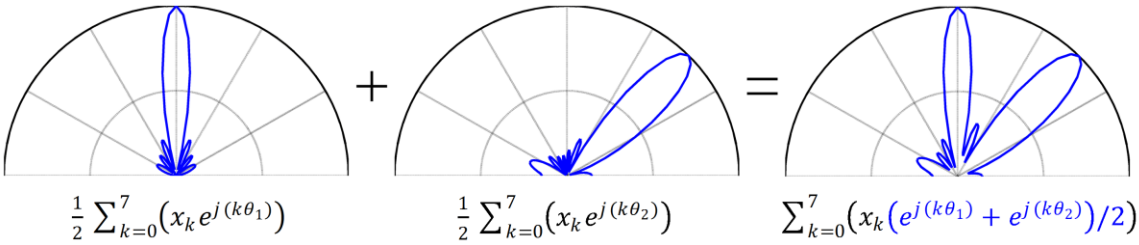


Figure 4.15 Creation of a single beam with two main lobes

The measured beam patterns with two main lobes are shown in Figure 4.16. The measured beam patterns show great consistency with the ideal patterns, which is difficult to achieve in analog beamforming.

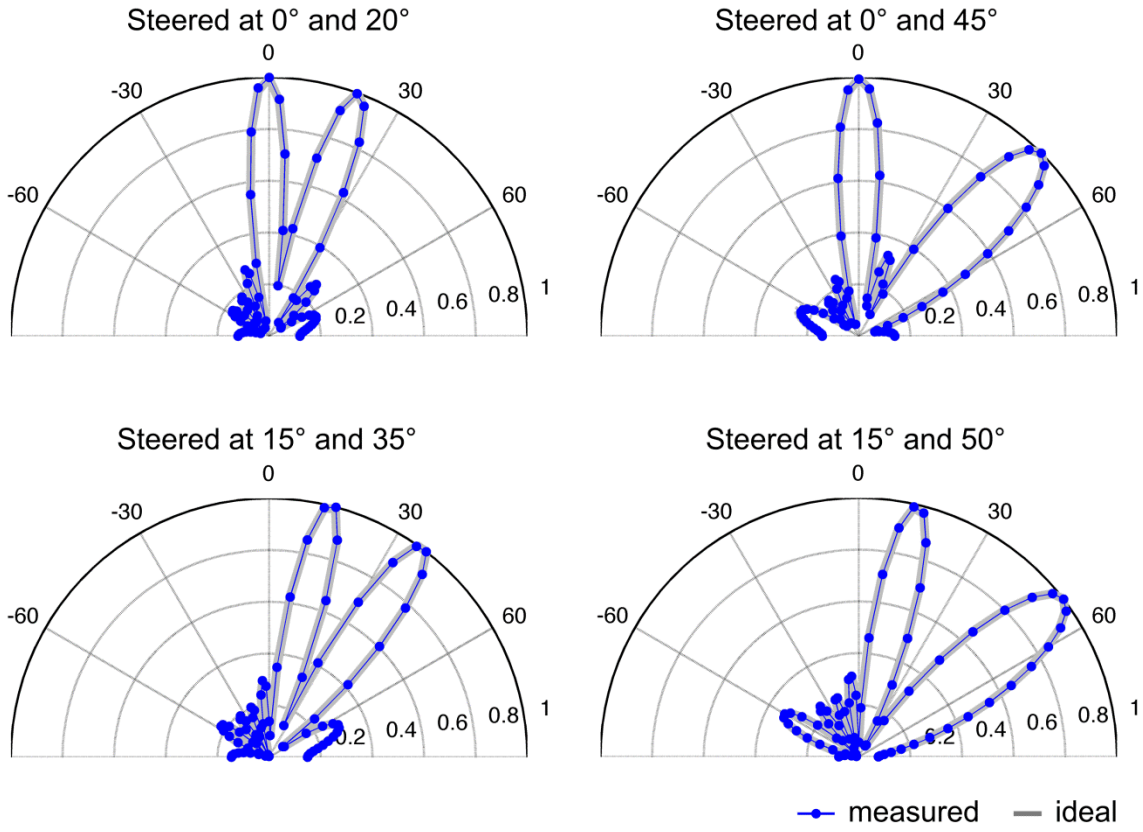


Figure 4.16 Ideal and measured beam patterns with two main lobes

The performance of the prototype II beamformer is summarized in Table 4.2.

Table 4.2 Performance summary of the prototype II beamformer

<table>
<tr><td colspan="2">Number of elements</td><td colspan="2">8</td></tr>
<tr><td colspan="2">Number of beams</td><td colspan="2">2</td></tr>
<tr><td colspan="2">Input IF [MHz]</td><td colspan="2">260</td></tr>
<tr><td colspan="2">IF bandwidth [MHz]</td><td colspan="2">20</td></tr>
<tr><td colspan="2">Sample rate [GS/s]</td><td colspan="2">1.04</td></tr>
<tr><td colspan="2">Overall array SNDR [dB]</td><td colspan="2">63.3</td></tr>
<tr><td colspan="2">SNDR improvement [dB]</td><td colspan="2">8.9</td></tr>
<tr><td colspan="2">Number of phase-shift steps</td><td colspan="2">240</td></tr>
<tr><td colspan="2">Technology</td><td colspan="2">65 nm CMOS</td></tr>
<tr><td rowspan="2">Power [mW]</td><td>CTBPDSMs</td><td>$13.1 \times 8 = 104.8$</td><td rowspan="2">123.7</td></tr>
<tr><td>DBF core</td><td>18.9</td></tr>
<tr><td rowspan="2">Core area [mm^2]</td><td>CTBPDSMs</td><td>$0.03 \times 8 = 0.24$</td><td rowspan="2">0.28</td></tr>
<tr><td>DBF core</td><td>0.04</td></tr>
</table>

CHAPTER 5 Future Work

With the unique combination of CTBPDSMs and BSP, a highly efficient implementation of IF-sampling DBF is achieved. The following improvements can be considered for more flexibility and better system performance:

- To support higher IF (or RF) inputs, the sample rate of the CTBPDSM can be increased. Increasing the sample rate also widens a bandwidth for the same SNR as far as quantization noise is concerned. However, the thermal noise density needs to be further reduced.
- To support multiple bands, a band-pass ADC with a wide tuning range of the center frequency can be considered.
- The main advantage of DBF is the ability to form multiple simultaneous beams from a shared frontend. The number of output beams can be relatively easily increased.
- Although CWM is used only for phase adjustment in the prototype beamformer, both amplitude and phase adjustments can be achieved by CWM. However, with CWM, the phase-shift resolution gets coarser as the amplitude decreases. To mitigate the degradation of the phase-shift resolution, the use of more basis vectors other than two I/Q vectors can be considered.
- Advanced DSP algorithms can be easily applied in DBF. Adaptive beamforming can be implemented together in the BSP digital beamformer.

CHAPTER 6 Conclusion

This thesis presents a new ADC-digital co-design approach for IF-sampling DBF with an array of CTBPDSMs and BSP. The unique combination of CTBPDSMs and BSP avoids high power consumption and large area, which have prevented the low-cost implementation of DBF. In the IF-sampling DBF architecture, un-decimated CTBPDSM outputs are directly processed for DDC and phase shifting. This enables to replace bulky digital multipliers for DDC and phase shifting with simple MUXs, reducing circuit complexity. In addition, the need for multiple decimators is removed by BSP. Two prototype beamformers are fabricated in 65 nm CMOS to demonstrate the efficiency of the IF-sampling BSP architecture. With an array of compact (0.03 mm^2) CTBPDSMs, and MUX-based DDC and phase shifting, the prototype I and II beamformers are smaller than a single CTBPDSM in [21−24]. The power consumption per unit element of the prototype II is only 6% of the FPGA implementation in [17]. Key contributions are summarized as follows:

- A new DBF receiver architecture with direct IF sampling is proposed.
- The DBF receiver architecture is efficiently implemented with a unique combination of CTBPDSMs and BSP. The main advantages of the combination of CTBPDSMs and BSP are listed as follows:
  - Bulky digital multipliers for DDC and phase shifting are replaced with MUXs.
  - The need for multiple decimators is removed (single decimation).

- A comparison of conventional DSP and BSP on implementing eight-element digital beamformer is provided.
- About an order of magnitude improvement of area efficiency is achieved in the prototype CTBPDSM.
- Two prototype beamformers with near ideal performance are presented. They are the first on-chip implementation of IF-sampling DBF. The prototype II is the first multi-beamforming DBF IC.

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