Low-temperature Electrodeposition of Crystalline Semiconductor Nano/Microstructures & Application of As-prepared Materials in Li-ion Batteries

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Chemistry)
In the University of Michigan
2017

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2017

DEDICATION

To my fiancée, parents, family and friends,

whose support and encouragement made this thesis possible.

Acknowledgements

I want to acknowledge my family, fiancée, teachers, friends and people who I got a chance to meet or know for making me who I am. I also like to thank my mentors, colleagues, all the staffs that helped me for making this thesis possible.

I cannot thank my family enough, especially my mom and dad, for teaching me how to think comprehensively, logically and creatively; be passionate, responsible and diligent about work, and be a good communicator. I want to thank my fiancée, Shuang for all the support and care in the past five years, all the joy you bring to my life, all the happy moments we spend together, and being smarter than me all the time. Thanks to my teachers and mentors, from kindergarten to undergrad, for all the knowledge and introducing me to science. I want to thank all my friends and roommates for the company during my years of adolescent for sharing all the fun, frustration and dirty secrets. I would also like to thank anyone who have inspired me at some point in my life for being great individuals whom other people can look up to.

In the past five years, I have been blessed to work with extremely talented and interesting colleagues. I want to thank Professor Maldonado for giving me the chance to be a scientist, and teaching me the skills that I will need for my future career. Thanks to everyone in the Maldonado group, for showing me how things work, helping with research and making this place like a family. I also want to thank professors and colleagues I have worked with for being open and collaborative, all the staff for being supportive and awesome at what they do. Finally, many thanks to people that I have hanged out with in the gym, on the pitch and at the bars for helping me be a graduate student that still has a life.

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ABSTRACT

Crystalline group IV semiconductor materials (i.e. Si and Ge) are essential components in many electronic and optoelectronic devices. Based on their alloying reactions with Li ion, Si and Ge are also potential rechargeable battery anode materials. In these and other applications, nanostructured forms of crystalline Group IV semiconductors particularly show enhanced and desirable properties, providing impetus for their development. The current synthetic methods for nano/microstructured group IV semiconductors usually demand high energy input, involve complicated instrumentation or require highly-refined precursors. The aim of this thesis is to develop non-energy-intensive synthetic methods, namely electrochemical liquid-liquid-solid (ec-LLS) processes, for the synthesis of nano/microstructured group IV semiconductor materials using simple instruments and common chemicals. Furthermore, this thesis also demonstrates that the ec-LLS grown materials can directly be used in energy storage devices and shows high performance. The essence of the ec-LLS process is the utilization of liquid metal (e.g. Ga (l), *e*GaIn (l), Hg (l)) electrodes for the electrodeposition of group IV semiconductors. The liquid metal serves as the cathode on which precursors are electrochemically reduced and the solvent phase for crystallization.

This dissertation summarizes results from several hypotheses that address the fundamental aspects and practical utility of ec-LLS for the preparation of crystalline Ge and Si. Chapter 2 examines the hypothesis that the size of the liquid metal electrode determines the diameter of ec-LLS grown Ge nanowires. The change in the morphology of Ge deposits when Ga reaches micrometer size is also shown. Chapter 3 focuses on the hypothesis that crystalline Si nanowires can be grown via ec-LLS process at low temperatures. The morphology and crystallinity of ec-LLS grown Si nanowires as a

function of substrate orientation, temperature and liquid metal identity is also discussed. Chapter 4 investigates the hypothesis that ec-LLS grown Ge microwires are electrochemically active to be used as Li-ion battery anode. The effect of Ga impurities on the performance of Ge anode is also discussed. Chapter 5 describes work illustrating that Si microwires can be prepared by ec-LLS with liquid metal electrodes showing high solubility for Si. Preliminary results are summarized that suggest further strategies to improve the prospects for this ec-LLS process. Overall, this dissertation will also serve as a foundation for future advancements in the ec-LLS preparation of other materials of interest.

CHAPTER 1

Introduction

A. Background

i. Properties and applications of group IV semiconductors

Semiconductors have conductivities in the range of 10^{-2} to 10^{9} ohm-cm, which is higher than that of insulators (10^{14} to 10^{22} ohm-cm), but lower than good conductors (~10^{-6} ohm-cm), such as metals.[1] The conductivity of semiconductors can be altered by introduction of impurities (i.e. doping) into the crystal structure, which lowers its resistance. The behavior of charge carriers (e.g. electrons, electron holes etc.) within semiconductors and at junctions, such as excitation by light and heat, and one-direction current flow forms the basis of photovoltaic and thermoelectric effects as well as amplification and switching functions.

In general, for electrons to flow in a solid, they must be in a partially filled band or have access to a nearby empty band. A band formed from n atoms contains 2n states. If each atom contributes one valence electron to the band, the band will be half full and the solid will possess the characteristic properties of a metal, which is electrons in the band changes their states with an applied electron field. If each atom contributes two valence electrons, the band will be exactly full if no other bands overlap in energy. All states in the band being full, an applied electric field cannot cause the electrons in the band to change their state, and therefore bands formed from the filled inner electronic shells of an atom do not normally lead to conductivity. For a solid to be an insulator, it is necessary for it to contain and even number of electrons per atom, and further it is necessary for the uppermost band containing electrons to be separated from other bands above by an energy gap >> kT (0.026 ev at room temperature) at the temperature of interest. Diamond is an insulator because it has four valence electrons and the relevant bands are separated by ~5 ev. Si and Ge have the same valence and crystal structure as diamond, but are semiconductors: the band separation here is of the order of 1 ev. The essential differences between insulators, semiconductors and metallic conductors may be attributed to differences in valency and the energy relationships of the various bands.[1]

Certain types of impurities and imperfections may affect drastically the electrical properties of a semiconductor. For example, the addition of phosphorous (P) to Si in the proportion of 1 P atom per 10^5 Si atoms increases the conductivity of pure Si by a factor of 10^6 at room temperature. Impurity atoms having additional and deficient valence electrons comparing to the host semiconductor crystal are n-type and p-type dopants respectively. For instance, Si and Ge crystallize in the diamond cubic structure with each atom forming four covalent bonds corresponding to the chemical valence four. If an impurity atom of five valence electrons, such as phosphorus (P), arsenic (As) or antimony (Sb), is substituted in the lattice in place of a normal atom, there will be one additional valence electron from the impurity atom. Therefore, an excess positive charge from the impurity atom which has lost one electron and an excess electron which is the carrier exist. On the other hand, the addition of trivalent impurities such as boron (B), aluminum (Al) or gallium (Ga) to Si or Ge creates deficiencies of valence electrons (i.e. 'holes'), which acts as the carrier.

Semiconductors materials with holes as the majority carriers are p-type, with electrons as the majority carriers are n-type. When p- and n- type materials are in contact with each other, a p-n junction forms. At the interface, some of the excess electrons from the n-type combine with 'holes' from the p-type. The resulting charge separation creates a depletion zone that impedes any further movement of electrons. An important property of p-n junctions is that they allow electron flow only from the n side to the p side when a forward bias is applied.

An important class of optoelectronic devices based on semiconductors is photovoltaics, such as solar cells. Light (photons) incident on the p-n junction gets absorbed by an electron, which is then excited to the conduction band. Once in the conduction band, the electron travels downhill to the n side of the junction, with a hole migrating to the p side. This creates a flow of current that is the reverse of what is seen in a forward biased p-n junction. The result is the conversion of light energy to electrical energy.

Group IV elements, such as Si and Ge form Li-rich binary alloys, so can be used to make high-capacity Li-ion battery electrodes.[2] The theoretical capacities of Si (4200 mAh g^{-1}) and Ge (1600 mAh g^{-1}) are significantly higher than commercial Li-ion battery anode graphite (372 mAh g^{-1}). The reaction of Li with Si and Ge to form Li_xM alloy operates at a chemical potential slightly higher than oxidation of Li, making it a suitable as the anode for Li-ion batteries. However, group

IV elements (i.e. Si, Ge, Sn, Pb) experience large volume expansion/contraction during the discharge/charge reactions.

ii. Practical Significance of Group IV Semiconductor Nanowires

Nanomaterials are defined as having at least one dimension between 1 and 100 nm. Advance in semiconductor industry have followed the Moore's Law, which states the number of transistors per unit area on integrated circuits doubles every year.[3] Moore's Law essentially requires the feature size of transistors to miniaturize to half its size every year, and the semiconductor industry entered the sub-100 nm regime in the early 2000s. Currently, 14 nm FinFET has been developed by Intel in 2014.[4] Semiconductor nanowires are attractive components for future nanoelectronics since they can exhibit a range of device functions. Nanowires can be used in the most basic component of integrated circuitry: the field-effect transistor (FET). Various nanowire materials and FET geometries have been utilized to take advantage of the small size (tens of nanometers), single crystallinity and potential low cost of semiconductor nanowires.[5] For example, FETs have been configured from nanowires by depositing the nanomaterial on an insulating substrate surface, making source and drain contacts to the nanowire ends, and then configuring either a bottom or top gate electrode, as shown in Figure 1.1a.[6] Shortening the active channel by chemically controlling the placement of contacts also provide an avenue for high density attainment.

Semiconductor photovoltaic devices can also benefit from nanowire geometries. Arrays of Si nanowires with radial p-n junctions could serve as an alternative to wafer-based Si geometries for solar energy conversion applications (Figure 1.1b). There are three potential benefits of Si nanowire-based solar cells. First, the high aspect-ratio nanowire array with conformal p-n junction on the nanowire surface decouples the absorption of light from charge transport by allowing lateral diffusion of minority carriers to the p-n junction (which is at most 50-500 nm away) rather than hundreds of microns away as in wafer-based Si solar cells. Secondly, the optical absorption of Si nanowire arrays is dramatically increased across the spectrum as compared to solid thin-film Si solar cells, owing to the sub-wavelength scale of the wires.[7] Finally, the use of chemical grown nanowire structures may yield solar cells with an improved cost benefit compared to wafer-based Si solar cells due to the lower materials consumption, yet potentially comparable efficiency to bulk crystalline Si solar cells.[8]

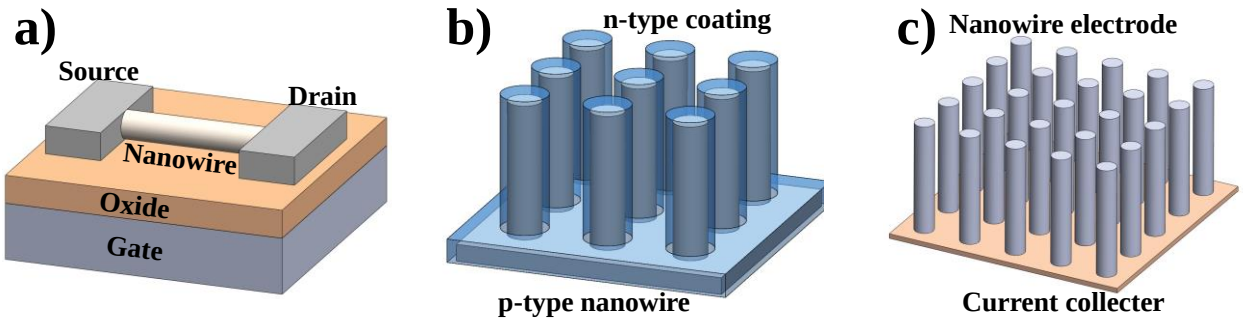

Figure 1.1. Schematic of a (a) field-effect transistor, (b) thin-film solar cell and (c) battery electrode using nanowires as a composition.

Group IV materials, especially Si and Ge possess high theoretical capacity as the anode material for Li-ion batteries, but are limited by 400% volume expansion upon insertion and extraction of lithium,[9] which results in pulverization and capacity fading. Nanowire structured Si and Ge electrodes (Figure 1.1c) offer superior properties than their bulk counterparts in the following three aspects. First, Si and Ge nanowires can accommodate large strain without pulverization by having reversible volume expansion/contraction and small grain size which prevents fracture formation. Second, the wires provide good electric contact with the current collector without addition of conductive additives since they can be grown directly on the conductive substrates. Third, the nanoscale diameter also provides short lithium diffusion distance which could increase the rate capability of nanowire battery electrodes.[10]

iii. Synthesis of Semiconductor Nanowires

The synthetic strategies for semiconductor nanowires can be categorized into 'bottom-up' and 'top-down' approaches. In the 'bottom-up' approach, a molecular species in the gaseous or liquid form is used as a precursor. The precursor molecules will then decompose under thermo-annealing or chemical reduction to form zero valent semiconductor atoms, which are the building blocks to form one-dimensional crystals with anisotropic catalysis (Figure 1.2). In 'top-down' processes, etching techniques are commonly used in conjunction with lithographic patterns on bulk semiconductors crystals to form array of vertical nanowires. A typical example of 'top-down' process is metal assisted chemical etching of Si to form Si nanowires (Figure 1.3). 'Top-down' approaches have advantages in terms of controllability and reliability. However, in order to develop next generation semiconductor nanowire devices, such as Si nanowire based devices, 'bottom-up' methods are superior for the following three important reasons. First, 'bottom-up' processes are more cost effective, since it starts with Si compounds which can be synthesized using sand (i.e. SiO_2) as the precursor, while 'top-down' approaches use single crystalline Si wafer, which is produce through an energy-intensive refining process. Second, 'bottom-up' methods are more versatile comparing to 'top-down' approaches, since the Si nanowires can be grown on a variety of substrates, which offers the possibility of direct device integration. Third, 'bottom-up' methods offer more variations for dopant control, such as dopant identity, concentration, gradient during different stages of nanowire growth which cannot be offered by 'top-down' processes. The

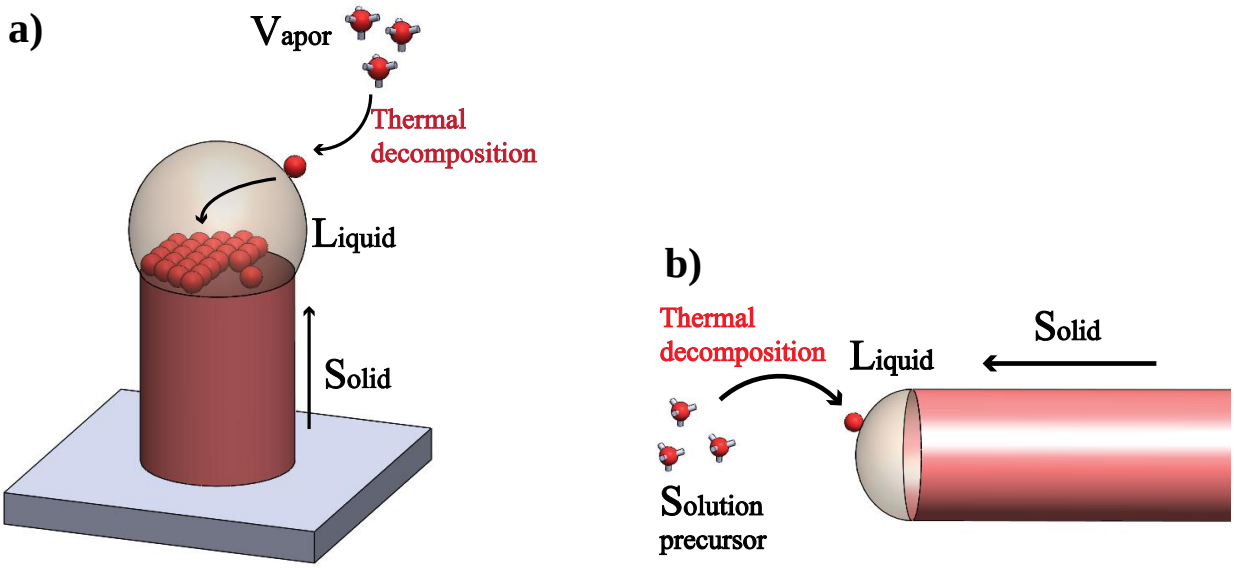

Figure 1.2. Schematic illustration of (a) vapor-liquid-solid process and (b) solution-liquid-solid process.

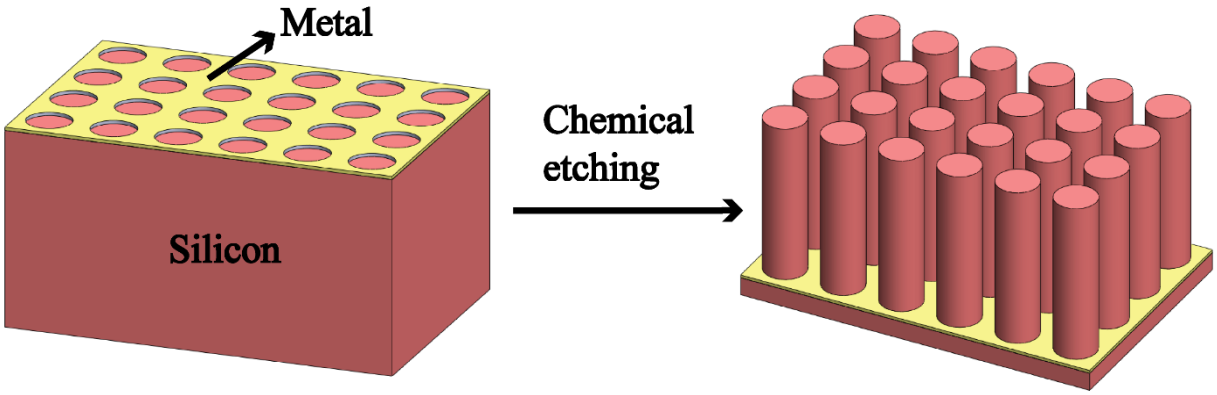

Figure 1.3. Schematic illustration of metal assisted chemical etching of Si.

variation in doping enables the direct fabrication of semiconductor nanowires of different carrier densities and p-n junctions.

Bottom up methods

There are generally two strategies to generate Si or Ge crystals with one-dimensional morphologies: metal-nanoparticle-mediated (MNM) methods and template-directed methods. The metal-nanoparticle-mediated methods use the liquid-solid interface to define the growth diameter of nanowires through a heterogeneous nucleation mechanism. Template assisted growth, on the other hand, uses a physical template with nanoscale channels to confine the nucleation and growth of semiconductor crystal.

Vapor-liquid-solid (VLS) and vapor-solid-solid (VSS) methods

The VLS crystal growth method is the most widely adopted approach to grow semiconductor nanowires. This process was originally developed by Wagner and co-workers serendipitously to produce micrometer-sized Si whiskers in 1960s[11]. VLS was then adopted by researchers in the nanoscience community to generate nanowires and nanorods from a rich variety of inorganic materials, including elemental semiconductors (e.g. Si, Ge),[12-14] III-V semiconductors (e.g. GaN, GaAs, InAs) [15-18] and II-VI semiconductors (e.g. ZnS, CdS, ZnSe).[19-22] A typical VLS process starts with the thermal decomposition of gaseous precursors. The growth species adsorbs on the surface of and subsequently dissolves into liquid nanodroplets of a catalyst metal, followed by nucleation of growth of crystalline wires. The one-dimensional growth is mainly induced and dictated by the liquid metal droplets, the sizes of which remain essentially unchanged during the entire process of wire growth. In this sense, each liquid droplet serves as a soft template to strictly limit the lateral growth of an individual wire. The steps involved in a VLS process are schematically illustrated in Figure 1.2a. Both physical methods (laser ablation, thermal evaporation, and arc discharge) and chemical methods (chemical vapor deposition (CVD)) have been employed to generate the vapor species required for the growth of nanowires.[23] By using Au nanoparticles as the catalyst for crystal growth, crystalline Ge and Si nanowires can be grown at around the eutectic temperature of Au-Ge and Au-Si, using silane, germane or their halogenated forms as the precursors.[14, 24]

In general, the growth temperature of VLS should exceed the eutectic temperature of catalyst-semiconductor element to keep the catalyst nanoparticles in a liquid phase. However, many experiments conducted below the eutectic temperature still afforded nanowires, and these

processes are called vapor-solid-solid (VSS). For example, VSS growth of Si nanowires was carried out using Cu, which is transformed into Cu_3Si once the reaction started, as the catalyst around 500 – 600 °C, 200 - 300 °C lower than the eutectic temperature of Si-Cu (802 °C). Real-time observations showed that wire growth involves rigid rotations of the catalyst particles and is by repeated ledge nucleation and flow at the Cu_3Si/Si interface.[25] The VSS process has been successfully applied to the growth of Si, Ge and GaAs nanowires. However, there is yet to be a generic mechanism for VSS processes comparing to VLS, and there are fewer cases in which nanowire growth is mediated by a metal catalyst in a solid phase. VSS offers an alternative method to grow semiconductor nanowires of which the eutectic temperature is very high, and has the potential to fabricate an abrupt junction when used on heterostructure nanowire growth.

Solution-liquid-solid (SLS), supercritical fluid-liquid-solid (SFLS) and supercritical fluid-solid-solid (SFSS) methods

As an analogy to the VLS process, SLS methods were developed to synthesis crystalline semiconductor nanowires in solution at relatively low temperatures (Figure 1.2b). In a typical procedure, metal nanocrystals (e.g. Au, Bi, Ga) were used as the catalyst which seeds the nucleation and a soft template to direct one-dimensional crystal growth. The growth species was generated through the decomposition of organometallic precursors on the surface nanocrystals. Using Ga nanoparticles in hexadecane solvent, crystalline Si nanowires were generated at as low as 200 °C.[26]

The use of a pressurized supercritical fluid can extend the solution-phase nanowire growth temperature up to ~650 °C, which allows for the use of metal nanocrystals with higher eutectic temperatures, and precursors that decomposes at higher temperatures to produce a wider range of semiconductor nanowires.[27] For example, bulk quantities of defect-free crystalline Si nanowires were produced using Au nanocrystals as the catalyst, diphenylsilane as the precursor in supercritical hexane at 500 °C and 270 bar.[28]

When various transition metal nanoparticles were employed to grow Si and Ge nanowires via SFSS, nanowires still grew even at a temperature more than 300 °C below the bulk metal-semiconductor eutectic temperature.[29-30] Ni nanocrystals were used for the synthesis of Si nanowires in supercritical toluene at a temperature range of 450-500 °C, and the eutectic temperature of Si-Ni is 816 °C. Ni nanocrystals induced Si crystallization through the solid-phase

alloying of Si in the Ni seeds and facilitated the growth of crystalline Si nanowires with minimum defects.

Template-directed synthesis

Template-directed synthesis represents a versatile route to fabricate 1D semiconductor nanostructures. The template serves as a scaffold within which a different material is generated in situ and shaped into a nanostructure with its morphology complementary to that of the template. A wealth of templates has been successfully demonstrated, such as channels within a porous material,[31-33] features on the surfaces of a solid substrate[34] and mesoscale structures self-assembled from block copolymers.[35-36] Template-directed synthesis provides a simple, high-throughput, and cost-effective procedure that also allows the topology present in a template to be duplicated in a single step.[23] Template directed synthesis can be coupled with VLS[32-33] or low temperature processes to produce semiconductor nanowires, such as electrodeposition.[31] There are two major drawbacks to this process. First, nanostructures synthesized using template-directed methods, especially low-temperature methods are often polycrystalline or amorphous as-prepared. Second, selective removal of the template using post-synthesis treatment (e.g. chemical etching or calcination) is necessary, complicating direct integration of as-prepared materials to device platforms.

In summary, existing bottom-up synthetic strategies for semiconductor nanowires requires at least 200 °C to produce crystalline materials and involves complicated instrumentations. Low-temperature methods, such as template-assisted electrodeposition only yields amorphous materials

Electrochemical Liquid-Liquid-Solid (ec-LLS) Process

As an electrochemical analog of the VLS and SLS process, electrochemical liquid-liquid-solid (ec-LLS) process was developed to produce crystalline semiconductors at low temperatures. To carry out this process, a low melting-point metal (e.g. Hg (l), Ga (l), *e*GaIn (l)) is used as the cathode for electrochemical reduction of precursors as well as the solvent for nucleation and crystal growth. After being reduced and adsorbed on the surface of liquid metals, the growth species will dissolve into the liquid metal, followed by nucleation and crystal growth after reaching supersaturation (Figure 1.4). Homogenous nucleation can take place within the liquid metal to form bulk semiconductor crystals when a macroscopic size liquid metal is used.[37-38] At the same time, nano/microstructured semiconductor crystals form through a heterogeneous nucleation

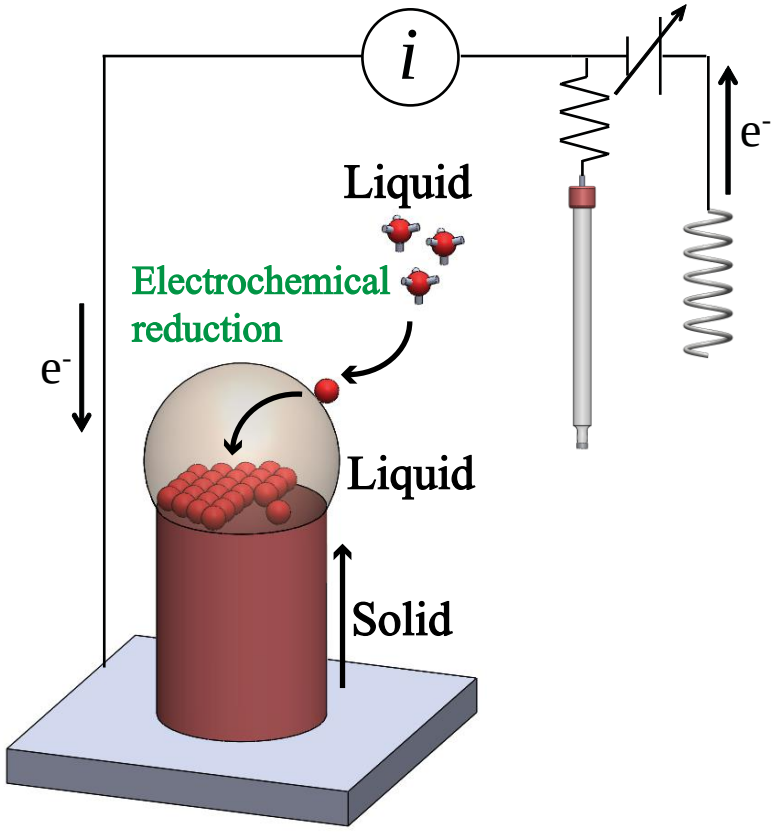

Figure 1.4. Schematic illustration of electrochemical liquid-liquid-solid process.

mechanism when nano/microdroplets of liquid metals are used.[39-40] Schematic illustrations of both processes are shown in Figure 1.5.

Ec-LLS extends the concept of metal-nanoparticle-mediated (MNM) methods to the solution based electrochemical system. Ec-LLS allows the crystal growth process to happen at lower temperatures comparing to VLS and SLS processes on two aspects. First, lower reaction temperatures are allowed when electrochemical reduction is used as the driving force to decompose the precursors instead of thermal decomposition. In both VLS and SLS processes, thermal decomposition of precursor molecules demands the process to be carried out at elevated temperatures (> 200 °C), even if certain noble metal nanocrystals catalyze the decomposition process.[41] Secondly, low melting-point liquid metals (e.g. Hg (T_m = -38.8 °C), Ga (T_m = 29.8 °C), *e*GaIn (T_m = 15.7 °C)) are used as the cathode in ec-LLS, which are molten (i.e. reaction state) when nanowire growth is carried out at near or below room temperatures. In VLS and SLS processes, noble metal (e.g. Au, Ag) nanocrystals are commonly used as the crystal growth catalyst, of which the eutectic temperature is > 360 °C. Most MNM methods require metal nanoparticles to be molten to achieve crystalline nanowire growth at decent yield, thus ec-LLS can be carried out at much lower temperature since the catalyst being used are molten at near room temperatures. There are exceptions in MNM methods where semiconductor nanowires growth are catalyzed by solid metal nanocrystals (i.e. VSS, SFLSS), and SLS process has also started to adopt low melting-point metal catalysts (e.g. Ga, Bi (T_m = 271.5 °C), Sn (T_m = 271.5 °C)), but up to now all ec-LLS covalent semiconductor nanowire growths are carried out at temperatures > 100 °C lower than the lowest-temperature SLS processes.[26, 42]

In the previous reports on Si electrodeposition on solid substrates, only amorphous deposits were obtained from low-temperature (<100 °C) electrodeposition experiments. Recently, we have seen Si crystal being produced *via* ec-LLS process at low temperatures.[38] The uniqueness of the ec-LLS process is that a Ga liquid metal electrode instead of a conventional solid electrode is used for the crystal growth process. Similar to VLS and liquid-phase-epitaxy (LPE) processes, in which a liquid mediate phase is used to facilitate the crystal growth, we believe that the liquid metal Ga in our system enable Si crystal growth at this low operation temperature. The liquid metal Ga serves as a sink for dissolution of crystal growth species (i.e. Si) which is reduced on Ga surface. Limited solubility of Si in Ga at this low temperature allows Si to reach supersaturation rapidly.[43] Si will begin to nucleate as a result of supersaturation, and liquid metal phase will give the Si little

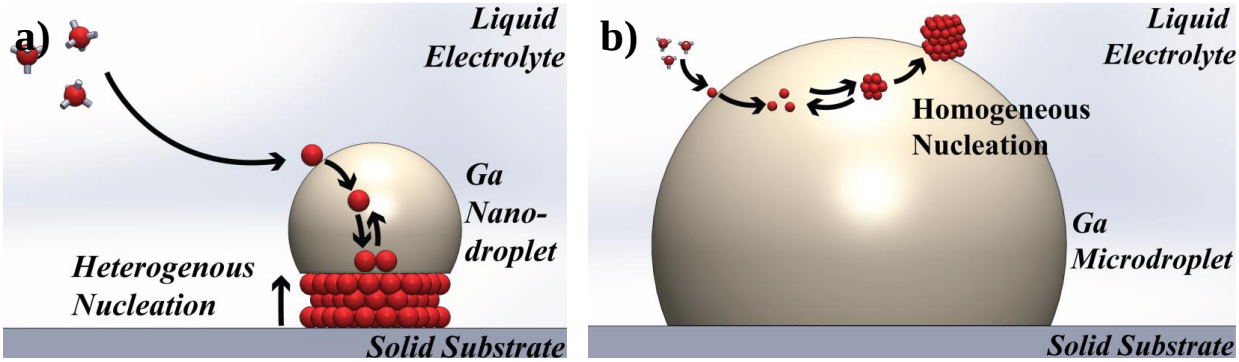

Figure 1.5. Schematic illustration of (a) heterogeneous nucleation and (c) homogenous nucleation.

dwelling time which enables Si atoms to find the right position to develop a crystal lattice. If a solid electrode is used, reduced Si will deposit on the substrate directly. Because there is no liquid mediate phase to create crystal growth condition, only amorphous deposits can be obtained.

B. Content Description

Chapter 2 discusses ec-LLS deposition of crystalline Ge nanowires as a function of Ga nanodroplet size. Direct preparation of crystalline Ge nanowires from dissolved aqueous solutions of GeO_2 *via* electrodeposition through an ec-LLS process using a variety of Ga nano/microdroplets has been demonstrated. A templated silica film featuring regularly spaced opening with defined sizes was prepared on n^+-Si substrates by a modified natural lithography patterning process. These platforms were used to electrodeposit Ga droplet arrays with defined sizes and pitch. The Ga nano/microdroplets subsequently facilitated Ge nanowire ec-LLS in water as a function of droplet size. The amperometric responses recorded during ec-LLS indicated an apparent size-dependence on the measured current-time transients. However, none of the recorded current-time profiles fit either Cottrell-type or standard nucleation models. Similarly, electron micrographs of the as-produced Ge nanowires showed a strong correlation between the base size of the Ge nanowires and the Ga droplet diameter. All nanowires featured a consistent taper, with a cone angle of approximately 10°. For the largest Ga droplets, no nanowires were observed under the employed ec-LLS conditions. Instead, a large isotropic Ge deposit covered with small Ge nanowires was observed. These cumulative results provide the first probe of the effects that liquid metal size(volume) have on electrodeposition by ec-LLS. Chapter 2 is reproduced with permission from *J. Electrochem. Soc*., **161**, D3044 (2014). (Copyright 2014, The Electrochemical Society)

Chapter 3 elaborates on the direct electrochemical deposition of crystalline Si nanowires at $T \geq 60$ °C. Direct synthesis of crystalline Si nanowires at low temperatures has been achieved through an ec-LLS process. Liquid metal nanodroplets containing Ga were used as both discrete ultramicroelectrodes and crystal growth seeds for Si nanowires. This new ec-LLS process was performed in propylene carbonate containing $SiCl_4$ at temperatures as low as 60 °C. X-ray diffraction and Raman spectra separately and independently indicated the nanowires were crystalline as prepared. Scanning electron micrographs of Si nanowires grown on both Si(111) and Si(100) substrates further showed that the direction of nanowire growth specifically followed the crystallographic orientation of the underlying substrate, indicating deposition with homoepitaxy.

Localized electron diffraction patterns collected from individual Si nanowires in a transmission electron microscope showed the characteristic pattern of the diamond cubic structure of crystalline Si. Additional experiments were performed that indicated the wetting of the electrodeposited Si by the liquid metal influenced the morphology of the resultant nanowire. These cumulative results support the overarching premise that ec-LLS is a unique synthetic method for crystalline Si nanowires at low temperatures. Chapter 3 is reproduced with permission from *RSC Adv.*, **6**, 78818 (2016). (Copyright 2016, Royal Society of Chemistry)

Chapter 4 details the process to fabricate high-performance polycrystalline Ge microwire film anodes for Li-ion batteries. A high-performance Li ion battery anode has been made using Ge microwire films with up to 10 at.% Ga content. These materials were prepared by the electrochemical liquid-liquid-solid (ec-LLS) process with *e*GaIn alloy droplets at T = 80 °C. The Ge microwires were studied as prepared and also after an annealing-etching sequence intended to lower Ga content. The as-prepared Ge microwires yielded an initial discharge capacity of 1350 mA h g^{-1} and retained more than 80% of their original capacity after 80 cycles when subject to discharge-charge cycles at 0.1 C. The treated Ge microwires still showed unusually large capacities and decent capacity retention, albeit less than the as-prepared materials. The cumulative data point to the premises that not only is ec-LLS amenable to making active Li^+ battery anodes, but it yields unique materials that suggest that Ga incorporation is beneficial to countering the material stress/fracturing incurred during Li^+ insertion. Chapter 4 is reproduced with permission from *ACS Energy Lett.*, **2**, 238 (2017). (Copyright 2017, The American Chemical Society)

Chapter 5 tests the efficacy of Si microwire growth via ec-LLS. Crystalline Si microwires were grown *via* ec-LLS galvanostatically at 140 °C. Temperature dependence studies of Si microwire ec-LLS were performed between 100 – 140 °C. *e*GaIn liquid metal electrode did not reduce Ga incorporation into Si microwires. Si microwires of higher crystallinity were not observed when EGaAg were used as the liquid metal electrode.

Chapter 6 presents data on three different unfinished projects. The first project aims at determining the metal-loading mechanism of ec-LLS process. Energy dispersive X-ray spectroscopy (EDS) and atom probe tomography (APT) were used to quantitatively determine impurity content in ec-LLS grown crystals. Dopant density in ec-LLS grown crystals were also derived from conductivity measurements. Second, electrochemical liquid-phase-epitaxy (ec-LPE) growth of Si thin film is demonstrated. Cyclic voltammetry and chronoamperometry were carried

out to study electrochemical reduction of $SiCl_4$ on Ga liquid thin films. Scanning electron microscopy (SEM) and powder X-ray diffraction (PXRD) were used to characterize the morphology and crystallinity of ec-LPE grown Si thin films. Third, a Si/Ge heterostructure is grown via ec-LLS and used as anode for Li-ion batteries. Galvanostatic charge-discharge measurement were carried out on the Si/Ge electrode in a half cell.

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CHAPTER 2

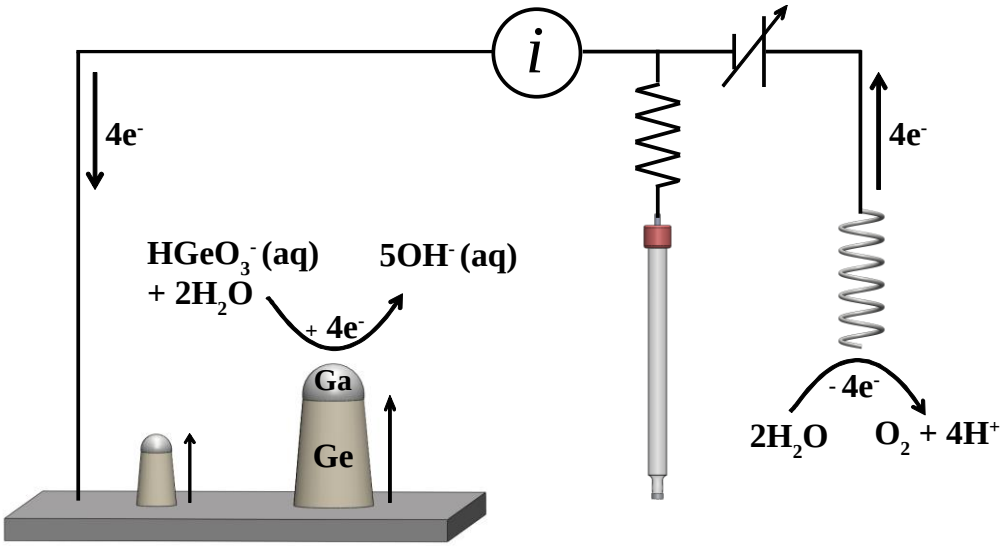
Electrochemical Liquid-Liquid-Solid Deposition of Crystalline Ge Nanowires as a Function of Ga Nanodroplets Size

A. Introduction

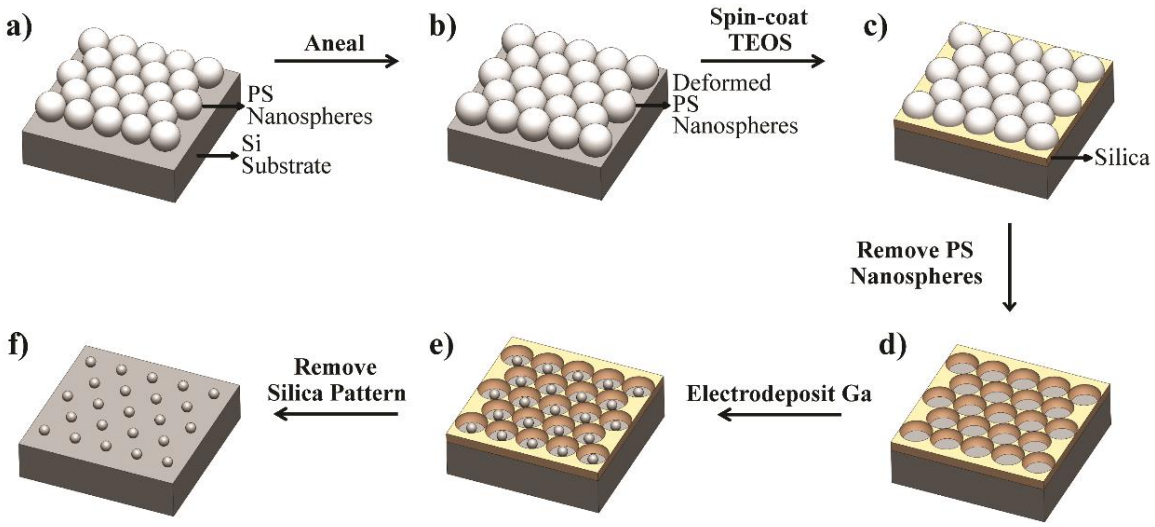
The ability to grow semiconductor nanostructures of desired sizes is key to making as-prepared materials suitable for device applications. Since Ge nanowires were grown from Ga nanodroplets of one uniform size via ec-LLS,[1] we started to explore the possibility of growing Ge nanowires of different sizes by using different size Ga nanodroplets. On the other hand, the morphology change of Ge nanowires grown from Ga droplets of different sizes can help us understand different ec-LLS nucleation modes.

In this chapter, we examine the hypothesis that the size of the nanodroplet affects the Ge nanowire ec-LLS process (Scheme 2.1), the observable electrochemical responses, and the resultant materials' morphological properties. We first show results for a modified natural lithography process with polystyrene spheres and solution cast silica for the preparation of Ga nanodroplet films on a flat conductive support (Scheme 2.2). We present results from experiments performed with n^+-Si(100) as the support substrates. In addition to being mostly inert towards H_2 evolution in water, these Si substrates can support crystalline Ge nanowire ec-LLS with heteroepitaxy.[1] Accordingly, results are presented where Ga nanodroplets films are used to conduct ec-LLS on n^+-Si(100) so as to produce individual crystalline Ge nanowires. The voltammetric and current-time transients are reported, as well as evidence indicating factors that impact epitaxy and deposition rates. Further data are presented that show the morphology of electrodeposited Ge follows the size of the Ga nanodroplets and that indicate pertinent aspects of the ec-LLS process.

B. Methods



Scheme 2.1. Schematic depiction of Ge nanowire ec-LLS process in water under potentiostatic control.



Scheme 2.2. Schematic depiction of preparation of Ga droplet arrays through natural lithography and Ga electrodeposition. (a) Deposition of hexagonally close-packed monolayer of polystyrene (PS) microspheres. (b) Annealing step to increase contact area between microspheres and substrate. (c) Spin-coating spin-on-glass solution to backfill void space. (d) Removal of PS microspheres resulting in patterned silica (SiO_x) film. (e) Electrodeposition of Ga nanodroplets within the silica pattern. (f) Removal of silica pattern through HF(aq) etch.

Materials and Chemicals. Acetone (Certified ACS, Fisher), ethanol (Certified ACS, Fisher), sodium dodecyl sulfate (99%, Acros Organics), tetraethyl orthosilicate (99+%, Aldrich), HCl (36.5 – 38 wt % in H_2O, Fisher), HF (49 wt % in H_2O, Transene Inc.), $Ga(NO_3)_3$ (99.9%, Aldrich), NaCl (99+%, Aldrich), GeO_2 (99.999%, Acros Organics), and $Na_2B_4O_7{\cdot}10H_2O$ (Analytical Reagent, Mallinckrodt) were used as received. Water with a resistivity > 18.2 MΩ·cm (Barnsted Nanopure) was used throughout. Single crystalline n^+-type Si(100) wafers (As-doped, $R < 0.007$ ohm·cm, 0.625 ± 0.020 mm thick) were obtained from Crysteco. Si wafers were cut into ~0.5 cm^2 squares, cleaned by immersing in a 3:1 (v/v) solution of 98% H_2SO_4 (Fisher) and 30% H_2O_2 (aq) (v/v, Fisher) for 1 hour, and stored submerged in water prior to use. Polystyrene micro/nanospheres (Polybead® Microspheres) with diameters of 0.75 μm, 2 μm and 10 μm were purchased as 2.5% solids (w/v) aqueous suspensions from Polysciences, Inc. A 100 × 15 mm plastic petri dish was used for monolayer film formation. The aqueous suspensions of polystyrene microspheres were centrifuged and collected apart from solvent, washed with ethanol to remove surfactant, and then re-suspended in a 1:1 (v/v) mixture of ethanol and an aqueous solution of 0.2 mM sodium dodecyl sulfate (SDS).

Formation of Close-Packed Monolayer of Micro/Nanospheres For close-packed films of small (diameter < 2 μm) polystyrene spheres, an interface self-assembly process[2] was used. Briefly, each Si substrate was placed on the bottom of a petri dish filled with an aqueous 0.2 mM SDS. A 3 μL drop of the polystyrene sphere suspension was then added to the top of the solution by first casting the suspension drop onto the bottom of a hydrophilic glass slide that was immersed at 45° (with respect to the plane of the petri dish) and then allowing the drop to slide down on to the petri dish solution. Upon reaching the glass slide/solution interface, the polystyrene spheres dispersed on the top of the solution and formed a colored film. Additional drops of polystyrene nanosphere suspensions were added in this way until the entire top of the solution was coated with sphere. The solution was then emptied out of the petri dish from the bottom without disturbing the Si substrate via a syringe. As the solution level decreased, the film of polystyrene spheres descended upon and coated the top of the Si substrate.

For close-packed films of large (diameter = 10 μm) polystyrene spheres, a spin-coating method[3] was used. A 2 μL drop of the polystyrene microsphere suspension was cast onto the front side of 5a Si substrate mounted in a spin coater (6800 Spin Coater Series, SCS). The substrate was spun nominally at 120 rpm for 2 minutes but the speed and duration were tuned slightly (by 5%)

to obtain uniform monolayer coverage on the substrate. Higher spin speeds resulted in more void areas within the film while lower spin speeds facilitated multilayer stacking.

The close-packed micro/nanosphere monolayer films were then annealed at 125 °C in air in a muffle furnace (Thermolyne Benchtop Muffle Furnace, 120 V, Thermo Scientific) to adhere the micro/nanospheres to the substrate and to increase the contact area between each micro/nanosphere and the Si substrate. The Si substrate was then etched with 5% HF(aq) to remove any native oxide without mechanical change to the polystyrene film. The coated Si substrate was then re-mounted onto the spin-coater and covered with a 'spin-on-glass' solution consisting of 0.2 M TEOS, 0.05 M HCl in water/ethanol 1:1 (v/v) solvent. The TEOS-covered Si substrate was spun at 650 rpm for 2 min to ensure complete infiltration of TEOS into the void spaces between the close-packed spheres and to allow for condensation formation of silica (SiO_x). The polystyrene film was then removed by immersion of the substrate in a vessel containing neat acetone inside a sonicator (Ultrasonic Cleaner Model 2510, Branson) 3 times for 5 min each. The resultant film constituted of periodic silica openings with defined openings at the bottom that exposed the bare underlying Si substrate. The area of these openings was defined both by the initial annealing step and the original size of the polystyrene micro/nanosphere.

Preparation of Ga Nanodroplet films The openings in patterned silica films were used to electrodeposit uniform Ga nanodroplets onto the Si substrate. The backside of the Si substrates was first scratched with a diamond tip scribe, etched locally with 5% HF(aq), rinsed clean, and then rubbed with Ga-In eutectic to make Ohmic contact. The Si substrates were then placed on a 1 × 2.5 × 0.2 cm stainless steel support. A Teflon cell featuring a 0.2 cm outer-diameter Viton O-ring was then press-fit on top of the Si substrates, exposing a surface area of ~0.1 cm^2. The cell was then filled with a buffered (pH = 2.5, adjusted by HCl) aqueous solution of either 0.01, 0.1 or 0.2 M $Ga(NO_3)_3$. All Ga and Ge electrodepositions were performed with a CH Instruments 760C potentiostat. A three-electrode configuration with a Pt mesh counter electrode and a Ag/AgCl (sat. KCl) reference electrode was employed. A current of 1.0 mA was applied for 3-90 s to reduce Ga into the openings in the silica film. Before use in ec-LLS, the silica pattern was then etched away using a brief immersion in 1% HF(aq) for 5-15 s.

ec-LLS of Ge Nanowires Ge ec-LLS was performed with the Ga nanodroplet films using an aqueous electrolyte containing 0.01 M $Na_2B_4O_7$ and dissolved GeO_2 at a formal concentration

of 0.1 M. A constant applied potential of -1.6 V vs Ag/AgCl was applied for 1 - 9 hr at room temperature.

Material Characterization Scanning electron microscopy was performed with a Philips XL30 FEG SEM operated at 15 kV with a secondary electron detector. Energy dispersive spectroscopy (EDS) was performed at 20 kV with an EDAX UTW detector. Particle size and nanowire orientation distributions were analyzed based on the SEM images using Adobe Photoshop CS3 and ImageJ (Version 1.45s). High resolution transmission electron microscopy (HRTEM) was conducted with a JEOL 2010F analytical electron microscope equipped with a zirconated tungsten (100) thermal field emission source at 200 kV acceleration voltages. Powder X-ray diffraction patterns were collected with a Bruker D8 Advance diffractometer equipped with a Cu Kα source, 0.6 mm incident beam slit and a Lynx Eye detector.

C. Results

Figure 2.1a shows a representative Si substrate coated by a close-packed monolayer of polystyrene microspheres with mean diameters ($\overline{d}$) of 2 μm. A representative electron micrograph of the packing of the individual microspheres is shown in Figure 2.1b. By the methods described here, domain sizes for highly ordered, close-packed monolayers of micro/nanospheres of 40 μm^2 were routinely observed, with little to no void space in between each ordered 2D domain. As prepared, the polystyrene spheres had minimal direct contact with the underlying Si substrate (Figure 2.1c). Upon annealing just above the glass transition temperature of polystyrene, the shape of the microspheres distorted slightly, significantly increasing the contact area with the underlying Si substrate (Figure 2.1d). Upon infiltrating the polystyrene microsphere monolayer with a 'spin-on-glass' solution, curing the infiltrated solution, and then removing the polystyrene microspheres, a one-layer-thick 'inverse opal' silica film coated the Si substrates (Figure 2.2). The salient feature for this work is the underlying Si substrate was only exposed at the bottom of the opal, with an opening size defined by the contact area of the annealed polystyrene microspheres. Through judicious selections of the original nano/microsphere size and annealing time, the diameters and pitches of the exposed openings could be tuned by over an order of magnitude.

The patterns as shown in Figure 2.2 were then filled with individual nanodroplets of liquid Ga by electrodeposition. The initial deposits within the templated film openings were particulate and several small Ga particles could be seen in each opening. Various methods were attempted to

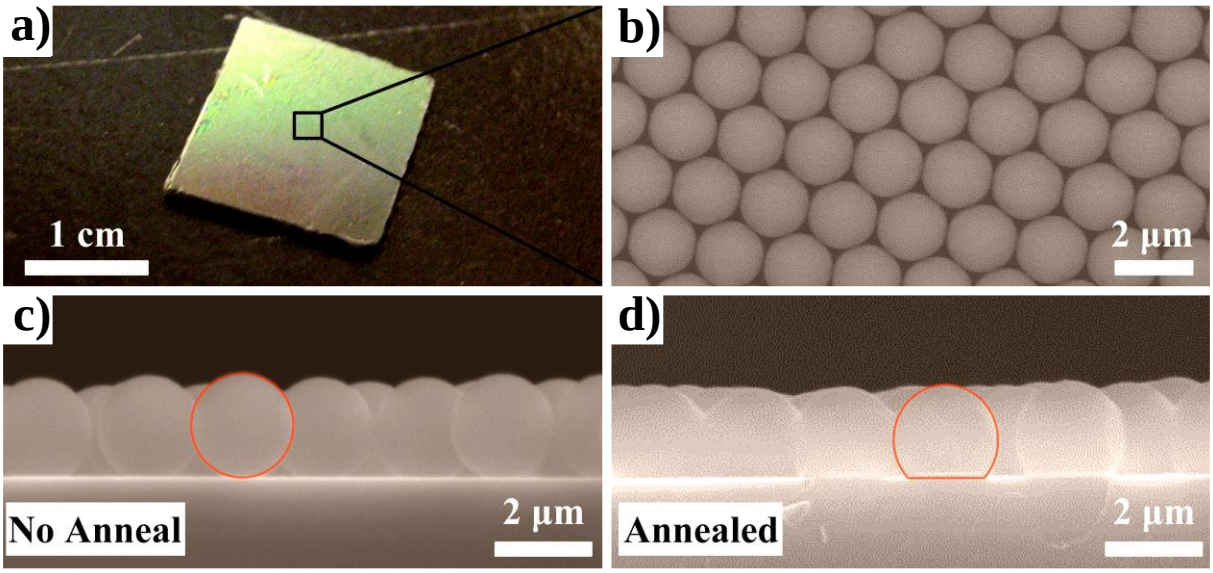


Figure 2.1. (a) Optical image of a 1 cm^2 n^+-Si substrate coated with polystyrene microsphere monolayer. (b) A top-down view scanning electron micrograph of hexagonally closed-packed monolayer. Cross-sectional electron micrographs of Si substrate decorated with PS nanospheres (c) before and (d) after annealing process. Red circle highlight microsphere shape before and after anneal.

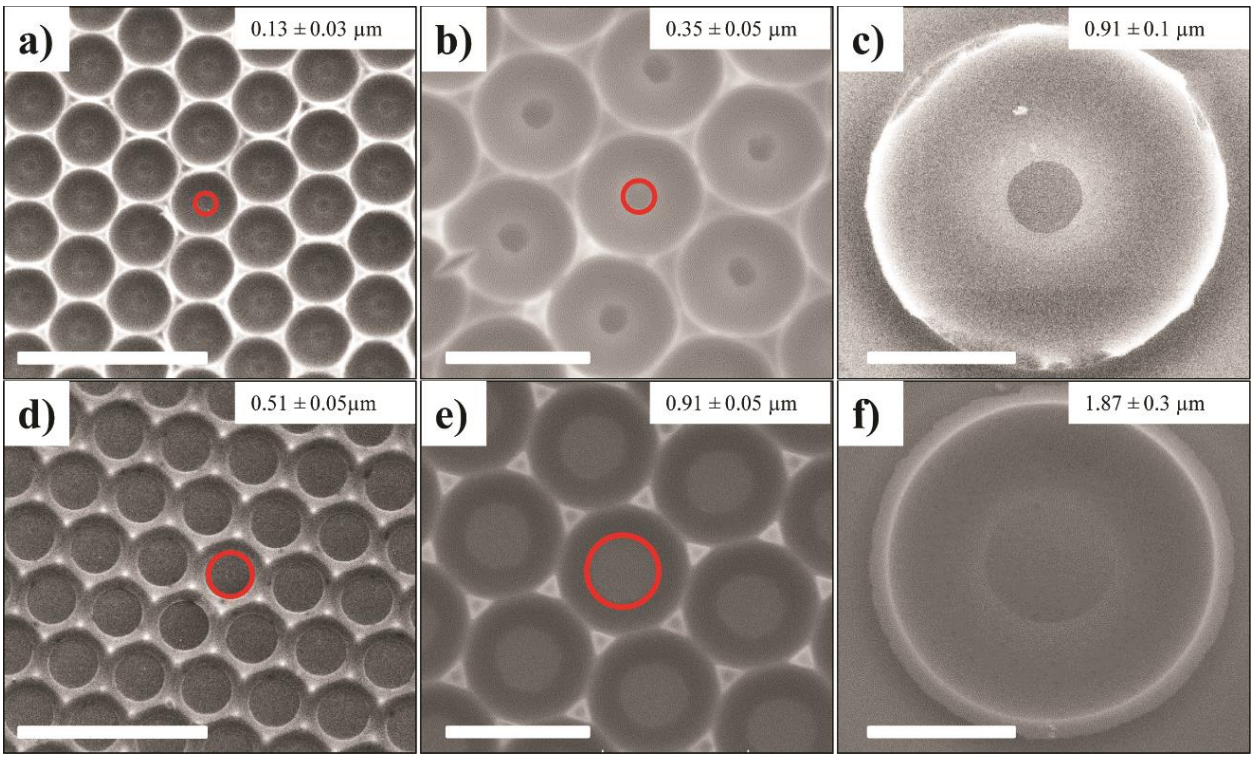


Figure 2.2. Scanning electron micrographs of silica pattern with different sizes of openings and pitch. (a-c) Silica pattern created by using 0.75, 2 and 10 µm polystyrene (PS) microspheres with 2 minutes annealing at 125 °C. (d-f) Silica pattern created by using 0.75, 2 and 10 µm PS microspheres with 4 minutes annealing at 125 °C. Scale bars: 2 µm. Red circles are guides to highlight exposed openings. The values in the upper right corner of each image indicate the average measured radius of the openings.

facilitate coalescence of the individual Ga nanodroplets into a single nanodroplet including extreme applied negative potentials, heating to ensure melting, and acid etching to remove surface oxides. Although each method was effective to some degree, the easiest and most consistent was an acid etching step and was adopted for subsequent experiments reported here.

After brief acid etching in 1% HF(aq), the silica template was removed and the Si substrates were only coated with regular patterns of Ga nanodroplets at the pitch and size defined by the previous template (Figure 2.3a-e). Large field-of-view scanning electron micrographs were analyzed to determine the distribution of sizes for each templating condition (Figure 2.4a-e). The monodispersity of the Ga nanodroplet size tended be greater for the templates with smaller openings. Nominally, the pitch and size of these nanodroplets corresponded to respective packing densities of 2.3×10^8, 2.1×10^8, 3.7×10^7, 3.5×10^7, and 1.3×10^6 cm^{-2}, respectively, and a total fractional area coverage of 1.3, 1.1, 2.3, 2.1, and 12.7 %, respectively.

These templated Ga nanodroplet films were then used as platforms for benchtop ec-LLS preparation of Ge nanowires. Representative voltammetric responses for a bare n^+-Si substrate and a n^+-Si substrate coated with Ga nanodroplets ($\overline{d}$ = 0.24 μm) are shown in Figure 2.5. In the absence of any film, the n^+-Si substrates were only active towards H_2 evolution at extreme (< -2.0 V vs. Ag/AgCl) applied bias. Upon decoration with Ga droplets, the activity for H_2 evolution increased slightly, with some modest H^+ reduction current apparent at <-1.6 V vs. Ag/AgCl. Immersion of this same electrode in an identical electrolyte that also contained dissolved GeO_2 yielded a substantially altered voltammetric response. In this case, an initial cathodic wave was noted at ~ -1.25 V vs. Ag/AgCl followed by an increased cathodic current at more negative potentials. Upon reversing the sweep direction, a crossover in the current-potential trace was observed, similar to the voltammetric feature reported in the voltammograms of metal electrodeposition on a solid electrode.[4]

A potential step waveform with E_{step} = -1.6 V vs. Ag/AgCl for t = 60 min was used for the ec-LLS Ge nanowire deposition. Representative chronoamperometric responses for early times ($0 < t < 2$ min) for substrates loaded with Ga nanodroplets with $\overline{d}$ = 0.05, 0.08, 0.24, 0.29, and 0.63 μm are shown in Figure 2.6. None of the recorded responses fit cleanly with either simple Cottrellian behavior. Further, the shape of the current transients changed noticeably as the mean diameter of the Ga nanodroplets increased. For the smallest nanowires, the current decreased

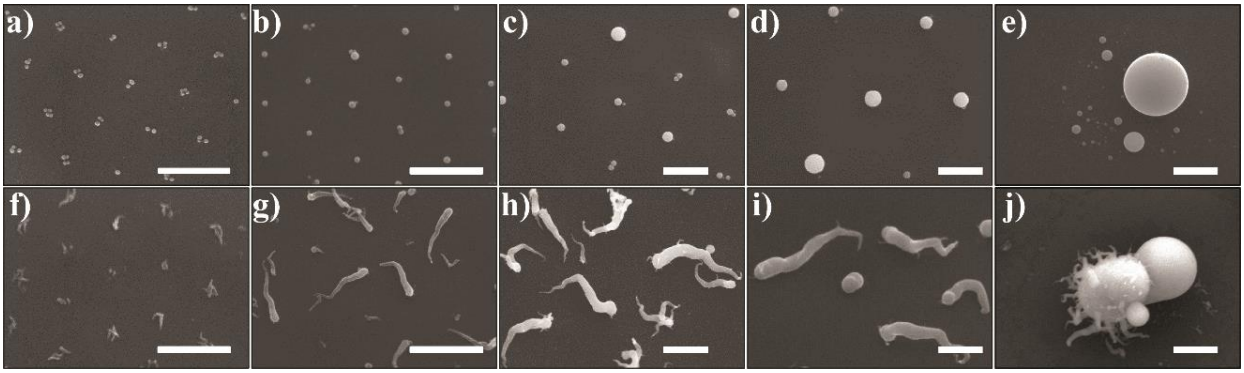


Figure 2.3. Scanning electron micrographs of Ga nanodroplets (a-e) before and (f-j) after Ge nanowire ec-LLS. Each vertical pair of images represents a matched pair of conditions, i.e. Ga nanodroplet films with the size and pitch shown in the top micrograph were used to electrodeposit the Ge nanowire films shown in the bottom image. Scale bars: 1 μm.

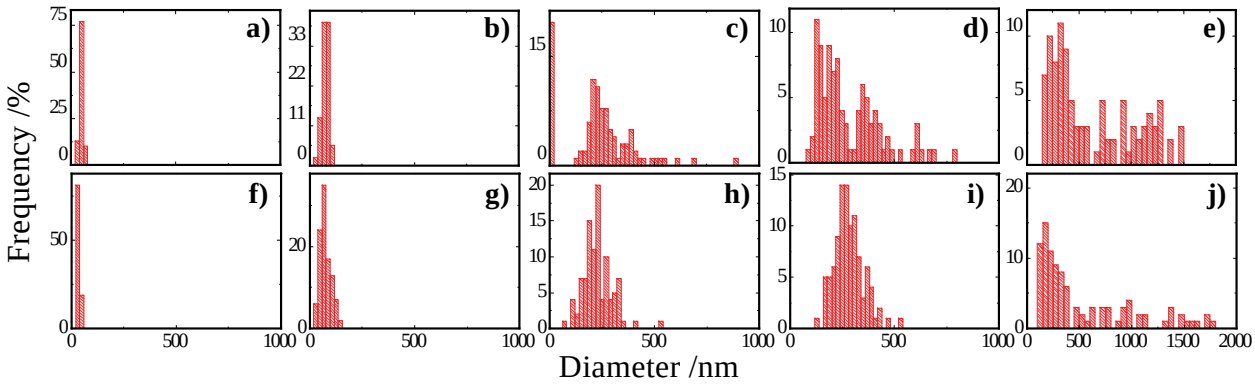


Figure 2.4. Observed distributions of (a-e) Ga nanodroplet diameters and (f-j) Ge nanowire base diameters for the corresponding samples shown in Figure 2.3.

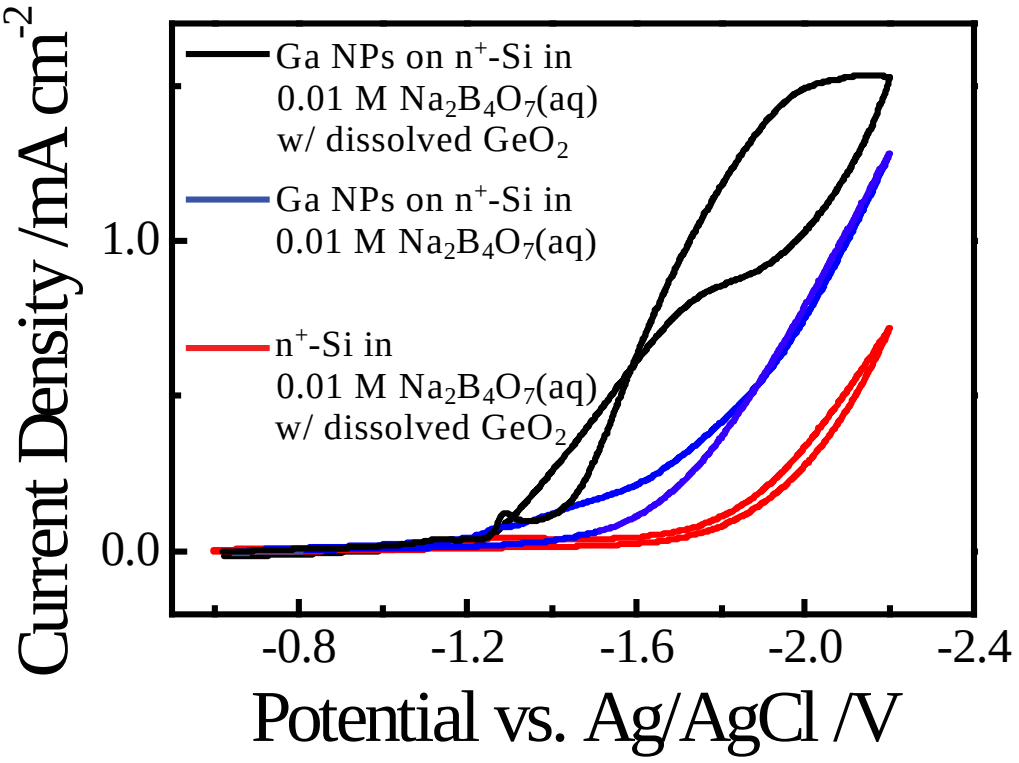


Figure 2.5. Current-potential response for n^+-Si electrode coated with Ga nanodroplets immersed in 0.1 M GeO_2 (aq) (black line), n^+-Si electrode coated with Ga nanodroplets in electrolyte without 0.1 M GeO_2 (aq) (blue line) and bare n^+-Si electrodes in electrolyte with 0.1 M GeO_2 (aq) (red line).

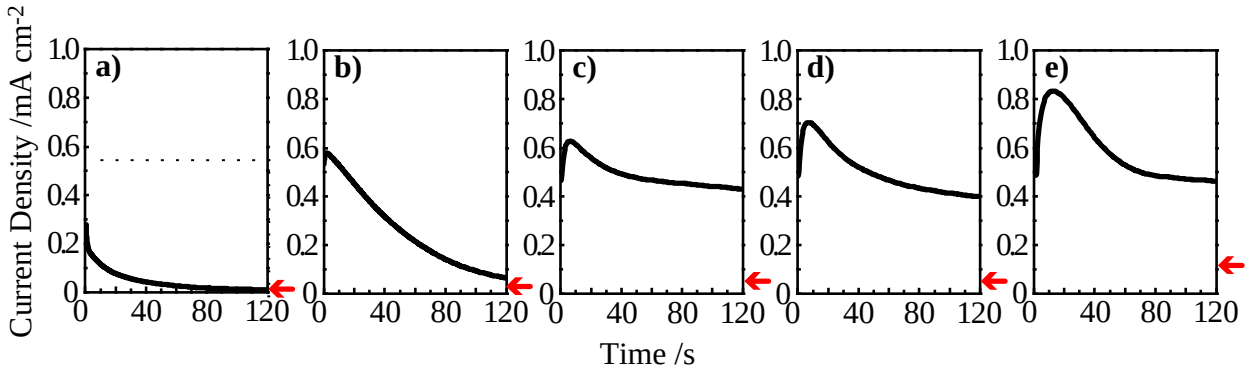


Figure 2.6. Current-time response for n^+-Si electrodes coated with Ga nanodroplets immersed in an aqueous solution containing 0.01 M $Na_2B_4O_7$ and 0.1 M GeO_2 and biased at -1.6 V vs Ag/AgCl. The chronoamperometric responses correspond to Ga nano/microdroplet films as shown in Figure 2.3(a), 2.3(b), 2.3(c), 2.3(d), and 2.3(e), respectively. Red arrows indicate steady-state current for H_2 evolution in just an aqueous solution of 0.01 M $Na_2B_4O_7$ after Ge ec-LLS.

almost instantly following the application of the bias. The decay was non-exponential and noticeably slowed in rate of decrease after ~1 s. This chronoamperometric response did not follow instantaneous/progressive nucleation models used to analyze typical electrodeposition processes.[5] The measured current density at 120 s ($i_{t = 120\ s}$) was small but remained non-zero ($i_{t = 120s}$ = 0.023 mA cm^{-2}). This residual current density corresponded to the same current density measured for H_2 evolution if the electrode was removed, washed, re-immersed in just blank electrolyte (i.e. no dissolved GeO_2), and biased at the same applied potential. For the next smallest diameter Ga nanodroplet films, the transient recorded during the ec-LLS process showed a slight hump in the current-time trace at t = 1.5 s, nominally similar to the increased current measured during the nucleation phase of a typical electrodeposition potential step experiment. Again, the current-time profile did not fit any known nucleation model and the value of $i_{t = 120s}$ (0.06 mA cm^{-2}) closely matched the current density measured for H_2 evolution in control experiments.

For increasingly larger diameter Ga nanodroplet films, the ec-LLS current after the appearance of a peak current was decidedly non-zero, with $i_{t = 120\ s}$ at an approximately constant value of ca. 0.45 mA cm^{-2} for the three largest Ga nanodroplets. In comparison, the separately measured steady-state faradaic current density for H_2 evolution at these electrode platforms was only 0.05 mA cm^{-2}, 0.05 mA cm^{-2}, and 0.11 mA cm^{-2}, respectively. To be clear, these values of $i_{t = 120s}$ were quasi-steady-state currents and not indefinitely unchanging, as after enough time (> 1000 s), all the current values slowly decreased to the current densities for H_2 evolution. Still, the large quasi-steady-state values of $i_{t = 120s}$ thus implied the balance of the current passed in this time window was related to the ec-LLS process and not H^+ reduction, i.e. the crystalline nanowire formation was ongoing. Accordingly, while the current-time profile at times shorter than the peak current ('hump') value moderately followed instantaneous nucleation (as has been observed previously[6]), the current-time responses at longer times for the larger Ga nanodroplets were decidedly not fit by any known nucleation model.

The resultant Ge nanowires from the ec-LLS process at each Ga nanodroplet are shown in Figure 2.4f-j, matched with the substrates in Figure 2.4a-e, respectively. These nanowires were largely single crystalline (i.e. the majority of nanowires viewed by TEM were confirmed as single-crystalline) as opposed to polycrystalline or amorphous, as verified by transmission electron microscopy (Figure 2.7). The scanning electron micrographs in Figure 2.4 show several noteworthy features. First, nanowires only were deposited at discrete locations, in accord with the

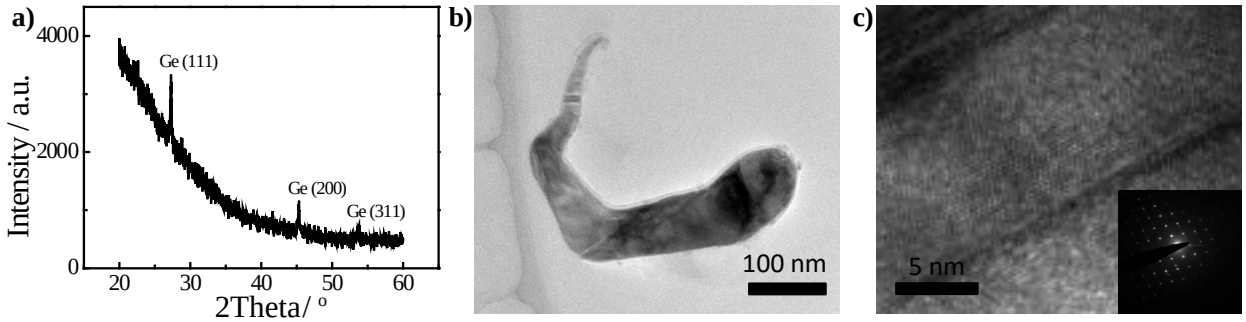


Figure 2.7. (a) Measured X-ray diffraction pattern collected after Ge electrodeposition with Ga nanoparticles possessing $\overline{d}$ = 0.08 μm at -1.6 V vs Ag/AgCl for 1 h. (b) Transmission electron micrograph of an individual Ge nanowire electrodeposited at −1.6 V vs Ag/AgCl for 1 h. (c) High-resolution transmission electron micrograph of same Ge nanowire as in (b). Inset: selected area electron diffraction pattern indicating a diamond cubic lattice and single crystallinity.

separate premises that ec-LLS can only be facilitated at the liquid metal and that the rate of electrodeposition of Ge on crystalline Si at these benchtop conditions is negligible.[1, 6] Second, the nominal size of the nanowires tracked the original size of the Ga nanodroplets. Figure 2.4f-j shows the corresponding base diameter distributions which closely follow those for the parent Ga nanodroplets in Figure 2.4a-e. Third, all electrodeposited Ge nanowires showed a consistent tapering from bottom to top. The apparent tapering for the nanowires in Figure 2.3f-i appeared invariant with respect to the parent Ga nanodroplet size, with cone angles measuring 10.2, 10.0, 10.7, and 9.1°, respectively. Fourth, the largest Ga drop sizes still facilitated Ge ec-LLS but did not yield a single electrodeposited Ge nanowire per Ga microdroplet.

Figure 2.8a shows a representative top-down electron micrograph of a Ge nanowire film made with small Ga nanodroplets. From this vantage point, the orientations of the majority of nanowires appeared random, i.e. no obvious specific set of orientations to suggest epitaxy with underlying Si substrate. Image analysis was performed to explicitly plot the frequency per angle of all possible orientations (Figure 2.8b). The aggregate distribution of measurements of the angles of orientation for each electrodeposited nanowire with respect to a reference line (e.g. the bottom edge of the image) did not show preferential direction, in contrast to a previous report.[1]

Elemental mapping of the electrodeposited materials after an intermediate time was performed to identify where the Ga micro/nanodroplet resides (i.e. on the substrate or on the nanowire). Figure 2.9 in conjunction with scanning electron microscopy indicated the ec-LLS experiments with the largest Ga droplets showed only a round mass of Ge rather than a high aspect-ratio morphology. There was clear separation between the Ga and Ge components, i.e. neither mass appeared to be a uniform mixture of the two elements. Under the employed conditions, the electrodeposited Ge appeared to be roughly the same volume as the Ga droplet and covered with numerous smaller Ge filaments/protrusions.

D. Discussion

Two distinct conclusions can be drawn from the presented data. First, the employed patterning method is useful for performing ec-LLS with precisely-sized liquid metal nanodroplets but introduces a complicating aspect with respect to crystallinity. Second, the data indicate the ec-LLS process is sensitive to the size of the employed liquid metal. The current-time transients for the Ge nanowire ec-LLS process are affected by the liquid metal nanodroplet size. Similarly, the

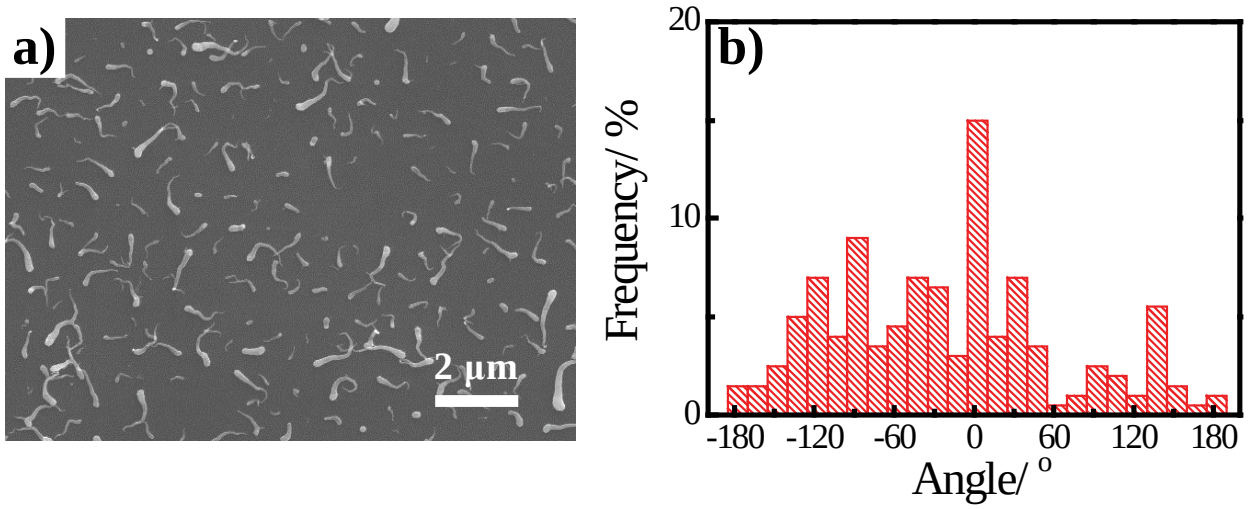


Figure 2.8. (a) Plan-view scanning electron micrograph of a Ge nanowire film prepared with ec-LLS performed in an aqueous solution containing 0.01 M $Na_2B_4O_7$ and 0.1 M GeO_2 and biased at -1.6 V vs Ag/AgCl. (b) Observed distribution of Ge nanowire orientations plan view image as in (a).

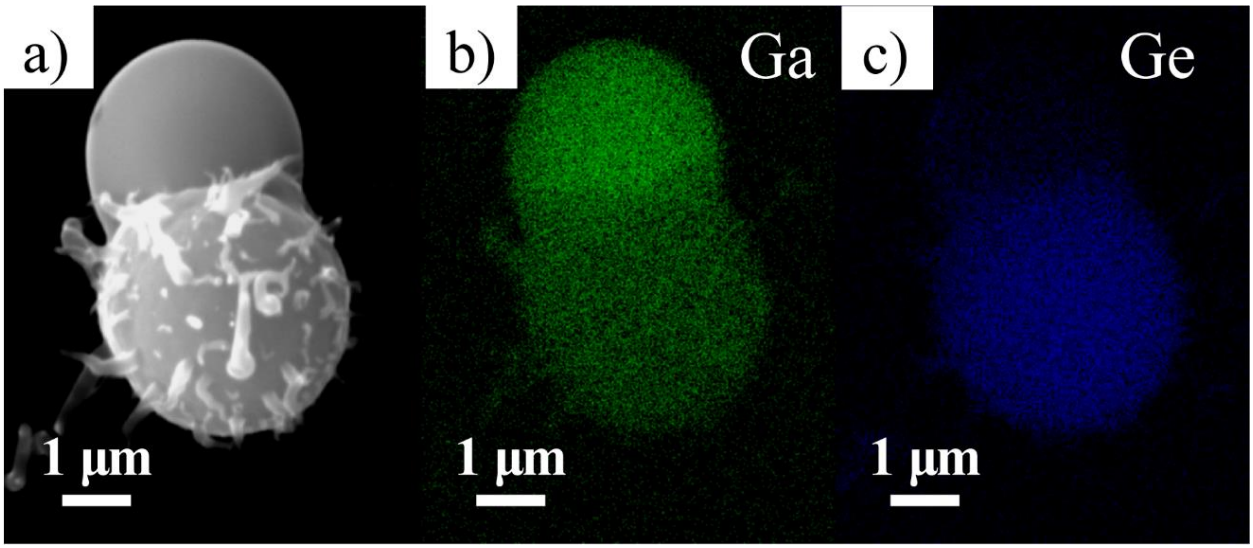


Figure 2.9. (a) Scanning electron micrograph of a Ge crystal prepared by ec-LLS in an aqueous solution containing 0.01 M $Na_2B_4O_7$ and 0.1 M GeO_2 and biased at -1.6 V vs Ag/AgCl with Ga microdroplet with a radius = 3 µm. (b,c) Energy dispersive spectroscopic elemental mapping of same area in (a) with b) the *K* line for Ga and c) the *K* line for Ge.

size of the liquid metal nanodroplet directly impacts the morphology of the resultant, as-prepared crystalline Ge materials. Each point is discussed separately below.

Natural Lithography for ec-LLS with Liquid Metal Nanodroplets Although sophisticated methods that pattern features well below a micron are constantly being developed and refined, patterning at this scale for benchtop research with high fidelity is still not routine. The natural lithography approach here with silica as a sacrificial templating material is an attractive method for preparing micro/nanodroplets with arbitrary pitches and diameters because it required no sophisticated instrumentation beyond a spin coater and oven. For the purpose of preparing group IV semiconductor nanowire films with definable nanowire sizes and density *via* ec-LLS in a simple process, this tactic proved effective. However, in the context of Ge ec-LLS for epitaxial crystal growth, the employed patterning process introduced one complicating factor - the likelihood of a surface oxide between the Si and Ga components. Although Ga will oxidize in air, at the negative electrochemical potentials suitable for Ge ec-LLS, any Ga oxide is likely electrochemically removed.[7] Unprotected Si exposed to air and even slightly elevated temperatures will rapidly form a thin surface oxide film that cannot be electrochemically removed.[8] Accordingly, the annealing and nano/microsphere removal steps undoubtedly introduced some surface oxidation of the Si substrate. Etching of the native oxide could not be performed without simultaneous degradation of the silica film. In this capacity, using an alternative templating material that could withstand etching steps would be beneficial. Nevertheless, since these substrates were degenerately doped and the native surface oxide was likely thin, electrodeposition was still possible on these platforms, i.e. electron transport from the Si substrate across the oxide to the Ga nanodroplet occurred at a sufficient enough rate to support heterogeneous reduction of dissolved GeO_2. The overall rate of the ec-LLS process was impeded by the absence of a pristine interface, slowing the crystal growth rates relative to our related previous study[1] of Ge ec-LLS (~ 0.2 vs ≥ 0.9 nm s^{-1}, respectively) for otherwise the same applied electrochemical conditions.

In this work, electrodeposition by ec-LLS still produced highly crystalline nanowires. However, the presence of an interfacial oxide apparently was sufficient to prevent *epitaxial* single crystalline Ge nanowire growth, as the cumulative data do not indicate a preferred nanowire orientation on these single crystalline electrode substrates. This observation means that direct and clean contact between the substrate and liquid metal is necessary for epitaxial nanowire electrodeposition by ec-LLS with Ga nanodroplets under these conditions.

Dependence of ec-LLS Nanowire Process with Flux Conditions and Liquid Metal Size

Although all electrodeposition experiments were performed for the same total time and under the same electrochemical conditions, the cumulative data suggest that the Ga droplet size impacted the ec-LLS process in multiple ways.

The quasi-steady-state current in the chronoamperometric data seen for the larger Ga nanodroplets implies two important aspects. First, time-invariant current strongly validates the notion that all GeO_2 reduction occurs exclusively at Ga. That is, when electrochemical reduction of dissolved GeO_2 occurs only at each Ga droplet, the Ga droplets are small enough to function as 'ultramicroelectrodes' operating with radial diffusion transport. At intermediate times, the total film electrode responses will mirror an array of ultramicroelectrodes that should exhibit time-invariant current responses when their diffusional fronts do not overlap.[9] Second, when a steady-state current for the reduction of Ge is observed and no amorphous Ge is produced/detected, ec-LLS must therefore proceed at the rate dictated by mass transport of GeO_2 to the Ga/electrolyte interface, i.e. ec-LLS is clearly not limited at short times by factors pertaining to either the kinetics of GeO_2 reduction or Ge nucleation/crystallization. Conversely, the lack of a steady-state characteristic in the chronoamperometric data for ec-LLS at the smallest Ga nanodroplets indicates those ec-LLS processes were not governed by mass transport of GeO_2 throughout the whole duration of ec-LLS or else they too would have exhibited some quasi-steady-state type behavior. Instead, some other (e.g. kinetic, crystallization) factor(s) dictated the rate of ec-LLS production of the smallest Ge nanowires. To be clear, at long times (>1000 s), the slow decrease of the current at large Ga droplets indicated that non-mass-transport factors impacted those ec-LLS processes at the latter stages. Still, the take home point is that changes in the flux conditions of the reduction of species in the electrolyte don't seem to affect whether ec-LLS occurs or not. Further, since the general shape of the resultant Ge nanowires was similar at both small and large Ga droplets, we conclude the mass transport of species to the liquid metal electrode in an ec-LLS process is not the most critical step with regards to crystal formation.

For ec-LLS experiments that yielded nanowires, two morphological features were consistent. First, each nanodroplet, irrespective of the apparent flux condition of GeO_2 to its surface, yielded largely just one single-crystalline Ge nanowire. On occasion, several clusters of nanowires could be seen, which we attribute to an insufficient coalescence following the initial electrodeposition of the Ga in the openings of the silica template. One single-crystalline nanowire

from one nanodroplet is consistent with the premise that just a one nucleation event occurred within the confined volume of a liquid metal nanodroplet. Again, this observation was independent of the apparent flux condition of GeO_2 to the nanodroplet/electrolyte interface. Second, the morphology of the nanowires from the larger and smaller nanodroplets was nominally the same. Both large and small nanowires produced through ec-LLS were tapered with a nominal cone-angle of 10° and showed no Ga accumulation at the tip apex. Tapering in catalyzed nanowire formation is common and can arise from multiple phenomena.[10] However, tapering in conjunction with a disappearance of the metal crystallization catalyst implies incorporation of the metal into/onto the nanowire. The cone angles measured here were comparable to other reports of tapered group IV nanowires where metal incorporation has been observed, albeit those instances were based on much higher temperature deposition processes.[10-12] For context, in group IV nanowires grown by vapor-liquid-solid processes, the size of the metal growth catalyst can strongly influence the extent of tapering.[11] Elemental mapping shown here does suggest some specific interaction between Ga and Ge. Ga was apparent in/on the electrodeposited Ge materials by EDS. However, the crystallographic data compiled here (Figure 2.7) and previously[1] argue strongly against a pure Ge-Ga alloy. Previous studies have shown that the liquid metal in the semiconductor acts as a dopant that increases conductivity (p-type for Ga in Ge).[13] Since the tapering of nanowires is largely independent of Ga nandroplet size, the data argue the intrinsic interactions (e.g. wetting, solubility) between the crystal and liquid metal in ec-LLS are likely the more relevant factors on nanowire morphology.[13-14] As argued for other nanowire growth models, changing the interfacial energies at the Ge-Ga interface through adsorbates[14] or the type of liquid metal should alter the tapering in nanowires produced by the ec-LLS shown here.[14] Such experiments will be reported in Chapter 3.

For the largest Ga droplets, the morphology of the as-produced crystalline Ge was decidedly not a single nanowire. Instead, large symmetric Ge crystallites coated with multiple nanowires were seen, indicating multiple nucleation events occurred during the ec-LLS process. We interpret the data to suggest that an initial large Ge crystal formed that was likely coated with enough Ga to form secondary ec-LLS sites. It is possible that given enough time, the large Ge deposits seen here would have become a microwire with an aspect ratio and cone angle similar to the nanowires shown here. Separate measurements without a template (and without a native oxide on the Si substrate) have shown the propensity for large Ga microdroplets to produce similarly tapered microwires (Figure 2.10)[15]. Still, in those observations additional ‘side’ nanowires as seen

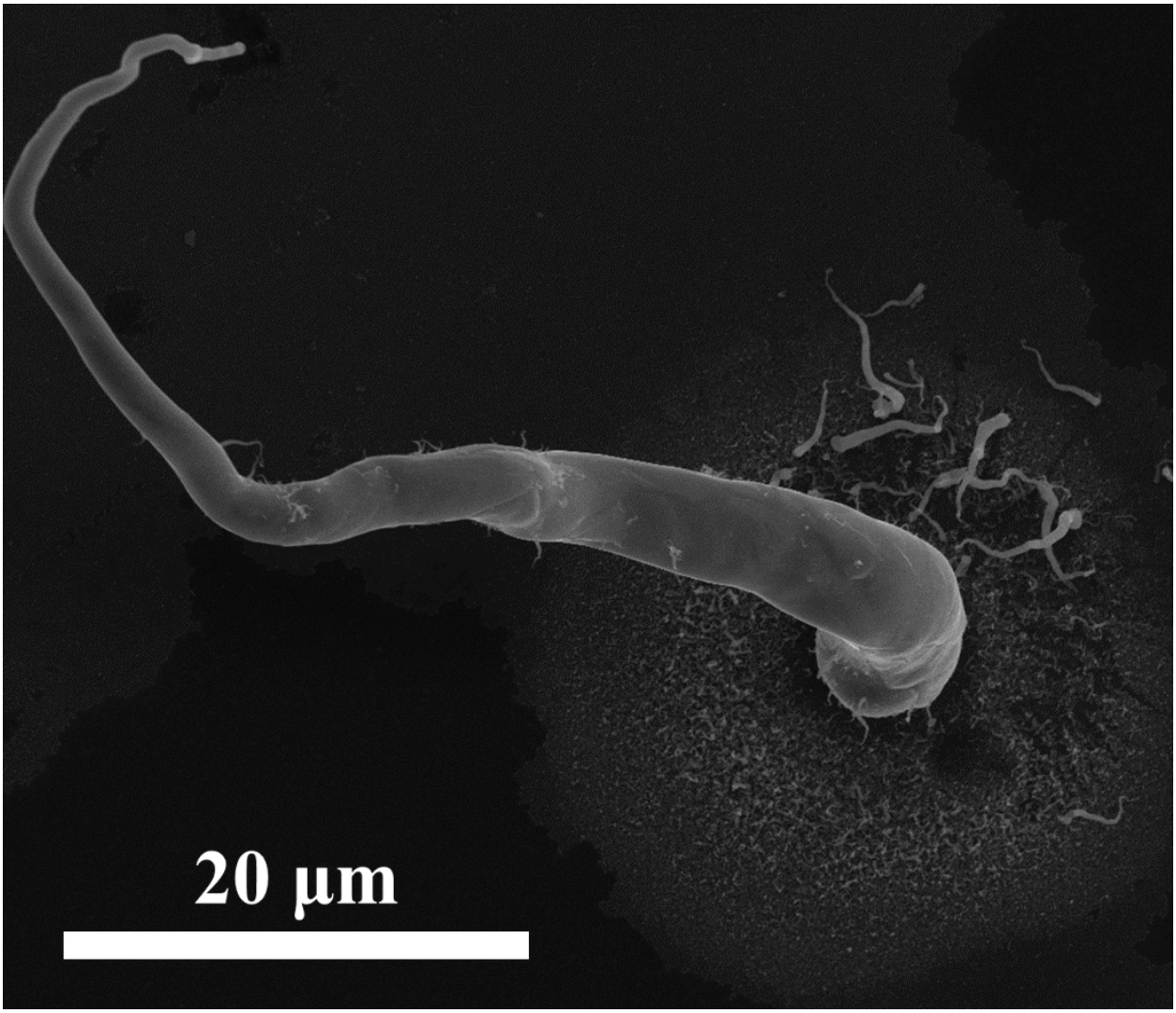


Figure 2.10. Scanning electron micrograph of a Ge microwire electrodeposited on a pristine n^+-Si substrate *via* ec-LLS using a Ga microdroplet prepared without natural lithography.

here in Figure 2.9 were observed, implying that past some critical size, the probability for multiple nucleation events becomes significant. Although not intended, the results thus show the possibility to build branched nanowires *via* ec-LLS if secondary crystallization nucleation events are purposely induced. Such tactics may be useful in increasing the volume fill fractions of nanowire films in applications like Li-ion batteries.[16]

A final comment should be made on further interpretation of the chronoamperometric response during nanowire growth by ec-LLS. The possibility of a 'moving boundary'[17] condition exists when the liquid metal remains affixed on the nanowire top. Specifically, during the course of the ec-LLS process, the site of GeO_2 reduction is displaced upward by the crystal growth. Thus, rapid nanowire crystal growths will necessarily complicate the ultramicroelectrode behavior. Both numerical modeling of the expected current-time transients for these ec-LLS experiments and the electrodeposition of widely spaced Ge nanowires (or just a single Ge nanowire) would be highly informative for more extensive correlations between the observed chronoamperometric data and the resultant crystal growths.

E. Conclusions

The presented data show the first direct assessment of the influence of Ga droplet size on the capacity to support Ge ec-LLS. Irrespective of size, all Ga droplets were active for producing crystalline Ge from an aqueous solution of dissolved GeO_2. These data show that Ge nanowire sizes can be predictably controlled using specifically-sized Ga nanodroplets. Steady-state features in the chronoamperometric responses for ec-LLS implied complex interdependence between mass transport of GeO_2 and crystal nucleation events. The data implicate factors other than Ga droplet size as the main factor that induces tapering the nanowires. Ga droplets with radii ≤ 0.63 μm produced only one single Ge crystalline nanowire. These data will be useful in learning how to tune the ec-LLS process as a tailorable synthetic strategy for nanowire materials in specific applications.

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CHAPTER 3

Direct Electrochemical Deposition of Crystalline Silicon Nanowires at $T \geq 60°$ C

A. Introduction

Silicon (Si) nanowires are promising materials for a wide variety of new technologies such as ultra-small transistors,[1] next-generation photovoltaics,[2] photoelectrochemical cells,[3] nanostructured thermoelectrics,[4] and rechargeable batteries.[5] A major impediment to the practical realization of Si nanowires for these applications is that existing bottom-up synthetic strategies are either energy intensive, involve high process temperatures, require evacuated reaction chambers, utilize toxic gaseous reactants, do not produce crystalline materials directly, or some combination thereof.[6-9] Ec-LLS process emerged as a low temperature crystal growth process to bridge this gap. We previously established the ec-LLS process for crystalline Si, using bulk liquid gallium (Ga) pool electrodes for the direct electrodeposition of crystalline Si microcrystals at temperatures below 100 °C.[10] Crystalline Ge nanowires were also grown via ec-LLS at room temperature using Ga nanodroplets.[11-12] Therefore, the preparation of crystalline Si nanowires by ec-LLS should be feasible.

In this chapter, we present data on an ec-LLS process that uses liquid Ga-containing nanodroplets to produce crystalline Si nanowires. Figure 3.1 schematically describes the method discussed herein. The purpose of these studies is to identify the influence that changes in temperature, underlying substrate, liquid metal composition, and wetting of the liquid metal on the underlying substrate have on the as-prepared Si materials. The data reported here advance four new concepts in the preparation of Si nanomaterials that have not been individually or collectively demonstrated. First, this report is the first communication of an electrolyte bath and set of electrochemical parameters that allow the selective electrodeposition of Si at Ga-based nanodroplet electrodes. Second, the results herein show that electrodeposition of Si at Ga-containing nanodroplets yields crystalline Si nanowires at temperatures as low as 60 °C and

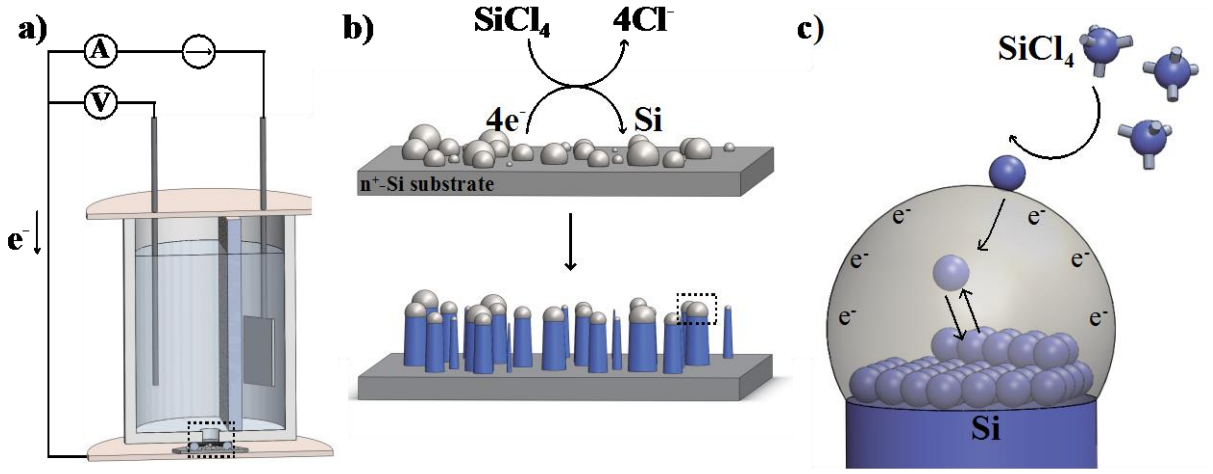

Figure 3.1. a) Schematic depiction of the three electrode electrochemical cell setup used for Si nanowire ec-LLS. A porous plate separated the working and reference electrode compartment from the counter electrode. b) A pictorial representation of the Si ec-LLS nanowire deposition process, where the electrochemical reduction of $SiCl_4$ seeded the growth of Si nanowires only at liquid metal nanodroplets. c) A microscopic illustration of the elementary steps in the Si nanowire ec-LLS process (not drawn to scale).

therefore represents a distinct ec-LLS process. Third, evidence contained in this report support the premise that *epitaxial* electrodeposition of crystalline Si nanowires is possible. Fourth, results from electron micrograph analyses indicate that modification of the surface of a liquid metal nanodroplet alters the shape of the resultant Si nanowire produced through ec-LLS. These points are detailed and discussed below.

B. Methods

Materials and Chemicals Methanol (ACS grade, BDH), acetone (ACS grade, BDH), HF (49%,Transene Inc.), $SiCl_4$ (99.99+%, Strem Chemicals), $Ga(NO_3)_3$ (99.9%, Aldrich), KNO_3 (99+%, Acros Organics), In (99.9+%, Aldrich) and Ga (99.99%, Aldrich) were used as received. Solutions of propylene carbonate (99.5%, Acros Organics) containing tetrabutylammonium chloride (TBACl) (95%, Alfa Aesar) were dried for 2 days after preparation with molecular sieves (4A, 8-12 mesh, Sigma-Aldrich) before use. Degenerately doped n^+-Si wafer substrates (Crysteco, <100> As-doped, <0.007 ohm cm, 0.625 ± 0.020 mm thick; MEMC, <111> As-doped, 0.003-0.004 ohm cm, 0.510-0.540 mm thick) were cleaned and then diced into pieces of approximately 0.6 x 0.6 cm. The silicon wafers were initially degreased with acetone and ethanol. These wafer sections were then etched for 1 min in 5% HF(aq) solution. Platinum mesh and wire (99.9% trace metals basis) were purchased from Sigma-Aldrich and flame cleaned in a propane torch before use. Water with a resistivity > 18.2 MΩ·cm (Barnsted Nanopure) was used throughout.

Electrodeposition of Ga Nanoparticles Ga electrodepositions were performed with a CH Instruments 760C potentiostat. The backsides of the Si wafer sections were first lightly scratched with a diamond-tip scribe, etched with 5% HF(aq), rinsed clean with water, and then rubbed with Ga-In eutectic alloy to make an Ohmic contact. The Si substrates were then placed on a 1 × 2.5 × 0.2 cm stainless steel support and mounted underneath a custom Teflon cell featuring a 0.6 cm outer-diameter Viton O-ring (size # 006). The cell was press-fit on top of the Si wafer sections, exposing a surface area of 0.077 cm^2. The cell was then filled with an aqueous solution of 0.1 M $Ga(NO_3)_3$ and 0.1 M KNO_3. A Pt mesh counter electrode and a Ag/AgCl (sat. KCl) reference electrode were employed for Ga electrodeposition. A constant bias of -1.8 V vs *E*(Ag/AgCl) was applied for 300 s to nucleate and grow discrete Ga nanodroplets. No effort was made here to rigorously control the size distribution of the droplets.

Ga-In eutectic alloy (*e*GaIn, 3:1 wt/wt) nanodroplets were also prepared but not by electrodeposition. Instead, liquid *e*GaIn immersed in glycerol/H_2O (1:1 v/v) with polyvinylalcohol (1 wt%) as a surfactant was sonicated to create a suspension of liquid metal nanodroplets.[13] *e*GaIn nanodroplets were then drop cast onto n^+-Si(100) substrates. These samples were dried under $N_2(g)$ and then plasma etched in an Ar plasma (Plasma Etch, PE-50) briefly to remove adsorbed polyvinylalcohol. For a subset of these samples, a thin layer of silica was then spin cast (2400 rpm) on top of the *e*GaIn nanodroplet film using a commercial spin-on glass (SOG) formulation (Filmtronics) diluted in ethanol (1:10 v/v).

Si Nanowire ec-LLS All Si ec-LLS experiments were performed with a CH Instruments 760C potentiostat in a custom-built two compartment glass cell separated by a porous frit and a hole at the bottom (Figure 3.1a). The hole at the cell bottom was center aligned with a Viton O-ring (size # 006) and press-fit on top of a Ga coated Si wafer section to make the seal. Experiments were performed with a three-electrode configuration, using a Pt sheet as the counter electrode and a flame cleaned Pt wire as the quasi-reference electrode, respectively. The cell was transferred into a N_2-purged dry glove box, loaded with 10-20 mL of electrolyte (0.5 M $SiCl_4$, 0.2 M TBACl in propylene carbonate) then heated to temperature. The cell was capped to prevent electrolyte evaporation and to fix the position of reference and counter electrodes. The cell temperature was established with a sand bath and monitored with a digital thermocouple. After each experiment, the cell was taken out of the sand bath immediately to cool radiatively. Upon cooling to room temperature, the Si wafer sections were removed from the cell, rinsed with water 3 times, and dried under flowing N_2(g). All presented voltammetry was *iR* compensated using the compensation function within the potentiostat software, using a 10 mV step potential.

Galvanostatic (i.e. constant applied current) electrodeposition experiments were favored instead of a potentiostatic (i.e. constant applied potential) protocol for two primary reasons. First, *iR* losses that arise from changes in the overall cell resistance, including the finite resistance of the growing semiconductor crystals, were not an issue in a galvanostatic electrodeposition since the compliance voltage (i.e. the max potential difference applied between the working and counter electrodes to ensure that the counter electrode is not current limiting) was sufficiently large. For the data shown here, the compliance voltage of the electrochemical instrumentation was ±13V, more than sufficient to sustain the applied currents. Conversely, changes in cell resistance in potentiostatic experiments require active *iR* compensation to maintain a constant applied potential.

Second, the Pt quasi-reference electrode was stable during the course of individual experiments but did not provide a stable absolute potential between experiments. Because the applied potential defines the overpotential to drive a redox reaction, we surmised that potentiostatic experiments run at the same nominal applied potential with respect to the Pt quasi-reference electrode would not necessarily be comparable. In contrast, galvanostatic electrodepositions were determined to be very reproducible in terms of the observables described below.

Material Characterization Bulk powder X-ray diffractograms were collected with a line focus Rigaku Rotating-Anode X-Ray diffractometer equipped with a Cu Kα source (λ = 1.5406 Å). Both the source and detector were scanned for data acquisition. Raman spectra were obtained using a Renishaw Raman microscope spectrometer equipped with a Nikon LU Plan 20x objective (*NA* = 0.4) and edge filters to reject the 785 nm excitation line of the diode laser. A total radiant power of 0.112 mW over a 20 μm^2 incident spot size for 30 s was used for spectral acquisition. Samples for transmission electron microscopy (TEM) were prepared by first removing the Si nanowires from the substrate by sonication in isopropanol for 30 s and then drop casting approximately 40 µL of this suspension onto 400 mesh copper TEM grids coated with an ultra-thin carbon film (Ted Pella). High-resolution transmission electron microscopy (HRTEM) and selected area electron diffraction (SAED) were performed with a JEOL 3011 TEM equipped with a LaB_6 source operated at 300 kV. Energy dispersive spectra were taken with an electron beam at 200 kV and an EDAX r-TEM detector within a JEOL 2010F Analytical Electron Microscope. Scanning electron micrographs (SEM) were taken at FEI NOVA Nanolab Dualbeam Workstation with a Schottky field emitter operated at 10 keV beam voltage and 0.54 nA beam current coupled with a through-the-lens detector. Cross-sectional images were collected with the vertically-mounted substrate tilted 45° towards the substrate surface plane.

C. Results

The voltammetric responses recorded for n^+-Si(111) electrodes and n^+-Si(111) electrodes coated with Ga nanodroplets are shown in Figure 3.2a. In the blank propylene carbonate electrolyte containing only tetrabutylammonium chloride (TBACl), the n^+-Si(111) electrode coated with Ga nanodroplets showed only a modest increase in cathodic current at -2.5 V vs a Pt quasi-reference electrode corresponding to the electroreduction of propylene carbonate. Upon addition of 0.5 M $SiCl_4$, the voltammetric response changed, with the onset of cathodic current

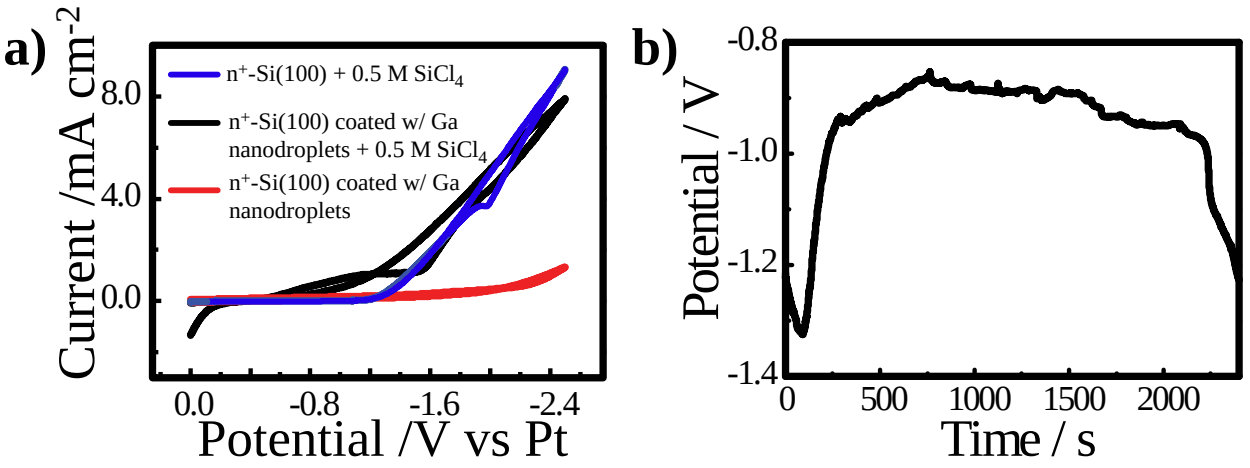

Figure 3.2. a) Voltammetric responses for a bare n^+-Si(111) electrode in propylene carbonate containing 0.2 M TBACl and 0.5 M $SiCl_4$ electrolyte, a n^+-Si(111) electrode coated with Ga nanodroplets immersed in propylene carbonate containing 0.2 M TBACl and 0.5 M $SiCl_4$, and a n^+-Si(111) electrode coated with Ga nanodroplets immersed in propylene carbonate containing only 0.2 M TBACl. (b) Chronopotentiometric response for a n^+-Si(111) electrode coated with Ga nanodroplets immersed in propylene carbonate containing 0.2 M TBACl and 0.5 M $SiCl_4$. A cathodic current of 0.32 mA cm^{-2} at T = 120 °C was used.

occurring at -0.4V vs a Pt quasi-reference electrode. The current passed at these more positive potentials corresponded to the electroreduction of $SiCl_4$,

$$SiCl_4 + 4e^- \rightarrow Si + 4Cl^-$$

In this same solution, the reduction of $SiCl_4$ did not occur on the bare n^+-Si(111) electrodes at potentials less negative than ~ -1.2 V vs the quasi-reference electrode. The data thus indicated there was a finite potential range spanning approximately 0.8 V where $SiCl_4$ electroreduction would occur predominantly at the Ga nanodroplets rather than at the underlying solid substrate.

Figure 3.2b shows a typical chronopotentiometric response for galvanostatic electrodepositions performed at a current density of 0.32 mA cm^{-2} at T = 120 °C. In these experiments, the electrode potential drifted to more negative values from the initial potential during the first 100 s before rapidly drifting back to potentials more positive than -1.0 V vs a Pt quasi-reference electrode. This pattern is consistent with electrochemical removal of any native oxide on the liquid metal droplets, which then allows electroreduction of $SiCl_4$ at oxide-free liquid metal interfaces at less negative potentials. The electrode potential then remained constant until ~ 2400s. Afterwards, the electrode potential drifted quickly to values more negative than -1.2V vs a Pt quasi-reference electrode, indicating the electroreduction of $SiCl_4$ at the underlying Si substrate. This shift to more negative potentials is consistent with loss of the liquid metal cap (*vide infra*), which then forces the electrochemical reduction of $SiCl_4$ to proceed at the bare Si surface. Accordingly, galvanostatic ec-LLS electrodepositions were limited to no more than 2400 s.

Figures 3.3a and 3.3b show scanning electron micrographs and optical photographs of the Ga nanodroplets on n^+-Si(111) substrates before and after a galvanostatic experiment in the $SiCl_4$ electrolyte for 40 min at T = 120 °C. The Ga nanodroplets were initially spherical with a high (> 120 °) wetting contact angle with the underlying Si.

These films appeared shiny with a metallic gray hue (Figure 3.3a inset). After performing an ec-LLS experiment for 40 min at 120 °C, the films appeared a dull, dark brown (Figure 3.3b inset). High magnification scanning electron micrographs showed that the n^+-Si substrate was coated with a film of Si nanowires instead of liquid metal nanodroplets. The individual Si nanowires ranged in diameter between 100 nm and 300 nm. The results shown here nominally followed our previous observations that the size of the initial nanodroplet determined the size of the base of the resultant nanowire (Figure 3.4), i.e. the sizes of the nanodroplet and the diameters of the resultant Si nanowire were strongly correlated.[12, 14] Further, the nanowires had the same

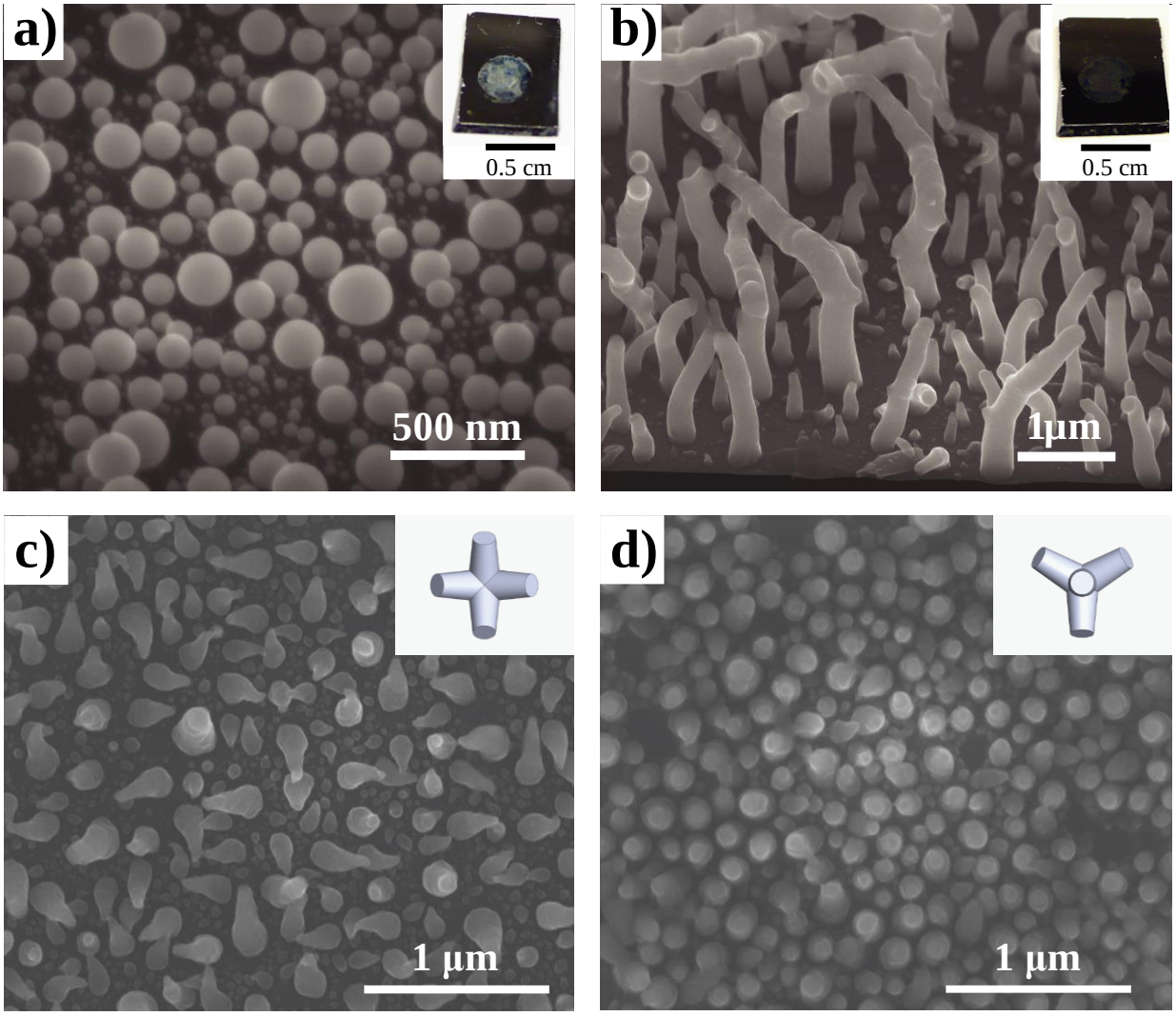

Figure 3.3. Scanning electron micrographs (viewed at a 45° tilt angle) of a n^+-Si(111) substrate coated with Ga nanodroplets (a) before and (b) after Si nanowire ec-LLS at T = 120 °C as in Figure 3.2b. Insets: Optical photographs of a film of Ga nanodroplets before and after Si nanowire ec-LLS. c) Electron micrographs (plan-view) showing orientation of as-prepared Si nanowires after ec-LLS at T = 90 °C on n^+-Si(100) and (d) n^+-Si(111) electrodes. The insets in (c) and (d) describe the four degenerate [111] directions expected for a diamond cubic lattice with respect to each surface plane.

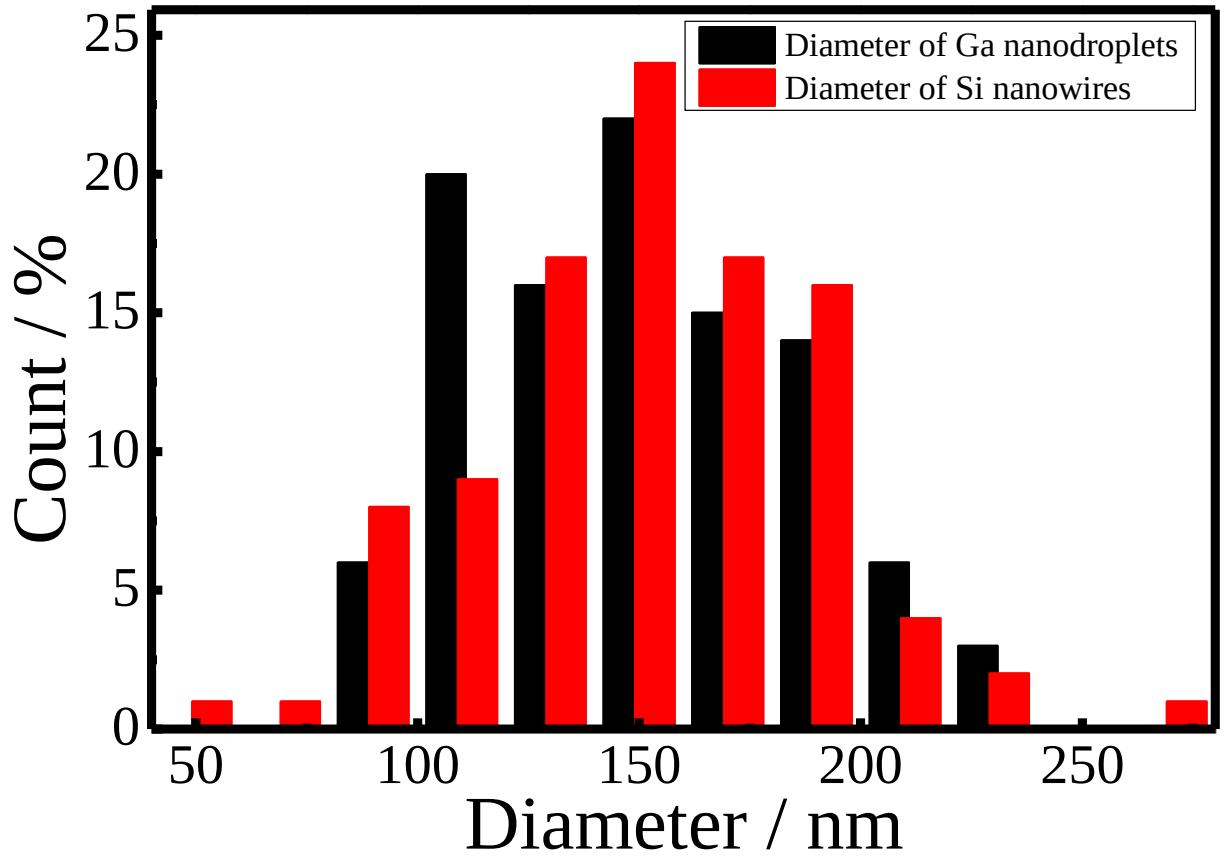

Figure 3.4. Size distribution of the diameters of Ga nanodroplets and Si nanowires shown in Figure 3.3a, b.

areal density as the Ga nanodroplets had prior to the galvanostatic experiment. However, all the nanowires prepared in this way showed a consistent tapered morphology, with an aspect ratio of 4 ± 1.1 and a cone angle of 3 ± 1° (N = 50). A large fraction of Si nanowires was kinked but otherwise oriented normal to the substrate surface plane. Similar to observations made during Ge nanowire ec-LLS, the observed Si nanowire length tracked with electrodeposition time, i.e. longer nanowires were produced with longer electrodeposition times. Also for these long ec-LLS experiments, Ga nanodroplets were not observed on the Si nanowires. For short ec-LLS experiments, a visible nanodroplet remained affixed on the Si nanowires that was confirmed to be composed predominantly of Ga (Figure 3.5). Si nanowire ec-LLS experiments were also performed as a function of temperature (Figure 3.6). At T = 40 °C, no nanowires were observed. Si nanowires were consistently seen at $T \geq 60$ °C, with longer nanowires produced at higher temperatures for the same total growth time. However, the taper of the nanowires was invariant to the experimental temperature. The orientation of the Si nanowires was sensitive to the crystallinity of the underlying substrate. Figures 3.3c and 3.3d shows plan view scanning electron micrographs of Si nanowires grown on n^+-Si(100) and n^+-(111) substrates, respectively. The insets on these figures show the four degenerate <111> directions at each surface plane. On the n^+-(111) substrates, the nanowires were largely normal to the substrate plane but on the n^+-Si(100) surface, the nanowires tended to grow in one of four directions, with 90° in-plane angle separation. These directions matched the four degenerate <111> directions on the (100) surface plane.

Ensemble measurements of the crystallinity of the as-prepared Si nanowires were separately performed. X-ray diffractograms were collected from films electrodeposited on n^+-Si(100) substrates (Figure 3.7a). Although the underlying substrate was a single crystal, diffraction peaks from the substrate for 2θ values between 20 and 60° were not observed due to selection rules that prohibit diffraction along the [100] direction.[15] After electrodeposition of Si nanowires, three diffraction peaks at 2θ = 29.1, 48.3, and 57.1° were consistently observed and indexed to diffraction at the (111), (220) and (311) planes. The signals for diffraction at the (220) and (311) planes indicated that although the nanowires initially grew along the [111] direction, they did not remain single-crystalline along their entire length. For Raman analysis, as-deposited Si nanowires had to be removed from the electrode support prior to inspection. Figure 3.7b shows a single peak at 518.9 cm^{-1}, red-shifted slightly from the expected position of 522 cm^{-1} for crystalline bulk Si.

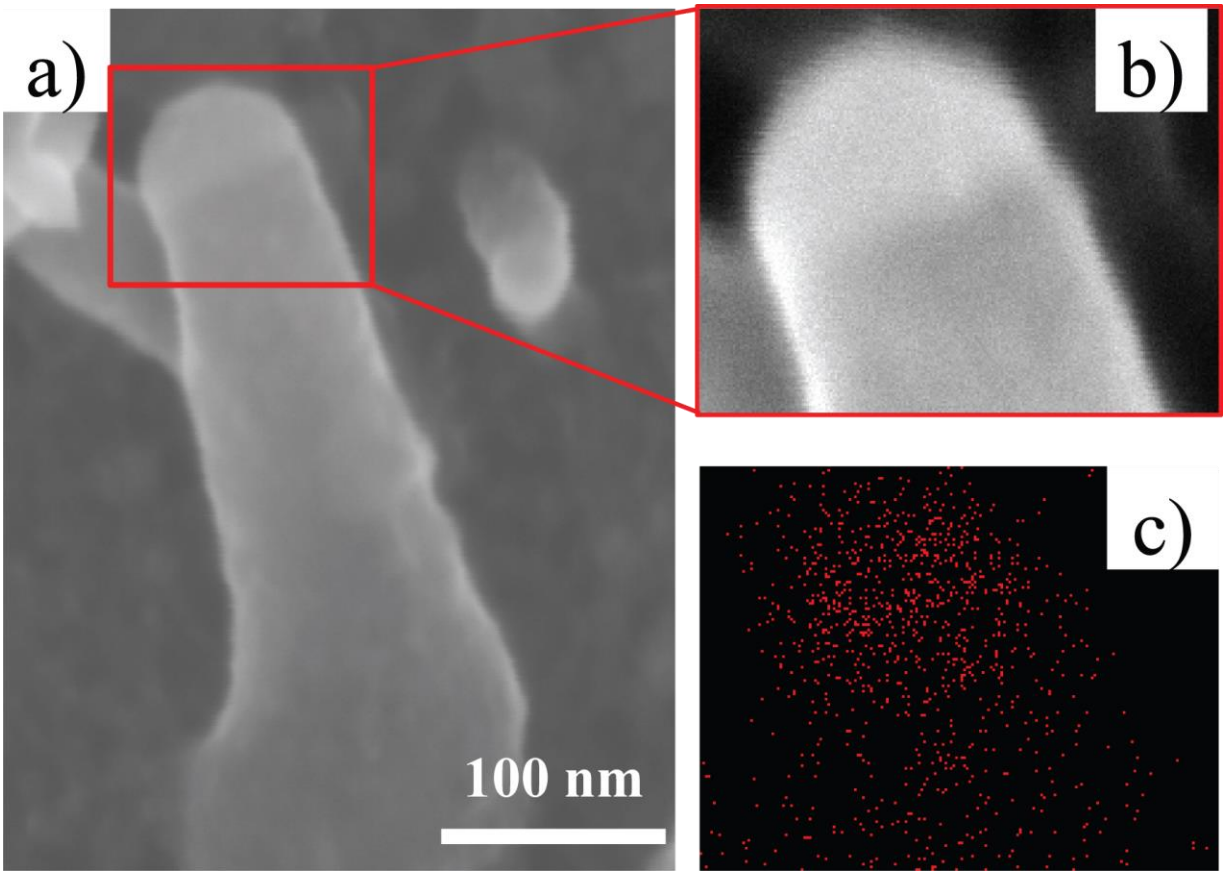

Figure 3.5. (a) Scanning electron micrograph of a Si nanowire prepared by 20 min ec-LLS electrodeposition at 120 °C. (b) Enlarged SEM image of the region indicated in (a). (c) EDX spectroscopic elemental mapping of Ga content in the cap of nanowire as shown in (b).

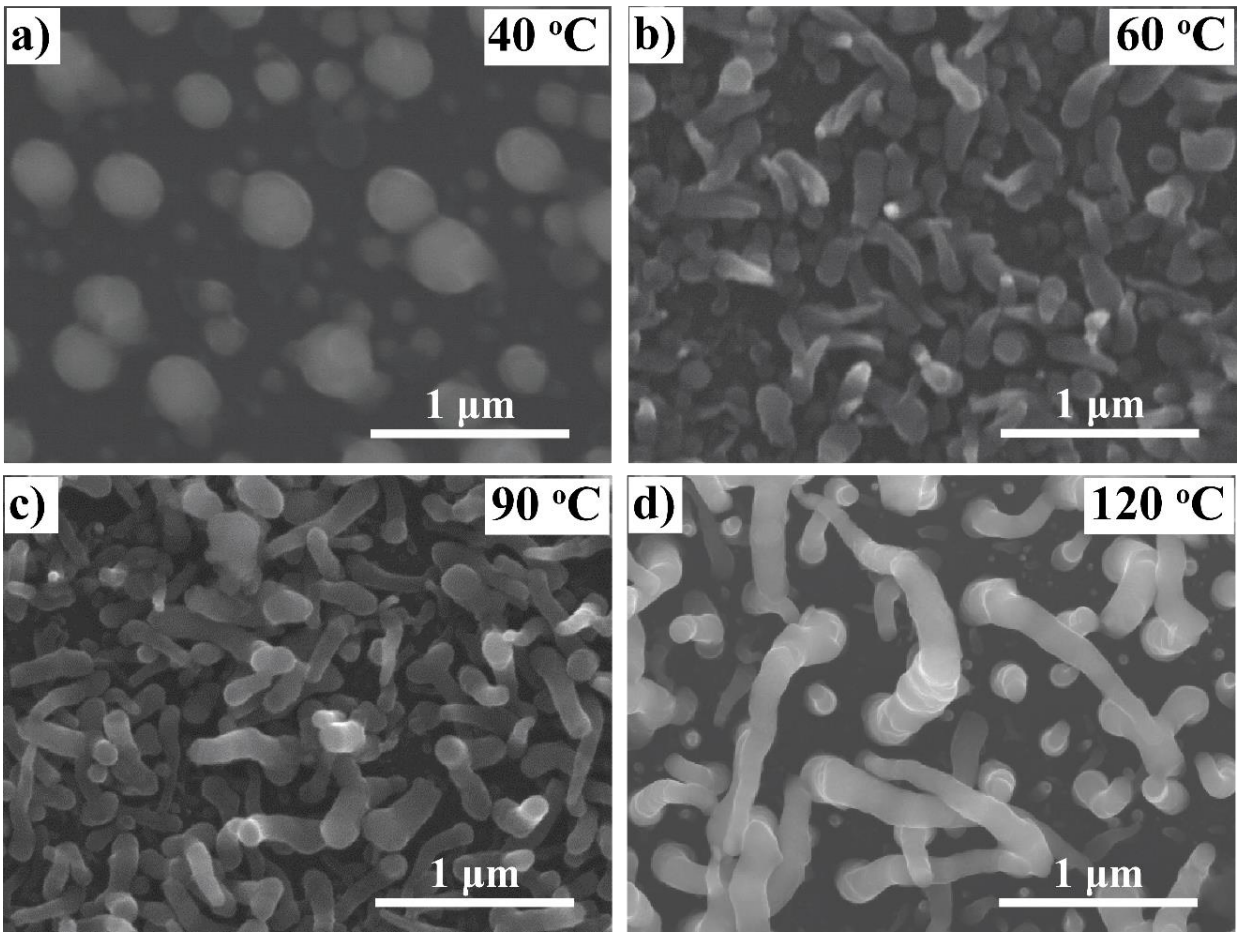

Figure 3.6. (a-d) Scanning electron micrographs of Ga coated n^+-Si(100) substrate after Si electrodeposition at (a) 120 °C, (b) 90 °C, (c) 60 °C and (d) 40 °C through ec-LLS process.

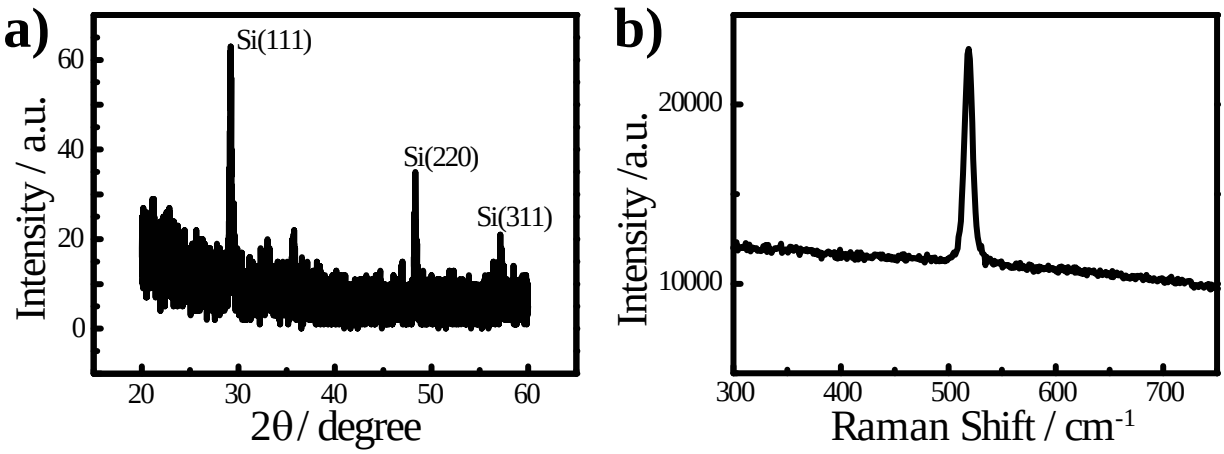

Figure 3.7. a) Powder X-ray diffractogram and (b) Raman spectrum of Si nanowires prepared by ec-LLS at T = 90 °C in propylene carbonate containing 0.2 M TBACl and 0.5 M $SiCl_4$ with an applied cathodic current of 0.32 mA cm^{-2}.

This signature had a linewidth of 9.5 cm^{-1}, notably wider than the linewidth of 3.5 cm^{-1} for bulk single-crystalline Si.[16]

Both high-resolution transmission electron micrographs and electron diffraction patterns were consistent with nanowires that were crystalline throughout. Figure 3.8 shows a section of a Si nanowire that had been removed by sonication from the deposition electrode then cast onto a Cu grid for imaging. Figure 3.8b presents a high-resolution image of the highlighted region on the nanowire in Figure 3.8a. Si <111> lattice fringes were perpendicular to the side-wall of the Si nanowire. The diffraction pattern in Figure 3.8c contains a set of spots consistent with a single crystal domain of Si viewed along the [011] zone axis. Since the Si crystals were ~200 nm thick in the radial direction, normally forbidden diffraction spots were also visible (e.g. (200) crystal planes) due to multiple scattering.[17] The extra spots in the diffraction pattern implied that stacking faults were present in this particular nanowire, which is also observable in the high-resolution image (Figure 3.8b).[18] The measured lattice constant for the Si(111) plane was 0.31 nm, commensurate with (111) lattice spacing of pure Si (0.313 nm).[19]

Additional experiments were performed to explore factors that affect the tapering of the Si nanowires prepared by ec-LLS. Specifically, the wetting of crystalline semiconductor nanowires by their liquid metal caps is well known to affect tapering by metal incorporation.[20-21] An earlier report by our group demonstrated that *e*GaIn droplets wet Ge less completely than Ga droplets, resulting in much less tapered Ge microwires.[22] Accordingly, Figure 3.9a shows a scanning electron micrograph of an individual Si nanowire prepared in the same fashion as those shown in Figure 3.3c, except that an *e*GaIn nanodroplet was used instead of a Ga nanodroplet. With this variation, a similar level of tapering (cone angle = 2° ± 1°, $N = 9$) was still observed, in contrast to our earlier observations with *e*GaIn in Ge microwire ec-LLS.[22] However, a separate factor that eliminated most of the nanowire tapering was identified. Figure 3.9b presents data from separate experiments that included a thin, discontinuous silica coatings on the substrate and *e*GaIn nanodroplets. In these experiments, a thin (~100 nm), discontinuous silica was cast on the liquid *e*GaIn nanodroplets and substrates through application of a spin-on-glass prior to attempting ec-LLS. The intent was to perturb mechanically the liquid metal wetting by the introduction of the silica layer prior to attempting ec-LLS (Figure 3.9c,d). Individual control experiments that did not include SOG but that included either identical extra drying time in air, the plasma cleaning step, or exposure to ethanol (without diluted SOG solution) never yielded any samples with nanowires

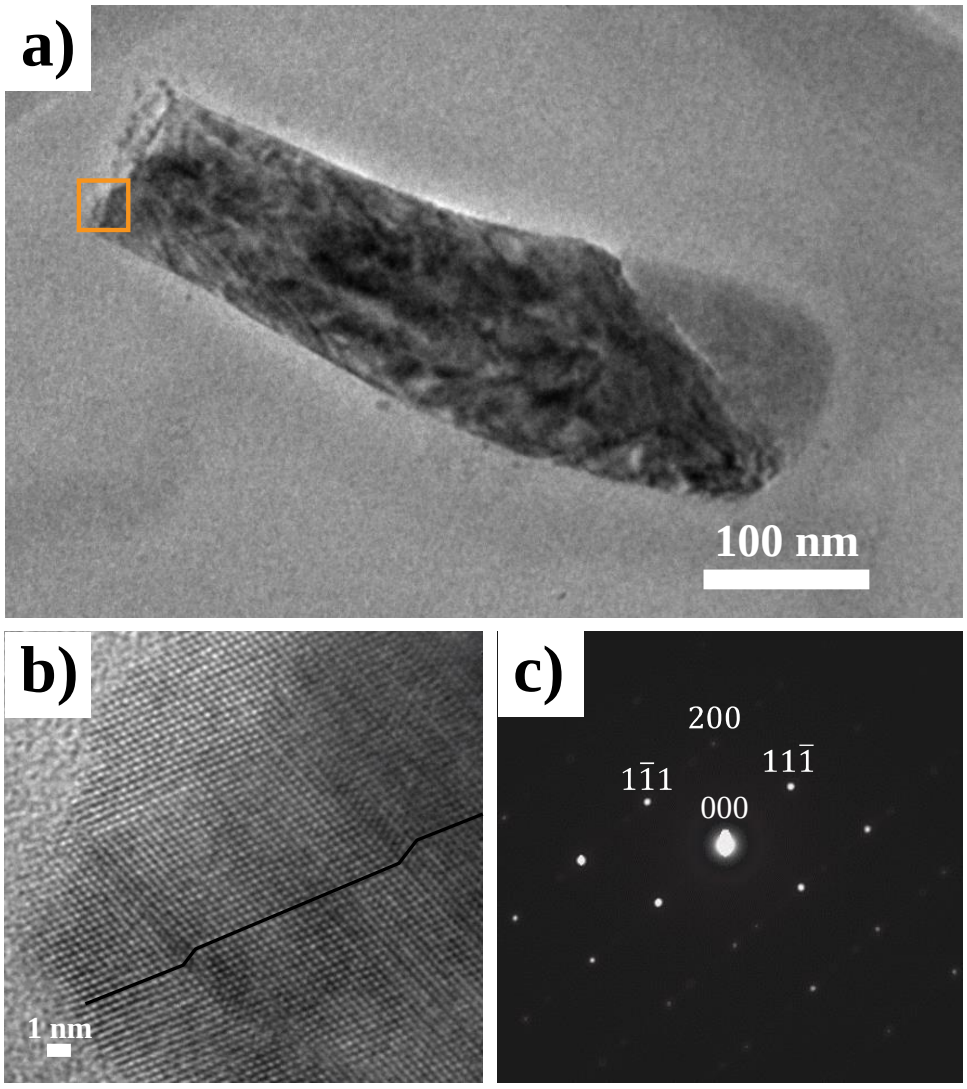

Figure 3.8. a) Low magnification transmission electron micrograph of a Si nanowire prepared after ec-LLS at T = 90 °C in propylene carbonate containing 0.2 M TBACl and 0.5 M $SiCl_4$ with an applied cathodic current of 0.32 mA cm^{-2}. (b) High magnification transmission electron micrograph of the regions indicated in (a). The two stacking faults in this image are highlighted with the thick black line. (c) Selected area electron diffraction pattern of the region shown in (b) taken along the [011] zone axis.

like those shown in Figure 3.9b. However, consistently, there were identifiable patches on substrates treated by spincasting SOG where Si nanowire electrodeposition did occur as shown in Figure 3.9b. To be clear, after silica coating, only one third of each sample's total surface area (as observed in three replicate trials) contained regions consisting of long Si nanowires. Still, at these locations, these electrodeposited Si nanowires showed less tapering and longer lengths. If residual liquid *e*GaIn nanodroplets remained on the Si nanowires, the apparent contact angle was high, i.e. the liquid metal was evident as a round nanodroplet.

D. Discussion

The data from Raman, X-ray diffraction, and electron microscopic analyses independently support the contention that Si nanowire growth by ec-LLS at liquid Ga-containing nanodroplets is possible. Further, the as-prepared Si nanowires are crystalline. Since there is no precedent for metal-catalyzed conversion of amorphous to crystalline Si[23] at the temperatures explored here, the inferred conclusion is this system is in fact a concerted electrodeposition-crystal growth process. That is, crystalline nanowires were directly produced *via* Si nanowire ec-LLS instead of a more typical electrodeposition of amorphous Si that was then crystallized through heating. The demonstration of epitaxy further supports this notion of a direct deposition of crystalline Si. The correlation between the nanodroplet size and the resultant nanowire width suggests that deterministic control over the Si nanowire morphology is possible. How the fidelity of Si nanowire ec-LLS compares to the control possible in other methods that also employ liquid metal droplets to catalyze the formation of Si nanowires (e.g. vapor-liquid-solid[6] and solution-liquid-solid[24] growths) is not clear at this juncture.

The ability to deposit crystalline Si nanowires at nearly ambient conditions (i.e. low temperature and atmospheric pressure) is advantageous. The independence from pressure/vacuum equipment greatly simplifies the design for a scaled up reactor. Further, the low temperatures mean nearly every conceivable conductive substrate type (e.g. metal, oxide, plastic) and low-cost reactor material are potentially compatible with Si nanowire ec-LLS. In these respects, and in conjunction with the fact that all the deposited nanowires are in intimate contact with a current collector, Si nanowire ec-LLS therefore seems uniquely suited for various device fabrications.

Still, this embodiment of Si nanowire ec-LLS does not represent an optimized process. First, the electrolyte was corrosive towards Ga. The hydrolysis of $SiCl_4$ with trace amount of H_2O[25]

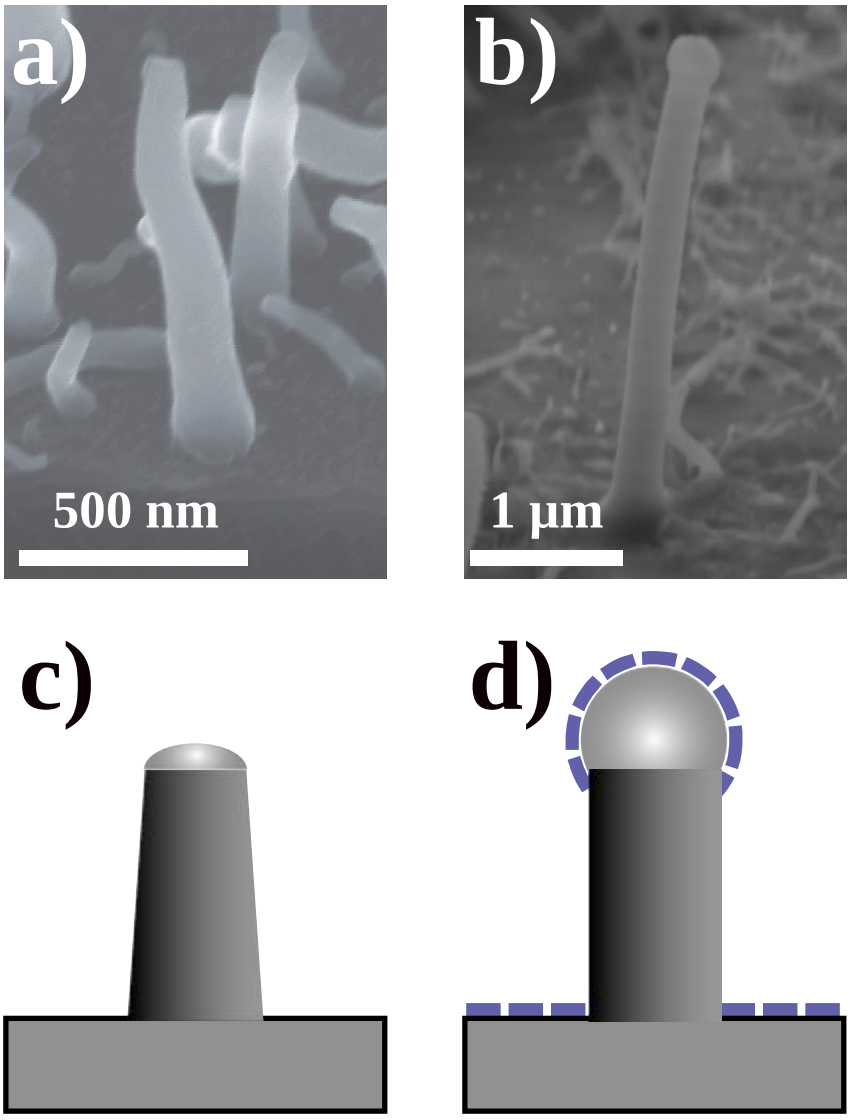

Figure 3.9. Scanning electron micrograph of an individual Si nanowire prepared by ec-LLS as in Figure 3 with (a) a film of uncoated *e*GaIn nanodroplets supported on a clean n^+-Si(100) substrate and with (b) a film of *e*GaIn nanodroplets coated by a thin spin-cast silica shell. c) Schematic depiction of a Si nanowire prepared by ec-LLS with a clean Ga nanodroplet initially resting on a clean substrate. d) Schematic depiction of a Si nanowire prepared by ec-LLS with a Ga nanodroplet and substrate coated by a thin, discontinuous silica layer.

caused etching of the liquid metal. In the absence of a negative applied bias at elevated temperatures, the Ga nanodroplets were not indefinitely stable in this electrolyte (Figures 3.10), dissolving and/or detaching from the underlying Si surface. This aspect limited the total time ec-LLS could be performed. Second, the liquid metal identity was not ideal for Si crystal growth. Although Si is soluble in liquid Ga, both the solubility is low[26] and the wetting properties of Ga/Si and *e*GaIn/Si apparently do not favor non-tapered nanowires, i.e. rigorously pure Si. With regards to the former point, there are potentially other low melting point metal alloys that have higher solubilities for Si. Such liquid metals should allow higher concentrations of Si before nucleation and crystal growth start, allowing the sustained growth of Si crystals at lower supersaturation levels.[27] The development of such liquid metals could improve the crystalline quality and is the focus of separate ongoing studies.

With regards to wetting, we have previously observed that liquid metal droplets can lose volume over time during nanowire ec-LLS because they wet the growing inorganic crystal too strongly.[11-12] The loss of liquid metal occurs because some amount is left at the crystal growth front between the Si crystal and liquid metal. As a result, not only is metal trapped within the growing Si crystal, the volume of the Ga droplet decreases continually as the nanowire grows longer. This particular aspect is not intrinsic to ec-LLS, as metal incorporation has been observed in other nanowire growth methods involving Group III liquid metals.[28] The red shift of the Raman phonon mode (relative to peak position measured for a Si single crystalline wafer) and the line width in the diffractograms are consistent with strain introduced by a non-zero concentration of Ga in the electrodeposited Si nanowires. Changing the composition of either the liquid metal or the electrolyte or both could help mitigate this issue. However, in the absence of detailed metallurgical data that would help predict what type(s) of liquid metal have favorable physicochemical, electrochemical, and wetting properties favorable to Si ec-LLS, identifying an optimal liquid metal is daunting. Nevertheless, the finding here that additional additives to the ec-LLS system can also affect wetting by the liquid metal (and thereby tapering of the resultant nanowire) is an important advancement. We recognize that the crude spin cast silica layers shown here are problematic and not refined. Further, although plasma etching was performed, the presence of residual organic matter could further complicate the nature of the interface. Still, with our spin cast silica layers, there were either macroscopic areas on the substrate where no Si electrodeposition occurred, implying a thickness that blocked all heterogeneous charge transfer,

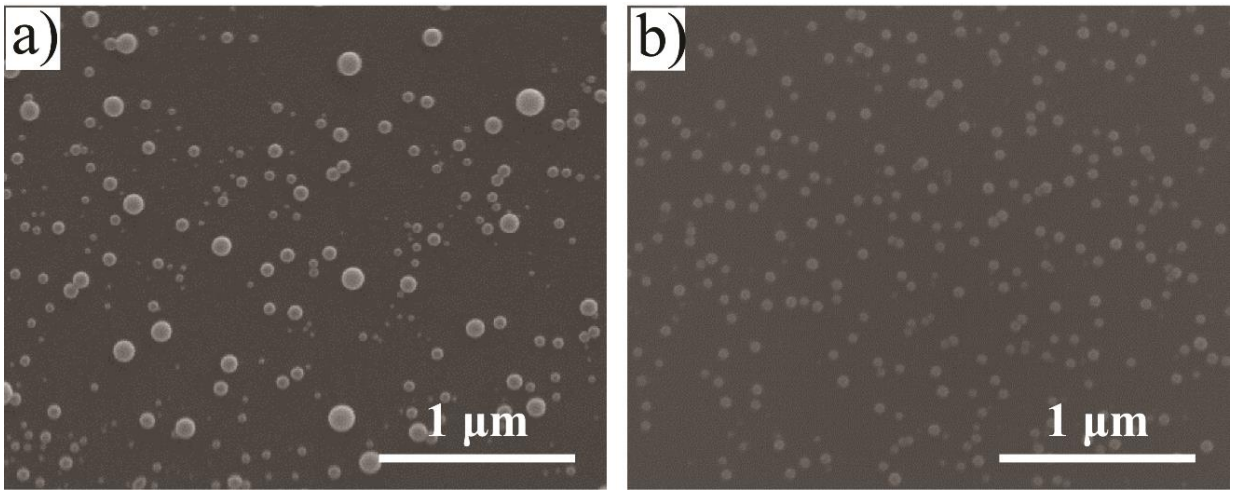

Figure 3.10. Ga nanoparticles on Si substrate formed by electrodeposition (a) before and (b) after immersing in 0.5 M $SiCl_4$ electrolyte for 1 hour at 100 °C.

and where Si electrodeposition did occur and resulted in normally tapered nanowires, suggesting no silica coating. Nevertheless, we do feel that the principle demonstrated by the areas featuring a thin coating is one that can be further developed. There is a plethora of different adsorbates, surfactants, and chelators that could be easily incorporated into this (and any other) ec-LLS experiment. Identifying which type of surface modifier is most effective will take additional research. Still, this concept adds a potentially powerful new dimension to exploit to advance ec-LLS as a useful synthetic method.

E. Conclusions

Crystalline Si nanowires were synthesized through an electrochemical liquid-liquid-solid deposition process utilizing supported liquid metal nanodroplets and $SiCl_4$ dissolved in propylene carbonate at temperatures as low as 60 °C. These results stand apart from all other previous Si nanowire electrodeposition reports in four important aspects: (*1*) the selective electrodeposition of Si at Ga-based nanodroplet electrodes has been identified; (*2*) the as-prepared Si nanowires were crystalline; (*3*) the Si nanowires grew with epitaxial relationship with respect to the substrate supporting the liquid metal nanodroplets; and (*4*) these cumulative properties were achieved at temperatures as low as 60 °C. This work also stands apart from vapor-liquid-solid or solution-liquid-solid processes in that an applied potential effected the necessary reducing condition and the driving force to nucleate and grow Si nanowires rather than high temperatures. Finally, this work is the first to show that agents that alter the surface properties of the liquid metal/substrate contact can strongly impact the morphology of the resultant crystals produced by ec-LLS. Although not exploited in this work, the results shown here suggest a direct pathway to the facile preparation of devices requiring electrically contacted Si nanowires.

F. References

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CHAPTER 4

High-Performance Polycrystalline Ge Microwire Film Anodes for Li Ion Batteries

A. Introduction

Si or Ge material with high aspect ratio form factors (i.e. wires, tubes) are mechanically resilient towards the insertion of Li^+ relative to their bulk analogs and are thus attractive for rechargeable Li^+ batteries.[1-2] However, thin nanowire electrodes suffer low coulombic efficiency and significant capacity loss in the first few cycles due to their large susceptibility to solid-electrolyte interface (SEI) layer formation. Conversely, Ge and Si microwires are less adversely affected by SEI formation since they have smaller surface to volume ratios,[3-4] but are more vulnerable to pulverization and thus typically demonstrate shorter cycle-life.[5] To date, the primary emphasis in the field has been focusing on thin nanowire/nanotube structures to address the SEI issue.[6]

An alternative approach to the realization of high capacity, high stability Li^+ battery anodes is to mitigate the stress issues from Li^+ insertion in larger microwires. A microwire electrode material with the capacity to accommodate the material damage incurred during lithiation would be less prone to issues related to SEI. In this regard, polymer coatings with 'self-healing' capabilities have been previously described to enhance mechanical stability of Si microparticle anodes, but only as a composite with carbon black to improve the electrode conductivity.[7] This chapter describes an alternative strategy for synthesis and design of battery electrodes based on liquid metals in microcrystalline Group IV materials. Liquid metals like gallium (Ga) do not impart high Li^+ insertion capacity (e.g. 769 mA h g^{-1} for liquid Ga)[8-9] but its incorporation in Group IV materials may still be beneficial. Here we demonstrate this concept with Ge microwires synthesized through an electrochemical liquid-liquid-solid (ec-LLS) process. Akin to vapor-liquid-solid nanowire growth,[10] ec-LLS uses liquid metals to catalyze the formation of crystalline semiconductors (Figure 4.1). The key distinction is that an electrochemical potential/current is

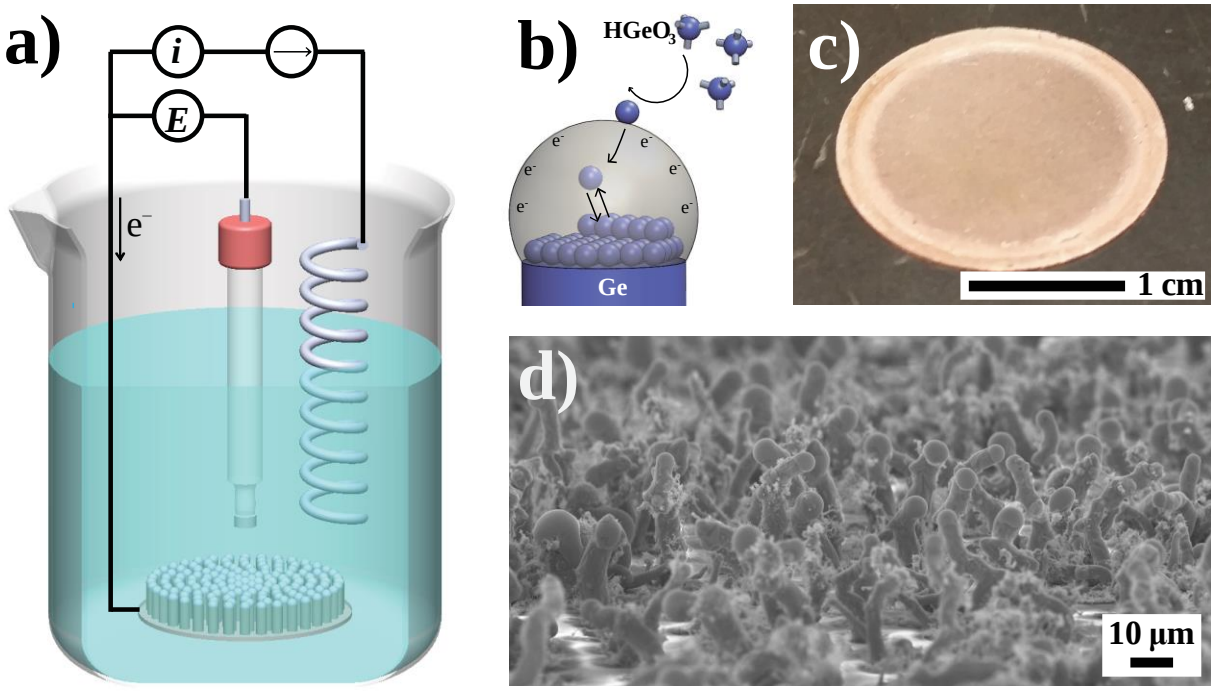

Figure 4.1. a) Schematic depiction of Ge microwire ec-LLS on Cu current collector in an aqueous solution using a three-electrode setup. (b) A microscopic illustration of the elementary steps in the Ge microwire ec-LLS process (not drawn to scale). (c) Optical photograph of a film of ec-LLS grown Ge microwires on Cu substrate, which is used as is in Li-ion battery coin cells. (d) Scanning electron micrograph of Cu foil patterned with SU-8 after Ge microwire ec-LLS at T = 80 °C for 4 hours.

applied that initiates and sustains crystal growth.[11] For the context of battery electrodes, ec-LLS is particularly advantageous because each crystalline material that forms is necessarily in direct electrical contact with a conductive substrate. In earlier work, we only showed that high-aspect-ratio Ge nanomaterials could be prepared with indium (In) nanoparticles and those materials exhibited high initial activity as Li^+ battery anodes.[12] In this work, we report that polycrystalline Ge microwires prepared by ec-LLS with Ga-based liquid metal droplets produced unique materials show both high initial and prolonged capacities for Li^+ insertion/removal. Results from electron microscopy, atom probe tomography, and X-ray diffraction analyses are presented that implicate the importance of residual Ga in the Ge microwires.

B. Methods

Materials & Chemicals Acetone (ACS grade, BDH), methanol (ACS grade, BDH), 2-propanol (ACS grade, BDH), Ga(l) (99.99%, Rotometals), In(s) (99.99%, GalliumSource), GeO_2 (99.999%, Alfa Aesar), $Na_2B_4O_7 \cdot 10H_2O$ (99 - 100%, Mallinckrodt®), copper foil sheets (127 mm x 500 mm x 0.51 mm, 99.9%, GalliumSource), 3-(Trimethoxysilyl)propylmethacrylate (MPTS, 98%, Sigma-Aldrich), SU8 2007 (Microchem Corp.), lithium foil (99.9%, Alfa Aesar), lithium hexafluorophosphate (99%), ethylene carbonate (anhydrous, 99%, Sigma-Aldrich), and dimethyl carbonate (anhydrous, ≥99%, Sigma-Aldrich) were used as received. Water was purified from a Barnstead Nanopure III purification system (>18 MG cm) and was used throughout.

Preparation of Patterned Copper Supports Photoresist films with evenly sized and spaced microwells of diameter 9.6 ± 0.6 μm were patterned on a Cu substrate using optical photolithography with a custom photomask (Fineline Imaging, Colorado Spring, CO). Copper foil sections were cut into 19 mm x 19 mm sections. These sections were degreased in acetone and methanol for 10 minutes each in an ultrasonic cleaner (Branson 2510, output 100W). The photolithography process was carried out in a clean room. Prior to spin casting SU-8, MPTS was spin-coated (3000 rpm for 30 s) to act as an adhesion promoter. Following, SU-8 2007 was spin-coated over the substrate and soft baked at 95 °C for 3 minutes. UV light exposure (OAI) for 20 s at 26 W cm^{-2}. Samples were then subject to a post-exposure bake at 95 °C for 5 minutes. Development for 4 minutes under agitation with SU-8 developer removed the unexposed regions of the photoresist. The substrates were then rinsed vigorously with 2-propanol and dried under N_2

(g). The mass of substrate with photoresist was measured using Sartorius ME36S microbalance (0.001 mg readability) as M_{sub}.

Preparation of eGaIn Microdroplets Coated Cu Gallium-Indium eutectic (*e*GaIn, 75 wt.% Ga, 25 wt.% In) was prepared by adding In pellets to Ga and physically mixing at room temperature. The mixture was then heated to 100 °C for 30 minutes to form a homogeneous alloy. To fill the patterned microwells on the foil with *e*GaIn, samples were fixed on a home-made vacuum chuck while ~1 mL of the heated liquid metal was dispensed on the surface of the hole array pattern. A lint-free towel (Kimtech W4, Fisher) was used to compress the liquid metal against the substrate and force it to wet the interior of each hole. The towel was continually rubbed across the template in all directions until all holes were filled. Excess liquid metal was removed by a doctor blade. The surface was wiped clean by using a methanol soaked lint-free towel.

Ge ec-LLS After filling the microwell arrays with *e*GaIn, the substrates were used as working electrodes in a custom single-chamber PTFE compression cell featuring a 1.3 cm^2 opening that defined the exposed electrode area. Electrical connection to each working electrode was made by contacting the stainless steel electrode support. 5 mL of aqueous electrolyte containing 50 mM GeO_2 and 10 mM $Na_2B_4O_7$ were added to the PTFE cell. A standard three-electrode configuration with a graphite counter electrode and a Ag/AgCl (sat. KCl) reference electrode was employed. A Metrohm Autolab PGSTAT302N was employed for all ec-LLS depositions. Ge ec-LLS was conducted galvanostatically at +0.5 mA/cm^2 in a temperature-controlled propylene glycol/water bath (BuchiWaterbath, B-481) held at 80 °C. Ge microwires with 15 µm and 30 µm heights were grown for 4 hours and 8 hours respectively. The long times were necessary to account for the low faradaic efficiency (6-10 %) of the ec-LLS process, as evolution of H_2 was significant at the copper/electrolyte interface. After deposition, as-prepared Ge microwire films were removed from the PTFE cell and then briefly soaked in 1.0 M HCl solution to etch the liquid metal droplet affixed at the top. The mass of the as-prepared Ge microwire film on Cu substrate was then measured with a Sartorius ME36S microbalance (0.001 mg readability) as M_{sub+Ge}. The net weight of Ge microwire film was calculated as (M_{sub+Ge} - M_{sub}). The Ge microwire film anodes had a loading density of approximately 1 mg cm^{-2}.

To eliminate the residual metal content in the Ge microwires, as-prepared Ge microwire film were heated at T = 250 °C for 30 minutes, put back into the PTFE cell, and then anodically

etched at a constant potential of -0.1 V vs *E*(Ag/AgCl, sat KCl) in 1.0M HCl for 30 minutes. This protocol did not cause any perceptible mass loss in the Cu foil substrates in control trials.

Li^+ Insertion/Removal Cycling Tests Coin cells were assembled in an Ar atmosphere glove box (O_2 < 0.4 ppm, H_2O < 0.1 ppm, Vacuum Atmosphere OmniLab). Each anode was placed in a 2032-type coin cell with a Li foil counter electrode and a glass microfiber separator (Whatman® glass microfiber filters, Grade GF/D). The separator was soaked in 1 M $LiPF_6$ dissolved in 1:1 (v/v) ethylene carbonate and dimethyl carbonate electrolyte before use. Galvanostatic charge-discharge experiments were performed on a Neware BTS-5V1MA cycler.

Materials Characterization Scanning electron microscopy imaging was conducted in a JEOL-7800FLV microscope with a field emission gun. Image analysis was carried out using ImageJ with electron micrographs taken with > 1000x magnification. Powder X-ray diffraction patterns were collected on a PANalytical Empyrean Alpha-1 diffractometer and parallel beam optics using Cu-Kα radiation (λ = 1.542 Å). The X-ray diffraction patterns were generated using scan step size of 0.002°. The positions of Ge (111), (220) and (311) diffraction peaks were analyzed using Jade 9 program. Cu-Kα2 background subtraction was performed to increase the accuracy of the simulation of diffraction peaks resulted from Cu-Kα1 beam diffraction. Cu (200) diffraction peaks from the Cu substrate were used to calibrate the 2θ positions of Ge diffraction peaks. Lattice constants of Ge were generated and refined using Jade 9 build-in functions.

Thin disks of Ge microwires were prepared using focused ion beam (FIB) milling and were characterized by transmission electron microscopy. FIB milling was performed in FEI NOVA NanolabDualbeam and FEI Helios Nanolab 650 Dualbeam workstations. Both systems were equipped with Schottky field emitters and Ga focused ion beams. For lift-out, Ge microwires were first sonicated in ~100 µL methanol for 30 s and re-dispersed on a n^+-Si wafer so the microwires were oriented on their sides. In the SEM/FIB workstation, an OmniprobeAutoProbe 200 micromanipulator equipped with a standard tungsten (W) probe tip (Ted Pella) was used to approach and contact single microwires on the substrate. A temporary Pt weld was made between the microwire and the W probe *via* electron beam assisted chemical vapor deposition (EBA-CVD) with a $C_5H_4CH_3Pt(CH_3)_3$ gas injection system. The single microwire was then lift-out using the micromanipulator and welded onto a post on TEM grids (PELCO® FIB Lift-Out TEM Grids, copper). The microwire was milled sufficiently thin to render it transparent for TEM (< 500 nm thick). Scanning transmission electron microscopy imaging was performed in a JEOL 2010F

analytical electron microscope equipped with a zirconated tungsten (100) thermal field emission tip. Selected area electron diffraction patterns were collected under normal transmission electron microscopy mode on the same instrument.

Atom probe tomography (APT) samples were prepared using Ge microwires dispersed on a n^+-Si wafer *via* an established method.[13] 2 µm of Pt layer was first deposited over an area (15 µm x 3 µm) on a Ge microwire by ion beam assisted chemical vapor deposition (IBA-CVD) with a $C_5H_4CH_3Pt(CH_3)_3$ gas injection system. Two mill cuts were executed sequentially using FIB along the long sides of the Pt coating on the Ge microwire to form a wedge shape Ge. The first single release cut was carried out on one side of the Ge wedge using FIB, and W probe was inserted and attached to release the end using IBA-CVD. The second release cut was done subsequently on the other end of the Ge wedge. The Ge wedge was lifted out and a slice of it was mounted on a LEAP microtip (Presharpened Microtip™ Coupon). The mounted slice was sharpened by 30 kV FIB first and final cleaning was done using 5 kV FIB. Laser-assisted APT was performed in Cameca LEAP 4000X HR Atom Probe using 355 nm laser excitation at a pulse frequency of 125 kHz and specimen temperature of 50 K. 20.0 million ions were collected by the detector for elemental analysis and reconstruction.

C. Results

Ge microwire films were prepared through a modified ec-LLS process. Figures 4.1a and 4.1b depict the three-electrode electrochemical cell and the basic premise of the ec-LLS growth of Ge microwire films performed in this work. Notably, we employed a patterned copper (Cu) foil substrate here. The miscibility of Ga, In and Cu[14] resulted in uncertainty in the precise liquid metal composition in the ec-LLS process, particularly at longer times where Ga and In more fully dissolve into Cu. Accordingly, all depositions were performed with substrates immediately after decoration by *e*GaIn droplets and the effective liquid metal composition during deposition was most likely an alloy of Ga-In with a minor fraction of Cu rather than pure *e*GaIn. Figure 4.1c shows an optical image of the resultant Ge microwire film on the Cu disk. Figure 4.1d shows a representative scanning electron micrograph of the as-prepared Ge microwire films.

In addition to the as-prepared materials, a method was developed to lower the residual metal content in the Ge produced by this ec-LLS method. Specifically, a brief thermal annealing at T = 250 °C for 30 min was employed to facilitate metal diffusion out of the Ge crystals. Then,

wet electrochemical etching was used to remove selectively metal without perturbing crystalline Ge. X-ray diffraction patterns of as-prepared Ge microwires, annealed Ge microwires, and annealed/etched Ge microwires are shown in Figure 4.2a. All three sets of data indicate these Ge materials were both fully crystalline (no broad signal at the low 2θ values that could suggest a significant amorphous content was observed) and the materials were polycrystalline without any obvious preferential orientation, i.e. the (111), (220), and (311) peaks showed the pattern of relative intensities expected for randomly oriented Ge crystal grains.[15]

Atom probe tomography was performed to assess the metal content in both the as-prepared Ge microwires and the annealed/etched Ge microwires.[16] Figure 4.2b shows results from atom probe tomography analysis of a section of a representative as-prepared Ge microwire that was lifted out using focused-ion beam (FIB) milling and then platinum-welded onto a Si post. Figure 4.2b is a three dimensional map of the atom distribution in the sectioned slab. Figure 4.2c is a cross-sectional plot of the atom concentrations of Ge, Ga, In, and Cu along one (z) axis. Three features in the atom probe data were notable. First, Ga, In, and Cu were all detectable in the as-prepared Ge microwires. Second, Ga was the dominant species, with In and Cu at concentrations $< 10^{-1}$ at %. Third, the tomographic data suggest the metals were uniformly dispersed in the electrodeposited Ge. On average, these Ge crystals had 8.1 ± 0.5 at.% Ga dispersed uniformly throughout. This loading far surpassed the equilibrium solubility of Ga in solid Ge at room temperature[17] and was consistent with 'colossal' residual metal loadings in crystal growths performed with metals that bind tightly with crystalline Group IV elements like crystalline Si growth in Al.[18] As seen in Figures 4.2d and 4.2e, the mild annealing/etching methodology decreased the overall metal contents, lowering In and Cu below the detection limit and dropping Ga to 3.3 ± 0.7 at.%. Notably, the remaining Ga was apparently concentrated in select regions and was no longer uniformly distributed.

Figure 4.3 compares the structural effects induced by Li^+ insertion in as-prepared and annealed/etched Ge microwires through scanning electron microscopy. Figures 4.3a and 4.3c show before and Figures 4.3b and 4.3d illustrate the respective materials after one galvanostatic cycle in 1 M $LiPF_6$ electrolyte at a rate of 0.1C. Comparison of Figures 4.3a and 4.3c illustrate that the annealing/etching treatment did not induce drastic changes in the microwire form factor and only introduced sporadic pits (where presumably Ga was etched out). However, comparison of Figures 4.3b and 4.3d show that after Li^+ insertion and removal the extent of irreversible volumetric

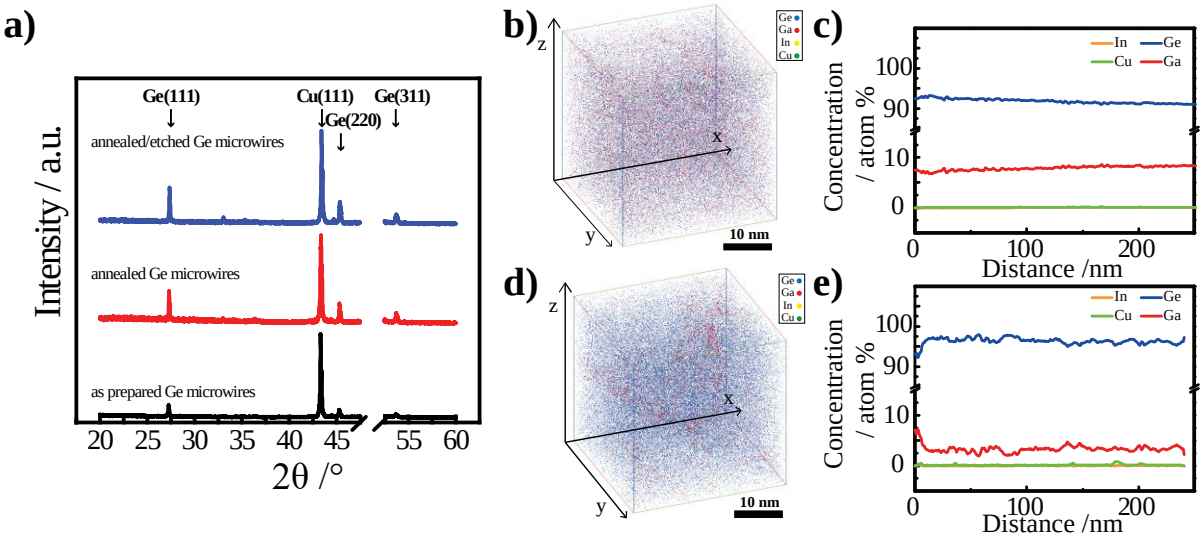

Figure 4.2. a) Powder X-ray diffractograms of as prepared ec-LLS grown Ge microwires, annealed Ge microwires and annealed/etched Ge microwires. Diffraction peaks for Ge and the underlying Cu foil are noted, respectively. b-e) Atom probe tomography analysis of the distribution and concentration of Ge, Ga, In and Cu in as-prepared and annealed/etched Ge microwires. (b, d) Reconstructed 3D image of a 30 nm x 30 nm x 30 nm volume within an as-prepared and annealed/etched ec-LLS-grown Ge microwire, respectively. (c, e) Line profile of atomic concentration of Ge, Ga, In and Cu in the Ge microwires in (b) and (d), respectively, along the z axis of the samples.

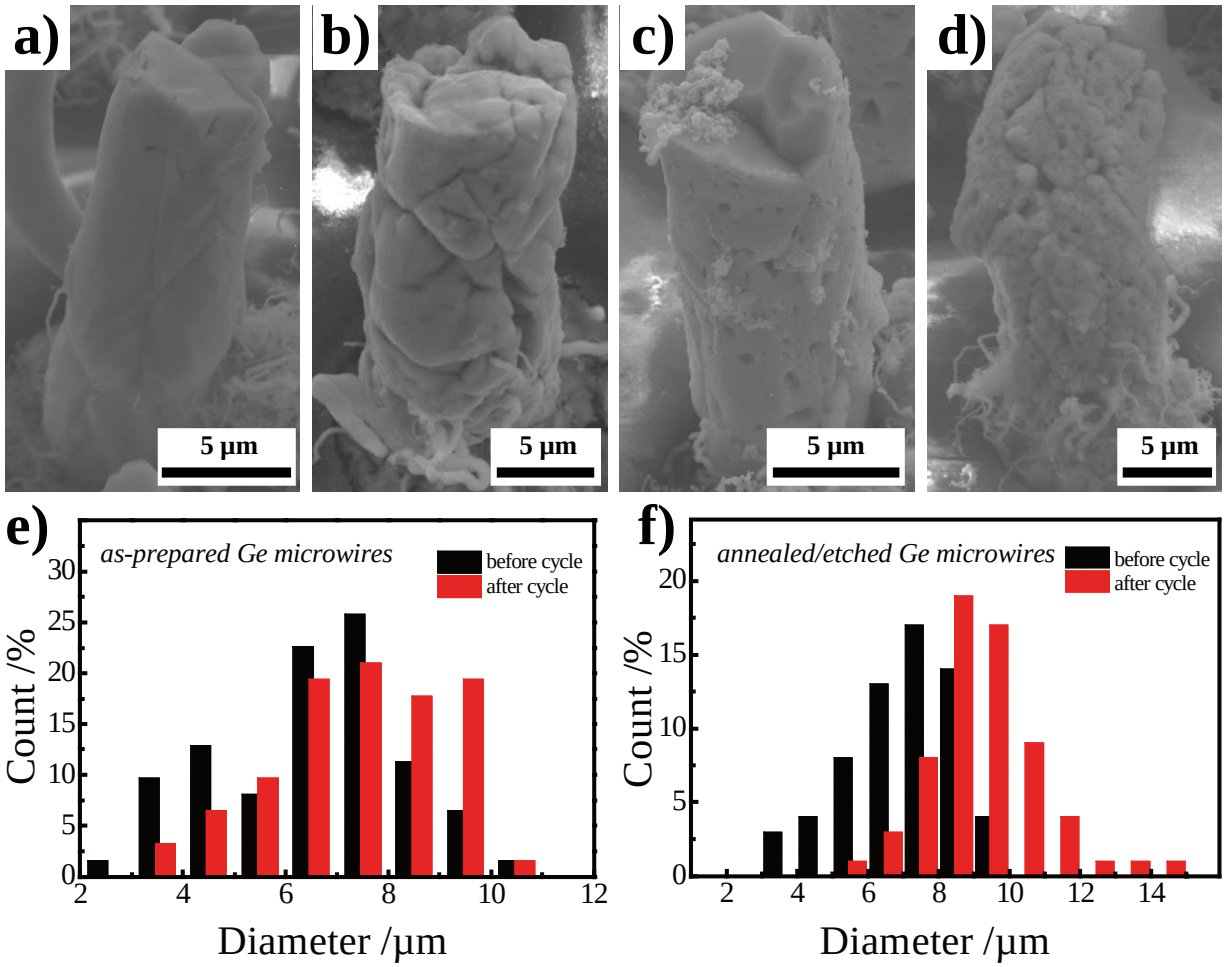

Figure 4.3. a, b) Electron micrographs of as-prepared ec-LLS grown Ge microwires before and after one galvanostatic cycle in 1 M $LiPF_6$ electrolyte at a rate of 0.1 C. (c, d) Electron micrographs of annealed/etched Ge microwires before and after one galvanostatic cycle in 1 M $LiPF_6$ electrolyte at a rate of 0.1 C. (e) Size distribution histogram of ec-LLS grown Ge microwires before and after 1^{st} cycle (f) Size distribution histogram of annealed/etched Ge microwires before and after 1^{st} cycle.

expansion was not the same in the two materials. As-prepared Ge microwires had diameters of 6 ± 2 μm before lithiation and 7 ± 2 μm after one cycle for Li^+ insertion/removal, indicating an irreversible volumetric expansion of ~ 20% (Figure 4.3e). In contrast, Ge microwires that had previously been etched to remove Ga showed diameters of 6 ± 2 μm before cycling and 9 ± 2 μm after cycling, indicating ~ 50% permanent expansion in the radial direction (Figure 4.3f).

Figure 4.4 shows the results from galvanostatic cycling in a two electrode coin cell with a Li metal foil counter electrode. All analyses were performed so that the potential of the cell was bounded between 0.01 V and 2.0 V vs $E(Li^+/Li)$. Figure 4.4a shows Li^+ insertion/removal took place between 0.4 - 0.1 V and 0.4 - 0.6 V, respectively, consistent with known cycling behavior of Ge anodes.[20] The differential capacity-potential responses for the first discharge/charge cycle of the as-prepared and annealed/etched Ge microwire films at a rate of 0.1 C are shown in Figure 4.4b. Two features are notable in the data. First, the data show that the as-prepared Ge microwires have lower overpotentials for Li^+ insertion/removal than the annealed/etched Ge microwires. Second, the as-prepared Ge microwires show small additional peaks in the cathodic sweep at +0.5 V and +0.8 V that are consistent with a small amount of Li^+ insertion occurring in Ga (see inset).[8] The long term capacity retentions for the as-prepared and annealed/etched Ge microwire films at a rate of 0.1 C are shown in Figure 4.4c. Both types of Ge microwires showed comparable capacities initially but their long term capacity retention differed significantly. As-prepared Ge microwire film electrodes lost only 10% of their initial capacity after 40 cycles while annealed/etched Ge microwires lost more than 35% of their initial capacity, in accord with the substantial capacity losses previously reported for other forms of microstructured, crystalline Ge electrodes.[5] Figure 4.4d shows the measured capacity values for the as-prepared Ge microwire film electrodes at a variety of cycling rates. At a cycling rate of 1C, a capacity of ~ 1000 mA h g^{-1} was still attained. The coulombic efficiency of the Ge microwire film anode was 92.0% for the first cycle and kept above 98% for the following cycles except when the cycle rate was 5C and 10C, where the capacities were so low that the inaccuracy in the coulombic efficiency measurements were large. Although the specific capacities were low at these fast cycling rates, the Ge microwires recovered 88% of their original 0.1 C capacity after 35 cycles at different high cycle rates (0.1 C, 0.2 C, 0.5 C, C, 2C, 5C, and 10C).

D. Discussion

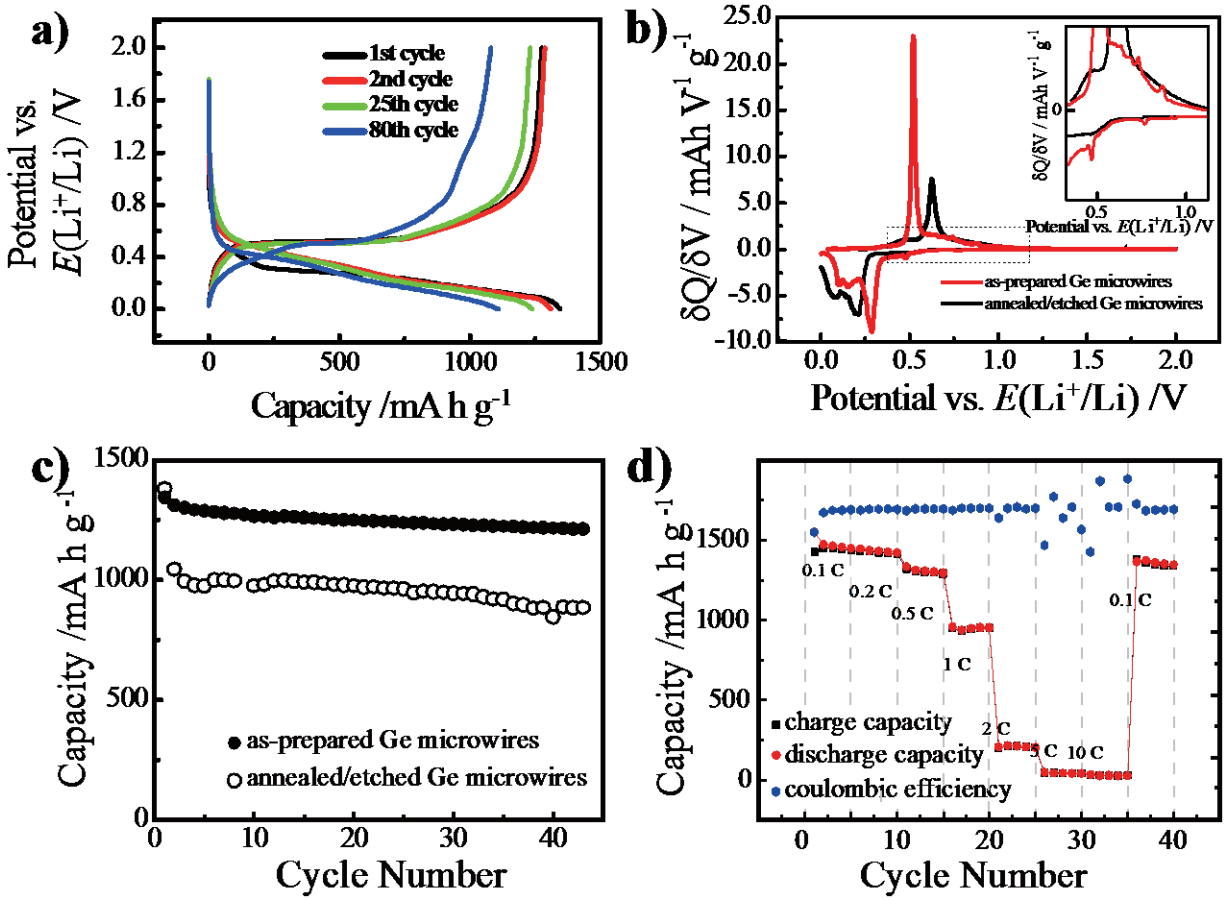

Figure 4.4. a) Selected galvanostatic discharge-charge cycles (1st, 2nd, 25th and 80th) for an as-prepared Ge microwire film electrode recorded at 0.1 C rate using Li foil as the counter electrode in 1 M $LiPF_6$ electrolyte. b) Differential capacity plot of the 1st cycle of as-prepared Ge microwires and annealed/etched Ge microwires. The electrodes were cycled at 0.1 C rate in 1 M $LiPF_6$ electrolyte. c) Galvanostatic discharge capacities of as-prepared Ge microwires (black circles) and annealed/etched Ge microwires (open circles) cycling at 0.1 C rate in 1 M $LiPF_6$ electrolyte. d) Galvanostatic charge (red circles) and discharge (black squares) capacities of as-prepared Ge microwire anode cycling at 0.1 C, 0.2 C, 0.5 C, C, 2C, 5C, 10C and 0.1 C rate in 1 M $LiPF_6$ electrolyte. The coulombic efficiencies for each charge-discharge cycle are indicated on the right y-axis (blue circles).

The cumulative results speak to three related points about ec-LLS and the preparation of anodes for rechargeable batteries. First, ec-LLS is a viable method to produce microcrystalline Ge materials directly that can serve as potent Li^+ battery anodes. Second, the polycrystalline Ge microwire film electrodes prepared by ec-LLS retain their shape (form-factor) after Li^+ insertion/removal cycling and show unusually long-lasting cycling behaviors relative to other crystalline Ge microstructure materials. Third, the specific inclusion of residual metal (Ga) in the as-prepared Ge microwires is beneficial in the context of Li^+ battery anodes as it significantly minimizes the structural damage induced by Li^+ insertion.

In general, these data speak to the power that electrodeposition specifically affords for the synthesis of structured battery materials. Specifically, electrodeposition necessarily results in active material that is wired to a current collector, as has been demonstrated recently for porous metal oxide battery cathodes.[19-20] This reports significantly expands the utility of ec-LLS for synthesis of rechargeable battery anodes made from Group IV materials.[12] Empirically, the Ge microwire film electrodes prepared here only suffered a 2.5% capacity loss from the first to second cycle, a substantial improvement over the 20% capacity loss[12] between the first and second cycles we observed previously with Ge nanowire films. More importantly, a key insight gained here is that the adhesion of even micron-sized materials on an inert current collector is still strong enough to preclude the need for a separate binder. That is, the electrodeposited Ge materials remain adhered to the Cu foil after repetitive cycling. This aspect is necessary for the realization of stable, large area battery anodes. Apparently, the intimate contact between Ge and Cu is not compromised by the strong lattice mismatch between these two materials. We surmise that the complete wetting of the (initial) *e*GaIn droplets on Cu ensures that Ge nucleates and grows directly on the metal substrate with many points of attachment. Separately, the benefit of microwires *vs* nanowires is the simultaneous mitigation of the SEI problems while increasing the total capacity since there is simply more Ge in an array of microwires than an array of nanowires that have the same pitch and height. A preliminary assessment was performed on the dependence of the cycling behavior of Ge anodes with the aspect ratio of microwires. Ge microwire anodes with smaller aspect ratios demonstrated noticeably better capacity retention over 25 cycles. (Figure 4.5) In this work, the packing density of the Ge microwires was not varied but could be increased simply by changing the pitch of the microwell pattern. Further, if absolute homogeneity of the microwires is not important, there are much simpler methods to produce more dense films of liquid metal droplets

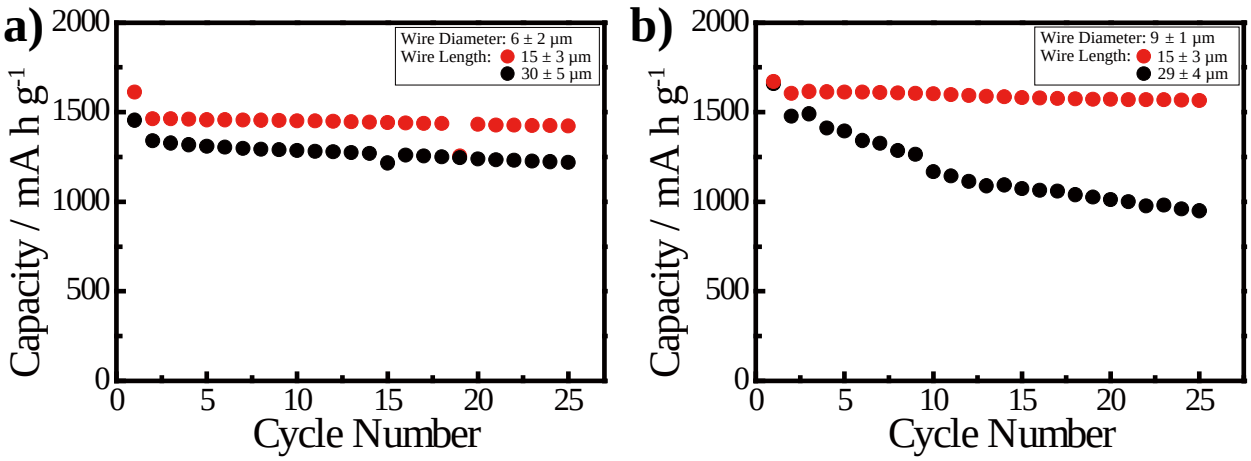

Figure 4.5. Ge anode capacity retention as a function of Ge microwire dimensions cycled at C/10 rate. (a) Discharge capacities of Ge microwires grown on 7.7 ± 0.5 µm Su-8 pattern. (b) Discharge capacities of Ge microwires grown on 11.5 ± 0.3 µm Su-8 pattern.

(e.g. pulse electroplating,[21] solution casting of droplet suspensions[22]). The results here serve as a reference point for future studies directed along these lines.

The long-lived cycling behaviors of the Ge microwire film electrodes presented in this work is unusual in the context of the available literature on microstructured crystalline Ge Li^+ battery anodes. Several reports have shown that crystalline Ge structures with features sizes comparable to the materials presented here quickly fail upon just a few cycles for Li^+ insertion/removal, particularly at cycling rates $\geq$ 0.2 C.[5] Specifically, microscopic analysis on Ge microwires with a nominal 1 μm diameter showed that stress dissipation occurred along the <110> direction and always results in substantial fracturing.[4] The origin of this critical mechanical failure is that when the hoop stress[4] is larger than the mechanical integrity of lithiated Ge, a large (micron-sized) fracture will form along the weakest crystallographic direction. The presumption has been that this is true of all crystalline Ge materials with a critical length scale greater than 1.2 μm.[4] The results presented here contrast that rationale. That is, the crystalline Ge microwires with lengths and diameters well in excess of 1 μm in this work did not suffer catastrophic mechanical failure and were able to be cycled up to 1C while still retaining useful capacities. Apparently, the distinguishing feature in the materials shown here is their *polycrystallinity*. The cumulative X-ray diffraction and electron microscopy data all indicate these Ge microwires are definitively not single-crystalline, unlike other materials produced by ec-LLS.[23] That is, unlike vapor phase methods to grow Group IV microwires,[10] the materials produced by ec-LLS on copper foils seem to avoid deleterious fracturing because the stress from volumetric expansion is not directed in a single direction throughout the entire microwire volume. This aspect is explicitly visualized directly in cross-sectional STEM data of an as-prepared Ge microwire that had been subject to 1 cycle of Li^+ insertion/removal (Supporting Information, Figure S2, Figure 4.6). The strong contrast between that fracture pattern and what is known for fractures in single-crystalline Ge microwires[4] are clear evidence the fracture stress occurs in several directions as opposed to being concentrated along one fault line and the fractures are <500 nm wide.

The most profound and unique finding in this work is that the inclusion of Ga in these polycrystalline Ge microwires is particularly beneficial. The experiments contrasting the performance of the as-prepared Ge microwire films with a comparatively high, homogeneous loading of Ga and the mildly annealed/etched Ge microwire films with a substantially lowered, heterogeneous loading of Ga demonstrated superior capacity retention and higher overall

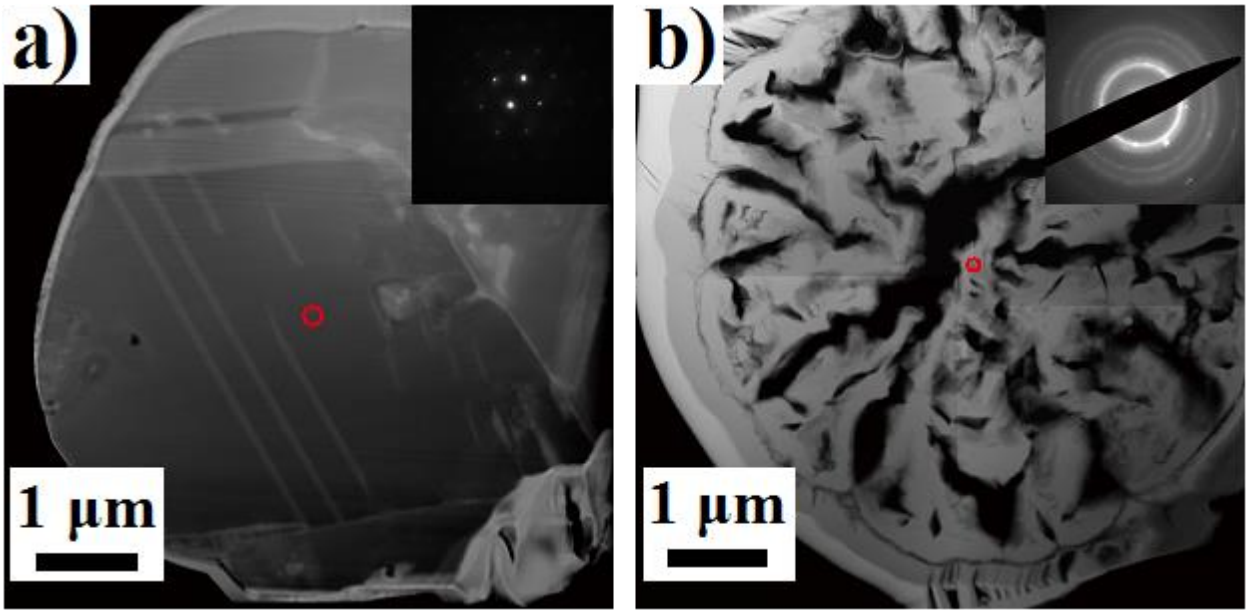

Figure 4.6. (a, b) Scanning transmission electron micrographs of Ge cross-sectional slices of as-prepared Ge microwires before and after cycling for Li^+ insertion/removal at 0.1 C in 1 M $LiPF_6$ electrolyte. Inset: Selected area electron diffraction patterns of areas indicated by red circles.

capacities when Ga was present and uniform. The presented results argue against the possibility that the annealing & etching steps to remove the residual Ga from the Ge microwires caused some catastrophic damage to the material prior to cycling for Li^+ insertion/removal. The collected X-ray diffraction patterns indicated no obvious loss/increase in crystallinity or selective etching of the Ge. The overall morphology of the microwires was nominally the same as the as-prepared Ge microwires. Further, the Ge microwires with the lowered residual Ga content still functioned as Li^+ battery anodes. The one perceptible physical change incurred by the Ga removal steps was the slight introduction of porosity of the Ge microwires (as seen in Figure 4), likely due to a Kirkendall effect from the faster diffusivity of Ga.[24] However, based on recent findings, increasing porosity ought to *enhance* the cycling maximum and stability in Ge microwires.[25] However, the data show clearly that even with that added improvement, the Ge microwires with lower levels of Ga showed inferior cycling behaviors as compared to the Ga-containing, as-prepared Ge microwires.

Whether the higher Ga content or more uniform distribution of Ga in the as-prepared Ge microwires was the more important aspect is unclear. However, both aspects are likely beneficial in the following contexts. The atom probe tomography data suggest that at least some of the residual Ga in as-prepared Ge microwires is located in the octahedral and tetrahedral interstitial sites of Ge lattice. Given the atomic radius of Ga is 4% larger than Ge,[26] the lattice of these as-prepared Ge microwires could be envisioned as a pre-strained material.[27-28] Pre-strained battery materials are reported to accommodate lithiation-induced stress better and fracture less extensively.[29] Therefore, the annealing/etching steps that lower the Ga content and concentrate specific areas (likely as crystal occlusions) could 'unstrain' the Ge and thereby lower its efficacy as an anode material. The Ge lattice constants calculated from the collected X-ray diffraction data were larger in the as-prepared materials (Table 4.1), consistent with the premise of some Ga site substitution that introduced strain the Ge. Separately, it is possible that non-substitutional Ga could separately act as a microscopic 'binder.' The act of inserting/removing Li^+ does not substantially alter the distribution of Ga in as-prepared Ge microwires (Supporting Information, Figure 4.7). The high affinity between Ga on Ge atoms, as indicated by the high Ga concentration (10^{21} Ga cm^{-3}) that a Ge crystal could accommodate[30] and the tendency of liquid Ga to coalesce[8] provides a possible means to heal lesser fractures formed during Li^+ insertion. Finally, during the discharge and charge processes for Li^+ cycling, both Ge and Ga should undergo Li^+ insertion/removal at similar potentials.[9, 31] The data in Figure 4.4b suggest this does occur to some extent. Accordingly,

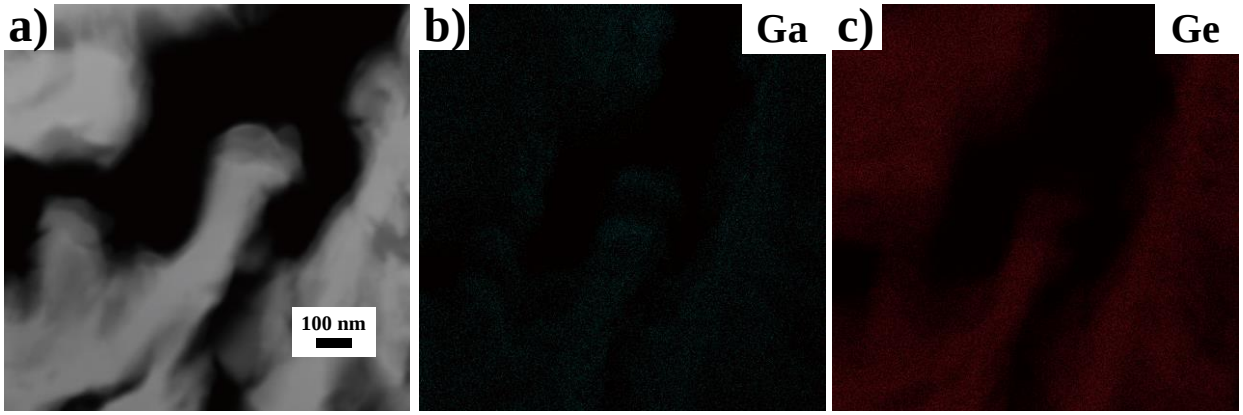

Figure 4.7. High magnification scanning tunneling electron micrographs of the sample shown in Figure S2. a) A high magnification view of one section of the material along a fracture. b, c) The corresponding elemental maps collected for Ga and Ge, respectively, in this sample.

a possibility remains that the uniform inclusion of Ga in a crystalline Ge matrix changes what lithium-containing compounds form upon reaching the most negative potentials, perhaps disfavoring the most highly lithiated forms of Ge (e.g. $Li_{22}Ge_5$) which correspond to the most extreme volume changes. The data in Figure 4.4b also indicate that only $Li_{15}Ge_4$ was produced on the initial cycle.[32] Experiments directed at more clearly identifying microscopically how residual Ga participates during Li^+ cycling are ongoing.

E. Conclusions

This work highlights the general virtues of ec-LLS for the preparation of high aspect ratio microcrystalline Ge microwire film electrodes and the unique nature of these Ge materials when prepared by ec-LLS with Ga-In-Cu alloy liquid metal droplets. When deposited directly on a Cu current collector, the resultant materials are innately high capacity Li^+ battery anodes. They can be readily incorporated into Li^+ conventional battery cells without the need for high temperature, expensive processing equipment or steps, or the incorporation of any additional binding agent. The crystalline Ge microwires produced here possess residual Ga that appears to be specifically beneficial to the operation of the Ge microwires as Li^+ battery anodes. Accordingly, this work represents a new possible direction in the design and synthesis of highly tailored rechargeable battery materials.

Table 4.1. Lattice constants and expansions of Ge microwires

	As-prepared Ge microwires	*Annealed Ge microwires*	*Annealed/etched Ge microwires*
Lattice constant (Å) [a]	5.6632	5.6590	5.6599
Lattice expansion [b]	0.30%	0.23%	0.24%

a. Lattice constants were calculated using the diffraction peak positions.

b. Lattice expansions were calculated using experimental lattice constants and standard data (5.6461 Å)[15].

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CHAPTER 5

Ec-LLS growth of Si Microwires with Different Liquid Metals

A. Introduction

This chapter investigates the experimental conditions that allow ec-LLS growth of Si microwires from microdroplets of Ga-based alloys. Si microwire ec-LLS not only completes the picture of ec-LLS Group IV semiconductor wire growth, test the limiting factors for Si crystal growth process, but also has practical significance in next generation semiconductor device applications.

Si microwires have been demonstrated to be ideal materials for solar cells[1], photoelectrochemical electrodes[2] and battery anodes[3]. For solar energy conversion applications, Si micro/nanowires demonstrate high light absorption efficiency, since it allows photon absorption along the height of the wires and carrier collection along the radial direction. Si microwires achieves higher open circuit potential comparing to Si nanowire solar cells, because the optimal radius to reduce saturation current which leads to voltage reduction, is of the order of the minority carrier diffusion length, which is always in the micrometer range.[1] Si micro/nanowires are ideal materials for Li-ion battery anodes due to their ability to accommodate volume expansion caused by lithiation. The microwire electrodes are more desired comparing to nanowire electrodes mainly because they suffer less capacity loss from Solid Electrolyte Interface (SEI) formation and achieve higher overall battery capacity.[3]

Ec-LLS growth of Si microwires illustrates the limitation in size, identity and nucleation mechanism for Si crystal growth by ec-LLS. Ec-LLS growth of Si wires relies on the heterogeneous nucleation mechanism, in which the growth species reaches supersaturation near the liquid metal/solid substrate interface and nucleates to from crystals. Accordingly, Si atoms must diffuse to the bottom of liquid metal droplet and attain a sufficient supersaturation to drive heterogeneous nucleation before homogenous nucleation elsewhere in the liquid metal takes place. At the same time, the liquid metal droplet should allow sufficient dissolution of Si within itself to provide the growth species for crystal growth.

Si microwire ec-LLS is limited by the solubility of Si in Ga at low temperatures. The solubility of Si in Ga is low (~10^{-8} at.% Si in Ga at 29.8 °C), and lower than that of Ge (~10^{-2} at.% Ge in Ga at 29.8 °C).[4] The low solubility possesses two potential problems. First, after being electrochemically reduced on the surface, Si could reach supersaturation rapidly at near-surface region in Ga for homogeneous nucleation before diffusing to the liquid droplet/solid substrate interface for heterogeneous nucleation.[5] Secondly, due to the low solubility, Si ec-LLS in Ga yields small crystal grains (< 500 nm).[6-7] The small grain sizes inhibit direct growth of single crystalline Si microwires and leads to less controlled microwire morphologies.

Experiments were done to explore the conditions for Si microwire ec-LLS from two different aspects. First, Si ec-LLS were carried out at different temperatures to study the temperature dependence of electrodeposition process. Secondly, different liquid metal droplets were used to study the dependence of Si microwire ec-LLS on liquid metal identities. By using scanning electron microscopy (SEM), energy dispersive X-ray spectroscopy (EDS) and powder X-ray diffraction (PXRD) techniques, the morphology, chemical composition and crystallinity of the as-deposited Si microwires were characterized.

Si microwires were grown *via* ec-LLS galvanostatically at 125 – 140 °C. Temperature dependence studies were performed between 100 – 140 °C, but inconsistent results appeared at elevated temperatures due to the volatility of the electrolyte. *e*GaIn were used as the liquid metal electrode to reduce Ga incorporation into Si microwires, but it did not seem to be effective. An effort to tune the solubility of Si in Ga based alloy were done using *e*GaAg alloys, but no difference in the deposits was observed from using these alloy droplets.

B. Methods

Materials and Chemicals Methanol (≥ 99.8%, ACS grade, Fisher Chemical), acetone (≥ 99.5%, ACS grade, Fisher Chemical), HF (49%, Transene Inc.), silicon(IV) chloride (99%, Alfa Aesar™), In (99.99%, GalliumSource), Ag (99.99+ %, Sigma Aldrich) and Ga (99.99%, Rotometals), Platinum mesh and wire (99.9%, Sigma Aldrich), SU-8 2007 (Microchem Corp.), S1813™ (MICROPOSIT™) were used as received. Solutions of propylene carbonate (PC) (99.5%, Acros Organics) containing tetrabutylammonium chloride (TBACl) (95%, Alfa Aesar) and tetrabutylammonium hexafluorophosphate ($TBAPF_6$) (≥99.0%, for electrochemical analysis, Sigma-Aldrich) were dried for 2 days with molecular sieves (4A, 8-12 mesh, Sigma-Aldrich)

before use. Ferrocene (98%, Sigma-Aldrich) was recrystallized in heptane before use. Degenerately doped n^+-Si wafer substrates (Crysteco, <100> As-doped, <0.007 ohm cm, 0.625 ± 0.020 mm thick; MEMC, <111> As-doped, 0.003-0.004 ohm cm, 0.510-0.540 mm thick) were cleaned and then used for photolithography. *e*GaIn were prepared by adding 25 wt. % In into Ga. *e*GaAg were prepared by adding 0.9 wt. % Ag into Ga. The alloys were then heated to 150 °C for 30 minutes to reach homogeneity. Water with a resistivity > 18.2 MΩ·cm (Barnsted Nanopure) was used throughout.

Constructing a Teflon Electrodeposition Cell The electrodeposition cell were made using Teflon (Rods Made from Teflon® PTFE), Aluminum plate, Chemical-Resistant PFA Compression Fitting (McMaster-Carr, Straight Adaptor for ¼'' Tube OD x ¼'' Male Pipe), Type 316 Stainless Steel Fully Threaded Stud and Zinc-Plated Steel Wing Nut (McMaster-Carr, 4-40 Thread Size). The Teflon were machined into two parts, cell body and cap, and assembled into an electrodeposition cell as shown in Figure 5.1a.

Constructing $Ag/AgCl_2^-$ Electrode A Pyrex glass tube, Pt wire, Ag rod, sleeve stopper septum (bottom I.D. x O.D. 1.5 mm x 3.9 mm, Sigma Aldrich) and 0.2 M TBACl solution in PC were used to make $Ag/AgCl_2^-$ electrode. After careful sanding and washing of Ag rods in water, AgCl was coated on Ag rods galvanostatically in 0.1 M HCl using a current density of 0.4 mA/cm^2 for 30 min. A short piece of Pt wire (0.5 mm in diameter and 1 cm long) was weld to the closed end of a piece of Pyrex glass tube (4 mm in inner diameter). The imperfect seal of Pt with Pyrex glass accounts for the very low leak rate of the filling electrolyte, which permits the necessary electrolytic contact with the working solution. The Pyrex tube was then filled with 0.2 M TBACl solution in PC. The Ag/AgCl rod was dried, inserted and sealed using a septum from the other end of the Pyrex tube. The electrode was then left 48 hours to reach equilibrium.

Calibrating $Ag/AgCl_2^-$ Electrode The potential of $Ag/AgCl_2^-$ electrode in PC was calibrated using cyclic voltammetry against Ferrocenium/Ferrocene (Fc^+/Fc) redox couple. A standard three-electrode set-up was used, with a Pt working electrode (2 mm diameter, CH Instruments, Inc), Pt mesh counter electrode and $Ag/AgCl_2^-$ reference electrode. 10 mM Ferrocene dissolved in PC with 0.2 M $TBAPF_6$ were used as the electrolyte. All cyclic voltammetry experiments were carried out with a Metrohm Autolab PGSTAT302N potentiostat with 50 mV/s scan rate in a glass cell.

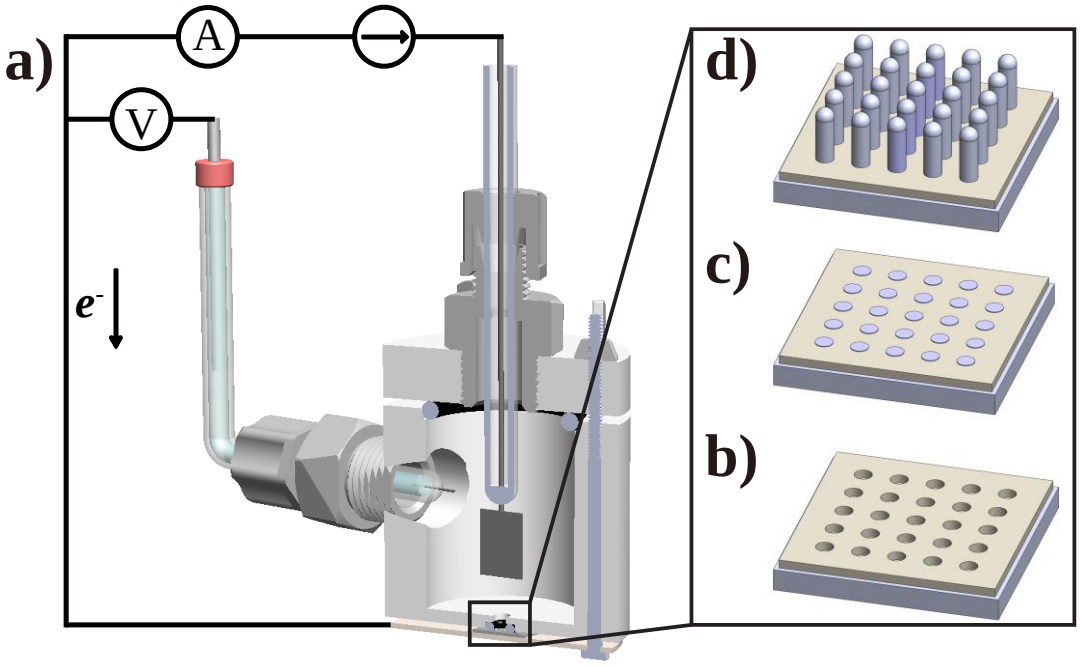

Figure 5.1. (a) Schematic illustration of the three-electrode Teflon cell used for Si ec-LLS. (b) Photoresist pattern coated Si substrate. (c) Pattern coated Si substrate filled with liquid metals. (d) Ec-LLS grown Si wires on patterned Si substrate.

Preparation of Patterned Si Substrate Hole arrays with 6 μm diameter, 6 μm pitch size and 2 μm thickness were patterned on all substrates using standard photolithographic procedures. Substrates (typically 10 x 10 mm and 0.6 mm thick) were degreased by sonicating for five minutes each in acetone, methanol, and water, then dried under a N_2(g) stream. For Si wafers, the native oxide was removed by etching in 5% HF for 60 s, rinsing vigorously with water, and drying under N_2(g), immediately prior to fabrication. A negative tone photoresist (SU-8 2025, Microchem Corp.) was then diluted from 68.6 % to 52.5 % total dissolved solids in cyclopentanone and stirred while covered for 60 minutes. The diluted SU-8 photoresist was spin-coated over the substrate and allowed to rest for two minutes at room temperature prior to soft baking on a hotplate at 95 °C for 3 minutes. The SU-8 coated substrate was placed on a vacuum chuck where the edge bead was manually removed with a razor blade by scraping ~1 mm inward along each edge. UV light exposure (OAI) for 11 s (Si) at 26 W/cm^2 through a custom-made contact photomask (Fineline Imaging, Colorado Springs, CO) was used to transfer the hole array patterns to the photoresist layer. Substrates were subject to a post exposure bake at 95 °C for 5 minutes on a hot plate. Development for 5 minutes under agitation with SU-8 developer (Microchem. Corp.) removed the unexposed regions of the photoresist. After development, the substrate was rinsed vigorously with 2-propanol, dried under N_2(g) and then annealed in air at 135 °C for 20 minutes to fully cross-link the SU-8 polymer. Substrates were then treated with an oxygen plasma at 20 sccm O_2(g) and 400 W (PE-50, Plasma Etch Inc.) for 3 minutes to remove un-crosslinked SU-8 from the surface of the photoresist.

Si ec-LLS To fill the patterned microwells on the Si substrate with Ga based liquid metals, samples were fixed on a home-made vacuum chuck while ~1 mL of the heated liquid metal was dispensed on the surface of the hole array pattern. A lint-free towel (Kimtech W4, Fisher) was used to compress the liquid metal against the substrate and force it to wet the interior of each hole. The towel was continually rubbed across the template in all directions until all holes were filled. Excess liquid metal on the surface of SU-8 and S1813 coated Si substrates was removed by using methanol and water soaked lint-free towels respectively. All Si ec-LLS experiments were performed with a Metrohm Autolab PGSTAT302N potentiostat in the custom-built Teflon cell (Figure 5.1a). The hole at the cell bottom was center aligned with a Viton O-ring (size # 006) and press-fit on top of a liquid metal coated Si wafer section to make the seal. Experiments were performed with a three-electrode configuration, using a Pt mesh as the counter electrode and a

$Ag/AgCl_2^-$ reference electrode. The cell was transferred into a N_2-purged dry glove box, loaded with 10-20 mL of electrolyte (0.5 M $SiCl_4$, 0.2 M TBACl in PC) then heated to temperature. The cell was capped to prevent electrolyte evaporation. The cell temperature was established with a sand bath and monitored with a digital thermocouple. After each experiment, the cell was taken out of the sand bath immediately to cool radiatively. Upon cooling to room temperature, the Si wafer sections were removed from the cell, rinsed with water 3 times, and dried under flowing N_2(g).

C. Results

Figure 5.2 shows the cyclic voltammograms of Fc^+/Fc redox couple ($E^o_{Fc+/Fc} = 0.400\ \text{V}\ vs.\ \text{NHE}$) in PC with $TBAPF_6$ as the supporting electrolyte.[8] Based on the positions of anodic (E_{pa} = 0.943 V) and cathodic (E_{pc} = 0.867 V) peaks, the formal potential of Fc^+/Fc redox couple is calculated using equation:

$$E^{O\prime}_{Fc+/Fc} = \frac{E_{pc} + E_{pa}}{2} = 0.90\ \text{V}\ vs\ Ag/AgCl_2^-$$

Since,
$$E^{O\prime}_{Fc+/Fc} \approx E^{O}_{Fc+/Fc} = 0.40\ \text{V}\ vs.\ \text{NHE}$$
$$E^{O\prime}_{Ag/AgCl} = -0.5\ \text{V}\ vs.\ \text{NHE}$$

The first four cycles of anodic and cathodic scans overlap well with each other, indicating good stability of the $Ag/AgCl_2^-$ reference electrode in PC.

Figure 5.3a shows the photoresist pattern on Si substrate. The sizes of the SU-8 patterns were measured to be 5.9 ± 0.4 μm, close to the nominal size of the photomasks. Ga were physically forced into the holes on the SU-8 patterns, with the excess droplets removed from the surface of the photoresist, leaving discrete Ga microdroplets as shown in Figure 5.3b. The Ga microdroplets appeared to be hemispherical as a result of surface tension and being in liquid phase.

Si microwires were grown between 120 - 140 °C galvanostatically *via* ec-LLS. Figure 5.4 shows the ec-LLS grown Si from Ga microdroplets produced at four different temperatures. At around 110 °C (Figure 5.4a), a mixture of Si nanocrystals and Ga were formed. The Si nanocrystals resembles the ec-LLS grown Si from a bulk Ga metal, which indicates a homogenous nucleation mechanism.[6] At 120 – 130 °C, microwire shaped Si deposits were formed. The caps of the wires contain Si nanocrystals similar to the Si deposit in Figure 5.4a. The bodies of the microwires did not show a smooth surface or indicate formation of faceted crystals (Figure 5.4b, c). At around

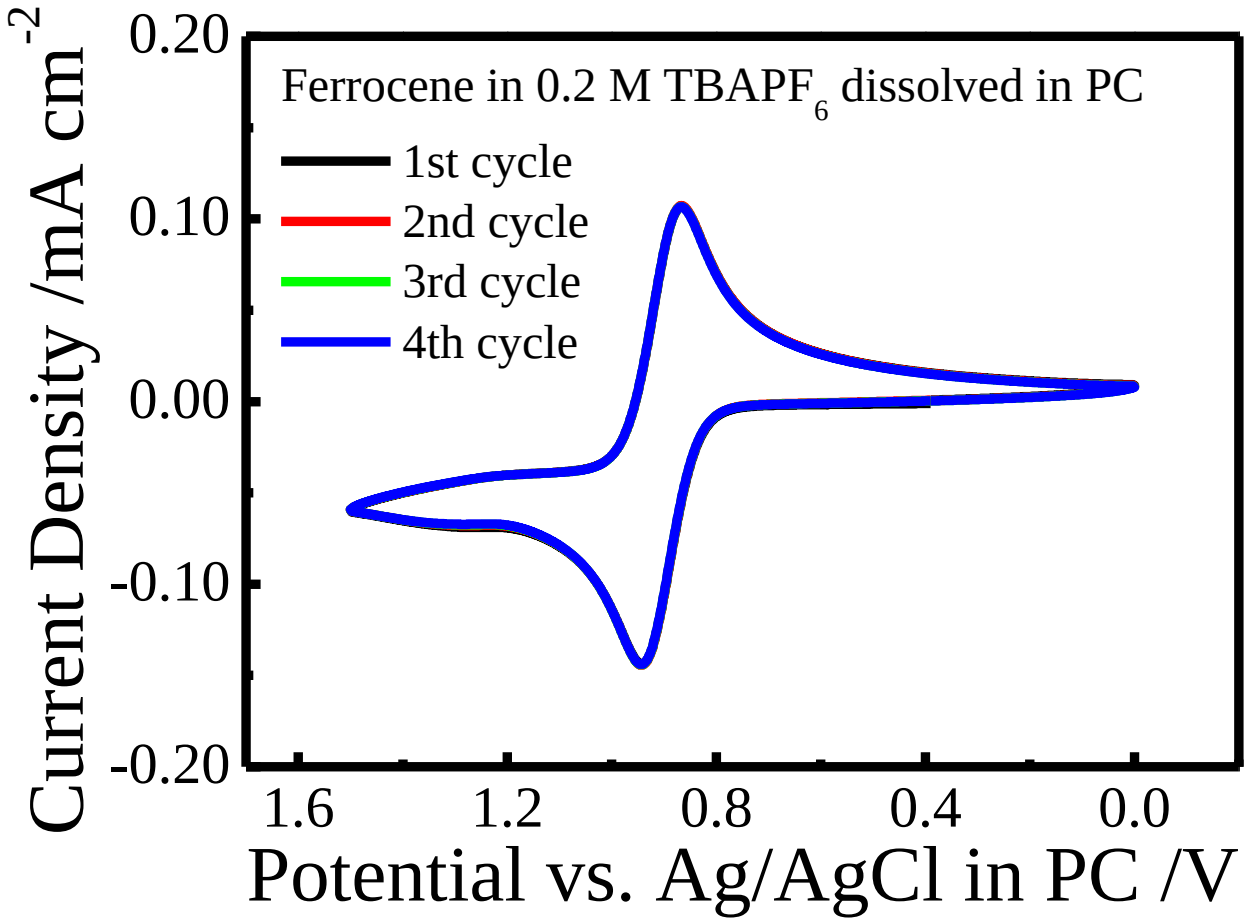

Figure 5.2. Cyclic voltammogram of Ferrocene on Pt electrode in 0.2 M $TBAPF_6$ dissolved PC at scan rate of 50 mV/s.

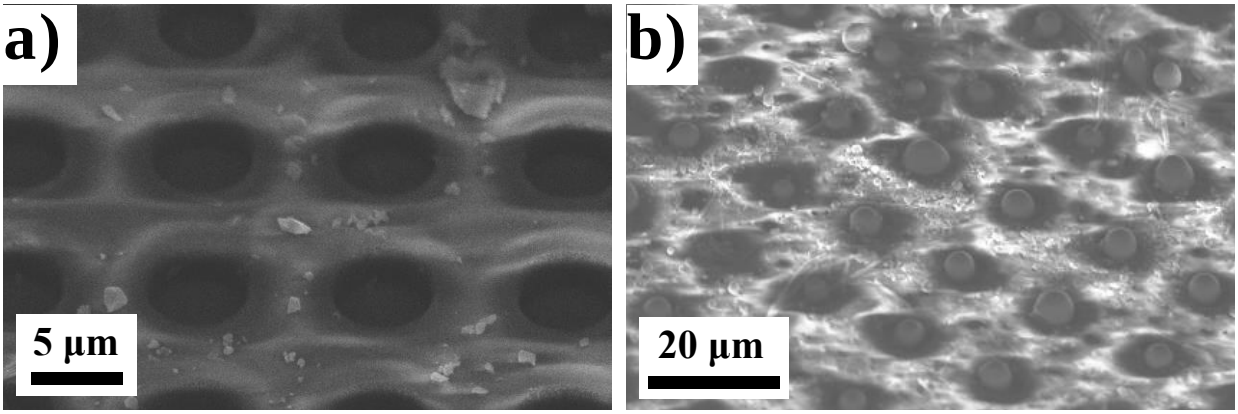

Figure 5.3. (a) SU-8 pattern of 6 µm hole size, 6 µm pitch size and 2 µm thickness. (b) SU-8 pattern filled with Ga microdroplets.

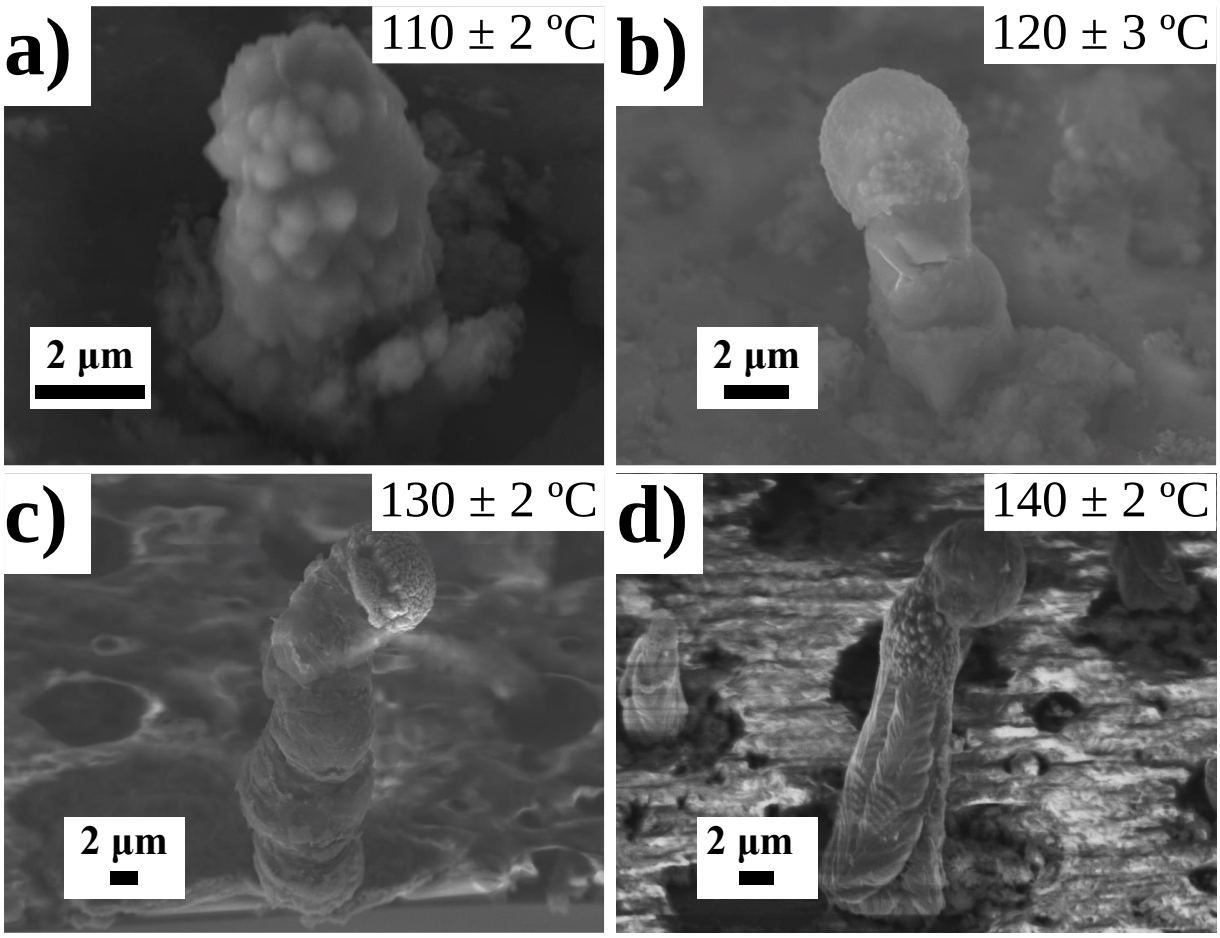

Figure 5.4. Ec-LLS grown Si microwires from Ga microdroplets at nominally (a) 110 °C (b) 120 °C (c) 130 °C and (d) 140 °C.

140 °C, Si microwires with a clear cap and body morphology were formed. The caps of the wires are spherical domes, implying a tip growth mechanism.[9] The body of the microwires are constituted by Si nanocrystals ordered in a layered fashion.

The chemical composition of Si microwires grown around 140 °C was examined to be Si with Ga impurities by EDS. Figure 5.5 demonstrates the EDS analysis of a single Si microwire using a scanning electron microscope. The EDS elemental map in Figure 5.5b and 5.5c shows the both the body and the cap are composed of Si and Ga. Si and Ga were distributed homogenously throughout the wire. Figure 5.5d shows the EDS spectrum of the body of the microwire. The peaks at 1.74 keV and 1.12 keV were attributed to the Kβ line of Si and Lβ line of Ga respectively, which indicates the wires are Si with Ga impurities.

Figure 5.6 shows a powder X-ray diffraction pattern of the Si microwires grown *via* ec-LLS at 140 ± 2 °C. The 2θ peaks around 28.4, 47.3 and 56.1 were indexed to be the diffraction peaks for Si (111), (220) and (311) planes.[10] The occurrence of three diffraction peaks indicates the Si microwires were polycrystalline. The low intensity was due to the small amount of Si microwires on the substrate. The background signal is from the glass slide substrate placed underneath the Si microwire sample being analyzed.

The use of Ga alloys, such as *e*GaIn and *e*GaAg, did not change the morphology of ec-LLS grown Si microwires. Ge microwires grown from *e*GaIn *via* ec-LLS showed less tapering comparing to wires grown from pure Ga.[11] However, Si microwires grown from *e*GaIn did not show any difference in morphology comparing to wires grown from pure Ga microdroplets as shown in Figure 5.7a. EDS mapping showed detectable Ga in the body of *e*GaIn grown Si microwires (Figure 5.7c). *e*GaAg was used to increase the solubility of Si in Ga, since Ag metal has high solubility of Ga in itself (11 at.% at 845 °C).[12] Figure 5.7b shows the Si microwire grown from *e*GaAg *via* ec-LLS at around 109 °C. The morphology of the Si microwire did not improve comparing to Si wires shown in Figure 5.4b, c as a result of increased Si solubility. The cap of the wire contains Si nanocrystals and the body of the wire shows a rough and non-faceted surface.

D. Discussion

Unlike in water where the solubility of AgCl is very low (1.3×10^{-5} M at room temperature), Ag^+ interacts strongly with Cl^- in aprotic solvents to form $AgCl_2^-$ or higher complexes.[13] A convenient way to determine the formal potential of the $Ag/AgCl_2^-$ electrode is through direct

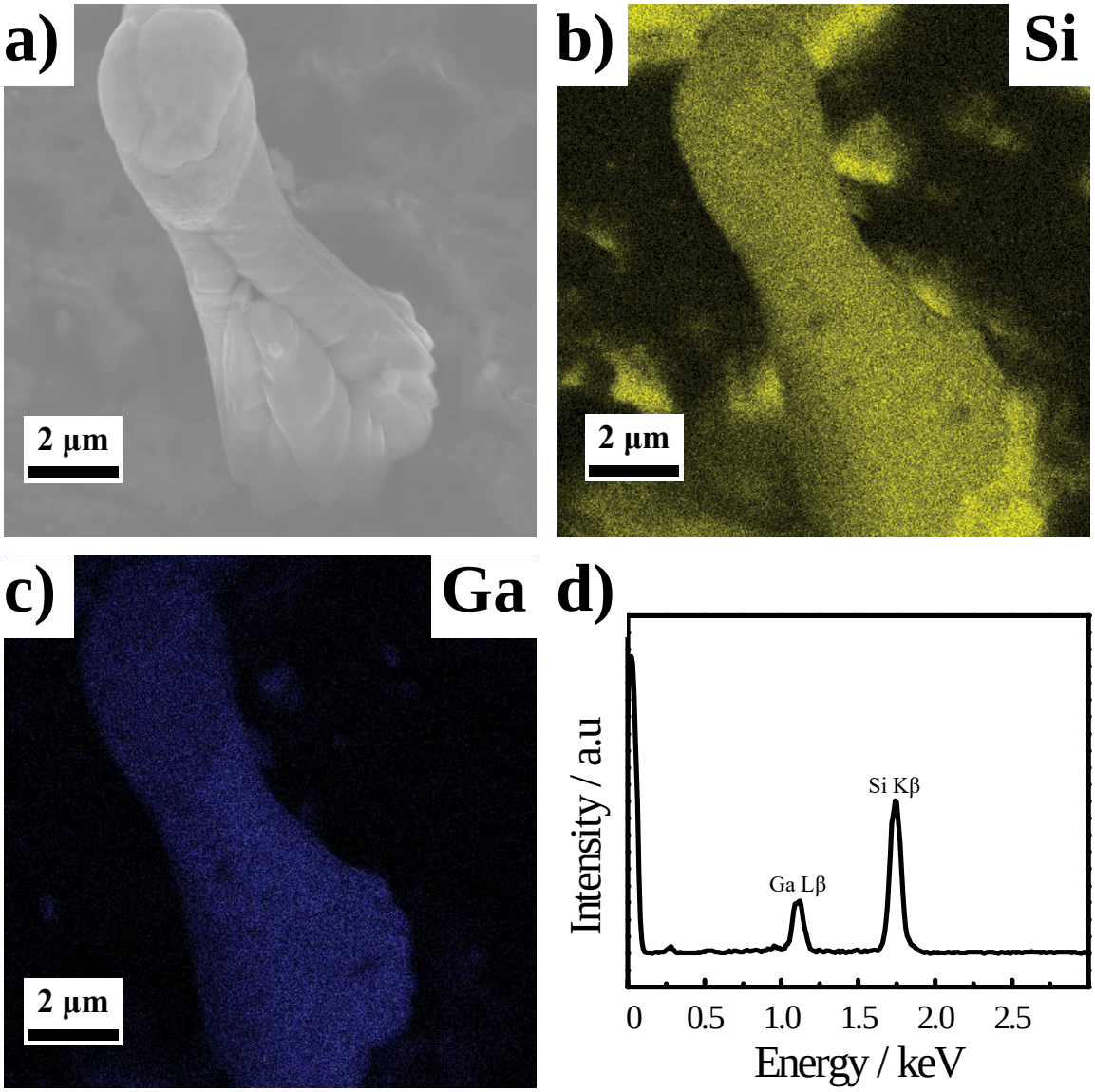

Figure 5.5. (a) Scanning electron micrograph of a Si microwire grown by ec-LLS. (b, c) Energy dispersive X-ray spectroscopic elemental map of a Si microwire. (d) Energy dispersive X-ray spectrum of the body of a Si microwire.

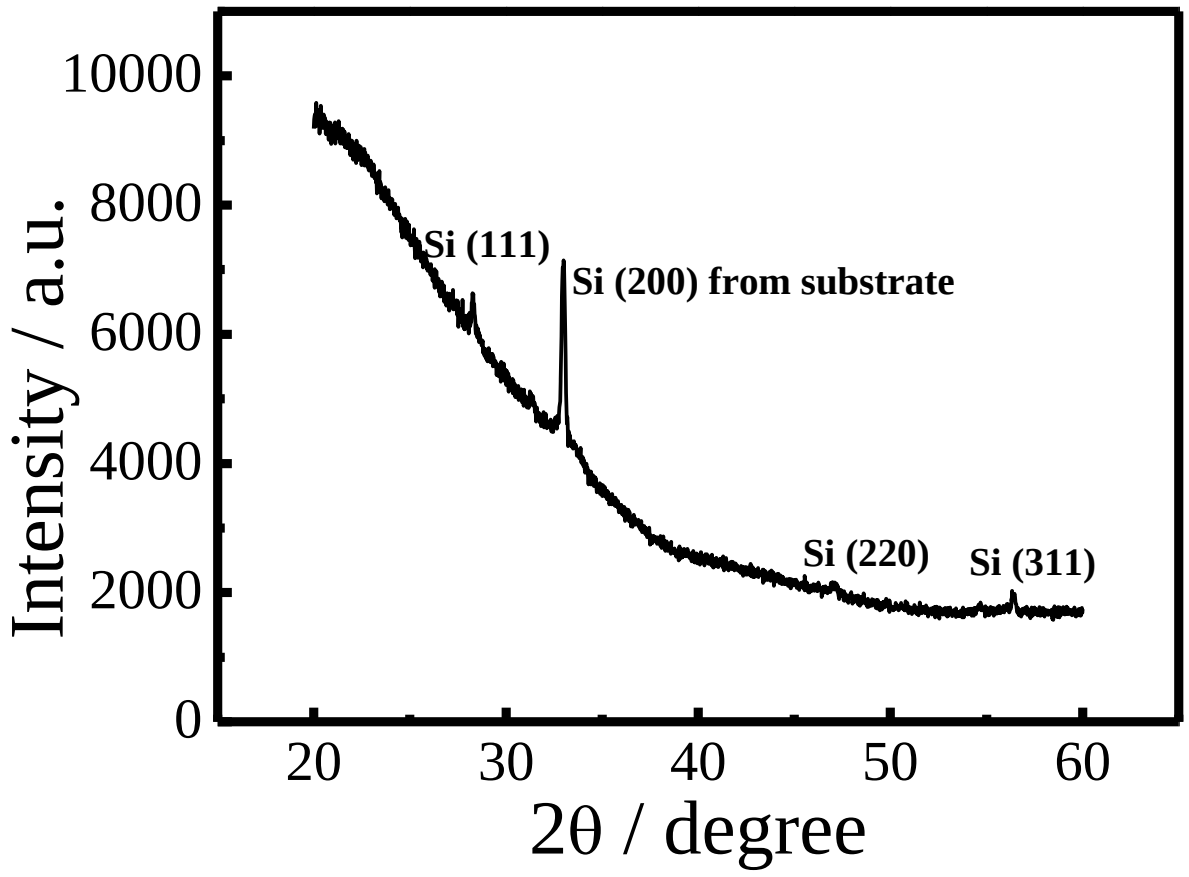

Figure 5.6. Powder X-ray diffractogram of a Si microwire coated n^+-Si(100) substrate.

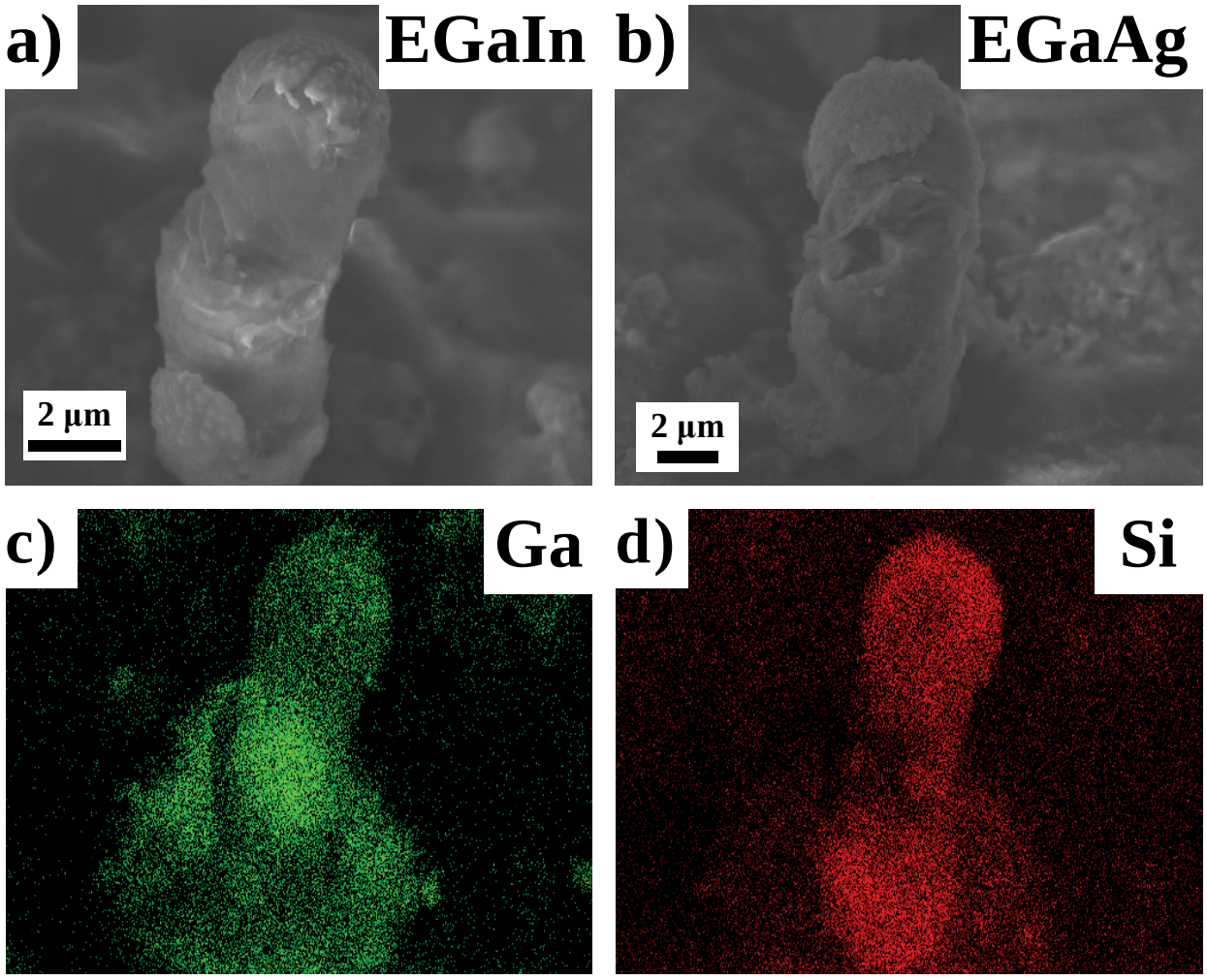

Figure 5.7. Scanning electron micrographs of Si microwires grown using (a) *e*GaIn (b) *e*GaAg microdroplets as the liquid metal electrodes at 108-110 °C. (c, d) Energy dispersive X-ray spectroscopic elemental map of the Si microwire in (a).

measurement using an internal reference, such as Fc^+/Fc redox couple. The formal potential ($E^{O\prime}_{Ag/AgCl}$) was measured to be -0.5 V ($vs.$ NHE), and was stable between different experiments. A stable and well-defined reference electrode allows the electrodeposition to be carried out *via* both potentiostatic and galvanostatic methods accurately.

The temperature dependence study demonstrates the practical limitation of Si microwire ec-LLS process. Heterogeneous nucleation and crystal growth from Ga nanoparticles take place at around 100 °C to produce Si nanowires.[7] However, when the size of the Ga droplets increase to micrometer range, homogenous nucleation dominates the crystal growth as shown in Figure 5.4a. The difference in the nucleation mode is a result of the size difference of the droplets. The micron size droplets create larger concentration gradients of Si between the near-surface of Ga droplets and liquid metal/substrate interface. The large Si concentration gradient allows the Si to nucleate at the near-surface region before the Si concentration at liquid metal/substrate interface is high enough for nucleation, even though homogenous nucleation requires higher supersaturation level comparing to heterogeneous nucleation.[14] When the depositions are carried out at higher temperatures, the diffusivity of growth species in liquid metal will increase according to following equation:[15]

$$D \propto \exp(-C\frac{T_B^m}{T})$$

C is a constant and T_B^m is the melting point of the liquid metal. The diffusivity (D) increases with increased reaction temperature (T), and the concentration of growth species will be more uniform (i.e. smaller gradient) within the liquid metal. As the crystal growth temperature is raised above a critical point, where the heterogeneous nucleation prevails over homogenous nucleation, crystal growth at liquid metal-solid substrate interface will push the liquid metal droplet up to facilitate a wire growth. As shown in Figure 5.4b, c and d, wire growth were observed when the reaction temperature is above 120 °C. The surface of the Si microwires are not as smooth as ec-LLS grown Ge microwires. It could be due to the fact that Si has lower solubility in Ga comparing to Ge, so with the same amount of growth species introduced into the droplet, it reaches a higher supersaturation level which results in smaller crystallites.[14] The height of different layered grains in the Si microwire in Figure 5.4d is around 500 nm which is comparable to the size of Si crystals produced by the homogenous nucleation mechanism.[6]

Even though Si microwires were produced *via* ec-LLS at 140 °C, the process lacks reproducibility due to volatility of the reaction electrolyte. We can calculate vapor pressure of the mixture system (p) using the Clausius Clapeyron equation:

$$\ln p = -\frac{\Delta H_v}{RT} + B$$

The ΔH_v is the latent heat of vaporization for the mixture system calculated by adding the ΔH_v for either component weighted by their mole fraction.[16-17] The mole fraction of 0.5 M $SiCl_4$ in PC is 4.3% $SiCl_4$ and 95.7% PC. Since the contribution of vapor pressure from $SiCl_4$ is four orders of magnitude higher than that of PC ($p^o_{SiCl_4}$ = 31.3 kPa, p^o_{PC} = 0.003 kPa at 25 °C), we could assume the vapor pressure of the mixture system (p) equals to the partial pressure of $SiCl_4$ (p_{SiCl_4}). The partial pressure of $SiCl_4$ calculated by Raoult's law is used as a reference point to generate B = 29.49.[17] T_b is calculated to be 100.5 °C as when p equals to one atmospherically pressure.

When the experiments are carried out at 140 °C, which is above the electrolyte's boiling point (T_b), the electrochemical reduction interface is frequently agitated by bubble formation in an unpressurized system, which leads to irreproducibility of electrodeposition results.

The EDS and XRD data collectively prove that the microwires are crystalline Si. EDS mapping and spectrum in Figure 5.5 prove that the microwires are Si with Ga impurities. The level of Ga content is similar to ec-LLS grown Si crystals from Ga.[6-7] Powder X-ray diffraction data confirms the crystallinity of as-prepared Si microwires. The Si microwires were grown on single crystalline n^+-Si(100) substrate, which does not show diffraction peaks besides Si (200). Therefore, the three other diffraction peaks in Figure 5.6 can be attributed to ec-LLS grown Si microwires.

To eliminate Ga from ec-LLS grown Si microwires, *e*GaIn was used as the liquid metal electrode instead of pure Ga. When used as the solvent for crystal growth, In incorporates less into crystals being grown.[11] At the same time, In enriches on the surface of *e*GaIn alloy.[18] Therefore, when *e*GaIn is used as the liquid metal electrode for Si ec-LLS, the In on liquid metal surface could preclude Ga from incorporating into the Si crystal. However, Figure 5.7c shows that Ga still incorporates into the body of Si microwires when *e*GaIn is used as the liquid metal electrode, and In was not detected in the Si microwire being grown. It is speculated that In was etched rapidly in the acidic $SiCl_4$ electrolyte, so it did not serve to preclude Ga incorporation.

Since the solubility of Si in Ga was one limiting factor for the growth of Si microwires at lower temperatures, Ag was introduced into the liquid metal to increase Si solubility. According

to the Ag-Ga phase diagrams, Ag has very limited solubility in Ga in the Ga rich region.[19-20] Experimentally, 0.9 wt.% of Ag was dissolved in Ga at ~100 °C and used as the liquid metal for Si crystal growth. However, Ag did not improve the Si ec-LLS process as can be observed from the results. First, Si nanocrystals are observed on the cap of Si microwire (Figure 5.7b) indicating high supersaturation and low Si solubility. Second, the body of Si microwire is not faceted, so large Si grains are not observed. It is speculated that *e*GaAg undergoes phase segregation and does not serve as a crystal growth solvent during the deposition process, because *e*GaAg is a metastable phase and will decompose to form Ga-Ag intermetallic when another species (i.e. Si) is introduced.

E. Conclusions

Crystalline Si microwires were produced *via* ec-LLS at > 120 °C. The Si microwires showed Ga incorporation and polycrystallinity. Designing a pressurized reaction cells will improve the reproducibility of the reaction and allow the experiments to be carried out at higher temperatures. Exploring Ga-free liquid metal electrodes that has higher Si solubility will allow growth of larger grain Si crystals without Ga impurities.

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CHAPTER 6

Future Work and Conclusions

A. Future Work

i. Doping mechanism of ec-LLS semiconductor growth

The doping level of ec-LLS grown semiconductor is higher than the solid solubility limits in the host material. For instance, the Ga concentration in Ge microwires is > 10.0 at.% (~ 3×10^{21} cm^{-3}), even though its maximum solid solubility is 4.9×10^{20} cm^{-3} at T = 670 °C.[1] On the other hand, when the resistivity of Ga grown Ge microwires were measured using current-voltage response, the dopant concentration was derived to be ~ 1×10^{18} cm^{-3}.[2] The discrepancy (three orders of magnitude) leads to the hypothesis that most of the Ga are inactive and reside in the interstitial site of Ge, and a small fraction of the Ga (~ 0.1%) are substitutional in the Ge crystal lattice contributing to its conductivity.

In order to test the aforementioned hypothesis, three sets of data need to be collected. First of all, the concentration of Ga in Ge needs to be measured quantitatively. Secondly, the charge carrier density in ec-LLS grown Ge needs to be determined. Thirdly, the effect of the large amount (~ 99.9%) of inactive Ga on Ge conductivity needs to be determined.

Ga impurities were first observed in ec-LLS grown Ge microwires by energy dispersive X-ray spectroscopy (EDS). The EDS spectrum is shown in Figure 6.1 which indicates Ga incorporation in Ge crystals. To gain more quantitative information on the Ga concentration in Ge, atom probe tomography (APT) was used to analyze a segment of Ge microwire grown from *e*GaIn microdroplet on a Si substrate. Figure 6.2 shows the tomographic distribution and concentration of different chemical compositions in ec-LLS grown Ge. The data suggests that there is 11.8 ± 0.7 at.% of Ga in Ge. As for the next step, Rutherford back scatter/channeling (RBS) and proton-induced X-ray emission data should be collected to determine substitutional fraction of Ga in the Ge lattice.[3] Carrier concentration in Ge could be determined by Hall effect measurement. Hall measurement of Ge nano/microwires can be carried out using a geometry described by Storm et al.[4]

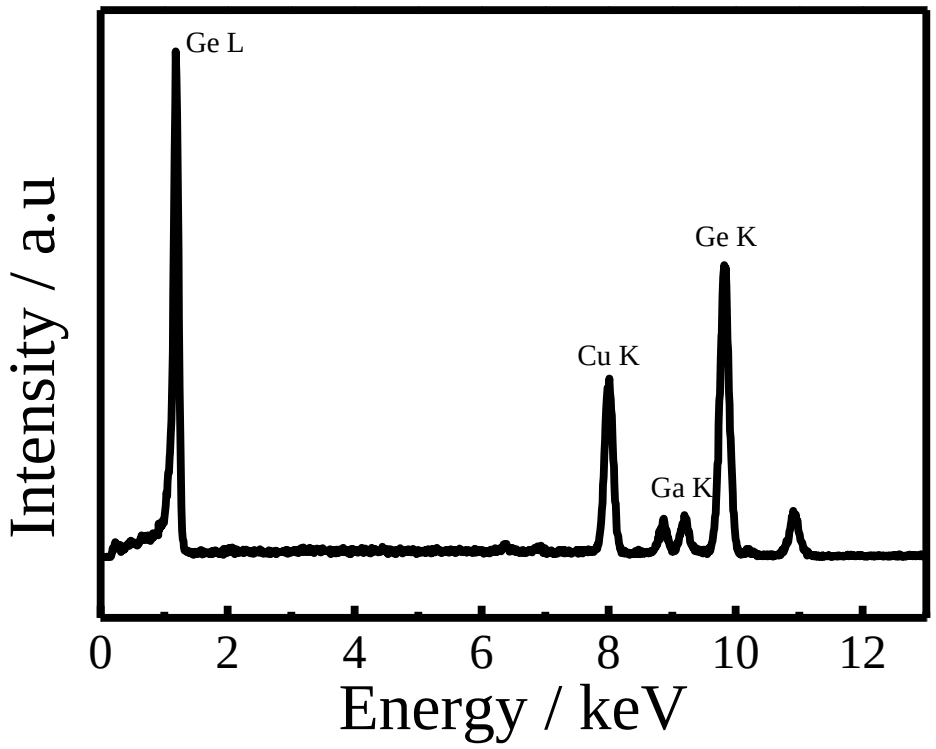

Figure 6.1. Energy dispersive X-ray spectrum of ec-LLS grown Ge using EGaIn as the liquid metal microelectrode.

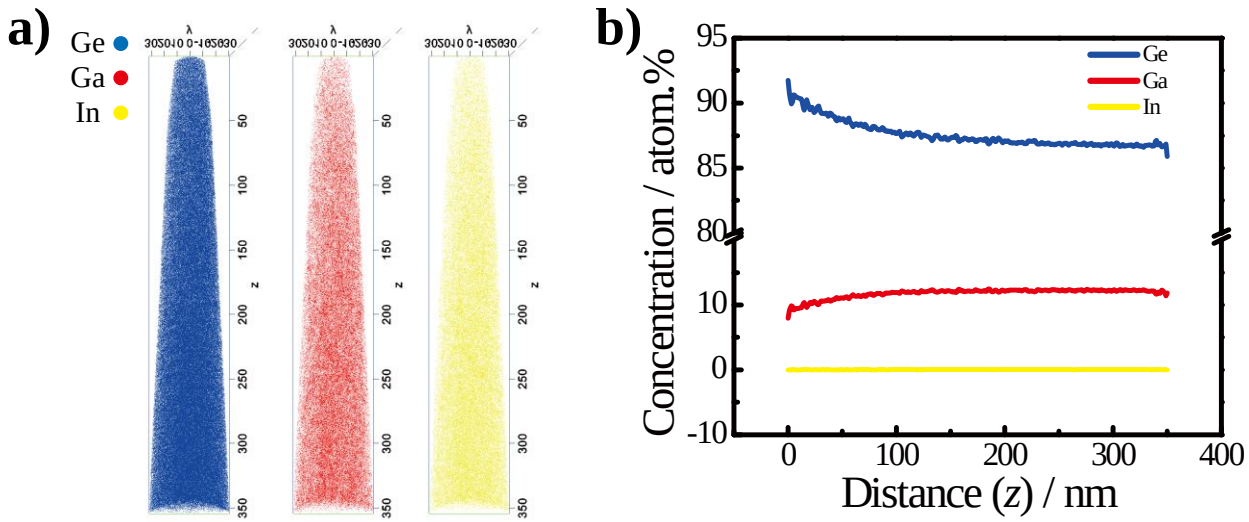

Figure 6.2. (a) Atom probe tomography analysis of the distribution of Ge, Ga and In in a slice of Ge crystal. (b) Line profile of atomic concentration of Ge, Ga and In in the slice of Ge crystal.

The substitutional Ga concentration measured from RBS and carrier concentration obtained from Hall measurement should be compared to determine the effect of inactive dopant (interstitial Ga) on Ge resistivity. Inactive dopant could give rise to negligible or non-negligible carrier scattering with respect to the ionized impurity scattering.[5] If Ga concentration measured with RBS correlates well with Hall measurement results, we can assume the effect of inactive Ga on resistivity is negligible. Otherwise, the scattering effect of Ga needs to be studied carefully.

ii. Electrochemical liquid-phase-epitaxy (ec-LPE) growth of Si thin films

Ec-LLS takes many forms, such as wire growth,[2, 6-8] bulk crystal growth[9-10] and thin film growth. Si thin films are used as both the substrate and absorber layer in solar cells,[11] and the active device layer in thin film transistors.[12] We hypothesize that by using a thin liquid Ga film, Si thin films can be produced via electrochemical liquid-phase-epitaxy (ec-LPE) using $SiCl_4$ electrolyte at around 100 °C.

First, an ec-LPE cell that allows the formation of Ga liquid metal thin film, as well as electrolyte transport to liquid metal surface for Si ec-LLS needs to be built. Secondly, experimental conditions allowing Si diffusion to the liquid metal/substrate interface and heterogeneous nucleation of Si on the substrate will be studied. Thirdly, the crystallinity, orientation, interface junction and electronic properties of the Si film needs to be determined.

To prepare the Ga thin film, fresh Ga (l) was dispensed on the channel created by SU-8 photoresist pattern on Si substrate. The Ga was spread out physically using a lint-free towel (Kimtech W4, Fisher) to cover the entire patterned channel. Since Ga forms oxide in air instantaneously[13], and gallium oxide could be a dielectric layer that impedes charge transfer, the gallium oxide formed between the liquid metal pool and Si substrate was also cleaned by 'wiping' with a lint-free towel.

A porous membrane (silicon carbide (SiC), Liqtech) was pressed on Ga to create a liquid thin film. The thickness of Ga film was defined by the height of photoresist pattern on the Si substrate. The small pore sizes (< 5 μm) on the front side of the membrane (Figure 6.4b) prevented Ga from diffusing through even under pressure, but allowed $SiCl_4$ electrolyte to transport to Ga surface to be electrochemically reduced. The SiC membranes were infiltrated with a hydrophobic material except for the area in the middle to confine the flow of the electrolyte (Figure 6.4a). The membrane with the hydrophobic material was pressed against a glass slide during curing (150 °C,

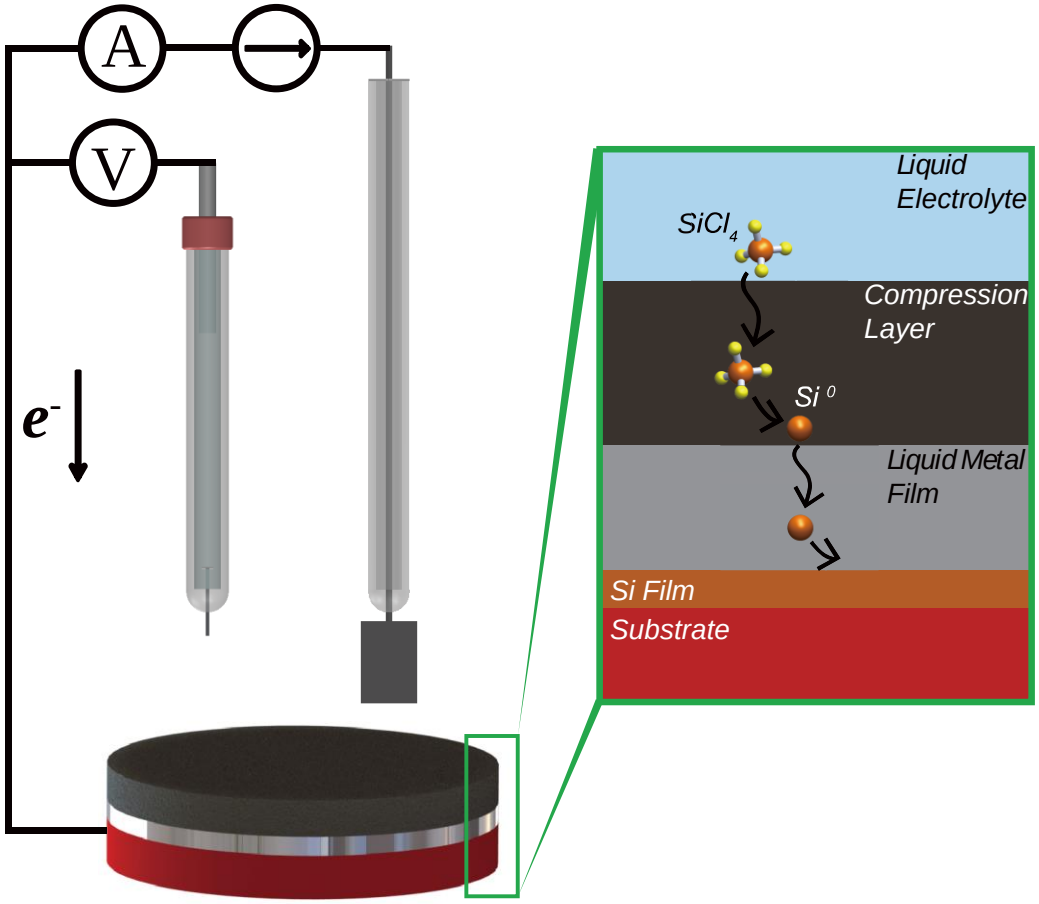

Figure 6.3. Schematic drawing of the Si ec-LPE process. Ga is compressed by Si substrate at the bottom, and a porous membrane that is permeable to electrolyte flow but resists infusion by the liquid metal at the top.

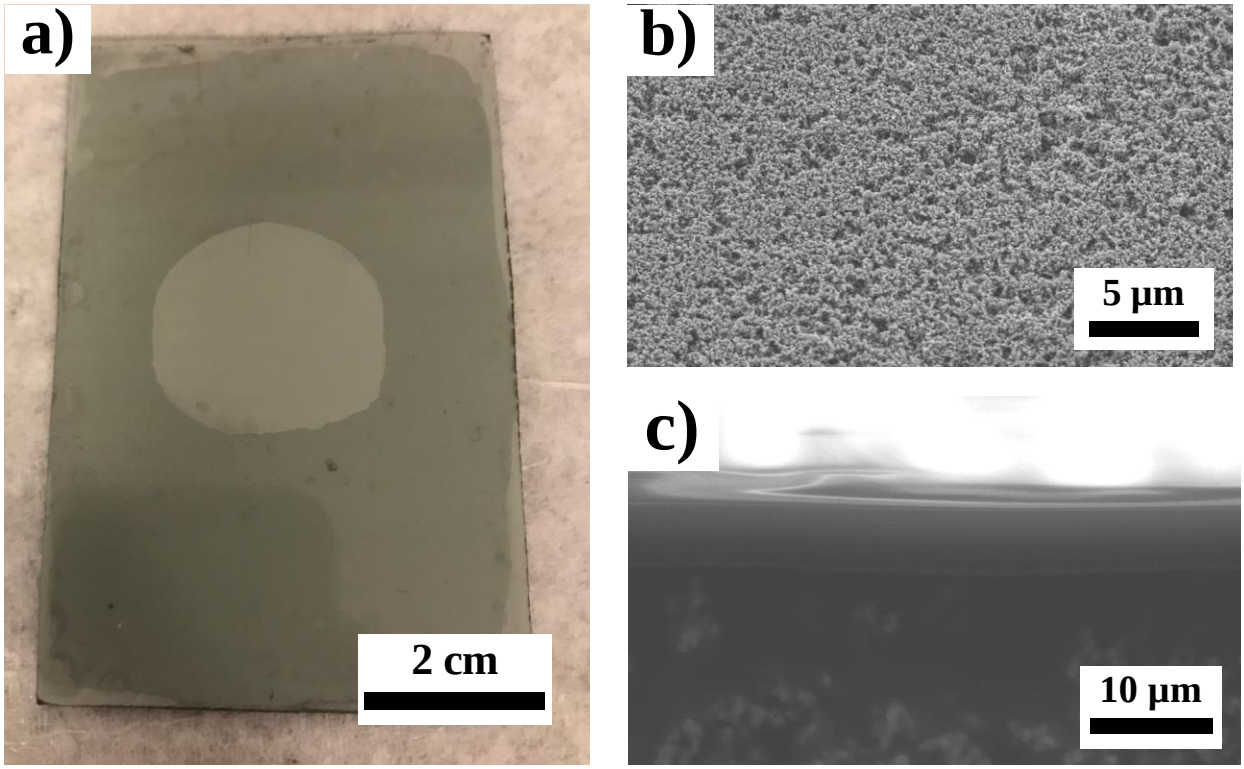

Figure 6.4. (a) Optical photograph of a hydrophobic material infiltrated SiC membrane. (b) Scanning electron micrograph of the front side of SiC membrane. (light color part in (a)). (c) Scanning electron micrograph of hydrophobic material on SiC surface.

10 minutes), so a flat hydrophobic layer of 4 ~ 6 μm thick above SiC surface was formed (Figure 6.4c).

The ec-LPE cell was transferred into a N_2-purged dry glove box after assembly. The electrolyte cell was filled with ~15 ml of electrolyte, capped with a Teflon piece with counter and reference electrodes affixed. $Ag/AgCl_2^-$ electrode in PC was used as the reference electrode, and was calibrated against Fc^+/Fc redox couple before use. The bottom plate of the cell was heated to reaction temperature and a reduction bias was applied to the bottom plate from a potentiostat.

Cyclic voltammetry was carried out to determine the potential for $SiCl_4$ reduction on Ga thin film electrode (Figure 6.5a). The reduction peaks between -1.3 ~ -1.5 V vs $Ag/AgCl_2^-$ is speculated to be reduction of Ga_2O_3 since the magnitude decreased more than 80% between the 1st and 2nd cycle. $SiCl_4$ reduction shows an onset around -1.6 V vs $Ag/AgCl_2^-$ in PC. Potentiostatic experiment (Figure 6.5b) at -1.8 V vs $Ag/AgCl_2^-$ was carried out to deposit a Si thin film on n^+-Si(100) substrate as shown in Figure 6.6a. Future experiments to study the effect of different deposition temperatures on deposit quality will be carried out. The correlation between film thickness and electrodeposition parameters (e.g. potential, time) should be studied to derive the crystal growth rate of Si ec-LPE process.

The crystallinity of the ec-LPE grown Si thin film was characterized by powder X-ray diffraction, but it did not show any difference comparing to the diffraction pattern of Si(100) substrate on which Si thin film was grown (Figure 6.6b). Grazing angle incidence X-ray diffraction needs to be carried out in the future, since it allows a clean diffraction pattern from the surface to be obtained. Scanning electron microscopy and transmission electron microscopy of the cross section of the ec-LPE grown Si film on Si substrate should be performed. SEM images could be used to characterize the general morphology of the film grown, and TEM can further characterize the crystallinity, junction structure of the as-prepared films. AFM should also be performed on the film to measure the film thickness and roughness with single nanometer resolution. Since the ec-LPE grown Si might have Ga impurities, which serves as a p-type dopant, and the film is grown on n^+-type Si substrate, it should form a p-n^+ junction or p^+-n^+ tunneling junction. Current-voltage measurement should be carried out on the as-grown Si film and n^+-Si substrate.

iii. Application of ec-LLS grown Si in Li-ion batteries

Si has the highest specific capacity (4200 mAh g^{-1}) out of all Li-ion battery alloy anodes.[14] Ec-LLS grown Si wires are ideal materials for Li-ion battery anodes due to the high specific

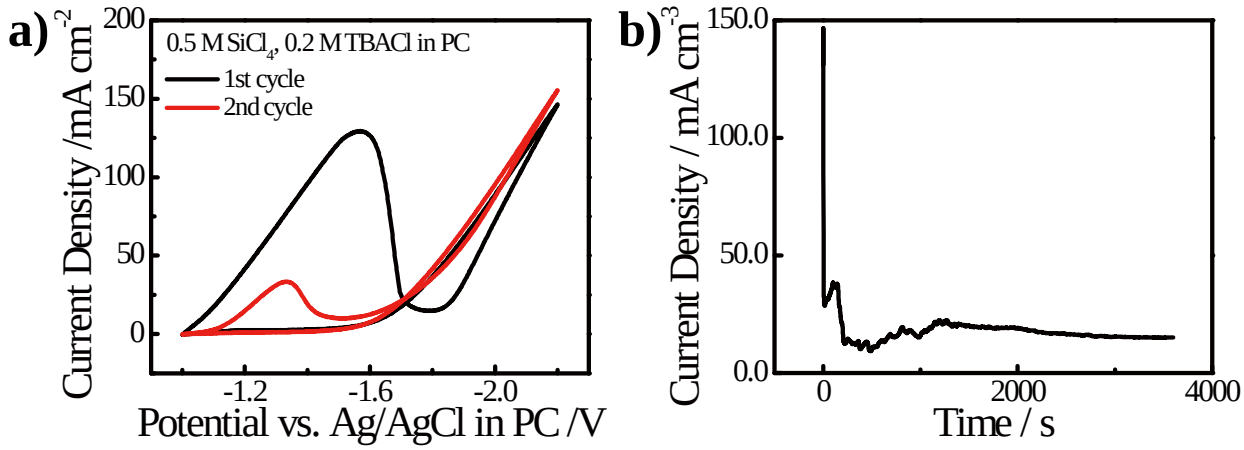

Figure 6.5. (a) Cyclic voltammogram of $SiCl_4$ on Ga thin film electrode at 110 °C. (b) Current response of $SiCl_4$ reduction at -1.8 V vs $Ag/AgCl_2^-$ in PC at 110 °C for 1 hour.

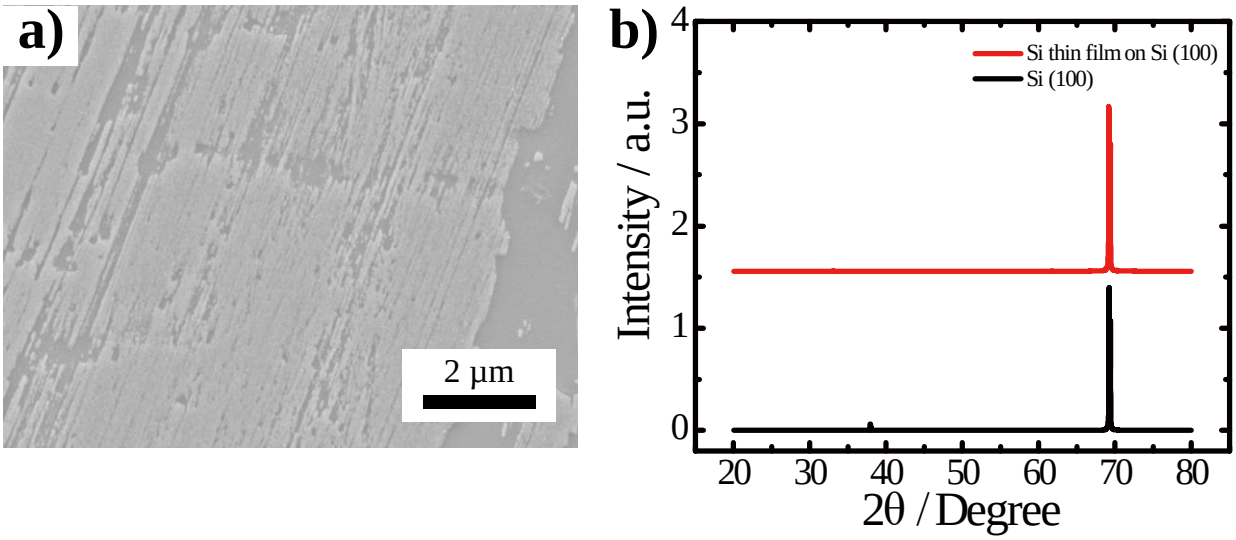

Figure 6.6. (a) Ec-LPE grown Si thin film on a n^+-Si(100) substrate. (b) X-ray diffractogram of ec-LPE grown Si thin film and Si(100) substrate.

capacity of Si, the wire morphology and Ga impurities.[15] However, clean Si wire ec-LLS from Ga droplets on a current collector (e.g. Cu, Stainless steel) is difficult, because it occurs at similar potentials comparing to amorphous Si deposition on the current collectors. The proposed solution here is to grow Si nanowire branches on ec-LLS grown Ge microwires, since Si grows on Ga selectively comparing to on Ge, and Ge microwires have been shown to grow on Cu substrates. The fabricated heterostructure could also take advantage of the large specific capacity of Si nanowires and high rate capability of Ge microwires to make hybrid and tunable Li-ion battery anodes.

First of all, a tandem ec-LLS growth needs to be carried out to grow the Ge microwires on Cu followed by Si nanowire ec-LLS on Ge microwires. Secondly, the morphology and chemical composition of the heterostructure needs to be characterized. Thirdly, the electrochemical properties of the as-prepared structure need to be tested in battery cells. The density and size of the Si nanowires need to be optimized to obtain maximized specific capacity and rate capability out of the Si/Ge anode.

A Cu substrate was patterned with SU-8 photoresist with 10 μm hole size, 10 μm pitch size and 2 μm thickness. *e*GaIn (l) were physicals forced into the pattern to form discrete liquid metal microdroplets. Ge ec-LLS were carried out on *e*GaIn microdroplets at 80 °C to form Ge microwires. The Ge microwire coated Cu substrates were cleaned, dried and immersed into $SiCl_4$ electrolyte for Si ec-LLS. Si nanowires were grown from the residual *e*GaIn nanodroplets on Ge microwire surface at 100 °C.

Scanning electron microscopy was used to characterize the morphology of the Si nanowire/Ge microwire heterostructure (Figure 6.7a). Energy dispersive X-ray spectroscopic mapping of the ec-LLS grown heterostructure showed the stem of the microwires was clearly Ge and the small branches were Si (Figure 6.7b, c).

The Cu foil coated with Si/Ge heterostructures were assembled into a button cell with a Li counter electrode to test their electrochemical performances. The capacity of the anode decayed > 30% from the 1st to the 2nd cycle and the overall capacity is lower than Ge microwire anodes (Figure 6.8).[15] Further studies on the failure mechanism of Si/Ge heterostructure should be carried out. The density, length and diameter of the Si nanowires could also be varied to test the effect on battery capacity and rate capability.

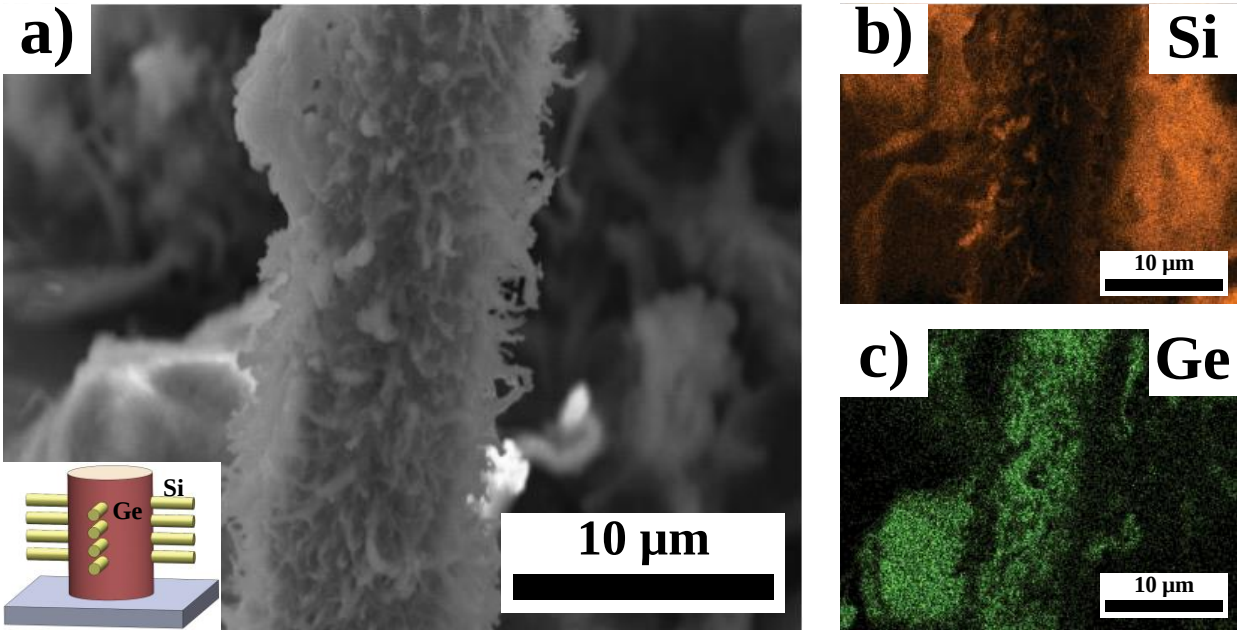

Figure 6.7. (a) Scanning electron micrograph of Si nanowire branched Ge microwire. Inset: schematic of the designed heterostructure. (b, c) Energy dispersive X-ray spectroscopic mapping of the ec-LLS grown heterostructure in (a).

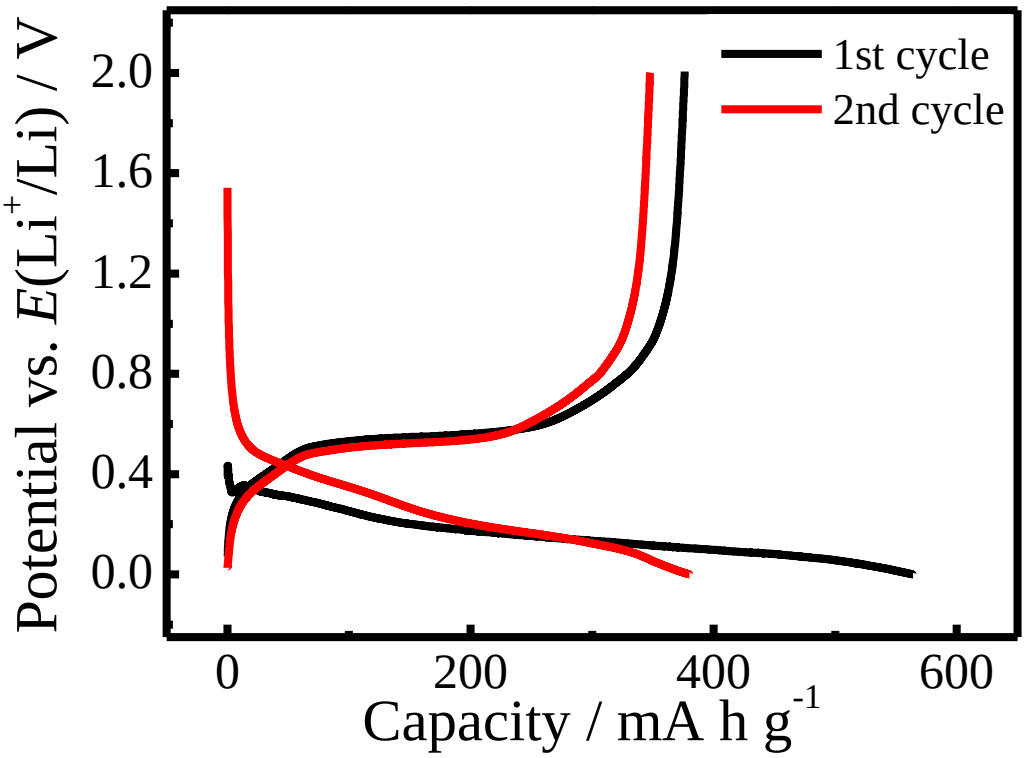

Figure 6.8. Galvanostatic discharge/charge curves of the Si/Ge heterostructure anode at 0.1 C rate.

B. Conclusions

This thesis has two major accomplishments in the field of solution crystal growth. First of all, it advanced the scope of the electrochemical liquid-liquid-solid process to Si and Ge nano/microcrystals with precise morphology control. Secondly, it has proven ec-LLS to be a method that produces high-performance anode materials for Li-ion batteries.

Ec-LLS, as an electrochemical solution growth method is one of the few that produces crystalline semiconductor materials at or below 100 °C. The ability to produce ec-LLS grown crystals of different useful morphologies is key to making this method relevant to various technologies. In this thesis, ec-LLS has been advanced to produce Ge/Si nanowires and microwires, in addition to Ge/Si bulk crystal growth developed in the past.[9-10] The prepared materials have shown controlled morphology and crystallinity using different forms of liquid metal, growth conditions and precursors.

To date, all crystals grown by ec-LLS exhibit measurable levels of residual metal. In this thesis, we have demonstrated ec-LLS grown microwires to be a Li-ion battery anode that has high specific capacity and long cycle lives. The high-performance is due both to the microwire morphology and Ga impurity incorporation. Therefore, impurity in ec-LLS grown crystal impede their use in devices using their semiconducting properties, but improves their performance in devices using their alloying properties.

Future directions should aim at understanding the impurity incorporation mechanism and precisely control the doping level in ec-LLS grown semiconductors. Only in this way, can ec-LLS grown materials be used in a wider range of semiconductor devices and making a greater impact to the materials science academy.

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