A Hands-On Approach to Advanced Undergraduate Instruction in Control and Circuitry in Power Electronics

Al-Thaddeus Avestruz[1], Candace Wilson[2], Robert W. Cox[3], Sara Campbell[1], Steven B. Leeb[1]

[1]Laboratory for Electromagnetic and Electronic Systems
Massachusetts Institute of Technology, Cambridge, MA USA

[2]Analog Devices, Wilmington, MA USA

[3]University of North Carolina, Charlotte
Room 235E, Woodward Hall, Charlotte, NC USA

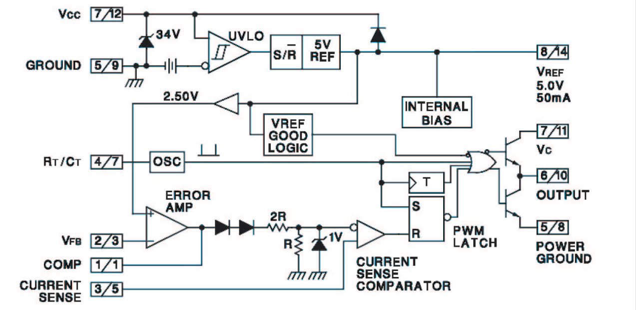
***Abstract*— We have developed a hands-on kit to teach control and circuits in power electronics. The kit consists of only discrete components to improve on what is missing from the contemporary IC design experience: the insight and intuition that arises from the building and testing of circuits where there is physical access to every node. The kit is modular and configurable, allowing the students to explore the design space with different topologies and component values, while trading-off bandwidth, power, and accuracy, among other things.**

I. INTRODUCTION

An integrated power electronic controller encompasses a range of analog and digital circuits and techniques. We have developed a hands-on kit for advanced undergraduates or beginning graduate students with circuits that consist of only discrete components, that is no building block ICs; much of what is missing from the contemporary IC design experience is the insight and intuition that arises from the building and testing of circuits where there is physical access to every node. In the kit, feedback and control is applied to circuits that control power electronics, while common elements such as differential pairs and current mirrors not only appear in familiar op-amps and comparators, but also in ostensibly arcane high side gate drivers, where one can demonstrate the use of high speed current switching. The kit is modular and configurable: students can explore the design space with different topologies and component values.

Companies are discovering that often, new electrical engineering graduates have limited knowledge about the activity of integrated circuit (IC) design. As a result, the initial training period is undesirably long and extensive. This is largely because it is challenging to duplicate the intricacies of IC design within the resource and time constraints of a typical electrical engineering curriculum. Additionally, it is difficult to keep abreast of the continually evolving IC fabrication process in industry.

Education in power electronics through hands-on approaches is continually evolving [1]–[6]. This paper presents the foundation for a new laboratory course. The objectives of the new course include the following: 1) introduce students to the fundamentals of power converter control theory, 2) teach students to design analog control circuitry block by block, 3) teach students to simulate models of their circuit designs, 4) instruct students on how to build and debug their circuits and compare experimental results with their simulated results. Ideally, the students obtain something foundationally similar to the IC design experience, while using discrete components and constructing on a breadboard or a pre-designed PC board with sockets for inserting components.



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 and CFP-14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

Fig. 1. The venerable Unitrode UC3842 provides the inspiration. The UC3842 has been used as a controller building block for many classically-controlled power converters. [7]

The practice of integrated circuit design is not an endeavor in isolation (although at times it may seem that way during the long hours of simulation and layout). Rather, much of it depends on how the circuit interacts with what can be considered the outside world. For example, in the design of a power electronic controller, one must consider the types of power MOSFETs that must be driven, along with sensing and power electronic topology. Additionally, one must consider what external components are required of the user: resistor and capacitor values must be reasonable; pin-count, for example, is reduced if components for external compensation are ground-

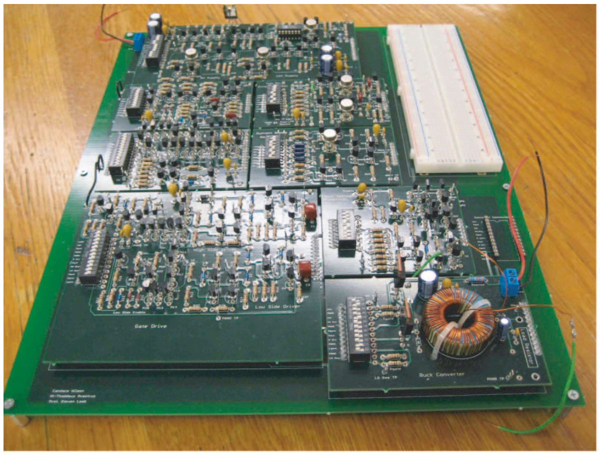


Fig. 2. The kit consists of individual functional modules that plug into a motherboard. The grounds are configurable and connections to each module can be individually switched.

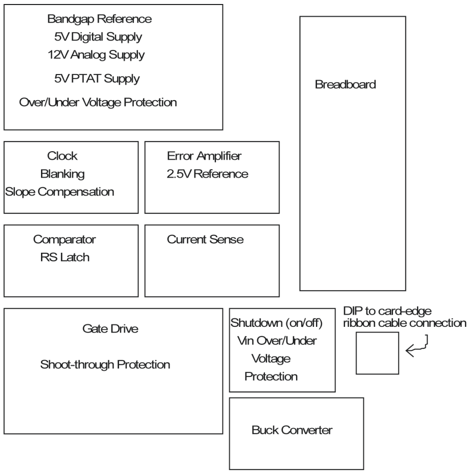


Fig. 4. Module layout of the kit motherboard.

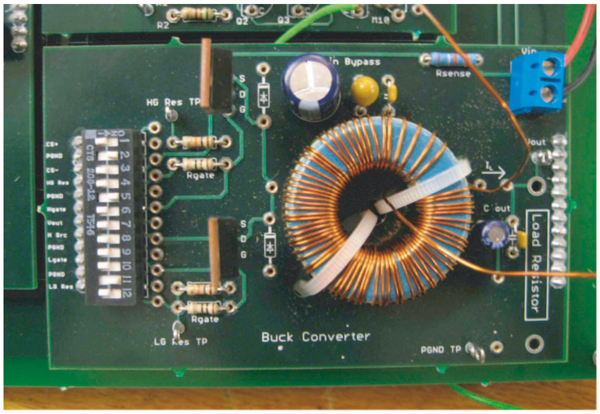


Fig. 3. Synchronous buck converter module.

referenced rather than floating, hence motivating designs that use an operational transconductance amplifier (OTA) as the error amplifier in PI (proportional-integral) controllers.

While device scaling is not easily available with a discrete design, the notion of current scaling is offered using resistors. Matching of active devices, while ordinary on a monolithic IC, requires us to provide matched pairs, or quads in a monolithic package, to properly make a bandgap reference, among other things. The modules are purposefully designed to be similar to circuits in ICs, although resistors and capacitors are used a bit more liberally. In these circuit designs, we avoid technology-dependent idiosyncrasies, whether IC or discrete.

Analog, digital and power electronics come together in what is consummately a mixed-signal design. Widely different time-scales are involved, with gate drive switching on the order of tens of nanoseconds and converter step responses on the order of a millisecond. Issues such as ground and supply partitioning become important along with the understanding of signal integrity.

Students are exposed to the practical application of classical control, which requires small signal approximations and averaged models. Minor loop compensation is revealed through current-mode control, which may require slope compensation.

The kit along with a mapping of its modules is illustrated in Figure 4. As one can see, a variety of analog and a few digital building blocks are represented.

II. PEDAGOGY

An objective of this approach is to expose students to not only the process of IC circuit design, but also to engineering design as a whole. As such, it is important to emphasize the need for both a *top-down* approach, which is a pervasive goal in industry along with a *bottom-up* approach, which is more prevalent in academia and research institutions. It is an approach that shepherds an idea to a product.

A typical course would include both a lecture or seminar followed by a unit of extensive laboratory exercises, which is then proceeded by an evaluation interview and a student demonstration.

A. System Level Design

The classic representation of a system level design is the block diagram, which is used to express the partitioning of functionality and the interconnection of a feedback and control system. Figure 4 not only illustrates the partitioning of functionality of a power electronic controller, but also represents a subdivision of pedagogic units.

As a product, an engineer is required to think about interface requirements—whether the context is system-level, board-level, device-to-device, signal integrity, or human interaction. These requirements are often derived in a top-down design formalism known as *use cases* [8]. In a power electronic controller, these issues include start-up, protection, shutdown, safe failure modes, and ESD, among others.[1]

At the beginning of each module, the student is required to construct a set of specifications for a particular design criteria,

---

[1] Electrostatic discharge. Although not explicitly addressed in this course, it is an example of a human interaction.

which in some cases may be student-selected and in other cases chosen by the instructor.

B. Feedback and Control

Familiarity with signals and systems and an exposure to classical control is preferable, but the fundamentals can be taught within the context of the course. Complexity in feedback stabilization depends on the choice of power converter topology—the simplest is the buck converter, which is a second-order system in voltage mode control and first-order in current-mode control; an increase in exercise difficulty can be achieved by using boost and buck-boost topologies, which include a non-minimum phase zero in their plant transfer function.

Minor loop compensation is introduced in current-mode control. In the existing module, peak current-mode control is implemented, but average current-mode control can be a topic for a final project or as an extension of the laboratory exercise.

C. Circuit Level Design

Success in large design projects is predicated on modularization and unit testing. The construction of the kit as a collection of daughterboards that plug into a motherboard encourages this type of thinking. Each daughterboard is a module that can be individually built and tested.

1) Circuit Building Blocks: The differential, or emitter-coupled pair along with the current mirror are a recurring element in the various modules. Some of the other circuit elements that are used are single-ended topologies such as a common emitter amplifier or an emitter follower. In the basic modules, we try to keep the circuits straightforward, but for laboratory exercises that ask for some innovation or in the final project, the students are encouraged to seek strategies and designs that show economy and elegance.

Among the things we would like students to consider are open-loop and closed-loop design options. In most instances, we strive for good open-loop characteristics so that our closed-loop behavior is better; other times, we have no control over the open-loop attributes and our only option is to place the system in a feedback loop.

2) Power Electronics: At a student's first glance, the power circuit appears to be the simplest. They are not yet aware of the richness of the design choices, even within a single topology, in power devices, magnetics, modes of operation, and control strategy, among others.

In the design of the power electronics, the students will design their own inductor and learn to select and size power devices, among other things. Power electronic design is a multi-dimensional effort, involving not only electrical, but also thermal and often mechanical design. [2] The choices made in the power electronic circuit will drive the controller design. We have chosen the continuous current mode, synchronous buck converter as a point of departure; there are other choices.

3) Designing Experiments and Measurements: A worthwhile exercise for the student in each lab module is to design methods to test functionality and measure parameters to verify that their specifications are met. For example, it is difficult to measure the dc characteristics of the error amplifier in Section III-D in the open-loop; although, we might encourage students to try. If, instead, they connect the amplifier as a follower, dc parameters such as offset voltage can be measured.

4) Equivalent Integrated Circuits: Although the discrete circuits that we use emulate those that appear in monolithic ICs, there are some notable differences. Resistors are not used as liberally in integrated circuits, but instead are replaced by active devices. Matching of transistors, both thermally and geometrically, is available only on a limited basis in discrete designs, but is assured on an IC.

A portion of each lecture or seminar on the equivalent integrated circuit design is appropriate. After first having the students design, construct, and test a discrete circuit module, they can be then be asked to design, simulate, and even lay out an equivalent integrated circuit, perhaps in CMOS as opposed to BJT. In this way, the learning effort stays connected to the design of ICs.

D. Design Process

In the contemporary spiral model for development, the process of design is iterated cyclically, with each iteration converging on the objective. Sometimes, the requirements are too aggressive and a revision of those requirements is acceptable, as long as the student understands the tradeoffs. The laboratory exercises are structured to encourage this type of process.

1) Calculation: Every design begins with a hand calculation; plausibility is observed by a *back-of-the-envelope* calculation, where order-of-magnitude quantities prevail. Engineering judgment is developed at this stage, where intuition and the ability to estimate allow the engineer to assemble, eliminate, and de-construct from a bewildering array of concepts. Ultimately, component values are calculated, so approximations and models, whether small-signal, linearization, or equivalent circuit, have to be appropriately chosen. It can be argued that one does not simulate or build unless one has a prediction of the outcome. To encourage this, students justify not only their choice of component values, but also the process and assumptions by which they had arrived at those values.

2) Simulation: While there is no doubt that simulation is an essential tool in modern circuit design, the speed and ease, which we value in industry, make it a crutch to learning. Simulation inherently contains many hidden assumptions and limitations, which the savvy and experienced engineer understands. SPICE, for example, does not predict thermal runaway; perhaps, it would be profitable to sacrifice a few NPN transistors to confound the students by having a textbook version of a discrete current mirror destroy itself. We can then demonstrate the use of resistors on the emitters and explain how emitter degeneration really behaves as implicit negative feedback.

Simulation tools such as SPICE and MATLAB do have a place in the learning of circuits and feedback. This laboratory course is intended to have a simulation component, but it is important to also choose examples that contrast occasions when simulation gives us answers that agree and on other occasions disagree with our hand calculations. On those occasions of disagreement, the student re-examines their assumptions and models, and revises their hand calculations. In addition, students should experience how painful it is to simulate a complete power electronic system in the time domain on a cycle-by-cycle basis using SPICE.

3) Building: It is almost a certainty that when the time comes to build and experiment, those who have not performed an adequate paper design inevitably suffer. Nature tends to expose non-robust designs; weaknesses that do not readily expose themselves can be accelerated by any number of “torture tests” that we instructors create. It is in building and experiment that we can confidently develop and calibrate intuition and judgment; we do so by requiring a design discipline where calculation, simulation and measurement are in agreement.

III. LABORATORY MODULES

A. Digital Logic and RS Latch

A power electronic controller is not exclusively an analog circuit domain; what makes it both challenging and interesting is that it is mixed-signal. On-chip logic is usually CMOS and in this module, students are exposed to transistor level design of logic gates and flip-flops. Figure 5 shows the schematic of the logic elements in the controller. This topic is a suitable introductory first laboratory, where students can become familiar with the lab kit, test instruments, simulation, and IC layout tools.

B. Comparator and Clock

A comparator is topologically similar to an op-amp, but with requirements that are germane to its operating context. In this unit, a student will connect a commercial op-amp such as the LM741 as a comparator and examine its transition characteristics and will have to explain why the LM741 is a poor comparator. The student will then design and build the comparator shown in Figure 6.

The clock shown in Figure 7 is a relaxation oscillator using the comparator that the student will have just designed and built. The frequency can adjusted externally to their abstracted IC controller using a capacitor and a resistor.

C. Voltage Regulators and Bandgap Reference

An obvious beginning to motivate the study of power conversion is a discussion of linear voltage regulators. In this unit, student build a linear regulator based on an operational amplifier and output driver, which is shown in Figure 8. The linear regulators that the students design and build become the internal rails for their controller. The thermal dissipation capability of these regulators become a salient limit to the power that is available to the rest of their controller. A useful exercise for the student is to naively estimate the power requirements of their controller circuit from the UC3842’s DIP package and then compare that with the datasheet’s power

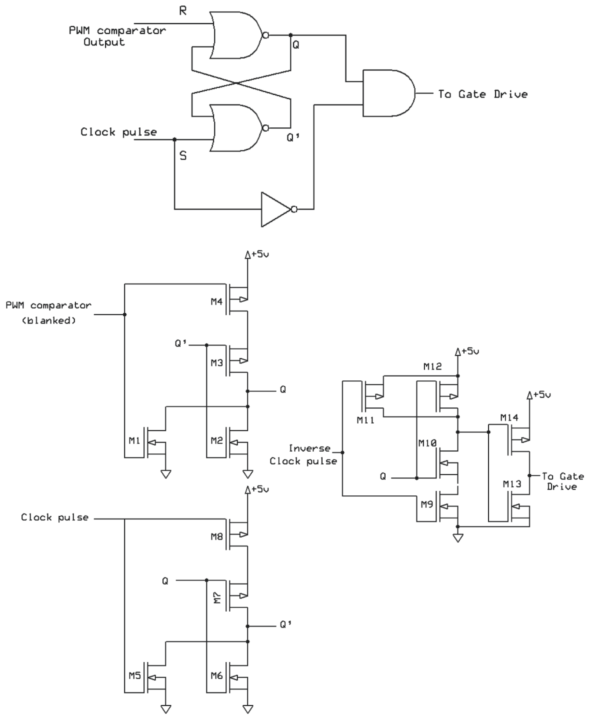
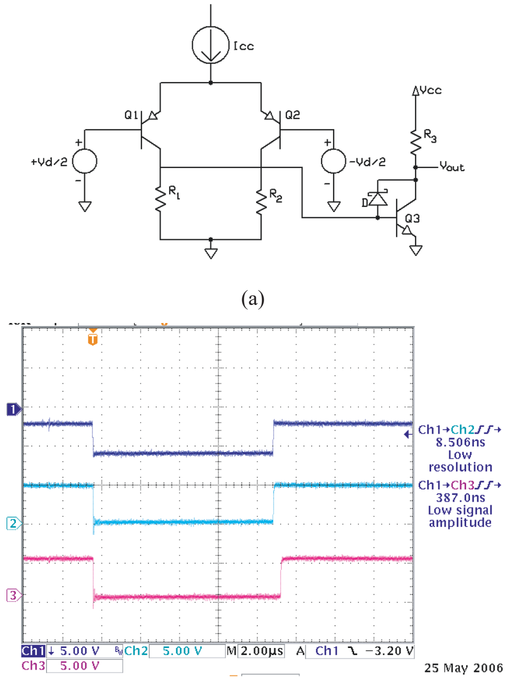


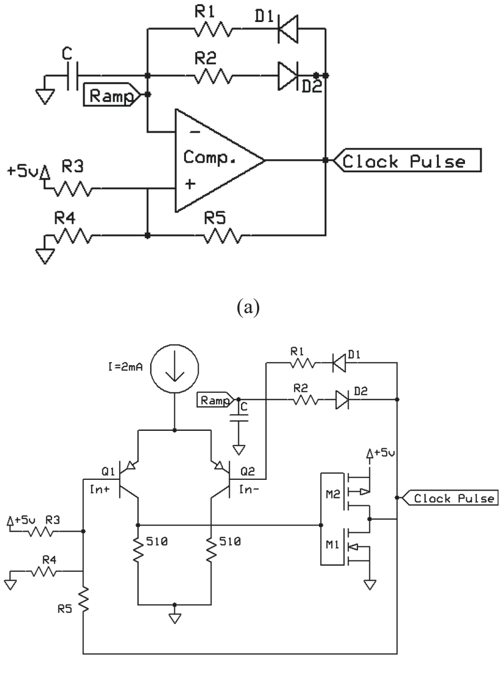
Fig. 5. Transistor level design of the logic for the PWM controller.



(a)

(b) Top: *Comparator Input.* Middle: *Output with Baker clamp.* Bottom: *Output without Baker clamp.*

Fig. 6. The comparator is topologically similar to an operational amplifier, but open-loop speed adds a design consideration. A careful examination of the risetime characteristics shows how the saturation of the output transistor increases the risetime to 387 ns from the 8.5 ns when using a Schottky diode as a Baker clamp.



(a)

(b)

Fig. 7. The clock which determines the PWM frequency is a relaxation oscillator.

consumption ratings. As their controller develops and as the students keep track of their power budget, they begin to notice the differences between a discrete and an IC design, leading them to understand how parasitics play a role in the power-speed tradeoff.

A common building-block in voltage regulators is the bandgap reference. Voltage references are a good point-of-departure for which to discuss the effects of temperature on circuits and devices. The usual bandgap references offer a solution by compensating the dominant linear term of a non-linear temperature coefficient, yet illustrating another example of linearization. Figure 9 illustrates the circuit. Matching transistors are required for Q_1 and Q_2 along with the current sources and the differential pairs. What is most notably missing is a start-up circuit. Why is this necessary? How do we design one into the circuit?

D. Error Amplifier

There are several design choices for an error amplifier. The most frequent design with which students have had experience is a closed-loop integrator, or perhaps proportional plus integrator, using an op-amp. In practice, feedback control elements—resistors and capacitors, are external components to the IC. An open-loop integrator based on an OTA (operational transconductance amplifier) allows the use of feedback elements that are ground referenced as shown in Figure 10, which results in smaller IC pin count. The tradeoff is poorer integrator accuracy and the requirement of a PTAT (proportional-to-absolute-temperature) tail current source for a loop bandwidth that is invariant to temperature. Students learn that integrator ramp accuracy is not critical in controller design, but offset might be and that a PTAT current source can easily be derived from a bandgap reference.

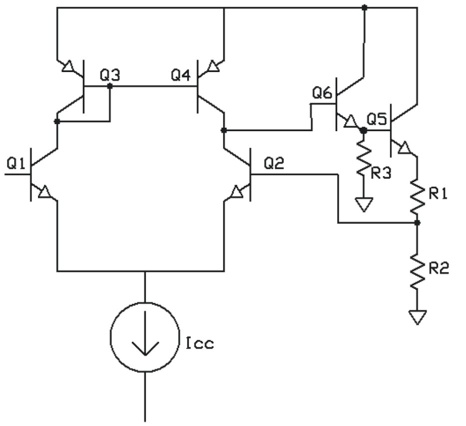


Fig. 8. A single-stage operational amplifier with a Darlington output stage is used as a voltage regulator. The compensation capacitor is not shown.

In this module, students learn to measure and test a subsystem that they discover is not well-behaved in the open-loop. How then does one measure offset voltage? What about AC characteristics and what are the large signal transient characteristics? Students might only be able to derive the small-signal bandwidth from a frequency sweep of the open-loop circuit. A possible solution is to connect the amplifier as a follower, but is there a good reason that the design be made stable for this configuration? The answer is usually yes and this allows the measurement of dc offset, and transient behavior from a step response. Most students will discover the slew rate limitations that they have forgotten to model in their calculations and might have to revise their choice of tail current and consequently their feedback components.

E. High-Side Current Sense Amplifier and Slope Compensation

There are several possibilities for a high-side current amplifier for peak current-mode control in a buck converter, including differencing amplifiers and current-mode circuits. Key requirements include good common-mode rejection and high speed; however, when gain accuracy and offset is not critical, an open-loop design (such as that shown in Figure 4) is suitable.

High-side peak current sensing is challenging, especially when it is performed on the side of the controlled-switch where the common-mode voltage changes with every switching instant. In this unit, students explore two ways of performing current sensing. The first, shown in Figure 11(a) is a closed-loop design based on a differencing amplifier. The second, an open-loop design is based on an OTA. Figure 11(c) shows the performance differences between the two designs.

The OTA design uses emitter degeneration to extend the linear range. Students calculate the required linear range and

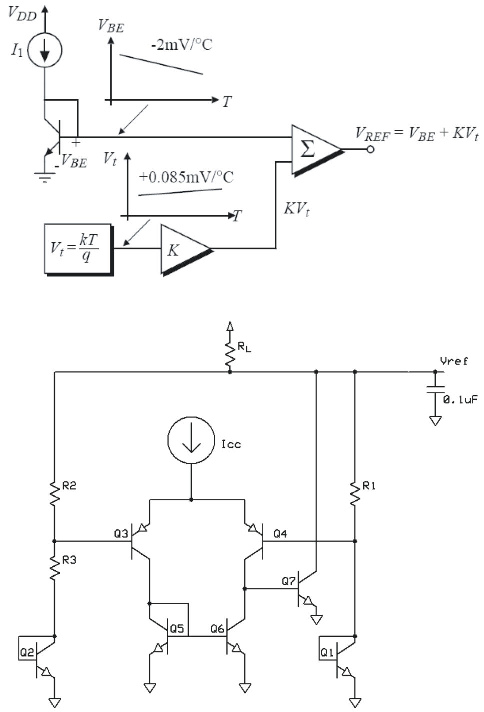


Fig. 9. Circuit for bandgap reference. Adapted from Grebene [9].

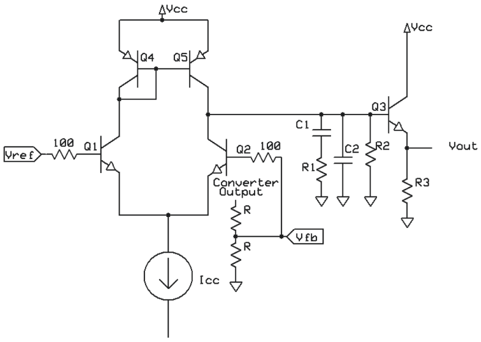
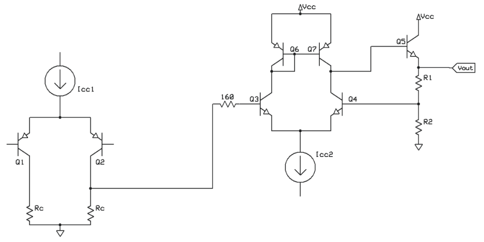


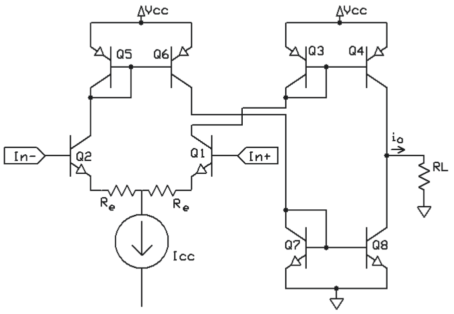
Fig. 10. The operational transconductance amplifier (OTA) is used to design an error amplifier with proportional plus integrator output (PI controller).

component values as well as the errors in both the open-loop and the closed-loop design. An investigation of the tradeoffs between an open-loop and a closed-loop design leads the student to understand that the errors in gain and offset are tolerable in the minor loop, but compromises in speed become critical.

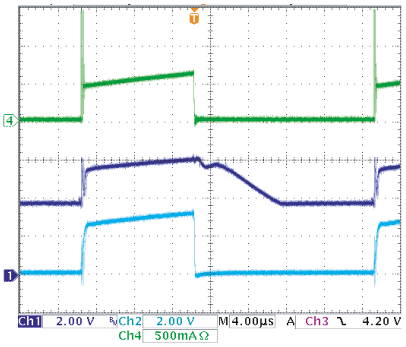
Slope compensation is a requirement for continuous current mode control with duty cycles over 50%. As part of this unit, a discussion in the tradeoffs between discontinuous versus continuous current modes of operation will motivate the additional complexity of slope compensation. In the UC3842, slope compensation is not available internally, but rather, is added with external components with a pseudo-ramp that is derived from the capacitor voltage in the clock as it is charged [7]. Figure 12 is an adaptation of this circuit. Students can choose to implement their own version of slope compensation.



(a) Differencing amplifier where the first differential amplifier provides a level-shift and differencing to the second stage gain. The circuit is obviously missing a compensation capacitor, which the student supplies.



(b) Emitter-degenerated OTA (operational transconductance amplifier).



(c) Top: *Tektronix Current Probe* (500mA/div). Middle: *Difference Amp Output* (2V/div). Bottom:*OTA Output* (2V/div).

Fig. 11. The closed-loop differencing amplifier shows poorer transient characteristics in comparison to the open-loop OTA.

F. Gate Drive and Leading Edge Blanking

On-chip gate drives require special attention because of the speed and voltage requirements, along with the potentially high peak currents. Totem pole NMOS gate drive outputs are typical. Figure 13 shows a design for a high side gate drive where fast switching can be achieved over a dynamic level shift using the already familiar emitter-coupled pair. The high-side gate drive derives its power using a diode charge pump, which is another interesting topic for discussion. There are limitations on switching frequency: too low and the high-side

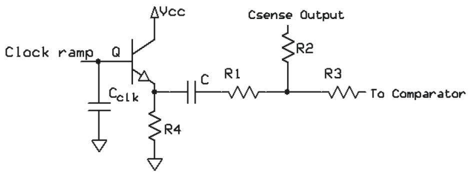


Fig. 12. Circuit for implementing slope compensation.

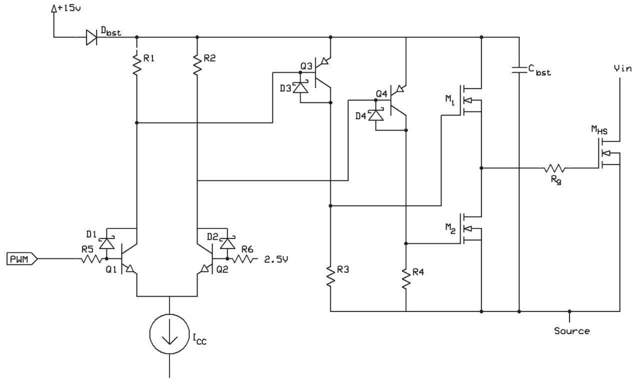


Fig. 13. High-side gate drive based on current switching of an emitter-coupled pair that is reminiscent of ECL logic.

drive voltage droops; too high and the gate drive losses become significant.

1) Shoot-Through Protection and Leading Edge Blanking: In the totem-pole structure that is used in the synchronous converters, the prevention of shoot-through of current between the upper and lower MOSFETs is critical. Figure 14 shows the design of high side and low enable that senses whether the complementary switch has turned off before enabling the other.

In peak current mode control, a large current transient appears through the MOSFET at the beginning of the switching instant, which is apparent in Figure 11(c). This often prematurely triggers the comparator in the peak current mode controller. Students experiment and investigate various solutions and their tradeoffs, including a low pass filter and leading edge blanking (shown in Figure 15).

G. Startup and Protection Circuits

Often an afterthought, the startup and protection circuits are required for robust design. Students carefully analyze the startup process and evaluate assumptions about the initial conditions of their devices, going through ”what-if” scenarios for their PWM controller.

The students will discover that if they test their protection circuits properly that under certain occasions the undervoltage and overvoltage lockouts oscillate. Why does this occur? What is a solution? With a little bit of thought, the answer is obvious: add some hysteresis.

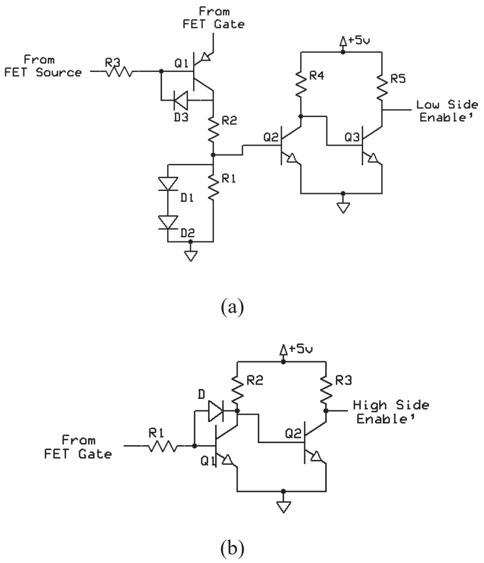


Fig. 14. Low-side (a) and high-side (b) enable circuits prevent shoot-through from top-side to bottom-side power MOSFETs.

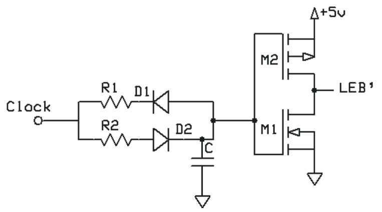


Fig. 15. Leading-edge blanking using what is essentially a one-shot on an inverter.

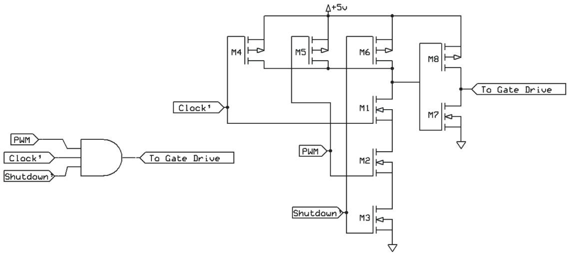
H. Putting It All Together: The Final Project

The final project offers the students an opportunity for innovation. Most often these innovations occur as bottom-up design, in the circuits and the feedback. This is partly due to limitations in using the kit as the stucture for the final project. As history has shown, the UC3842 is a versatile part, much like the 555-Timer IC. For example, variable frequency controllers such as constant on- and off-time, as well as critical conduction controllers can be designed and configured from the basic building blocks in the kit.

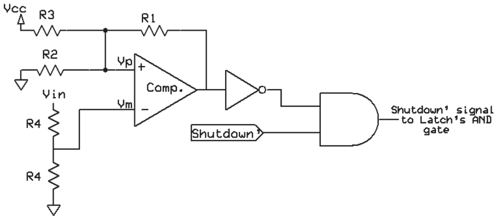
There are quite a variety of other optimizations that are suitable for a final project: minimization of controller power dissipation, perhaps through adaptive biasing; minimizing power consumption; or designing their own functional block such as a soft-start, among others.

IV. CONCLUSIONS ON KIT DESIGN

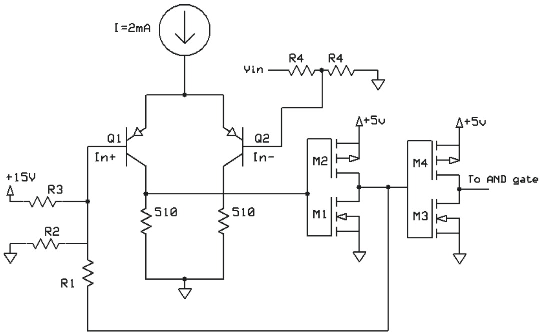
There are several requirements to the design of this laboratory kit. Pin sockets are used for all components so the modules are reusable while also minimizing soldering. The modularity of the motherboard/daughterboard design and the configurability of grounds and other connections allows the



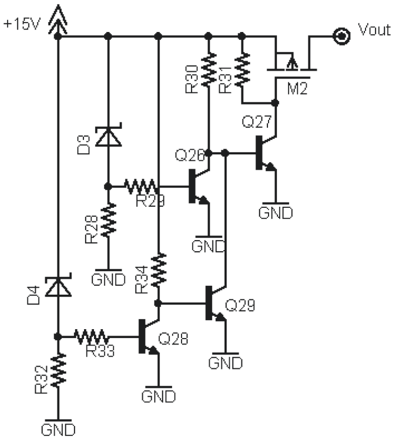
(a) Shutdown Logic



(b) Power Input Undervoltage Lockout.



(c) Transistor Schematic of the Power Input Undervoltage Lockout.



(d) Lockout for Undervoltage and Overvoltage of Controller Input Rail.

Fig. 16. Basic protection circuitry for the power electronic controller.

course and the circuits to evolve and to allow maintenance by only replacing only those modules that are damaged. Testpoints to which instrumentation and probes may be clipped are available on most of the nodes.

The course syllabus is continually evolving and developing. Our goal is to provide a platform that can also evolve and develop.

ACKNOWLEDGMENT

This work was supported by the Center for Materials Science and Engineering, a Materials Research Science and Engineering Center funded by the National Science Foundation under award number DMR 02-13282, and by the Grainger Foundation. The authors gratefully acknowledge the valuable advice of Professor James Kirtley.

REFERENCES

[1] C. Wilson, "Development of a laboratory course in power electronic control circuitry based on a pwm buck controller," Master of Engineering, MIT, 2006.
[2] M. Alvira, "Courseware development for a laboratory class in power electronics," Master of Engineering, MIT, 2005.
[3] R. S. Balog, Z. Sorchini, J. W. Kimball, P. L. Chapman, and P. T. Krein, "Modern laboratory-based education for power electronics and electric machines," *IEEE Transactions on Power Systems*, vol. 10, no. 2, pp. 538–547, 2005.
[4] J. Hudgins, A. Montti, and R. Dougal, "Control system laboratory: A power electronics teaching experience," in *COMPEL 2002*. Mayaguez, Puerto Rico: IEEE, 2002.
[5] N. Mohan, W. Robbins, P. Imbertson, T. Undeland, R. Panaitescu, A. Jain, P. Jose, and T. Begalke, "Restructuring of first courses in power electronics and electric drives that integrate digital control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 429–437, 2003.
[6] P. T. Krein and P. W. Sauer, "An integrated laboratory for electric machines, power systems and power electronics," *IEEE Transactions on Power Systems*, vol. 7, no. 3, pp. 215–222, 1992.
[7] Unitrode, "Unitrode application note u-100a: Uc3842/3/4/5 provides low cost current mode control," p. 15.
[8] I. Alexander and T. Zink, "Introduction to systems engineering with use cases," *Computing and Control Engineering Journal*, vol. 13, no. 6, pp. 289–297, 2002, tY - JOUR.
[9] A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*. New York: John Wiley and Sons, 1984.