Energy Efficient Pipeline ADCs Using Ring Amplifiers

by

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ABSTRACT

Pipeline ADCs require accurate amplification. Traditionally, an operational transconductance amplifier (OTA) configured as a switched-capacitor (SC) amplifier performs such amplification. However, traditional OTAs limit the power efficiency of ADCs since they require high quiescent current for slewing and bandwidth. In addition, it is difficult to design low-voltage OTAs in modern, scaled CMOS. The ring amplifier is an energy efficient and high output swing alternative to an OTA for SC circuits which is basically a three-stage inverter amplifier stabilized in a feedback configuration. However, the conventional ring amplifier requires external biases, which makes the ring amplifier less practical when we consider process, supply voltage, and temperature (PVT) variation. In this dissertation, three types of innovative ring amplifiers are presented and verified with state-of-the-art energy efficient pipeline ADCs. These new ring amplifiers overcome the limitations of the conventional ring amplifier and further improve energy efficiency.

The first topic of this dissertation is a self-biased ring amplifier that makes the ring amplifier more practical and power efficient, while maintaining the benefits of efficient slew-based charging and an almost rail-to-rail output swing. In addition, the ring amplifiers are also used as comparators in the 1.5b sub-ADCs by utilizing the unique characteristics of the ring amplifier. This removes the need for dedicated comparators in sub-ADCs, thus further reducing the power consumption of the ADC. The prototype 10.5b 100 MS/s comparator-less pipeline

ADC with the self-biased ring amplifiers has measured SNDR, SNR and SFDR of 56.6 dB (9.11b), 57.5 dB and 64.7 dB, respectively, and consumes 2.46 mW, which results in Walden Figure-of-Merit (FoM) of 46.1 fJ/ conversion·step.

The second topic is a fully-differential ring amplifier, which solves the problems of single-ended ring amplifiers while maintaining the benefits of the single-ended ring amplifiers. This differential ring-amplifier is applied in a 13b 50 MS/s SAR-assisted pipeline ADC. Furthermore, an improved capacitive DAC switching method for the first stage SAR reduces the DAC linearity errors and switching energy. The prototype ADC achieves measured SNDR, SNR and SFDR of 70.9 dB (11.5b), 71.3 dB and 84.6 dB, respectively, and consumes 1 mW. This measured performance is equivalent to Walden and Schreier FoMs of 6.9 fJ/conversion·step and 174.9 dB, respectively.

Finally, a four-stage fully-differential ring amplifier improves the small-signal gain to over 90 dB without compromising speed. In addition, a new auto-zero noise filtering method reduces noise without consuming additional power. This is more area efficient than the conventional auto-zero noise folding reduction technique. A systematic mismatch free SAR CDAC layout method is also presented. The prototype 15b 100 MS/s calibration-free SAR-assisted pipeline ADC using the four-stage ring amplifier achieves 73.2 dB SNDR (11.9b) and 90.4 dB SFDR with a 1.1 V supply. It consumes 2.3 mW resulting in Schreier FoM of 176.6 dB.

CHAPTER 1

Introduction

The analog to digital converter (ADC) is one of the most essential building blocks in electronic systems. Even though signal processing is nowadays mostly done in digital domain thanks to cost effective integration and energy efficient operation from the process scaling, the system still requires ADCs to convert real world analog signals to digital data. In other words, ADCs work as interfaces between the real analog signals such as images, sounds, various sensor (temperature, pressure, etc.) signals, and radio frequency signals for communications to the digital world. As the use of portable electronic devices greatly increases, to enhance battery lifetime, the energy efficiency becomes one of the most important specifications in ADC design. Therefore, researchers have been trying to find ways to improve energy efficiency of ADCs.

1.1 ADC Figure of Merits and Research Trend

In order to fairly compare the energy efficiency of ADCs with different specifications, researchers have come up with figures of merit (FoM). ADC FoMs combine several performance metrics which directly affect the energy efficiency, such as power consumption, conversion speed, and effective resolution, into a single number for simple comparison. One of the most widely used FoMs is the Walden FoM (FoM_W) [1] which is based on an empirical relationship

from extensive ADC performance survey data. Walden found a trend from his resolution vs. conversion rate survey that for every doubling conversion rate the resolution decreases by one bit. From this finding, he suggested FoM_W as the follows:

$$FoM_W = \frac{P}{f_s \cdot 2^{ENoB}} \text{ [Joule/conversion·step]} \tag{1.1}$$

where, P is power consumption, f_S is conversion rate, and ENoB is effective number of bits. ENoB is derived from signal to noise and distortion ratio (SNDR) as the following equation.

$$\text{ENoB} = \frac{SNDR - 1.76}{6.02} \tag{1.2}$$

FoM_W well represents the energy efficiency of low resolution ADCs (< 10b) ADCs. Therefore, it is commonly used for low resolution ADCs. However, for noise limited, moderate-to-high resolution ADCs, FoM_W does not captures power and noise tradeoff, which typically requires a quadrupling of power to reduce noise voltage by half for every additional bit of effective resolution [2].

The Schreier FoM (FoM_S), is a widely used FoM, that captures this quadrupling of power per bit tradeoff and formulates it in a logarithmic scale dB [3]. Schreier originally proposed FoM with dynamic range (DR) and bandwidth (BW) of oversampling delta-sigma ADCs as:

$$FoM_{S,DR} = \text{DR (dB)} + 10\log\left(\frac{BW}{P}\right) \text{ [dB]}. \tag{1.3}$$

$FoM_{S,DR}$ well represents the one bit (6.02 dB) increase in dynamic range with a 4× increase in power, resulting in the same energy efficiency. The modified FoM_S [4] is more widely used, which replaces DR with SNDR, and the bandwidth with half of the Nyquist sampling rate (f_s), to compare high resolution Nyquist ADCs and oversampling delta-sigma ADCs.

$$FoM_S = \text{SNDR (dB)} + 10\log\left(\frac{fs/2}{P}\right) \text{ [dB]} \tag{1.4}$$

ADCs performance surveys based on these FoMs from two top international circuit design conferences (i.e. International Solid-State Circuit Conference, and Symposium on VLSI Circuits) [5], [6] show that energy efficiency is clearly improving. For almost two decades, FoM_S of leading edge energy efficient ADCs has improved by about 1dB per year (Figure 1.1). In other words, there has been an energy efficiency improvement of 26% per year. This improvement is achieved through research innovation and engineering optimization.

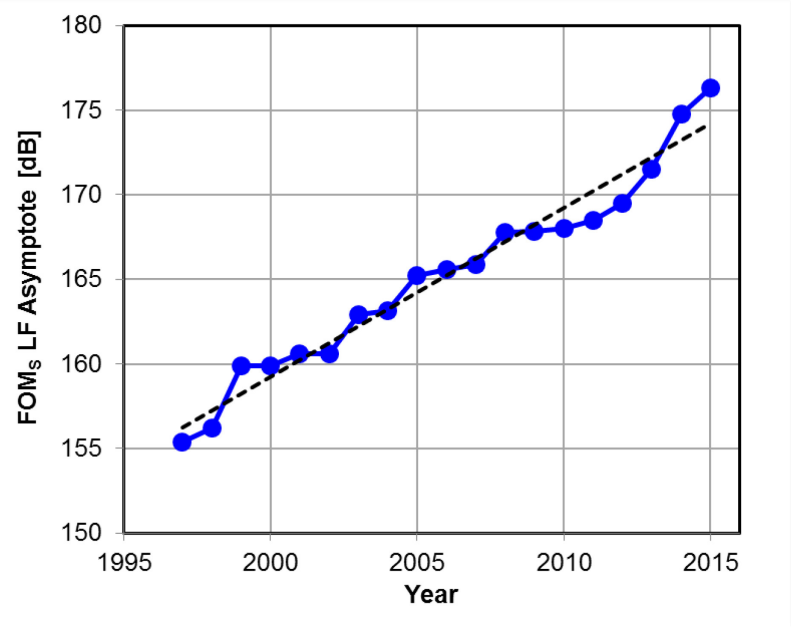

Figure 1.1. FOM_S trend over time (low-frequency asymptote).

The fit line has a slope of about 1 dB per year [6].

1.2 Pipeline ADC Research Trends

Among the various types of ADCs such as flash, pipeline, algorithmic, successive approximation register (SAR), counting or slope, and delta-sigma, the pipeline ADC is a popular architecture since it covers a resolution range from moderate to high resolution (6 to 16b) with wide range of conversion rate (1 MHz to 10 GHz) as shown in the ADC survey chart in Figure 1.2 [5]. This specification range is adequate for many applications including wireless

communications (i.e. CDMA, WCDMA, LTE/4G, and WiFi), digital cameras, camcorders, and ultrasound imaging. Several pipeline ADCs are usually employed in a smart phone. However, the use of operational transconductance amplifiers (OTAs) for switched-capacitor (SC) residue amplification limits energy efficiency since they require high quiescent current for suppressing noise, and satisfying slewing and bandwidth requirements. This dissertation focuses on novel energy efficient OTA replacements for switched-capacitor residue amplifiers.

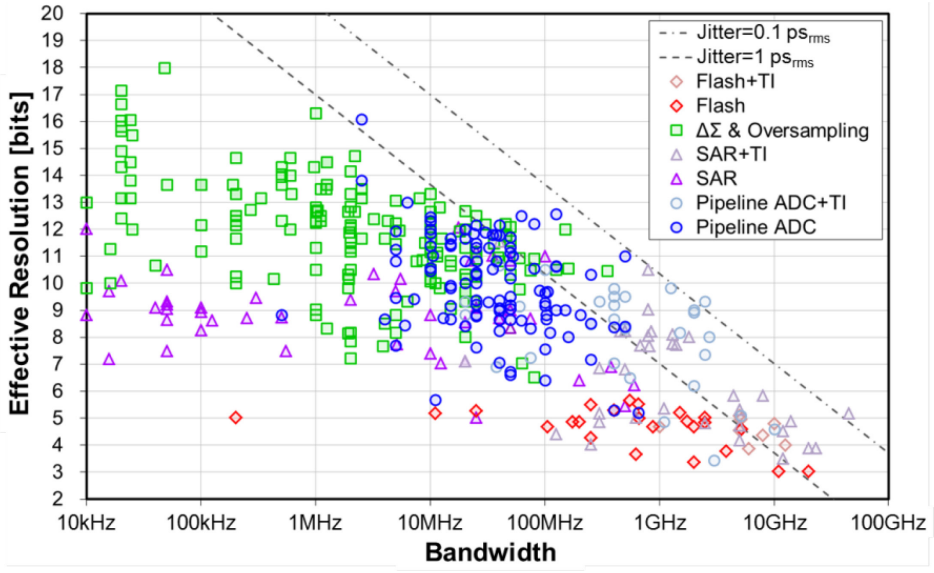

Figure 1.2. Effective resolution vs. bandwidth ADC survey chart. [5]

In order to improve the energy efficiency of pipeline ADCs, researchers have optimized the power consumption of the OTAs in each pipeline stage [7]. Since the noise requirement of a stage is reduced by gain of the previous stage, the power consumption of the OTAs as well as the size of sampling capacitors in a pipeline ADC can be scaled down along the pipeline. In addition, researchers have also optimized the architecture of pipeline ADCs by reducing the number of OTAs used in a pipeline ADC by increasing stage resolution [8], [9]. Increasing stage resolution, especially increasing the resolution of the first stage also reduces non-linearity caused by capacitor mismatch in subsequent stages capacitive digital to analog converter (CDAC).

However, these optimization techniques have limited ability for improving the energy efficiency because they still require a large power consumption for the first stage OTA and there is limit in the scaling power consumption of OTAs in subsequent stages.

Further energy efficiency improvements in pipeline ADC have been made with the switched OTA technique [10], [11] and OTA sharing technique [12]–[15]. These techniques use the fact that the OTA in a pipeline stage has an idle period during the sampling phase of the stage. The switched OTA technique turns off the OTA during the idle phase. However, this technique has the drawback of reduced operating speed since the OTA requires an additional start-up time during every amplification phase. This reduced operating speed can be alleviated by partially turning off the output stage in a multi-stage OTA [11], but this technique trades off the speed and power consumption of the first stage of the OTA during the idle phase. The OTA sharing technique shares an OTA for two or more stages, by using the fact that the pipeline stages work during alternate clock cycles; when even numbered stages are in amplification phase, odd numbered stages are in sampling phase, and vice versa. In other words, one OTA serves as the residue amplifier in two stages during two different clock phases. OTA sharing reduces the number of OTAs by half. However, since an idle period is needed to cancel offset of the OTA by auto-zeroing [16], these techniques can be applied only if the OTA offset is tolerable.

The above energy efficiency improvement techniques depend on conventional OTA SC circuits. However, designing conventional OTAs is getting more difficult with process scaling, since process scaling tends to be more favorable for digital circuits than analog circuits [17]. Process scaling reduces both supply voltage and intrinsic device gain. This means it is getting harder to achieve sufficiently high gain to meet the accuracy requirement of residue generation. The reduced supply voltage makes it hard to use cascode gain boosting since this significantly

reduces the output dynamic range. Multi-stage OTAs can enhance overall OTA gain, but these further increase power, and also require complex compensation schemes [18].

Several alternative approaches have been proposed to overcome the problems of conventional OTA-based SC circuits, including inverter-based SC circuits [19], [20], and zero-crossing-based circuits [21]–[28]. Inverter-based SC circuits have limited accuracy, due to the limited gain of a single inverter, so the application of the inverter-based SC circuits is usually limited to delta-sigma ADCs, which have a relaxed OTA gain requirement. Zero-crossing-based circuits replace the OTA with a comparator (or zero-crossing detector) and current sources, and have the benefit of slew-based charging. Although, the concept of the zero-crossing-based circuit [21] is simple, the non-idealities of the building blocks and the open loop nature of its operation limit gain accuracy. Various techniques tackle these limitations [24]–[28], but these techniques make the zero-crossing more complex and limit efficiency.

Another attractive alternative is the ring amplifier [29]–[32]. The ring amplifier is essentially a stabilized offset-canceled three-stage inverter which has the benefit of slew-based charging. In addition, ring amplifiers have a near rail-to-rail output swing because the output stage is a simple inverter that operates in sub-threshold in steady state. Ring-amplifier-based SC circuits use feedback just as conventional OTA based SC circuits do, and therefore the accuracy depends on the gain of the ring amplifier. The required gain can be relatively easily achieved from three gain stages. Although, the simple structure of the ring amplifier is attractive, the requirement for external bias voltages limits the practicality when we consider PVT variation.

1.3 Research Contributions and Overview

This research presents three novel ring amplifiers, which improve energy efficiency and practicality compared to conventional ring amplifier. Three prototype pipeline ADCs based on the novel ring amplifiers achieve state-of-the-art energy efficiencies. The first novel ring amplifier is a self-biased ring amplifier which makes the ring amplifier simpler, more energy efficient, and more robust to PVT variation by removing the need for external bias voltages, and improving energy efficiency of the first stage inverter. In addition, a comparator-less sub-ADC exploits a unique characteristic of ring amplifiers.

The conventional ring amplifier and the self-biased ring amplifier use a single-ended architecture which suffers from even order harmonics and is susceptible to common mode and supply voltage variation. The use of a pseudo-differential architecture and pseudo-differential common mode feedback (CMFB) can somewhat alleviate these problems; however, the pseudo-differential CMFB reduces effective gain of ring amplifiers. The second novel ring amplifier is a fully-differential ring amplifier which solves the problems of the single-ended and pseudo-differential architectures.

The last novel ring amplifier is a four-stage fully-differential ring amplifier which achieves even higher gain for high resolution pipeline ADCs in deep sub-micron CMOS processes. Furthermore, the noise of a SC residue amplifier is further improved without burning additional power by filtering out the dominant noise source during an auto-zeroing phase.

1.4 Outline of the Dissertation

The rest of this dissertation is organized as follows. Chapter 2 reviews the conventional ring amplifier in depth, and discusses its benefits and limitations. Our approach to the conventional ring amplifier in this chapter is somewhat different to that in the original ring amplifier paper [30] which analyzes it as a zero-crossing based circuit. Chapter 2 analyzes the ring amplifier as a regular amplifier and verifies this analysis with various simulations.

Chapter 3 introduces the self-bias ring amplifier and explains its benefits over the conventional ring amplifier. In addition, an improved auto-zero scheme, and comparator-less sub-ADC technique are also presented. A 10.5b, 100 MS/s prototype pipeline ADC demonstrates the effectiveness of these new techniques.

Chapter 4 introduces the fully-differential ring amplifier and the implementation of a 13b, 50 MS/s SAR-assisted pipeline ADC using it. Furthermore, an improved first-stage SAR CDAC switching technique is presented which improves both the CDAC switching energy efficiency and linearity.

The four-stage fully-differential ring amplifier is presented in Chapter 5, as well as a 15b, 100 MS/s SAR assisted pipeline ADC implementation using it. An auto-zero noise filtering method for the four-stage ring amplifier is also presented for further noise reduction. This does not consume extra power, and is more area efficient than conventional auto-noise reduction techniques. In addition, a systematic mismatch free SAR CDAC layout method is presented. Finally, Chapter 6 summarizes the research contributions.

CHAPTER 2

Review of Conventional Ring Amplifier

2.1 Stabilized Three-Stage Inverter

The ring amplifier is an energy efficient and high output swing alternative to an OTA for use in SC amplifiers [29]–[32]. The ring amplifier is based on an offset-canceled three-inverter stage amplifier as shown in Figure 2.1. A capacitor, C_1 stores the voltage difference between a desired common mode voltage V_{CM} and the trip point voltage of the first inverter. This voltage on C_1 is refreshed during a reset phase. Although a cascade of three inverter stages can achieve high gain, a three-stage inverter amplifier is not stable in a feedback network, such as the SC amplifier shown in Figure 2.1. This is because this amplifier has three poles close in frequency resulting a negative phase margin.

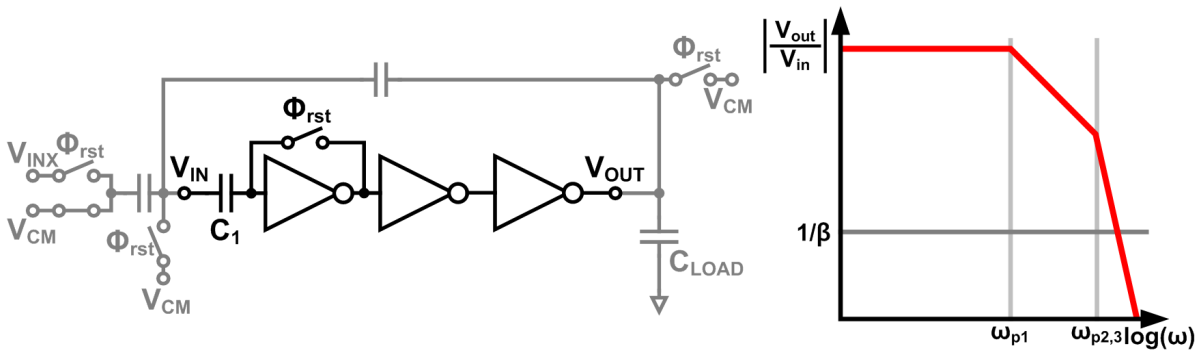

Figure 2.1. An offset canceled three-stage inverter in a SC feedback amplifier configuration and its frequency response.

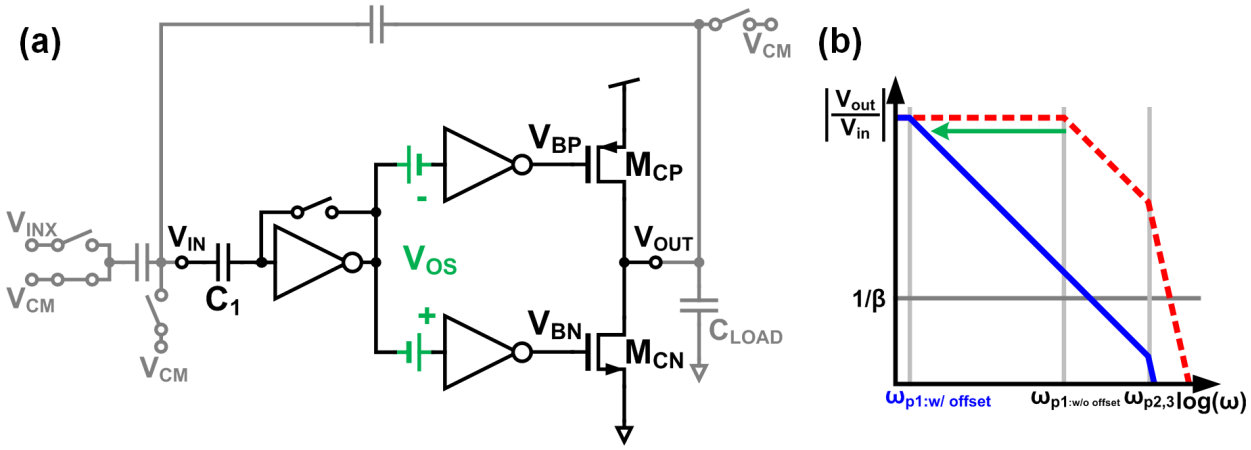

Figure 2.2. Conceptual ring amplifier in a SC feedback amplifier configuration and its frequency response.

In order to stabilize the three inverter stage amplifier, [29]–[31] split the second stage of the amplifier into two separate inverter gain paths, and apply an offset voltage, V_{OS}, at the inputs of these two second stage inverters[1] as shown in the conceptual ring amplifier of Figure 2.2(a). One second-stage inverter drives the gate of the PMOS transistor of the third stage (V_{BP}) while the other drives the gate of the NMOS transistor (V_{BN}). The offset voltages of the two second stage inverters are tuned to bias the third stage transistors, M_{CP} and M_{CN}, in sub-threshold as V_{IN} approaches V_{CM} :

$$V_{BP} > V_{DD} - |V_{th:P}|,\ V_{BN} < V_{th:N} \tag{2.1}$$

In this way, as V_{IN} approaches V_{CM}, the output resistance of the third stage dramatically increases, forming a dominant pole that stabilizes the overall amplifier (Figure 2.2(b)). While settling, this ring amplifier has a high output slewing current. However, when it is settled the

[1] [32] introduces a fine ring amplifier which applies an offset voltage at the output of the second stage inverter, without splitting the second stage inverter, to more precisely control the output stage overdrive voltage. This fine ring amplifier offers a higher gain but a reduced slew rate. The reduced slew rate is overcome by using the ring amplifier in [29]–[31] in parallel with the fine ring amplifier.

current from the output stage, operating in sub-threshold, is negligible. Figure 2.3 shows the conventional, practical implementation of a ring amplifier [29]–[32]. The capacitors, C_2 and C_3, act as the floating bias offset voltage sources in Figure 2.2. An external bias voltage, V_{OS}, sets these capacitor voltages during a reset period.

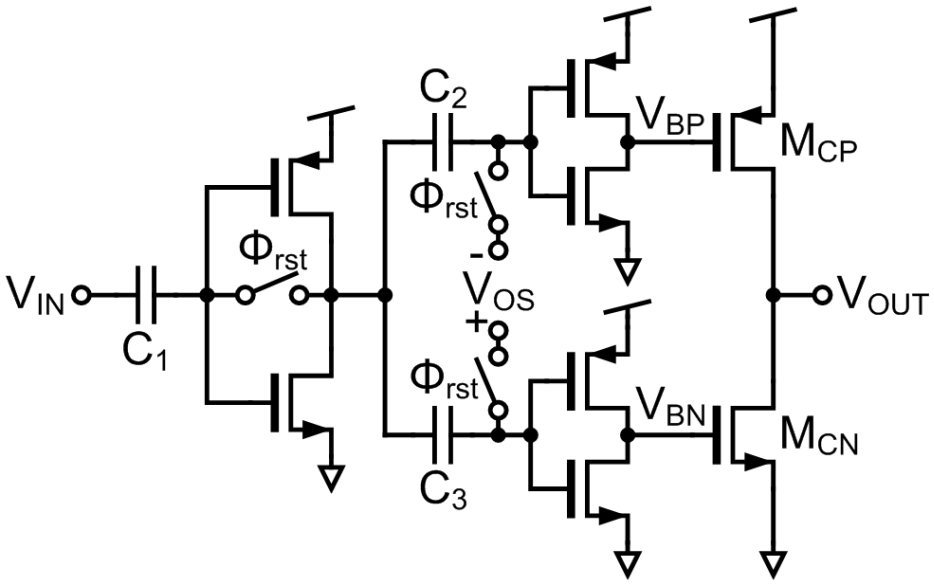

Figure 2.3. Conventional ring amplifier.

2.2 Stability Requirements

A positive small-signal phase margin is a necessary but insufficient condition for stability of the ring amplifier. In fact, a ring amplifier can become unstable due to large signal effects even if there is a positive phase margin. This is because the current of the last stage transistors changes dramatically around the target settling point, making the large signal behavior of the ring amplifier highly nonlinear. As an example, Figure 2.4 shows the simulated large signal behavior of the ring amplifier in the SC amplifier configuration[2], shown in Figure 2.2. In this example, the ring amplifier has phase margin of 73º when V_{IN} is at V_{CM}, but is still unstable.

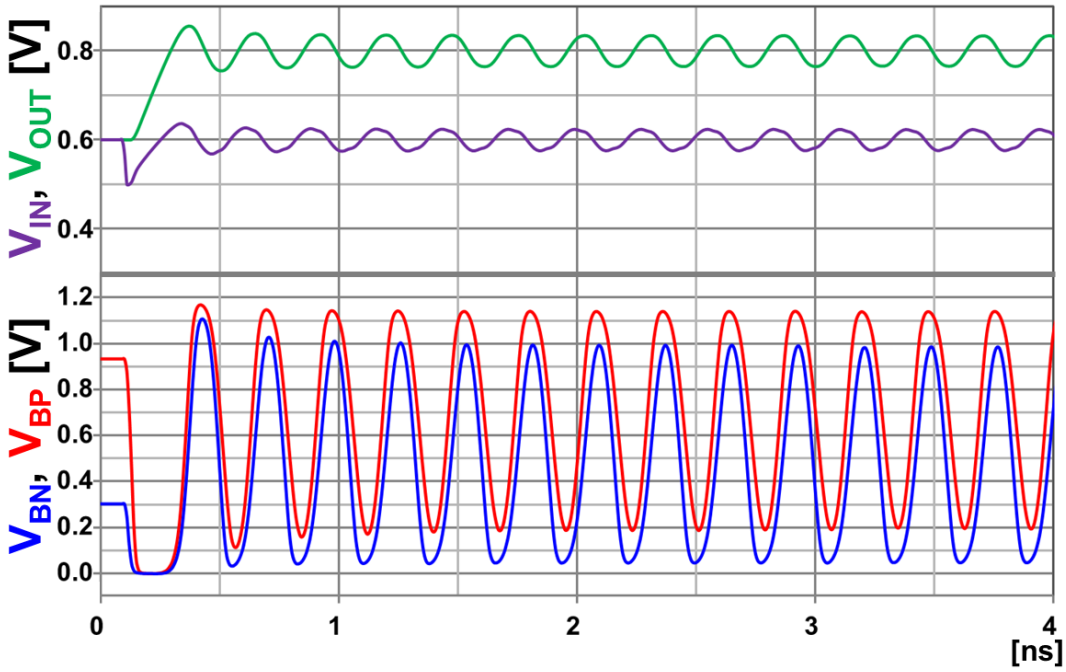

Figure 2.4. Simulated transient response of the ring amplifier of Figure 2.2.

The ring amplifier oscillates even with 73º of positive phase margin.

[2] Ideal switches without charge injection or clock feed-through are used in this simulation for clarity.

The simulation shown in Figure 2.4 begins as the amplifier emerges from the reset phase. If the overall SC amplifier input, V_{INX}, is higher than V_{CM}, the ring amplifier input, V_{IN}, initially falls at the beginning of the amplification phase and the gain of the first and the second inverter stages causes the gate voltages, V_{BP} and V_{BN}, of the last stage PMOS and NMOS transistors to hit ground. In this condition, the PMOS transistor of the last stage strongly conducts so that the output of the ring amplifier, V_{OUT}, slews towards V_{DD} (i.e. 1.2 V in this example). Ideally, this slewing should stop as V_{IN} reaches V_{CM} (i.e. 0.6 V), but here slewing continues and V_{IN} overshoots V_{CM} because the inverters and the feedback path have a finite response time. This V_{IN} overshoot causes V_{BN} and V_{BP} to reach V_{DD}, strongly turning on the NMOS of the last stage and causing V_{OUT} to start slewing down towards ground. If this falling slew rate is similar to the previous rising slew rate, then slewing and overshoot repeat in alternate directions, leading to sustained oscillation.

As seen in this example, the ring amplifier can still oscillate even if there is a substantial positive phase margin. In order to prevent this sustained oscillation, we must configure the circuit so that the overshoot decreases each successive oscillation. The overshoot is proportional to the gain of the three stages, the slew rate, the feedback factor, and the response time. Therefore, reducing the gain of the three stages (Figure 2.5), or reducing the slew rate (Figure 2.6), or reducing the feedback factor (Figure 2.7) can reduce overshoot. Reducing the response time by increasing the bandwidth of the first and the second inverters (Figure 2.8) also reduces the overshoot[3]. The gain and the feedback factor are usually determined by the target application, thus this tuning is best done by reducing the slew rate and increasing the first and second inverter bandwidths. Tuning is a tradeoff between the speed needed for the application and the power consumption.

[3] These observations agree well the equation (8) in [30].

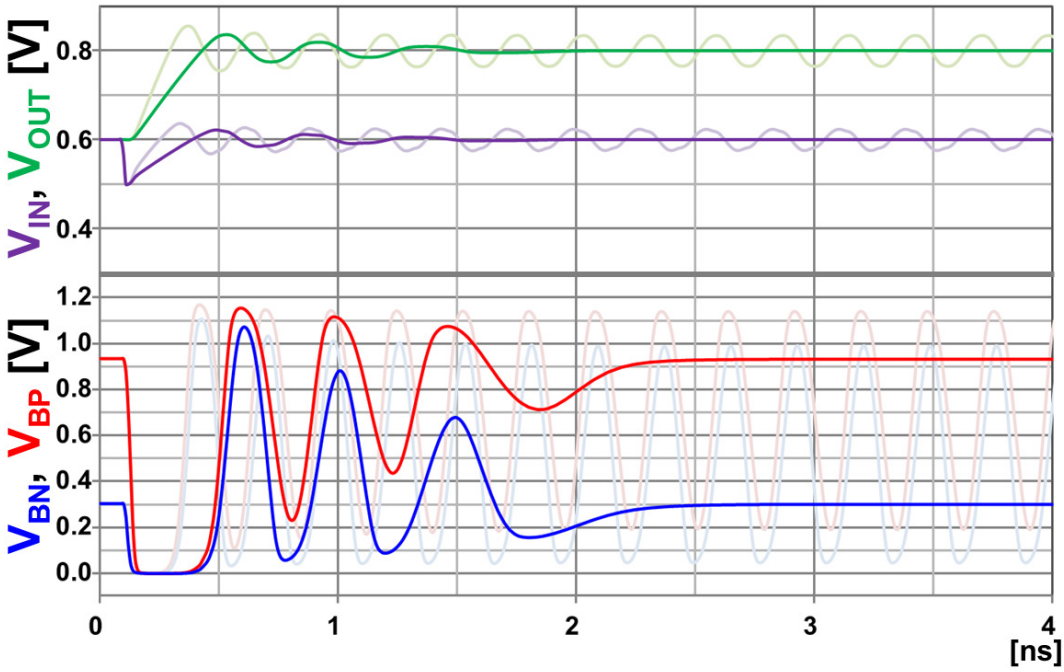

Figure 2.5. Stabilization of the ring amplifier from the simulation result of Figure 2.4 by reducing the first and second stage gain by half.

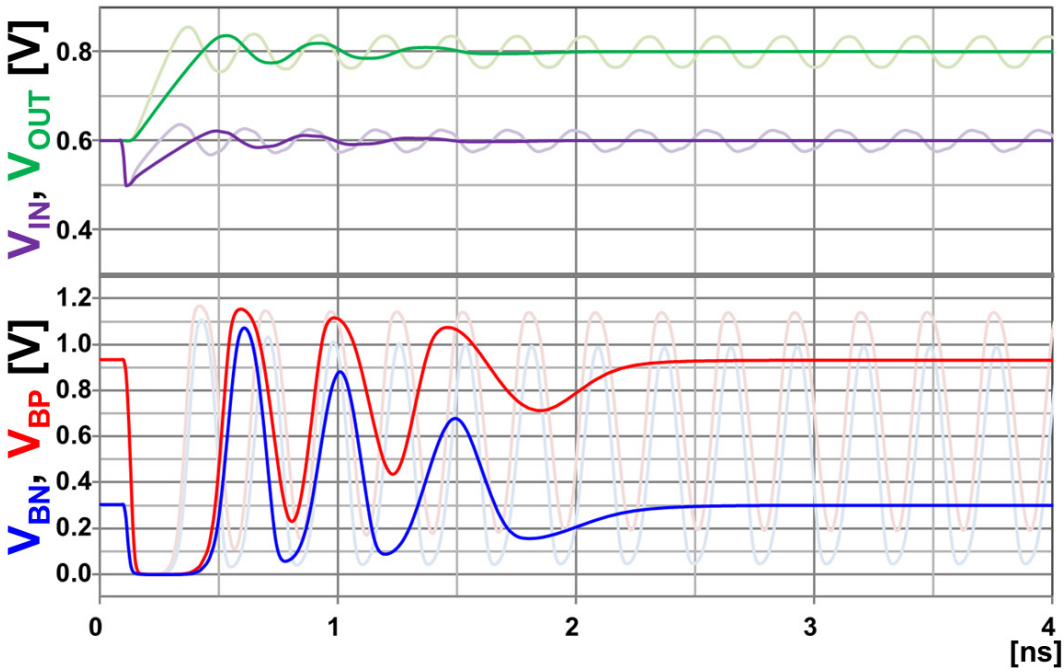

Figure 2.6. Stabilization of the ring amplifier from the simulation result of Figure 2.4 by reducing the slew rate by half.

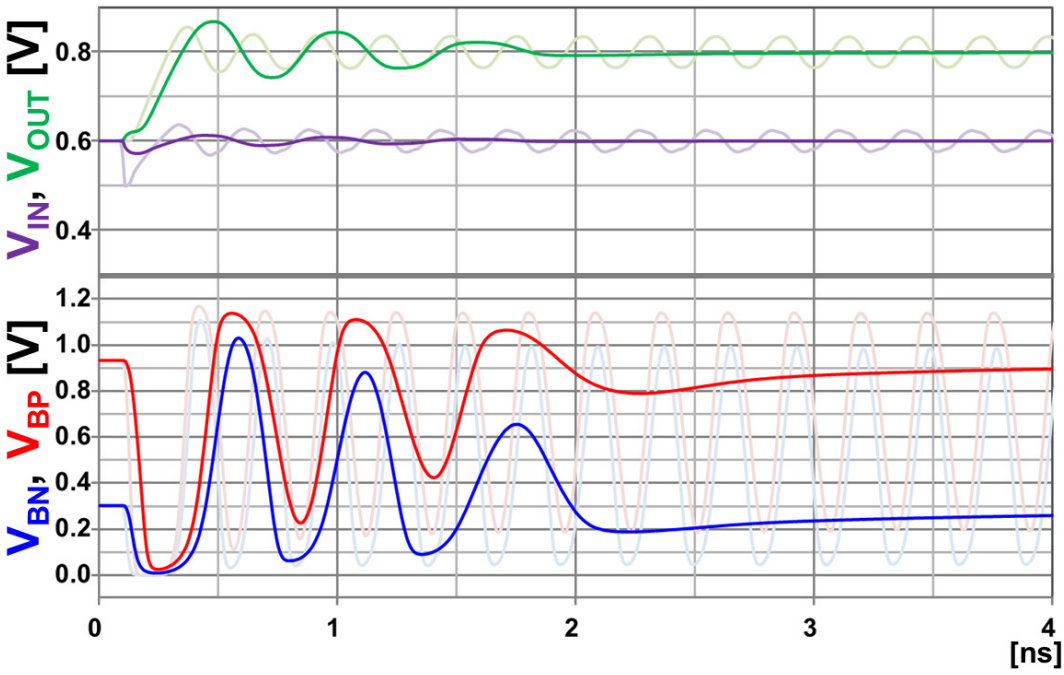

Figure 2.7. Stabilization of the ring amplifier from the simulation result of Figure 2.4 by reducing the feedback factor by half.

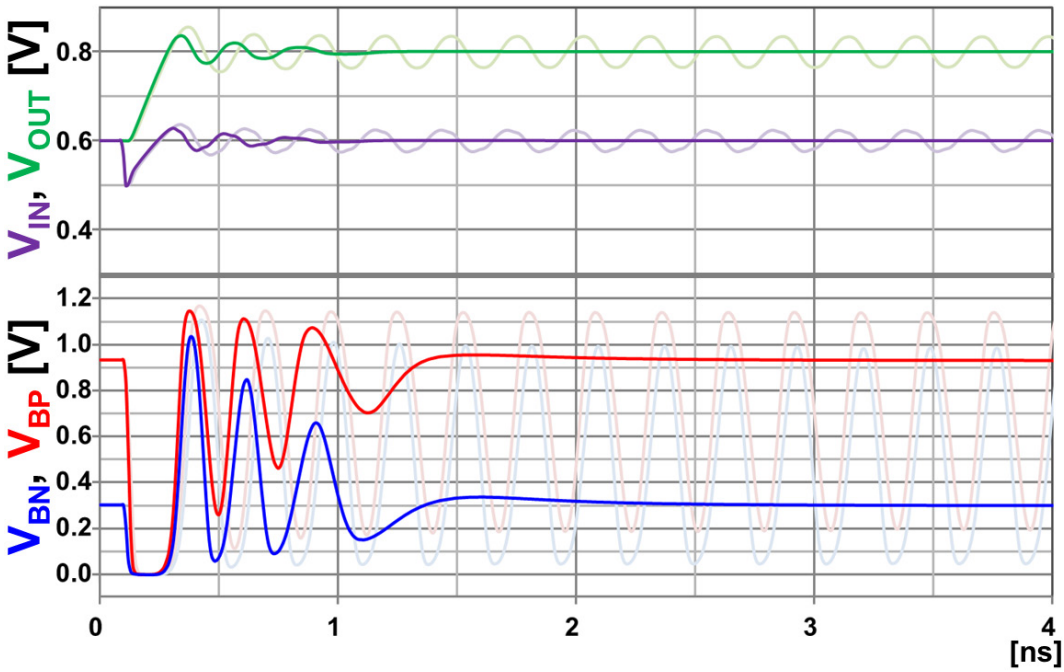

Figure 2.8. Stabilization of the ring amplifier from the simulation result of Figure 2.4 by increasing the first and second stage bandwidth twice.

2.3 Ring Amplifier Gain Considerations

The ring amplifier has high gain, thanks to its three stages. One might argue that the dead-zone voltage (V_{OS} in this chapter) determines the gain of the ring amplifier. Indeed, [30] analyzes the accuracy of the virtual ground (i.e. the inverse of the ring amplifier gain) is defined as $|V_{OS}/A_1|$, where A_1 is the gain of the first stage inverter. The dead-zone approximation is based on the assumption that the last stage transistors become ideal on/off current sources. In practice, all three stages contribute to the gain of the ring amplifier because the last stage still conducts sub-threshold current in steady-state condition and acts as inverter having low bandwidth.

Figure 2.9 plots the simulated ring amplifier small signal gain and effective gain from a SC amplifier configuration versus the embedded offset, V_{OS}. The conceptual ring amplifier in Figure 2.2 (with entire three stage offset cancelation) is used for this simulation. The effective ring amplifier gain is back calculated from the gain error of a SC amplifier. The effective gain is simulated at two different clock frequencies of 10 MHz and 100 MHz to separate the insufficient settling time caused gain error from the gain error due to the finite ring amplifier gain.

As shown in Figure 2.9, the effective gain of the ring amplifier tracks the small signal gain of the ring amplifier when there is a sufficient settling time (i.e. with a slow clock frequency, 10 MHz for this simulation). Here, the gain reduction between the small signal gain and the effective gain is caused by capacitive divider formed by the offset storage capacitor, $C_{C,}$ and the first stage input capacitance and the common mode feedback capacitor. With a faster clock frequency (100 MHz), the effective gain of the ring amplifier drops steeply as V_{OS} increases when V_{OS} is higher than 65 mV. This drop in effective gain is because the bandwidth of the ring amplifier is not sufficient to settle for the given operating frequency, and not because the accuracy is inversely proportional to V_{OS}. The gain of the ring amplifier falls if V_{OS} is increased

over 40 mV because the gain of second stage inverter falls as one of the transistors in the second stage inverter starts operating in the triode region.

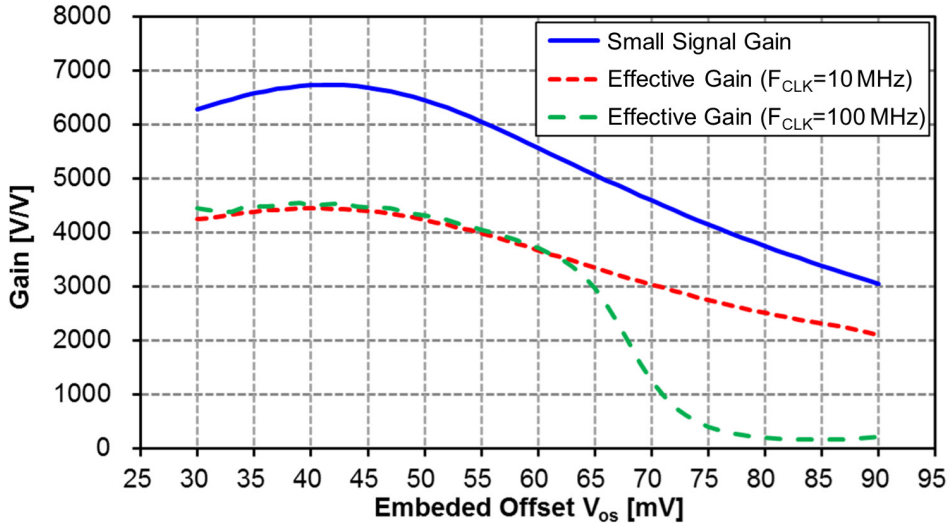

Figure 2.9. Simulated ring amplifier small signal gain and the effective ring amplifier gain calculated from the gain error of a gain stage with various embedded offset voltage V_{OS}.

2.4 Benefits and Limitations of the Conventional Ring Amplifier

The ring amplifier delivers high gain from its three gain stages without the need for complicated gain enhancement techniques. Furthermore, the ring amplifier can slew very efficiently because the third stage inverter acts as a pair of digital switches during slewing. However, the conventional ring amplifier circuit has drawbacks because it depends on the external offset voltage, V_{OS}. The quiescent voltages of V_{BP} and $V_{BN,}$ when V_{IN}=V_{CM}, must be set within narrow voltage windows as illustrated in Figure 2.10. If the quiescent overdrive voltages of the last stage are set too high then the ring amplifier can oscillate because the output resistance of the third inverter stage is never sufficiently large to create a sufficient phase margin. On the other hand, if the quiescent overdrive voltage is too low, the bandwidth of the last stage is

reduced and the ring amplifier might not settle fully within the given settling time. With a low quiescent overdrive voltage, even if the ring amplifier settles in the given settling time, the second stage inverters operate in the triode region resulting in a low overall three-stage gain[4]. Setting V_{OS} for these narrow V_{BP} and V_{BN} voltage windows is difficult when we consider PVT variation of the second and third stage inverters. Furthermore, the common mode of V_{OS} also determines the output common mode voltage of the ring amplifier. The common mode of V_{OS} is amplified by gains of the second and third stages to set the output common mode voltage. This is also affected by PVT variation making it difficult to set the output common mode within a certain range. Some of the PVT variation issue can be solved by using on-chip biases that track PVT variation [16]. However we still need to consider the device to device variation which can cause large output common mode variation. The device to device variation is particularly problematic since the ring amplifier uses almost minimum sized transistors [31].

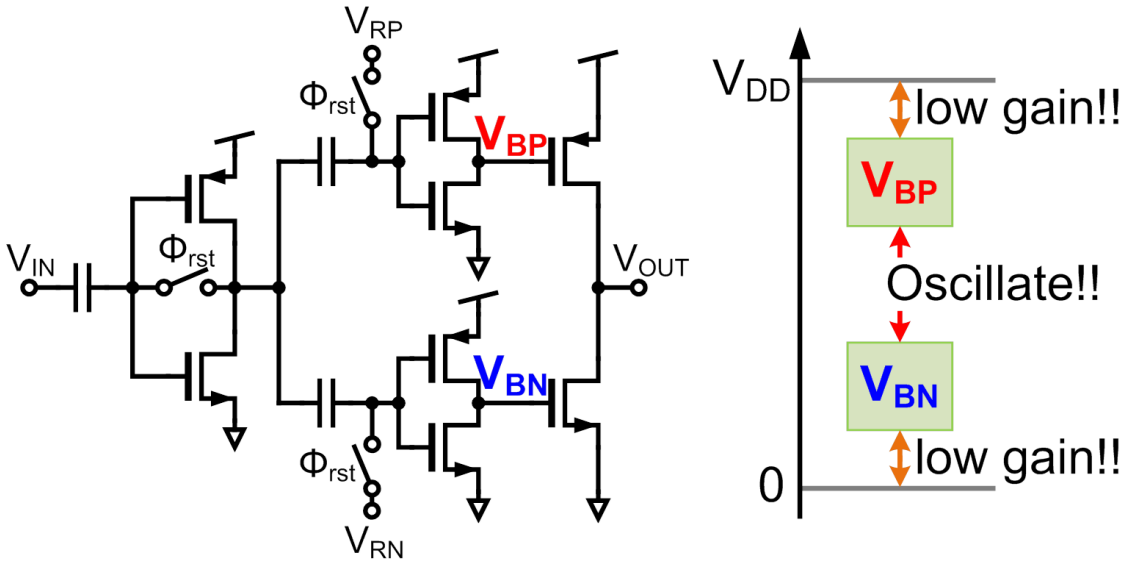

Figure 2.10. The third stage quiescent offset voltage range of the conventional ring amplifier.

[4] This low second stage gain can be avoided by applying the offset voltage at the output of the second stage inverter without using two second-stage inverters [32]. However this reduces the offset voltage setting accuracy since the sampled offset leaks through parasitic diodes of the switches because the voltages of offset sampling capacitors exceed the rails during slewing - the amount of leakage depends on slewing time.

CHAPTER 3

A Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers

3.1 Self-Biased Ring Amplifier

In this section, we introduce the new self-biased ring amplifier and explain its benefits. We adopt high threshold devices for the last stage inverter to extend the stable offset (V_{OS}) range. We also eliminate the external biases and the split second stage inverter. We dynamically apply an offset using a resistor in the second stage to make the ring amplifier more practical and power efficient.

3.1.1 Introducing High Threshold Device for the Last Stage

We introduce high threshold devices in the third stage of the ring amplifier to take advantage of their higher output resistance. Because we can get orders of magnitude higher output resistance from the high threshold voltage device inverter[5], we can extend the V_{OS} range

[5] This also reduces the slewing current of the ring amplifier. However, for same sized last stage transistors, the output resistance in steady state is two to three orders of magnitude higher while the slewing current is reduced by a half to a quarter. Therefore, the use of high threshold voltage devices for the last stage is beneficial although we need to increase the size of the last stage to make the slewing current the same.

(or the range quiescent overdrive voltages V_{BP} and V_{BN}) as illustrated in Figure 3.1. This extended V_{OS} range increases the robustness of the ring amplifier to PVT variation.

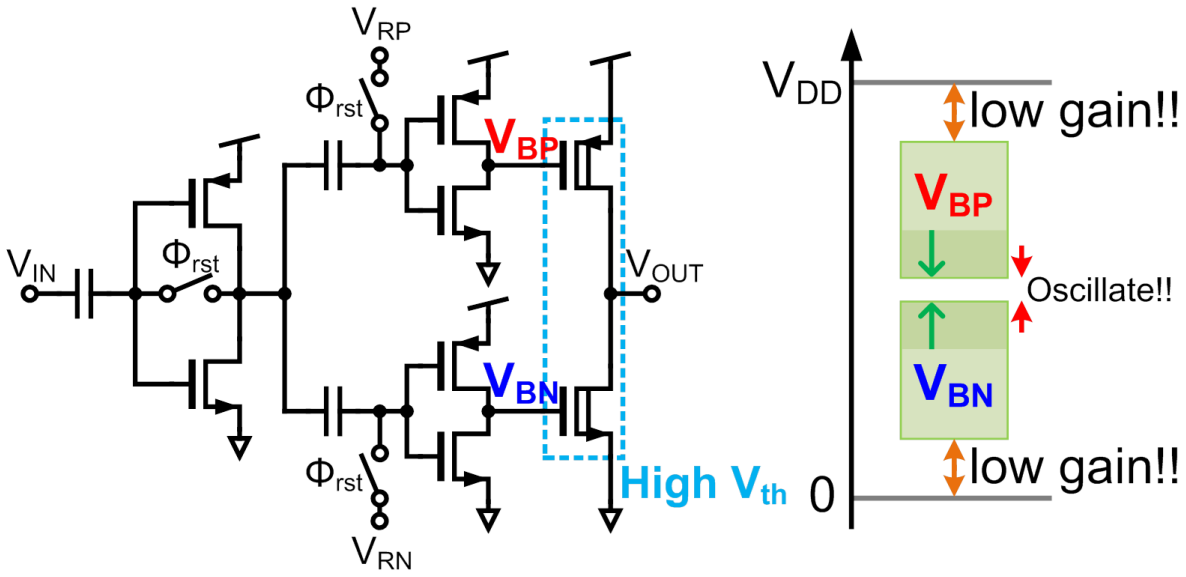

Figure 3.1. Modified ring amplifier with high V_{TH} last stage and the third stage quiescent offset voltage range of the ring amplifier.

3.1.2 Ring Amplifier without Offset Biasing

Adopting high threshold devices for the last stage allows us to stabilize a three-inverter stage amplifier without the split second stage and offsets, as shown in Figure 3.2. When the sum of threshold voltages of transistors in the third stage inverter is higher than the power supply voltage (i.e. $V_{TH:N}+|V_{TH:P}| > V_{DD}$), then third stage operates in the sub-threshold region. The three-stage inverter is stabilized since the third stage forms a dominant pole due to the significantly higher output resistance from the sub-threshold operation. This simple three-stage ring amplifier has two advantages compared to the conventional ring amplifier. Firstly, the reduced number of second stage inverters, together with the removal of the offset capacitors and the switches, reduces the loading on the first stage, allowing us to reduce the power consumption of the first inverter while maintaining the same first stage bandwidth. Secondly, we can auto-zero

the entire three inverter stages as in Figure 3.2 and this gives us a more stable output common mode even with PVT variation, and the device to device variation. However, this simplified offset-less ring amplifier is not practical because the power supply voltage condition ($V_{TH:N}+|V_{TH:P}| > V_{DD}$) is not always true.

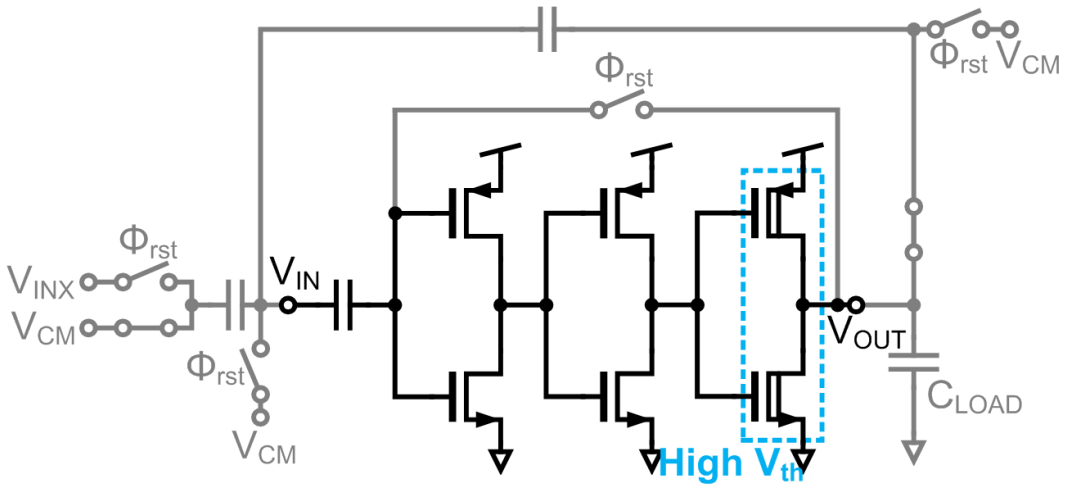

Figure 3.2. Offset-less ring amplifier. This can be stabilized when the sum of the last stage inverter transistors threshold voltage is higher than the power supply voltage.

3.1.3 Dynamic Offset Using Resistor in the Second Stage Inverter

In order to avoid these constraints on the power supply voltage, while keeping the advantages of a single inverter-based second stage without external biases, we embed a polysilicon resistor, R_B, between the drains of the NMOS and PMOS transistors of the second-stage inverter, as shown in Figure 3.3. The resistor R_B dynamically applies an offset to gate voltages, V_{CP} and V_{CN}, of the third stage inverter transistor thanks to the IR drop due to the inverter short circuit current. There is now a voltage offset between the gates of the last stage PMOS and NMOS transistors when V_{in} is close to the virtual ground. As we can see in Figure 3.4, the second inverter still drives the last stage rail-to-rail when the ring amplifier input, V_{in}, is away from the virtual ground. The offset voltage variation caused by the R_B resistance variation

and the second inverter short circuit current variation is acceptable as long as it is within the stable V_{OS} range. As explained in sub-section 3.1.1, the acceptable V_{OS} range is extended by using high threshold device in the last stage. This increases the design margin for offset voltage variation.

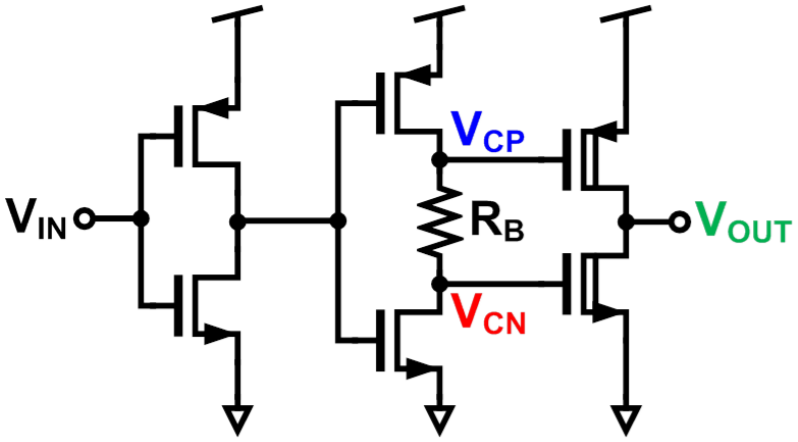

Figure 3.3. Ring amplifier with dynamic offset using a resistor R_B.

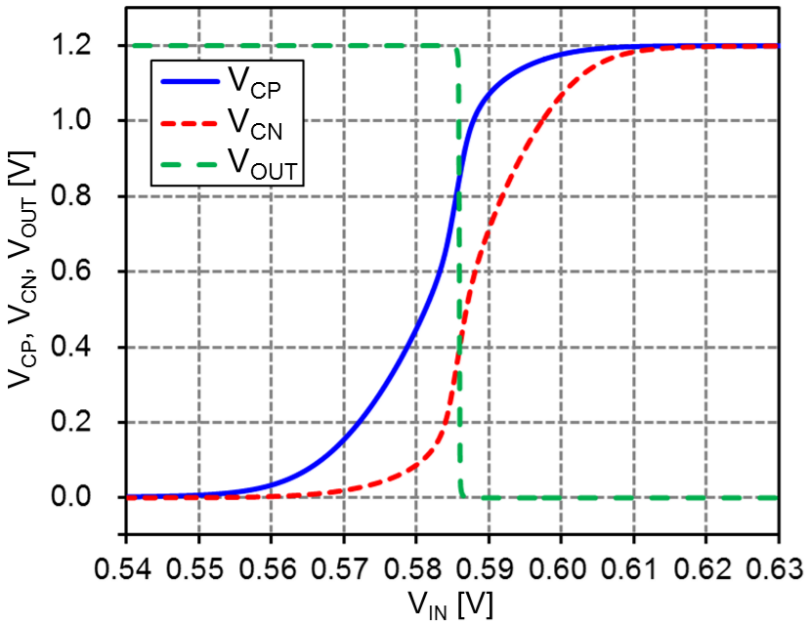

Figure 3.4. Dynamic offset DC response.

This resistor based dynamic offset ring amplifier has another benefit. Since the offset depends on the short circuit current of the second stage inverter, this offset tracks the power supply voltage. This means the ring amplifier with dynamic offset biasing can operate over a wider V_{DD} range. The short circuit current of the second-stage inverter can be calculated from the NMOS saturation region square law equation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}\left(\frac{V_{DD}}{2} - V_{TH:N}\right)^2 \tag{3.1}$$

This assumes that the second inverter is balanced so that the trip point of the second inverter is $V_{DD}/2$. As shown in equation (3.1), the inverter current increases quadratically as V_{DD} increases and therefore the voltage across R_B also increases quadratically. Ideally, the offset voltage should linearly track[6] V_{DD} to maintain the same overdrive voltage on the last stage transistors regardless of V_{DD}. Nevertheless, the increase in IR drop with V_{DD} along with the extended offset range facilitated by the high threshold voltages of the last stage ensures a wide V_{DD} operating range.

3.1.4 Noise and Power Optimization

We optimize the noise and the power consumption of the first stage inverter. The first stage inverter is the dominant noise source of the dynamic offset ring amplifier in Figure 3.3. Although flicker noise is mostly removed by the auto-zeroing [16], thermal noise cannot be cancelled. Since the thermal noise of an inverter is inversely proportional to the g_m of the inverter, we must increase g_m to reduce the thermal noise. For a given length and for a fixed gain, the only way to increase the g_m of an inverter is to increase the width of the inverter. However, increasing the width also increases the power consumption.

[6] This can be achieved by using triode mode N/PMOS resistors instead of a poly resistor. However the use of triode mode transistors also increases the loading capacitance of the second stage and therefore also the power consumption of the ring amplifier.

If we also adjust the power supply voltage of the first inverter then we do not have to significantly increase power consumption to reduce the thermal noise. In fact, we can get a higher g_m for a given quiescent current, I_D, from an inverter when we reduce the power supply voltage. Since the g_m of a MOS transistor is $2I_D/(V_{GS}-V_{TH})$ when we assume strong inversion operation, then assuming the trip point of the inverter is $V_{DD}/2$, we get g_m/I_D of an inverter as:

$$\frac{g_m}{I_D} = \frac{2}{\left(\frac{V_{DD}}{2} - V_{TH:N}\right)} + \frac{2}{\left(\frac{V_{DD}}{2} - |V_{TH:P}|\right)}. \tag{3.2}$$

Equation (3.2) shows that g_m/I_D of an inverter increases as we decrease V_{DD}.

Figure 3.5 shows the simulated g_m and bandwidth of the first stage inverter at the trip point versus the first stage inverter V_{DD} ($V_{DD:inv1}$). The short circuit current of the first stage inverter is fixed in this simulation by changing the width of the inverter. We can get a close to maximum bandwidth with about 2.8 times higher g_m compared with the default power supply (1.2 V) when $V_{DD:inv1}$ is around 0.85 V. As we see from the simulation, we can get optimum g_m and bandwidth with a lower $V_{DD:inv1}$ which allows us to reduce the thermal noise of the first stage inverter without significantly increasing power consumption.

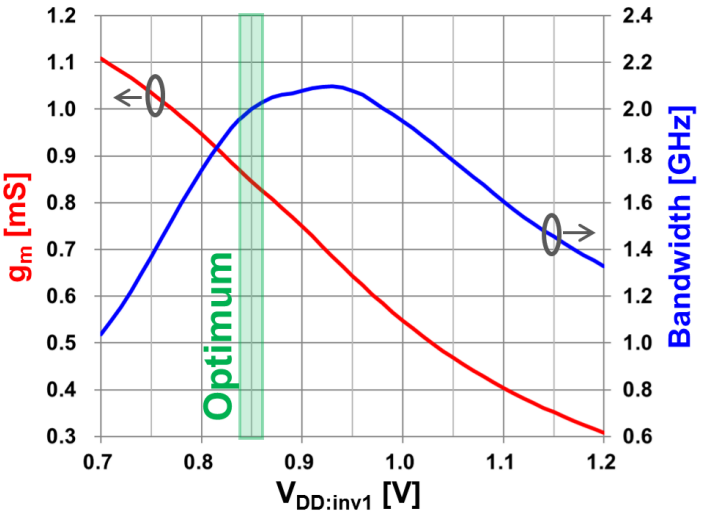

Figure 3.5. Simulated first stage bandwidth and transconductance versus first stage power supply voltage ($V_{DD:inv1}$) with fixed stage current.

Instead of using an external voltage, we lower $V_{DD:inv1}$ using a diode-connected NMOS (M_{NR}) as shown in Figure 3.6. The diode connected M_{NR} works as an internal regulator and effectively lowers the power supply voltage of the first stage inverter without additional power consumption. The size of M_{NR} needs to be large to reduce the regulated voltage variation. Figure 3.6 shows the final structure of the self-biased ring amplifier.

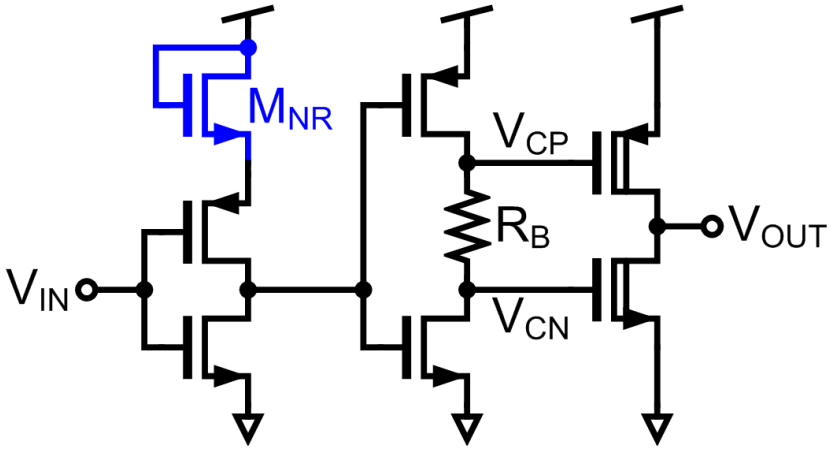

Figure 3.6. Self-biased ring amplifier.

3.2 Ring Amplifier Auto-Zero

As discussed in the previous section, unlike the conventional ring amplifier, which only cancels the offset of the first stage, we auto-zero the entire input offset of the self-biased ring amplifier. The auto-zeroing is required to cancel the difference between V_{CM} and the input common voltage of the ring amplifier. This also removes the output offset of the ring amplifier, unlike the conventional ring amplifiers [29]–[32], and this helps maximize the usable dynamic range of the output swing. In this section, we explain the problems of auto-zeroing the ring amplifier in a flip-around 1.5b multiplying digital to analog converter (MDAC) gain stage (Figure 3.7), and introduce a new scheme that overcomes these problems.

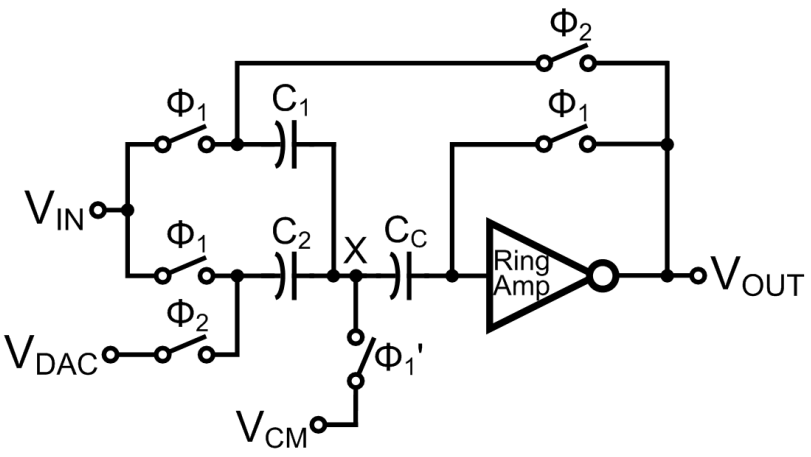

Figure 3.7. Auto-zeroed flip-around 1.5b MDAC gain stage using a ring amplifier.

3.2.1 Stability during Auto-Zero

We first consider stability during the auto-zero. When Φ_1 is high (i.e. the sampling/auto-zeroing phase) the MDAC stage in Figure 3.7 samples the input, V_{in}, onto the sampling capacitors C_1 and C_2, and at the same time samples the offset of the ring amplifier on the offset sampling capacitor, C_C. Then, when Φ_2 is high (the amplification phase), the MDAC stage amplifies the sampled voltage by transferring the sampled input charge to C_1 capacitor. During the amplification phase, the ring amplifier sees the sampling capacitors of the next pipeline stage as the load capacitance. In addition, the feedback factor during the amplification phase is about a half. However, during the sampling/auto-zeroing phase, the offset sampling capacitor, C_C, is the only load, and also the feedback factor increases to about one. The increased feedback factor and the reduced load capacitance (i.e. assuming $C_C < C_1+C_2$) during the auto-zero phase make the ring amplifier hard to stabilize because these reduce the phase margin. It is possible to design a ring amplifier that is stable during auto-zeroing with this condition, but this requires higher power consumption than that required for the amplification phase. If C_C is equal to C_1 and C_2, then to stabilize the ring amplifier during the auto-zero phase, the second and third poles of the

ring amplifier need to be four times higher than that required to stabilize it during the amplification phase. This requires at least four times higher power for the first and second inverters.

One approach to improving stability during the sampling/auto-zeroing phase without using more power is to increase the C_C capacitance, but this is not desirable for moderate resolution ADCs where the auto-zero related noise is not dominant. In order to stabilize the ring amplifier during auto-zero, and considering the twice larger feedback factor, C_C needs to be at least twice as large as sampling capacitance of the next stage ($C_C > 2(C_1+C_2)$). However, that would require a large area since C_C should be a floating capacitor and floating capacitors such as metal-insulator-metal (MIM) or metal-oxide-metal (MOM) have a relatively low per unit area capacitance. A high density MOS capacitor can be used for C_C, but a MOS capacitor has a relative large bottom plate parasitic capacitance. The large bottom plate parasitic capacitance of C_C on the virtual ground node X increases the gain error during the amplification [33] because the bottom plate capacitance of C_C steals some of the sampled signal charge due to the imperfect virtual ground.

Instead of using a large C_C, we periodically add a loading capacitor C_{LA}, as shown in Figure 3.8. C_{LA} is connected to the output of the ring amplifier during the auto-zero phase, but not during the amplification phase. The sum of C_C and C_{LA} needs to be at least twice as large as the next stage sampling capacitors (i.e. $C_C+C_{LA} > 2(C_1+C_2)$). However, the use of a large C_{LA} does not require much area because we can use a high per unit area capacitance MOS capacitor, since one terminal of C_{LA} is always connected to ground. In addition, the addition of C_{LA} does not increase power consumption since the sampled offset voltage on C_{LA} stays constant in every cycle.

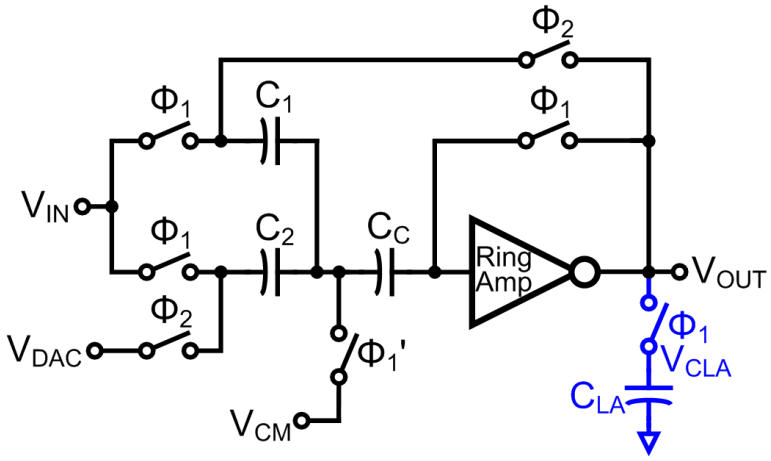

Figure 3.8. Auto-zeroed flip-around 1.5b MDAC gain stage using a ring amplifier with stabilization loading capacitor C_{LA}.

3.2.2 Improved Auto-Zero Switch to Eliminate Gain Error

Another important consideration is the gain error due to the parasitic capacitance across the auto-zero switch. As shown in Figure 3.9, the source-drain parasitic capacitance, C_{SD}, of a conventional auto-zero switch scheme causes a gain error during the amplification phase. As the ring amplifier output voltage, V_{OUT}, moves during the amplification phase, C_{SD} steals (or injects) charge from (or to) the C_C capacitor and this also changes the sampled input charge in the sampling capacitors, C_1 and C_2. In addition, the change in charge on C_C also moves the virtual ground voltage, V_X, from V_{CM}, which also causes a gain error. The gain of the MDAC gain stage in Figure 3.9 including the gain error caused by C_{SD} can be calculated as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{1+\left(\frac{1}{C}+\frac{2}{C_C}\right)C_{SD}}. \tag{3.3}$$

where C_1 and C_2 have the same value C, V_{DAC} is equal to V_{CM}, and we assume the ring amplifier has infinite gain and zero offset for simplicity. As we can see from the equation, C_{SD} is problematic for gain accuracy.

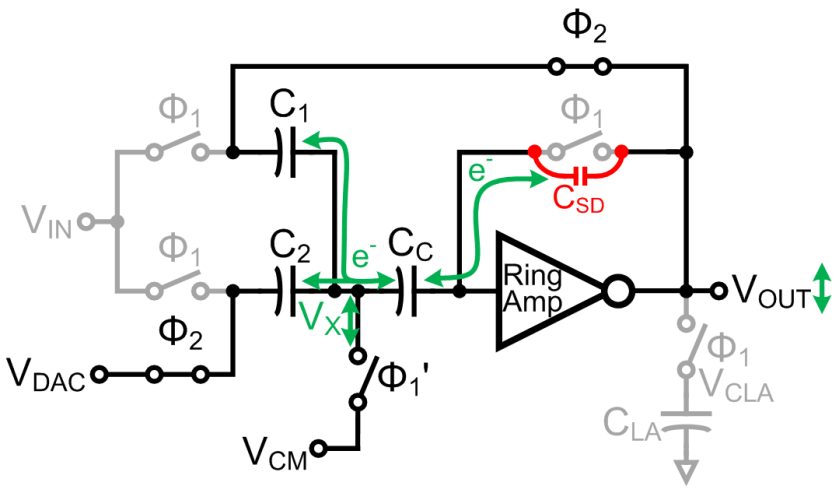

Figure 3.9. Gain error mechanism due to the parasitic capacitance of the auto-zero switch.

One way to reduce this gain error is to minimize C_{SD} using layout techniques. For example, we can minimize C_{SD} by extending the distance between the source and drain of the auto-zero switch, or by adding a shield in between. However, we cannot completely eliminate this gain error because C_{SD} still exists due to the electrical field in the substrate and we cannot completely shield over the gate poly.

We introduce an improved auto-zero switch, as shown in Figure 3.10, to eliminate the C_{SD} related gain error. This improved auto-zero scheme makes use of the sampled ring amplifier offset voltage, V_{CLA}, stored on $C_{LA,}$ which we already use to stabilize the ring amplifier during the auto-zero phase. During the auto-zero phase, the scheme works in the same way as a conventional auto-zero by turning on the switches S_{AZ1} and $S_{AZ2,}$ and turning off the switch S_{AZ3}. During the amplification phase, S_{AZ1} and S_{AZ2} are turned off and S_{AZ3} connects the intermediate auto-zero switch voltage, V_{AZ}, to the sampled offset voltage, V_{CLA}, which effectively grounds C_{SD} to V_{CLA}. In this way, C_{SD} no longer affects the charge on the other capacitors, even as V_{OUT} moves.

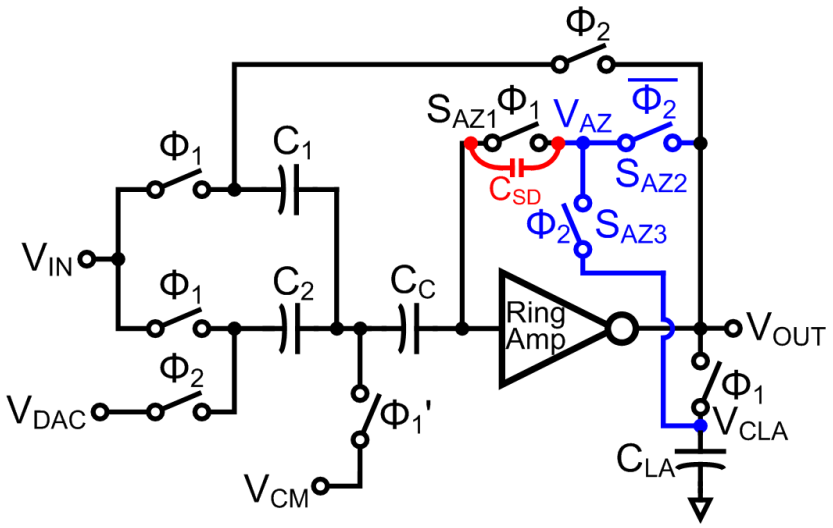

Figure 3.10. An improved auto-zero switch that is free from C_{SD} related gain error.

3.3 Comparator-Less Sub-ADC Using Ring Amplifier

We introduce a comparator-less MDAC stage that uses the self-biased ring amplifiers as comparators by exploiting a unique characteristic of the ring amplifier. As discussed in CHAPTER 2, during the amplification phase, the second stage outputs reach ground when the ring amplifier output slews up, and the second stage outputs reach V_{DD} when the ring amplifier output slews down. In other words, the second stage output voltage indicates the amplification direction during ring amplifier output slewing. In fact, the first two stages of the ring amplifier work as an offset canceled continuous time comparator at the beginning of the amplification as a byproduct of the slow response of the last stage. We can use this amplification direction information as the next stage MDAC sub-ADC decision. This allows us to further reduce the power consumption of a ring amplifier based pipeline ADC by eliminating dedicated clocked comparators for the sub-ADCs.

In order to properly use this direction information from the ring amplifier, we first ensure the amplification always starts from V_{CM}. To ensure this, we reset the sampling capacitors C_1 and

C_2 using a short pulse Φ_{1R} before the sampling phase, as shown in Figure 3.11. This resetting operation also reduces the maximum slew requirement by half, which allows us to further reduce the ring amplifier power consumption for the same operating speed.

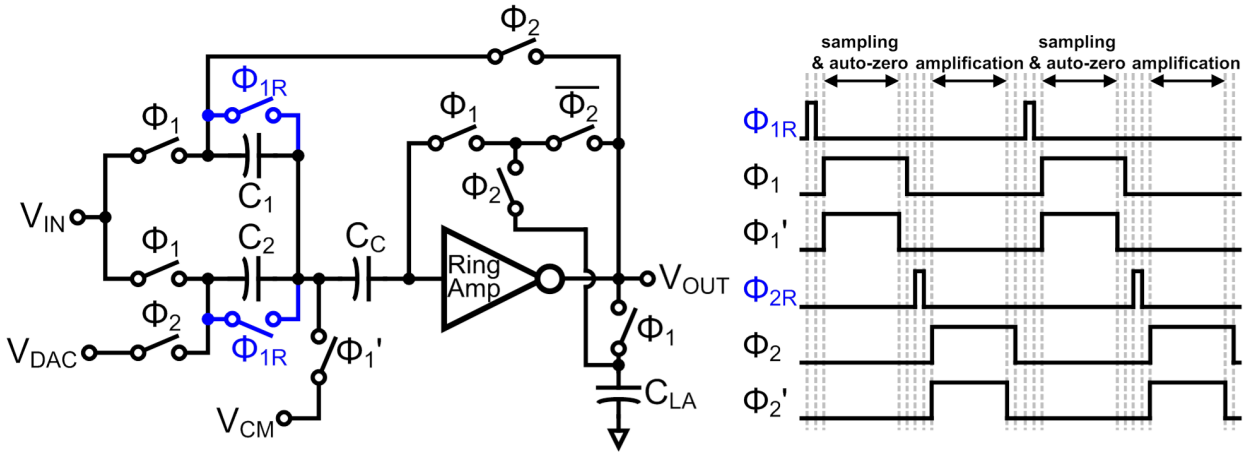

Figure 3.11. Modification of the ring amplifier MDAC to use the amplification direction information.

We can sample the amplification direction from the second stage output V_{CP} of the self-biased ring amplifier (Figure 3.6) by using a minimum sized NOR gate and a set-reset (SR) latch as in Figure 3.12. The latch consists of weak back-to-back inverters, and pull-down set-reset NMOS transistors. The latch can be set or reset by turning on only one of the pull down transistors. Figure 3.13 shows a simulation of the MDAC gain stage (Figure 3.11) with the direction sampling circuit for various input voltages. The NOR gate inverts V_{CP} during the amplification phase and outputs 0 during the sampling phase. The supply voltage of the NOR gate is reduced by a diode connected NMOS transistor in order to reduce the logic threshold voltage of the gate. This helps to get the correct NOR trip-point for the direction sampling and prevents unwanted short circuit current after the ring amplifier slewing due to the lower than V_{DD} quiescent voltage of V_{CP}. The SR latch is reset right before the amplification phase and samples

the amplified direction information from the NOR gate output V_{DIR}. We can use the latch output, Q, as the next MDAC stage sub-ADC result. A similar circuit samples the opposite direction information from the opposite side of the MDAC pseudo-differential stage. The simple decoding circuit in Figure 3.14 decodes the two direction information bits (Q+ and Q-) to provide the 1.5b sub-ADC result for the next stage.

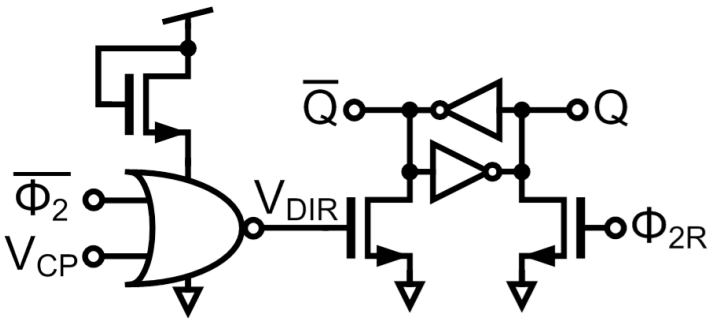

Figure 3.12. Amplification direction sampling circuit.

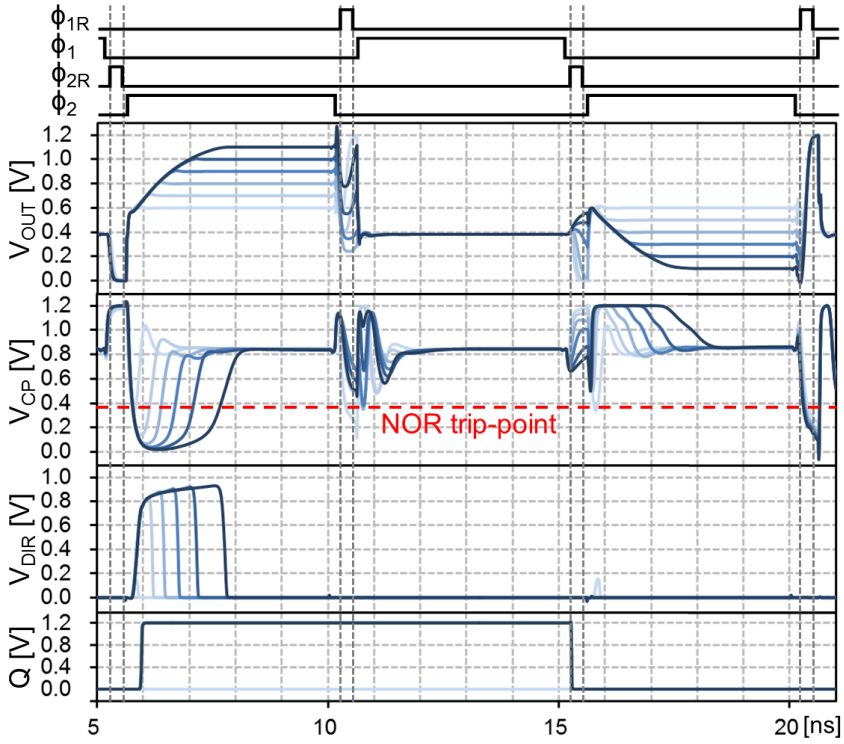

Figure 3.13. Simulation of the MDAC gain stage in Figure 3.11 with the amplification direction sampling circuit in Figure 3.12 for various input voltages.

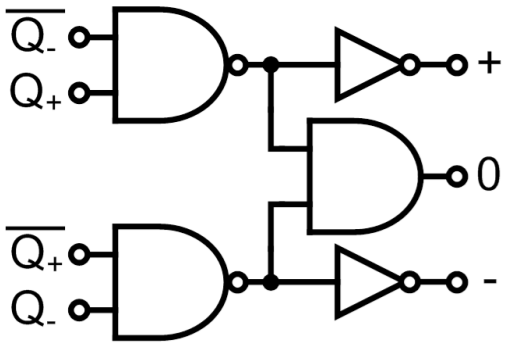

Figure 3.14. Amplification direction information to 1.5b sub-ADC result decode logic. Q_+ and Q_- are from each side of the pseudo-differential ring amplifier MDAC gain stages.

The auto-zero ensures the correct amplification direction even with PVT variation, while the NOR trip-point and the ring amplifier slew rate define the threshold of the direction sampling. The direction sampling threshold voltage tends to be close to V_{CM} because V_{CP} drops near ground for even slightly positive V_{OUT} slewing and the slew is tuned to be slow (about half of amplification period for maximum swing) for better power efficiency. Therefore, even with some PVT variation, the thresholds are well within the redundancy ($\pm 1/2V_{ref}$) of the 1.5b/stage pipeline ADC.

3.4 ADC Implementation and Measured Results

A 100 MS/s, 1.5b/stage 10.5b pipeline ADC [34] is implemented as a proof of the concept prototype to demonstrate the effectiveness of the self-biased ring amplifier. As shown in Figure 3.15, the ADC is composed of a flip-around sample and hold amplifier (SHA) [9], [35] with the bootstrapping input switches [36], nine 1.5b flip-around MDAC stages, and dummy loading for the last stage. Figure 3.16 and Figure 3.17 show the pseudo-differential ring amplifier based flip-around SHA and MDAC gain stage used in the ADC. The pseudo-differential CMFB in [29] is

implemented for all stages. The SHA also works as the first MDAC 1.5b sub-ADC[7]. To further optimize the power efficiency, the seven last MDAC stages are scaled down by half compared to the first two MDAC stages. Identical self-biased ring amplifiers are used for the SHA and for the first two MDACs. The SHA uses a sampling capacitance (C_S) of 400 fF and the first two MDAC stages use sampling capacitors (C_1, C_2) of 200 fF. The SHA and the first two MDAC stages use 200 fF offset storage capacitors (C_C). The ring amplifiers used in the seven last MDAC stages use half width transistors and a doubled resistance R_B when compared with the ring amplifier of the first two MDAC stages. R_B is doubled to generate the same bias voltages, V_{CP} and V_{CN}, as the first two stages with half the inverter short-circuit current.

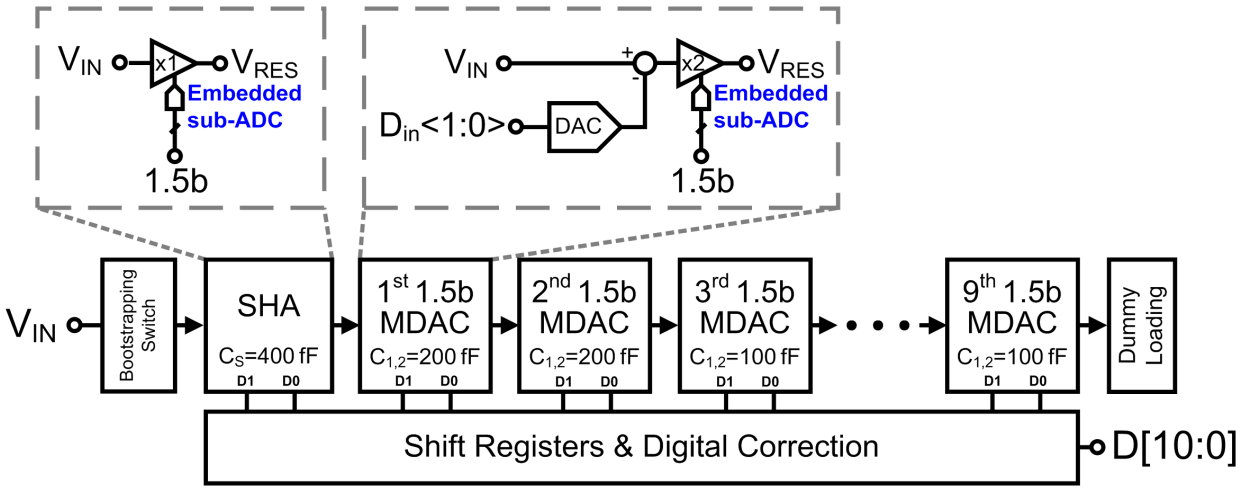

Figure 3.15. Prototype ADC structure.

[7] We implement the SHA in this ADC to demonstrate a completely comparator-less pipeline ADC. We can eliminate SHA as in [31] if we use a conventional flash ADC for the first stage sub-ADC. The elimination of SHA also improves SNR and power efficiency of the ADC since the SHA adds noise to the sampled input signal without providing amplification. From a power consumption point of view, it is better to use this ring amplifier based comparator-less MDAC for all stages except the first stage sub-ADC for better energy efficiency.

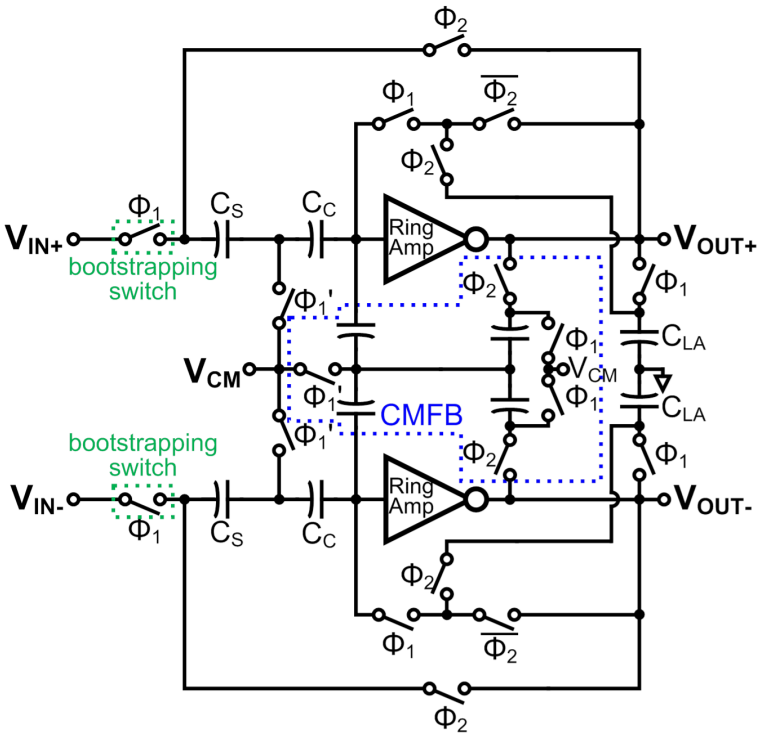

Figure 3.16. Pseudo-differential ring amplified based flip-around sample and hold amplifier.

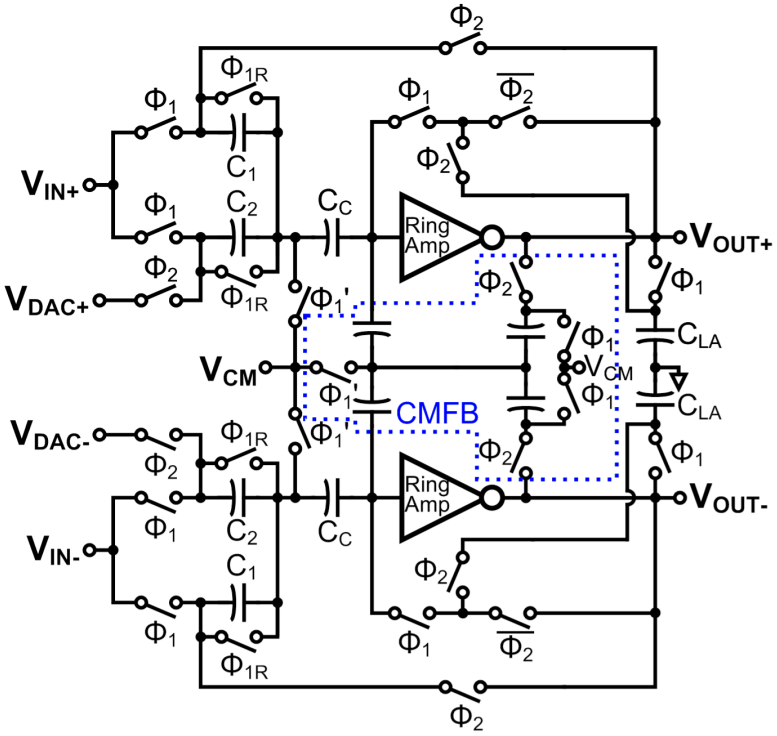

Figure 3.17. Pseudo-differential ring amplified based MDAC gain stage.

The prototype ADC is fabricated in a single poly nine metal (1P9M) 1.2 V 65 nm CMOS process. The ADC core fits within a small area of 0.097 mm^2, as shown in the die microphotograph in Figure 3.18. A summary of performance is shown in Table 3-1[8]. The top and bottom references are set at 1.1 V and 0.1 V thanks to the wide swing of the ring amplifier which results a full-scale differential input signal of 2 V_{pk-pk}. Linearity plots (Figure 3.19) measured at 10b and at a full conversion rate of 100 MS/s, show that the measured DNL and INL are within ±0.22 LSB and -0.62/+0.54 LSB, respectively. As shown in the measured spectrums (Figure 3.20), at a 100 MHz sampling rate the ADC achieves 57.9 dB SNDR, 58.2 dB SNR, and 71.9 dB SFDR with a 10.08 MHz input, and 56.6 dB SNDR, 57.5 dB SNR, and 64.7 dB SFDR with a Nyquist frequency input. Figure 3.21 summarizes the measured SFDR, SNR, and SNDR versus input frequency. The ADC has a quite flat SNR response while SFDR (also SNDR affected by SFDR) is degraded at higher input frequency due to imperfect bootstrapping sampling switch design. The ADC has linear SNDR response up to the full-scale (Figure 3.22). For a 2 V_{pk-pk} input swing, the SNDR with a Nyquist input frequency remains higher than 56 dB over an analog power supply voltage range from 1.2 V to 1.28 V (Figure 3.23). This proves that the dynamic bias using a resistor, R_B, effectively tracks the power supply voltage variation. The SNDR increases as the supply voltage increases up to 1.26 V because the g_m of the first stage inverter increases as the supply voltage increases, and the increased g_m reduces thermal noise of the ring amplifiers. However, the SNDR drops when the supply voltage is higher than 1.26 V because the quiescent offset voltage across R_B increases faster than the supply voltage, and this causes the second stage to operate in the triode region resulting a lower overall three-stage gain. This reduced overall gain gives us a lower SFDR and thus also a reduced SNDR.

[8] The ADC measurements have been updated since those reported in [34]. The measurements in [34] were degraded by digital output I/O related supply noise. The ADC and the test board were revised to achieve better isolation between the ADC core and the digital output I/O.

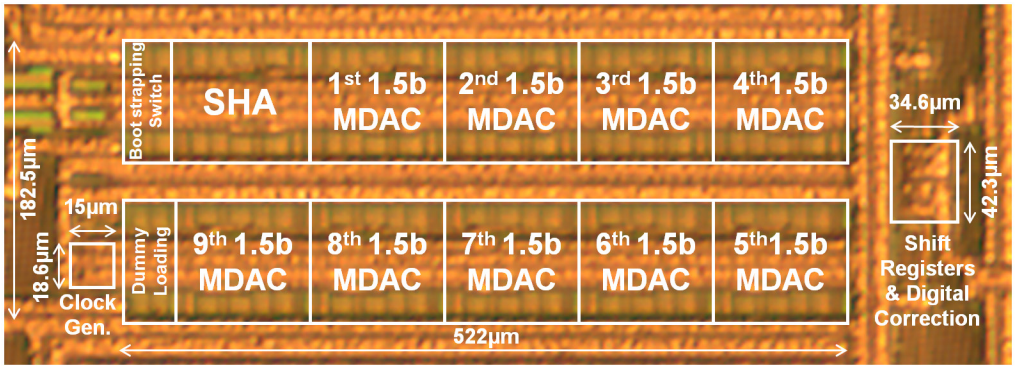

Figure 3.18. Die microphotograph of prototype ADC.

Table 3-1. ADC performance summary.

Resolution	10.5 bit	
Supply	1.2 V (Analog, Clock), 0.75 V (Digital)	
Sampling Rate	100 MS/s	
Technology	65 nm 1P9M CMOS	
Active Area	0.097 mm^2	
Input Range	2.0 V_{pk-pk} differential	
DNL (10 bit)	-0.22/+0.22 LSB	
INL (10 bit)	-0.54/+0.62 LSB	
Power Consumption	2.46 mW Total: 2.33 mW (Analog + CLK), 61.6 µW (Ref.), 65.4 µW (Digital)	
	F_{in}=10.08 MHz	**F_{in}=49.97 MHz**
SNDR	57.9 dB	56.6 dB
SNR	58.2 dB	57.5 dB
SFDR	71.9 dB	64.7 dB
ENOB	9.33 bit	9.11 bit
FoM_W	38.4 fJ/conv-step	44.5 fJ/conv-step

The ADC consumes a total power (excluding I/O) of 2.46 mW at the full conversion speed of 100 MS/s, with a Nyquist frequency input. This results in a figure-of-merit (FoM) of 38.4 fJ/conversion-step for a 10.08 MHz input, and 44.5 fJ/conversion-step for a Nyquist frequency input. This power consumption is comprised of the 1 mW ring amplifier static power dissipation, 62 µW for the reference, and 65 µW for the shift register and digital correction. The remaining 1.33 mW is consumed by the clock generator and the ring amplifier dynamic power consumption.

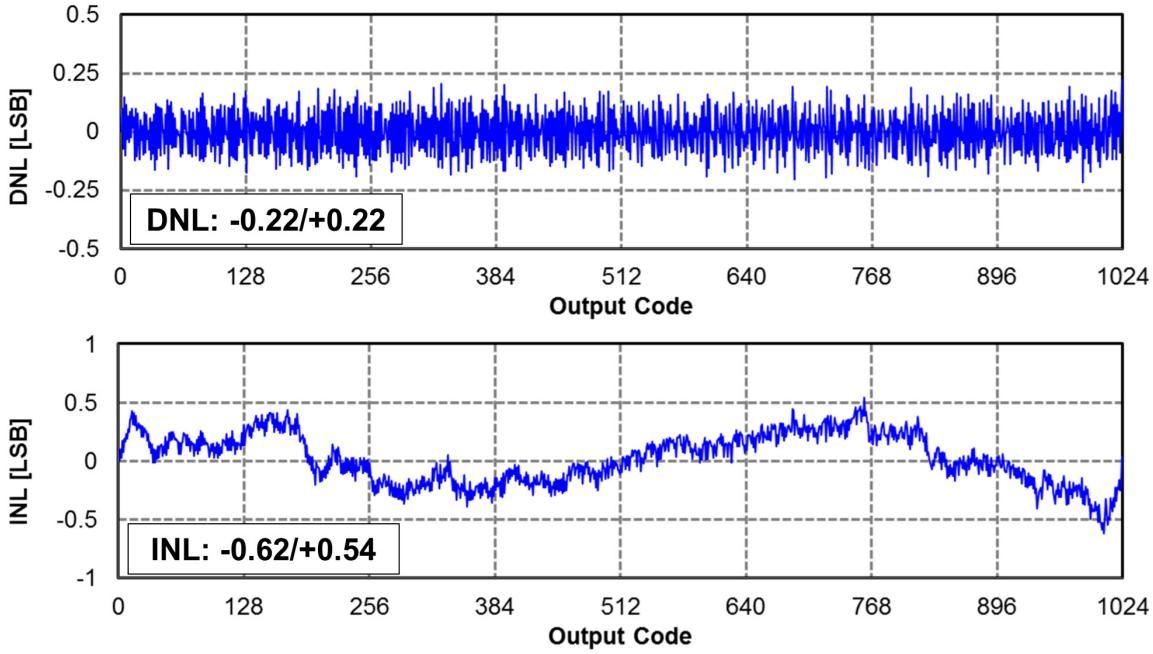

Figure 3.19. Measured DNL and INL at 10b level, 100 MSPS.

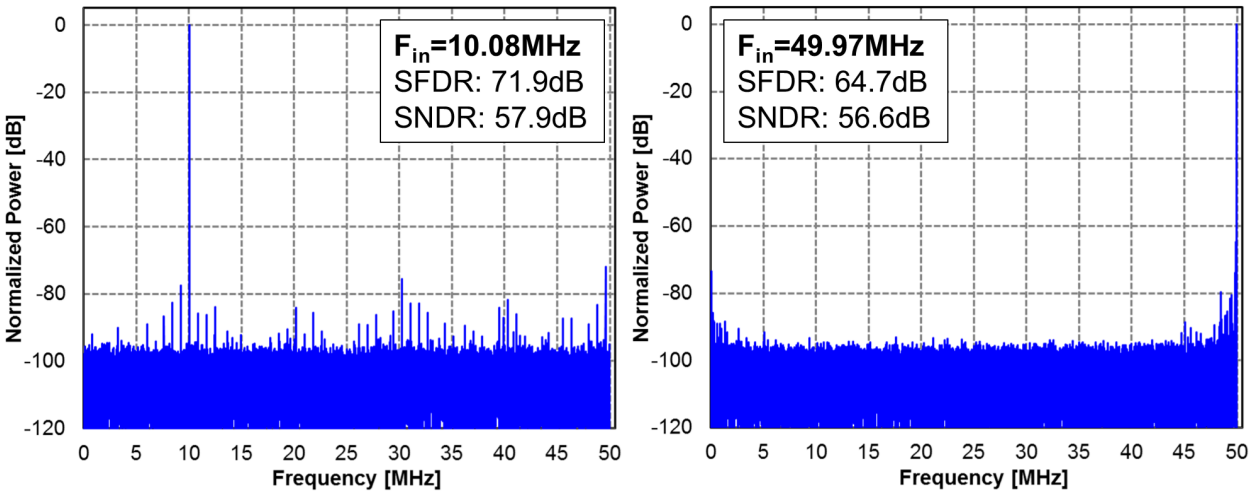

Figure 3.20. Measured spectrums for 10.08 MHz and 49.97 MHz inputs sampled at 100 MS/s (65536 point FFT).

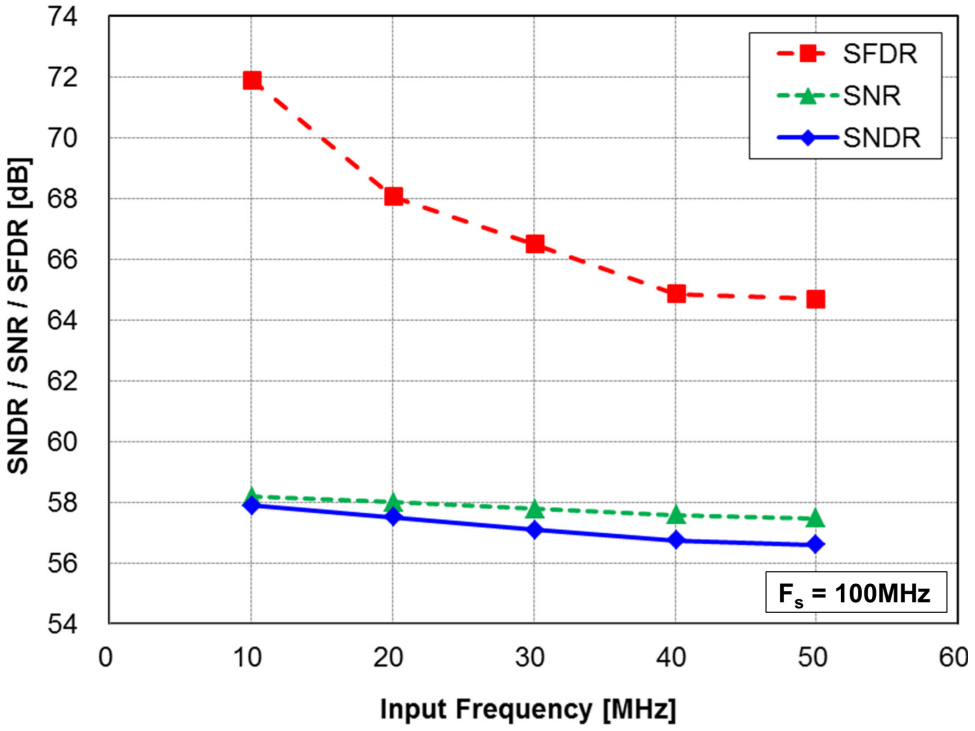

Figure 3.21. Measured SFDR, SNR, and SNDR versus input frequency.

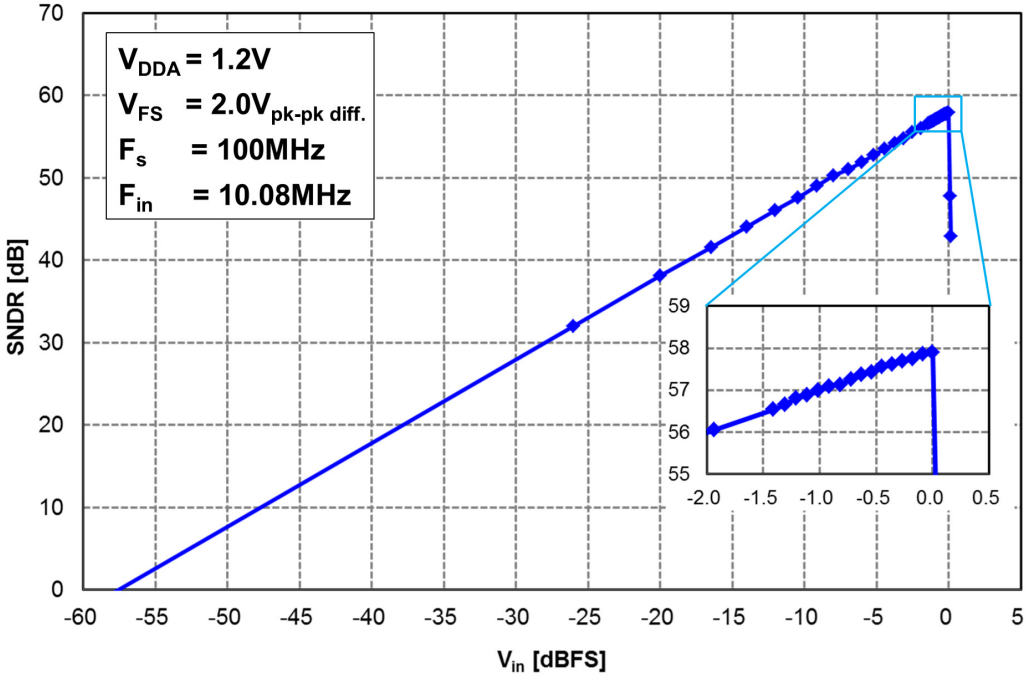

Figure 3.22. Measured SNDR versus input amplitude.

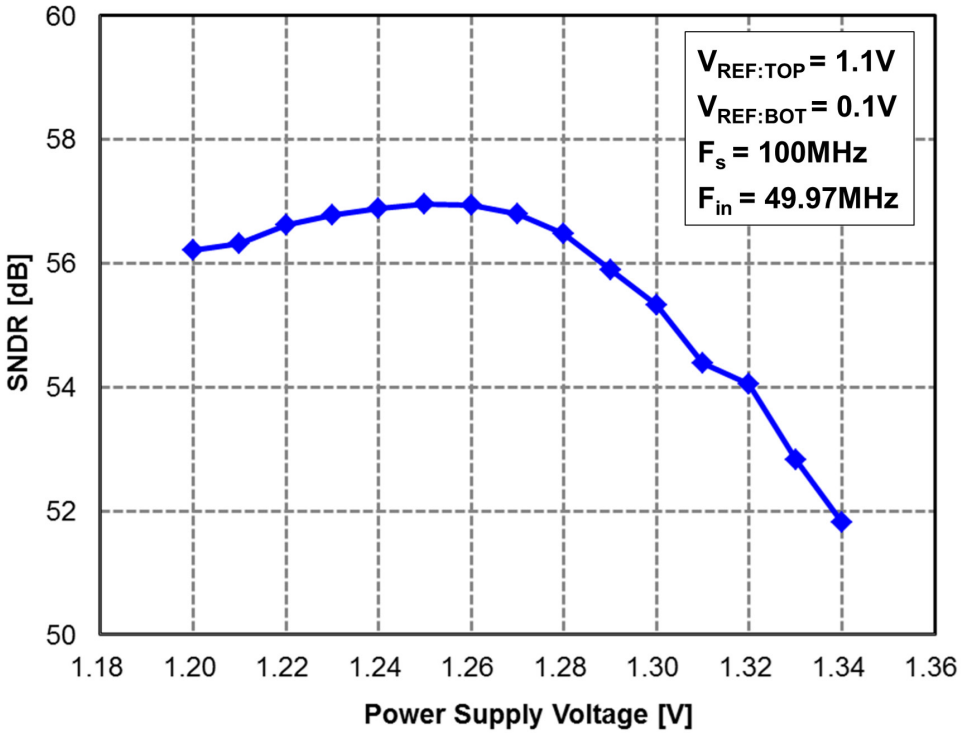

Figure 3.23. Measured SNDR versus analog power supply.

Table 3-2. Performance comparison with the conventional ring amplifier based ADCs.

		This Work	VLSI 2012 [31]	ISSCC 2012 [29]	VLSI 2013 [32]
Resolution		10.5 bit	10.5 bit	15 bit	15 bit
Sampling Rate		100 MSPS	30 MSPS	20 MSPS	20 MSPS
ADC Architecture		1.5b/stage	1.5b/stage	3b/stage	3b/stage
Amp. Structure		Self-biased ring amp only	Ring amp only	Ring amp + split-CLS	Coarse + fine ring amplifier
Technology		65 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS
Active Area		0.097 mm^2	0.50 mm^2	1.98 mm^2	1.98 mm^2
Peak result	**ENOB**	9.33 bit	9.9 bit	12.5 bit	12.3 bit
Nyquist freq.	**ENOB**	9.11 bit	~9.18 bit (from JSSC 2012 [28] graph)	~11.83 bit (from JSSC 2012 [28] graph)	-
Total Power		2.46 mW	2.6 mW	5.1 mW	2.96 mW
FoM (peak result)		38.4 fJ/conv-step	90 fJ/conv-step	45 fJ/conv-step	29 fJ/conv-step
FoM (Nyquist freq. input)		44.5 fJ/conv-step	149.4 fJ/conv-step	70 fJ/conv-step	-

Table 3-2 compares the performance of the prototype ADC with conventional ring amplifier based ADCs. This work achieves a three times better FoM (with Nyquist frequency input) than [31] which uses the same 1.5b/stage ADC structure. In addition, the FoM of the prototype ADC is better than or comparable to more energy effective structured ADCs [29], [32]. These results show the effectiveness of the self-bias ring amplifier.

Figure 3.24 compares the FOM with pipeline ADCs presented at ISSCC (1997-2015) and the VLSI Symposium (1997-2014) [5]. The FOMs of [29] and [31] are updated with the Nyquist frequency input values for a fair comparison. Excluding the SAR-assisted pipeline ADCs which have a more efficient hybrid SAR and pipeline ADC architecture [37], this work has a state-of-the-art FOM among the pipeline ADCs.

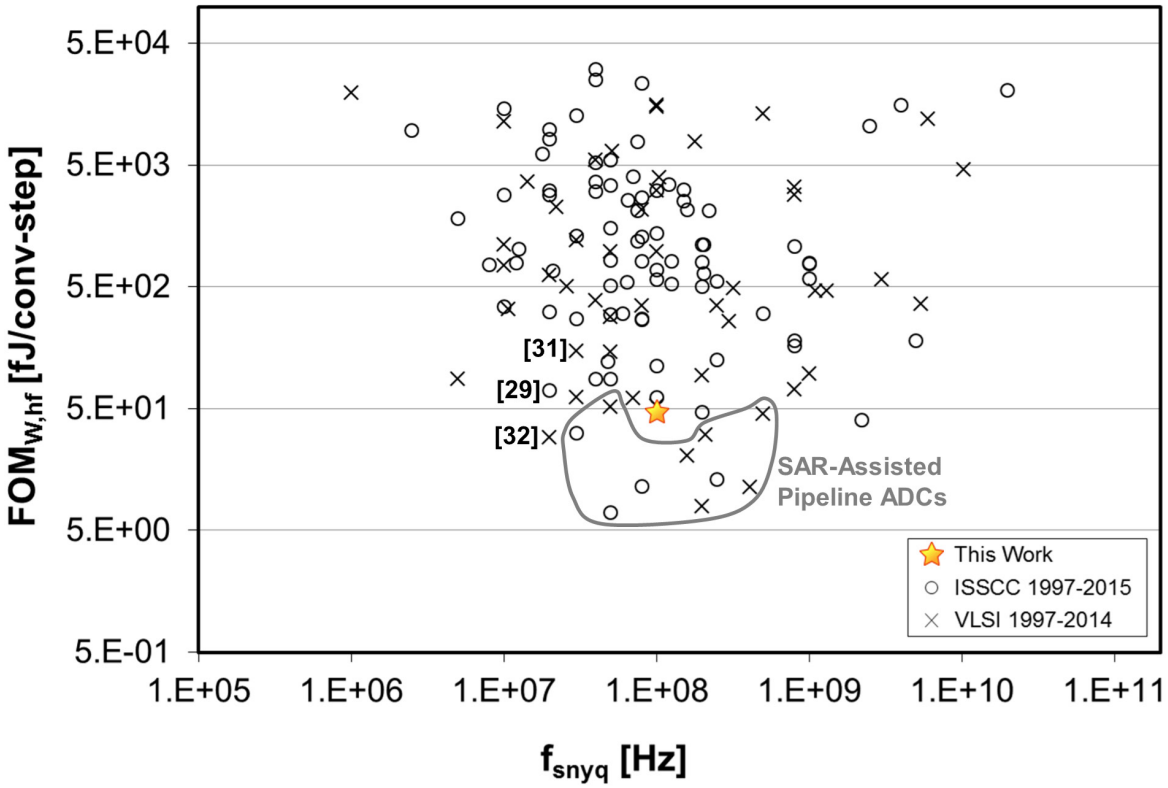

Figure 3.24. FOM comparison with pipeline ADCs presented at ISSCC 1997-2015 and VLSI 1997-2014 [5]

3.5 Conclusion

This research proposes a self-biased ring amplifier. The elimination of external biasing makes the ring amplifier more practical and power efficient while keeping the benefits of the conventional ring amplifier, such as slew based charging and a near rail-to-rail output swing. The use of high threshold voltage devices for the last-stage inverter and simple resistor-based dynamic biasing in the second stage facilitate a single inverter second stage and the elimination of external biasing. In addition, an improved auto-zero scheme eliminates the gain error caused by the parasitic capacitor of the auto-zero switch. The ring amplifiers function as continuous time comparators for the sub-ADCs. Thanks to these techniques, the prototype ADC achieves 56.6 dB SNDR for a Nyquist frequency input, sampled at 100 MS/s, and consumes only 2.46 mW.

CHAPTER 4

A Fully-Differential Ring Amplifier Based SAR-Assisted Pipeline ADC

4.1 Introduction

The SAR-assisted pipeline ADC architecture [37], [38] is an energy efficient hybrid architecture for high resolution that pipelines two SAR ADCs, coupled by a residue amplifier, as shown in Figure 4.1. The two SAR ADCs work as high-resolution sub-ADCs for the two pipeline stages to give the SAR-assisted pipeline ADC several advantages over conventional flash sub-ADC based pipeline ADCs and conventional SAR ADCs [37].

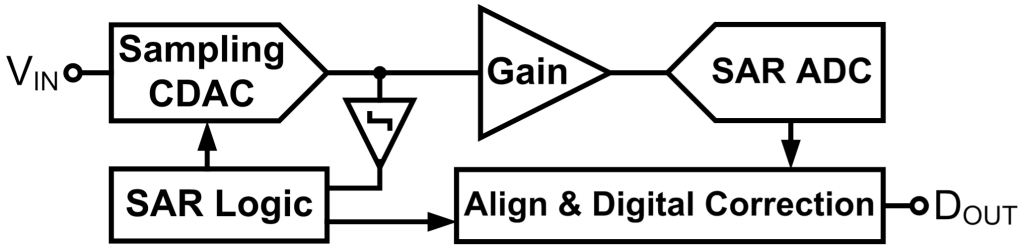

Figure 4.1. SAR-assisted pipeline ADC block diagram.

Let's first look at it as a pipeline ADC. We can improve ADC linearity and reduce amplifier power consumption in a pipeline ADC as we increase the resolution of the first-stage sub-ADC [8]. A SAR sub-ADC uses less power than a flash sub-ADC. Another important benefit of the

SAR first-stage sub-ADC is that it removes sampling mismatch between the sub-ADC and the MDAC, thereby removing the need for a dedicated frontend SHA.

The SAR-assisted pipeline ADC also has benefits over conventional SAR ADCs. In order to implement a high resolution ADC using conventional SAR ADC, the comparator needs to consume high power to reduce the noise, or requires several additional comparison cycles to average the noise out [39]–[41]. On the other hand, since the SAR-assisted pipeline ADC only uses low resolution SAR ADCs for a high overall resolution ADC, we can reduce the power consumption of the comparator, because the comparator is not noise constrained for the low resolution. In addition, pipelining relaxes the speed bottleneck of the conventional SAR architecture. The SAR-assisted pipeline ADC tolerates settling errors of the first-stage SAR capacitive DAC (CDAC) as long as these remain within the error correction range of the stage redundancy. Therefore, we can increase the speed of the first stage SAR ADC compared to the conventional SAR ADCs

Despite these benefits, the use of a double-cascoded telescopic OTA based switched-capacitor (SC) residue amplifier in conventional SAR-assisted pipeline ADCs [37], [38], [42] limits efficiency because the OTA is power hungry and has a limited output swing. The limited output swing necessitates a reduced residue gain and requires power consuming second-stage reference scaling [37], [38], or the use of an R-2R DAC based second-stage SAR ADC [42]. Dynamic amplifiers, which operate as open-loop time-domain integrators, are a lower power alternative for residue amplification [43]–[49]. Although integration provides the benefit of noise-filtering [46], [47], the open-loop nature of dynamic amplification requires calibration to achieve accurate residue gain, and the calibration increases design complexity and test cost, and limits the robustness to process, supply voltage, and temperature (PVT) variation [44].

This research introduces a 13b 50 MS/s fully-differential ring amplifier based SAR-assisted pipeline ADC [50], which achieves better efficiency (6.9 fJ/conversion·step) than conventional approaches and does not need calibration. A comparison of the Walden FOM (fJ/conversion·step) for conventional approaches (Figure 4.2) shows that calibrated SAR-assisted pipeline ADCs with dynamic amplifiers[9] tend to achieve better efficiency. Instead, this work a presents a new fully-differential ring amplifier that enables accurate SC residue amplifier gain without the need for calibration. This ring amplifier has the advantages of energy efficient slew-based charging as well as a near rail-to-rail output swing, and is robust to PVT variation.

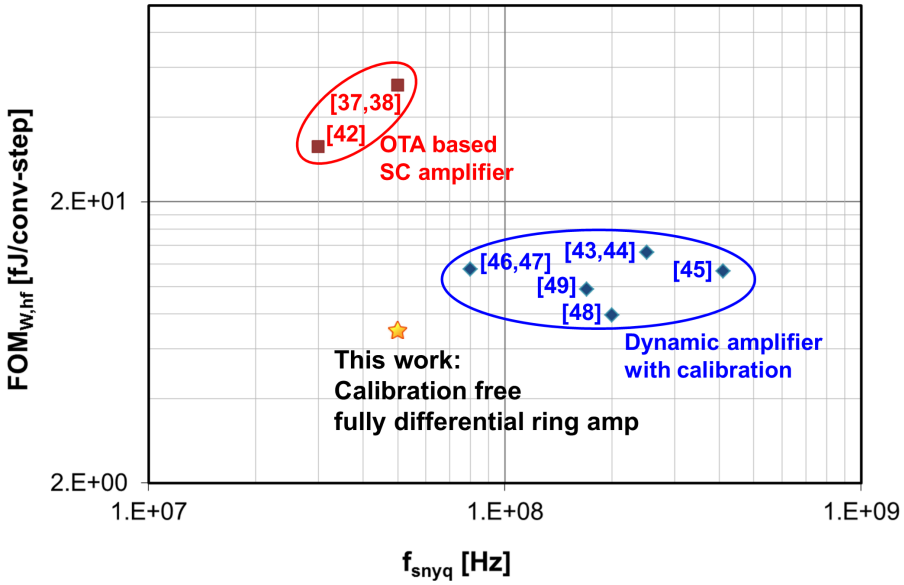

Figure 4.2. Walden FOM comparison with conventional SAR-assisted pipeline ADCs.

This work also improves the accuracy and the energy efficiency of the CDAC in the first-stage SAR sub-ADC. The first-stage CDAC draws a considerable amount of power from the references since it has a large capacitance to achieve low kT/C noise for high resolution. In addition, the accuracy of the first-stage CDAC must satisfy the linearity requirements of the full

[9] [43]–[49] achieve higher speed by using a 2× interleaved architecture and advanced CMOS processes (40 nm or 28 nm).

ADC resolution because DAC errors are not corrected by digital error correction. [46], [47] reduce the first-stage CDAC switching energy by floating three quarters of the two MSB capacitors and the remaining LSB capacitors during the three MSB decisions, but conventional approaches [43]–[49] still need to calibrate the first-stage CDAC in order to meet the required linearity. This research presents an improved first-stage CDAC switching technique, which we name *floated detected-and-skip* (FDAS) switching, that further reduces the first-stage CDAC switching energy and also improves DAC linearity to achieve 13b linearity without calibration.

The remainder of this chapter is organized as follows; Section 4.2 introduces the new fully-differential ring amplifier. Then, Section 4.3 presents the architecture of the prototype ADC, Section 4.4 explains how FDAS first-stage CDAC switching reduces the CDAC switching energy and improves linearity, and Section 4.5 gives a detailed description of the ADC implementation. Finally, in Section 4.6, we present measurements of the prototype ADC, and conclude the chapter in Section 4.7.

4.2 Fully-Differential Ring Amplifier

In this section, we briefly review conventional single-ended ring amplifiers and discuss their benefits and drawbacks. Then, we introduce the fully-differential ring amplifier and give a detailed explanation of its operation.

4.2.1 Conventional Ring Amplifiers Review

Conventional ring amplifiers [30], [34], [51], in Figure 4.3 are an energy efficient wide-swing alternative to an OTA for SC circuits. A ring amplifier is essentially a three-stage inverter amplifier stabilized in a feedback network by operating the last stage in the sub-threshold region

when it is in steady state. The sub-threshold operation of the last stage ensures a high output resistance to form a dominant pole for stable feedback operation.

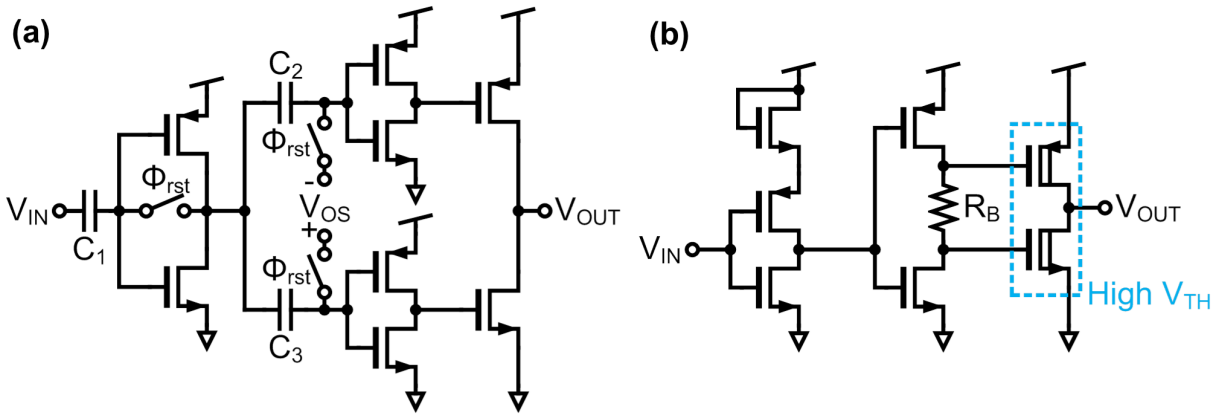

Figure 4.3. Conventional ring amplifiers. (a) original ring amplifier [30], (b) self-biased ring amplifier [34], [51].

Ring amplifiers have several important advantages over OTAs. First, they easily produce high gain from the three cascaded gain stages. Second, ring amplifiers achieve efficient slew-based charging, as the last stage operates as digital switch during slewing and is in cut-off (in deep sub-threshold) when the amplifier is settled. Third, ring amplifiers have an almost rail-to-rail output swing because the last stage is a simple inverter operating in sub-threshold region.

Although conventional ring amplifiers have several benefits over OTAs, they are limited to single-ended, thus these ring amplifiers have all of the disadvantages of single-ended structures. These disadvantages include the lack of inherent common mode and supply rejection, and the susceptibility to even order harmonics. The use of pseudo-differential structures and pseudo-differential common mode feedback (CMFB) [30], [34], [51] (Figure 4.4) can somewhat alleviate these problems. The pseudo-differential CMFB in Figure 4.4 consists of the capacitors C_{S+}, C_{S-} and C_F, related switches, and the common mode voltage reference (V_{CM}). C_{S+} and C_{S-} sense the deviation of the output common mode from V_{CM} and feedback this to the ring amplifier

inputs using C_F. However, this pseudo differential CMFB also reduces the effective ring amplifier gain to $A_V \cdot C_C/(C_C+C_F+C_{IN})$ due to the capacitive divider formed at the input of the ring amplifier, where A_V is the small signal gain of the ring amplifier, C_C is the offset canceling capacitance for auto-zero, and C_{IN} is the input parasitic capacitance of the ring amplifier.

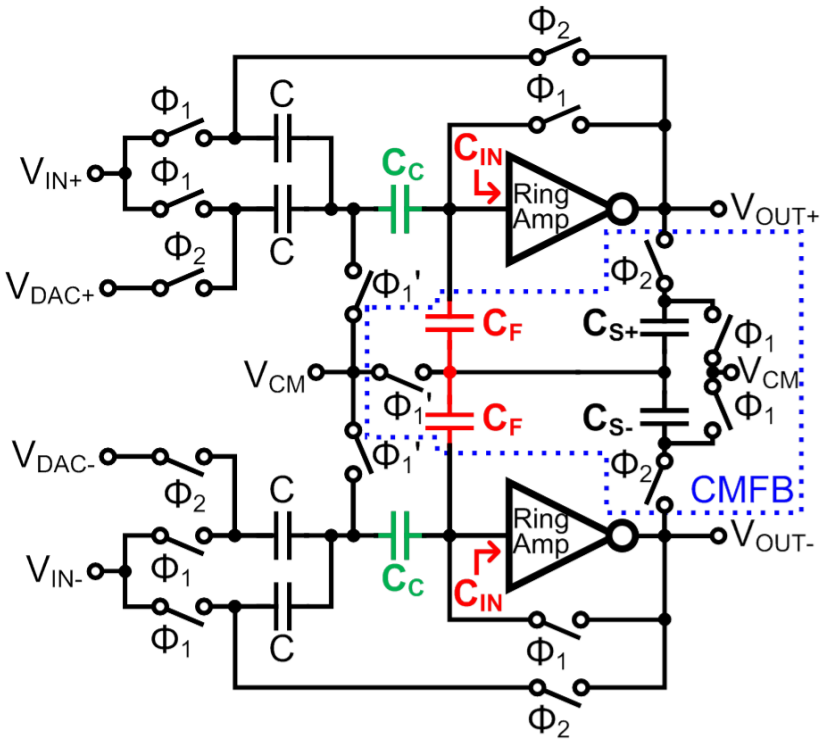

Figure 4.4. Pseudo-differential MDAC gain stage in [34], [51].

4.2.2 Fully-Differential Ring Amplifier

We introduce a new fully-differential ring amplifier [50] that fully utilizes the ring amplifier gain and solves the limitations of the single-ended structure. A single differential ring amplifier replaces the two single-ended ring amplifiers in the conventional pseudo differential implementation. Figure 4.5 shows the fully-differential ring amplifier along with the bias and CMFB circuits. In order to make the ring amplifier fully differential, we replace the first stages of the two self-biased ring amplifiers [34], [51] with a single differential pair. We use the current

reuse technique to reduce the thermal noise of the first stage, which is the dominant noise source in the ring amplifier. In order to reduce the thermal noise, we increase the transconductance of the first stage since thermal noise is inversely proportional to transconductance. The use of both PMOS and NMOS input devices maximizes transconductance for a given current bias. To save power, an enable switch at the bottom of the NMOS tail current source, controlled by signal Φ_{EN}, turns off the ring amplifier when it is not used.

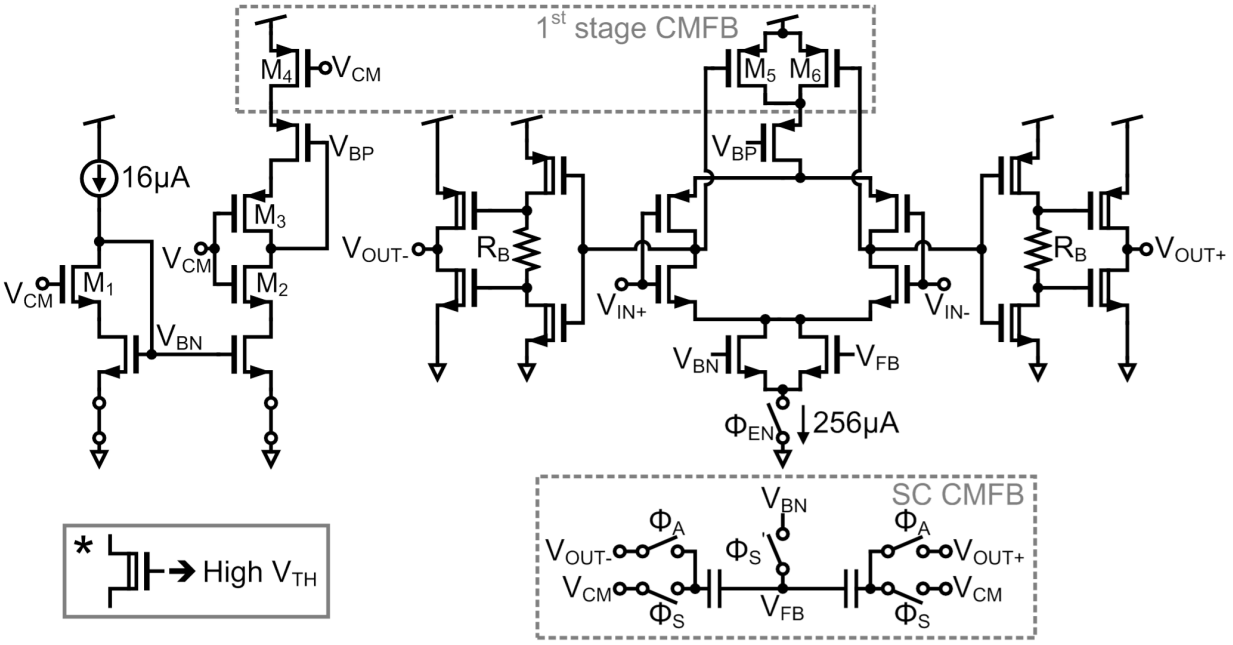

Figure 4.5. Fully-differential ring amplifier, bias, and CMFB.

The first stage has both PMOS and NMOS tail current sources, which means that the first stage functions as a current starved inverter for the common mode of the input. A PMOS triode device based CMFB [52], consisting of M_4, M_5, and M_6, coarsely sets the common mode at the output of the first stage during auto-zero. The widths of the transistors in the bias circuit are 16 times smaller than the widths of the corresponding transistors in the half circuit of the first stage. V_{CM} is used as the cascode bias voltage for the bias circuit on the left hand side of Figure 4.5 replicating the input voltage to the first-stage PMOS and NMOS devices. The use of V_{CM} as the

cascode bias voltage also sets the ring amplifier input close to V_{CM}. The first stage (and also the ring amplifier) produces the highest gain when the inputs, V_{IN+} and V_{IN-}, are close to V_{CM}. Since the auto-zero sets the ring amplifier input and output voltage close to the input voltage which produces the highest gain, which is around V_{CM} in this case, the bias circuit sets the input voltages of the ring amplifier close to V_{CM} during auto-zero. We also use a separate SC CMFB circuit to set the overall output common mode of the ring amplifier to V_{CM} during the amplification phase. We do not perform CMFB on the ring amplifier output during auto-zero because the ring amplifier output common mode does not affect the ring amplifier differential input offset.

The second and third stages are inverter-like structures. As with the self-biased ring amplifier [34], [51], the resistors, R_B, (Figure 4.5) in the second stages dynamically apply offset voltages to the last stages. A limitation is that this dynamic biasing reduces the $|V_{DS}|$ of the second-stage transistors when current is flowing. In steady state, this causes the second-stage transistors to operate close to (or in) the triode region, greatly reducing the second-stage gain and also the gain of the entire ring amplifier. We use high V_{TH} devices in the second stage to prevent this gain reduction. The higher threshold voltage extends the second-stage output voltage range for which the transistors operate in saturation. The simulated small-signal ring amplifier gain is higher than 80 dB for an output swing from 0.1 V to 1.1 V with a 1.2 V supply.

4.3 Proposed ADC Architecture

The prototype ADC [50] consists of a 6b first-stage SAR ADC, a 32× gain residue stage based on the fully-differential ring amplifier, and an 8b second-stage SAR ADC. Figure 4.6 shows the proposed ADC architecture. The ADC resolves 13b after digital correction with a

single bit of stage redundancy. The ADC accepts a 2.4 $V_{pk\text{-}pk\ diff}$ rail-to-rail input. Unlike conventional SAR-assisted pipeline ADCs [37], [38], [42]–[49], this work uses a full residue gain of 32, considering a single bit of stage redundancy, thanks to the wide output swing of the ring amplifier - this makes the second stage simpler and more efficient, and further relaxes the second-stage noise requirement. With the full residue gain and one bit of redundancy the ideal output range of the residue gain stage is from 0.3 V to 0.9 V, assuming the first-stage CDAC and comparator are ideal. The rest of the ring amplifier output range accommodates the 1b redundancy.

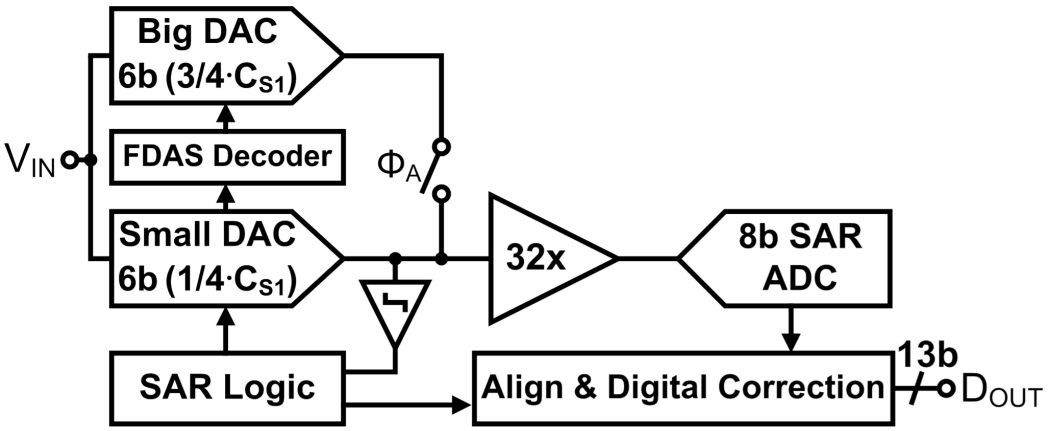

Figure 4.6. Proposed ADC architecture.

The first-stage SAR CDAC, as shown in Figure 4.6, is divided into two separate capacitor arrays, *Big DAC* and *Small DAC*, to reduce the first-stage CDAC switching energy[10] and the INL due to the first-stage CDAC capacitor mismatch. The total sampling capacitance (differential) of the first-stage CDAC is 4pF to meet the 13b kT/C noise requirement for residue generation. On the other hand, the first-stage SAR sub-ADC needs only to achieve 6b kT/C noise performance. In order to utilize these differing noise requirements to both reduce the CDAC switching energy

[10] A similar technique, independently developed in [53], divides the first-stage CDAC to reduce the first-stage CDAC switching energy.

and to improve linearity, we divide the first-stage CDAC into two CDACs, as shown in Figure 4.6. The SAR ADC uses only *Small DAC*, which has a quarter of the sampling capacitance, to reduce power consumption. The remaining three quarters of the sampling capacitance is contained in *Big DAC*. Merged capacitor switching (MCS) [54] in the SAR ADC reduces the SAR DAC energy consumption. In addition, bottom plate input sampling enhances the accuracy of the MCS based SAR ADC by setting the comparator input to the common mode voltage during sampling, thus avoiding the effects of the nonlinear parasitic capacitance on the comparator input. Asynchronous SAR logic [55] eliminates the need for a high frequency clock and reduces errors due to comparator meta-stability.

Big DAC samples the same input signal as *Small DAC*, and together with *Small DAC* generates a residue voltage based on the decisions from the *Small DAC* based SAR ADC. Energy efficient switching is achieved with the FDAS CDAC switching technique, which is derived from [56]. (Details of how FDAS switching both reduces the CDAC switching energy and improves linearity of the first-stage CDAC are discussed in the next section.) When the first-stage conversion is finished, the residues of *Big* and *Small DACs* are merged together to meet the 13b kT/C noise requirement and are then amplified by 32× using the residue amplifier. Mismatch between the overall DAC and the quantized value of the *Small DAC* SAR ADC is corrected by the 1b stage redundancy.

As shown in Figure 4.7, we use an auto-zeroed fully-differential ring amplifier based SC amplifier for residue amplification. Φ_A controls the amplification phase, and Φ_S and Φ_S' are sampling/auto-zero phase control signals. The actual implementation is fully differential. Auto-zeroing is used to fully utilize the output swing of the ring amplifier so that we can maximize the digital correction range. A large (4 pF) offset cancelation capacitor, C_{AZ}, reduces auto-zero noise

folding [16]. However, the use of a big C_{AZ} capacitance does not increase power consumption, because the sampled voltage on C_{AZ} stays constant. This big capacitance also stabilizes the ring amplifier during the auto-zero phase by presenting a large load to the ring amplifier output, and reducing the dominant pole frequency and the slew rate. The small feedback factor (~1/33) during the amplification phase also helps the stabilization of the ring amplifier [51].

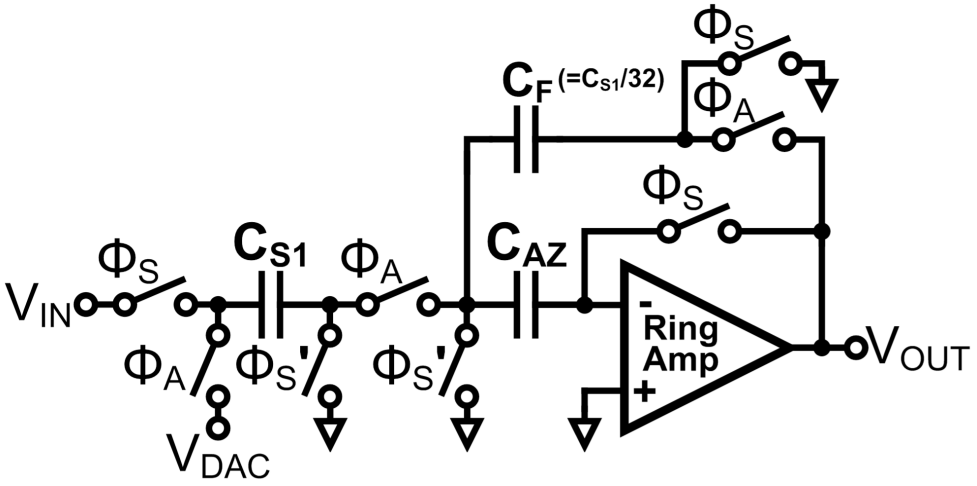

Figure 4.7. Residue gain stage structure. Actual implementation is fully differential.

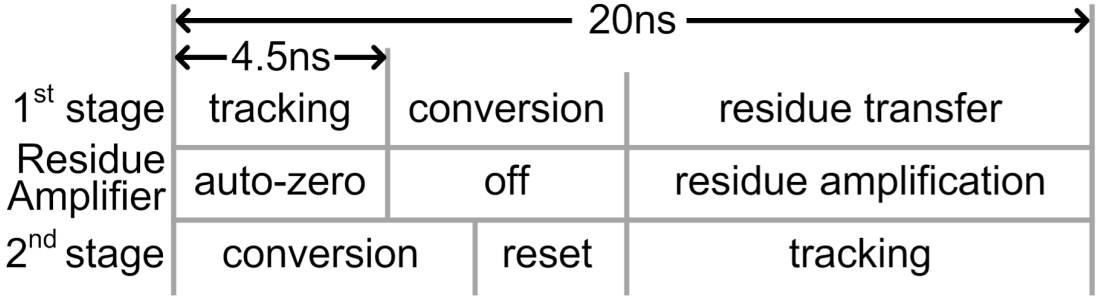

Figure 4.8. Simplified ADC timing diagram.

As shown in the simplified ADC timing diagram, Figure 4.8, the ring amplifier is turned off during the first-stage SAR ADC conversion to reduce the power consumption. The amplification starts asynchronously after the first-stage SAR ADC conversion is complete to maximize the duration of the residue amplification phase. The amplified residue is sampled and then quantized

by an 8b second-stage SAR ADC, which also uses MCS, bottom plate input sampling, and asynchronous SAR logic. As shown in Figure 4.8, the second-stage CDAC is reset after the 8b decision so that residue amplification always starts from V_{CM}. This reset operation improves the power efficiency of the ring amplifiers by halving the maximum slew rate required of the ring amplifier [51].

4.4 FDAS First-Stage CDAC Switching

As mentioned in the previous section, we use FDAS switching in the first-stage CDAC. This section explains the operation of FDAS switching, and how it both reduces the first-stage CDAC switching energy and improves the DAC linearity.

4.4.1 Switching Energy Reduction

One of the switching energy losses in conventional SAR operation comes from the binary search. Figure 4.9 shows an example of residue generation for a 4b *Big DAC* using MCS switching. In this example, *Big DAC* is switched directly based on the *Small DAC* MCS decisions. The DAC output voltage, V_{DAC}, starts at the inverse of the DAC input ($-V_{IN}$) because we use bottom plate input sampling. As shown in Figure 4.9, if we generate the *Big DAC* residue using a binary search and MCS, we will have opposite direction switching in some cases. Although this opposite direction switching is necessary for the binary search, it is wasteful for residue generation. However, we can avoid this wasteful switching energy since we already know the decisions of the *Small DAC* SAR ADC.

In order to reduce this switching energy loss for *Big DAC*, we adopt detect-and-skip (DAS) switching [56]. Figure 4.10 shows an example of DAS switching for residue generation in a 4b

Big DAC. DAS detects the opposite direction switching from the *Small DAC* SAR ADC decisions, and skips this opposite direction switching for *Big DAC* by connecting the corresponding switches to V_{CM}. Even though we avoid opposite direction switching using DAS switching, we still get the same overall residue as with MCS switching. Although it might be expected that decoding the *Small DAC* SAR decisions for DAS switching would require a complicated algorithm [56], it turns out that a simple decoding method can be used. As shown in Figure 4.10, when the MSB of the *Small DAC* SAR decision is 0, this decoding is a simple left circular shift of the *Small DAC* SAR decision results and the replacement of V_{DD} connections with V_{CM} connections. Similarly, as shown in Figure 4.11, when the MSB of the *Small DAC* SAR decision is 1, the decoding is a simple left circular shift of the *Small DAC* SAR decision results and the replacement of ground (GND) connections with V_{CM} connections. In this way, we avoid significant switching energy loss related to the binary search in the first-stage CDAC.

Another switching energy loss in the conventional SAR CDAC operation comes from the successive capacitor switching needed after each decision. A conventional SAR CDAC successively switches a capacitor after every decision in the binary search. Figure 4.12(a) shows an example of successive switching in a 2b CDAC. When the MSB switch flips from ground to reference voltage, V_R, the CDAC consumes CV_R^2 of switching energy, and then when the LSB switch flips, the CDAC consumes a further $0.25CV_R^2$ of switching energy. Therefore, in this example, the CDAC consumes a total switching energy of $1.25CV_R^2$. Although this energy consumption due to successive switching is unavoidable with a single capacitor array SAR DAC, here since we already know the result from the *Small DAC* SAR ADC we can avoid some of this switching energy for *Big DAC*.

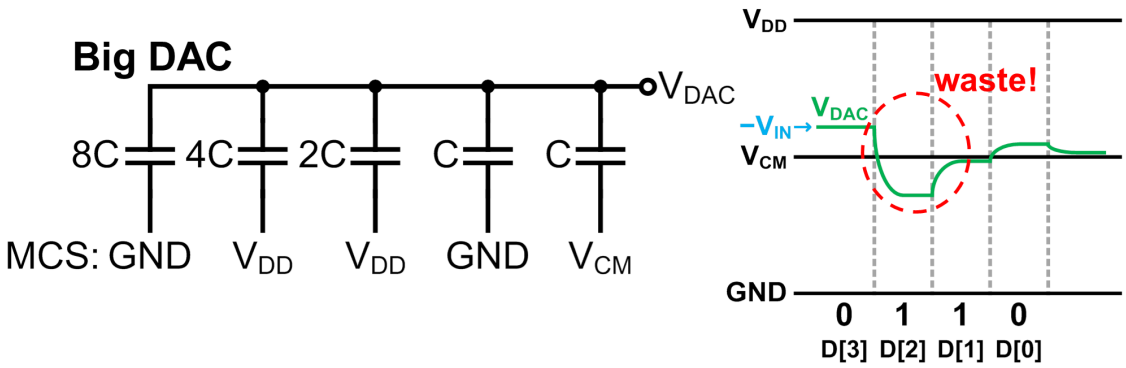

Figure 4.9. MCS switching 4b *Big DAC* residue generation example.

The bottom plates are switched to the final states.

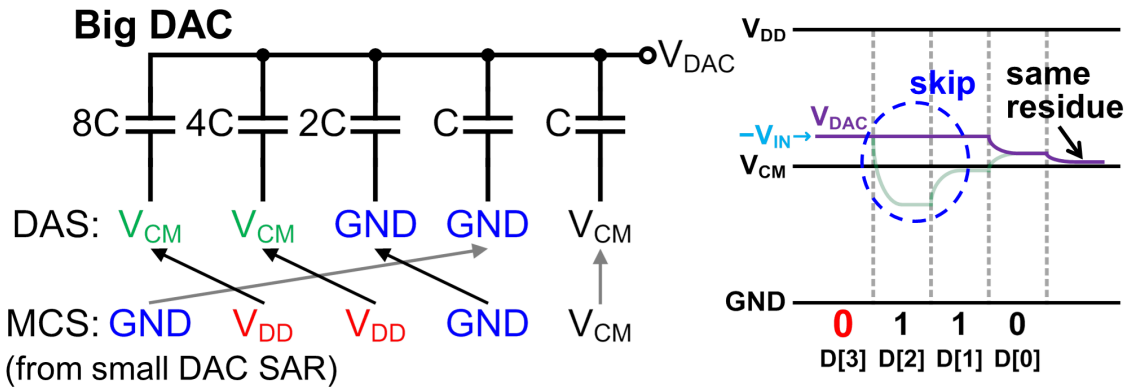

Figure 4.10. Detect-and-skip (DAS) switching 4b *Big DAC* residue generation example when the MSB (D[3]) of *Small DAC* SAR is 0. The bottom plates are switched to the final states.

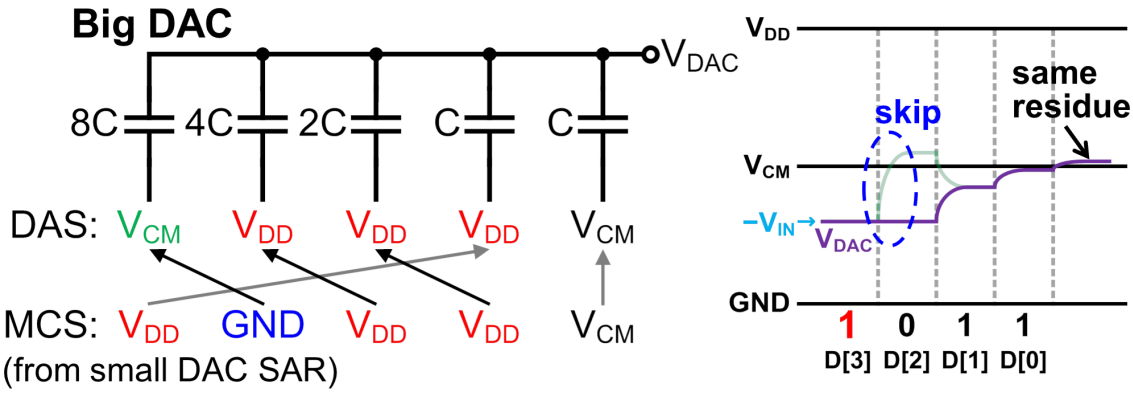

Figure 4.11. Detect-and-skip (DAS) switching 4b *Big DAC* residue generation example when the MSB (D[3]) of *Small DAC* SAR is 1. The bottom plates are switched to the final states.

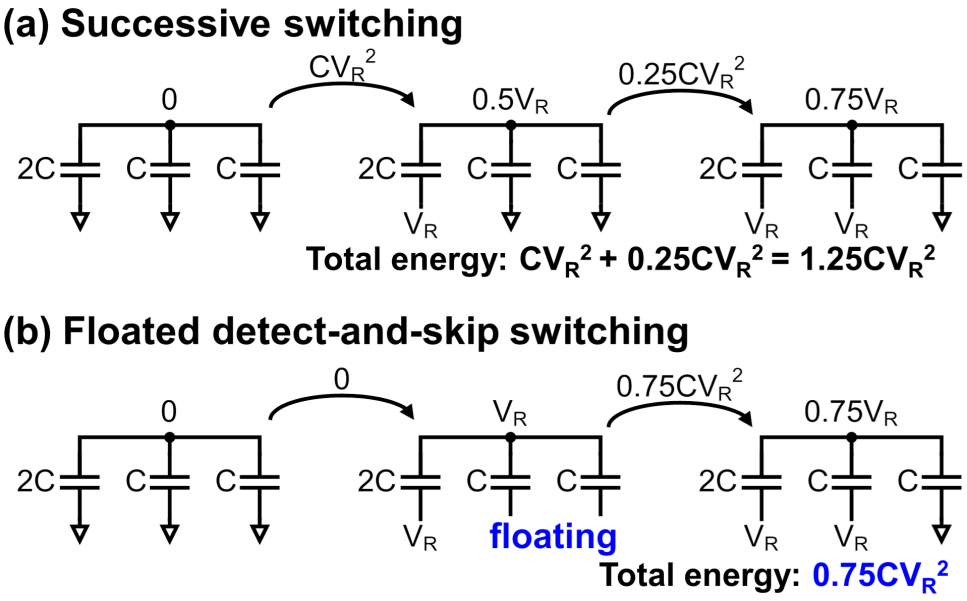

Figure 4.12. 2b CDAC switching example. (a) successive switching,

(b) floated detect-and-skip switching.

In order to reduce switching energy loss from successive switching, [56] uses aligned switching (AS) together with DAS. This technique sets *Big DAC* switches only after the *Small DAC* SAR ADC is completely finished. However, aligned switching requires additional settling time or alternatively bigger switches with increased DAC encoder power consumption to minimize the additional settling time. Instead of using DAS and AS together, we introduce floated DAS (FDAS) in which we flip *Big DAC* switches immediately after each corresponding *Small DAC* SAR bit decision, while the undecided capacitors are floated. Figure 4.12(b) shows a 2b example of FDAS switching. When the MSB capacitor switch flips, the CDAC does not consume switching energy since there is no charge movement because all the other capacitors are floated. Then, when the LSB and the dummy switch flip, the CDAC consumes $0.75CV_R^2$ of switching energy. Thus, in this example we save $0.5CV_R^2$ of switching energy by using FDAS switching. Another benefit of FDAS switching is it does not require additional settling time for

Big DAC switching. The MSB capacitors of *Big DAC* have plenty of settling time because MSB switching occurs early.

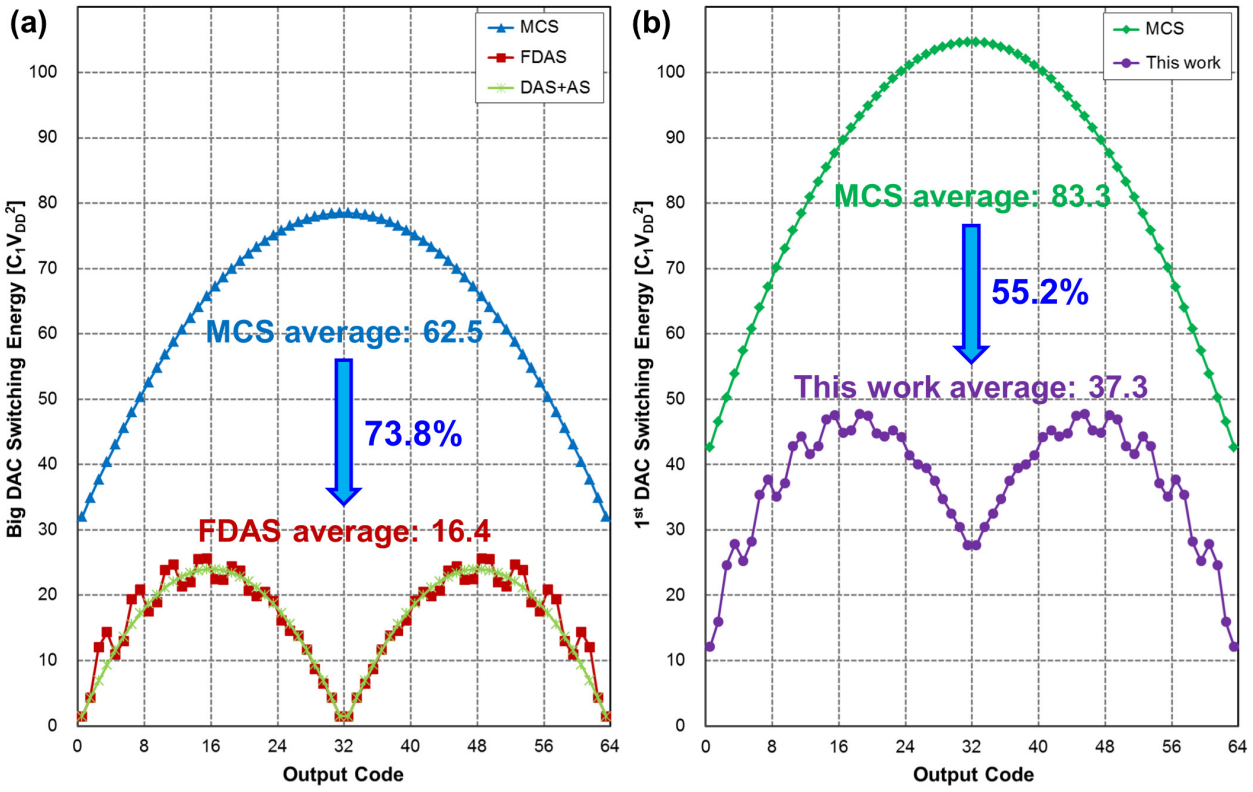

Figure 4.13. Calculated 6b CDAC switching energy comparison. (a) *Big DAC* switching energy, (b) the first-stage CDAC switching energy.

Figure 4.13 shows comparisons of calculated 6b CDAC switching energy. *Big DAC* use $3C_1$ as a unit capacitor and the first-stage CDAC use $4C_1$ as a unit capacitor. The CDACs uses V_{DD} and ground as references. When we compare FDAS *Big DAC* switching with MCS *Big DAC* switching (Figure 4.13(a)), FDAS consumes 74 % less switching energy on average. FDAS *Big DAC* switching consumes slightly more switching energy (2.7 %) than DAS with AS [56] (Figure 4.13(a)) because the last two LSBs and the dummy switches flip together at the end of the *Small DAC* SAR decision. However, FDAS switching has the significant advantage of not requiring additional settling time for *Big DAC* and this allows us to reduce the size of *Big DAC*

switches, which itself reduces the power consumption of the FDAS encoder. When we compare the first-stage DAC switching energy in this work (i.e. MCS *Small DAC* switching and FDAS *Big DAC* switching) with MCS only first-stage CDAC switching (Figure 4.13(b)), this work consumes 55 % less switching energy on average.

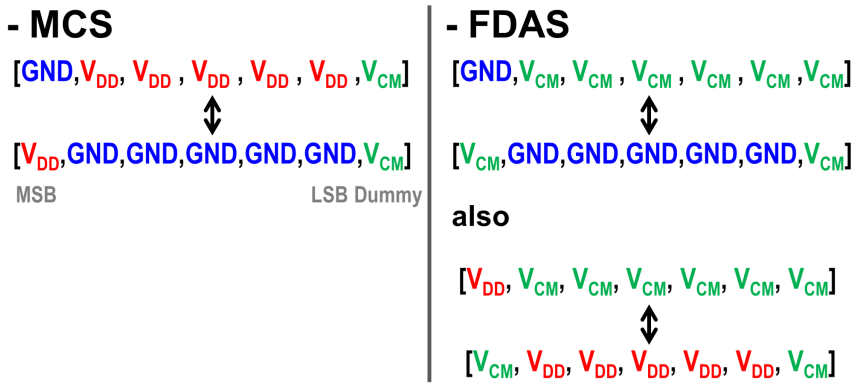

Figure 4.14. Worst case INL of 6b CDAC switching for MCS and FDAS.

4.4.2 Linearity Improvement

FDAS (and also DAS, although not mentioned in [56]) switching also reduces INL errors due to the first-stage CDAC capacitor mismatch. As shown in Figure 4.14, the worst case INL with MCS occurs when the MSB switch flips between V_{DD} and GND. However, the worst case INL with FDAS occurs when the MSB switch flips between GND and V_{CM}, or between V_{DD} and V_{CM}. Since the voltage swing is halved in FDAS switching, the worst-case voltage error is also halved and thus the worst case INL is halved. This INL improvement is the same as for the early reset merged capacitor switching (EMCS) algorithm in [57]. In fact, FDAS decoding result is the same as EMCS algorithm decoding result. Figure 4.15 shows the results for Monte Carlo simulation of the root-mean-square (RMS) INL of the first-stage CDAC (10k iterations) for a one sigma unit capacitor mismatch of 0.3 %. *Big DAC* use $3C_1$ as a unit capacitor and the first-stage CDAC use $4C_1$ as a unit capacitor. The simulation shows that the maximum RMS INL for

FDAS *Big DAC* switching is 52 % lower than for MCS *Big DAC* switching (Figure 4.15(a)). The RMS INL due to the overall first-stage CDAC is 38 % less than for an MCS only first-stage CDAC (Figure 4.15(b)).

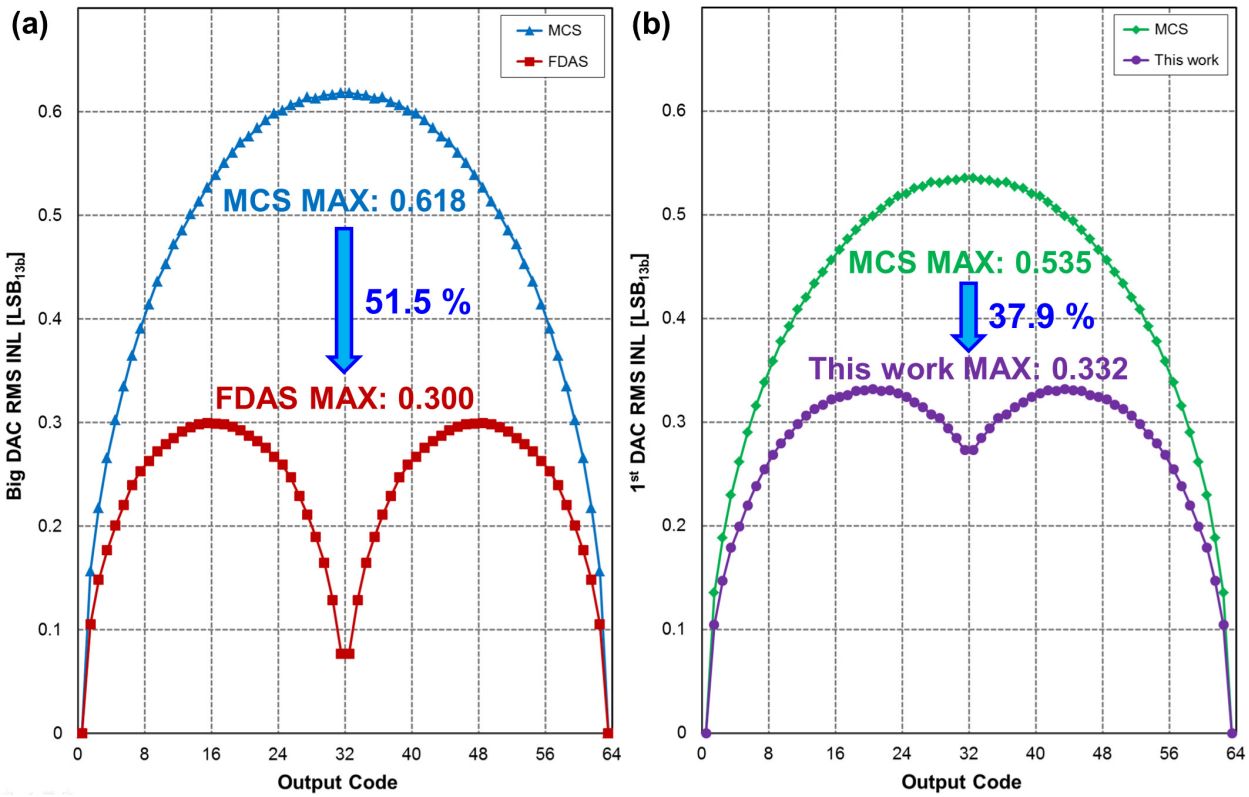

Figure 4.15. Simulated RMS INL due to the first-stage CDAC mismatch with 10k iteration and a one sigma C_1 mismatch of 0.3 %. (a) RMS INL due to *Big DAC*, (b) RMS INL due to the first-stage CDAC.

4.5 Detailed ADC Implementation

A 50 MS/s 13b SAR-assisted pipeline ADC [50] is implemented to demonstrate the effectiveness of the fully-differential ring amplifier and FDAS first-stage CDAC switching. Figure 4.16 shows a detailed ADC block diagram and the timing for the prototype ADC. We implement a bootstrap clock generator [36] which distributes the sampling clock and deep N-well bias voltages to the input switches of the first-stage CDAC. The improved auto-zero

switching in [51] is used to eliminate the gain error caused by the parasitic capacitance across the auto-zero switch. The auto-zero capacitors, C_{AZ}, are implemented MIM capacitors to reduce bottom plate parasitic capacitance. The comparator (Figure 4.17) used in this ADC is a low noise single-phase dynamic latched comparator [58]. The one sigma offset of the first-stage comparator is designed to be lower than 0.1 LSB at 6b resolution to ensure that the first-stage offset error stays within the one bit digital correction range. The SAR DACs are implemented with custom designed encapsulated MOM capacitors, laid out in common centroid as shown in Figure 4.18. The letter A identifies the feedback capacitors for amplification, D identifies dummies to reduce the effects of edge conditions, 0 identifies the LSB dummies, and the other numbers identify the corresponding bits in the 6b DAC. The unit capacitance of the first-stage CDAC, C_1, is 7.9 fF and the unit capacitance of the second-stage CDAC, C_2, is 2.6 fF.

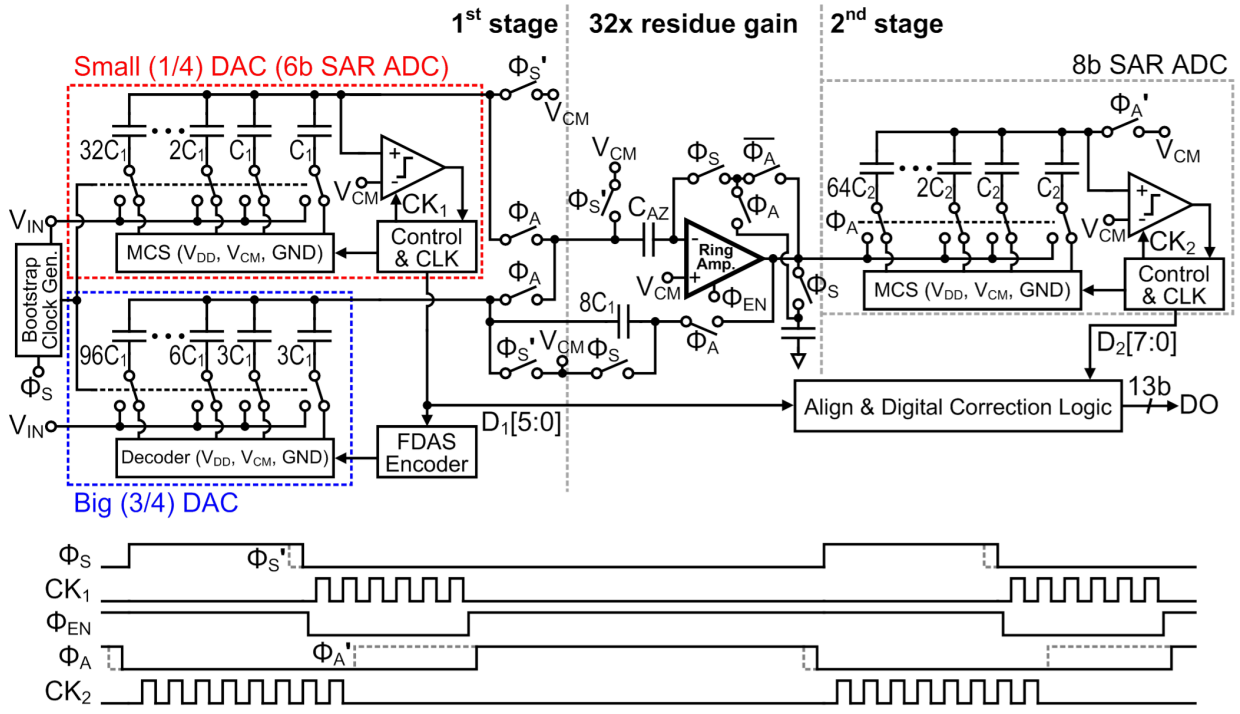

Figure 4.16. Block diagram and timing of the prototype ADC (Actual implementation is fully differential). CK_1, CK_2, and rising edges of Φ_{EN}, Φ_A and Φ_A' are asynchronously generated.

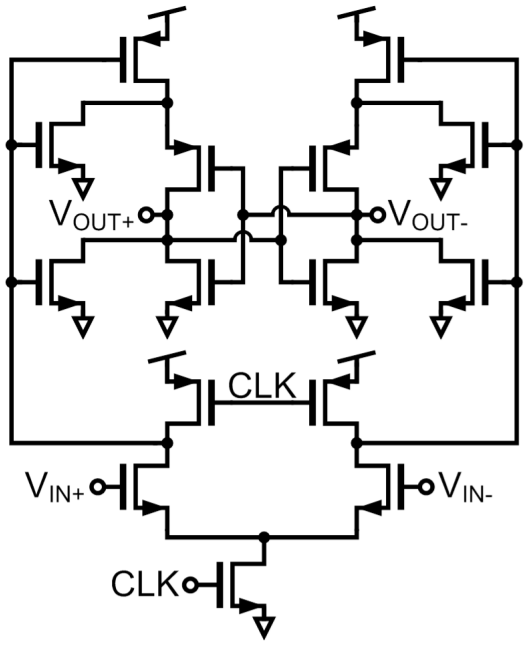

Figure 4.17. Low noise single phase dynamic latched comparator [58].

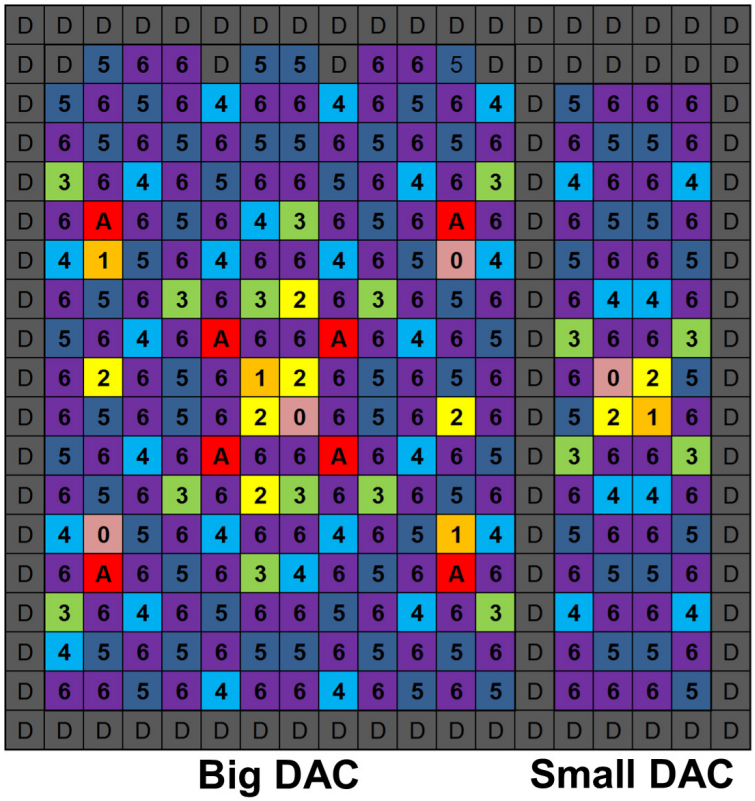

Figure 4.18. Common centroid first-stage CDAC layout map.

The ADC only requires a single reference voltage, V_{CM}, since it uses a full residue gain (32×), and both of the SAR ADCs support a rail-to-rail input. The SAR ADCs use V_{DD} and GND as the high and low references. The high reference is separated from the main V_{DD} in the chip and connected to the main V_{DD} on the test board for measurement purposes. The ADC requires a 25 % duty cycle 50 MHz external clock for sampling. All the other control signals are generated on chip.

4.6 Measurement Results

The prototype ADC is fabricated in a single-poly nine metal (1P9M) 1.2 V 65 nm CMOS process. The ADC occupies a small area of 0.054 mm^2, as shown in the die microphotograph in Figure 4.19. A summary of the measured performance is given in Table 4-1. The ADC output is decimated by two to avoid the effects of I/O switching noise on ADC performance. The ADC supports a full-scale rail-to-rail swing differential input signal of 2.4 $V_{pk\text{-}pk}$. The ADC achieves 13b linearity without calibration, thanks to the linearity improvement due to FDAS CDAC switching. Linearity plots (Figure 4.20) measured at 13b and at a full conversion rate of 50 MS/s, show that the measured DNL and INL are within -0.50 / +0.58 LSB and -0.83 / +0.96 LSB, respectively. As shown in the measured spectrums (Figure 4.21), at a 50 MS/s the ADC achieves 71.5 dB SNDR (11.6b ENoB), 71.9 dB SNR, and 87.0 dB SFDR with a 10.1 MHz input, and 70.9 dB SNDR (11.5b ENoB), 71.3 dB SNDR, and 84.6 dB SFDR with a Nyquist frequency input. Figure 4.22 summarizes the measured SFDR, SNR, and SNDR versus input frequency. The ADC has a quite flat SNDR response and higher than 83.9 dB SFDR for all input frequencies. The ADC has linear SNDR response up to the full-scale (Figure 4.23).

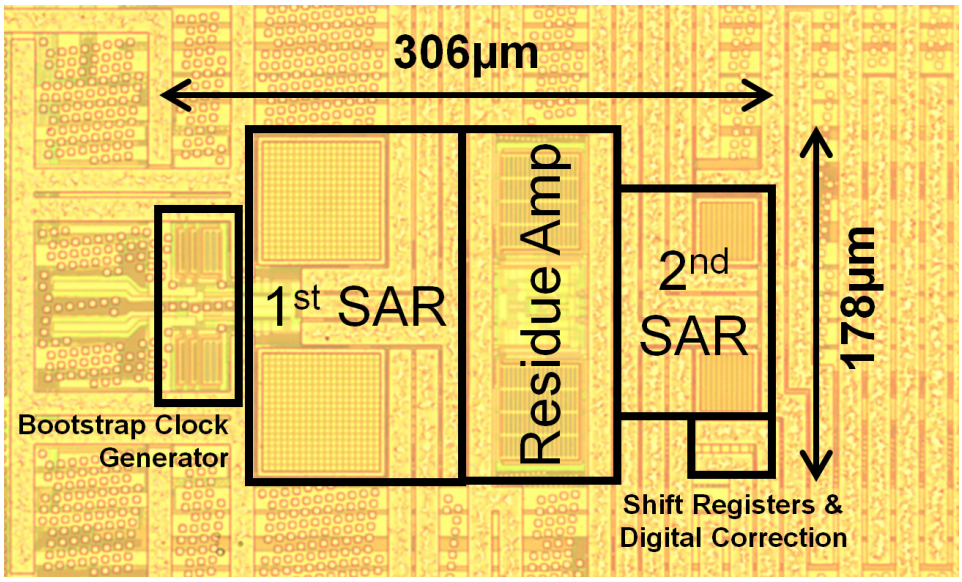

Figure 4.19. Die microphotograph of prototype ADC.

Table 4-1. ADC performance summary.

Resolution	13 bits	
Supply	1.2 V (Ring amp, SAR logic, V_{REF+}), 0.6 V (V_{CM}), 0.8 V (Shift register & digital correction)	
Sampling Rate	50 MS/s	
Technology	65 nm 1P9M CMOS	
Active Area	0.054 mm^2	
Input Range	2.4 V_{pk-pk} differential	
DNL	+0.58/-0.50 LSB	
INL	+0.96/-0.83 LSB	
Power Consumption	1 mW Total: 366 µW (Ring amp), 510 µW (SAR logic, bootstrapping clock), 95 µW (Ref.), 29 µW (Shift reg. & correction)	
	F_{in}=10.1 MHz	**F_{in}=24.95 MHz**
SNDR	71.5 dB	70.9 dB
SNR	71.9 dB	71.3 dB
SFDR	87.0 dB	84.6 dB
ENOB	11.6 bits	11.5 bits
FoM_W [$P/(F_s \cdot 2^{ENOB})$]	6.5 fJ/conv-step	6.9 fJ/conv-step
FoM_S [SNDR+10log(F_S/2/P)]	175.5 dB	174.9 dB

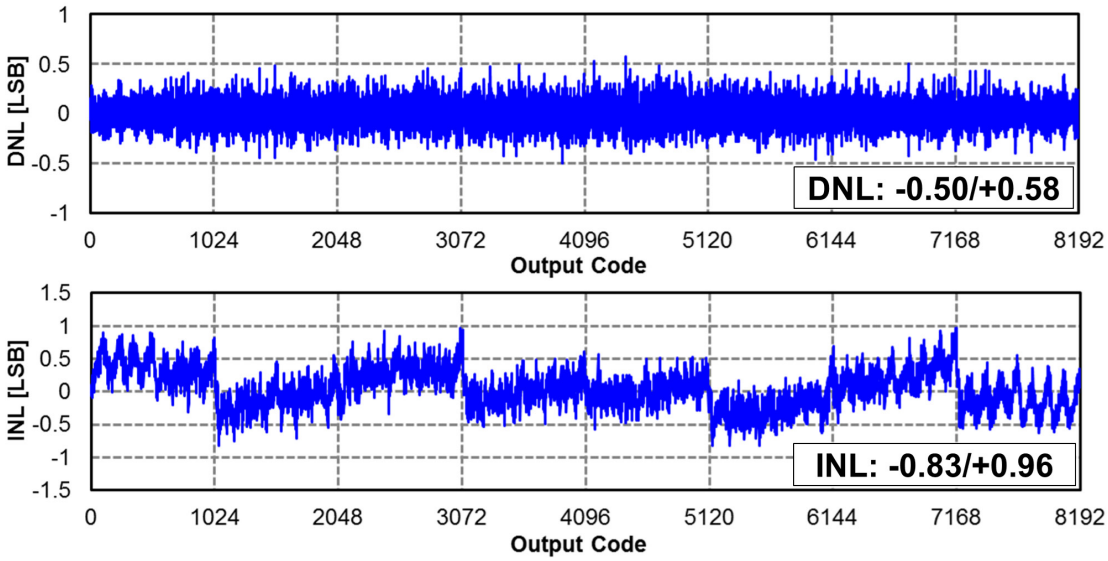

Figure 4.20. Measured DNL and INL at 50 MSPS (Decimated by 2).

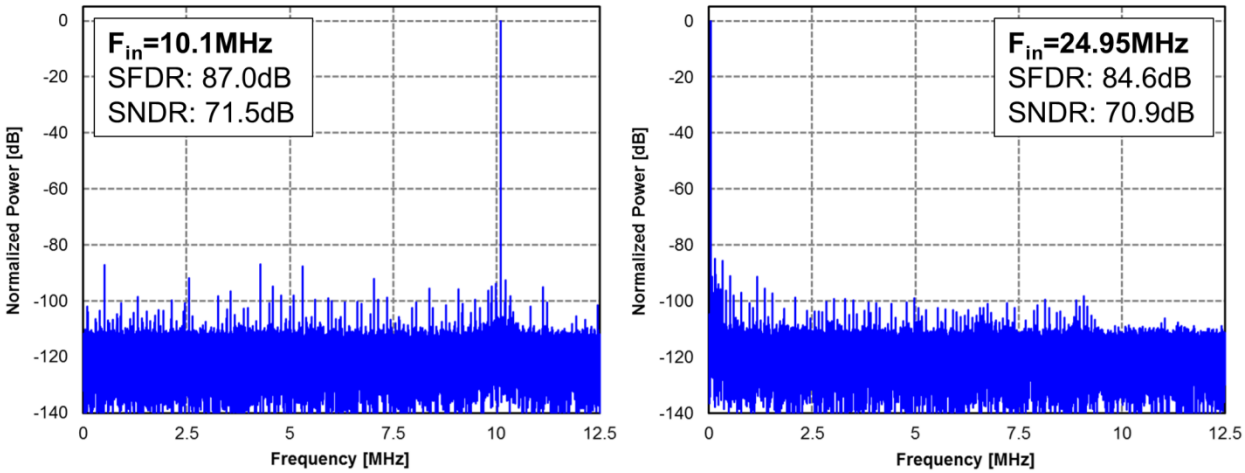

Figure 4.21. Measured spectrums for 10.1 MHz and 24.95 MHz inputs sampled at 50 MS/s (Decimated by 2, 65536 point FFT).

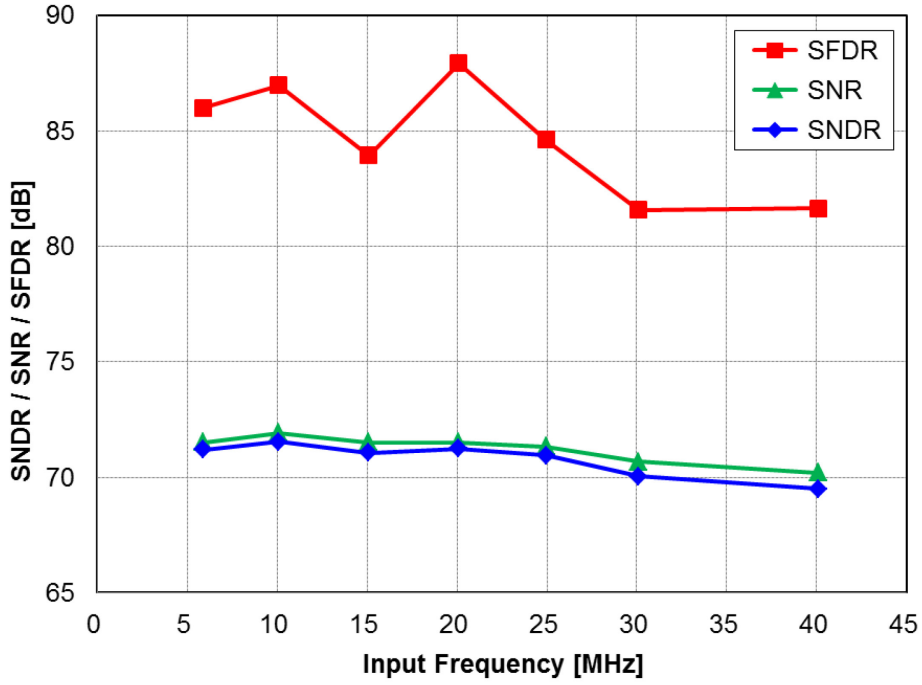

Figure 4.22. Measured SFDR, SNR, and SNDR versus input frequency (Decimated by 2).

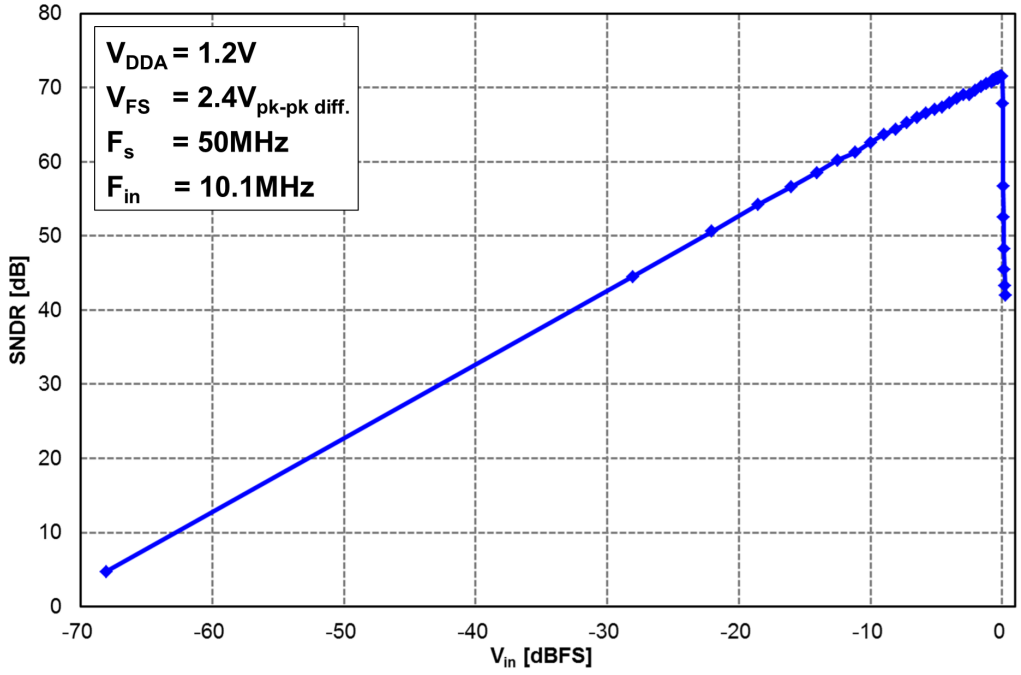

Figure 4.23. Measured SNDR versus input amplitude (Decimated by 2).

We swept the ring amplifier power supply voltage to check the robustness of the fully-differential ring amplifier. For a rail-to-rail input swing and a Nyquist frequency input, the SFDR and SNDR remain flat over a ring amplifier power supply voltage range from 1.15 V to 1.25 V (Figure 4.24), deviating by 0.73 dB and 0.45 dB, respectively. This proves that the fully-differential ring amplifier is very robust to supply voltage variation. The fully-differential ring amplifier has a flat gain response over supply voltage variation. The second-stage gain decreases when the supply voltage increases since the higher IR drop from the dynamic offset biasing resistor pushes the second-stage transistors towards the triode region. On the other hand, the higher offset voltage due to the increased IR drop leads the last stage operating deeper in the sub-threshold region resulting in a higher last stage gain. The gain changes in the second and the last stage are somewhat compensated; therefore the overall ring amplifier gain stays quite flat over a wide supply voltage range. Simulations indicate that the small signal gain of the fully-differential ring amplifier decreases by only around 1 dB over a supply voltage range from 1.15 V to 1.25 V. We also swept the ambient temperature to check the robustness of the fully-differential ring amplifier. The ADC has a higher than 81.0 dB measured SFDR and a higher than 69.7 dB measured SNDR over a -20 $^{\circ}$C to 80 $^{\circ}$C temperature range (Figure 4.25), proving that the fully-differential ring amplifier is also quite robust to temperature variation.

The ADC consumes a total power (excluding I/O) of 1 mW at the full conversion speed of 50 MS/s, with a Nyquist frequency input. This result is equivalent to Walden and the Schreier FoMs of 6.5 fJ/conversion·step and 175.5 dB, respectively, for 10.1 MHz input, and 6.9 fJ/conversion·step and 174.9 dB, respectively, for a Nyquist frequency input. The total power consumption is comprised of 366 μW for the ring amplifier, 510 μW for the SAR logics,

comparators, and the bootstrapping clock generator, 95 µW for the references, and 29 µW for the shift register and digital correction power.

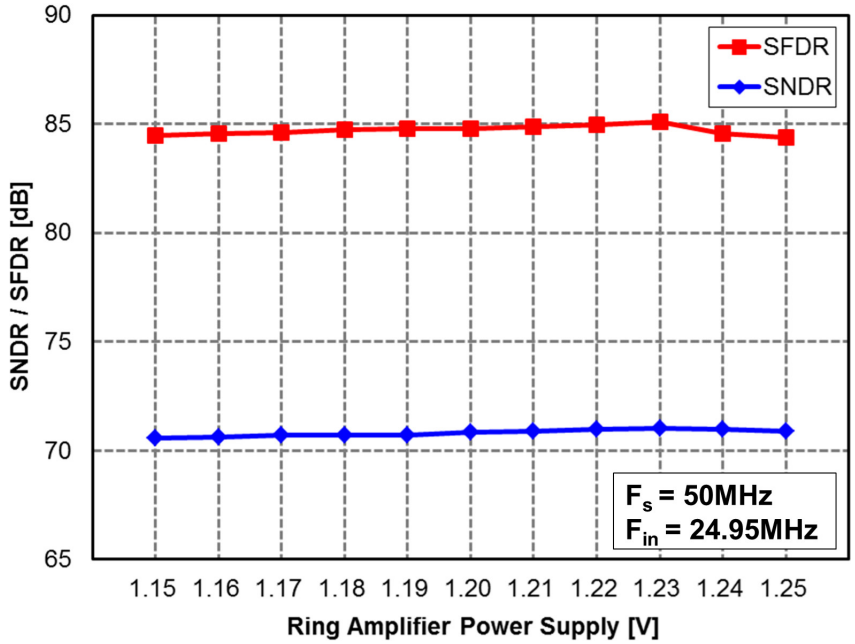

Figure 4.24. Measured SNDR and SFDR versus ring amplifier power supply (Decimated by 2).

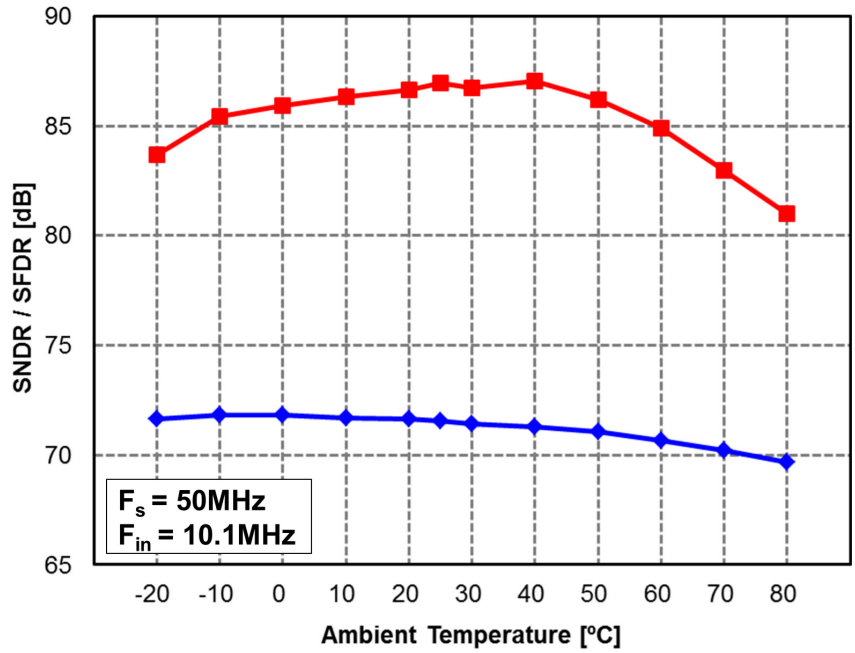

Figure 4.25. Measured SNDR and SFDR versus ambient temperature (Decimated by 2).

Table 4-2 compares the performance of the prototype ADC with conventional SAR-assisted pipeline ADCs. This work achieves less than 1 LSB INL at 13b resolution, and the highest SNDR and SFDR without calibration. In addition, this work has the best Walden and Schreier FoMs. Figure 4.26 and Figure 4.27 compare the Walden and the Schreier FoMs with ADCs presented at ISSCC 1997-2015 and VLSI symposium 1997-2014 [5]. This work achieves state-of-the-art Walden and Schreier FoMs.

Table 4-2. Performance comparison with the conventional SAR-assisted pipeline ADC.

	This Work	**VLSI 2010 [38]**	**ISSCC 2012 [42]**	**ISSCC 2014 [46]**	**VLSI 2014 [48]**
Resolution [bits]	13	12	14	14	14
F_S [MS/s]	50	50	30	80 (2x interleaved)	200 (2x interleaved)
Technology	65 nm CMOS	65 nm CMOS	130 nm CMOS	28 nm CMOS	28 nm CMOS
Active Area [mm^2]	0.054	0.16	0.24	0.137	0.35
Analog Supply [V]	1.2	1.3	1.2	1.0	0.9
ADC FS [$V_{pk\text{-}pk\ diff.}$]	2.4	2	2	1.4	-
Residue Amp. Structure	Fully diff. ring amplifier	Telescopic amplifier	Telescopic amplifier	Dynamic amplifier	Dynamic amplifier
Calibration	No	No	No	Yes (gain, offset, DAC)	Yes (gain, offset, DAC)
|INL| [LSB]	≤ 0.96	≤ 1.5	≤ 3.52	-	-
|DNL| [LSB]	≤ 0.58	≤ 0.75	≤ 0.89	-	-
Nyquist freq. SNDR [dB]	70.9	64.4	70.4	66.0	65.0
Nyquist freq. SFDR [dB]	84.6	75.0	79.6	74.0	-
Total Power [mW]	1.0	3.5	2.54	1.5	2.3
FOM_W [fJ/conv-step]	6.9	51.8	31.3	11.5	7.9
FOM_S [dB]	174.9	162.9	168.1	170.3	171.4

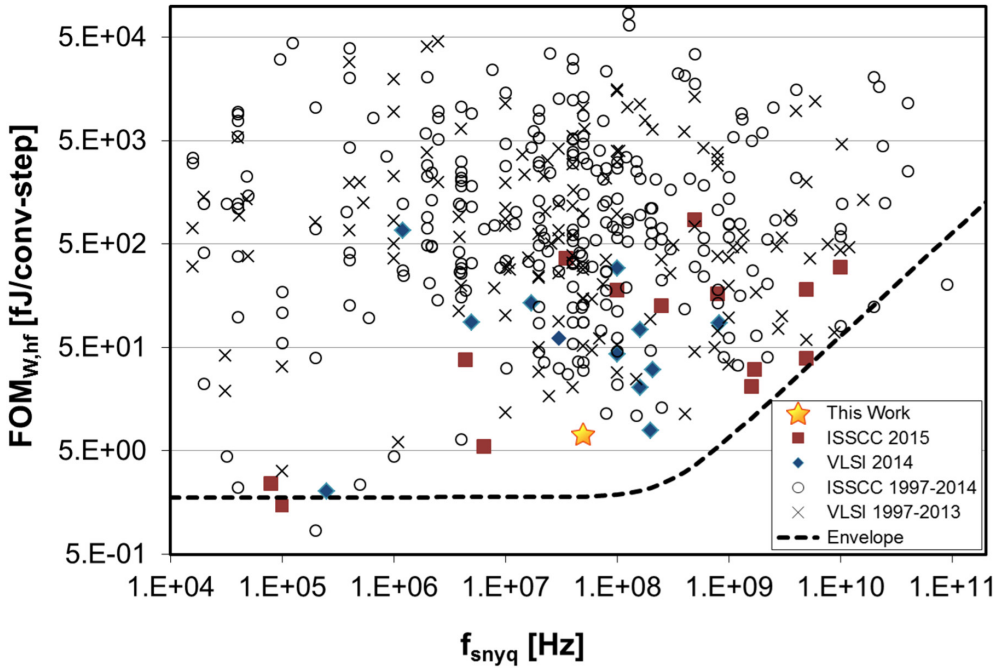

Figure 4.26. Walden FOM comparison with ADCs presented

at ISSCC 1997-2015 and VLSI 1997-2014 [5].

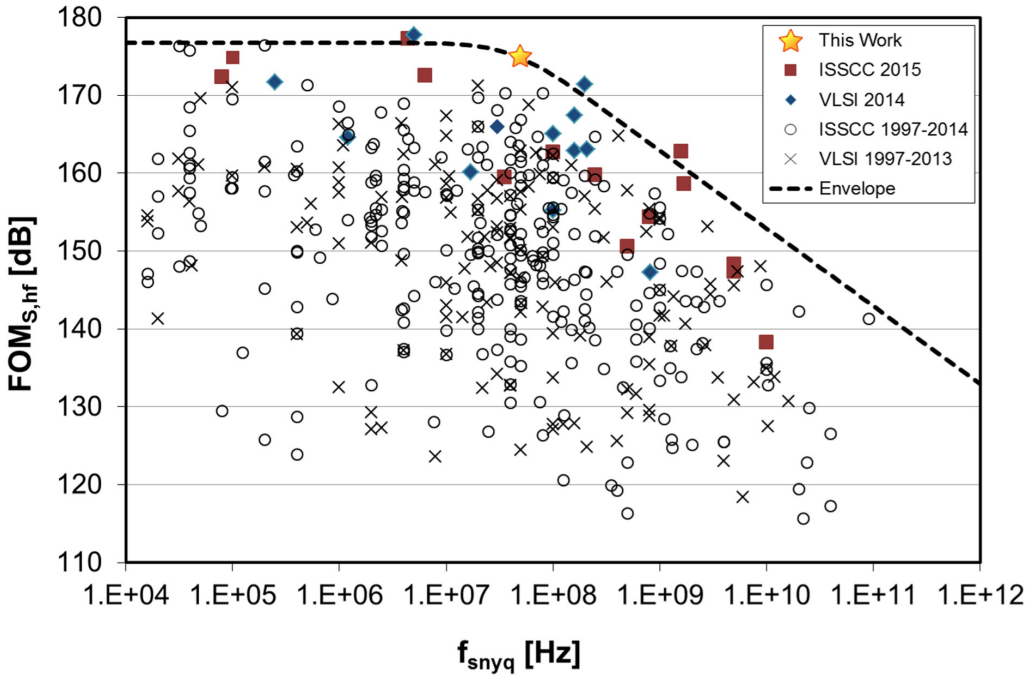

Figure 4.27. Schreier FOM comparison with ADCs presented

at ISSCC 1997-2015 and VLSI 1997-2014 [5].

4.7 Conclusion

This research introduces a fully-differential ring amplifier based SAR-assisted pipeline ADC. The new fully-differential ring amplifier solves the limitations of conventional single-ended ring amplifiers, and allows us to achieve power efficient amplification without calibration, thanks to energy-efficient slew-based charging, an almost rail-to-rail output swing, and higher overall gain. We introduce FDAS first-stage CDAC switching, which reduces the CDAC switching energy and also improves DAC linearity, by utilizing the differing noise requirements of the first-stage sub-ADC and MDAC. With these two techniques, the calibration free prototype ADC achieves 70.9 dB SNDR for a Nyquist frequency input sampled at 50 MS/s and consumes only 1 mW. The Walden and the Schreier FoMs of this work are 6.9 fJ/conversion·step and 174.9 dB, respectively, which are the best reported to date (as of December, 2015) for an ADC with a sampling speed faster than 6 MS/s.

CHAPTER 5

A Four-Stage Ring Amplifier Based SAR-Assisted Pipeline ADC

5.1 Introduction

As discussed in previous chapters, ring amplifiers [29], [30], [34], [50], [51], [59] are a compelling energy-efficient alternative to OTAs in switched-capacitor (SC) circuits. Ring amplifiers offer several benefits over OTAs including slew-based charging, near rail-to-rail output swing, and high gain from three stages. However, even though 80 dB gain from the fully-differential ring amplifier, discussed in the previous chapter, is quite high (especially in 65 nm CMOS process), it can only enable a resolution of up to 13b. Therefore, if we are targeting an even higher resolution, such as 15b, the gain of the three-stage ring amplifier is not enough. In addition, as the fabrication process scales down, it is getting harder to achieve enough gain for moderate resolution applications even with three stages because of the low intrinsic gain in advanced CMOS [17]. Although increasing the length of inverters or cascoding can increase ring amplifier gain, a drawback is that the increased output resistance significantly reduces the speed of the ring amplifier, resulting in limited performance.

In order to overcome this limitation of the conventional ring amplifiers, we present the first four-stage fully-differential ring amplifier. The additional stage degrades the speed of the ring amplifier much less than techniques that increase output resistance. We also propose an auto-zero noise filtering technique for the four-stage fully-differential ring amplifier to reduce auto-zero related noise without consuming extra power. This approach is more area efficient than the conventional auto-zero noise reduction method [16], [20]. In addition, we introduce a SAR CDAC layout method with identical unit cell and routing which is compact and free from systematic mismatch. We verify these new techniques with a 15b 100 MS/s calibration-free SAR-assisted pipeline ADC [60].

The remainder of this chapter is organized as follows; Section 5.2 introduces the new four-stage fully-differential ring amplifier. Then, Section 5.3 presents the auto-zero noise filtering technique, Section 5.4 gives a detailed description of the ADC implementation, and Section 5.5 introduces a systematic mismatch free SAR CDAC layout method. Finally, in Section 5.6, we present measurements of the prototype ADC, and conclude the chapter in Section 5.7.

5.2 Four-Stage Fully-Differential Ring Amplifier

In this section, we briefly review why a straightforward four-stage ring amplifier is not applicable for a feedback network. Then, we introduce the four-stage fully-differential ring amplifier and give a detailed explanation of its operation.

5.2.1 Problems of a Straightforward Four-Stage Ring Amplifier

Making a four-stage fully-differential ring amplifier may sound straightforward, such as by simply adding one more stage to the three-stage fully-differential ring amplifier discussed in the

previous chapter, as shown in Figure 5.1. However, unlike the case with three-stage ring amplifiers, making a dominate pole at the output of the final stage [51] does not properly stabilize the straightforward four-stage ring amplifier. This is because in feedback, the common mode of a four-stage ring amplifier can latch to the supply voltage or the ground. Latching happens because the four-stage ring amplifier has positive common mode signal gain. Therefore, although the differential signal feedback forms a negative feedback to the first-stage, as shown in Figure 5.1, the common mode signal forms a positive feedback which results in latching.

Similar to the case of the three-stage fully-differential ring amplifier discussed in the previous chapter, passive CMFB techniques, such as SC CMFB through the second stage tail current bias and triode device based CMFB [52] for both differential amplifiers can be used in this straight forward ring amplifier. However, the common mode feedback path open loop gain of these techniques is not high enough to suppress the positive common mode gain of the four-stage main signal path, for preventing latching. This is especially problematic when we consider the input common mode offset and the unity gain feedback factor for auto-zero.

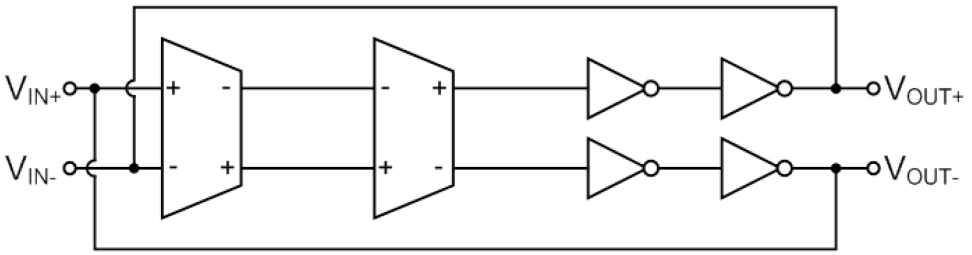

Figure 5.1. A four-stage ring amplifier in a feedback network.

In theory, an active CMFB circuit shown in Figure 5.2 could prevent this common mode latching, however such a CMFB circuit must dominate the feedback loop and thus it would consume almost as much power as the ring amplifier itself. Therefore, it is not an energy efficient solution. This is especially challenging during auto-zero as the feedback factor is high.

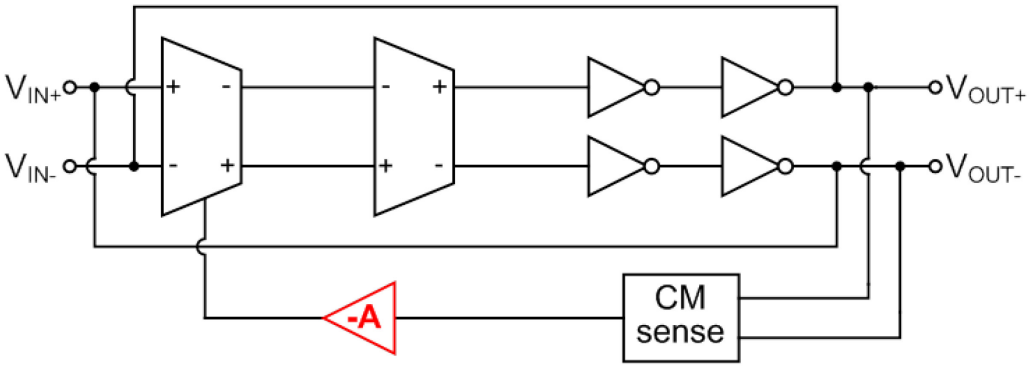

Figure 5.2. A four-stage ring amplifier in a feedback network with an active CMFB.

5.2.2 Auto-Zero with Second-Stage Auxiliary Amplifier

In order to solve the common mode latching problem when operating in feedback, we introduce a new auto-zero technique that uses the second-stage auxiliary amplifier, as shown in Figure 5.3. This modified auto-zero avoids common-mode latching because it operates through negative feedback for both the differential signal and the common mode signal.

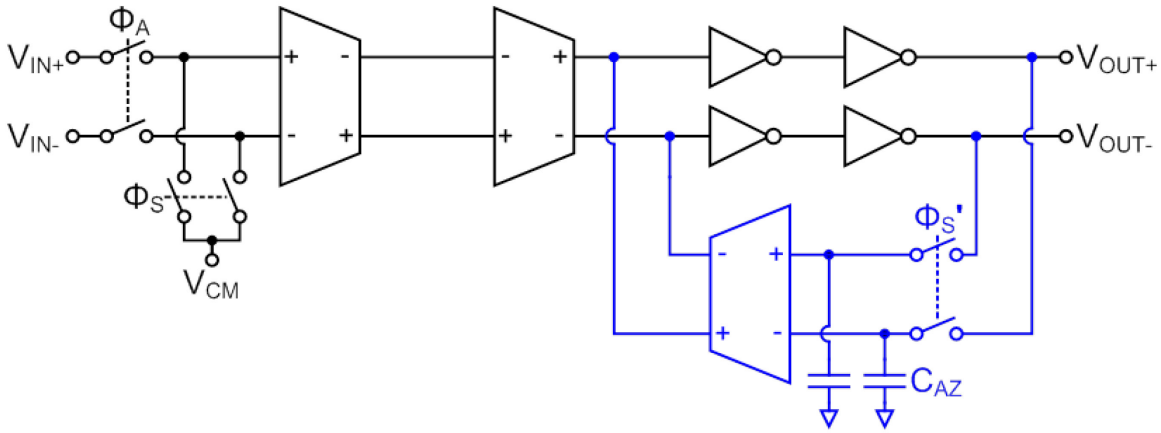

Figure 5.3. Proposed four-stage ring amplifier with second stage auxiliary amplifier auto-zero.

The auto-zero works as the follows. In the auto-zero phase (i.e. Φ_S is high), the input of the first-stage is connected to the common mode bias, V_{CM}. Next, the three-stage feedback through the auxiliary second-stage amplifier samples the output offset of the first-stage and the input

offsets of the second to fourth stages onto the auto-zero capacitors, C_{AZ}. In order to stabilize the feedback and reduce the noise folding of the auto-zero, relatively big C_{AZ} capacitors (4 pF) are used. However, the use of big C_{AZ} capacitors does not cause a significant area penalty. We can use high density MOS capacitors stacked with MOM capacitors to minimize area since one node of C_{AZ} is always connected to ground.

During the amplification phase (i.e. Φ_A is high), the sampled offset in C_{AZ} cancels the entire ring amplifier offset, thus a ring amplifier based SC residue amplifier performs offset free residue amplification. Another benefit of this auto-zero method is the drain to source parasitic capacitance of the auto-zero switches does not cause gain mismatch during the application phase [34], [51] since the auto-zero switches are not in the main signal path of the amplification phase.

After auto-zero, the output common mode of the SC residue amplifier using the four-stage ring amplifier always starts from near the desired common mode. This is because auto-zero cancels not only the offset in the differential signal path but also the offsets in the common signal path. Since the output common mode is near the desired common mode and the feedback factor of the amplification phase is much lower than one (for example 1/65 for gain of 64×), we can reliably set the common mode of the four-stage ring amplifier with passive only CMFB during the residue amplification phase.

5.2.3 Four-Stage Ring Amplifier

The four-stage ring amplifier (Figure 5.4) consists of a first-stage differential pair, two second-stage differential pairs in parallel, two third-stage inverters with dynamic biasing resistors, R_B, and two last-stages inverters. One of the second-stage differential pairs is the main signal amplifier, and the other is an auxiliary amplifier for auto-zero.

The differential pairs reuse current in PMOS and NMOS input devices. This reuse maximizes transconductance for a given bias current thus reducing thermal noise. NMOS triode-device CMFBs in the first and second stage differential pairs (marked as 1st stage CMFB and 2nd stage CMFB) set the common mode of the differential pairs, which works as coarse CMFB for the entire ring amplifier during the auto-zeroing and the residue amplification period. A separate SC CMFB controls the tail current biases in the second-stage to set the ring amplifier output common mode to V_{CM} during the residue amplification period.

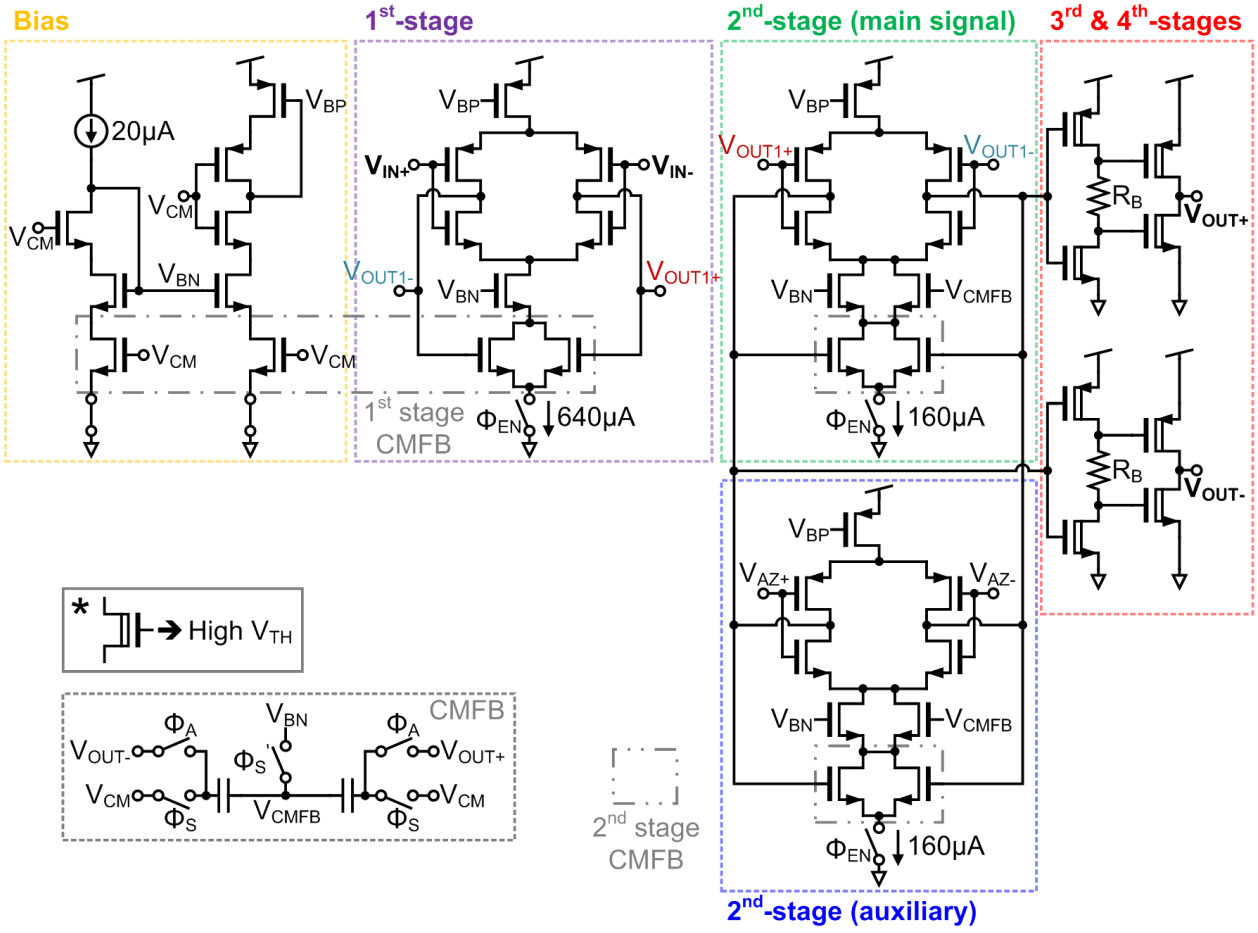

Figure 5.4. Four-stage fully-differential ring amplifier and biasing.

The third and fourth stages use exactly the same architecture as that of the last two stages of the fully-differential ring amplifier [50], [59]. We adopt high V_{th} devices for the fourth-stage to extend the high output resistance offset biasing range. In the third-stage, high V_{th} devices increase the third-stage gain by extending the third-stage output voltage range for which the transistors operate in saturation region. The resistors, R_B, in the third-stages dynamically apply offset voltages to the last-stages using the short circuit current of the third-stage. The replica biasing circuit [59] forces the ring amplifier produces the highest gain when the inputs are around V_{CM}. Enable switches controlled by Φ_{EN} turn off the ring amplifier when it is not used to save power. The simulated small-signal gain of the ring amplifier is higher than 90 dB over an output swing from 0.1 V to 1.0 V with a 1.1 V supply.

5.3 Auto-Zero Noise Reduction

In this section, we briefly review the benefits and problems of auto-zero, as well as the conventional auto-zero noise reduction method. Then, we introduce a new auto-zero noise filtering technique and compare its benefits with existing techniques through simulation results.

5.3.1 Review of Auto-Zero

Auto-zero offers several benefits for SC circuits [16]. Auto-zero cancels amplifier offset by sampling the offset with offset sampling capacitors during the auto-zero phase and subtracting the sampled offset from the signal path during the amplification phase. This maximizes the redundancy error correction range for SC residue amplifier based MDAC pipeline stages, since it maximizes the usable output swing range. Auto-zero also cancels low frequency noise, such as flicker (1/f) noise. For low frequency noise (i.e. compared to the auto-zero frequency), the noise can be approximated as an offset thus it is canceled out along with the amplifier offset. Another

important benefit of auto-zero is it helps stabilize the common mode by canceling the common mode offset, as discussed in the previous section.

However, a problem of auto-zero is it increases the overall SC circuit noise. When the offset sampling capacitors sample the amplifier offset, they also sample the thermal noise of the amplifier. The sampled noise adds to the amplifier noise during the amplification phase in the offset canceling process since the thermal noise of the amplifier in the auto-zero phase and the amplification phase are uncorrelated. In order to reduce this auto-zero related noise, larger offset sampling capacitors are used to reduce the amplifier thermal noise bandwidth during the auto-zero phase [20].

5.3.2 Auto-Zero Noise Filtering

Instead of using larger offset sampling capacitors, we directly filter out the dominant first-stage noise to save area. We add additional first-stage loading capacitors, C_F in Figure 5.5, to reduce the bandwidth of the first-stage during auto-zero, thus filtering the first-stage noise during the auto-zero phase. This is possible because the first-stage is not connected in the feedback path in the auto-zero configuration. C_F is connected some delay after the beginning of the auto-zero phase (using Φ_F) to prevent slow initial settling of the first-stage. This insures that the output of the first-stage always settles to its output offset even with the reduced bandwidth. In order to sufficiently filter out the first-stage noise, C_F needs to be quite large (8 pF). However, the use of a large capacitance does not increase the first-stage power consumption because the sampled voltage in C_F is almost the same for every cycle. During the amplification phase, C_F is disconnected from the first-stage to achieve high first-stage bandwidth as is required to stabilizes the four-stage ring amplifier in the feedback network.

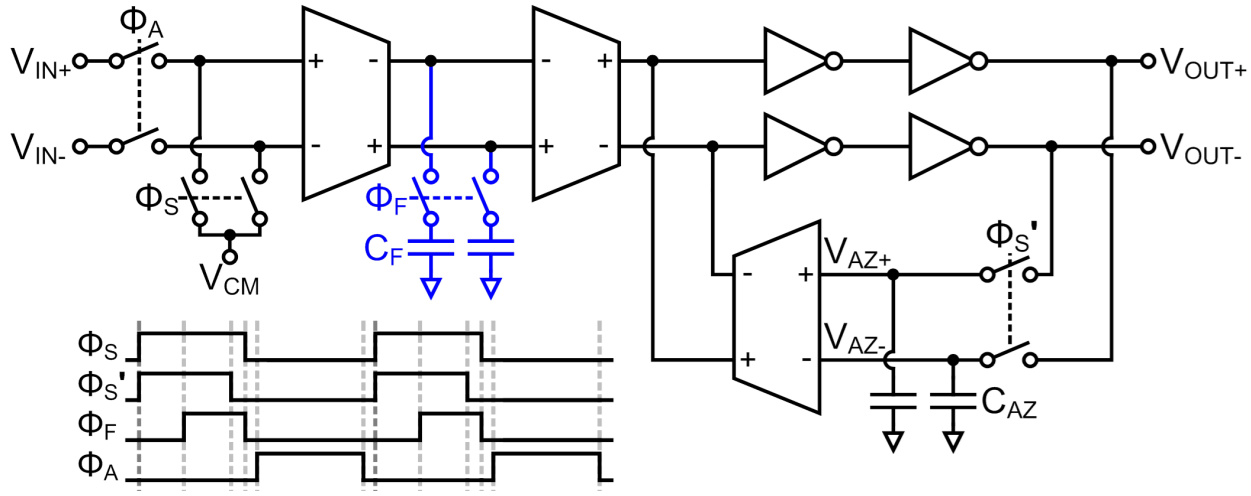

Figure 5.5. Simplified four-stage ring amplifier in auto-zero configuration and timing diagram.

In order to compare the noise reduction efficiency of our auto-zero noise filtering technique with the conventional auto-zero noise folding reduction method, we performed transient noise simulations with 10,000 simulation iterations. The output auto-zero noise of 64× gain residue amplifier is calculated by subtracting the output noise power of an ideal auto-zero 64× gain residue amplifier from the output noise power of the actual auto-zero 64× gain residue amplifier and then take the square root of the subtraction result to get the RMS noise. This method isolates the auto-zero noise from other circuit noise sources, including the ring amplifier noise during the amplification phase and the input kT/C noise. The ideal auto-zero residue amplifier is implemented using ideal voltage sources which have the exact offset voltages instead of using C_{AZ} capacitors and auto-zero switches. This eliminates the auto-zero related noise in the ideal auto-zero amplifier by removing the ring amplifier noise sampling of the auto-zero operation.

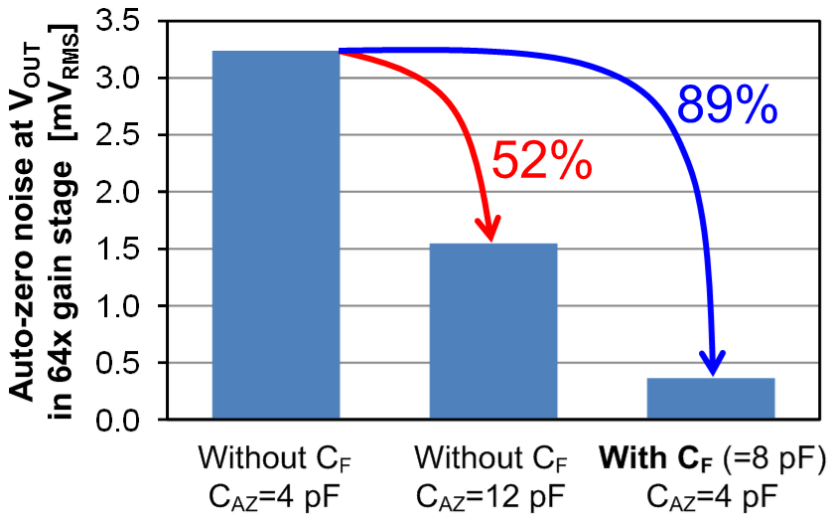

Figure 5.6. Auto-zero noise filtering transient noise simulation.

Figure 5.6 summarizes the transient noise simulation results. As a default, 4 pF of C_{AZ} is used without the auto-zero noise filtering method giving a 3.2 mV RMS output auto-zero noise. When we apply the conventional auto-zero noise folding reduction method which we increase C_{AZ} by 8 pF (total 12 pF C_{AZ}), the RMS output auto-zero noise is reduced by 52%. In contrast, when we use the additional 8 pF of capacitance for our auto-zero noise filter, C_F, it reduces the RMS output auto-zero noise by 89%. This proves that the auto-zero noise filtering reduces the noise far more efficiently than with the same additional capacitance when compared with conventional auto-zero noise folding reduction using a larger C_{AZ} [20]. This is because the auto-zero noise filtering method reduces the thermal noise bandwidth more with the additional 8 pF capacitance than that of the conventional method.

5.4 ADC Implementation

The four-stage ring amplifier is implemented in a SAR-assisted pipeline ADC [60]. Figure 5.7 shows the simplified ADC architecture and Figure 5.8 shows the block diagram and timing of the ADC. The ADC comprises of a 7b first-stage SAR ADC, a 64× residue gain stage, and a 9b second-stage SAR ADC. With one bit of stage redundancy, the ADC resolves 15b after digital correction. The first-stage CDAC is divided into separate *Big* (4 pF, 32 fF of unit C_B) and *Small* (128 fF, 1 fF of unit C_S) *CDACs* to reduce switching energy and to improve linearity through floated-detect and skip (FDAS) switching [50], [59]. In order to further improve the first stage CDAC switching energy and linearity from our in the previous chapter, we increase the ratio between *Big* and *Small CDAC* from 3:1 to 31:1, and generate the residue only with *Big CDAC* as in [53]. *Big* and *Small CDACs* sample the same input, and then *Small CDAC* performs high-speed SAR conversion. *Big CDAC* generates a low noise residue voltage by applying the decision of *Small CDAC* SAR ADC with FDAS encoding. FDAS switching reduces *Big CDAC* switching energy by 74 % and worst case RMS INL by 52 % avoiding need for calibration [50], [59]. The comparator used in this ADC is a low noise single-phase dynamic latched comparator [58]. The SAR ADCs use merged capacitor switching (MCS) [54] and asynchronously generated clocks.

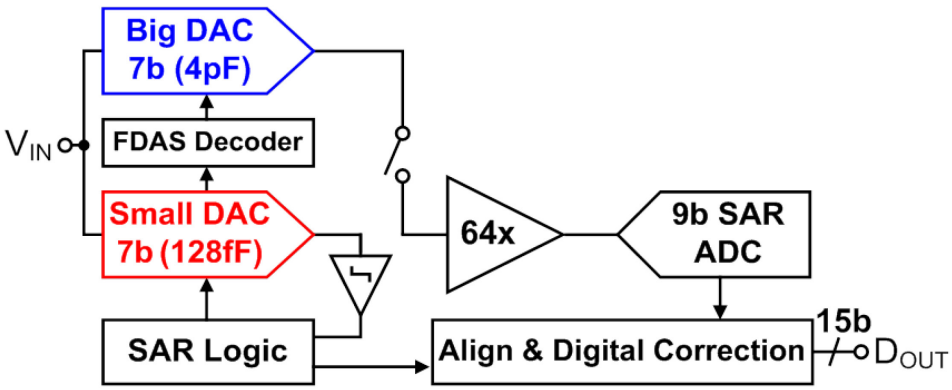

Figure 5.7. Simplified ADC architecture.

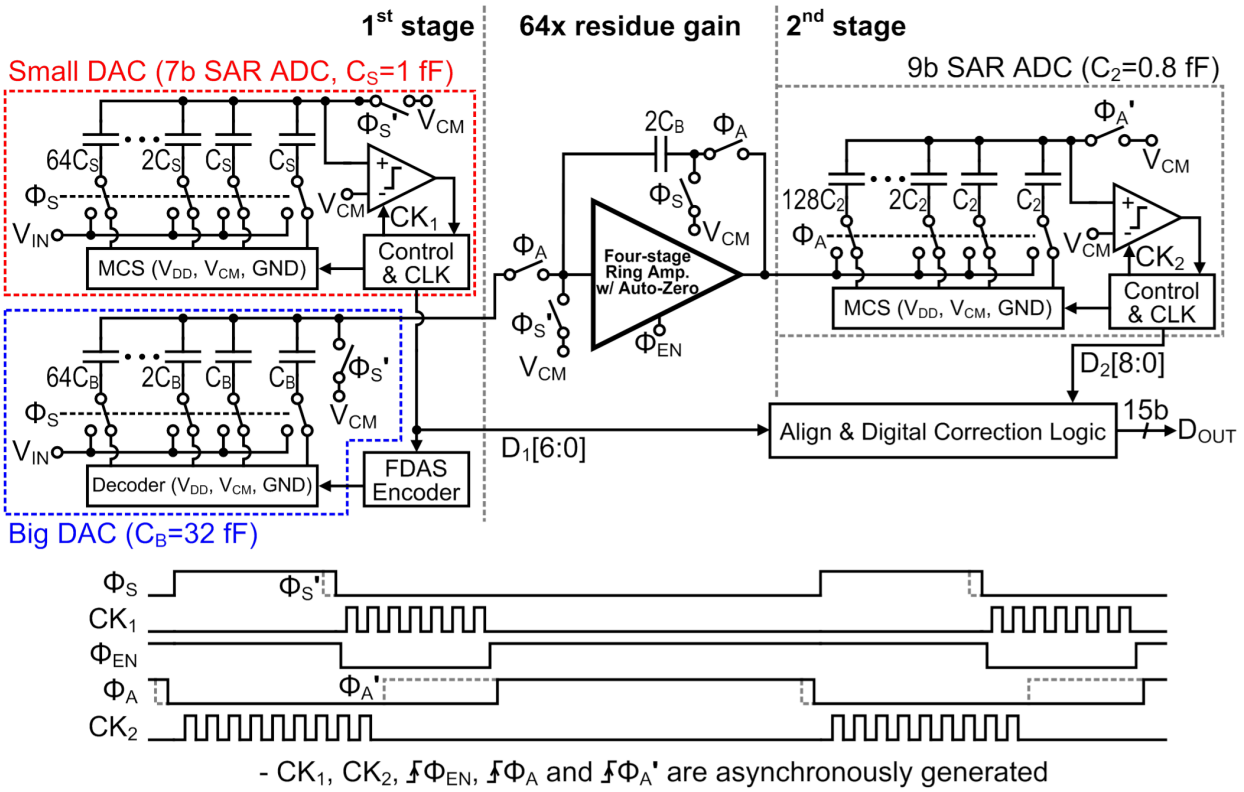

Figure 5.8. Block diagram and timing of the ADC (Actual implementation is fully differential).

The ADC only requires a single reference voltage, V_{CM}, since it uses a full residue gain (64×), and both of the SAR ADCs support a rail-to-rail input. The SAR ADCs use V_{DD} and GND as the high and low references. The high reference is separated from the main V_{DD} on chip and connected to the main V_{DD} on the test board for measurement purposes. The ADC requires a 25 % duty cycle 100 MHz external clock for sampling. All the other control signals are generated on chip.

5.5 Systematic Mismatch Free SAR CDAC Layout

The SAR CDACs are implemented with fully symmetric (including bottom plate routing) MOM capacitors, laid out in common centroid to minimize systematic mismatch. Figure 5.9 shows *Big CDAC* common centroid layout map. The letter A identifies the feedback capacitors for amplification, D identifies dummy structures to reduce the effects of edge conditions, 0 identifies the LSB dummy, and the other numbered capacitors are related to the corresponding bits in the 7b DAC. Although a common centroid CDAC layout is desirable to compensate the first order gradient related systematic mismatch, the required complex bottom plate routing may cause a systematic mismatch which can causes a big INL error in the middle of an INL graph.

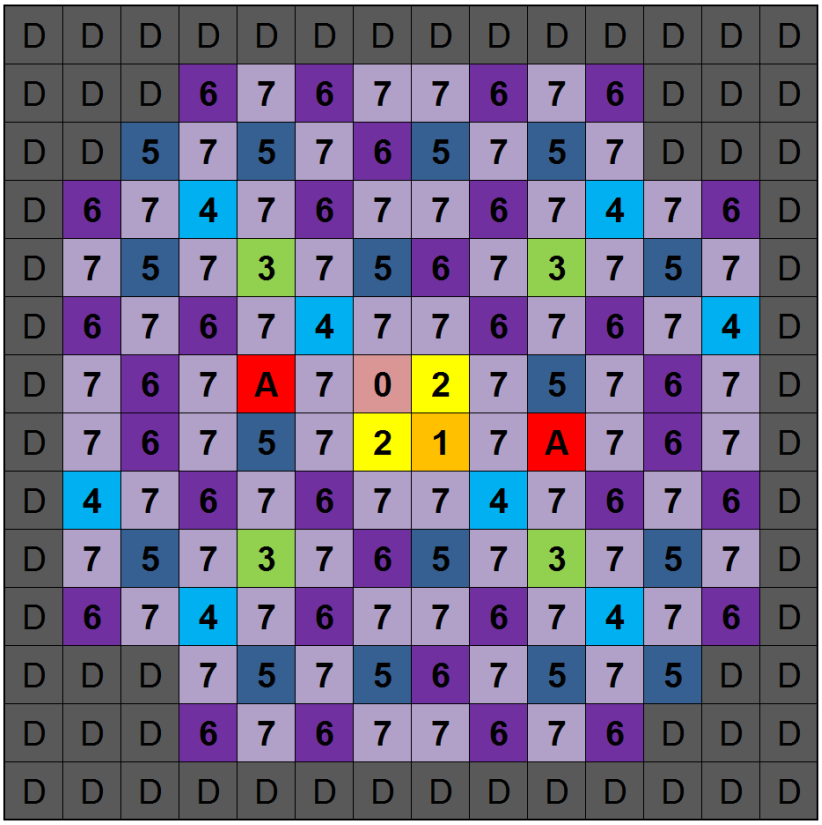

Figure 5.9. Common centroid first-stage *Big CDAC* layout map.

In order to avoid the systematic mismatch caused by the complex bottom plate routing, we use a custom-designed encapsulated MOM capacitor as shown in Figure 5.10, which prevents unwanted parasitic capacitance to the top plate. It consists of an M2 solid plane bottom plate, via2 to via7 bottom plate side walls, M3 to M7 MOM capacitors with bottom plate side walls, via3 to via6 top plate connections, and an M8 solid plane bottom plate. We rotate even numbered metal MOM capacitors 90° to maximize the capacitance.

To route the top plate, as shown in Figure 5.11, we modified M5 MOM capacitors adding more top plate fingers, cut out M5 bottom plate side wall, and bring three M5 top plate fingers outside of the bottom plate capsule. In addition, we shield the M5 top plate routing using M4, via4, via5, and M6 by extending the bottom plate side walls to prevent unwanted parasitic capacitances from the bottom plate routings.

In order to prevent systematic mismatch caused by complex bottom plate routing, we route the bottom plates with uniform routing patterns using vertical M1 strips under the M2 bottom plate as shown in Figure 5.12. This also makes the CDAC layout compact. Each M1 strip is assigned to a corresponding CDAC bit. However, if we connect a M1 strip to M2 bottom plate using via1 under M2 plate as shown in Figure 5.12, the via1 may cause unwanted bumps or dents during the fabrication process. These bumps or dents on the M2 bottom plate can be a source of systematic mismatch. In order to prevent this via1 caused systematic mismatch, we add a tab on the M2 bottom plate as shown in Figure 5.13 and place the via1 connections under the tab.

With the proposed encapsulated MOM capacitor, and the top and bottom plate routing methods, we can make a compact CDAC layout with identical cell and routing patterns as shown in Figure 5.14. The only differences between the capacitors are the via1 connection locations.

Since the CDAC layout consists of almost exactly the same patterns without unwanted parasitic capacitances to the top plate, the CDAC is free from systematic mismatch.

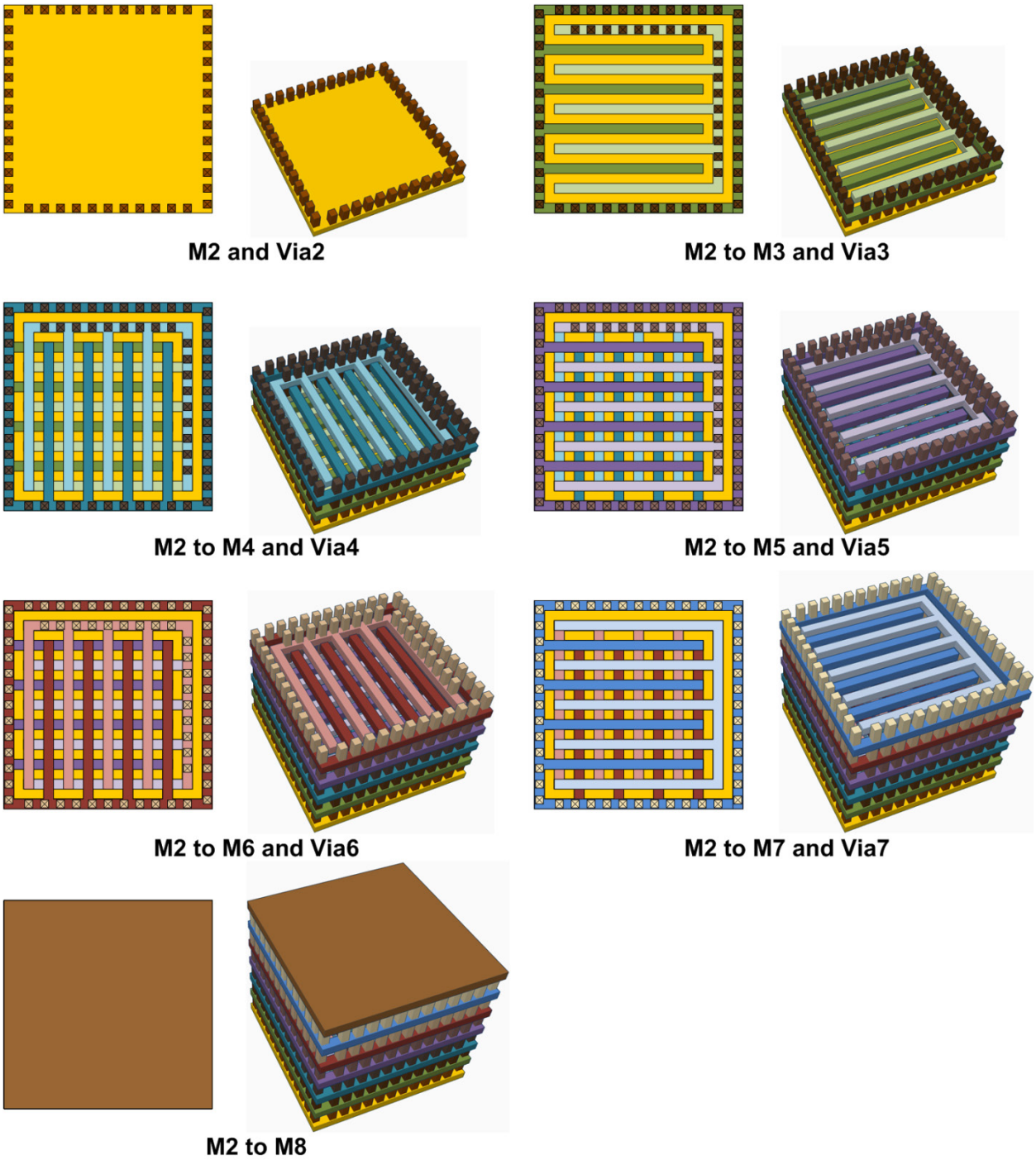

Figure 5.10. Custom designed encapsulated MOM capacitor top and 3D view.

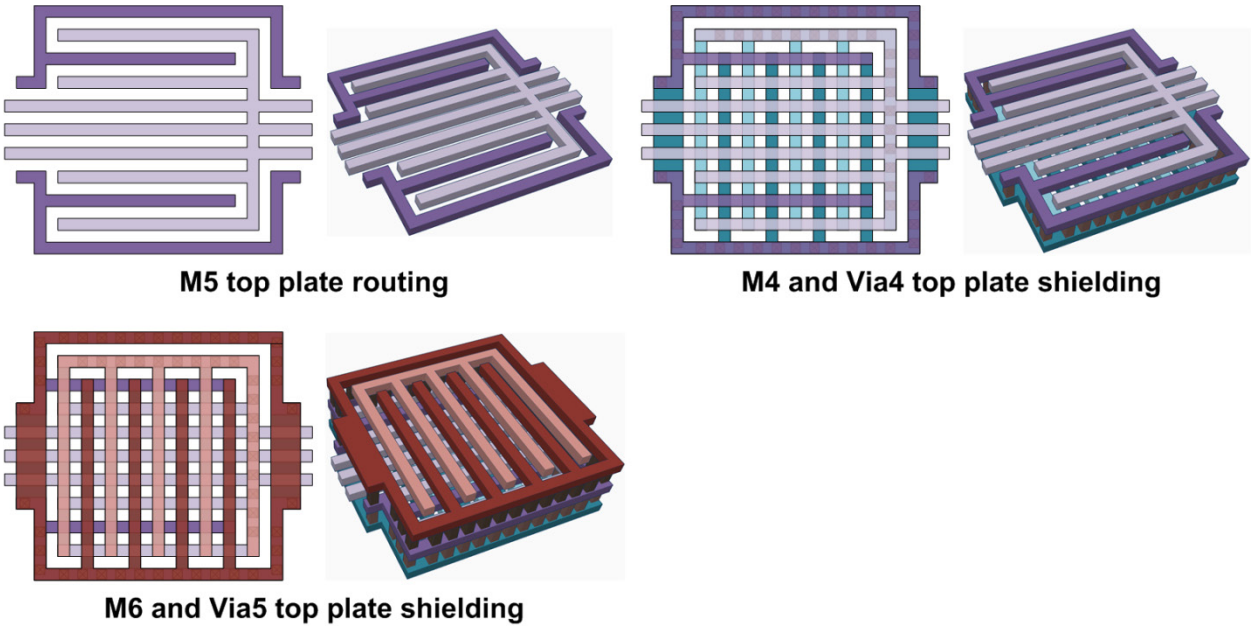

Figure 5.11. Top plate routing and shielding top and 3D view.

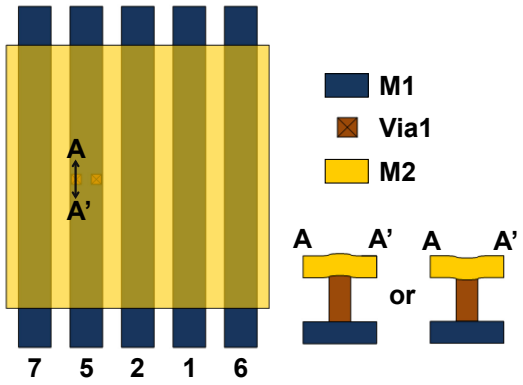

Figure 5.12. Bottom plate routing with M1 strips and via1 connections under M2 bottom plate.

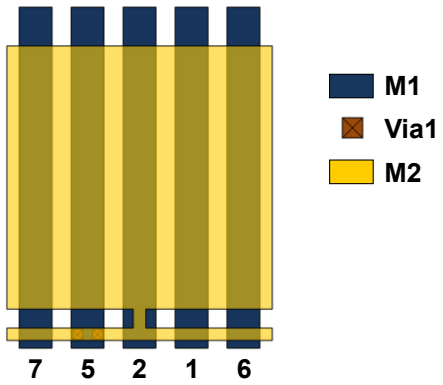

Figure 5.13. Bottom plate routing via1 connections under an additional M2 tab.

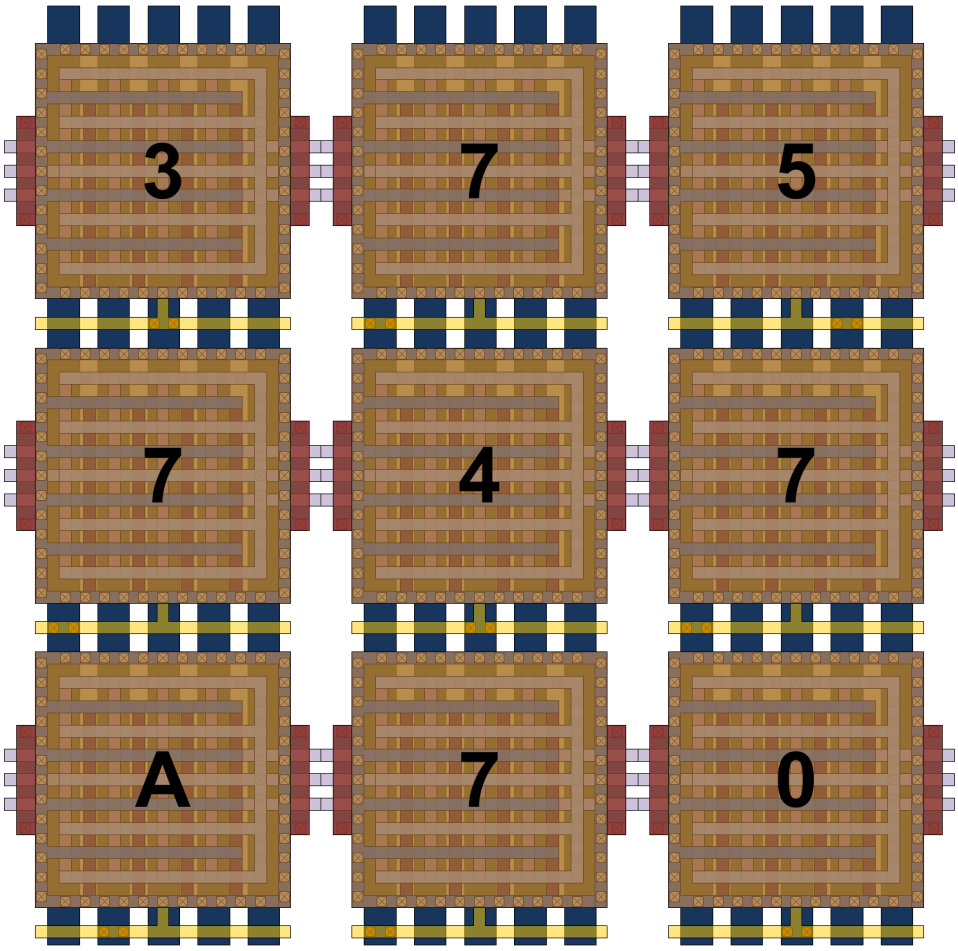

Figure 5.14. Partial Big CDAC common centroid layout.

5.6 Measured Results

The prototype ADC is fabricated in a single-poly ten metal (1P10M) 40 nm CMOS and runs from a 1.1 V supply voltage. The ADC occupies 0.068 mm^2 as shown in the die microphotograph in Figure 5.15. Thanks to the wide output swing of the ring amplifier, the maximum input swing is a rail-to-rail 2.2 Vpk-pk even with the 64× full residue gain. The ADC output is decimated by two to avoid the effects of I/O switching noise on ADC performance. The measured DNL and INL at 15b and at a full conversion rate of 100 MS/s are -0.56/+0.67 LSB and -2.31/+2.19 LSB, respectively (Figure 5.16) which achieves almost 14b linearity without calibration thanks to the linearity improvement from FDAC CDAC switching and the systematic

mismatch free CDAC layout. As shown in the measured spectrums (Figure 5.17), at 100 MS/s the ADC achieves 73.2 dB SNDR (11.9b ENoB), 73.3 dB SNR, and 90.4 dB SFDR with a 5.9 MHz input. The auto-zero noise filtering improves SNDR by 1.2 dB (13% noise reduction) without extra power consumption.

The ADC consumes a total power (excluding I/O) of 2.3 mW at the full conversion speed of 100 MS/s. This result is equivalent to Walden and the Schreier FoMs of 6.0 fJ/conversion·step and 176.6 dB, respectively, for 5.9 MHz input. The total power consumption is comprised of 994 µW for the ring amplifier, 1065 µW for the SAR logics, comparators, and the bootstrapping clock generator, 182 µW for the references, and 59 µW for the shift register and digital correction power. Table 5-1 summaries the ADC performance.

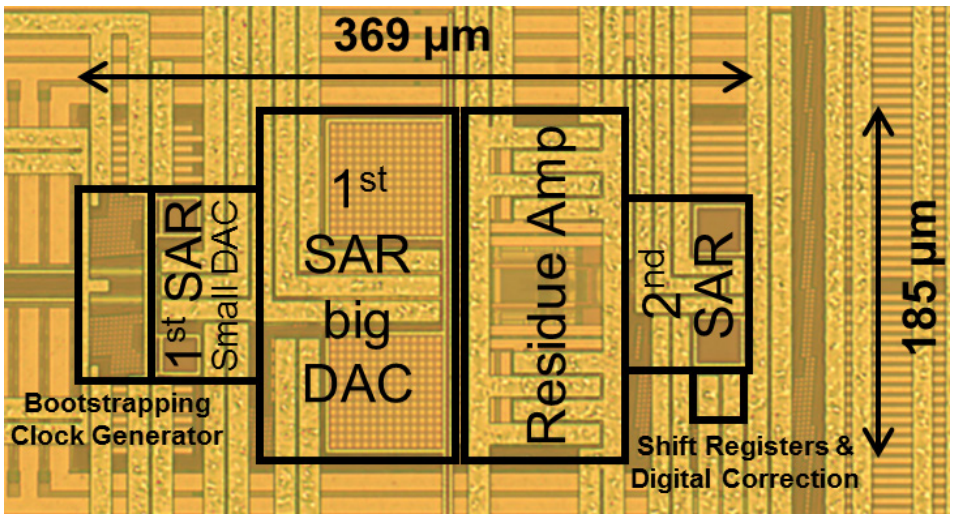

Figure 5.15. Die microphotograph.

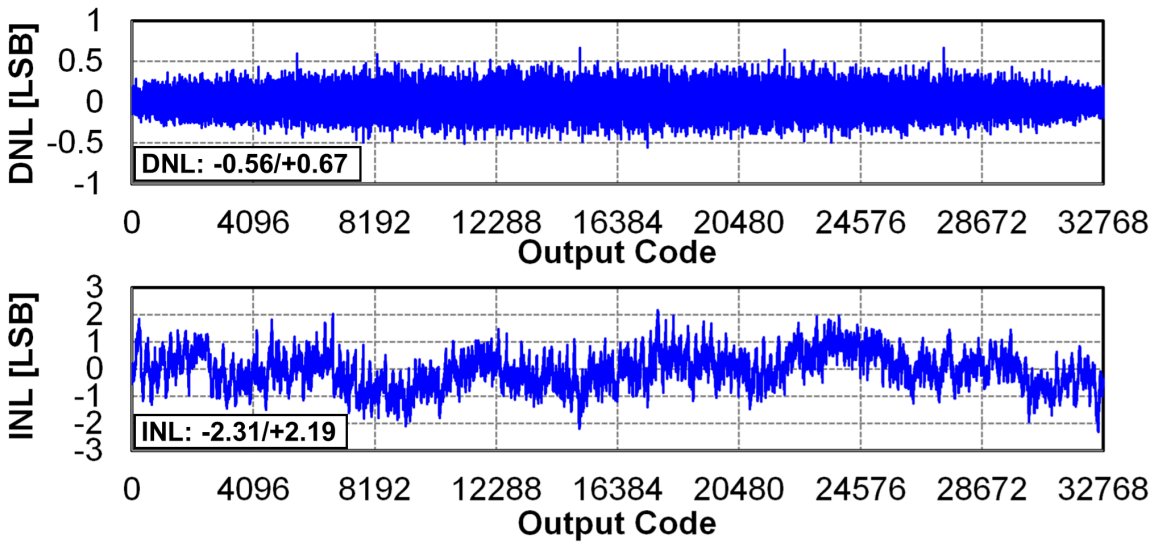

Figure 5.16. Measured Linearity.

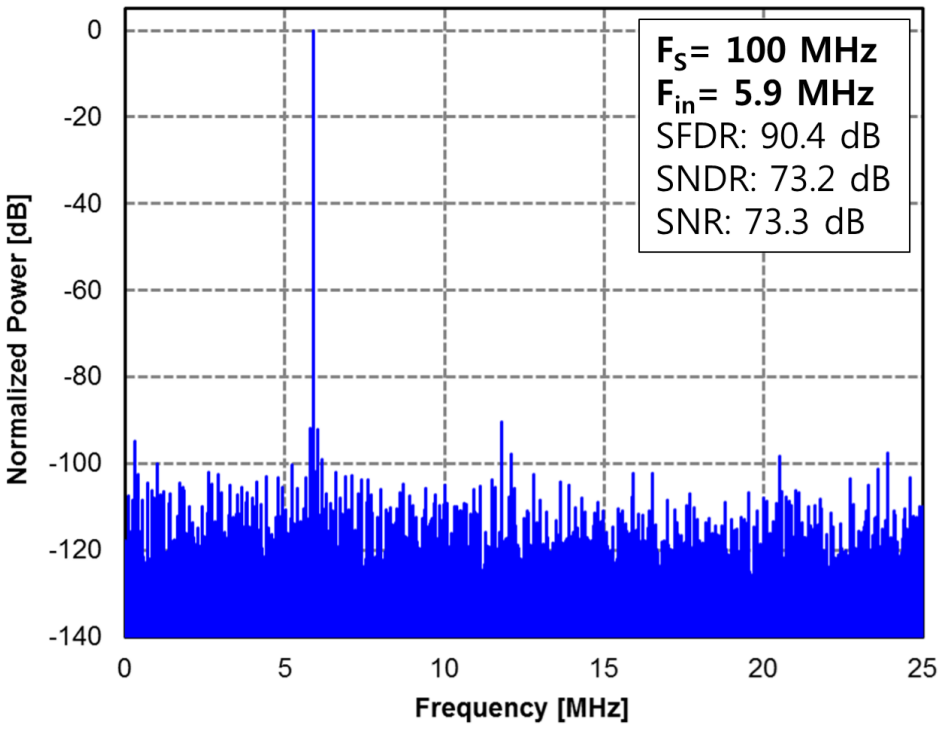

Figure 5.17. Measured spectrums for 5.9 MHz inputs sampled at 100 MS/s

(Decimated by 2, 2^{20} point FFT).

Table 5-1. ADC Performance Summary.

Resolution	15 bits
Analog Supply	1.1 V
Sampling Rate	100 MSPS
Technology	40 nm 1P10M CMOS
Active Area	0.068 mm^2
Input Range	2.2 V_{pk-pk} differential
SNDR	73.2 dB @ 5.9 MHz Input
SNR	73.3 dB @ 5.9 MHz Input
SFDR	90.4 dB @ 5.9 MHz Input
ENOB	11.9 bits @ 5.9 MHz Input
DNL with 15 bits output	-0.56 / +0.67 LSB
INL with 15 bits output	-2.31 / +2.19 LSB
Total Power	2.3 mW (excluding only I/O power)
FoM_W	6.0 fJ/conv-step
FoM_S	176.6 dB

Table 5-2 compares the performance of the prototype ADC with conventional SAR-assisted pipeline ADCs and SAR-assisted digital slope ADC [61]. This work achieves the lowest worst case INL at 15b resolution, and the highest SNDR and SFDR without calibration. In addition, this work has the best Schreier FoM. Figure 5.18 compares the Schreier FoM with ADCs presented at ISSCC 1997-2016 and VLSI symposium 1997-2016 [5]. This work achieves a state-of-the-art Schreier FoM.

Table 5-2. Performance comparison with the conventional two-stage SAR ADC.

	This Work	ISSCC2015 [50] (Ch. 4)	ISSCC2016 [61]	ISSCC2014 [46]	VLSI2014 [48]
Resolution [bits]	15	13	12	14	14
F_S [MS/s]	100	50	100	80 (2x interleaved)	200 (2x interleaved)
Technology	40nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS	28nm CMOS
Active Area [mm^2]	0.068	0.054	0.0047	0.137	0.35
Analog Supply [V]	1.1	1.2	0.9	1.0	0.9
ADC FS [$V_{pk\text{-}pk\ diff.}$]	2.2	2.4	1.6	1.4	-
Residue Amp. Structure	Four-stage ring amplifier	Three-stage ring amplifier	None (digital slope 2nd stg)	Dynamic amplifier	Dynamic amplifier
Calibration	No	No	Yes (offset, DAC)	Yes (gain, offset, DAC)	Yes (gain, offset, DAC)
|INL| [LSB]	≤ 2.31	≤ 0.96 (3.8 @15b)	≤ 0.82 (6.56 @15b)	-	-
|DNL| [LSB]	≤ 0.67	≤ 0.58	≤ 0.53	-	-
SNDR [dB]	73.2	70.9	64.4	66.0	65.0
SFDR [dB]	90.4	84.6	75.4	74.0	-
Total Power [mW]	2.3	1.0	0.35	1.5	2.3
FOM_W [fJ/conv-step]	6.0	6.9	2.63	11.5	7.9
FOM_S [dB]	176.6	174.9	176.0	170.3	171.4

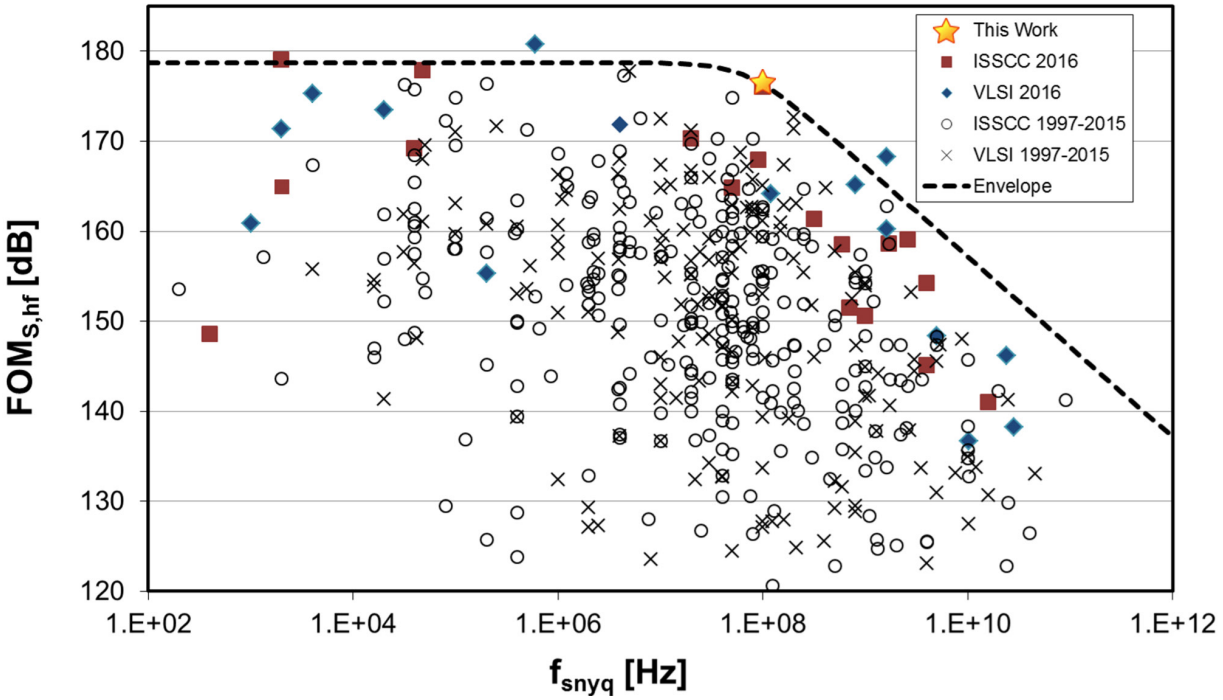

Figure 5.18. Schreier FOM comparison with ADCs presented

at ISSCC 1997-2016 and VLSI 1997-2016 [5].

5.7 Conclusion

This research introduces a four-stage fully-differential ring amplifier based SAR-assisted pipeline ADC. The new four-stage fully-differential ring amplifier further improves the gain of the ring amplifier without sacrificing speed while maintaining the benefits of the ring amplifiers such as energy-efficient slew-based charging, an almost rail-to-rail output swing. We also introduce a novel auto-zero noise reduction technique which filters out the dominant first-stage noise directly without extra power consumption, and has better area efficiency than the conventional auto-zero noise folding reduction method. In addition, we introduce a SAR CDAC layout method with identical unit cells and routing which is compact and is free from systematic mismatch. With these three techniques, the calibration-free prototype ADC achieves 73.2 dB SNDR and 90.4 dB SFDR for a 5.9 MHz input sampled at 100 MS/s and consumes only 2.3 mW. The auto-zero noise filtering improves SNDR by 1.2 dB. The Walden and the Schreier FoMs for this work are 6.0 fJ/conversion·step and 176.6 dB, respectively, which are state-of-the-art energy efficiency.

CHAPTER 6

Conclusion

The use of OTAs based SC amplifier for pipeline ADCs residue amplifier has limited the energy efficient of conventional pipeline ADCs. Not only are OTAs power hungry, but it is also getting harder to implement high gain and wide swing OTAs in advanced CMOS processes because of the reduced device intrinsic gain and supply voltage. The ring amplifier is an attractive alternative to OTAs for SC circuits, and has several benefits over OTAs such as energy efficient slew based charging, near rail-to-rail output swing, and easily achievable high gain from cascaded three stages. However, the use of external reference voltage based floating capacitor biasing makes the conventional ring amplifier vulnerable to PVT variation and thus limits its practicality. In addition, the single ended architecture of the conventional ring amplifier makes it susceptible to even-order distortion, and has limited common-mode and supply rejection. The research outlined in this dissertation developed more energy efficient and practical ring amplifiers and implemented energy efficient pipeline ADCs using these ring amplifiers. As shown in the Schreier FoMs comparison chart (Figure 6.1), this work achieves state-of-art energy efficient ADCs with three innovative ring amplifiers.

The first part of this dissertation introduces an innovative self-biased ring amplifier which makes the ring amplifier more practical and power efficient. The use of high V_{TH} devices for the

last stage inverter extends the stable operating bias range for the last stage. The dynamic offset voltage biasing using embedded resistor in the second stage inverter eliminate the need of external biasing and enables entire three stage auto-zeroing which improves PVT variation tolerance. Furthermore, the reduced supply voltage of the first stage inverters further improves the energy efficiency of the ring amplifier. In addition, we use the intermediate output of the self-biased ring amplifier for sub-ADC decision of the next pipeline ADC stage which eliminate dedicated comparators for sub-ADC, thus further improves the energy efficiency of the pipeline ADC. The proposed techniques are verified in a 10.5b 100 MS/s comparator-less pipeline ADC fabricated in a 65 nm CMOS process. The measured SNDR, SNR and SFDR are 56.6 dB (9.11b), 57.5 dB and 64.7 dB, respectively, and the ADC consumes 2.46 mW. This result is equivalent to an FoM_W of 46.1 fJ/ conversion·step and FoM_S of 159.7 dB, which are state-of-art for pipeline ADCs using conventional architectures.

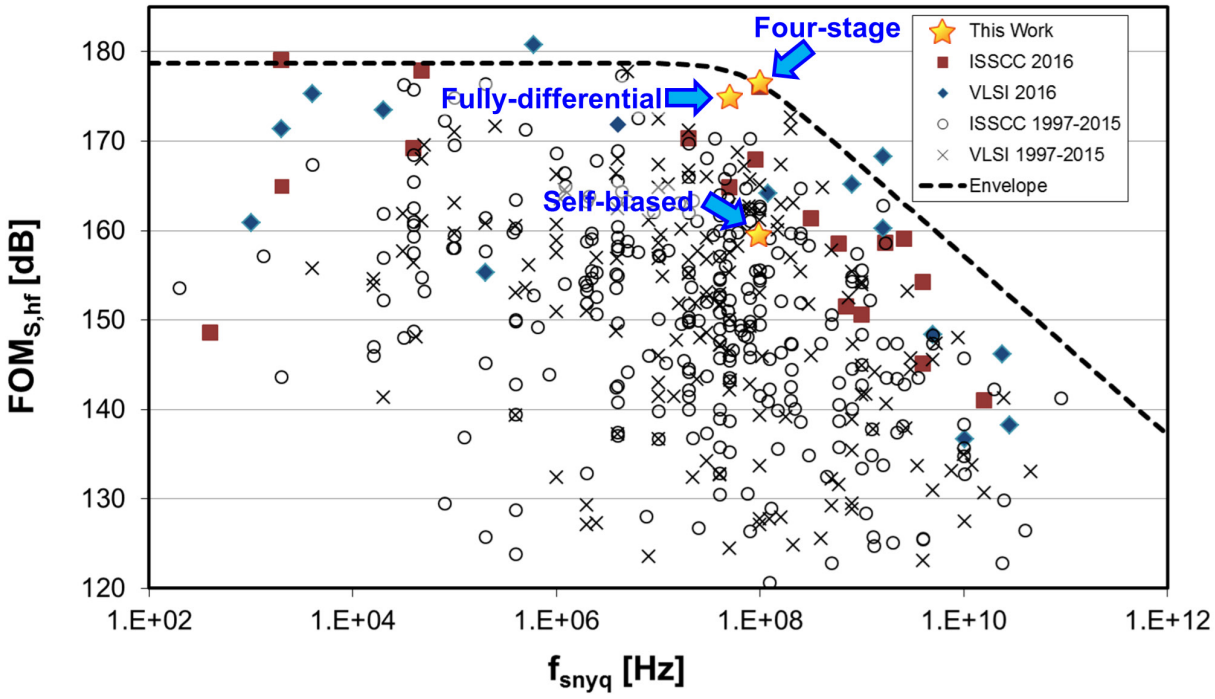

Figure 6.1. Schreier FOM comparison with ADCs presented

at ISSCC 1997-2016 and VLSI 1997-2016 [5]

The second part of this dissertation introduces a novel fully-differential ring amplifier. The replacement of the first stages inverters with differential pairs makes the ring amplifier fully differential. Current reuse differential pairs maximize the transconductance for a given bias current. The fully-differential ring amplifier is verified in a 13b 50 MS/s SAR-assisted pipeline ADC fabricated in a 65 nm CMOS. In order to further improve the energy efficiency of the SAR-assisted pipeline ADC, an improved first stage SAR CDAC switching method, named floated detected-and-skip (FDAS) is also proposed. FDAS improves both switching energy efficiency and linearity of the CDAC. The measured SNDR, SNR and SFDR are 70.9 dB (11.5b), 71.3 dB and 84.6 dB, respectively, and the ADC consumes 1 mW. This measured performance is equivalent to a Walden and Schreier FoMs of 6.9 fJ/conversion·step and 174.9 dB, respectively, which are the best reported as of December, 2015 for an ADC with a sampling speed faster than 6 MS/s.

The last parts of this dissertation introduces a new four-stage fully-differential ring amplifier which further enhances the gain of the ring amplifier without sacrificing the speed. The auto-zero using a second stage auxiliary amplifier insures stable auto-zeroing and prevents the common mode latching during the amplification phase. A novel auto-zero noise filtering technique is also proposed which eliminates about 90% of auto-zero related noise by filtering out the dominant first stage noise during auto-zeroing. In addition, a compact SAR CDAC layout method is presented that is systematic mismatch free by using common centroid layout with identical unit cells and routing. These techniques are verified in a 15b 100 MS/s SAR-assisted pipeline ADC fabricated in a 40 nm CMOS process. The measured SNDR, SNR and SFDR are 73.2 dB (11.9b), 73.3 dB and 90.4 dB, respectively, and the ADC consumes 2.3 mW resulting in a state-of-the-art FoM_W of 6.0 fJ/conversion·step and FoM_S of 176.6 dB.

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