Advanced Nanofabrication Technologies for Processing Layered Semiconductors and Device Applications

by

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Dedication

For everyone who has gently touched my life,

I dedicate this dissertation to all of you.

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Abstract

Two-dimensional layered semiconductor materials, such as transition metal dichalcogenides (TMDCs), recently received a great deal of interest due to their excellent electronic, optoelectronic and mechanical properties, as well as large abundance of relevant bulk materials on earth. Especially for semiconductor-related applications, TMDCs can be used for making highly sensitive sensors, high-performance thin-film transistors (TFTs) that are potentially immune to short-channel effects, and ultra-thin flexible photovoltaic (PV) and photodetection devices.

However, to utilize layered semiconductors for innovative device applications, we still need to (i) create scalable manufacturing methods with a high throughput for device production, (ii) develop proper material processing technologies to generate stable and reproducible doping effects in 2D semiconductors, therefore enabling diverse optoelectronic and electronic applications, (iii) advance the device physics to leverage the uniquely advantageous electronic, structural, and mechanical properties of TMDCs in device application fields, such as information processing and data storage.

The research presented in this dissertation sought to address the challenges mentioned above with a special focus on the following three topics: (1) development of nanoimprint/nanoprint-based processes for producing device structures based on layered semiconductors; (2) invention of a plasma-assisted doping technology for making TMDC-based nanoelectronic devices such as rectifying diodes and ambipolar transistors; (3) fabrication and

characterization of TMDC-based memory devices with multi-bit storage capability, simple device structure, and low production cost.

The first part of my thesis presents a nanoimprint/nanoprint-based method for fabricating TMDC-based (*e.g.*, MoS_2, WSe_2) field-effect transistors. The field effect transistors (FETs) made from produced multilayer MoS2 flakes exhibit very consistent performance with high on/off ratios in the range of 10^5 -10^7. The characterization data measured from these FETs show that produced MoS2 flakes have a high uniformity of electronic properties.

The second part of my thesis presents a novel plasma-assisted doping technology for modulating the electronic properties of layered semiconductor materials such as TMDCs. Taking MoS_2 as an exemplary TMDC under study, *via* plasma doping, we have demonstrated *p*-type MoS_2 transistors that can be complementary to pristine *n*-type MoS_2 transistors, potentially enabling applications in CMOS circuits. Moreover, *via* applying plasma doping for selected areas, we have created 2D diodes with high rectification degrees and a superior long-term stability at room temperature.

The third part of my thesis presents a study on the abnormal charge-trapping and memory characteristics of few-layer WSe_2 transistors. In addition, I present an innovative device application of MoS_2 in making floating-gate-free, non-volatile, multi-bit memory FETs, which has a unique combination of excellent retention/endurance characterisitcs, simple device structures and extremely low fabrication cost.

These presented works provide nanofabrication and material processing solutions for making nanoelectronic devices based on emerging layered semiconductors, which can be generally utilized for making a broad range of functional devices based on various layered materials (*e.g.*, graphene and topological insulators). Especially, the plasma doping method

demonstrated in my research holds the potential to be further developed into an industrial material processing technology for precisely tailoring the band structures of TMDCs to achieve desirable characteristics for various device applications. In addition, the obtained device physics knowledge associated with MoS_2 and WSe_2-based multi-bit charge memory states is anticipated to greatly leverage the unique electronic and structural properties of layered semiconductors for scalable data storage and emerging analog computing applications.

Chapter 1 Introduction

1.1 New Opportunities of Transition Metal Dichalcogenides (TMDCs)

Recent research has suggested that the dimensionality plays a critical role in determining the fundamental material properties, in addition to the composition and arrangement of atoms. One of the most striking highlight is the rapid research progress of graphene over the past few years. As the representative of atomically layered materials, graphene exhibits extraordinary condensed-matter phenomena that are absent in bulk graphite [1-3]. While being fundamentally and technologically interesting due to a variety of excellent electrical and mechanical properties, graphene is chemically inert and without a sizable bandgap, which in turn limit its further device application in semiconductor engineering. Therefore, during the continuous academic exploration of other atomically layered materials, transition metal dichalcogenides (TMDCs) have emerged as a promising material candidate for making advanced nanoelectronics due to its sizable bandgaps, excellent optoelectronic and mechanical properties, large abundance of relevant bulk materials, as well as good compatibility to planar nanofabrication processes [4-8].

As shown in Figure 1.1, the general TMDC chemical formula is MX_2, where M is a transition metal element from groups IV, V, and VI, and X is a chalcogen element such as S, Se, and Te [9-11]. Because of a broad range of applicable combinations between transition metal

and chalcogen elements, the bulk TMDC materials provide versatile electrical properties ranging from insulators such as HfS_2, semiconductors such as MoS_2 and WS_2, semimetals such as WTe_2 and $TiSe_2$, to metals such as NbS_2 and VSe_2. Moreover, a few bulk TMDCs (*i.e.,* $NbSe_2$ and TaS_2) exhibit low-temperature phenomena including superconductivity, charge density wave (a periodic distortion of the crystal lattice) and Mott transition (metal to non-metal transition) [12-14].

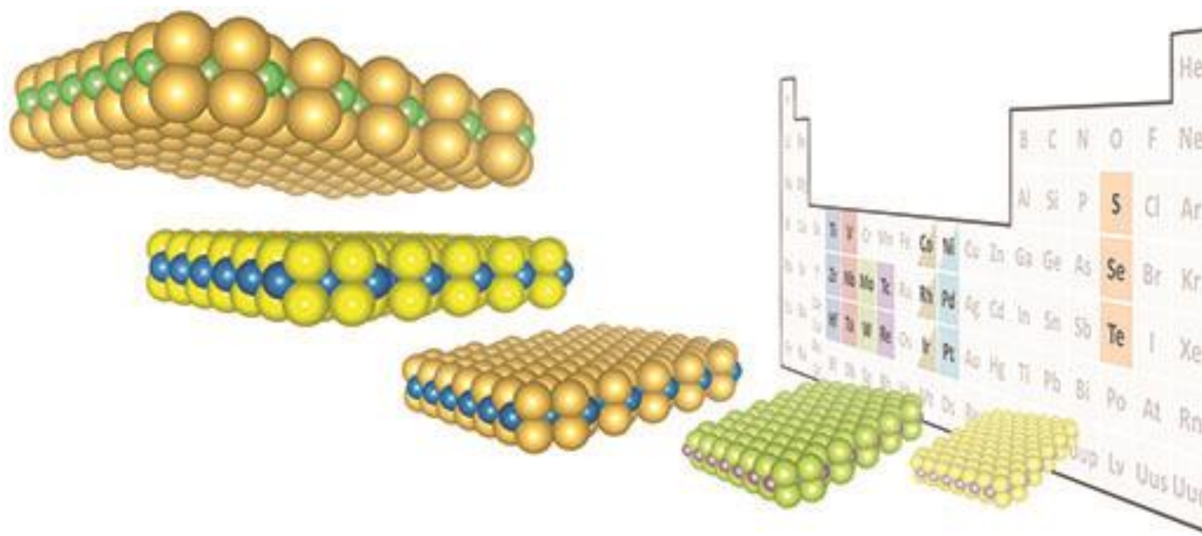


Figure 1.1 Structure of monolayer transition metal dichalcogenides (TMDCs). The transition metals and the three chalcogen elements that predominantly crystallize in those layered structure are highlighted in the periodic table. Partial highlights for Co, Rh, Ir and Ni indicate that only some of the dichalcogenides form layered structures. For example, NiS_2 is found to have apyrite structure but NiTe is a layered compound. Courtesy of reference [7]

In a single TMDC layer, a quintuple layer structure is formed by covalently bonding the metal and chalcogen atoms together. Then through the weak van der Waals force, multiple quintuple layers are stacked together in a multilayer TMDC flake [9, 15, 16]. Due to the relatively weak interlayer interaction, it is possible to obtain single-layer or few-layer TMDC through a

mechanical exfoliation process of TMDC bulk ingot [17-19]. Here, the exfoliation of bulk TMDC into mono- or few-layers largely preserves the material properties, and also leads to additional favorable characteristics due to confinement effects [20-22]. These properties thus offer opportunities for both fundamental and technological research in a variety of fields, going beyond graphene and opening up new paths for inorganic two-dimensional (2D) atomically layered semiconductor materials. A series of new prototype devices based on TMDC materials have been successfully demonstrated, including high-performance thin-film transistors (TFTs) [4, 23-25], highly sensitive chemical/biological sensors [26-28], phototransistors [29], multibit non-volatile transistor memories [30], and photovoltaic (PV) devices with high quantum efficiencies [31, 32], *etc.*

One of the most widely studied TMDC material is MoS_2, and its 3D atomic structure is illustrated in Figure 1.2. It has become a popular test-bed material for investigating TMDCs as it shares similar mechanical and electrical properties with other layered semiconductors, which makes the fabrication processes developed based on MoS_2 generally applicable to all other TMDCs. In the single-layer form, MoS_2 has a direct bandgap of ~1.8eV, while in the bulk form, it has an indirect bandgap of ~1.2eV [4]. Thus, MoS_2 flakes can serve as a valuable complement to zero-bandgap graphene for semiconductor-related device applications in both monolayer and multilayer structure. Moreover, attributed to the strong in-plane covalent bonds in two-dimensional layers, MoS_2 exhibits excellent mechanical properties. For example, the breaking strength (15 N m^{-1}), the in-plane stiffness (180 N m^{-1}), and the Young's modulus of MoS_2 layers (270 GPa) are comparable to those of steel respectively [33]. These properties make MoS_2 a promising material candidate for novel flexible wearable electronic and photonic application. In addition,

MoS_2 has a specific surface area of as large as 412 m^2 g^{-1} due to its large lateral sizes and atomically thin thicknesses [34], comparable to the chemically exfoliated graphene sheets (2150 m^2 g^{-1}) [35]. Such large specific areas could be exploited for a variety of surface-area-sensitive device applications, including solar cells [36], photocatalysis [37], electrocatalysis [38] and supercapacitors and other energy storage media [39]. Furthermore, such high specific surface areas could enable MoS_2 to serve as cost-efficient building blocks for synthesizing new functional composites [40-42]. With all these superior merits, a broad range of device applications based on MoS_2 has been demonstrated as far, such as thin-film transistors (TFTs) that are immune to short-channel effects [43], phototransistors [29], highly sensitive chemical sensors [44], and emerging valleytronic devices based on the unique optical response in MoS_2 [45].

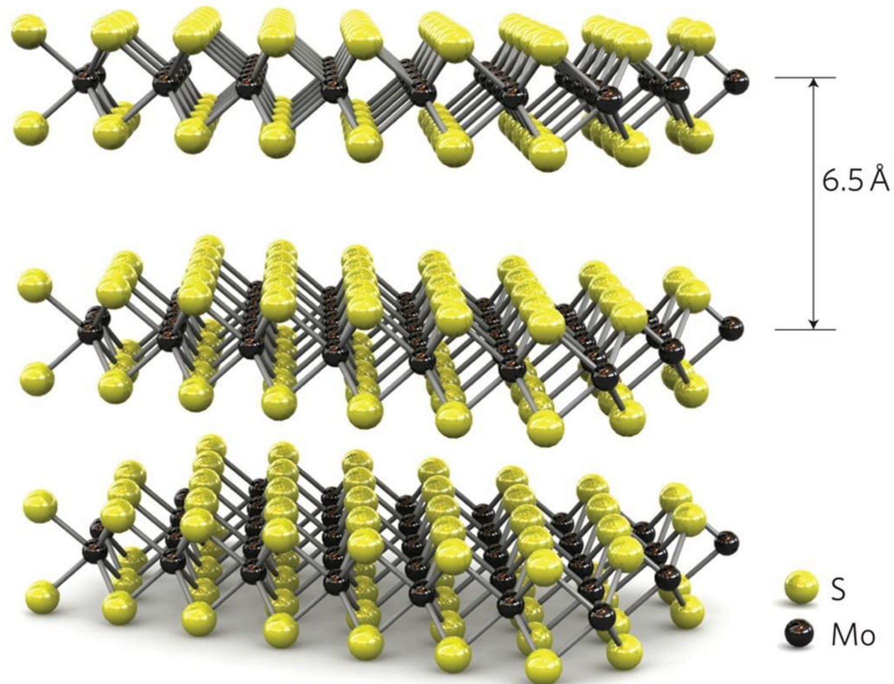


Figure 1.2 3D Model of MoS_2 Structure. Single layers with 6.5 Å thick can be exfoliated by using micromechanical cleavage. Courtesy of reference [4]

1.2 Need of New Nanofabrication and Doping Technologies for Electronic Device Manufacturing Based on Few-Layer Transition Metal Dichalcogenides

Due to the relatively weak interlayer interaction (*i.e.,* van der Waals force), the current most popular method to obtain single-layer or few-layer TMDC is mechanical exfoliation using scotch tape, as shown in Figure 1.3 [17-19]. It is an easy, simple and cost-efficient approach for fundamental research, which largely preserves the properties of atomically layered materials. This method also leads to additional favorable characteristics due to confinement effects [20-22]. Especially because of the attractive properties of monolayer TMDC structure including atomic scale thicknesses, direct bandgaps and strong valley-selective circular dichroism, a great deal of research effort has been directed to explore the chemical synthesis of monolayer TMDC over large areas [46-48] to enable device application with ultimate scaling of vertical dimension [43], such as light-emitting diodes [5], strong valley-selective circular dichroism, low-energy-dissipation valleytronic devices [45, 49]. Kang's group has demonstrated the MOCVD growth of single-layer MoS_2 flakes over large area, as shown in Figure 1.4 [50].

Although many research efforts have been focusing on TMDC monolayers, multilayer/few-layer structures are indeed desirable by many practical scale-up applications, because of the excellent transport properties (*e.g.*, relatively high mobility) and sizable electronic/photonic state densities for driving upscalable electrical/optical signals [51, 52]. For example, the multilayer TMDC structure provides higher photon absorption for optoelectronics application [32, 53, 54] and larger driving current for power electronic devices [51]. However, in spite of the breakthroughs and progresses in TMDC-based prototype device demonstration, the research and industry societies lack upscalable manufacturing techniques capable of producing orderly-arranged, high-quality,

highly-uniform TMDC device structures over wafer-scale areas. Especially, the community needs top-down lithography-fashion techniques capable of producing pre-structured TMDC nano/microstructures with deterministic and uniform feature dimensions and physical properties.

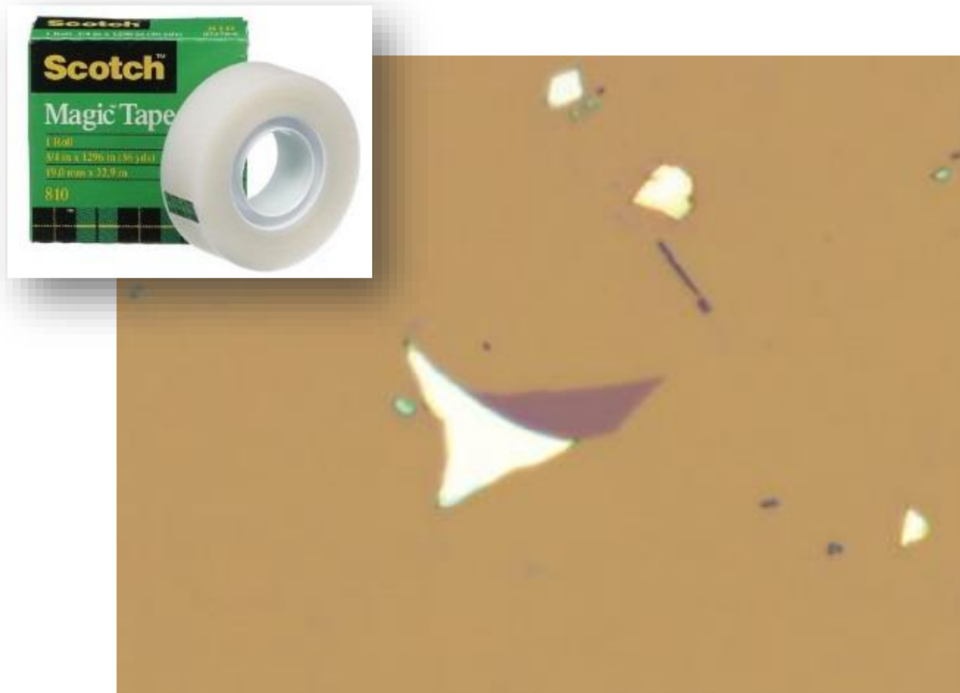


Figure 1.3 Optical image of a single layer of MoS_2 (thickness, 6.5 Å) deposited on top of a silicon substrate with a 270-nm-thick SiO_2 layer. Courtesy of reference [4]

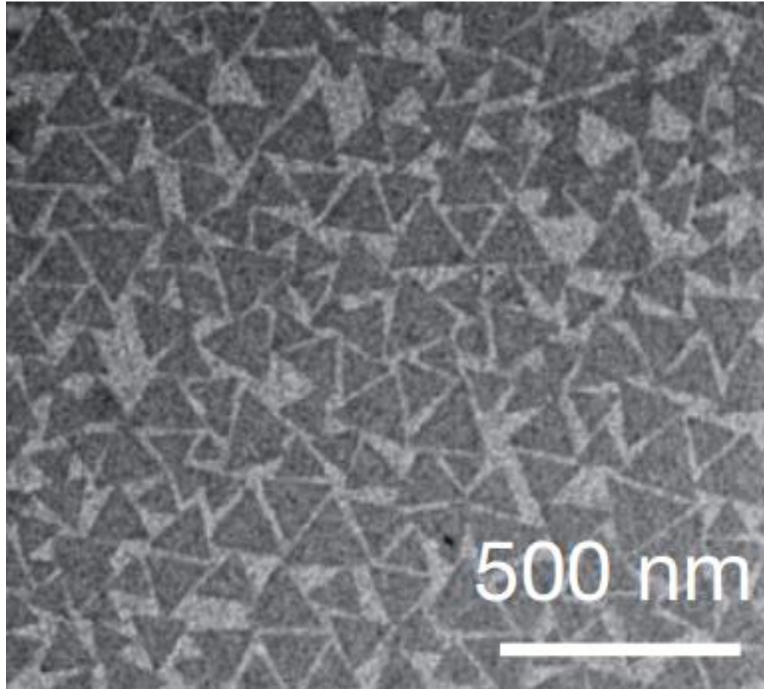


Figure 1.4 SEM images of MOCVD-grown monolayer MoS_2. Courtesy of reference [50]

On the other side, with the recent development of TMDC-based semiconductor applications such as thin-film transistors [55, 56], highly sensitive sensor [28, 57] and integrated logic circuit [58], a great deal of research efforts has been invested to create upscalable doping techniques for further realization of TMDC-based stable *p-n* junctions, complementary electronic circuits and novel optoelectronic devices [59, 60].

The conventional doping approaches in semiconductor industry such as thermal diffusion and ion implantation can't be directly applied to 2D materials, as they create too much damage to the atomically thin TMDC flakes due to the high power density. Therefore, many research groups tried to establish new stable doping methods specifically designed for multilayer TMDC materials. For example, Fang's group used potassium dispenser to obtain degenerate *n*-doping effect in MoS_2, which can improve the contact resistances between TMDCs and metals, as shown in Figure 1.5

[59]. Zhang's group cooled down the MoS_2 transistor to very low temperature (*i.e.*, ~ 180 K) and then used ionic liquid gate to form and control the *p-n* junction in device, as shown in Figure 1.6 [60]. Ozone treatment [61] has also been tested to create a moderate doping in graphene, while its doping effect has a limited life time due to the desorption of physisorbed ozone that is weakly attached to graphene surface. As a summary, for the nanomanufacturing process at high volume, we need to explore innovative doping approaches for creating stable *p-n* junctions and rectifying diode structures in MoS_2 and other TMDC materials for long-term applications at ambient conditions.

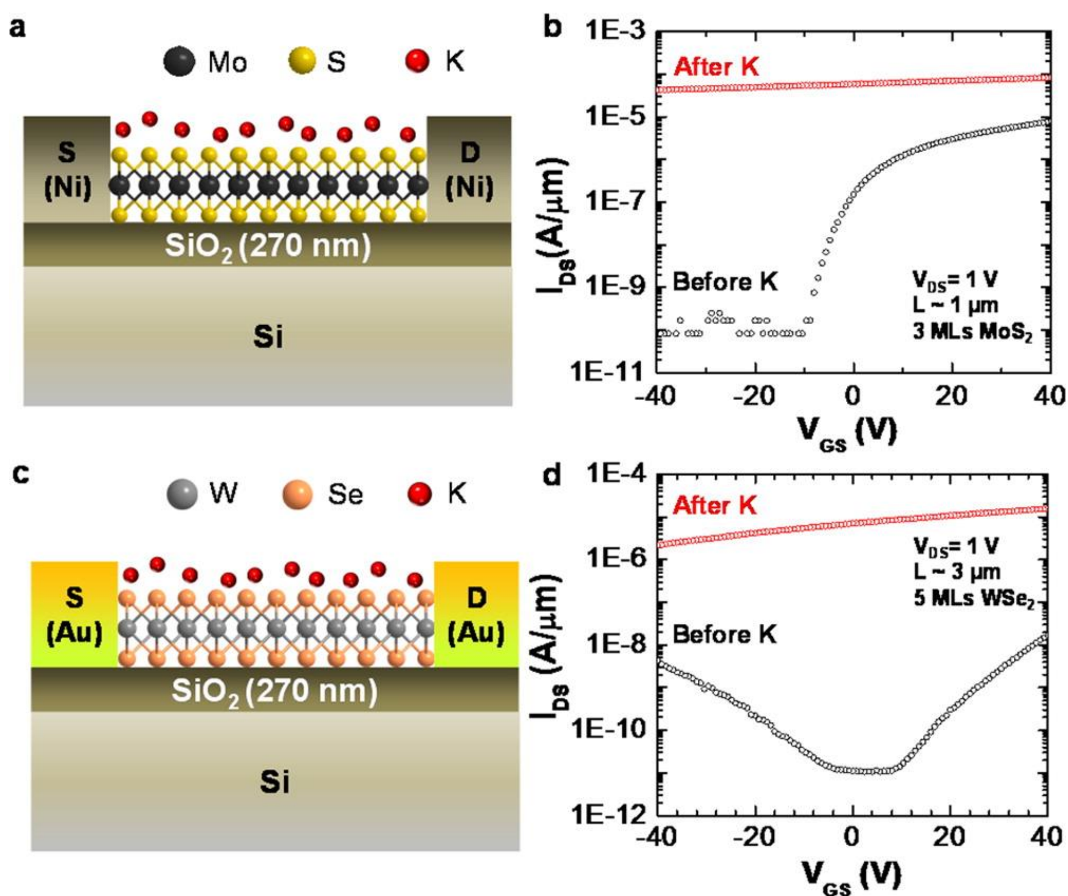


Figure 1.5 "Blanked" (*i.e.,* unpatterned) *n*-doping of few-layer MoS_2 and WSe_2 by K. (a, c) The schematic of K doping of the entire channel for MoS_2 and WSe_2 devices, respectively, with (b, d) showing the corresponding transfer

characteristics before (black symbols) and after (red symbols) doping. Courtesy of reference [59]

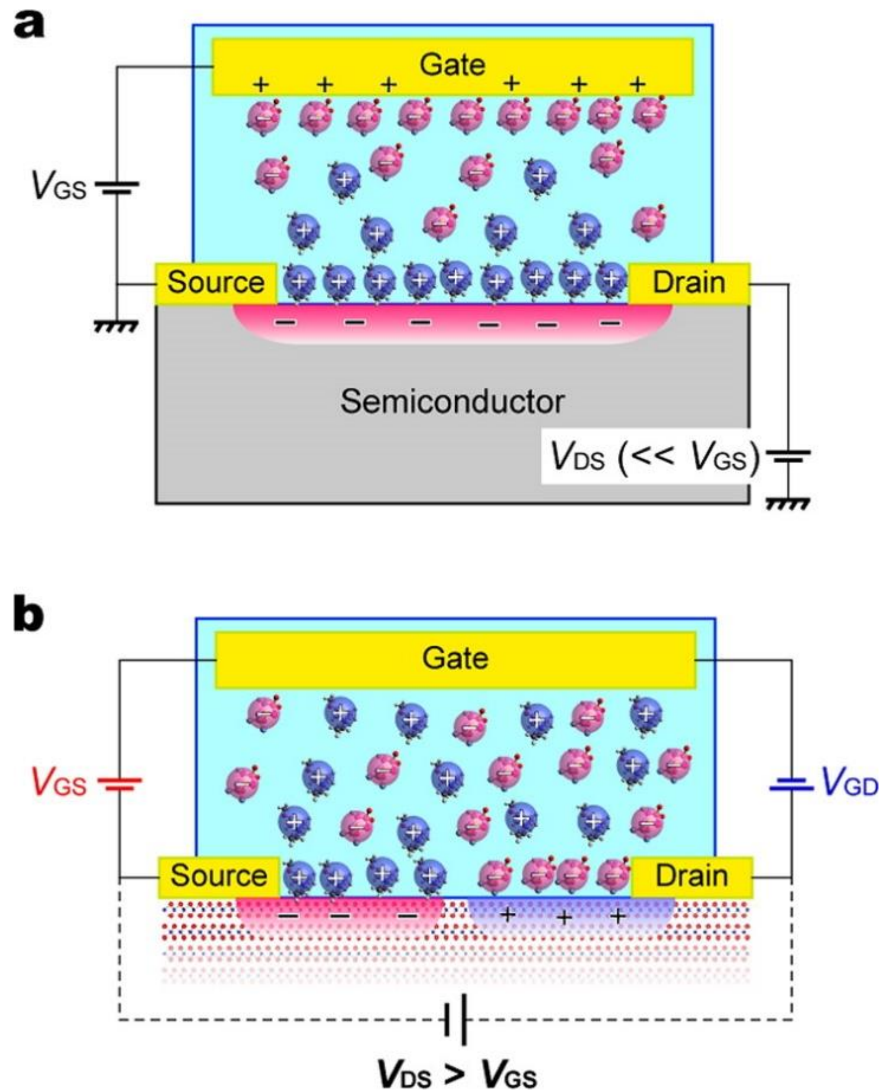


Figure 1.6 Schematics of unipolar and ambipolar carrier accumulation in electric double-layer transistors (EDLT). (a) A unipolar carrier accumulation mode. When V_{DS} is much smaller than V_{GS}, the transistor channel is formed by a single type of carrier. (b) An ambipolar carrier accumulation mode and formation of a *p-n* junction on the channel surface. When V_{DS}-V_{GS} is larger than a certain threshold, the effective gate voltage measured from the drain electrode becomes sufficiently negative to create hole accumulation. The induced holes near the drain electrode and the remaining electrons around the source electrode form a *p-n* junction on the channel of the EDLT. Courtesy of reference [60]

1.3 Attractive Charge-Trapping Mechanism and Memory Storage Properties of Transition Metal Dichalcogenides

The charge-trapping phenomena has been observed in the transfer characteristics of various electronic devices based on TMDCs (*e.g.,* MoS_2, WSe_2) [29, 62], and these phenomena could be attributed to a few possible mechanism including charge traps at moisture molecules, TMDC/SiO_2 interfaces or fabrication-induced defects or other structures in TMDC layers [63]. To construct reliable low-cost, high-performance nanoelectronic devices such as field-effect transistors (FETs) based on emerging 2D layered semiconductor materials, we need to understand the charge-trapping phenomena in such devices, as these trapped charges significantly affect the reliability, durability, and operation speed of FETs as well as other FET-related devices [64], such as biosensors [27, 28, 65, 66], flash memories [67-69], and photo-transistors [29]. Moreover, these charge-trapping mechanisms in atomically layered semiconductors hold the potential to be exploited to further leverage the unique electronic and structural properties of such TMDCs for providing new cost-efficient storage solution with multibit data storage and analog computing capability.

As the solid state drive (SSD) technologies such as flash memory have held higher and higher market share, the main challenge for scale-up SSD applications remains to be the cost, as the current price for solid state drive is still about 7-8 times more expensive per unit of storage than traditional hard disk drive. Therefore, the industry has been actively looking for cost-efficient SSD solution including innovative memory architectures as well as fabrication technology. One of such efforts is to create multibit memory cell, which can significantly improve the data storage density and reduce fabrication cost per unit of storage [70-75]. For example, Guo's group built multibit memory transistors based on organic semiconductors with ambipolar transport properties, as shown

in Figure 1.7 [76]. Sohn's group demonstrated multibit memory transistors based on special nanostructure materials (*i.e.,* nanoribbon integrated with nanoparticles) in combination of floating gate structure, as shown in Figure 1.8 [73]. However, the fabrication processes of all these memory cell structures require precise deposition and patterning of multiple semiconductor layers to create several floating gates and blocking/tunneling layers [70, 71, 77]. As a result, the complicated fabrication process inevitably increase the overall manufacturing cost.

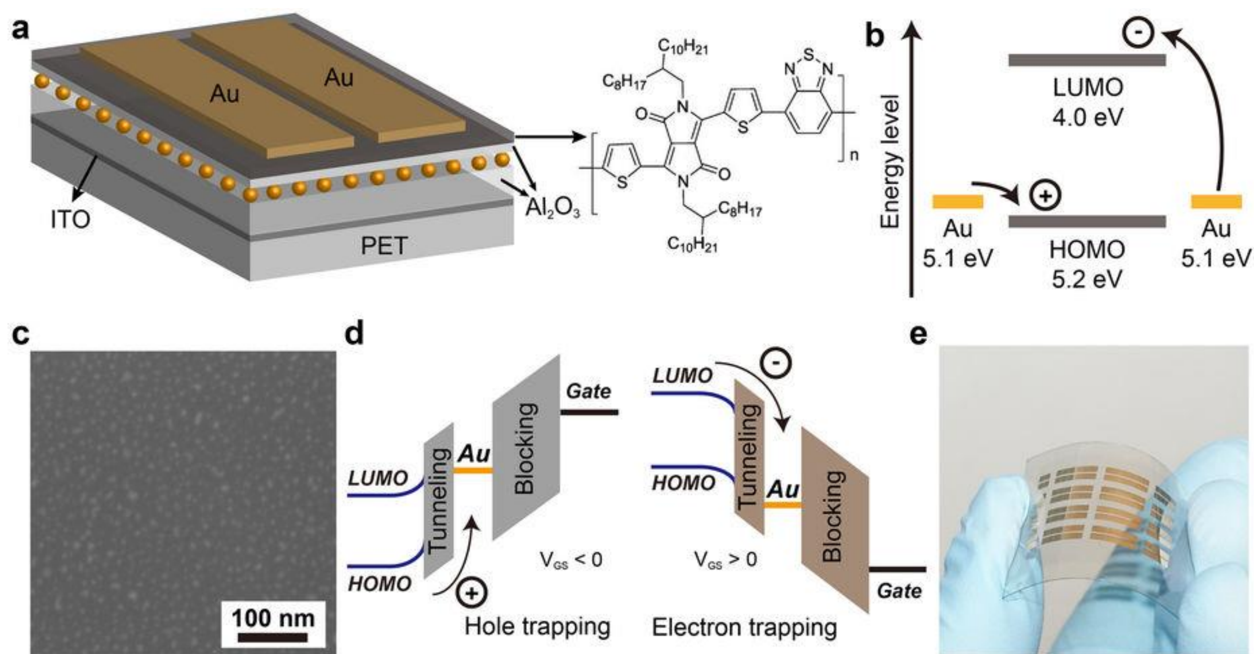


Figure 1.7 (a) Three-dimensional schematic diagram of the ambipolar memory device and the chemical structure of PDPP-TBT. (b) Band diagram of PDPP-TBT in contact with gold electrodes. (c) SEM image of Au nanoparticle monolayer. (d) Energy band diagrams of the memory transistor at hole trapping mode and electron trapping mode. (e) Optical image of the flexible memory device on PET substrate. Courtesy of reference [76]

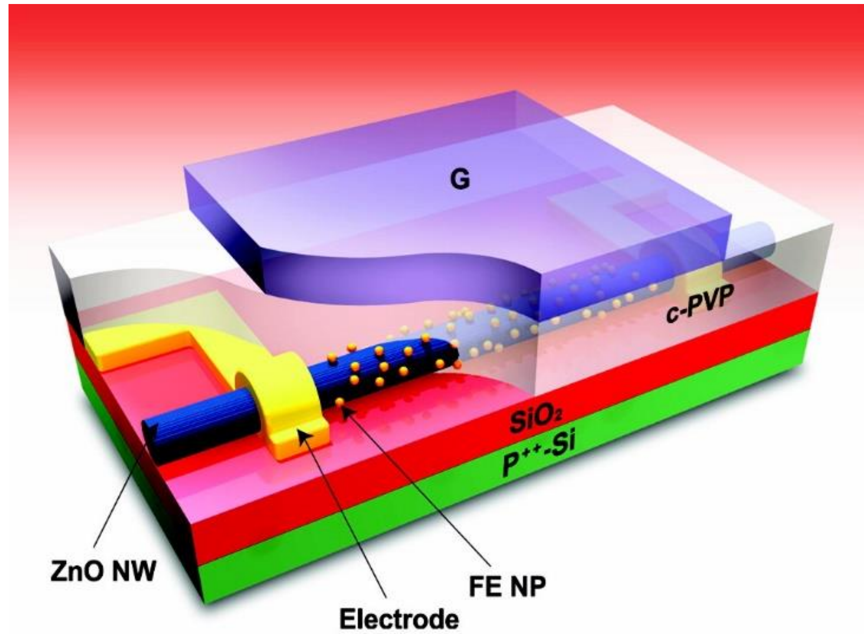


Figure 1.8 A schematic view of a top-gate FET based nonvolatile memory device. For a top-gate ZnO NW FET where a ZnO NW is incorporated with FE NPs, cross-linked poly(4-vinylphenol) (c-PVP) was used as a gate dielectric. Courtesy of reference [73]

In the recent research, the two-dimensional (2D) layered transition metal dichalcogenides (*e.g.*, MoS_2, WSe_2) were envisioned to provide a promising non-volatile SSD solution to address this challenge [67-69, 78, 79]. These works motivate and inspire additional research efforts to exploit unique properties of emerging TMDCs for making new transistor-based memory devices with a unique combination of excellent retention and endurance property, meanwhile with simple structure and low fabrication cost.

1.4 Summary of Dissertation

In summary, I have finished a series of nanofabrication and device-oriented projects toward addressing the scientific and technical challenges discussed in Section 1.2 and 1.3. The whole dissertation is divided into three main parts: (1) nanoimprint-assisted shear exfoliation technology

for generating few-layer TMDC device structure arrays over large areas (Chapter 2); (2) plasma-assisted doping technology for fabricating TMDC-based rectifying diodes (Chapter 3); (3) abnormal charge-trapping mechanisms observed in TMDCs, such as MoS_2 and WSe_2, as well as multi-bit memory devices based on such mechanisms (Chapter 4 and 5).

In Chapter 2, I present a nanoimprint-based approach to produce ordered, pristine multilayer TMDC device structures with a high uniformity of feature dimension sizes and transport properties. In this approach, termed as nanoimprint-assisted shear exfoliation (NASE), a prepatterned bulk TMDC stamp is pressed into a polymeric fixing layer and the imprinted TMDC features are exfoliated along a shear direction. This shear cleaving scheme can significantly enhance the exfoliation efficiency and thickness uniformity of exfoliated flakes in comparison with previously reported mechanical exfoliation processes. Furthermore, I have preliminarily demonstrated that multiple NASE-produced transistors and biosensors exhibit excellent device-to-device performance consistency. For example, the relative standard deviations of the electrical parameters (*e.g.,* field-effect mobility, On/Off currents, subthreshold swing, and threshold voltage) in NASE-produced transistors range from 21 to 23%. Finally, a molecular dynamics modeling analysis of the scaling behavior for NASE process is presented.

In Chapter 3, I present a method for making stable MoS_2-based rectifying diodes using the selected-area plasma treatment to few-layer MoS_2 flakes. The transport characterization and X-ray photoelectron spectroscopic analysis of MoS_2 transistors blank-treated by using different plasma species confirm that the rectifying characteristics of MoS_2 diodes are attributed to plasma-induced *p*-doping, which creates *p*-*n* junctions in intrinsic *n*-type MoS_2 layers. Such plasma-doped diodes exhibit high forward/reverse current ratios (*e.g.*, ~ 10^4 within a range of V = ±1 to ±2V for SF_6

plasma-treated diodes) and a superior long-term stability at room temperature. This plasma doping technology is anticipated to play an important role in the development of various MoS_2-based nanoelectronic devices for practical electronic applications. In addition, the presented plasma-assisted doping process could be generally used for functionalizing other two-dimensional materials.

In Chapter 4, I present a study on the abnormal charge-trapping and memory characteristics of few-layer WSe_2 transistors. This work shows that multiple charge-trapping states with large extrema spacing, long retention time, and quasi-analog tunability can be excited in the transistors made from mechanically-exfoliated few-layer WSe_2 flakes, whereas they cannot be generated in widely studied few-layer MoS_2 transistors. Such unique charge-trapping characteristics of WSe_2 transistors are attributed to the exfoliation-induced interlayer deformation on the cleaved surfaces of few-layer WSe_2 flakes, which can spontaneously form ambipolar charge-trapping sites. The additional results from surface characterization, charge-retention characterization at different temperatures, and density functional theory computation strongly support this explanation. Furthermore, this work has also demonstrated that the charge-trapping states excited in multiple transistors could be calibrated into consistent multi-bit data storage levels for making working memories.

In the project presented in Chapter 5, the plasma-treated MoS_2 transistors are systematically investigated to create new low-cost, non-volatile, highly durable memories with a multi-bit data storage capability. I have experimentally demonstrated binary and 2bit/cell (4-level) data states suitable for year-scale bit information storage applications, as well as 3bit/cell (8-level) states for day-scale storage. This multi-bit memory capability is attributed to plasma-induced doping of the

top MoS_2 layers that can spontaneously form a charge trapping structure with multi-level data states. My Kelvin force microscopy results strongly support this explanation. In addition, the programming speed of such memories can be improved by using nanoscale-area plasma treatment. My research provides scientific insights to leverage the unique structural property of TMDCs for low-cost, scalable memory and emerging analog-computing applications.

Chapter 2

Nanoimprint-Assisted Shear Exfoliation (NASE) for Producing Multilayer Transition Metal Dichalcogenide Device Arrays

2.1 Introduction

Because of the excellent electronic, photonic and mechanical properties, large natural abundance on the earth, as well as good compatibility to planar nanofabrication processes, the atomically layered transition metal dichalcogenides (TMDCs) (*e.g.*, WSe_2 and MoS_2) have recently emerged as attractive material candidates to potentially enable a variety of novel functional devices with high cost efficiency [4-8]. A series of new prototype devices based on TMDC layers have been demonstrated in the research laboratories, such as high-performance thin-film transistors (TFTs) [4, 23-25], highly sensitive chemical/biological sensors [26-28], phototransistors [29], multibit non-volatile transistor memories [30], and photovoltaic (PV) devices with high quantum efficiencies [31, 32], *etc.* To leverage the superior electronic/photonic characteristics of such devices for practical scale-up applications, the research community currently needs new nanomanufacturing methods capable of producing TMDC device arrays with deterministic and uniform properties. A great deal of recent research effort focuses on the attractive properties

associated with monolayer TMDC structures, such as direct bandgaps, which are suitable for light-emitting applications [5], strong valley-selective circular dichroism, which can potentially enable future low-energy-dissipation valleytronic devices [45, 49], as well as atomic scale thicknesses that represent the ultimate scaling of material dimension in the vertical direction and can potentially enable miniaturization of electronic devices beyond Moore's Law [43]. Therefore, there have been many material-synthesis-oriented works seeking to product TMDC monolayers over large areas [46, 48, 80]. In spite of such intensive effort related to monolayers, many important nanoelectronic/optoelectronic applications, such as transistor-based memories/sensors [27, 28, 30], photovoltaics [32, 53, 54], and power switching TFTs [51], indeed demand high-quality multilayer TMDC structures, because multilayer structures can provide excellent transport properties (*e.g.*, relatively high mobility) and sizable densities/amounts of electronic/photonic states, enabling device applications that need to drive large current/voltage signals or absorb a large amount of photons [51, 52]. However, currently there are very few research efforts dedicated to fabricate high-quality multilayer TMDC structures with a high uniformity of thickness and electronic/photonic properties over large areas. Especially, the research society needs the upscalable production technology of multilayer TMDC device arrays or large-scale circuits.

In this chapter, we presented a top-down nanofabrication approach capable of producing pristine multilayer MoS_2 fake arrays with a high uniformity of flake thicknesses (*i.e.*, relative thickness error ~ 12%) over cm^2-scale areas. Using the as-produced MoS_2 flakes, we also demonstrated multiple working transistors and electronic biosensors which exhibited very consistent performance. Specifically, in this presented nanofabrication process, termed as nanoimprint-assisted shear exfoliation (NASE), multilayer MoS_2 structures pre-patterned on a bulk

MoS_2 stamp were imprinted into a polymeric fixing layer and subsequently exfoliated along a shear direction using a motorized roller tool. As compared to previously reported exfoliation methods for generating layered materials [55, 81], NASE can result in significantly improved transfer efficiency of pre-structured MoS_2 features as well as uniformity of resultant flake thicknesses. Our transistor-based biosensors made from NASE-produced MoS_2 flakes exhibited a high device-to-device consistency in the sensor responses to specific biomarkers. We have preliminarily demonstrated quantification of a standard curve for tumor necrosis factor-alpha (TNF-α) detection by using multiple such biosensors. And our molecular dynamics (MD) modeling analysis further indicated that the NASE process can potentially create TMDC device structures with nanoscale lateral dimensions.

2.2 Methods and Materials

2.2.1 Fabrication of MoS_2 Stamps

The bulk MoS_2 ingots for making NASE stamps were purchased from SPI, Inc. The ingot size is ~ 1 cm^2. The prepatterning of bulk MoS_2 stamps was performed using a method previously reported by us [55]. In particular, the protrusive mesa structures on MoS_2 stamps were formed by using SF_6 reactive ion etching (RIE) (RIE parameters: SF_6 flow rate 20 sccm, chamber pressure 20 mTorr, RF power 200 W). The etching rate of this RIE receipt was measured to be ~100 nm/min in our RIE tool (Plasma-Therm790).

2.2.2 Thermal NIL of Pre-structured MoS_2 Structures into PS Fixing Layers

A 50nm polystyrene layer was coated on the SiO_2/Si substrates which are pre-cleaned by standard RCA cleaning process. The MoS_2 stamp was subsequently firmly pressed to the SiO_2/Si substrates by using a homemade pressing tool that can generate a gauge pressure as large as 3MPa. Then the T-NIL process was performed in a Shellab 1407 vacuum oven at 140°C for 10 min.

2.2.3 Setup and Operation of The Lab-Made Motorized Roller Tool for Generating Shear Exfoliation

Figure 2.4 (a) shows our lab-made motorized roller tool. The main roller (diameter: 60 mm; width: 150 nm) is responsible for generating the relative shear displacement between a stamp/substrate pair. It was made of Aluminum alloy and coated with a 3 mm thick urethane rubber layer to provide a conformal contact between the roller and the flat sample holder as well as enhance the friction between the roller and the stamp (or the substrate). The vertical stage can generate adjustable gauge pressure (or force) between the roller and the flat sample holder (or between the MoS_2 stamp and the imprinted substrate). In a typical NASE process, this vertical force is adjusted to be ~200 N. The roller is driven by a brushless motor (USM425-401W from Oriental Motor U.S.A. CORP.), which is coupled with an electric speed controller (USP425-1U from Oriental Motor U.S.A. CORP.) to provide continuous variation of rotation speed. The web speed measured at the roller surface can be controlled within a range of 0 to 30 mm/sec. In a typical NASE process, this speed is adjusted to be ~3 mm/sec, and the typical operation time for a shear exfoliation cycle is 5 sec.

2.2.4 Raman and AFM Characterizations

The Raman spectra of NASE-produced MoS_2 flakes were measured using a Renishaw inVia microscope equipped with a 633nm laser. The surface topography of MoS_2 flakes was characterized using a Veeco Dimension Icon Atomic Force Microscope.

2.2.5 Fabrication and Characterization of Back-Gated MoS_2 FETs and FETs-Based Biosensors

To make a working FET array, a SiO_2-coated p+-Si substrate bearing NASE-produced multilayer MoS_2 flakes was first etched by O_2 plasma, and the PS regions not covered by MoS_2 flakes were completely removed. There were residual PS layers under MoS_2 flakes, which were estimated to be thinner than 5 nm. Afterward, all MoS_2 flakes were thinned from 50 to 100 nm to~20 nm by using SF_6 plasma (power: 40 W; precursor flow rate: 10 sccm; pressure 10 mTorr; etching rate: ~ 20 nm/min). The effect of this plasma recipe on various FET parameters was studied through comparing the transfer characteristics of MoS_2 FETs measured before and after their MoS_2 channels were thinned by plasma. Figure 2.1 shows the transfer characteristics of a typical PS-free MoS_2 FET measured before (blue curve) and after (red curve) its NASE-produced MoS_2 channel was thinned from 75 nm to 33 nm by using SF_6 plasma (power: 40 W; precursor flow rate: 10 sccm; pressure: 10 mTorr; etching rate: ~20 nm/min). After this thinning process, the On/Off ratio was greatly enhanced from 7×10^3 to 4×10^6; the carrier mobility was slightly reduced from 55 cm^2/Vs to 48 cm^2/Vs; the subthreshold swing (SS) was not noticeably changed (~ 9 V/dec); and the threshold voltage (V_T) was slightly modified from -21 V to -16 V (*i.e.*, a slight plasma-induced *p*-doping effect. Note that the increase of plasma power can result in a more

prominent doping effect in MoS_2 layers). Therefore, our current plasma thinning recipe can prominently improve the On/Off ratio of a multilayer MoS_2 FET without significantly degrading other FET parameters. In addition, our FETs made from un-thinned NASE-produced MoS_2 flakes exhibit very similar performance as compared to the FETs made from the MoS_2 flakes that were exfoliated using the scotch tape method. This implies that the NASE-induced mechanical damage to the top surfaces of MoS_2 flakes, if any, does not result in a significantly degraded performance of the FETs made from these flakes.

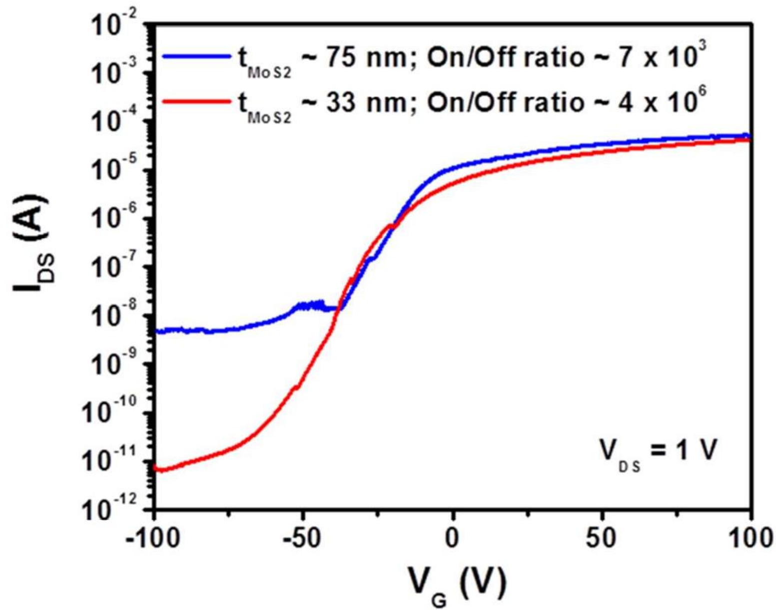


Figure 2.1 Transfer characteristics of a MoS_2 FET measured before (blue) and after (red) its MoS_2 channel was thinned from 75 nm to 33 nm.

After this thinning process, the drain (D) and source (S) contacts of the FET array were fabricated using photolithography followed with metal deposition (5 nm Ti and 50 nm Au) and lift-off in a solvent. The p^+-Si substrate was used as the common back gate, and the thermally grown

SiO_2 layer (300 nm thick) served as the gate dielectric (the effective gate dielectric for a FET also includes a residual PS layer). All FET characteristic curves were measured by using an HP-4145B semiconductor parameter analyzer at the room temperature, which was connected to a LakeShore probe station.

For converting a MoS_2 FET into a biosensor to detect TNF-R molecules, we first need to passivate its D/S contact electrodes to eliminate the effect of antibody-antigen binding on the contact resistances between D/S contacts and the MoS_2 channel. In this work, we used patterned photoresist layers (~2 μm thick SU8) to fully cover and passivate D/S contacts. Figure 2.2 (a) shows an optical micrograph of a representative MoS_2 FET biosensor, in which the D/S contacts are passivated by photoresist layers. After the electrode passivation, the multilayer MoS_2 channel needs to be functionalized with antihuman TNF-R antibody receptors. Figure 2.2 (b) illustrates the antibody functionalization protocol used in this work, which includes (1) incubating MoS_2 FETs into a 5% (3-Aminopropyl) triethoxysilane (APTES) solution (from Sigma-Aldrich Co. LLC.) for 1 h; (2) incubating the MoS_2 channels silanized with APTES in a 5% solution of glutaraldehyde (GA, from Sigma-Aldrich Co. LLC.) in phosphate buffered saline (PBS) for 2 h; (3) incubating FETs in an antihuman TNF-R antibody solution for 1 h; and (4) TNF-R detection. Specifically, for Step (4) TNF-R detection, we perform the following steps: (a) incubate an as-functionalized FET sensor in a target TNF-R solution (solvent: 1×PBS) for 20—30 min to ensure that the (TNF-R)-antibody association/dissociation reaction reach to the equilibrium state; (b) rinse away unreacted TNF-R molecules with DI water; (c) blow dry the sensor and measure its transfer characteristics using a semiconductor analyzer.

It should be noted that although our as-fabricated MoS_2 FETs can be characterized in a relatively dense array (device spacing could be as small as 10-15 μm), as shown in Figure 2.7 (b), our current FET biosensors have to be characterized in a much more dispersed array configuration (device-to-device spacing: 3-5 mm), because extra space is needed by each sensor for hosting liquid droplets of target solutions as well as passivated large electrodes. However, by integrating additional microfluidic structures for confining analyte solutions to individual sensors, this issue is anticipated to be addressed in the future.

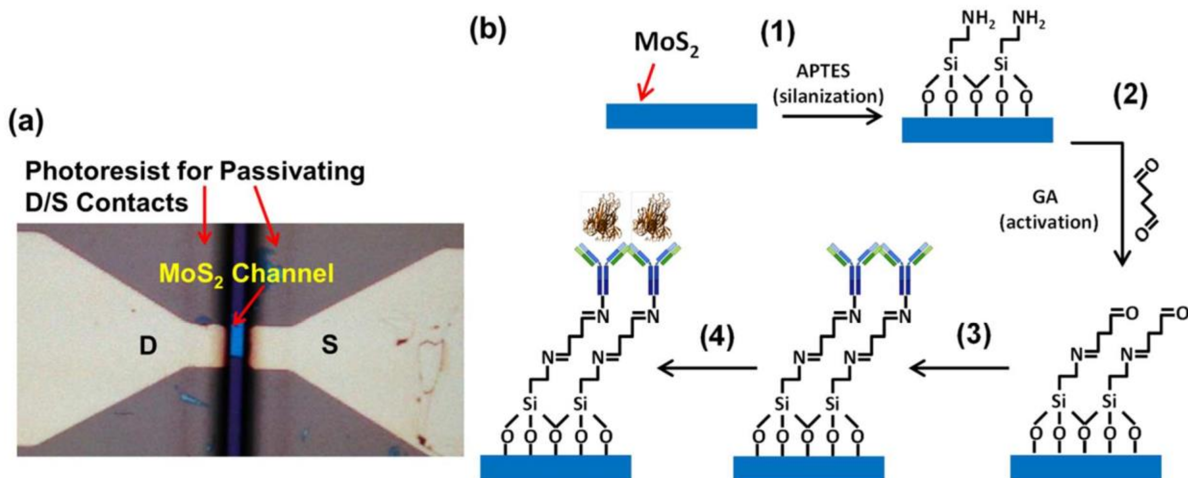


Figure 2.2 Passivation and functionalization of MoS_2 biosensors: (a) optical micrograph of a representative MoS_2 FET biosensor, in which the drain (D)/source (S) contacts are passivated by photoresist layers (SU8); (b) chemical protocol for functionalizing MoS_2 FET sensors with anti-human TNF-α antibody receptors for detecting TNF-α molecules: (1) Immerse the FET into a 5% APTES solution and incubate it for 1 hour. (2) The MoS_2 surface silanized with APTES reacts with a 5% solution of glutaraldehyde (GA) in phosphate buffered saline (PBS) for 2 hours, followed by rinsing with PBS buffer. (3) The MoS_2 surface is then incubated with an anti-human TNF-α antibody solution for 1 hour. (4) The as-functionalized sensor is incubated with TNF-α solutions with incremental concentrations (20-30 min for each concentration) for studying the sensor responses at the equilibrium state and the affinity of the antibody-(TNF-α) pair.

2.2.6 Molecular Dynamics Simulation

The molecular dynamic (MD) simulations for our NASE process were performed using the large-scale atomic/molecular massively parallel simulator (LAMMPS) package which was developed at Sandia National Laboratories. In our simulations, each graphene layer was modeled using an adaptive interatomic reactive empirical bond order (AIREBO) potential function [82], while the carbon-carbon interaction between two graphene layers was modelled by a registry-dependent potential [83]. With this set-up, we obtained in-plane carbon-carbon distance of 1.401 Å, equilibrium interlayer spacing of 3.365 Å in AB stacking, cohesion energy of 45.2 meV per atom with respect to one graphene layer (*i.e.*, cleavage energy per atom), and interlayer shear modulus of 5.01 GPa (C_{44}) and intralayer shear modulus of 38.8 GPa (C_{33}). For the description of the intermolecular and intramolecular interactions in polystyrene (PS), we used the optimized potentials for liquid simulation (OPLS) force field [84]. A three-stage energy minimization and isobaric-isothermal simulation of the bulk PS system provided us with a density of 1005 kg/m^3. Afterwards, we placed few-layer graphene flakes at a distance of 2.5 Å above the bulk polystyrene and adopted the conjugate gradient method to perform the energy minimization of the system before initiating the MD integration, as shown in Figure 2.12 (a). A 12 Å cut-off radius was applied for Coulomb and van der Waals interactions. The electrostatic interactions were treated by using the particle-particle particle-mesh (PPPM) method with a precision of 10^{-4}. The dielectric constant was set to 1. Periodic boundaries were applied in x and y directions during the simulations. This is consistent with our NASE setup for generating periodic layered structures. A Verlet time-integration scheme was applied throughout the whole simulation. Following the initial setup shown in Figure 2.3 (a), the PS layer was subjected to a 10 ns isothermal ensemble at $T = 500$ K, using the

Nose-Hoover thermostat. This ensemble simulated the thermal nanoimprint step of a NASE process. After this step, the few-layer graphene mesas were fully imprinted into the PS layer, as shown in Figure 2.12 (b). After the thermal nanoimprint step, the well-equilibrated configuration was obtained by cooling down the system from T = 500 K to room temperature at 1 bar using the NPT simulation with the set temperature T lowered by 10 K every 10 ns (effective cooling rate 1 K/ns). In the following simulations of shear exfoliation of imprinted few-layer graphene structures, the top-most layers of all few-layer graphene mesas and 2 Å of the PS layer from the bottom were set as rigid. To fully mimic the experimental setup, the top-most mesa layer was pulled away along a shear direction (*i.e.*, x-axis direction) with speed of 2×10^{-4} Å/ps, which corresponds to the web speed of our 60-mm-diameter roller rotating at an angular speed of ~6 RPM.

2.3 Result and Discussion

2.3.1 Experimental Result of Nanoimprint-Assisted Shear Exfoliation (NASE)

Our fabrication method for producing multilayer TMDC flake arrays with uniform thicknesses is schematically illustrated in Figure 2.3. This new method is termed as nanoimprint-assisted shear exfoliation (NASE). In a NASE process, first a bulk TMDC ingot is pre-structured with protrusive multilayer mesa arrays by using photolithography followed with plasma etching (Figure 2.3 (a)). After this process, this ingot becomes a bulk TMDC stamp. More details about the TMDC stamp fabrication has been reported in our previous work [55]. Here, the protrusive mesa height can be well controlled through adjusting the plasma etching duration. This mesa height will determine the imprint depth (d_{NIL}) resulted by the stamp [85]. When the stamp is ready, a substrate (*e.g.*, glass, Si, or SiO_2) is spin-coated with a polymeric fixing layer (*e.g.,* thermoplastics or cross-

linkable polymers), and the TMDC stamp is subsequently pressed into the fixing layer on the substrate through a nanoimprint lithography (NIL) process (Figure 2.3 (b)). Afterwards, a lab-made motorized roller tool is used to displace the TMDC stamp along the substrate surface (*i.e.*, a shear direction). Due to such a shear displacement, the TMDC mesas already imprinted into the fixing layer can be exfoliated away from the bulk stamp (Figure 2.3 (c)). The thicknesses of exfoliated multilayer TMDC flakes are anticipated to be mainly determined by the imprint depth (d_{NIL}) (Figure 2.3 (d)). In comparison with previously reported exfoliation methods for generating layered materials, such as electrostatic exfoliation, plasma-assisted nanoimprint [55], and mechanical cutting/transfer-printing [81], the unique shear exfoliation mechanism involved in NASE can result in a significantly improved transfer-printing efficiency of pre-structured TMDC features as well as the higher uniformity of exfoliated TMDC feature thicknesses. In comparison with chemical synthesis approaches for generating multilayer TMDCs, NASE can produce TMDC structures with the larger average crystal domain size (10s-100s μm), the higher ordering of interlayer stacking configurations [86, 87], and therefore the better transport properties [32, 46-48]. Furthermore, NASE can be generalized for producing high-quality multilayer structures of other atomically layered materials, such as highly ordered pyrolytic graphite (HOPG) and emerging topological insulators (*e.g.*, Bi_2Se_3 and Bi_2Te_3).

Additional etching/ablation processes (*e.g.*, layer-by-layer plasma etching or laser ablation approaches) could be subsequently applied after NASE process, which can further adjust the thicknesses of NASE-produced TMDC flakes to meet the requirements of various device applications [88, 89], such as monolayers for light-emitting devices [5], 10-30 nm thick flakes for making high-mobility transistors [51, 52], and 50-200 nm flakes for photovoltaic devices [31, 32].

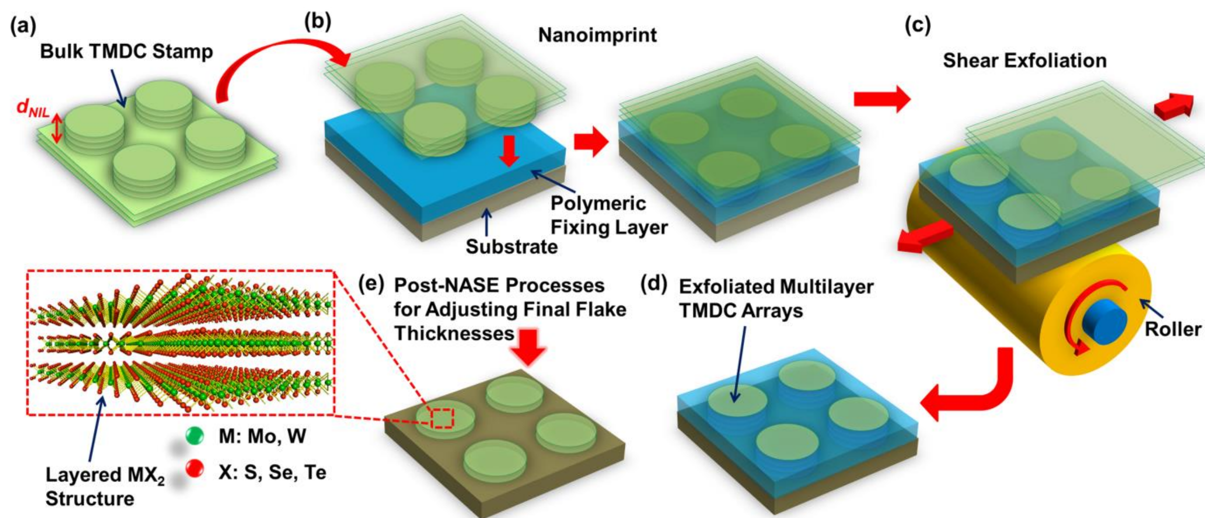


Figure 2.3 Illustration of nanoimprint-assisted shear exfoliation (NASE) for producing few-layer/multilayer TMDC device structure arrays: (a) fabrication of a bulk TMDC stamp bearing protrusive device features; (b) nanoimprint process for pressing the protrusive features on the bulk TMDC stamp into a polymeric fixing layer coated on a substrate; (c) exfoliation of imprinted TMDC features along a shear direction, which is actuated by a motorized roller tool; (d) multilayer TMDC flakes imprinted/exfoliated by NASE, which are expected to exhibit a high uniformity in thickness as well as electronic properties; (e) post-NASE processes for further adjusting the final thicknesses of exfoliated TMDC flakes to meet various device application requirements.

Figure 2.4 (a) shows a photograph of our lab-made motorized roller tool to perform the shear exfoliation of multilayer TMDC structures onto the substrate. This tool consists of an AC brushless motor with an electric speed controller, a flat sample holder for immobilizing either the stamp or the substrate, a motor-driven roller for generating the relative shear displacement between the stamp and the substrate, and a vertical stage for applying a gauge pressure to maintain the stamp flat during the shear exfoliation. In particular, the web speed of the roller surface can be adjusted in the range of 0-3 cm/s. The vertical stage bearing a set of coil springs can generate an

adjustable gauge pressure (0-0.5 MPa) to press the TMDC stamp firmly against the substrate, therefore effectively avoiding the formation of wrinkles in exfoliated TMDC features.

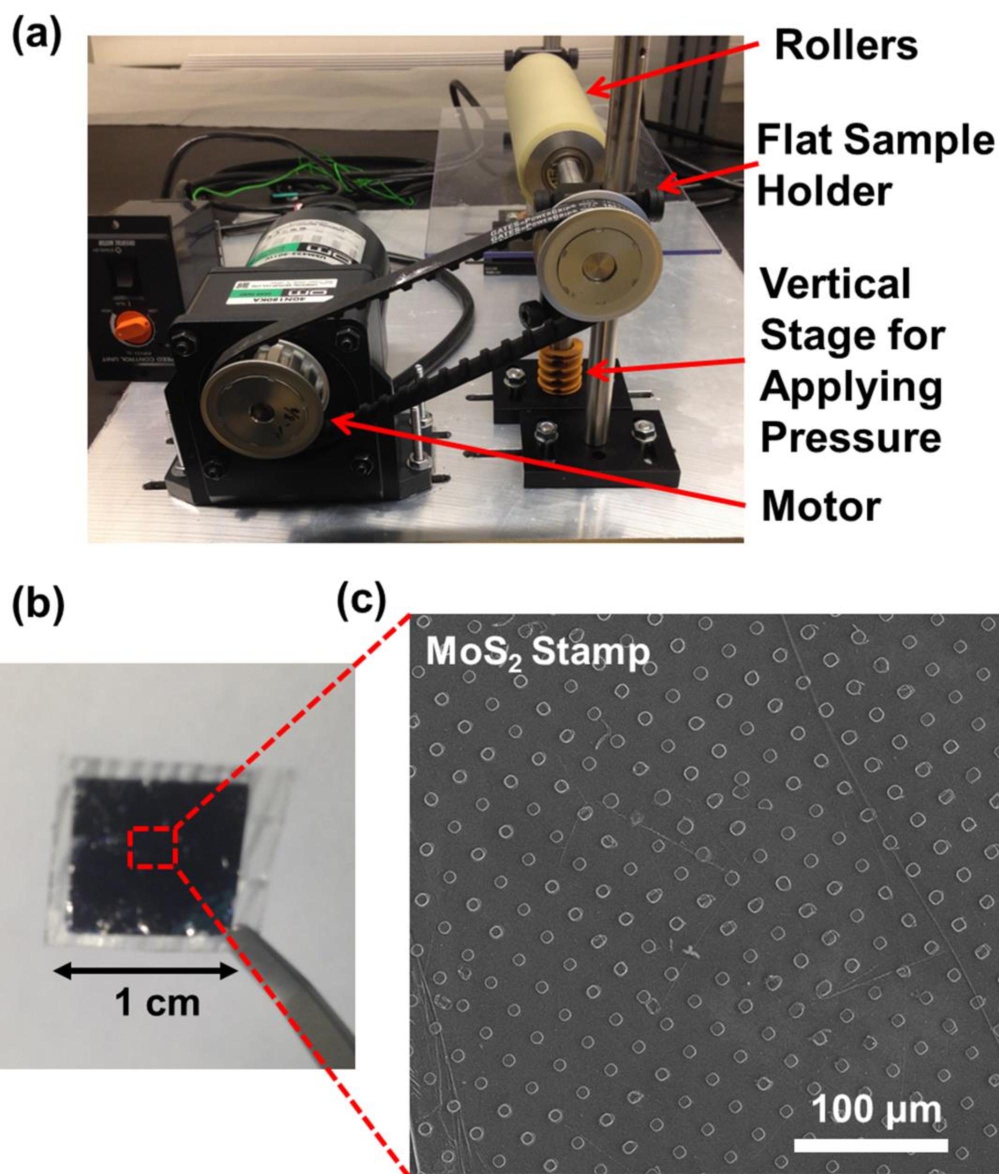


Figure 2.4 Photographs of (a) the motorized roller tool for performing NASE processes and (b) an exemplary 1 cm-size MoS_2 stamp. (c) shows the SEM image of this stamp, which bears 50 nm-high, 15 μm-size protrusive pillar arrays.

We chose MoS_2 as the test-bed material to investigate our NASE processes in this work, because (i) MoS_2 is the most widely studied TMDC material; (ii) MoS_2 and other TMDCs share very similar mechanical properties, which makes the nanofabrication processes developed in this work generally applicable to all other TMDCs. Figures 2.4 (b) and (c) display an optical micrograph (OM) and a scanning electron micrograph (SEM) of an exemplary MoS_2 stamp pre-structured with 50 nm high, 15 µm size pillar arrays, respectively. The size of the whole stamp is ~ 1 cm. More details about the roller tool, the fabrication of bulk MoS_2 stamps, and the NASE process are described in Section 2.2 Methods and Materials.

Figure 2.5 (a) shows NASE-produced MoS_2 flakes under optical microscope, which were exfoliated into a 55 nm thick polystyrene (PS) fixing layer coated on a SiO_2/Si substrate (SiO_2 thickness, 300 nm). The micrographs were captured from different locations over the whole NASE-processed area (~1 cm^2), as mapped in the inset photograph of the whole NASE sample. Raman spectroscopy was performed to identify the existence of exfoliated MoS_2 flakes in the imprinted PS layer. Our Raman results show that more than 80% of imprinted wells in the PS fixing layer have MoS_2 flakes. Figure 2.5 (b) shows a typical Raman spectrum of a NASE-produced MoS_2 flake, which exhibits two characteristic peaks, A_{1g} and E_{2g}, corresponding to the in-plane and out-of-plane vibration modes of MoS_2 layers, respectively [90]. For most NASE-produced MoS_2 flakes, their A_{1g}-E_{2g} peak spacing are larger than 19 cm^{-1}. This indicates that most NASE-produced flakes are multilayer MoS_2 structures [91]. Our OM and Raman characterizations show that NASE can produce orderly arranged multilayer MoS_2 device structures over cm-scale areas. Although most imprinted well pixels in PS fixing layers have high-quality MoS_2 flakes faithfully exfoliated from the bulk stamps, observable imperfection features still occur during a NASE process. Figure 2.5 (c)

displays the OM images of typical imperfection features occurring in NASE, which includes (i) imprinted PS wells without MoS_2 (*i.e.*, no exfoliation), (ii) imprinted wells with broken MoS_2 fragments (*i.e.*, incomplete exfoliation), (iii) MoS_2 dislocated away from the imprinted PS wells, and (iv) non-uniform thickness distribution within individual flakes. The occurring probabilities of these imperfection features may be relevant to mechanical properties of TMDC stamps and polymeric fixing layers, flatness/total size of TMDC stamps, geometric dimensions of pre-structured TMDC structures, and NASE processing parameters (*e.g.*, roller speed and vertical pressure), *etc*. Especially, we found that the aspect ratio (*i.e.*, the ratio between the height and lateral size of a feature) of protrusive mesas pre-structured on TMDC stamps greatly affects the quality of NASE-produced flakes. In particular, given a fixed lateral size of mesas of 15 μm, our current NASE system can easily exfoliate 40-200 nm high MoS_2 mesas without resulting in significant imperfections. However, when the initial mesa thickness is thinner than 40 nm, the occurring probability of broken, wrinkled, and dislocated mesa flakes is significantly increased. Therefore, as mentioned above, the better route for producing 0.7-40 nm thick, 15 μm size MoS_2 flake arrays (*i.e.*, monolayer to 60-layer structures) is to employ NASE for producing uniform flake arrays thicker than 40 nm, and subsequently perform a post-NASE etching process to thin the NASE-produced flakes. For example, Liu *et al*. has demonstrated layer-by-layer thinning of multilayer MoS_2 structures [88]. These thinning approaches in combination with NASE can produce uniform MoS_2 flake arrays with arbitrary thicknesses to meet the requirements of different device applications. To fully understand the role of other factors in generating imperfections during NASE processes and optimize the processing conditions to eliminate the imperfection features displayed in Figure 2.5 (c), in the future more nanomechanics-oriented works will be performed.

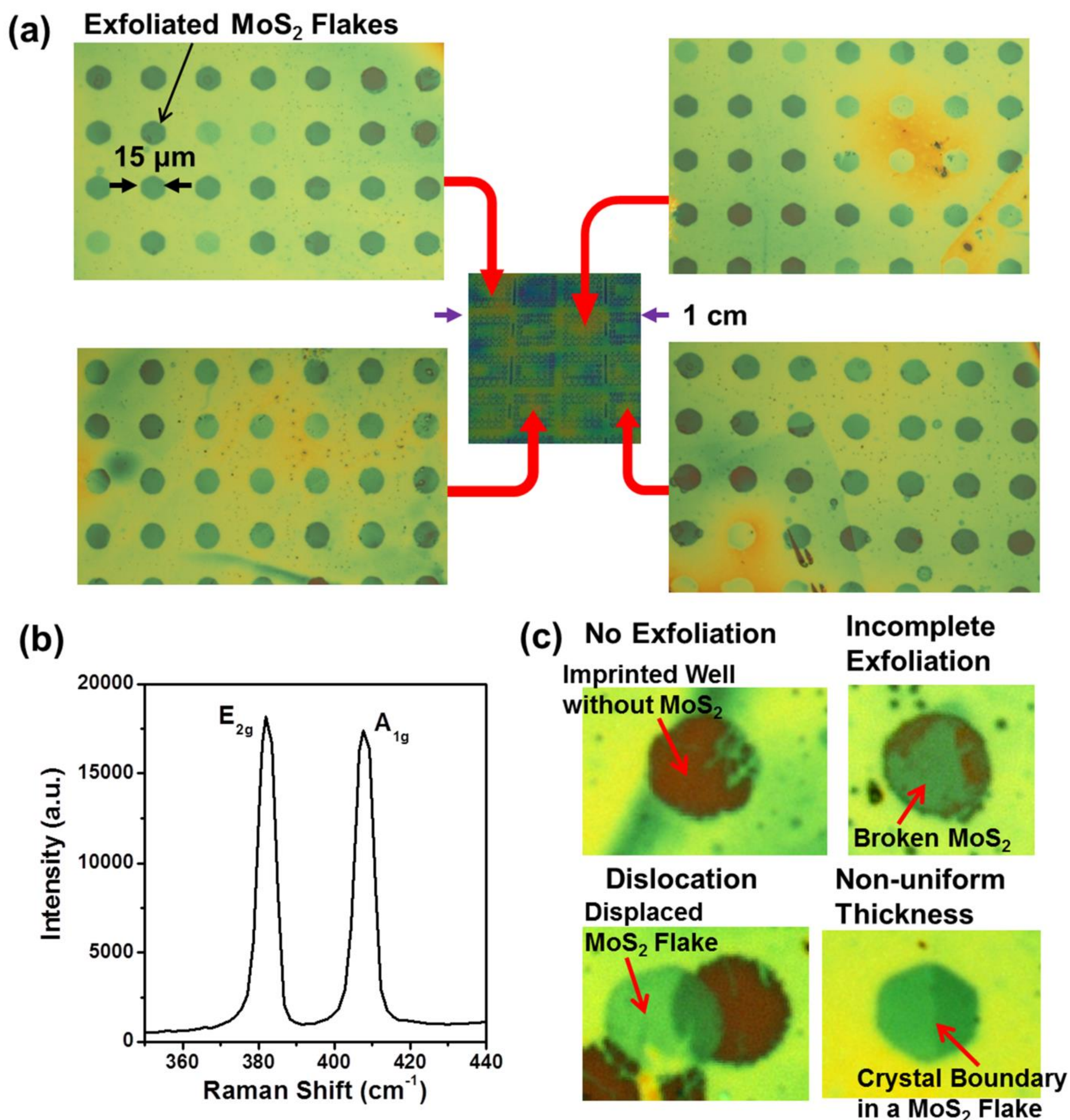


Figure 2.5 NASE results: (a) four optical micrographs of MoS_2 flake arrays imprinted/exfoliated into a PS fixing layer coated on a SiO_2/Si substrate by using NASE, which were captured from different locations over the whole NASE-processed area (~1 cm^2), as mapped in the inset photograph of the whole NASE sample; (b) Raman spectrum of an exemplary multilayer MoS_2 flake; (c) optical micrographs of typical imperfections that occur in NASE.

The thicknesses of NASE-produced MoS_2 flakes cannot be directly measured by using atomic force microscopy (AFM) or the color coding method [92], as they are embedded into the polymeric fixing layers. Especially, it is noted that our MoS_2 flakes, under OM illumination, exhibit varying colors ranging from green to deep blue, as demonstrated in Figure 2.5 (a). Such a color variation among MoS_2 flakes are mainly attributed to the spatial variation of the PS film thickness or the residual layer thickness (RLT), which are caused by the nonflatness of our current MoS_2 stamps (or current commercially available MoS_2 ingots). Therefore, such a color variation does not correctly indicate the thickness distribution among exfoliated MoS_2 flakes. To evaluate the uniformity of NASE-produced MoS_2 flake thicknesses, we employed AFM to measure the effective well depth (d_W) values of imprinted PS wells bearing exfoliated MoS_2 layers, as illustrated in Figure 2.6 (a). The d_W value of a MoS_2-embeded well is assumed to be the difference between the imprint depth (d_{NIL}, or the initial height of MoS_2 mesas pre-structured on the stamp) and the thickness (t_{MoS2}) of the MoS_2 flake embedded inside this well. Figure 2.6 (b) shows a 3-D AFM image of an exemplary NASE-produced MoS_2 flake exfoliated into an imprinted PS well. The dashed line indicates an AFM scanline that is re-plotted in Figure 2.6 (c). The d_W value of this MoS_2-embeded well is measured from the topographic difference between the center of this MoS_2 flake and a location outside the well, as indicated by the red arrows in Figure 2.6 (c). For this specific imprinted well, d_W is measured to be ~0, indicating that $t_{MoS2} \sim d_{NIL} = 50$ nm. Figure 2.6 (d) displays the statistics of d_W/d_{NIL} values measured from 100 imprinted wells bearing MoS_2 flakes. These structures were produced in a single NASE process. Figure 2.6 (d) shows that the standard deviation of d_W/d_{NIL} data (or the relative thickness error of NASE-produced multilayer MoS_2 flakes) is estimated to ~12%. This relative thickness error is much smaller comparing to

those of multilayer structures fabricated by previously reported exfoliation-based methods [55, 81, 93-95].

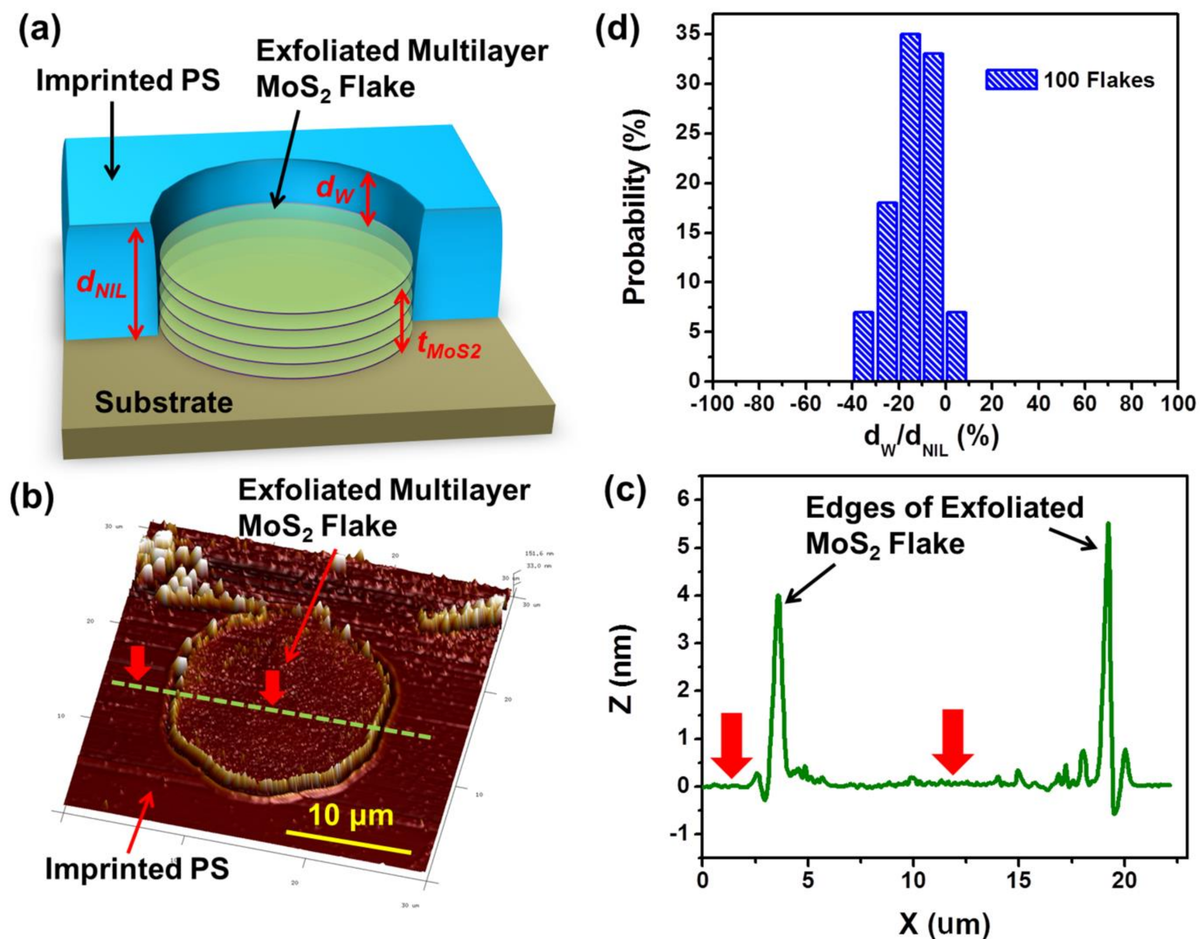


Figure 2.6 AFM characterization of NASE-produced MoS_2 flakes exfoliated into a PS fixing layer: (a) schematic of a multilayer MoS_2 flake with thickness of t_{MoS2} exfoliated into an imprinted PS well with imprint depth of d_{NIL}, resulting in an effective well depth of d_W; (b) an exemplary 3-D AFM image of a multilayer MoS_2 flake exfoliated into an imprinted PS well; (c) an AFM scanline extracted from the AFM image shown in (b) (*i.e.*, the dashed line shown in (b)), from which the d_W value of this MoS_2-embeded well can be measured from the topographic difference between locations denoted with arrows; (d) statistics of d_W/d_{NIL} data measured from 100 MoS_2-embeded wells, which shows that the standard deviation of d_W/d_{NIL} data (or the relative thickness error of NASE-produced multilayer MoS_2 flakes) is estimated to ~12%.

2.3.2 Transistor Array Made from NASE-Produced MoS_2 Channels

To evaluate the uniformity of the electronic properties of multilayer MoS_2 flakes produced by NASE, back-gated field-effect transistor (FET) arrays were fabricated with NASE-produced MoS_2 channels and the statistical data of the multiple FET transfer characteristics was obtained. Figure 2.7 (a) schematically illustrates the FET structure. Figure 2.7 (b) shows the SEM images of a representative FET array made from the multilayer MoS_2 flakes produced in a NASE process. For all as-fabricated FETs, the channel width (W) and length (L) are 15 and 10 μm, respectively; the MoS_2 channel thickness is around 20 nm; the back-gate dielectric consists of a 300 nm thick thermally grown SiO_2 layer plus a residual PS layer. Here, the residual PS thickness ($t_{residual}$) under each MoS_2 channel is estimated to be thinner than 5 nm by using $t_{residual} = t_{PS} - d_{NIL}$, in which t_{PS} is the initial PS layer thickness before the NASE process. More details about the fabrication of MoS_2 FET arrays can be found in Section 2.2.5.

It should be noted that our current post-NASE FET fabrication process sometimes results in the peeling off of the NASE-produced MoS_2 flakes and thus need to be further optimized. This is because of the poor adhesion between layered materials and most of substrate materials. This issue is not only for NASE-produced MoS_2 samples, but also generally for all 2D layered materials. Exploring the ultimate solution to this problem is underway but still beyond the scope of the present work. Fortunately, in our work, the survived MoS_2 flakes remain staying at their original locations in the array, and the yields of working FETs over cm^2-scale areas are typically 50-60% (the yield of NASE-produced MoS_2 flakes is ~80%). Such samples are sufficiently good for providing a number of FETs to evaluate the uniformity of the electronic properties of NASE-produced MoS_2 flakes.

Appendix A displays the transfer characteristics (*i.e.*, drain-source current (I_{DS}) -gate voltage (V_G) curves measured under a given drain-source voltage (V_{DS} = 1 V)) across 45 as-fabricated FETs. These FETs were made from the multilayer MoS_2 flakes produced in a NASE process and distributed over a 1 cm^2 area. Figure 2.7 (c-f) show the statistics of field-effect mobility (μ), On/Off currents (I_{ON} is the I_{DS} measured at V_G = 60 V; I_{OFF} is the minimum value of I_{DS} within the V_G range of (60 V), subthreshold swing (SS), and threshold voltage (V_T) data, which were extracted from the transfer characteristic curves of these 45 FETs. Specifically, the mean values of μ, I_{ON}, I_{OFF}, SS, and V_T were statistically measured to be $\mu = 46 \pm 10$ cm^2/ (V s), $I_{ON} = 24.0 \pm 5$ μA (or, 1.60 ± 0.33 μA per 1 μm channel width), $I_{OFF} = 21 \pm 20$ pA, SS = 11.9 ±2.7 V/dec, and $V_T = 28 \pm 8$ V, respectively. First, it should be noted that the relatively large SS values of our FETs are attributed to the relatively thick back-gate dielectric (*i.e.*, 300 nm SiO_2) used here, and such SS values could be significantly reduced by using much thinner dielectrics. The I_{OFF} data of our FETs exhibit a much larger relative standard deviation (~95%) as compared to other parameters, which is mainly attributed to the measurement precision (2-10 pA) of our semiconductor analyzer. The quantity V_T could have zero or negative values, and therefore the relative standard deviation of V_T data is meaningless for evaluating the uniformity of our FETs. Therefore, we specifically use the relative standard deviations of μ, I_{ON}, and SS data for evaluating the uniformity. The relative standard deviations of these parameters range from 21 to 23%. This shows that even though our post-NASE FET fabrication process is yet to be optimized, our current FET arrays made from NASE-produced multilayer MoS_2 flakes already exhibit a good uniformity in critical FET parameters. The observed variances in the performance parameters of our FETs are mainly attributed to several possible factors, including (1) the device-to-device variance in the residual PS

layer thicknesses; the NASE-introduced defects, as discussed above (Figure 2.5 (c)); (3) the contaminants introduced during the post-NASE FET fabrication processes; (4) intrinsic non-uniformity of the material properties of initial MoS_2 ingots (*e.g.*, crystal orientations, domain size distributions, and intrinsic defects).

To further investigate the effect of the residual polystyrene (PS) layers on the uniformity of the electronic properties of NASE-produced MoS_2 flakes, another batch of MoS_2 FETs were fabricated using an alternative method to eliminate residual PS. To make such FETs, a SiO_2-coated p^+-Si substrate bearing NASE-produced MoS_2 flakes was soaked in toluene for 1-2 h. Until this step, the sample had not been subjected to any plasma etching. Therefore, the imprinted PS on the substrate (including the residual PS layers under MoS_2 flakes) was able to be completely removed because there is no cross-linking in PS. However, this cleaning process displaced (and even peeled) many MoS_2 flakes and only a few survived MoS_2 flakes were chosen for making FETs. Because the selected MoS_2 flakes had been shifted away from their original array configurations, we had to perform repetitive lithography, metal deposition, and lift-off processes for making multiple FETs. In particular, special finger contacts (5 nm Ti/50 nm Au) were fabricated to access to individual selected MoS_2 flakes. This was a time-consuming task and resulted in a much lower device yield as compared to the method, discussed above, for making FET arrays with the residual PS. Figure 2.8 displays two representative back-gated FETs made from multilayer MoS_2 flakes that were cleaned by Toluene. Figure 2.9 shows the transfer characteristics of 11 such FETs made from PS-free multilayer MoS_2 flakes, and Figure 2.10 displays the statistics of (a) mobility (μ), (b) On/Off currents (I_{ON} and I_{OFF}), (c) subthreshold swing (SS), and (d) threshold voltage (V_T)

data measured from these 11 FETs. For the following discussion, these FETs are referred to as PS-free FETs, and the previous array FETs as shown in Figure 2.7 are referred to as PS-retained FETs.

First, our device characterization shows that the field-effect mobility data measured from our PS-retained FETs (*i.e.*, $\mu = 46 \pm 10$ cm^2/(V s)) have a slightly smaller mean value and a slightly larger standard deviation in comparison with those measured from our PS-free FETs (*i.e.*, $\mu = 53 \pm 7$ cm^2/(V s)). This slight difference is attributed to the roughness scattering at the MoS_2/PS interface, which could slightly reduce the field effect mobility of the multilayer MoS_2 FET and broaden the dispersion of the mobility values measured from different FETs. Because such a PS-induced mobility reduction is estimated to be only ~13%, we can think that the presence of residual PS between multilayer MoS_2 flakes and SiO_2 gate dielectrics does not result in a detrimental damage to the mobility property of multilayer MoS_2 FETs. In comparison with our PS-retained FETs, our PS-free FETs exhibit a smaller average SS (*i.e.*, SS = 8.4 ± 1.1 V/dec for PS-free FETs, whereas SS = 11.9 ± 2.7 V/dec for PS-retained ones). This difference is attributed to that the residual PS layer under a MoS_2 FET channel introduces an additional capacitor connected with the SiO_2 capacitor in series, which decreases the overall gate dielectric capacitance and therefore increases the SS value of this FET. In addition, the relative standard deviation of the SS data measured from PS-retained FETs (~23%) is noticeably larger than that measured from PS-free FETs (~13%). This is attributed to the non-uniformity of the residual PS layer thicknesses under NASE-produced MoS_2 flakes, which may introduce an additional non-uniformity in back-gate capacitances and hence the SS data of PS-retained FETs. In comparison with PS-free FETs, the PS-retained FETs have statistically more positive V_T values (*i.e.*, $V_T = -27 \pm 10$ V for PS-free FETs,

whereas V_T = 28 ± 8 V for PS-retained ones). This difference is presumably attributed to the polymer-induced surface-charge-transfer (SCT) doping (*p*-type doping) in MoS_2 channels.

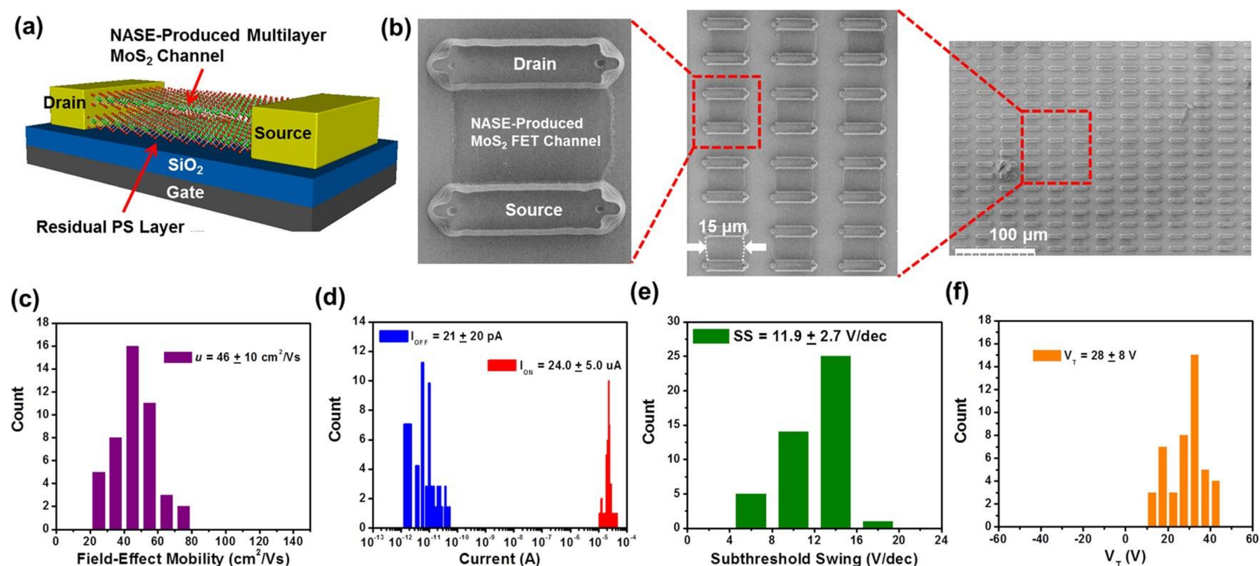


Figure 2.7 Back-gated FET arrays made from NASE-produced MoS_2 flakes: (a) Schematic illustration of a back-gated MoS_2 FET. (b) SEM images of a representative FET array made from the multilayer MoS_2 flakes (thickness ~20 nm) produced in a NASE process. For all FETs, the channel width (W) and length (L) are 15 and 10 μm, respectively; the back gate dielectric is 300 nm SiO_2 + residual PS (estimated to be thinner than 5 nm). The following graphs display the statistics of (c) mobility (μ), (d) On/Off currents (I_{ON} and I_{OFF}), (e) subthreshold swing (SS), and (*f*) threshold voltage (V_T) data measured from 45 MoS_2 FETs fabricated by a NASE process. Appendix A lists the transfer characteristics of these 45 FETs.

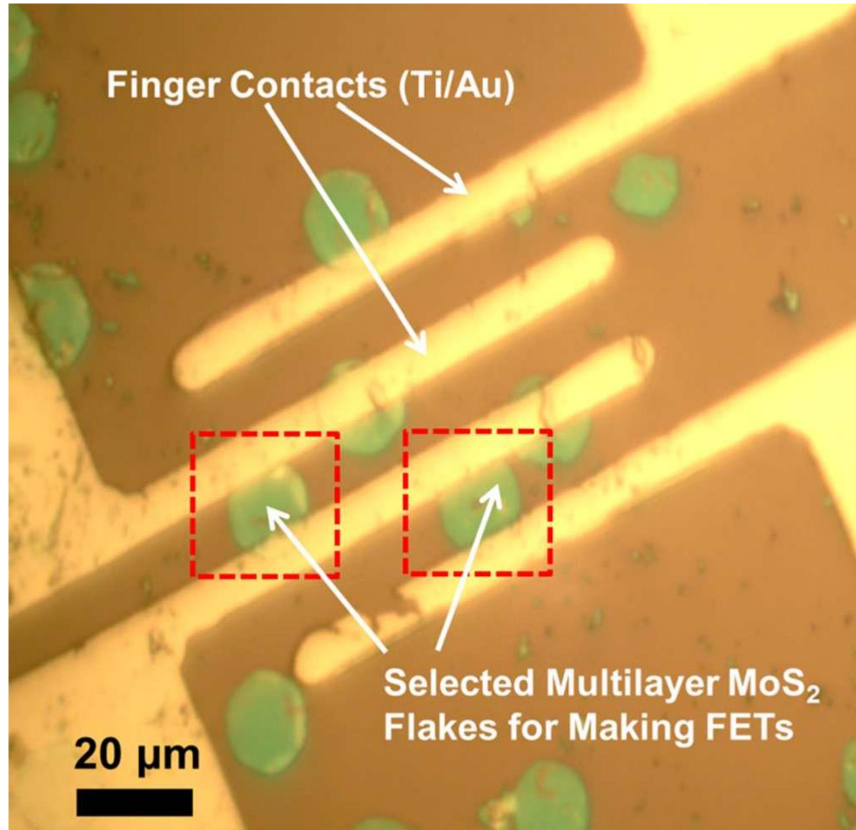


Figure 2.8 Optical micrograph of two representative back-gated FETs made from selected NASE-produced multilayer MoS_2 flakes. These NASE-produced MoS_2 flakes (~30 nm thick) were soaked in toluene for 1-2 hours in order to remove the residual PS layers under them. This toluene etching process shifted most MoS_2 flakes away from their original locations in the array. Therefore, to make working FETs, special finger contacts (5 nm Ti/50 nm Au) were fabricated to access to individual selected MoS_2 flakes.

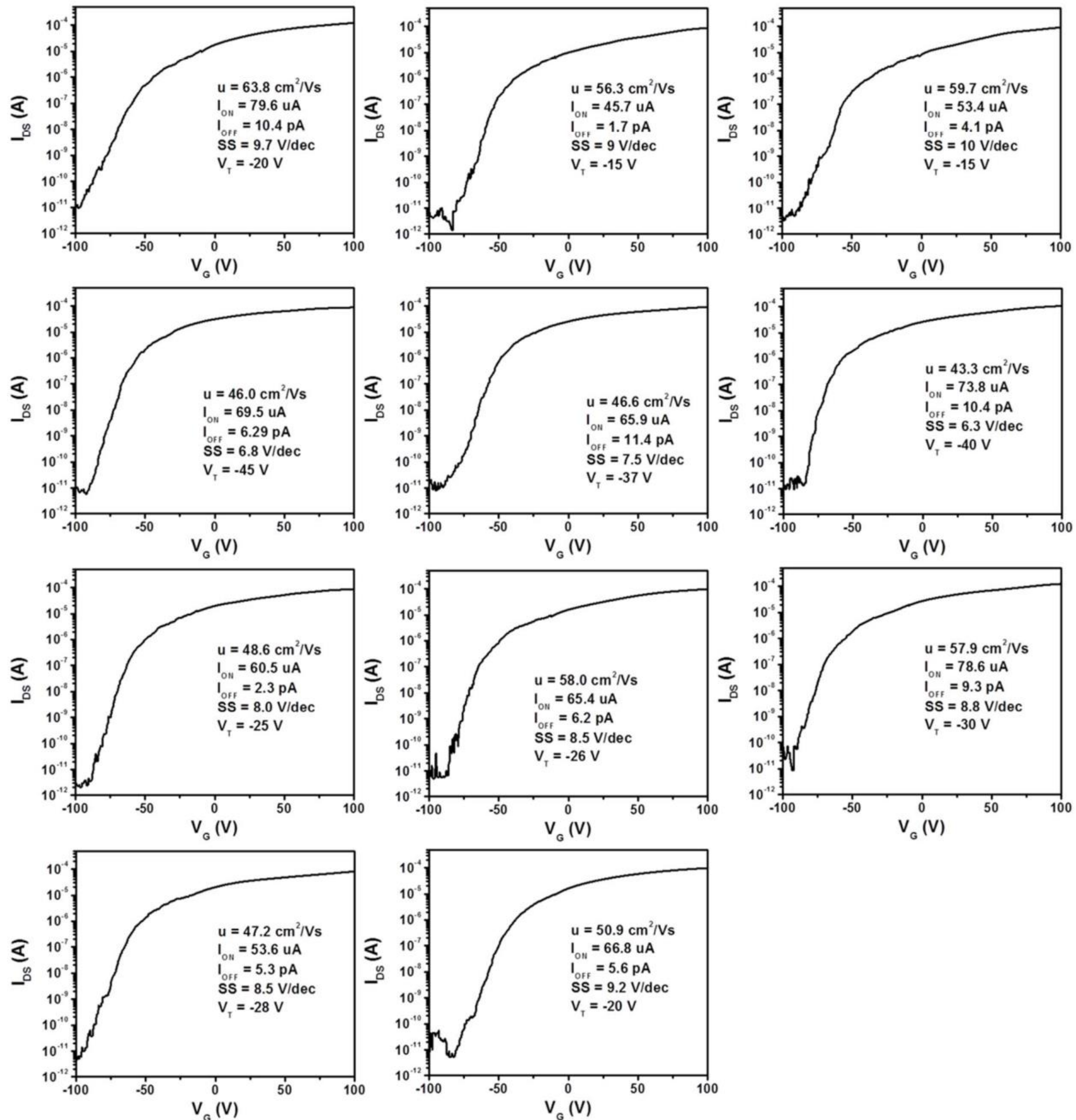


Figure 2.9 Transfer characteristics of 11 back-gated field-effect transistors (FETs), which were made from NASE-produced multilayer MoS_2 flakes. For these FETs, the residual PS layers under MoS_2 channel flakes were completely removed by toluene. This toluene cleaning process shifted MoS_2 flakes away from their original locations in the array. Therefore, these devices had to be fabricated using repetitive lithography and metallization processes, resulting in a much lower yield as compared to the method for making FET arrays along with the residual PS.

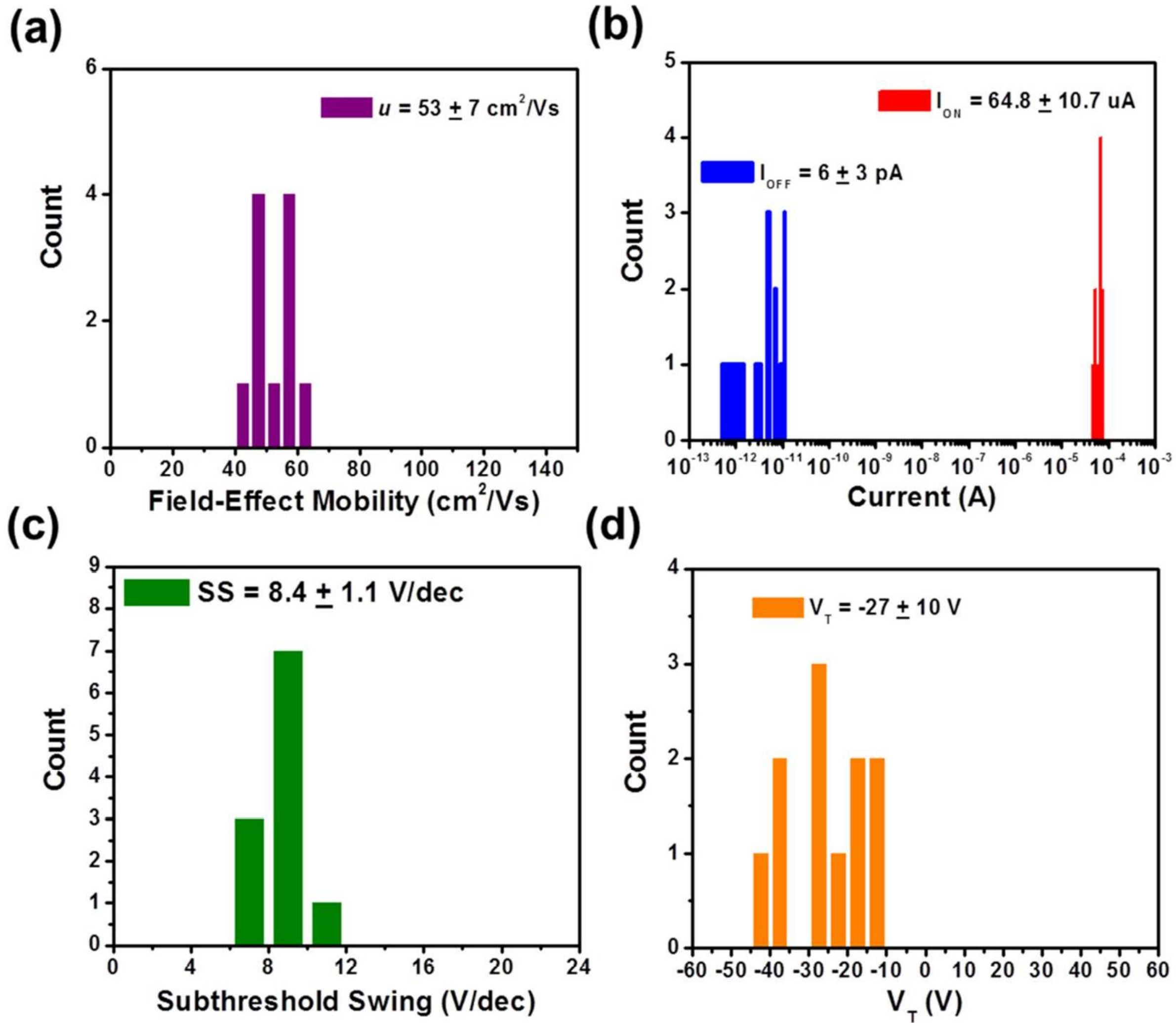


Figure 2.10 Statistics of (a) mobility (μ), (b) On/Off currents (I_{ON} and I_{OFF}), (c) subthreshold swing (SS), and (d) threshold voltage (V_T) data measured from 11 FETs made from NASE-produced MoS_2 flakes. These selected MoS_2 flakes were cleaned with toluene. Figure 2.9 lists the transfer characteristics of these 11 FETs.

More importantly, our NASE-produced MoS_2 transistors can be directly implemented as electronic biosensors for detecting and quantifying specific illness-related biomarkers. In this work, we specifically demonstrated quantification of a standard curve for tumor necrosis factor-alpha (TNF-α) detection by using multiple MoS_2 FET biosensors. Figure 2.11 (a) illustrates a MoS_2 FET

sensor functionalized with anti-human TNF-α antibody receptors for detecting TNF-α molecules. The details about fabrication and bio-functionalization of NASE-produced MoS_2 FET biosensors are described in the section of Methods and Materials. To realize biomarker quantification, multiple sensors with consistent sensor responses to specific biomarker concentrations are needed. We choose the relative change of ON-state I_{DS} under a fixed set of V_G and V_{DS}, *i.e.*, $R = (I_{DS(anti)}-I_{DS})/I_{DS}$, as the sensor response quantity. Here, $I_{DS(anti)}$ is referred to be the ON-state I_{DS} measured from an as-functionalized sensor (*i.e.*, TNF-α concentration n = 0). Figure 2.11 (b) shows the transfer characteristics of eight different MoS_2 FETs measured under a set of incremental TNF-α concentrations (*i.e.*, n = 0, 60 fM, 600 fM, 6 pM, and 60 pM). The sensor responses (*i.e.*, values of $R = (I_{DS(anti)}-I_{DS})/I_{DS}$) were extracted at a fixed V_G=98 V (*i.e.*, ON-state) and plotted with respect to TNF-α concentration (n) in Figure 2.11 (c). Figure 2.11 (c) shows that the R-n relationships measured from multiple NASE-produced sensors exhibit a high degree of device-to-device consistency and can serve as a standard curve for TNF-α quantification. These R-n relationships can be well fitted with Langmuir isotherm, and the equilibrium constant of the antibody-(TNF-α) pair was extracted to be $K_D = 308 \pm 33$ fM. These device demonstrations have preliminarily demonstrated that NASE can produce multilayer TMDC device structures with a high uniformity of electronic properties. In addition, it should be noted that our MoS_2 FET biosensors exhibit a very low limit-of-detection (LOD) (estimated to be lower than 60 fM). In combination with the device multiplexing capability of NASE process, such a fM-level LOD would potentially enable new bioassay chips offering single-molecule-level analysis capabilities.

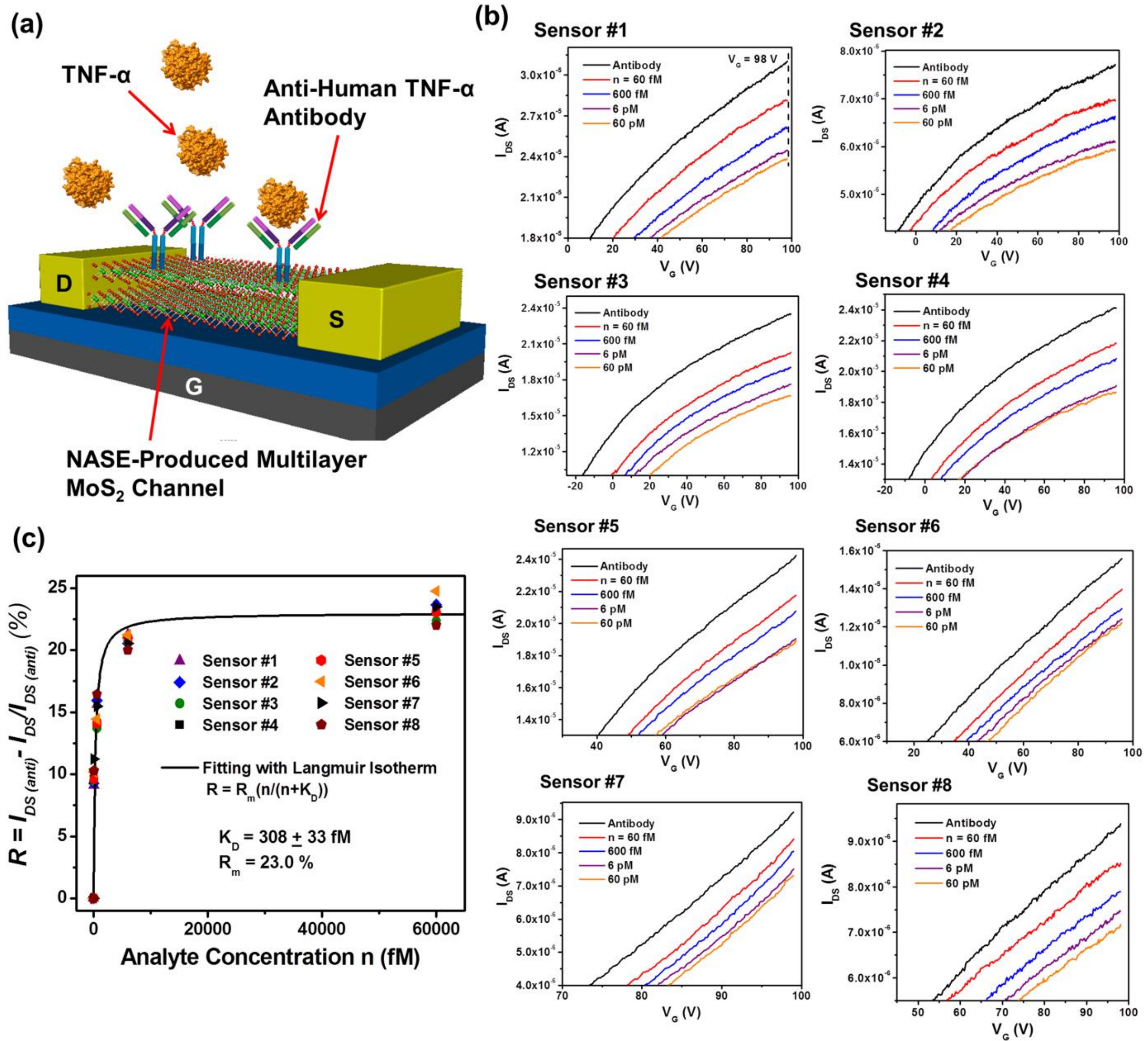


Figure 2.11 MoS_2 transistor biosensors made from NASE-produced multilayer MoS_2 flakes: (a) illustration of a MoS_2 transistor biosensor, in which anti-human TNF-α antibodies are directly functionalized on the MoS_2 transistor channel; (b) sensor responses (*i.e.*, transfer characteristics) to various TNF-α concentrations (*i.e.*, n = 0, 60 fM, 600 fM, 6 pM, and 60 pM) measured from eight different sensors; (c) calibrated responses (*i.e.*, relative change of ON-state I_{DS} measured at a fixed V_G=98 V) with respect to n, measured from difference sensors, which exhibit a high degree of device-to-device consistency and can be well fitted with Langmuir isotherm.

2.3.3 Molecular Dynamics Simulation of NASE process

In our work, we have experimentally demonstrated that NASE could produce multilayer TMDC structures with microscale lateral sizes. To further evaluate the scalability of NASE for generating atomically layered structures with nanoscale lateral dimensions, we performed a molecular dynamics (MD) simulation of NASE processes for exfoliating nanoscale-lateral-size layered structures. In this simulation work, we specifically simulated the shear exfoliation of few-layer-graphene nanostructures into PS fixing layers, because few-layer-graphene has the simpler crystal structure than TMDCs, which can simplify our simulation, but graphene layers exhibit very similar mechanical properties with most TMDCs. Figure 2.12 shows the simulation results of a NASE process for exfoliating 5 nm size, 4-layer graphene mesas into a PS layer. In particular, Figures 2.12 (b)-(e) display a set of snapshots of the simulated post-nanoimprint shear exfoliation stages at a set of selected times (t = 0, 50, 90 ns). These dynamic simulation results show that at least three layers from a mesa can be reliably exfoliated and trapped into the imprinted PS well, whereas the layer closest to the top edge of the PS well (*i.e.*, the green layer shown in Figure 2.12) exhibits a significant probability to be dislocated out of the PS well. Figure 2.12 (f) shows a zoomed view of the interface between the graphene layer edges and the sidewall of the imprinted PS well. From Figure 2.12 (f), it can be observed that the imprinted well is deep enough to prevent the trapped graphene layers from sliding over one another. This guarantees that the imprinted/exfoliated multiple layers can retain their original AB-stacking mode after a NASE process. These MD simulation results imply that NASE could be potentially used for generating high-quality nanoscale-lateral-size layered device structures. More details about the MD simulation setup are described in Section 2.2 Materials and Methods.

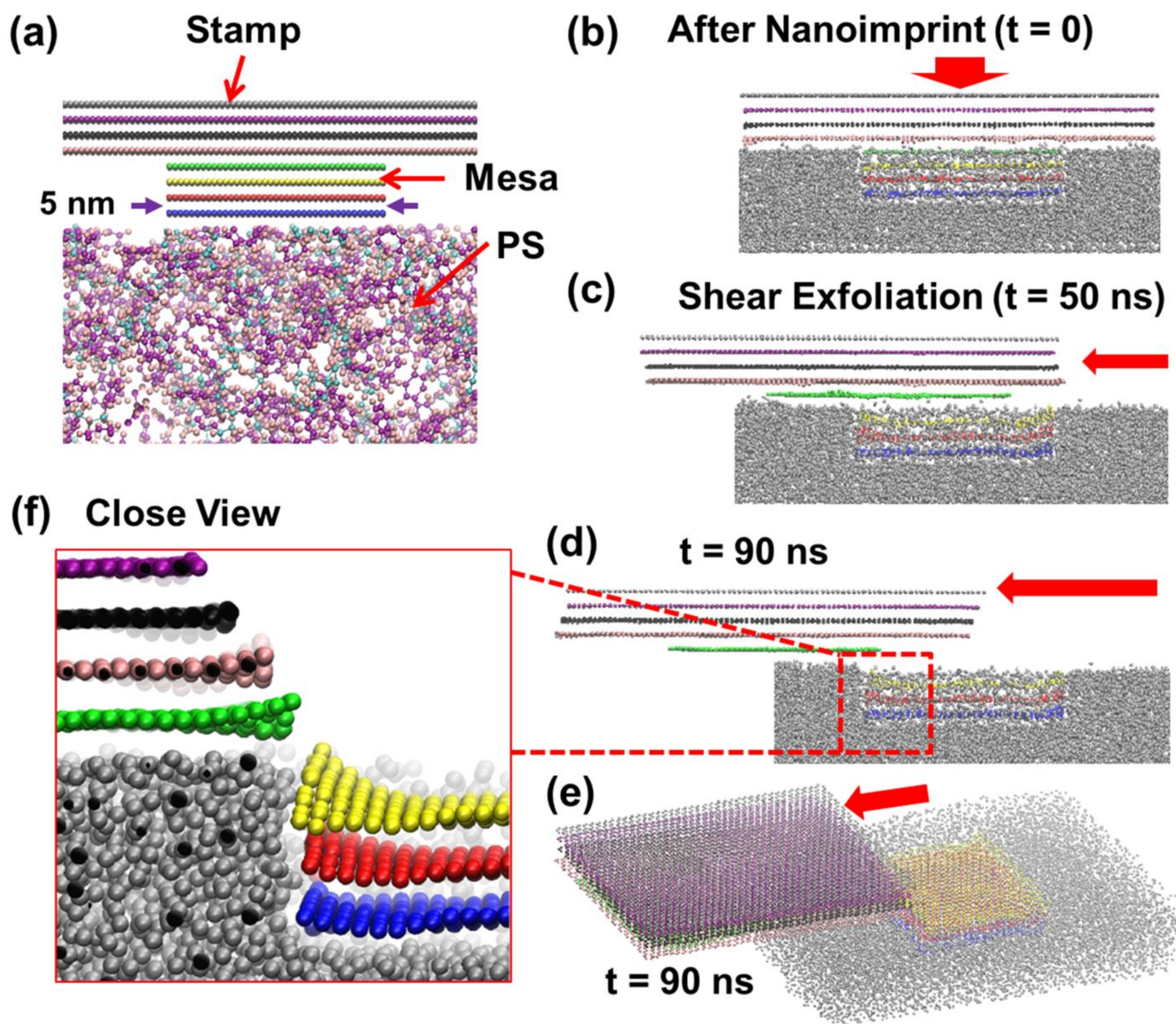


Figure 2.12 Molecular dynamics (MD) simulation of a NASE process for exfoliating atomically layered nanostructures: (a) a selected part of the 3-D simulation region, showing the cross-sectional view of the initial configuration of a NASE process, involving a graphite stamp bearing 5 nm size, 4-layer mesas and a PS fixing layer; (b)-(d) cross-sectional snapshots of the MD simulation result of a post-nanoimprint shear exfoliation course at t = 0, 50, 90 ns; (e) a 3-D snapshot of the simulated system at t = 90ns; (f) a zoomed view of the imprinted PS well bearing graphene layers, especially displaying the interface between the edges of exfoliated layers and the sidewall of the imprinted PS well.

Additionally, we also used MD simulations to evaluate the effects of the geometric dimensions of pre-structured stamping structures on the resultant morphology of NASE-produced

layered nanostructures. For example, we simulated a NASE process for exfoliating relatively low-aspect-ratio graphene nanostructures (*i.e.*, 50 nm size, bilayer graphene mesas pre-structured on a stamp), as shown in Figure 2.13. Specifically, Figures 2.13 (a) and (b) display two cross-sectional snapshots of the post-nanoimprint shear exfoliation course taken at t = 0 and 1 ns, respectively. Figure 2.13 (b) shows that the imprinted bilayer mesa is pulled out of the imprinted PS by the bulk stamp moving along a shear direction, and the imprinted PS well fails to immobilize such low-aspect-ratio structures. This can be attributed to the fact that the layered structures with a lower aspect-ratio possess much lower bending rigidity than the ones with a higher aspect-ratio, because the bending rigidity of a solid flake can be expressed as $Eh^3/12(1\text{-}v^2)$, where E, h, and v are the Young's modulus, thickness, and Poisson's ratio of the flake. Therefore, relatively low-aspect-ratio layered structures can easily deform under the shear stress exerted by the bulk stamp, and therefore they can be easily pulled out of the imprinted well. Our simulation shows that the initial form of such shear-stress-induced deformation in exfoliated mesa layers is a set of nanoscale wrinkles. Figures 2.13 (c) and (d) display the tilted and side views, respectively, of a 3-D snapshot of the low-aspect-ratio graphene layers at t = 1 ns, which exhibits a set of wrinkle features induced by the shear dislocation process. Such wrinkle features do not appear in relatively high-aspect-ratio layered nanostructures (*e.g.*, 5 nm size, 4-layer mesas shown in Figure 2.12) due to their large in-plane stiffness. In addition, our simulations indicate that the large deformations created in relatively low-aspect-ratio layered structures can reduce the cohesive energies of graphene/graphene as well as graphene/PS interfaces, and further enhance the occurring probability of the detachment of imprinted/exfoliated layers from the PS layer. Therefore, our MD simulation results, consistent with our experimental results, also suggest that NASE is more suitable for producing uniform

multilayer structures with relatively high aspect-ratios than to producing monolayer/few-layer structures with relatively low aspect-ratios. However, as mentioned above, NASE-produced multilayer structures with uniform initial thicknesses could be further trimmed to arbitrary thinner thicknesses by using established layer-thinning approaches [88, 89]. As discussed above, in a real NASE process, when a MoS_2 stamp is sheared horizontally, a vertical pressure is applied to the stamp to avoid the ripple formation. More details on the relationship between the flake rigidity and the required vertical pressure is qualitatively discussed in Appendix B.

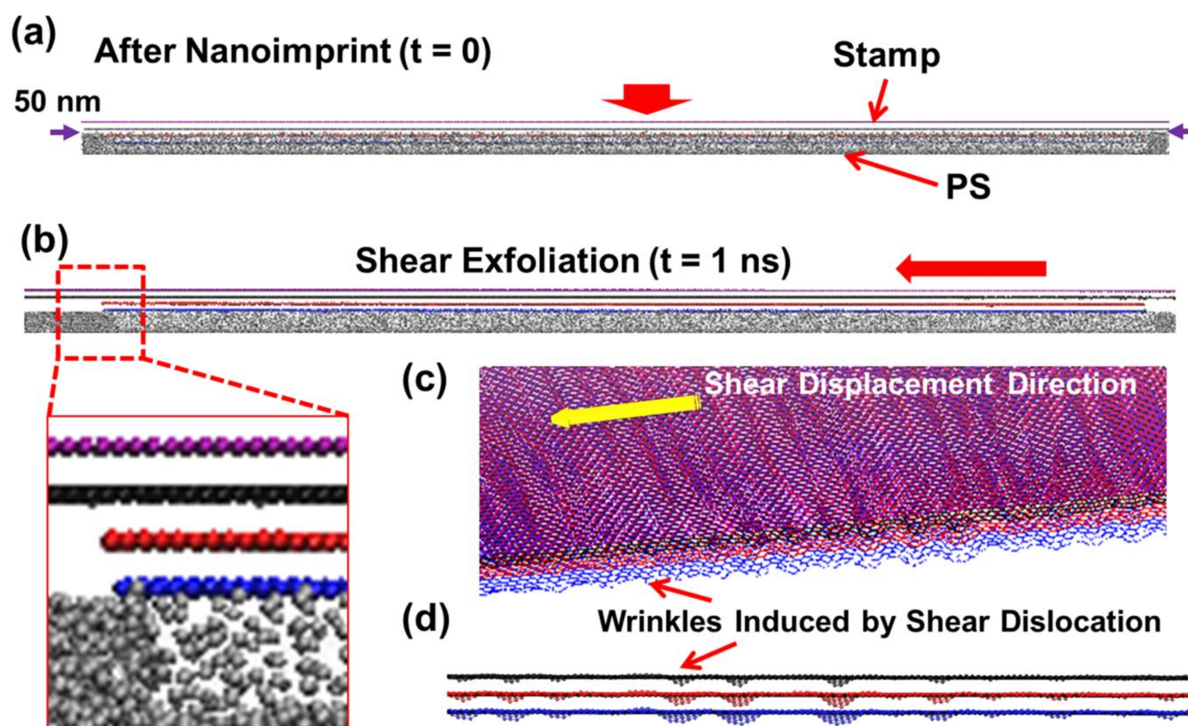


Figure 2.13 Molecular dynamics (MD) simulation of a NASE process for exfoliating relatively low-aspect-ratio layered structures: (a) a cross-sectional snapshot of the NASE stage, in which a graphite stamp bearing 50 nm size, bilayer mesas has been imprinted into a PS fixing layer (*i.e.*, $t = 0$); (b) a cross-sectional snapshot of the post-nanoimprint shear exfoliation course taken at $t = 1$ ns; (c) and (d) are tilted and side views, respectively, of a 3-D snapshot of the simulated system at $t = 1$ ns, which exhibits wrinkle features induced by the shear dislocation process.

2.4 Summary

In conclusion, we present a top-down nanofabrication method termed as nanoimprint-assisted shear exfoliation (NASE), which is capable of producing high-quality multilayer TMDC device structures with a high uniformity in both feature thicknesses and electronic properties. NASE uniquely combines the nanoimprinting and shear exfoliation of pre-structured layered nano/microstructures into polymeric fixing layers. Our experiments demonstrate that such a NASE mechanism can result in high-quality 40-200 nm high, 10-15 μm size MoS_2 flake arrays with a high uniformity of flake thicknesses (*i.e.*, relative thickness error ~ 12%) over cm^2-scale areas, which surpasses the performance of previously reported exfoliation methods for generating layered materials, in terms of large-area ordering and thickness uniformity of exfoliated structures. Using NASE, we have demonstrated the fabrication of multiple working FETs and FET-based biosensors with multilayer MoS_2 channels. These functional devices exhibit very consistent performance, and the characterization data measured from these devices show that NASE-produced MoS_2 flakes have a high uniformity of electronic properties. Especially, our FET-based biosensors exhibit a high device-to-device consistency in the sensor responses to specific biomarkers. Using multiple such biosensors, we have preliminarily demonstrated quantification of standard curves for fM-level illness-related biomarker detection as well as biomarker-antibody affinity properties. Furthermore, our MD simulation results of NASE processes suggest that the presented shear-exfoliation mechanism could be further developed for generating nanoscale-lateral-size layered structures for meeting the ever-evolving demands for device miniaturization. Such a MD simulation model also provides critical information for understanding the effects of the geometric dimensions of pre-structured stamping structures on the resultant morphology of NASE-produced layered

nanostructures. This work advances critical nanofabrication/nanomanufacturing knowledge toward ultimately realizing upscalable production of highly uniform TMDC device arrays, and the presented NASE approach could potentially be exploited to leverage the superior properties of TMDCs for scale-up electronic applications.

Chapter 3

MoS_2 Rectifying Diodes Formed by Plasma-Assisted Doping

3.1 Introduction

For practical device application, the NASE-produced flake array need to be further doped. For example, to further realize MoS_2-based complementary electronic circuits and novel optoelectronic devices based on the valley-sensitive optical properties of MoS_2, ones demand upscalable techniques for realizing controlled doping and creating *p-n* junctions in MoS_2 and other 2D semiconductors. Fang *et al*. recently reported the degenerate *n*-doping of MoS_2 and WSe_2 layers using a potassium dispenser, which can improve the contact resistances between these 2D materials and metals [59]. Zhang *et al*. formed rectifying *p-n* junctions in liquid-gated MoS_2 field-effect transistors (FETs), but the direct observation of rectifying effects needs the cooling of the FETs below the glass transition temperature (*i.e.*, ~ 180 K) of the gating liquid in the ambipolar region [60]. In addition, Yuan *et al*. found that the ozone treatment can dramatically decrease the sheet resistance of graphene films by *p*-doping, but such *p*-doping can only remain for hours [61]. This is attributed to the desorption of physisorbed ozone that is weakly attached to graphene [61]. Therefore, it is highly desirable to develop new methods for creating stable *p-n* junctions and

rectifying diode structures in MoS_2 and other TMDCs for long-term applications at ambient conditions.

In this chapter, we create stable rectifying diodes working at ambient conditions with the selected-area treatment of MoS_2 films with fluorine (F)-and oxygen (O)-contained plasma recipes. To identify the underlying physical mechanism responsible for such plasma-induced rectifying characterisitics, we systematically investigated the transport and surface-compositional properties of FETs blank-treated with plasmas. These works unambiguously confirm that the rectification behavior of our MoS_2 diodes is attributed to the plasma-induced *p*-doping in the intrinsic *n*-type MoS_2 flakes, which further forms a stable *p-n* junctions.

3.2 Fabrication of MoS_2 Diode by Plasma-Assisted Doping

To fabricate MoS_2 diodes, first multilayer MoS_2 flakes were exfoliated onto p^+-Si/SiO_2 substrates (oxide thickness, t_{ox}=300 nm) by using previously reported printing methods [55, 94, 95]. The flake thickness was characterized by a color coding method and subsequently confirmed by using an atomic force microscope (AFM). Figure 3.1 (a) shows an optical microscope (OM) image of printed MoS_2 flakes (size ~ 10 μm) that exhibit different colors corresponding to different flake thicknesses. MoS_2 flakes with average thickness within a range of t = 20 to 25 nm were chosen for this work, because of relatively high yield of such flakes. To enable selected-area plasma treatment of MoS_2 flakes, photolithography was performed to form patterned resist layers that cover half the area of each of chosen flakes. The uncovered regions of these flakes were treated or partially etched with one of widely used plasmas (*e.g.*, SF_6, CF_4, CHF_3, O_2, CH_4, H_2, and Ar) using a reactive ion etching (RIE) tool (Plasma-Therm 790 Etcher). For all plasma recipes, the

RF power was 100 W and the pressure was 10 mTorr. All recipes can result in the physical or/and chemical etching of MoS_2 flakes. The final thickness of selected areas treated by these plasmas is always controlled to be ~67% of the initial flake thickness (*i.e.*, the final thickness of plasma-treated areas, t_F = 13-16 nm). For example, Figure 3.1 (b) shows the OM image of a MoS_2 flake treated by CF_4 plasma. The untreated region exhibits light blue color (thickness, t~20 nm), while the plasma-treated region shows dark blue color (thickness, t ~ 13 nm). After the plasma treatment, photoresist was removed, and Ti/Au (5 nm/50 nm) electrodes were fabricated using photolithography, metal deposition, and lift-off. As shown in Figure 3.1 (b), drain (D) and source (S) contacts are referred to the electrodes in contact with plasma-treated and untreated MoS_2 regions, respectively. The distance between D/S contacts is ~5 μm. In measurment, D/S/Si substrate contacts were biased to ground, D/S voltage (V_{DS}), and back gate voltage (V_G), respectively, as illustrated by Figure 3.1 (c).

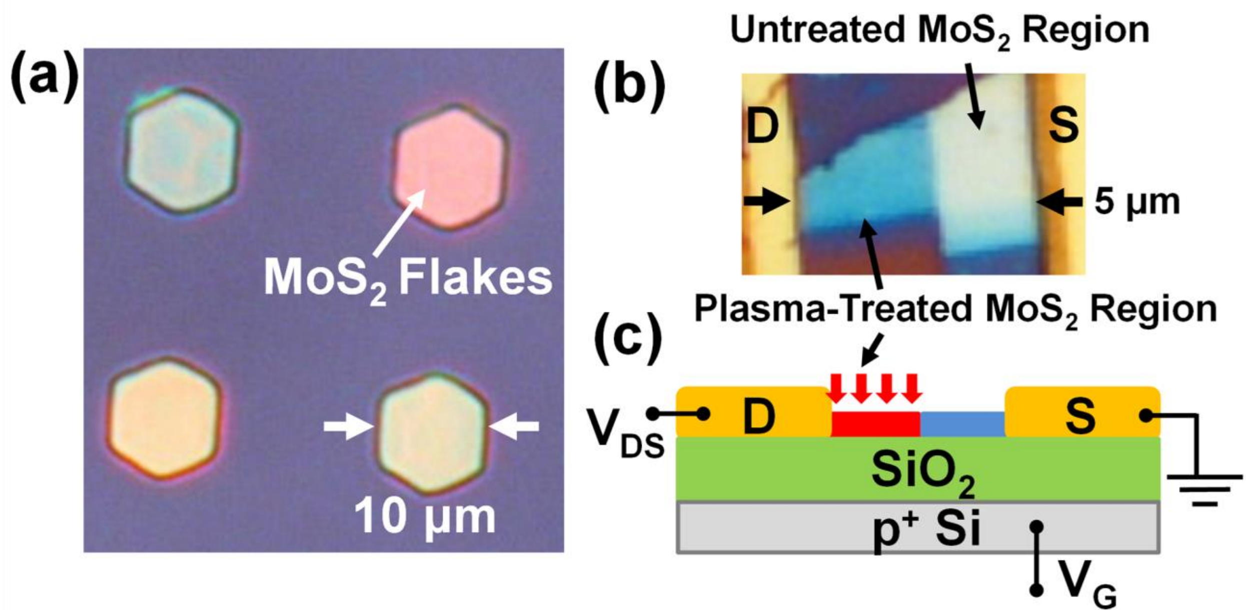


Figure 3.1 OM images of (a) exfoliated pristine MoS_2 flakes, and (b) a fabricated MoS_2 rectifying diode with selected area treated with CF_4 plasma. (c) Illustration of the electrical measurement setup of a back-gated MoS_2 diode.

3.3 Result and Discussion

3.3.1 Transport Characteristics of MoS_2 Diode and FET Formed by Plasma-Assisted Doping

Our electrical characterization result shows that only MoS_2 diodes treated with F- or O-contained plasmas (*e.g.*, SF_6, CHF_3, O_2, and CF_4) exhibit significantly current rectifying properties. Therefore, the following anlaysis and discussion only focus on the devices processed with these plasmas. Figures 2 (a)-(d) diplay I_{DS}-V_{DS} characteristics of MoS_2 diodes treated with SF_6, CHF_3, CF_4 and O_2 plasmas, respectively. All diodes exhibit a strong current rectification within a range of $V_{DS}= \pm 4$ V ($V_G= 0$ V). We use forward/reverse current ratios (I_F/I_R) measured at $|V_{DS}|= 1$ V (*i.e.*, $I_F(V_{DS}=1\ V)/I_R(V_{DS}= -1V)$) to evaluate the rectification degrees of all MoS_2 diodes (note that the I_F/I_R value for each of diodes is annotated in Figure 3.2). Based on this standard, the ranking order of plasma recipes in terms of their resulted rectification degrees (or I_F/I_R values) of diodes is SF_6> CHF_3> CF_4>O_2 (this order has been verified by testing several batches of diodes). Especially, SF_6-treated diodes exhibit the highest rectification degree ($I_F/I_R > 10^4$), which is also among the highest I_F/I_R values ever reported for rectifying diodes made from 2D materials [60, 96]. In addition, our MoS_2 diodes exhibit a superior long-term stability of transport characteristics. For example, Figure 3.2 (e) shows I_{DS}-V_{DS} characteristics of a SF_6-treated diode, which were measured 0 (dashed line) and 30 (solid line) days after the device fabrication (the device was stored at ambient conditions). After such a long-time storage, the device exhibits no significant degradation of the rectifying

property. This result indicates that such plasma-treated MoS_2 diodes are suitable for long-term applications at ambient conditions.

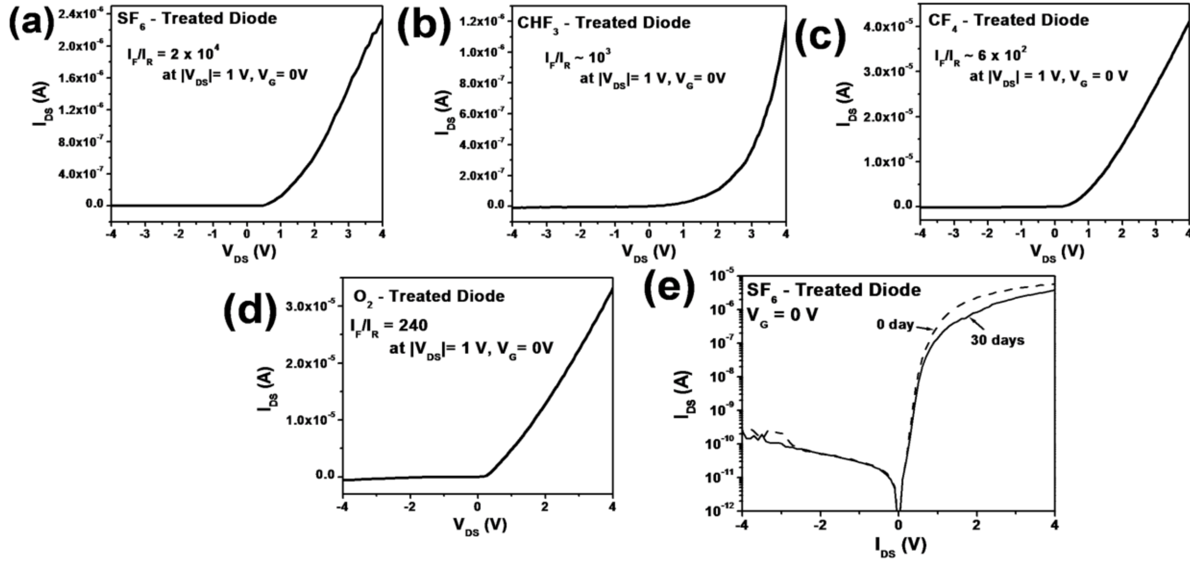


Figure 3.2 I_{DS}-V_{DS} characteristics of MoS_2 diodes treated by (a) SF_6, (b) CHF_3, (c) CF_4, (d) O_2-based plasmas (for all curves, $V_G = 0$ V). (e) Semi-logarithmic plots of I_{DS}-V_{DS} characteristic curves ($V_G = 0$ V) of a SF_6-treated diode, which were measured 0 (dashed line) and 30 (solid line) days after the device fabrication.

To further explore the in-depth device physics responsible for the rectifying characteristics of our MoS_2 diodes, we fabricated several back-gated FETs, in which the channels are made from 20-25 nm thick MoS_2 flakes blank-treated with the same plasma recipes (other fabrication details are the same as those for making diodes). Figure 3.3 shows I_{DS}-V_G characteristics of these FETs as well as a control FET made from an untreated MoS_2 flake. The untreated FET exhibits *n*-type conduction within a range of $V_G = \pm 100$ V, which is attributed to the intrinsic *n*-doping associated with naturally formed S-vacancies in pristine MoS_2 [97], and the threshold gate voltage ($V_{th\ (e)}$) of

the *n*-type conduction is arround -50 V. In comparison with the $V_{th\ (e)}$ of this untreated FET, $V_{th\ (e)}$ values of FETs treated with O_2, CF_4, CHF_3, and SF_6 shift toward more positive gate voltages and are measured to be +15, +44, +45, and a value > +100 V (*i.e.*, out of the range of V_G), respectively. In addition, within the range of V_G= ±100 V, CF_4-, CHF_3-, and O_2-treated FETs exhibit an ambipolar transport property with both *n*-type and *p*-type characteristics, and the SF_6-treated FET even shows a hole-dominated *p*-type transport property. These results indicate that the plasma treatment can induce *p*-doping in MoS_2 flakes. The *p*-doping strength in a FET can be qualitively characterized by the positive shift of the $V_{th\ (e)}$ of this plasma-treated FET relative to that of the untreated FET. The more positive shift of the $V_{th\ (e)}$ means the stronger *p*-doping strength. The ranking order of plasma recipes in terms of their resulted *p*-doping strengths is SF_6> CHF_3~ CF_4> O_2, which is similar to their ranking order in terms of their resulted rectification degrees of diodes. Therefore, it is strongly suggested that the rectifying property observed in our diodes can be attributed to the plasma-induced *p*-doping in originally *n*-type MoS_2 flakes, which forms *p-n* junctions in MoS_2; the stronger *p*-doping isexpected to result in the larger built-in potential barrier in a *p-n* junction and therefore the higher rectification degree of the diode.

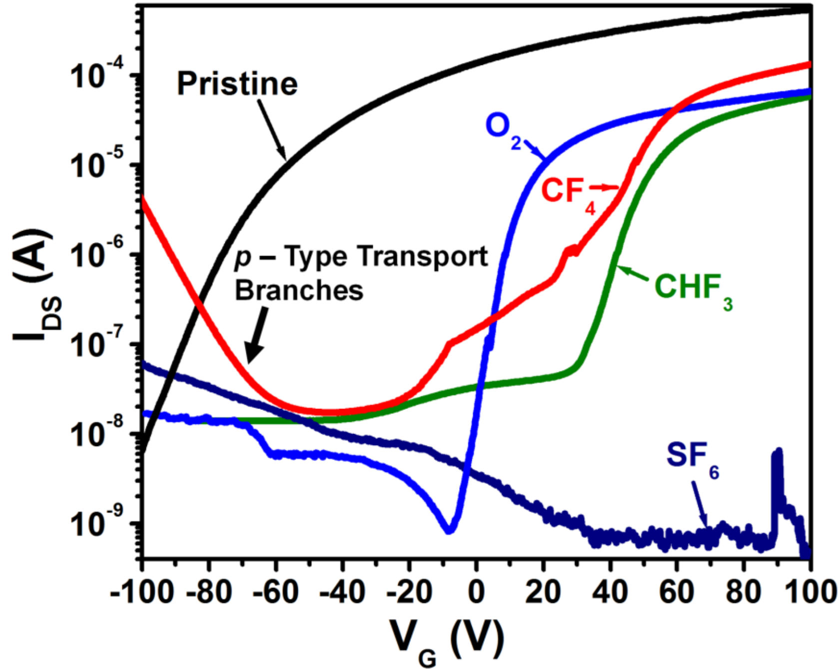


Figure 3.3 I_{DS}-V_G characteristics of back-gated MoS_2 FETs blank-treated with the same set of plasma recipes as the ones that were used for making diodes, as well as an untreated pristine FET (for all curves, V_{DS} = 5 V).

Another possible origin of the observed rectifying property in MoS_2 diodes is the Schottky barrier potentially formed between the Ti-based drain (D) electrode and the *p*-doped MoS_2 region (note that the Ti source (S) electrode and the untreated *n*-type MoS_2 region have been shown to be in a quasi-Ohmic contact) [52, 98]. To evaluate this possibility, I_{DS}-V_{DS} characteristic curves (V_G = 0 V) of FETs blank-treated with various plasmas were measured and plotted in Figure 3.4. Figure 3.4 shows that SF_6, CHF_3, O_2-treated FETs still exhibit a quasi-Ohmic contact property in spite of plasma-induced *p*-doping in MoS_2, which is probably due to the diffusion of metal atoms from electrodes into 2D layers [99, 100]. Therefore, it is safely concluded that the rectifying property of MoS_2 diodes made by using SF_6, CHF_3, O_2 plasma recipes is indeed mainly attributed to the *p-n* junctions formed by the selected-area plasma treatment. However, the CF_4-treated FET shows a

slight Schottky-like contact property. Although such a weak Schottky-like contact is not anticipated to result in a significant current rectification effect [101], we temporarily attribute the rectifying behavior in CF_4-treated diodes to the net effect of a *p-n* junction connected in series with a Schottky-like junction.

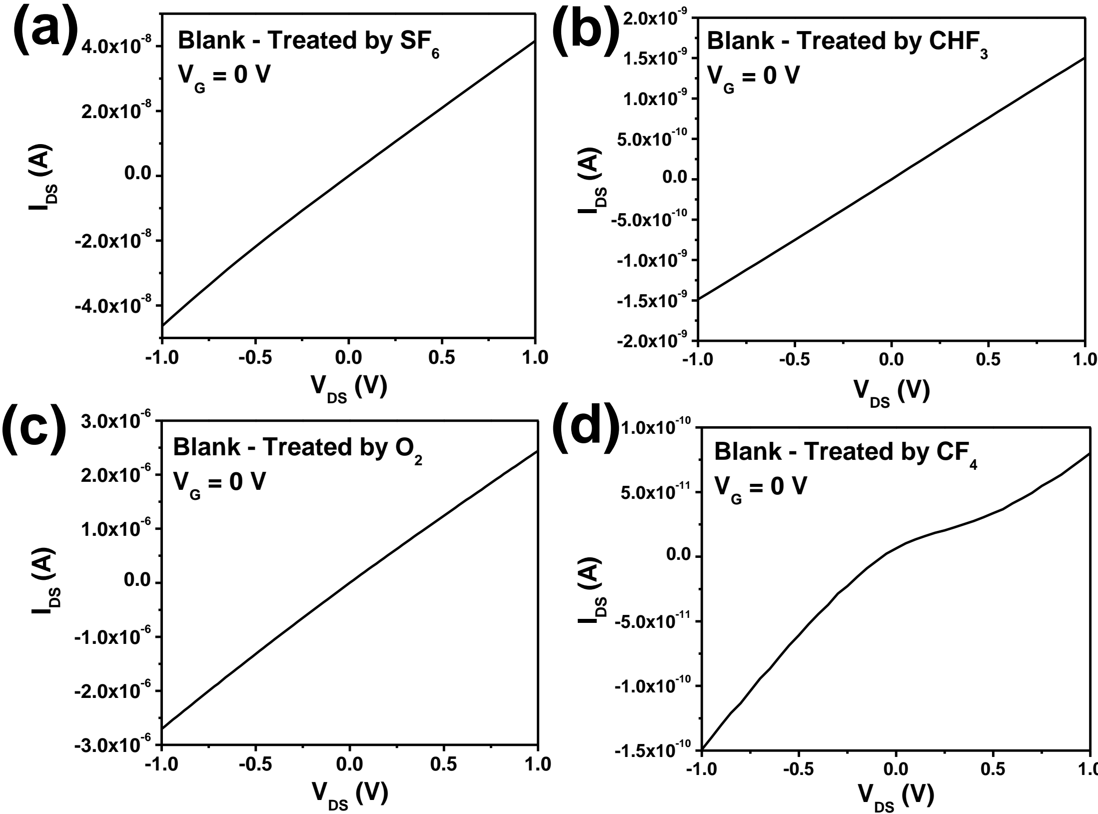


Figure 3.4 I_{DS}-V_{DS} characteristic curves of MoS_2 FETs blank-treated with (a) SF_6, (b) CHF_3, (c) O_2, and (d) CF_4 plasmas. Here, V_G is fixed to 0 V. SF_6, CHF_3, O_2-treated FETs exhibit quasi-Ohmic contacts between Ti electrodes and *p*-doped MoS_2 channels, whereas the CF_4-treated FET shows a slight Schottky-like contact property.

3.3.2 X-ray Photoelectron Spectroscopy (XPS) Surface Analysis of Plasma Treated MoS_2 sample

For additional evidence of plasma-induced *p*-doping in MoS_2, we performed a surface analysis *via* X-ray photoelectron spectroscopy (XPS). Figure 3.5 (a) shows the binding energy peaks of Mo $3d_{5/2}$ and Mo $3d_{3/2}$ electrons in plasma-treated and untreated (pristine) MoS_2 films. In comparison with the Mo $3d_{5/2}$ and Mo $3d_{3/2}$ peaks of the untreated film, the peaks of all plasma-treated films are wider, and their maxima shift toward the lower binding energy values (the relative shift values are labeled in Figure 3.5 (a)). Such a downshift of the peaks is attributed to the *p*-doping process, since it indicates a relative shift of the Fermi level toward the valence band edge [59, 102, 103]. The more negative shift of the elemental electron binding energy means the smaller energy difference between the Fermi level and the valence band edge, and therefore the stronger *p*-doping characteristics. Based on the negative shifts of Mo $3d_{5/2}$ and Mo $3d_{3/2}$ peaks labeled in Figure 3.5 (a), the ranking order of our plasma recipes in terms of their resulted *p*-doping levels is SF_6> CHF_3> CF_4> O_2 that is very similar to the ranking obtained from the FET characterization. Thus, in combination with both diode and FET characterizations, the XPS surface analysis provides a solid verification of the plasma-induced *p*-doping as well as the formation of rectifying *p-n* junctions in MoS_2 films.

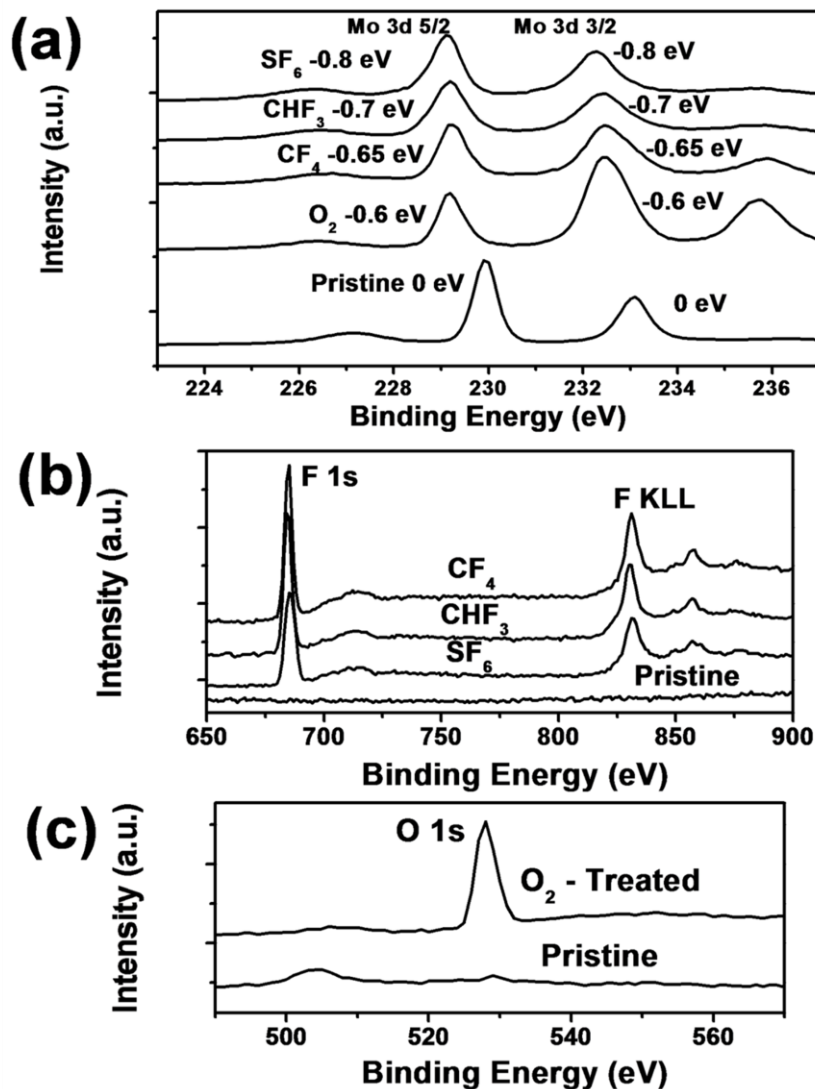


Figure 3.5 XPS surface analysis of plasma-treated and untreated (pristine) MoS_2 flakes with binding energy peaks of (a) Mo $3d_{5/2}$ and Mo $3d_{3/2}$, (b) F 1s and F KLL, (c) O 1s electrons.

Moreover, the XPS surface analysis also provides clues about the specific types of *p*-dopants (or acceptors) introduced by plasma processes. Figures 3.5 (b) and (c) show that the XPS spectra of MoS_2 films treated with F-contained plasmas (*i.e.*, SF_6, CHF_3, and CF_4) and O_2 plasma exhibit prominent binding energy peaks associated with electrons in F (*i.e.*, F 1s and F KLL) and O

(*i.e.*, O 1s) atoms, respectively, and these F and O-related peaks do not appear in the XPS spectra of untreated pristine films. Based on this fact and that only F- and O-contained plasmas can result in diodes with high rectification degrees and FETs with *p*-type transport characteristics, it is strongly suggested that F and O atoms are the critical dopants responsible for the *p*-doping in MoS_2. Yue *et al*. recently performed a first-principle study of the substitutional doping of MoS_2 layers, which shows that the incorporation of F, O, and other typical dopant atoms into MoS_2 layers can induce the surface charge transfer processes between incorporated atoms and MoS_2 layers [97]. Because of the relatively strong electronegativity of F and O atoms, the excess electrons are preferentially transferred from MoS_2 layers onto F and O atoms, resulting in *p*-doping in MoS_2 layers [97]. The excess charge amounts transferred onto F and O dopants were calculated by Yue *et al.* to be 0.675 and 0.903 electron/dopant atom, respectively [97]. This theoretical work also suggests that F and O atoms can be used as effective *p*-type dopants for functionalizing MoS_2 devices, consistent with our experimental work.

3.3.3 Applicability of Plasma-Assisted Doping Technology

To further justify our plasma treatment process as a useful doping approach to create MoS_2-based diodes, ambipolar or *p*-type FETs, we preliminarily evaluated the effect of plasma doping on the transport properties of MoS_2 flakes. Based on the transport characteristics displayed in Figure 3.3, the field-effect electron mobility values of untreated, O_2, CF_4, and CHF_3-treated FETs are extracted to be 68, 15, 37, and 20 cm^2/Vs, respectively. Although the plasma treatment processes can noticeably reduce the electron mobility of few-layer MoS_2 flakes, the resulted mobility values are still high enough for practical electronic applications. Especially, using high-*k* gate dielectrics, the mobility values of these plasma-treated FETs are expected to be improved by at least one order

of magnitude (*i.e.*, comparable to those of doped Si) [4], which is attributed to the dielectric screening effect [104].

Finally, it should be noted that our plasma doping methods are not suitable for functionalizing MoS_2 monolayers, as plasma bombardment can always physically etch the MoS_2 layers. However, in combination with the precise control of the final film thickness, this technique is very useful for electronic and optoelectronic applications based on few-layer or multilayer MoS_2 films, such as complementary electronic circuits, photovoltaic cells, flexible TFTs, and photodetectors, *etc*.

3.4 Summary

In summary, the selected-area plasma treatment of MoS_2 flakes with F- or O-contained plasmas can create diodes with high degree of rectificaion effect. The FET transport characterization in combination with the XPS surface analysis of MoS_2 films blank-treated with plasmas confirms that the rectifying behavior of our MoS_2 diodes is attributed to the plasma-induced *p*-doping into initially *n*-type MoS_2 flakes, which forms stable *p-n* junctions. Such plasma-doped diodes exhibit high forward/reverse current ratios (*e.g.*, ~ 10^4 for SF_6-treated diodes) and a superior long-term stability at ambient conditions. They are suitable for optoelectronic and nanoelectronic applications based on emerging 2D materials. In addition, the presented plasma-assisted doping method could be generally used for creating MoS_2 FETs with ambipolar or hole-dominated *p*-type characteristics as well as functionalizing other emerging layered transition metal dichalcogenides.

Chapter 4

Abnormal Multiple Charge Memory States in Few-Layer WSe_2 Transistors

4.1 Introduction

Although we have presented both new manufacturing and doping methods for TMDC materials in previous chapters, the interface of 2D semiconductor materials has intense charging trapping phenomena comparing to Si materials. To make fully operational TMDC-based FETs for practical applications, we need to obtain an in-depth understanding of the charge-trapping mechanisms in such FETs, because charge-trapping processes significantly affect the reliability, durability, and operation speed of FETs as well as other FET-related devices [64], such as FET biosensors [65, 66, 105, 106], flash memories [67-69, 78, 79], and photo-transistors [29]. In addition, the newly identified charge-trapping schemes in TMDCs and other layered semiconductors could be further investigated and exploited to produce new memory devices with multibit data storage and analog computing capability. In our recent work, we found that an exfoliated few-layer MoS_2 flake, after a plasma doping process, has a rough (or rippled) top layer [30]. When incorporated into a FET structure, this rough layer can serve as a charge-trapping layer interfacing with the underlying pristine layers that serve as the FET channel [30]. This device

structure can function as a FET memory and enable multibit data storage (*i.e.*, year-scale binary or 2-bit data storage; day-scale 3-bit data storage) [30]. This work is anticipated to motivates and inspires further efforts to identify the charge-trapping mechanisms in other relevant TMDCs and leverage the unique electronic and structural properties of such layered semiconductors for emerging cost-efficient data storage application.

In this chapter, we systematically investigate the charge-trapping characteristics of the FETs made from mechanically-exfoliated few-layer WSe_2 flakes. We show that with no need to treat such WSe_2 FETs with plasma species or other energetic particles, we can directly create multiple charge-trapping states in the FETs through applying electrical pulses with different magnitudes. The excited charge-trapping states exhibit relatively large extrema spacing, long retention time, and analog tunability. Such charge-trapping states cannot be generated in pristine few-layer MoS_2 FETs or monolayer WSe_2 FETs, but they are similar to those excited in plasma-doped MoS_2 FETs [30]. A series of surface characterization results of as-exfoliated few-layer WSe_2, as-exfoliated few-layer MoS_2, and plasma-doped few-layer MoS_2 flakes strongly imply that the unique charge-trapping states observed in a few-layer WSe_2 FET could be attributed to exfoliation-induced deformation or twisting in the WSe_2 layers very close to the cleaved surface of a mechanically-exfoliated WSe_2 FET channel. Such deformation features could result in ambipolar charge-trapping sites in such twisted or deformed WSe_2 layers. Our additional results from charge-retention characterization at different temperatures and density functional theory (DFT) computation strongly support this explanation. Finally, this work also demonstrates that the long-lasting charge-trapping states excited in our WSe_2 transistors can be further calibrated into consistent multibit data storage levels for information storage application.

4.2 Methods and Materials

4.2.1 Fabrication of Field-Effect Transistors (FETs) with Mechanically-Exfoliated Few-Layer WSe2 and MoS2 Channels

The few-layer WSe_2 FETs are fabricated by using our mechanical printing method previously reported [55, 105]. WSe_2 channel thicknesses are specifically controlled to be 10-15 nm, aiming to achieve relatively high field-effect mobility and On/Off current ratio [98, 107]. The channel length is 5 μm, and the average channel width ranges from 6 to 10 μm. Ti (5 nm)/Au (50 nm) source-drain (D-S) electrodes are fabricated by using photolithography followed with metal deposition and lift-off in a solvent. The p^+-Si substrates serve as back gates (G). Thermally grown SiO_2 layers (300 nm thick) serve as the gate dielectrics. The process for fabricating few-layer MoS_2 FETs is the same as that for making WSe_2 FETs.

4.2.2 Plasma Doping for Creating Long-Lasting Charge-Trapping States in Few-Layer MoS_2 FETs

The top layers of as-exfoliated few-layer MoS_2 FET channels are doped with O_2 plasma treatment in an inductively coupled plasma-based (ICP) reactive ion etching (RIE) tool. The RF power is fixed to 200 W; the pressure is 10 mTorr; the precursor gas flow rate is 10 sccm; and the processing time for each FET is fixed to 2 min.

4.2.3 Electrical Characterizations of Charge-Trapping States in Few-Layer WSe_2 and MoS_2 FETs

The electrical characterizations of FET devices are performed in a LakeShore™ probe station. The probe station is connected with a HP4145 semiconductor parameter analyzer that can generate gate voltage (V_G) pulses with duration width of 1 s. To characterize the hysteretic behaviors of the transfer characteristics of the FET, drain-source current (I_{DS})-gate voltage (V_G) curves are acquired along two different V_G sweep directions with a constant sweep rate of 10 V/s. To configure the FET into two extrema charge-trapping states, +/-100V V_G pulses (duration Δt: 1 s) are applied to excite the highest/lowest-conductance states in the FET channel. To evaluate the retention characteristics of excited charge-trapping states, time-dependent I_{DS} values (*i.e.*, I_{DS}-t curves) are measured under fixed V_{DS} and V_G (typically $V_G = 0$ and $V_{DS} = 0.05$ V) after the initial setting of the FET with specific V_G pulse signals.

4.2.4 Surface Characterizations of Few-Layer WSe_2 and MoS_2 FET Channels

For surface analysis of few-layer WSe_2 and MoS_2 transistor channels, we perform the lateral force microscopy (LFM, or friction-mode atomic force microscopy (AFM)) characterizations using a XE-70 AFM Park System equipped with an AFM contact tip (PPP-CONTSCR™ from NANOSENSORS). In addition, scanning electron microscopy (SEM) is performed using a Hitachi SU8000 In-line FE-SEM with accelerating voltage of 2 kV. High resolution electron microscopy (HRTEM) images of few-layer WSe_2 and MoS_2 cleaved surfaces are obtained using a JEOL™ 2010F analytical electron microscope with accelerating voltage of 200 kV.

4.2.5 Density Functional Theory (DFT) Computation

Ab initio calculation of the banding energies of charge-trapping states in the twisted WSe_2 bilayer structure is performed using the ABINIT code (Version: 7.8.2). We can use this DFT tool based on pseudopotentials and plane-wave or wavelet bases to calculate the total energies, charge densities, and electronic structures of the 2D crystal systems consisting of multiple electrons and nuclei. Specifically, a unit cell model of the twisted WSe_2 bilayer structure is constructed based on atomic positions, which reflect the relative displacement and rotation between two twisted WSe_2 layers. The crystal potential is calculated based on the input atomic pseudopotentials. In this calculation, we use either an input wave function or simple Gaussians to simulate the initial charge density and screening potential. Afterwards, the plane wave coefficients are iteratively adjusted with a self-consistent algorithm until a sufficient convergence is reached in the energy. The detailed parameters for ABINIT code setup is listed in Appendix C.

4.3 Result and Discussion

4.3.1 Comparison of Retention Characteristics in Few-Layer WSe_2 and MoS_2 FET

A representative back-gated FET with a mechanically-exfoliated few-layer WSe_2 channel is shown in the optical micrograph in Figure 4.1 (a). The WSe_2 channel thickness is ~15 nm, the channel length is 5 μm, and the average channel width is ~9 μm. A pair of Ti (10 nm)/Au (50 nm) electrodes serve as drain (D) and source (S) contacts. The p^+-Si substrate is used as the back gate (G) with a thermally grown SiO_2 surface layer (300 nm thick) as the gate dielectric. Figure 4.1 (b) shows the transfer characteristics (*i.e.*, drain-source current (I_{DS})-gate voltage (V_G) curves) of this WSe_2 FET, which exhibit a typical *p*-type transport behavior. The I_{DS}-V_G curves were acquired

along two different V_G sweep directions with a constant sweep rate of 10 V/s and exhibit a prominent hysteretic behavior. Such hysteresis indicates the existence of charge-trapping states in the FET, which could be attributed to several possible mechanisms, including (i) moisture-induced charge traps [63, 64, 108], (ii) charge traps (*e.g.*, dangling bonds) at the TMDC/dielectric (*i.e.*, WSe_2/SiO_2) interfaces [64], or (iii) fabrication-process-induced defects or other structures in TMDC layers [30].

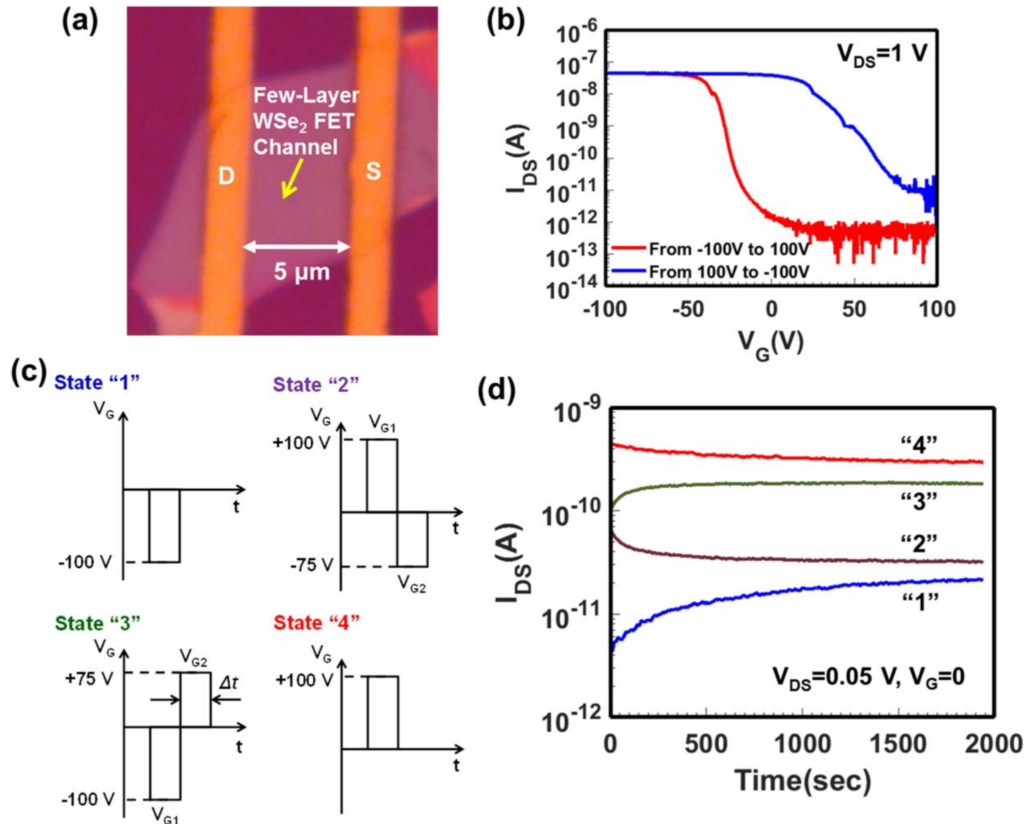
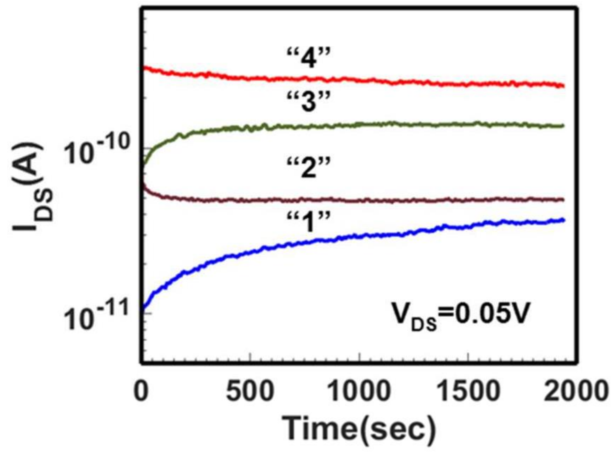


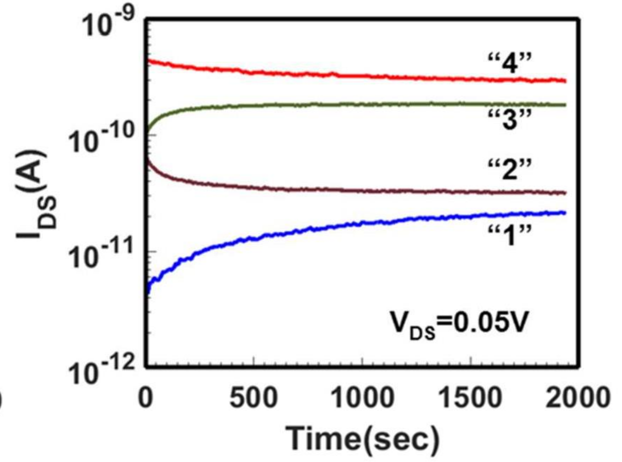
Figure 4.1 Charge-trapping characteristics of a representative back-gated few-layer WSe_2 FET: (a) optical micrograph of the FET consisting of a mechanically exfoliated few-layer WSe_2 channel (thickness: 15 nm, length: 5 μm, average width: ~ 9 μm), a pair of Ti/Au drain/source contacts, a p^+-Si back gate, and a 300 nm SiO_2 back-gate dielectric; (b) transfer characteristic curves (I_{DS}-V_G curves acquired along two different V_G sweep directions with a sweep rate of 10 V/s); (c) the V_G signals

used for setting the FET into four charging states (Δt = 1 s); (d) charge retention characteristics (*i.e.*, I_{DS}-t curves under V_{DS}= 0.05 V and V_G= 0 V) of the FET, which were measured at the four charging states set by the V_G signals illustrated in (c).

For more information about the origin of the charge-trapping behavior observed in the few-layer WSe_2 FETs, we characterized the retention properties of these charge-trapping states. Specifically, to excite a charge-trapping state, a V_G pulse signal with relatively large amplitude is applied to induce the trapping of a specific amount of charged carriers, which shifts the threshold voltage (V_{th}) of the FET and therefore modulates the I_{DS} value measured under given V_G and V_{DS}. After the excitation, the I_{DS} measured under fixed V_G and V_{DS} (here, V_G = 0 and V_{DS} = 0.05 V) is evaluated as a function of elapsed time (t). This I_{DS}-t curve manifests the retention characteristic of a charge-trapping state. Figure 4.1 (c) illustrates the signal profiles of four V_G pulses (referred as to Signals "1" to "4") used for setting the representative FET into four discernible charging states, which are referred as to States "1" to "4", respectively. Figure 4.1 (d) displays the experimentally measured I_{DS}-t curves corresponding to these four charge-trapping states. Here, Signals "1" and "4" are -/+100 V, 1s V_G pulses, which are used for setting the FET into two extreme charge-trapping states with the lowest and the highest channel conductance (or I_{DS} values), respectively. As shown in Figure 4.1 (d), the FET under study exhibits a relatively large initial extrema spacing ~100 (*i.e.*, the ratio between I_{DS} values set at States "4" and "1" is measured to be about 100 at t = 0). Such large extrema spacing allows the excitation of additional intermediate charging states between States "1" and "4" in an analog fashion. Specifically, Signals "2" and "3" plotted in Figure 4.1 (c) are used to set the FET into the intermediate charging states. Signal "2" ("3") is a dual-pulse signal that consists of one +100V (-100V), 1s pulse (V_{G1}) immediately followed with another -75V (+75V), 1s pulse (V_{G2}). Here, the first pulse (V_{G1} = -/+100 V) is used to reset the FET back to the

initial neutral state through releasing any previously trapped charge with the same polarity as that of the to-be-trapped charge, and the second pulse (V_{G2} = +/-75 V) sets the FET into a new intermediate charge-trapping state. As shown in Figure 4.1 (d), all four charge-trapping states excited in the WSe_2 FET exhibit very long retention times and can be well differentiated from each other after several days. Such long retention times imply that the observed charge-trapping states in the WSe_2 FET should not be mainly attributed to moisture-induced charge traps or the charge traps at TMDC/dielectric interfaces, because such traps typically exhibit much shorter retention times (10s to 100s sec) [63, 64]. In addition, we fabricated and characterized another ten FETs based on mechanically-exfoliated few-layer WSe_2. After applied with the same V_G pulses plotted in Figure 4.1 (c), all these ten FETs exhibit very similar charge-trapping states with relatively large extrema spacing, long retention time, and analog tunability. Figure 4.2 specifically lists the retention (or I_{DS}-t) characteristics of the multiple charge-trapping states excited in these FETs. These results confirm that the observed charge-trapping phenomena is a generic characteristic of mechanically-exfoliated few-layer WSe_2 FETs.


"4"
"3"
"2"
"1"
V_{DS}=0.05V
I_{DS}(A)
Time(sec)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V_{DS}=0.05V
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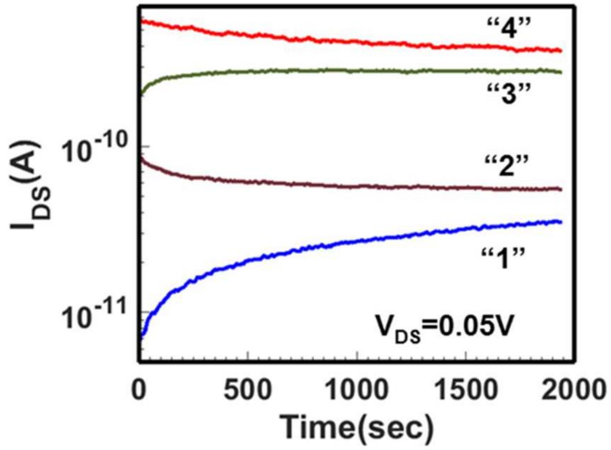
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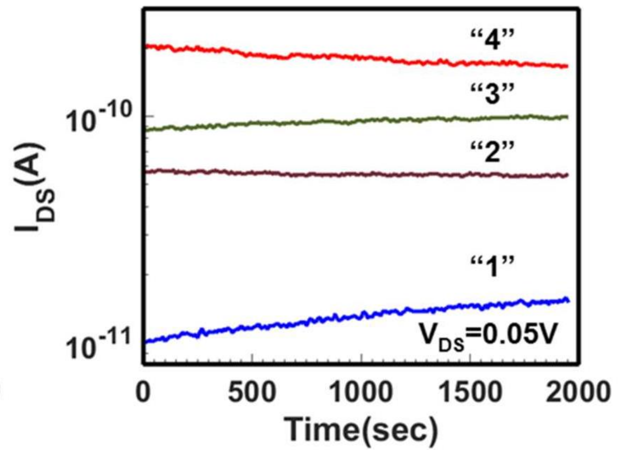
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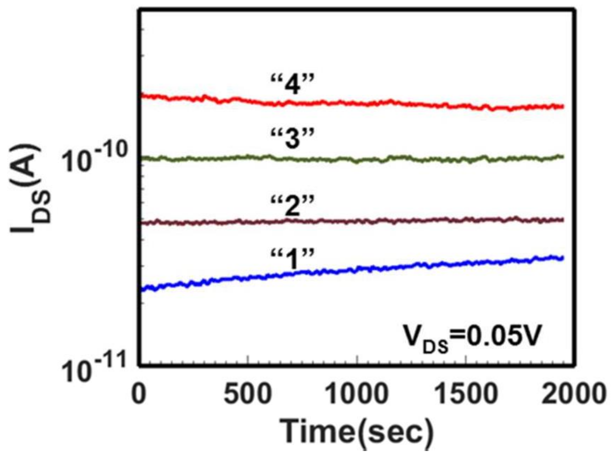
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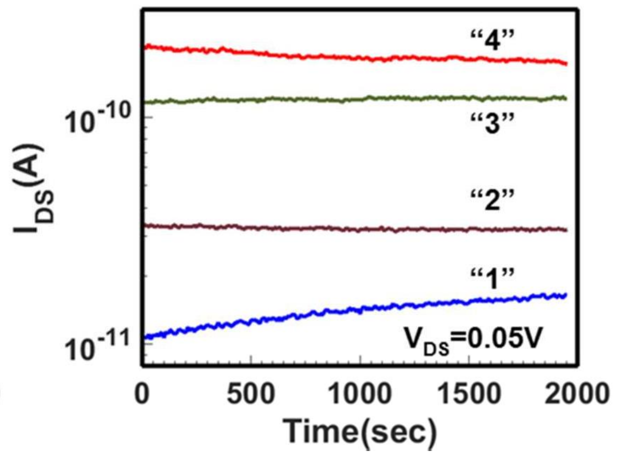
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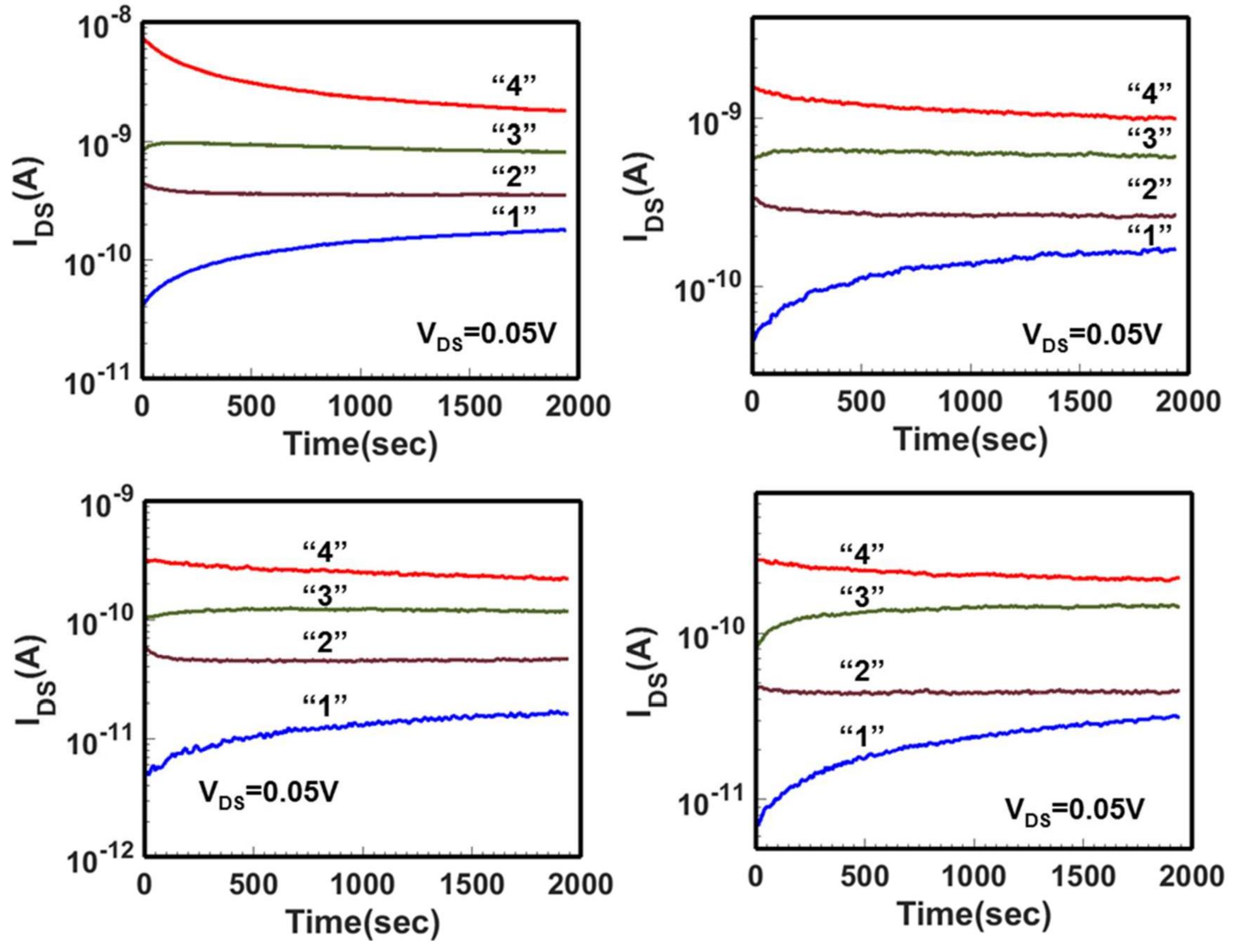


Figure 4.2 Retention characteristic curves (*i.e.*, I_{DS}-t curves) of multiple charge-trapping states (States "1" to "4") measured from ten few-layer WSe_2 FETs. The pulse signals used for setting States "1" to "4" are plotted in Figure 4.1 (c). All few-layer WSe_2 FETs have charge-trapping states with relatively large extrema spacing, long retention times, and analog tunability.

For the further identification of the physics mechanism of the observed charge-trapping states in few-layer WSe_2 FETs, we also fabricated and characterized FETs based on mechanically-exfoliated few-layer MoS_2 flakes, which have similar dimensions as those of the WSe_2 FETs discussed above. Figure 4.3 (a) shows the scanning electron micrograph (SEM) of a representative few-layer MoS_2 FET with channel thickness of ~15 nm, channel length of 5 μm, and average

channel width of ~10 μm. Figure 4.3 (b) shows the transfer characteristics of this FET, which exhibit a *n*-type transport behavior and a relatively mild hysteresis. We further studied the retention characteristics of the charge-trapping states associated with this hysteresis. In particular, Signals “1” and “4” displayed in Figure 4.1 (c) was applied to set the MoS_2 FET into two extreme charge-trapping states with the lowest and the highest I_{DS} values, which are referred as to States “1” and “4”, respectively. Figure 4.3 (c) shows the retention characteristics (*i.e.*, I_{DS}-t curves measured under V_G = 0 and V_{DS} = 0.05 V) of these two charge-trapping states. In comparison with the corresponding charge-trapping states excited in the WSe_2 FET, States “1” and “4” in the MoS_2 FET exhibit much smaller initial extrema spacing (less than 10) and much shorter retention times. The I_{DS} values of these two states quickly relaxed to almost the same value within 1500 s. More quantitatively, the I_{DS}-t retention curves can be fitted with a biexponential equation (Eqn 4.1).

$$I_{DS}(t) = I_0 + I_1 e^{-t/\tau_1} + I_2 e^{-t/\tau_2} \tag{4.1}$$

For States “1” and “4” shown in Figure 4.3 (c), τ_1/τ_2 parameters are fitted to be 694.28s/698.10s and 86.19s/576.88s, respectively. Such relatively short retention times strongly imply that the charge-trapping states observed in the MoS_2 FET are very like due to the charge traps at TMDC/dielectric interfaces or moisture molecules [63, 64]. This result shows that few-layer WSe_2 and few-layer MoS_2 FETs have significantly different charge-trapping characteristics. However, our previous work has shown that plasma-doped few-layer MoS_2 FETs indeed exhibit multiple (or continuously tunable) charge-trapping states with very long retention times, which can be exploited to make multibit memory devices (*i.e.*, binary and 2-bit data levels for year-scale data storage; 3-bit data levels for day-scale storage) [30]. To re-verify this previous result, the MoS_2 FET under study was also treated with O_2 plasma (the details of plasma doping are described in the section of

Methods and Materials). Figure 4.3 (d) displays the I_{DS}-t retention characteristics of four charge-trapping states (States “1” to “4”) excited in this plasma-doped MoS_2 FET by using the V_G pulse signals plotted in Figure 4.1 (c). Consistent with our previous work, this plasma-doped MoS_2 FET have multiple charge-trapping states with a much larger initial extrema spacing (~100) and much longer retention times in comparison with those in the undoped pristine MoS_2 FET [30]. These states are similar to those excited in the few-layer WSe_2 FET (Figure 4.1 (d)). Based on our previous surface characterization works and Kelvin force microscopy (KFM) analysis results, the charge-trapping states observed in a plasma-doped few-layer MoS_2 FET are attributed to the plasma-doping-induced interlayer deformation in the few-layer MoS_2 channel. Specifically, the top layer, when doped with O_2 plasma, is rippled and deformed relative to the underlying intact layers. Such an interlayer deformation forms an ambipolar charge-trapping layer interfacing the underlying MoS_2 channel layers and enables the non-volatile retention of charged carriers as well as the reversible modulation of polarity and amount of the trapped charge [30]. More details on MoS_2 memory transistor will be discussed in Chapter 5. Based on this previous study on plasma-doped MoS_2 memory FETs, we tentatively hypothesize that the long-lasting charge-trapping states newly identified in pristine few-layer WSe_2 FETs are also attributed to process-induced interlayer deformation in few-layer WSe_2 channels. Furthermore, these interlayer deformations could be attributed to the mechanical exfoliation process, as we do not need any plasma doping treatment to form such charge traps in WSe_2 FETs.

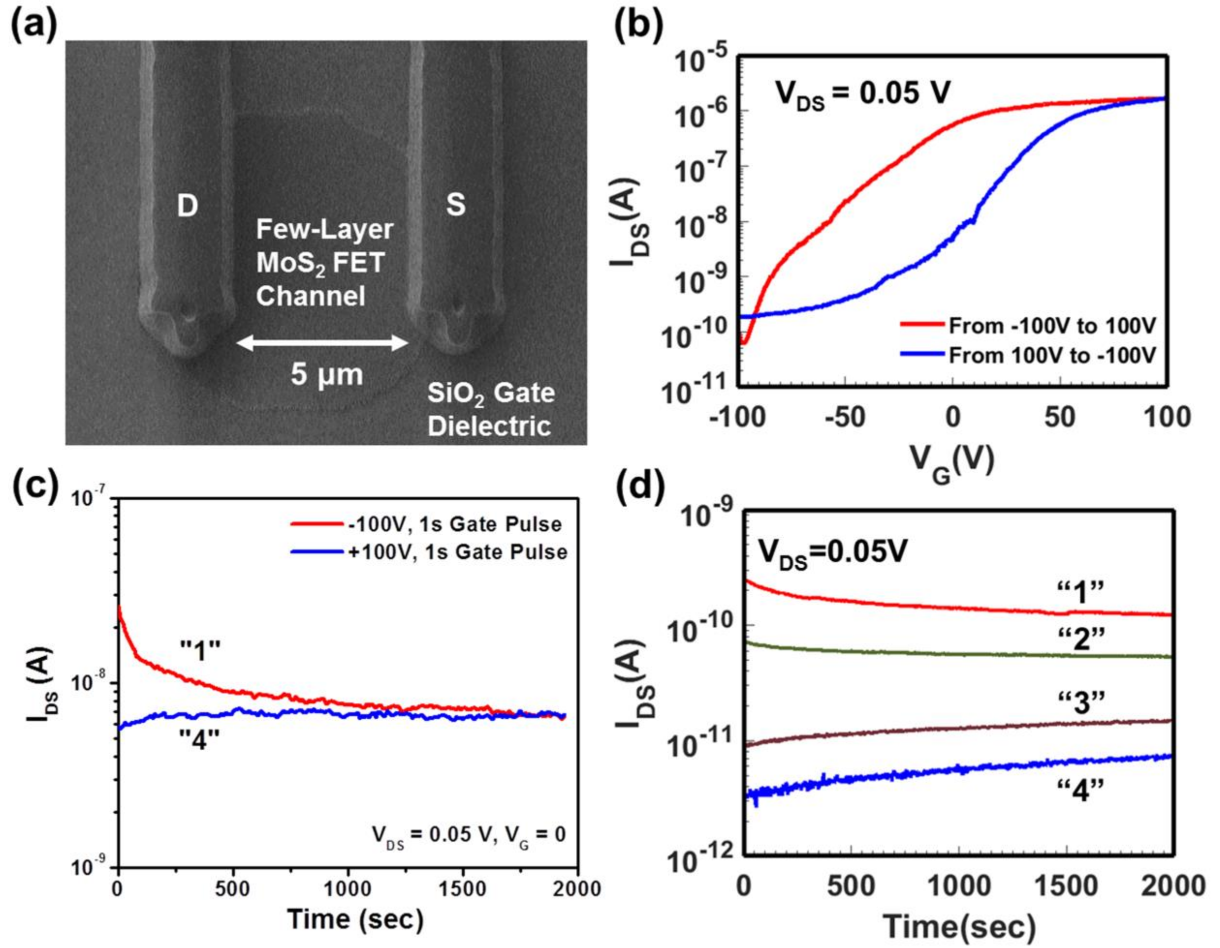


Figure 4.3 Charge-trapping characteristics of a representative back-gated few-layer MoS_2 FET: (a) SEM of the FET consisting of a mechanically exfoliated few-layer MoS_2 channel (thickness: 15 nm, length: 5 µm, average width: ~ 7 µm), a pair of Ti/Au drain/source contacts, a p^+-Si back gate, and a 300 nm SiO_2 back-gate dielectric; (b) transfer curves (I_{DS}-V_G curves acquired along two different V_G sweep directions with a sweep rate of 10 V/s); (c) charge retention characteristics (*i.e.*, I_{DS}-t curves under V_{DS}= 0.05 V and V_G= 0 V) of the FET, which were measured at the two charging states set by the V_G signals (states "1" and "4") illustrated in Figure 4.1 (c); (d) charge retention characteristics of the FET after O_2 plasma doping, which were measured at the four charging states set by the V_G signals illustrated in Figure 4.1 (c).

4.3.2 Hypothesized Model for Long-Lasting Charge-Trapping States in Few-Layer WSe_2

If the proposed hypothesis about the charge-trapping mechanism in few-layer WSe_2 is valid, the observed long-lasting charge-trapping states are then anticipated to be a unique property of few-layer WSe_2 and should not be observed in monolayer structure. To verify this expectation, we also fabricated and characterized monolayer WSe_2 FETs. Figure 4.4 (a) displays the optical micrograph of a representative monolayer WSe_2 FET with channel length of 5 μm and average channel width of ~6 μm. Other structural parameters of such monolayer FETs are the same as those of few-layer FETs. Figure 4.4 (b) shows the I_{DS}-V_G characteristic curves of the monolayer WSe_2 FET, which were acquired along two different V_G sweep directions with a sweep rate of 10 V/s. These I_{DS}-V_G curves exhibit a hysteresis, indicating the existence of charge traps in the FET. Figure 4.4 (c) shows the retention characteristics (*i.e.*, I_{DS}-t curves measured under $V_G = 0$ and $V_{DS} = 0.05$ V) of two extrema charge-trapping states excited by +/-100V, 1s gate pulses. Different from the long-lasting charge-trapping states observed in few-layer WSe_2 FETs, these two extrema states in the monolayer FET exhibit a much smaller initial extrema spacing (less than 10) and much shorter retention times, and they completely merge together in a short elapsed time of ~1700 sec. The absence of long-lasting charge-trapping states in monolayer WSe_2 FETs further confirms that the long-lasting charge-trapping behavior previously observed is indeed a unique characteristic of few-layer (or multilayer) WSe_2 structures.

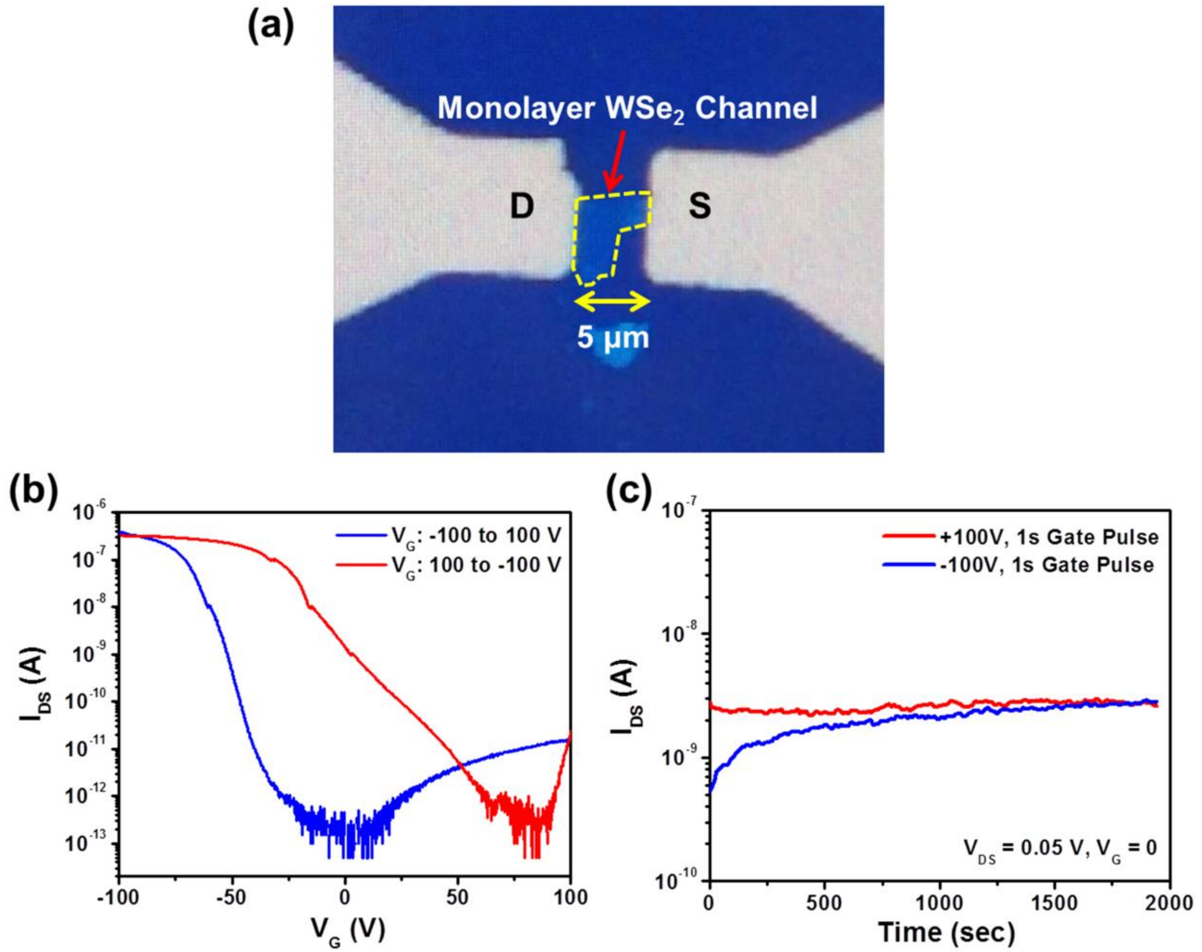


Figure 4.4 Charge-trapping characteristics of a monolayer WSe_2 FET: (a) optical micrograph of a representative monolayer WSe_2 FET; (b) transfer characteristic curves (I_{DS}-V_G curves acquired along two different V_G sweep directions with a sweep rate of 10 V/s); (c) retention characteristics of two charge-trapping states excited by +/-100V, 1s gate pulses.

Based on the electrical characterizations of both plasma-doped few-layer MoS_2 and monolayer WSe_2 FETs, we further sort out the hypothesized origin for the long-lasting charge-trapping states formed in few-layer WSe_2 FETs, as illustrated in Figure 4.5. Figure 4.5 (a) illustrates the previously identified mechanism for explaining the plasma-doping-induced charge-trapping states in MoS_2 FETs. In particular, the as-exfoliated few-layer MoS_2 flake has a flat and

smooth cleaved surface. The subsequent plasma doping process results in the deformation or ripple of the outmost MoS_2 layer on the cleaved surface, which in turn forms gaps between the outmost doped MoS_2 layer and other intact layers [30]. Such gaps serve as the tunneling barriers for effectively retaining the trapped charge, resulting in long charge retention times [30]. Figure 4.5 (b) illustrates the hypothesized mechanism for explaining the charge-trapping states in few-layer WSe_2 FETs. We speculate that a few-layer WSe_2 flake naturally has a rippled or deformed outmost layer on the cleaved surface as it is mechanically exfoliated from the bulk material (or stamp). Such a mechanically-deformed outmost WSe_2 layer is expected to offer similar functionalities to those of the MoS_2 layer with plasma-induced ripple structure, and could serve as an effective long-lasting charge-trapping layer without the need of plasma treatment.

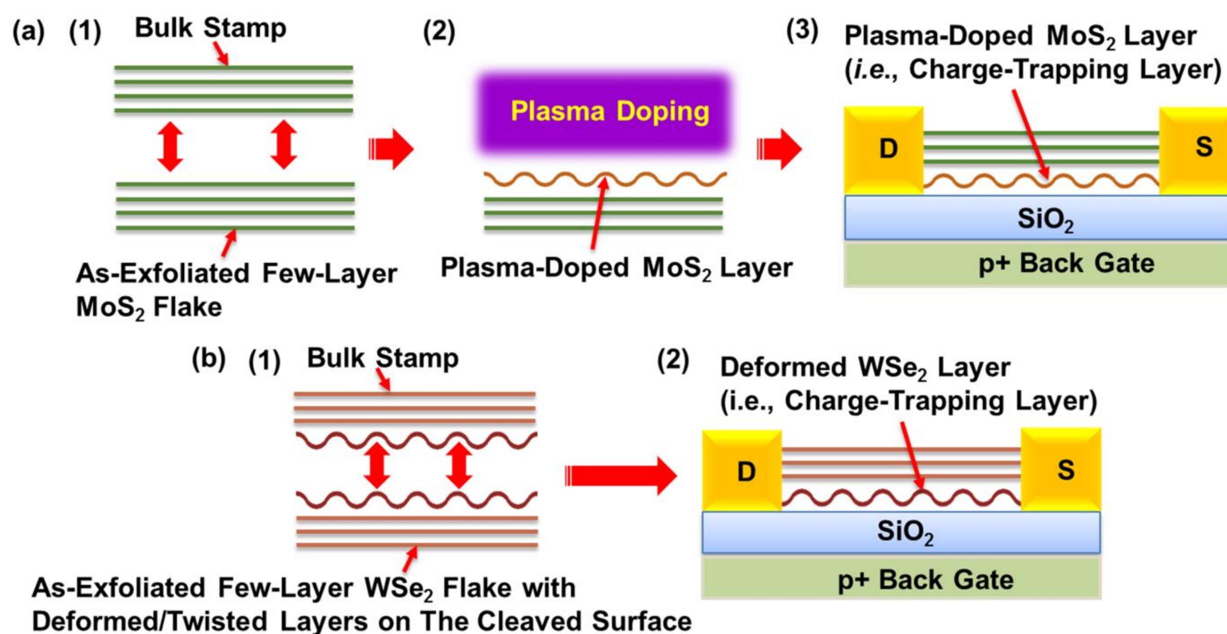


Figure 4.5 Hypothesized models for explaining the observed charge-trapping characteristics of (a) the plasma-doped few-layer MoS_2 FET and (b) the as-exfoliated few-layer WSe_2 FET: When a few-layer MoS_2 flake is cleaved from a bulk stamp, its cleaved surface is expected to be smooth and flat. The subsequent

plasma doping process makes the top MoS_2 layer rough. This rippled layer serves as an effective charge-trapping layer. When a few-layer WSe_2 flake is cleaved, the mechanical exfoliation process is hypothesized to directly result in a rippled cleaved surface. The rippled WSe_2 top layer directly serves as an effective charge-trapping layer with no need of plasma doping.

To further support our hypothesized mechanism, we performed a series of surface characterizations, including atomic force microscopy (AFM), scanning electron microscopy (SEM), and high-resolution transmission electron microscopy (HRTEM), to experimentally verify the existence of exfoliation-induced interlayer deformation in few-layer WSe_2 flakes. Figure 4.6 displays the friction-mode AFM (or lateral force microscopy (LFM)) images of the cleaved surfaces of an as-exfoliated few-layer WSe_2 channel (Figures 4.6 (a) and (b)) and an as-exfoliated few-layer MoS_2 channel (Figures 4.6 (c) and (d)). These LFM images are presented as the spatial functions of the torsional signals (ΔV) directly measured by the AFM cantilever. Here, ΔV is related to the friction force (F_f) between the cantilever and the target surface *via* Eqn 4.2, where S is the cantilever torsional sensitivity and k_t is the cantilever torsional spring constant.

$$F_f = \Delta V \times S \times k_t \tag{4.2}$$

Figure 4.6 shows that the WSe_2 channel surface exhibits a much larger spatial variation of friction force (or coefficient) values in comparison with the MoS_2 channel. This result indicates that the cleaved surfaces of few-layer WSe_2 flakes have a relatively larger topographic fluctuation in comparison with those of few-layer MoS_2 flakes.

Figure 4.7 shows the SEM images of (a) an as-exfoliated few-layer WSe_2 FET channel, (b) an as-exfoliated few-layer MoS_2 channel, and (c) an O_2-plasma-doped few-layer MoS_2 channel. The as-exfoliated MoS_2 channel exhibits an atomically smooth cleaved surface, whereas the as-exfoliated WSe_2 channel, even without being treated with any plasma species or energetic particles,

exhibits a cleaved surface rich of exfoliation-induced ripple structures. This observation is consistent with the AFM result. In addition, Figure 4.7 (c) shows that the plasma-doped MoS_2 channel also has a highly rippled cleaved surface. As discussed above, such rippled cleaved surfaces (or outmost layers) in both as-exfoliated WSe_2 and plasma-doped MoS_2 FET channels are expected to result in the long-lasting charge-trapping states observed in these FETs.

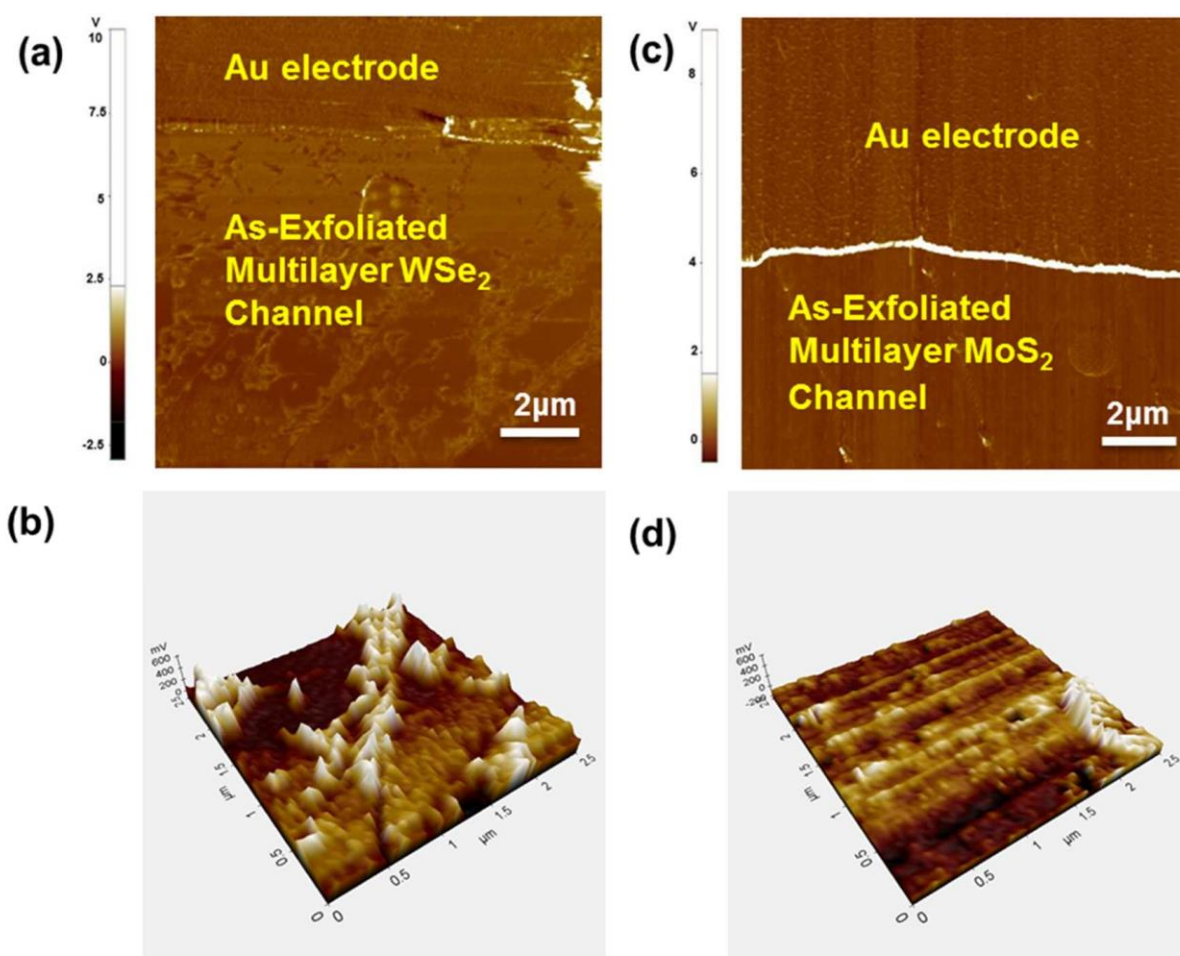


Figure 4.6 Friction-mode AFM images of the cleaved surfaces of an as-exfoliated few-layer WSe_2 flake ((a) top view and (b) tilted view) and an as-exfoliated few-layer MoS_2 flake ((c) top view and (d) tilted view)

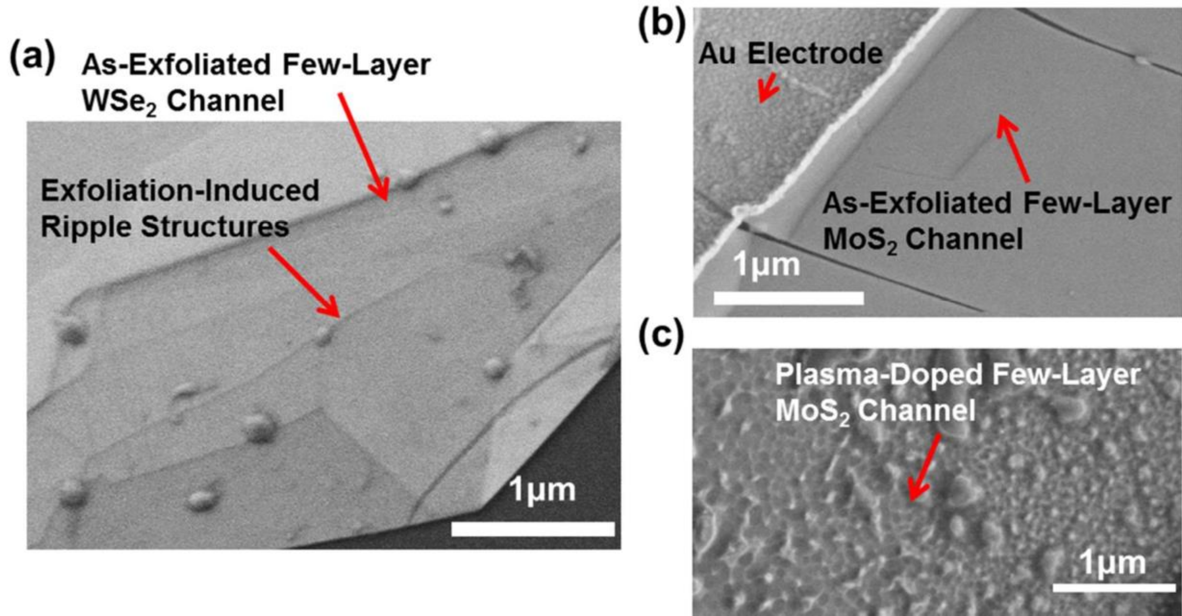


Figure 4.7 SEM images of (a) an as-exfoliated few-layer WSe_2 channel, (b) an as-exfoliated few-layer MoS_2 channel, and (c) an O_2-plasma-doped few-layer MoS_2 channel. The as-exfoliated MoS_2 channel features a smooth and flat cleaved surface, whereas the plasma-doped MoS_2 channel and the as-exfoliated WSe_2 channel feature rough cleaved surfaces with rippled structures.

Based on the AFM and SEM characterizations, we further speculate that the ripple structures observed on the cleaved surfaces of few-layer WSe_2 and plasma-doped MoS_2 flakes could induce relative deformation, displacement, and/or lattice incommensurateness between the outmost TMDC layers and the underlying intact layers, which could be observed in the form of Moiré patterns from the top view of crystal lattice [109-111]. Such Moiré patterns are even expected to exist within the regions without observable ripple features under the AFM/SEM tools, because the lattice incommensurateness effect induced by distant ripple structures could extend to these regions. HRTEM can serve as an effective tool for identifying such Moiré patterns. Figure 4.8 displays the HRTEM images of an as-exfoliated few-layer MoS_2 flake (Figure 4.8 (a)), an O_2-plasma-doped few-layer MoS_2 flake (Figure 4.8 (b)), and a representative as-exfoliated few-layer

WSe_2 flake (Figures 4.8 (c) and (d) are low-magnification and high-magnification views, respectively). As expected based on the SEM characterization, the as-exfoliated MoS_2 flake exhibits a highly crystalline cleaved surface without any Moiré patterns (Figure 4.8 (a)), indicating that the mechanical exfoliation process does not induce observable relative displacement or lattice incommensurateness in the outmost few layers. The plasma-doped MoS_2 flake exhibits an amorphous surface morphology (Figure 4.8 (b)), which represents the crystal damage induced by plasma doping. More strikingly, the cleaved surface of the as-exfoliated WSe_2 flake exhibits quasi-periodic Moiré patterns with periods ranging from 2 to 6 nm, which are superimposed with the highly crystalline lattice of WSe_2 (Figures 4.8 (c) and (d)). The observation of such Moiré patterns further identifies the existence of exfoliation-induced ripple (or other deformation) structures in few-layer WSe_2 flakes, and it also strongly implies that the presence of such ripple structures could result in interlayer displacement or twisting in the regions without visible ripples. As shown in Figure 4.8 (c), there is a spatial variation of orientations and periods in the observed Moiré patterns over the WSe_2 surface, which implies that the lattice incommensurateness effect induced by mechanical exfoliation is not spatially uniform.

The observed differences in the surface morphologies and resulted charge-trapping characteristics between as-exfoliated few-layer WSe_2 and MoS_2 flakes are tentatively attributed to the different mechanical properties of WSe_2 and MoS_2. Specifically, the recent work by Zhang *et al.* shows that the Young's modulus of WSe_2 layers is about two-thirds of those of MoS_2 and other TMDC layers and one-sixth of that of graphene layers [112]. The relatively smaller thickness-independent Young's modulus of WSe_2 layers could make the cleaved WSe_2 layers more compliant to the external exfoliating stresses in comparison with other TMDC layers and result in a high

density of deformation nanostructures, such as ripples and interlayer twists, on the cleaved surfaces [113]. In addition, W and Se atoms are significantly heavier than Mo and S atoms, respectively. Such a large difference in atomic weights could result in other complicated distinctions between WSe_2 and MoS_2 layers. To quantify such anticipated distinctions, additional first-principles calculations will be needed in the future work.

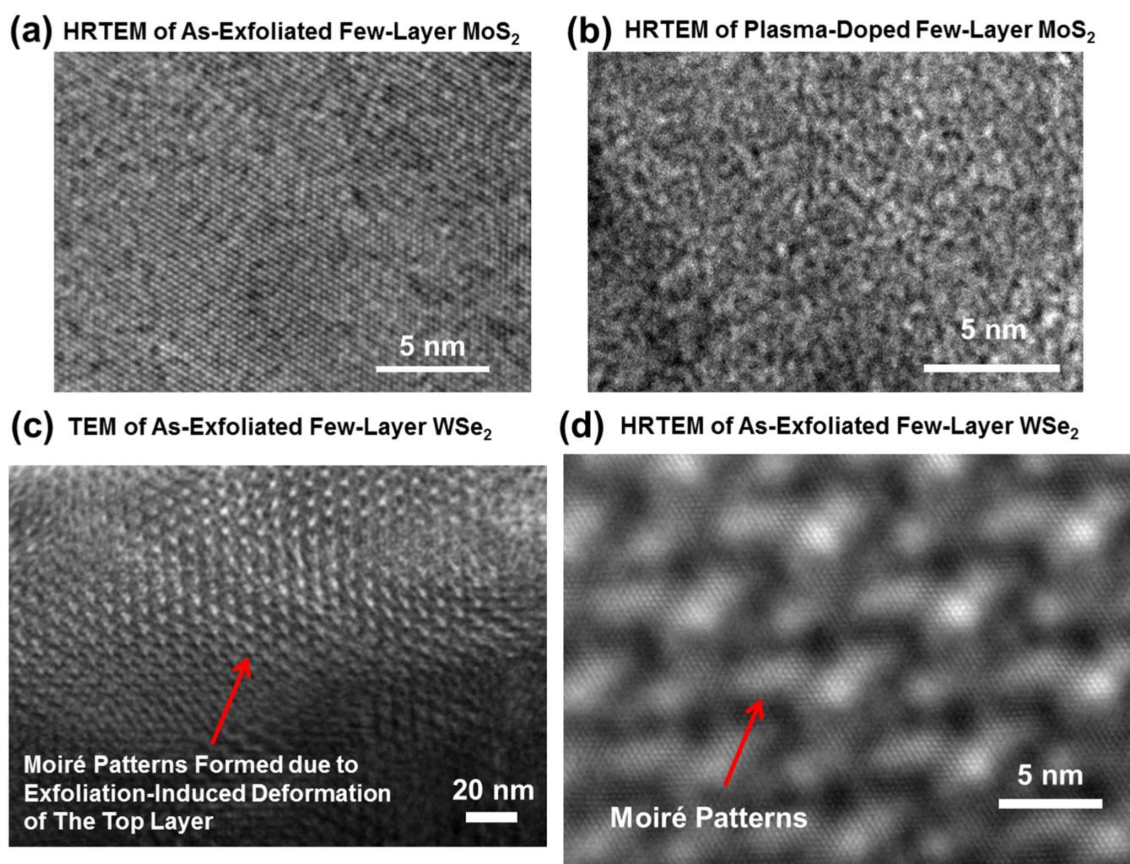


Figure 4.8 HRTEM images of (a) an as-exfoliated few-layer MoS_2 flake, (b) an O_2-plasma-doped few-layer MoS_2 flake, and (c)/(d) an as-exfoliated few-layer WSe_2 flake. The plasma-doped MoS_2 flake exhibits a rough and amorphous surface, which is attributed to the plasma doping. The as-exfoliated WSe_2 flake exhibits quasi-periodic Moiré patterns with periods of 4-6 nm, which is attributed to the exfoliation-induced deformation and displacement of the top WSe_2 layer relative to the underlying layers.

4.3.3 Evaluation of Binding Energy in Charge-Trapping States *via* DFT Computation

Previous works have indicated that such Moiré pattern effect can spatially modulate the interlayer coupling of conduction/valence band states originated from different layers and hence the electronic structures at 2D interfaces, leading to spatial trapping of electrons/holes and spatial variation of electrostatic potential [109-111]. For example, Kang *et al.*'s density functional theory (DFT) work indicates that the Moiré pattern formed at a $MoS_2/MoSe_2$ heterojunction with lattice incommensurateness can result in strong localization of valence band maximum (VBM) states with binding energies larger than 200 meV due to the spatial variation of the interlayer coupling of V_2 states (*i.e.*, Γ point) from both layers as well as localization of conduction band minimum (CBM) states due to the Moiré pattern-induced lateral electrostatic potential with binding energies ~100 meV [109].

Since the translational displacement between two WSe_2 layers with the identical lattice period cannot form a Moiré pattern, the observed Moiré patterns in our few-layer WSe_2 samples are presumably attributed to the interlayer twist induced by the mechanical exfoliation process. The interlayer twist angle (θ) and the resulted Moiré pattern period (P) are correlated by $P = a/\theta$, where a is the in-plane lattice constant (for WSe_2, $a = 0.3297$ nm). The Moiré pattern periods observed in our WSe_2 samples range from 2 to 6 nm, upon which the corresponding interlayer twist angles are estimated to be 3°-10°. Currently, our team lacks a sophisticated tool capable of completely computing the band structures of the electronic Moiré patterns formed in twisted few-layer WSe_2 flakes and precisely evaluating the resulted charge-trapping states. Here, we only use a twisted WSe_2 bilayer structure as the model to provide a first-order estimation of the binding energies of the charge-trapping states associated with the observed Moiré patterns. Figure 4.9 (a) illustrates the

top-view Moiré pattern formed in the twisted bilayer structure. There are various stacking regions within a Moiré pattern period, among which the Bernal (AB) stacking region (denoted as AB) and the direct (AA) stacking region (denoted as AA) are the most representative for characterizing the electronic Moiré structures, as illustrated in Figure 4.9 (b) [109]. Using a DFT tool, we computed the local band structures of AB and AA stacking regions at a twist angle of 5°. More details about this DFT computation are described in the Section 4.2.5 and Appendix C. Figure 4.9 (c) displays the computed band structures of these two representative stacking regions. In particular, Figure 4.9 (c) only shows the *E(k)* branches associated with valence-band-maximum (VBM) and conduction-band-minimum (CBM) states, because they are the primary bands determining the electronic properties of a twisted bilayer structure. This DFT result indicates that the VBM energy of a twisted WSe_2 bilayer structure prominently varies within a Moiré pattern period (fluctuation ΔE_V ~ 0.2 eV). Such a fluctuation of VBM energy can very likely result in charge-trapping sites with a binding energy ~ 0.2 eV. The CBM energy exhibits a relatively smaller fluctuation of 0.04 eV within the Moiré pattern. Therefore, this DFT result implies that the binding energy for holes is larger than for the one for electrons in the long-lasting charge traps in twisted few-layer WSe_2 structures.

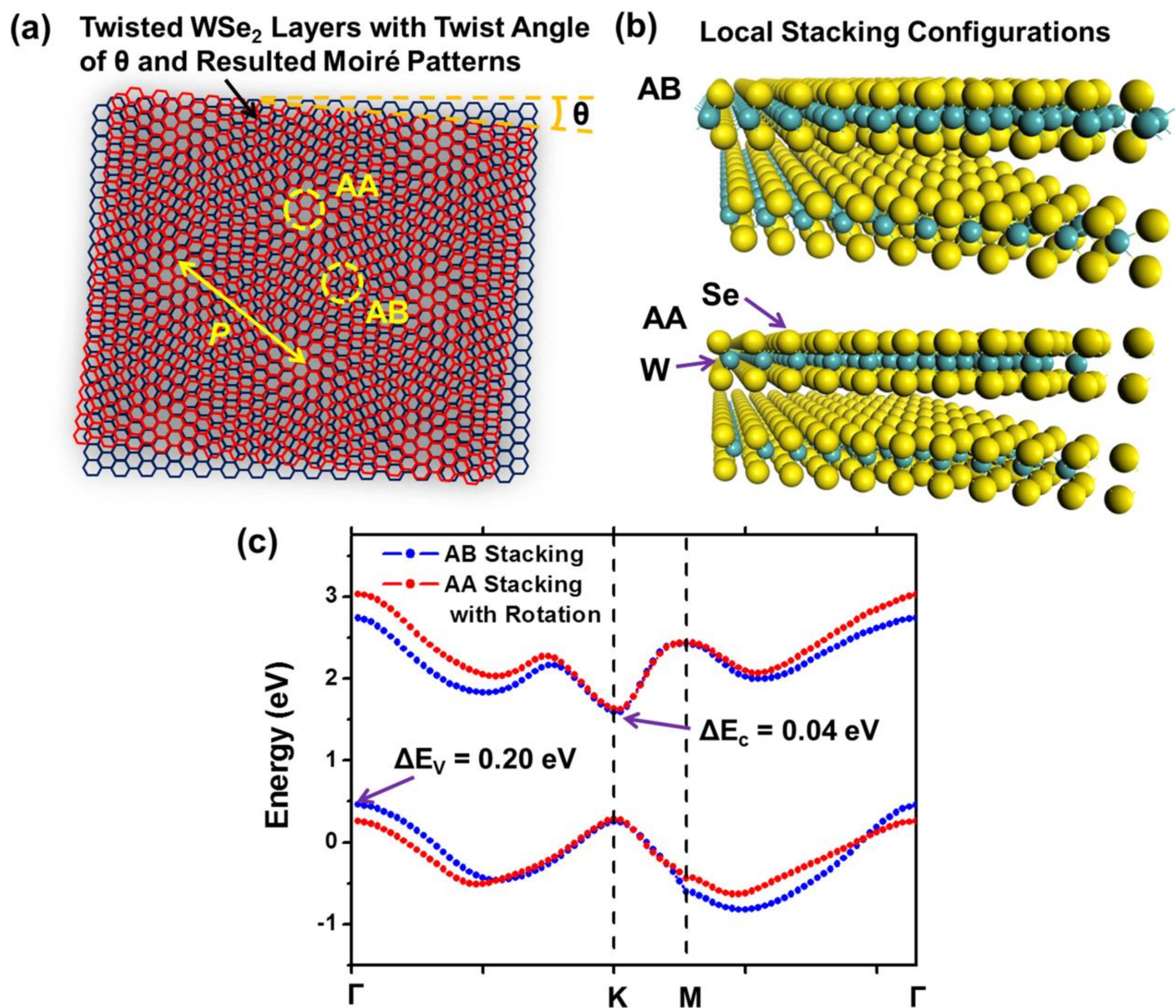


Figure 4.9 DFT computation for estimating the binding energies of charge-trapping states in few-layer WSe_2 FETs: (a) illustration of the Moiré patterns observed in a twisted WSe_2 bilayer structure; (b) illustrations of two representative local stacking configurations (*i.e.*, regions of Bernal (AB) stacking and direct (AA) stacking with an interlayer rotation (θ = 5°)); and (c) computed band structures of these two representative stacking regions. Here, only the *E(k)* branches associated with VBM and CBM states are plotted, because they are the primary bands determining the electronic properties of a twisted bilayer structure.

4.3.4 Evaluation of Binding Energy in Charge-Trapping States *via* Temperature-Dependent Retention Characteristics

To experimentally evaluate the binding energies of long-lasting charge traps in few-layer WSe_2 FETs, we further measured the retention characteristics of charge-trapping States "1" and "4" excited in a WSe_2 FET under different ambient temperatures (T). Figure 4.10 displays the temperature-dependent retention characteristics (*i.e.*, I_{DS}-t curves) of States "1" (*i.e.*, hole-trapping state) and "4" (*i.e.*, electron-trapping state) excited in a few-layer WSe_2 FET by using -/+100 V, 1s V_G pulses. Figures 4.10 (a)-(d) show the I_{DS}-t curves measured at T = 25, 50, 75, and 100 ºC, respectively. The dashed lines in Figures 4.10 (a)-(d) denote the I_{DS} levels associated with the neutral (or permanently stable) states of this WSe_2 FET at different temperatures. Figure 4.10 shows that the discharging-induced relaxation of a charge-trapping state to the neutral state becomes faster at the higher temperature. The trapping time is defined as the time duration measured since the excitation of a charge-trapping state until the complete relaxation of this state to the neutral point. As demonstrated in Figure 4.10, in our experiments, the trapping time of a charge-trapping state is either directly measured at the intersection between its I_{DS}-t curve and the I_{DS} level of the neutral state, or approximately estimated at the intersection between the linear extension of its I_{DS}-t curve in the logarithmic scale and the neutral I_{DS} level. Figure 4.11 shows the Arrhenius plot of measured (or estimated) trapping times (t) of charge-trapping States "1" (*i.e.*, hole-trapping state) and "4" (*i.e.*, electron-trapping state) versus $1/T$. The t data measured at T = 50-100 ºC (or T = 323-373 K) can be well fitted with the Arrhenius equation (Eqn 4.3), in which k_B is Boltzmann's constant, T is the absolute temperature, and E_B is the binding energy of trapped carriers.

$$t \propto e^{\frac{E_B}{k_B T}} \tag{4.3}$$

By this fitting, the binding energies of electrons (E_{Be}) and holes (E_{Bh}) are estimated to be ~0.4 and ~0.7 eV, respectively. Partially consistent with the DFT computation result, this experimental result also shows that in a few-layer WSe_2 FET channel, the binding energy of hole-trapping states is larger than that of electron-trapping states. Our experimentally measured binding energies are noticeably larger than the DFT-calculated ones. This is probably because of that there might be other process-induced deformation features in few-layer WSe_2 flakes, which we have not identified yet, and such features might result in charge traps with the larger binding energies in comparison with in-plane interlayer twists. Finally, it is noted that for both electron- and hole-trapping states, the trapping times measured at T = 25 ^oC (or the room temperature) prominently deviate from the corresponding Arrhenius functions. This could be attributed to the existence of metastable charge-trapping states between charge-trapping State "1" (or "4") and the neutral state, which could effectively retard the discharging process at the room temperature.

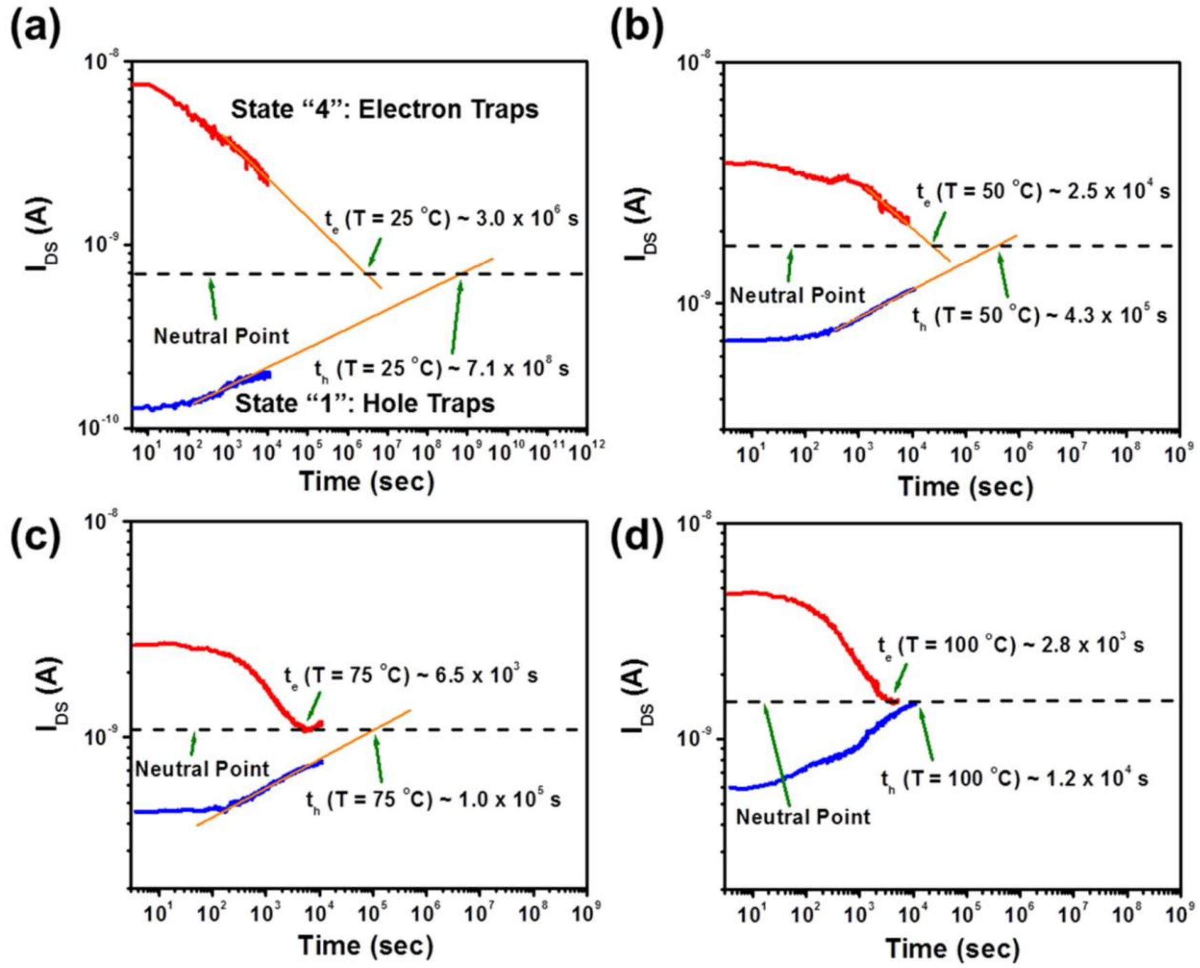


Figure 4.10 Temperature-dependent retention characteristics (*i.e.*, I_{DS}-t curves measured at $V_G = 0$ and $V_{DS} = 0.05$ V) of States "1" (*i.e.*, hole-trapping state) and "4" (*i.e.*, electron-trapping state) excited in a few-layer WSe_2 FET by using -/+100 V, 1s V_G pulses. The charge retention tests were performed at different ambient temperatures, including T = 25, 50, 75, and 100 ^{o}C. The dashed lines denote the neutral (or permanently stable) states of the WSe_2 FET at the different temperatures.

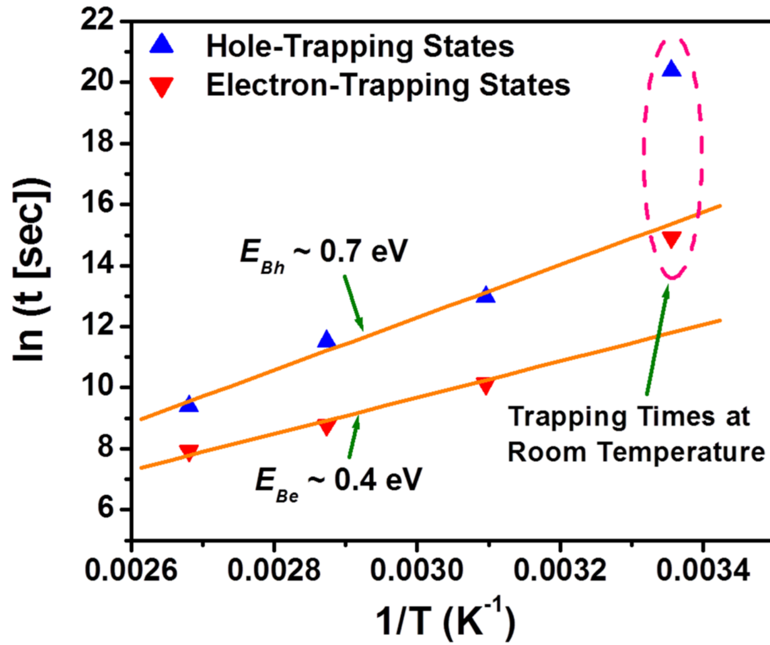


Figure 4.11 Trapping times (*t*) extracted from temperature-dependent retention characteristics of charge-trapping States "1" (*i.e.*, hole-trapping state) and "4" (*i.e.*, electron-trapping state) in a few-layer WSe_2 FET, which are plotted as a function of temperatures.

4.3.5 Metastable Charge-Trapping States in Few-Layer WSe_2

As shown in Figure 4.7 and Figure 4.8, the surface characterization results exhibit very different surface morphologies in as-exfoliated WSe_2 FETs and plasma-doped MoS_2 FETs, although both types of the FETs have similar long-lasting charge-trapping states. This has motivated us to further analyze the fine difference between these two types of the FETs in their charge-trapping characteristics. As shown in Figure 4.1 (d) and Figure 4.2, the four charge-trapping states excited in any of our WSe_2 FETs exhibit a different relaxation (or discharging) behavior in comparison with those excited in plasma-doped MoS_2 FETs (*e.g.*, those shown in Figure 4.3 (d)).

Specifically, for a MoS_2 FET, there is a single neutral (or permanently stable) state between two intermediate charge-trapping states (*i.e.*, States “2” and “3”). The charge-trapping states with initial I_{DS} values higher than the I_{DS} of this neutral state exhibit a slow I_{DS}-reduced relaxation behavior, whereas the states with initial I_{DS} values lower than this neutral state exhibit a slow I_{DS}-enhanced relaxation behavior. However, for a WSe_2 FET, four excited charge-trapping states indicate the existence of at least two metastable states, one of which is between States “1” and “2”, and the other is between States “3” and “4”. Such a difference in the relaxation behaviors is attributed to the difference between as-exfoliated WSe_2 flakes and plasma-doped MoS_2 flakes in their surface morphologies, as manifested in Figure 4.7 and Figure 4.8. The existence of metastable charge-trapping states in few-layer WSe_2 FETs could be further investigated and exploited to enable multibit data storage applications. To fully understand the formation of such metastable charge-trapping states, additional DFT works are needed in the future research.

Additionally, we have demonstrated that the charge-trapping states excited in WSe_2 FETs could be modulated by not only gate pulses but also drain-source (D-S) pulses. Figure 4.12 shows the characterization of the charge-trapping states modulated by D-S pulses. In this experiment, a few-layer WSe_2 FET was firstly set to the highest-conductance metastable charge-trapping state by a +100V, 1s gate pulse. Afterwards, a set of four D-S pulses were applied to set the FET into four different charge-trapping states with sequentially decreased initial I_{DS} values, which are referred as to States “1” to “4” here. These four D-S pulses are +0.5V, +0.062μA, 1s (State “1”); -0.5V, -0.32μA, 1s (State “2”); +2V, +0.19μA, 1s (State “3”); -2V, -1.4μA, 1s (State “4”), which are sketched in terms of their power levels in Figure 4.12 (a). Before being applied with each D-S pulse, the FET was set back to the highest-conductance metastable charge-trapping state that is

denoted by the orange bar in Figure 4.12 (b). The corresponding retention characteristics (*i.e.*, I_{DS}-t characteristic curves measured under V_{DS} = 0.05 V and V_G = 0 V) of these four charge-trapping states were recorded and plotted in Figure 4.12 (b). Here, it should be noted that the power levels of the V_{DS} signals applied for characterizing the charge retention characteristics (*i.e.*, 0.05-1.5 nW) are much lower than those of the D-S pulses for modulating the charge-trapping states (0.03-3 μW). Therefore, the I_{DS}-t characterization is not expected to prominently affect the present charge-trapping state. This experiment shows that D-S pulses in combination with gate pulses can indeed be used to modulate the charge-trapping states in few-layer WSe_2 FETs. More importantly, all these charge-trapping states exhibit an I_{DS}-reduced relaxation behavior and gradually relax further away from the highest-conductance metastable state. This observation further indicates the existence of additional metastable charge-trapping states below the highest-conductance metastable state in a few-layer WSe_2 FET. To further verify this fact, we performed the similar test on another WSe_2 FET that was initially set to the lowest-conductance metastable charge-trapping state by a -100V, 1s gate pulse. A set of three D-S pulses (*i.e.*, +0.35V, 10nA, 1s (State "1"); +1.5V, 70nA, 1s (State "2"); +2.0V, 280nA, 1s (State ""3)), as sketched in terms of their power levels in Figure 4.12 (c), were used to excite three different charge-trapping states (*i.e.*, States "1" to "3") in the FET, and the retention characteristics of these states were measured and plotted in Figure 4.12 (d). All these three states exhibit an I_{DS}-increased relaxation behavior and relax further away from the initial lowest-conductance metastable state (denoted by the violet bar in Figure 4.12 (d)). This test indicates the existence of additional metastable charge-trapping states above the lowest-conductance metastable state in a few-layer WSe_2 FET. As analyzed in our previous work about plasma-doped MoS_2 FET memories, the gate-pulse-mediated switching among different charge-

trapping states in such few-layer-TMDC FETs could be attributed to the gate-voltage-mediated tunneling across the energy barriers between the charge-trapping layers and the transporting channel [30]. This observed D/S-pulse modulation of charge-trapping states are presumably resulted from the hot carrier injection into the charge-trapping sites in the WSe_2 layers.

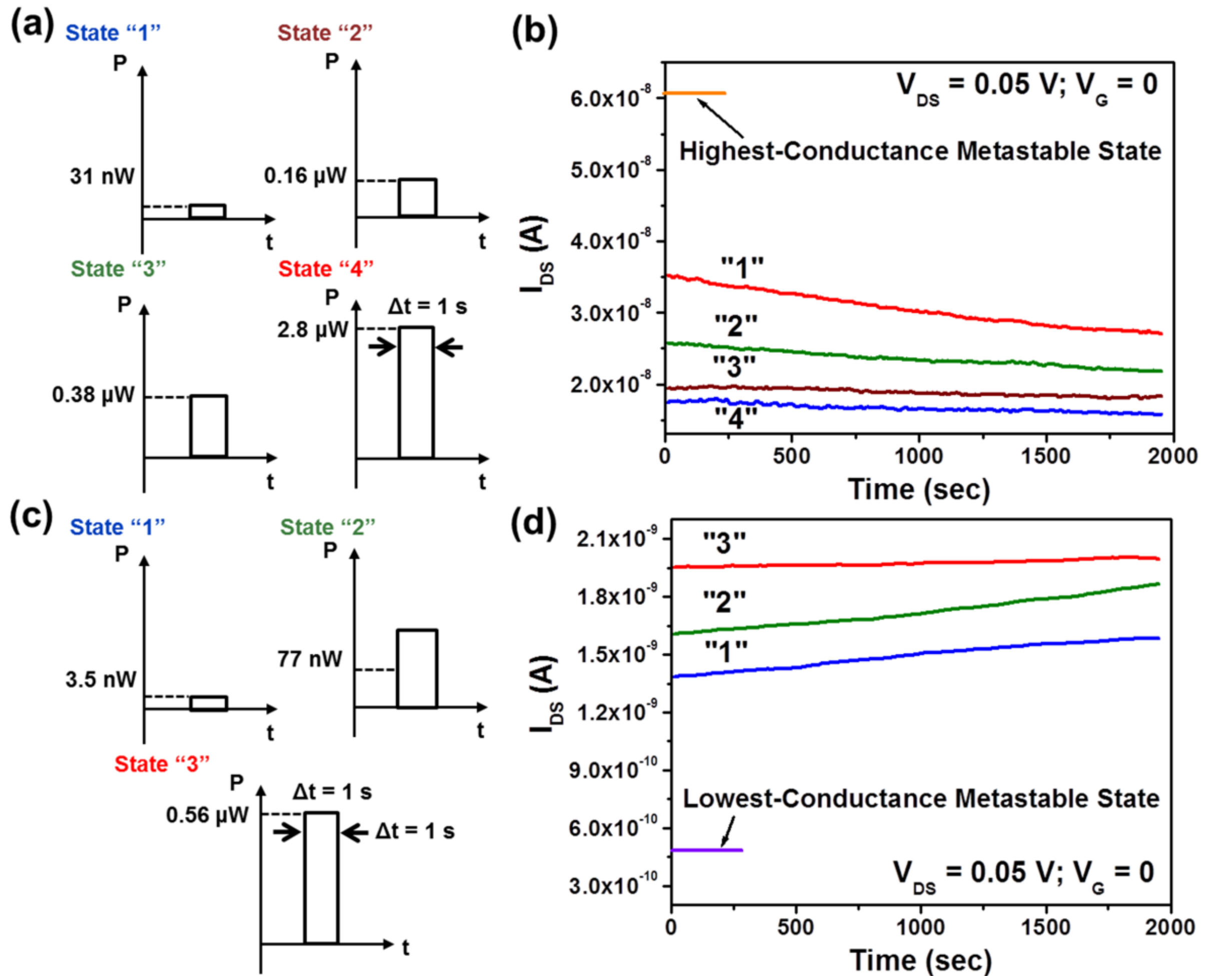


Figure 4.12 Charge-trapping states excited in few-layer WSe_2 FETs using drain-source (D-S) pulses: a set of four D-S pulses, as sketched in (a), were used to excite four charge-trapping states in a WSe_2 FET, and the retention characteristics (*i.e.*, I_{DS}-t characteristics) of these states were measured and plotted in (b). Before being set into each state, the FET was set back to the highest-conductance metastable

charge-trapping state, as indicated by the orange bar. Another set of three D-S pulses, as sketched in (c), were used to excite three charge-trapping states in another WSe_2 FET, and the retention characteristics of these states were measured and plotted in (d). Before being set into each state, the FET was set back to the lowest-conductance metastable charge-trapping state, as denoted by the violet bar.

4.3.6 Multibit Memory Application for Few-Layer WSe_2 FET

The charge-trapping states formed in mechanically exfoliated few-layer WSe_2 flakes could be further studied and exploited for multibit memory solution with high cost efficiency. One of the expected challenges for making such memories is that the exfoliation-induced deformation structures as well as Moiré patterns at cleaved WSe_2 surfaces exhibit a high degree of disorder and are expected to result in a large device-to-device variation in the physical parameters associated with the charge-trapping states designated to specific data levels. To minimize such a variation, we attempt to calibrate the I_{DS} values associated with different charge-trapping states and obtain calibrated data levels (S_n) using Eqn 4.4.

$$S_n = \frac{\log(I_n(t)/I_1(0))}{\log(I_4(t)/I_1(0))} \tag{4.4}$$

In Eqn 4.3, $I_n(t)$ is the I_{DS} value of the nth charge-trapping state at elapsed time of t, and the indexing for n is consistent with that used in Figure 4.1 and Figure 4.2. $I_1(0)$ and $I_4(0)$ are the initial I_{DS} values of States 1 and 4 (*i.e.,* the lowest and highest-conductance states set by -/+100V, 1s gate pulses), respectively. Figure 4.13 (a) shows the retention characteristics of four calibrated data levels measured from a representative WSe_2 FET. These four data levels are calibrated from charge-trapping states “1” - “4” and can be directly referred as to S_1, S_2, S_3, S_4, respectively, or S_{00}, S_{01}, S_{10}, S_{11} for representing 2-bit data storage states. Figure 4.13 (b) exhibits a column chart showing the calibrated 2-bit data levels measured from six WSe_2 FETs that were fabricated in the

same batch. Here, the heights of columns represent the relaxation ranges of corresponding calibrated data levels within 2000 sec, and the arrows indicate the relaxation directions of calibrated data levels (or corresponding I_{DS} values). Figure 4.11 displays the detailed retention characteristic curves (*i.e.*, S_n-t curves) of these six FETs. Figure 4.13 (b) preliminarily demonstrates that multiple WSe_2 FETs exhibit a good device-to-device consistency in calibrated 2-bit data levels. Our experiments indicate that these 2-bit data levels remain to be discernible within day-scale elapsed times. Because of the existence of metastable charge-trapping states (one is between S_{00} and S_{01} levels, and the other is between S_{10} and S_{11} levels), the resulted binary data storage states are expected to be nonvolatile and have a high device-to-device consistency. Furthermore, we also performed a cycling endurance test on a representative FET. Specifically, during each endurance characterization cycle, the FET was sequentially programmed into "1" to "4" (or "S_{00}" to "S_{11}") states by using the corresponding V_G signals illustrated in Figure 1 (c). The FET underwent 100 sequential endurance test cycles. Figure 4.14 displays the initial I_{DS} data (recorded at V_{DS}=0.05 V, V_G= 0 V) measured at all test cycles. Such cycling endurance test data indicates a repeatable 2-bit memory storage capability in the few-layer WSe_2 FET.

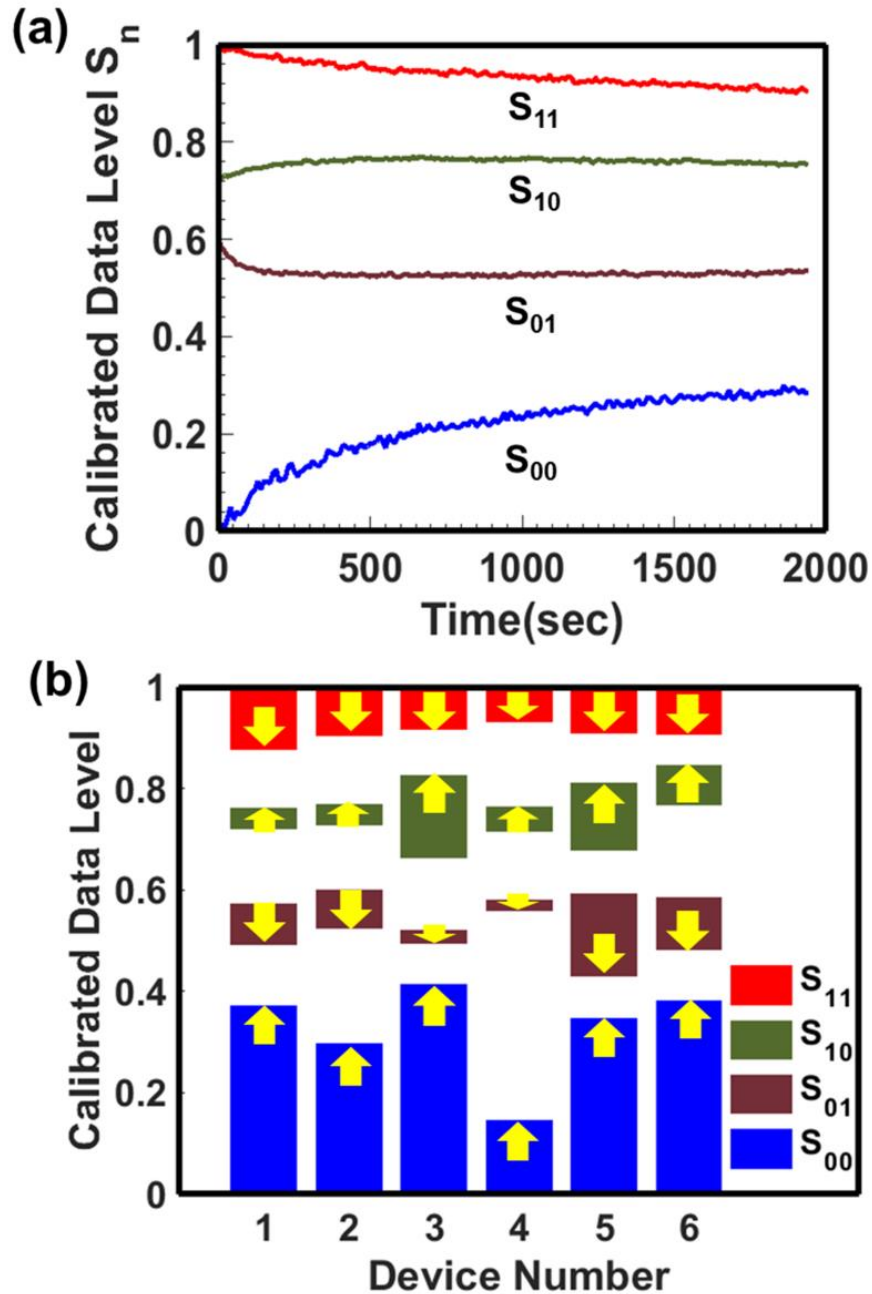


Figure 4.13 Preliminary evaluation of the applicability of mechanically exfoliated few-layer WSe_2 FETs for data storage applications: (a) retention characteristics of four calibrated data levels (or 2-bit memory states) programmed in a representatively few-layer WSe_2 FET; (b) calibrated data levels measured from six WSe_2 FETs fabricated in the same batch. Here, the heights of columns represent the relaxation ranges of corresponding calibrated data levels, and the arrows indicate the relaxation directions of calibrated data levels (or corresponding I_{DS} values).

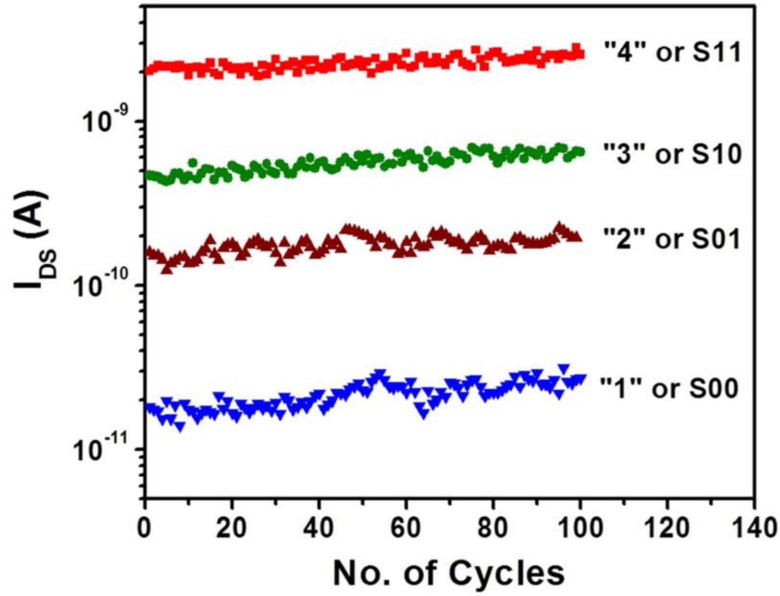


Figure 4.14. Cycling endurance test of a representative FET: *i.e.*, Multiple charge-trapping states or data levels (*i.e.*, the initial I_{DS} data measured at V_{DS}= 0.05 V, V_G= 0 V after the excitations by respective V_G signals illustrated in Fig. 1 (c)) recorded for 100 sequential endurance test cycles (for each endurance characterization cycle, the FET is sequentially programmed into "1" to "4" (or "S00" to "S11") states, demonstrating a repeatable 2-bit memory capability).

Finally, we investigated the effects of different excitation signal durations on the charge-retention characteristics of WSe_2 FETs. Specifically, Figure 4.15 (a) displays a set of hysteretic transfer curves of a representative WSe_2 FET, which were acquired at different V_G sweep rates (3, 17, 83, 165 V/s). These curves indicate that the increase of V_G sweep rate from 3 to 165 V/s only causes a very slight reduction of the hysteresis window (*i.e.,* from 60 to 56 V). In addition, Figure 4.15 (b) shows the retention characteristics (*i.e., I_{DS}–t* curves) of charge-trapping states "1" and "4" in the FET, which were excited by ±100 V_G pulses with different durations (0.01, 0.1, and 1 s). Such retention test results show that the V_G pulses with durations in the range of 10 ms to 1 s result in very similar charge-retention characteristics for WSe_2 FETs.

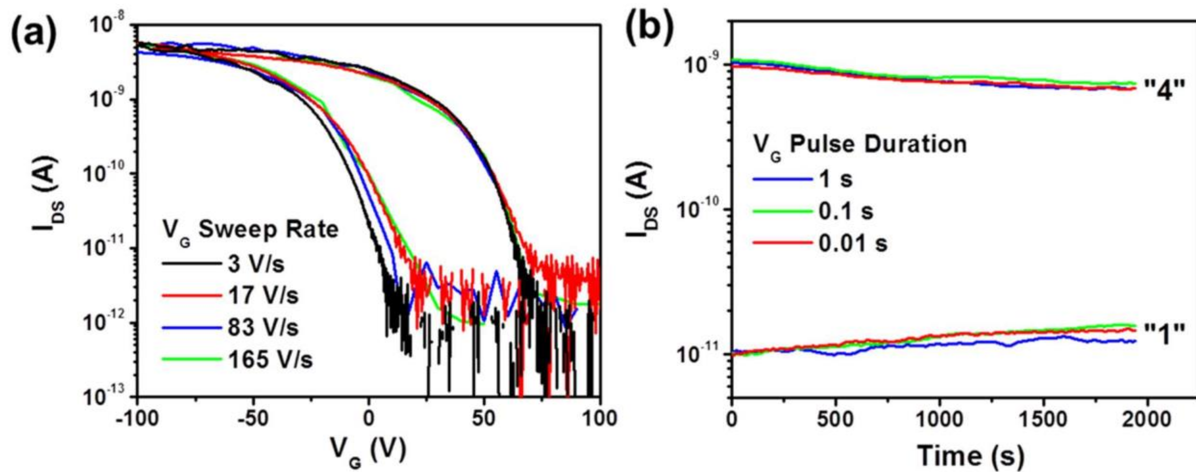


Figure 4.15 Effects of different excitation signal durations on the charge-retention characteristics of WSe_2 FETs: (a) hysteretic transfer characteristic curves of a representative WSe_2 FET acquired at different V_G sweep rates (3, 17, 83, 165 V/s); (b) retention characteristics (*i.e.*, I_{DS}-t curves measured at V_G = 0 and V_{DS} = 0.05 V) of charge-trapping States "1" and "4" excited by $\pm$100 V_G pulses with different durations (0.01, 0.1, and 1 s).

4.4 Summary

In summary, we studied the FETs with mechanically-exfoliated few-layer WSe_2 channels and found that such WSe_2 FETs demonstrated abnormal charge-trapping characteristics, *i.e.,* long-lasting charge-trapping states with relatively large extrema spacing and analog tenability. Plasma-doped few-layer MoS_2 FETs also exhibit similar long-lasting charge-trapping states, but as-exfoliated MoS_2 FETs do not have such states. Based on these device results, we hypothesize that the observed long-lasting charge-trapping states in few-layer WSe_2 FETs are caused by the exfoliation-induced ripple structures or interlayer displacements/twists at cleaved WSe_2 surfaces. Our surface analysis results in combination with additional characterization of monolayer WSe_2

FETs strongly support this hypothesis. Especially, the HRTEM characterization verifies the existence of top-view Moiré patterns due to exfoliation-induced interlayer twisting and lattice incommensurateness, which are expected to generate charge-trapping states with relatively large binding energies. In addition, we also identified the existence of multiple metastable charge-trapping states in few-layer WSe_2 FETs, which can be controlled by both gate and drain-source pulses. Finally, the charge-trapping states excited in a WSe_2 FET can be calibrated into multibit data levels. We demonstrated that multiple WSe_2 FETs fabricated in the same batch exhibit a high device-to-device consistency in their calibrated 2-bit data levels. This work advances the understanding of charge-trapping characteristics of emerging nanoelectronic devices made from layered semiconductors. The observed long-lasting and metastable charge-trapping states could be further studied and exploited to create innovative cost-effective memory devices with multibit data storage capability.

Chapter 5

Multibit Data Storage States in Plasma-Treated MoS_2 Transistors

5.1 Introduction

The exploration of charge trapping mechanism in TMDCs inspires us to leverage the unique structure properties of TMDCs in innovative information storage applications. Although solid state drive (SSD) technologies such as flash memory have become more and more popular nowadays, the main challenge remains to be the cost as the current SSDs are still about 5 times more expensive per unit of storage than the conventional hard disk drives (HDDs). To produce much cheaper SSDs, it is desirable to develop new low-cost memory fabrication processes, as well as new memory architectures for improving the storage density. One of such efforts is to create multibit data storage memory devices to achieve a higher storage density [70-75]. The fabrication of multibit flash memories needs precise deposition of multiple semiconductor layers and multiple overlay processes to create complicated memory transistors consisting of multiple floating gates and blocking/tunneling layers [70, 71, 77]. This significantly increases complexity and cost of memory cells [70, 71, 77]. The recent efforts have also demonstrated other prototype multibit memories based on different materials and device structures, including memories based on organic

semiconductors with ambipolar transport properties [72], memory transistors based on nanostructured materials [73], flash memory-like transistors with capacitively coupled nanoparticle (NP)-based floating gates [74], and multi-level resistive memories based on phase-change materials [114]. Relatively complicated and expensive processes are still demanded for making these devices. Therefore, new types of multibit memory with a unique combination of excellent retention/endurance property, simple structure, and low cost are highly desirable.

Two dimensional (2D) layered transition metal dichalcogenides (TMDCs), such as MoS_2, WSe_2, and WS_2, were recently envisioned as promising material candidates for making low-cost, high-performance field-effect transistors (FETs) [4-8]. In addition, 2D heterostructures consisting of MoS_2 and other 2D layers have been used for making new non-volatile memory transistors [67-69, 78, 79]. These works motivate and inspire additional research efforts to leverage unique electronic and structural properties of emerging TMDCs in new cost-effective memory applications.

In this chapter, we present the fabrication and characterization of new MoS_2-based non-volatile multibit memory FETs with an excellent combination of retention/endurance properties and simple cell architecture. In the previous work, we have demonstrated the exfoliation-induced interlayer deformation can enable charge trapping states in TMDCs. Comparing to mechanical exfoliation, plasma doping can serve as a more reliable approach for generating reproducible deformation nanostructures in TMDC layers, and therefore creating more consistent charge-trapping states suitable for multi-bit data storage applications. Using such plasma-treated MoS_2 FETs, we have demonstrated highly reliable binary and 2-bit (*i.e.*, 4-level) data states with potential for year-scale data retention, as well as 3-bit (*i.e.*, 8-level) data states at least suitable for day-scale

storage. In addition, our research indicates that the memory FETs fabricated by nanoscale-area plasma treatment exhibit a faster programming speed than that of FETs made by blank plasma treatment. Such a new memory capability is hypothesized to be caused by the spontaneous separation of plasma-doped MoS_2 layers from undoped layers, which forms an ambipolar charging layer interfacing the FET channel through a tunneling barrier. This structure can enable the non-volatile retention of charged carriers as well as the reversible modulation of polarity and amount of trapped charges, ultimately resulting in multi-level data states in FETs. Furthermore, this hypothesis is strongly supported by the Kelvin force microscopy (KFM) results.

5.2 Methods and Materials

5.2.1 Fabrication of the Initial Field-Effect Transistors Using Exfoliated Pristine MoS_2 Flakes

In this work, the initial MoS_2 FETs are fabricated by using our previously reported printing-based approach [55]. MoS_2 channel thicknesses (t_{MoS2}) are specifically controlled to be 15-30 nm, aiming to achieve relatively high field-effect mobility values (μ = 20 to 30 cm^2 /Vs) [98, 107]. The channel lengths (L) are 2 to 10 μm, and the average channel widths (W) are 5 to 15 μm. Ti (5 nm)/Au (50 nm) electrode pairs serve as drain (D) and source (S) contacts, which are fabricated by using photolithography followed by metal deposition and lift-off in a solvent. The p^+-Si substrates are used as back gates (G). Thermally grown SiO_2 layers (300 nm thick) are used as the gate dielectrics. Here, the reason that such relatively thick SiO_2 layers are used as gate dielectrics is that we employ a simple color coding method for quickly locating MoS2 flakes with suitable thicknesses (15-30 nm) [60]. In this method, MoS_2 flakes are usually deposited on Si substrates coated with 300 nm thick SiO_2 layers, which can result in an optimal color contrast of few layer

MoS_2 device features against the substrate background under the illumination of a regular mask aligner and can therefore make it convenient to perform overlay alignment. However, with the alternative advanced imaging tools (*e.g.,* a Micro-Raman tool) to identify MoS_2 feature thickness, it is possible to use much thinner gate dielectrics and further scale down the required programming voltages.

5.2.2 Water Vapor Treatment of MoS_2 FETs Using Atomic Layer Deposition (ALD) Processes

An ALD tool (Oxford Instruments, OpAL^{TM}) is employed to treat as-fabricated pristine MoS_2-based back-gated FETs with water vapor and subsequently cover the moisture-treated MoS_2 channel surface with an Al_2O_3 film. This Al_2O_3 film on top of the MoS_2 surface serves as an encapsulation layer for retaining the trapped water molecules at the MoS_2/Al_2O_3 interface for a long time. In addition, the MoS_2 FETs treated by using this ALD-assisted moisture treatment process exhibit a more prominent hysteresis of the transfer characteristics than the moisture-treated FETs without encapsulation layers. The moisture treatment is performed at 80°C under a water vapor pressure of 100 Torr for 1 min. During the subsequent Al_2O_3 deposition, the precursor (*i.e.*, $Al(CH_3)_3$(trimethylaluminum (TMA)) and water vapor are alternately entrained in the Ar carrier flow. The carrier gas flow rate is 50 sccm. In particular, during each of ALD cycles, (1) the TMA precursor is pulsed for 20 ms (pressure: 100Torr, temperature: 80°C); (2) the precursor is purged away by the carrier gas for 4s; (3) water vapor (pressure: 100Torr, temperature: 80°C) is pulsed for 20 ms and held for 4s. Such an ALD cycle is repeated for 230 times and the final Al_2O_3 encapsulation film thickness is ~30 nm.

5.2.3 Plasma Treatment for Converting MoS_2 FETs into Multibit Memory FETs

The top layers of MoS_2 FET channels are treated with various plasmas (*i.e.,* O_2, SF_6, CF_4, and CHF_3) in an inductively coupled plasma-based reactive ion etching (RIE) tool. For all plasma recipes, the RF power is fixed to 200 W, the pressure is 10 mTorr, the precursor gas flow rate is 10 sccm, and the treatment time for each FET is fixed to 2 min. The surface morphology of plasma-treated MoS_2 FETs is characterized by using a scanning electron microscope (SEM).

5.2.4 Electrical Characterizations of Plasma-Induced Binary and Multibit Memory States

The memory FETs are characterized in a LakeShore probe station connecting to a HP4145 semiconductor parameter analyzer that can generate gate voltage (V_G) pulses with duration widths ranging from10 ms to 1 s. To characterize the hysteretic behaviors of the transfer curves of memory FETs, drain-source current (I_{DS})-gate voltage (V_G) curves are acquired along two different V_G sweep directions with a constant sweep rate of 10 V/s. To configure a memory FET into binary data states, a +100 V (-100 V) V_G pulse (duration Δt: 10ms to 1 s) is applied to induce a low(high)-conductance "erase" ("write") state in the FET. To evaluate the retention properties of data states, time-dependent I_{DS} values (*i.e.,* I_{DS}-t curves) are measured under fixed V_{DS} and V_G (typically $V_G = 0$ and $V_{DS} = 0.01$ to 0.1 V) after the initial settings of the memory FET with specific V_G pulses. A Kelvin force microscope (Veeco NanoMan Dimension V system, equipped with Pt/Ir-coated tips with tip radius $R \approx 20$ nm and resonant frequency $f_0 \approx 75$ kHz) is applied to detect both the polarity and amount of the trapped charge in plasma-treated MoS_2 layers, which are modulated by the V_G pulse amplitude.

5.3 Result and Discussion

5.3.1 Multibit Memory States in Plasma-Treated MoS_2 FET

As illustrated in Figure 5.1 (a), a simple plasma treatment converts a few-layer MoS_2 back-gated FET into a memory cell. In this work, the initial MoS_2 FETs were fabricated by using a printing-based approach previously published [55]. MoS_2 channel thicknesses (t_{MoS2}) were controlled to be 15-30 nm, aiming to achieve relatively high field-effect mobility values (μ = 20 to 30 cm^2/Vs) [98, 107]. Channel lengths (L) were 2 to 10 μm, and the average channel widths (W) were 10 to 15 μm. Ti (5 nm)/Au (50 nm) electrode pairs served as drain (D) and source (S) contacts. The p^+-Si substrates were used as back gates (G). Thermally grown SiO_2 layers (300 nm thick) were used as the gate dielectrics. To generate the memory capability, the top surfaces of MoS_2 FET channels were treated with various plasmas (*i.e.*, CHF_3, CF_4, and O_2) by using a reactive ion etcher (RIE). For all the plasma recipes, the precursor gas flow rate was 10 sccm; the RIE power was 100 W; and the treatment time was 1 min. Figure 5.1 (b) shows the optical micrograph (OM) of an exemplary MoS_2 memory FET treated with O_2 plasma (L=2 μm; W~5 μm; t_{MoS2}~20 nm). The memory FETs were characterized by using a HP4145 semiconductor parameter analyzer that can generate gate voltage (V_G) pulses with duration widths ranging from 10 ms to 1 s. To characterize the hysteretic behaviors of the transfer curves of memory FETs, drain-source current (I_{DS})-gate voltage (V_G) curves were acquired along two different V_G sweep directions with a constant sweep rate of 10 V/s. To configure a memory FET into binary data states, a +100V (-100V) V_G pulse (duration Δt: 10 ms -1 s) was applied to induce a low (high)-conductance "erase (ER)" ("write (WR)") state in the FET. In addition, to evaluate the retention properties of data

states, time-dependent I_{DS} values (*i.e.*, I_{DS}-t curves) were measured under fixed V_{DS} and V_G (typically $V_G = 0$ and $V_{DS} = 0.01$ to 0.1 V).

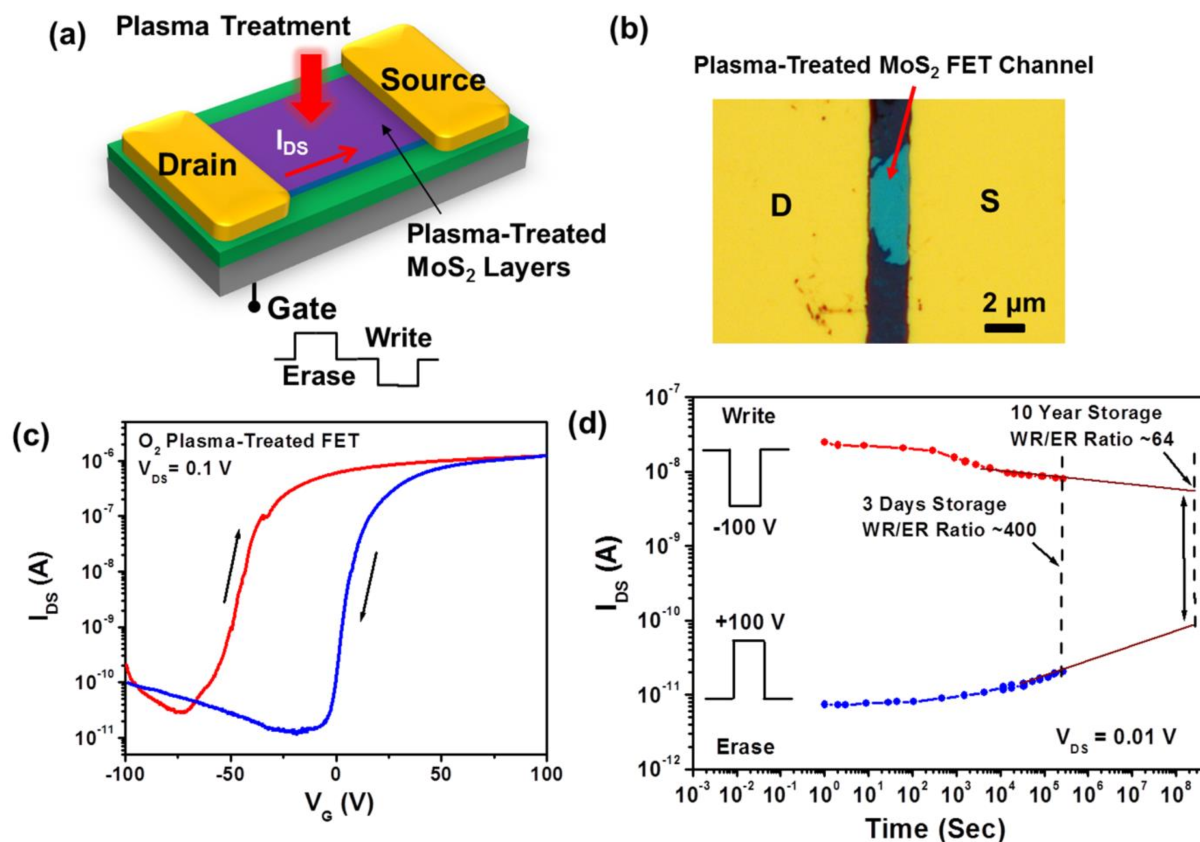


Figure 5.1 (a) Illustration of a back-gated MoS_2 memory FET created by a simple plasma treatment. (b) Optical micrograph of a memory FET consisting of an O_2 plasma-treated MoS_2 channel (thickness: 20 nm, length: 2 µm, average width: ~ 6 µm), Ti/Au D/S contacts, and a p^+-Si back gate. (c) Transfer curves (I_{DS}-V_G curves acquired along two different V_G sweep directions with a sweep rate of 10 V/s) and (d) retention characteristics (I_{DS}-t curves under V_{DS}= 0.01 V and V_G= 0 V recorded for 3 days) of the memory FET shown in (b). The insets in (d) show the ±100 V 1 s pulses applied at the back gate for retention measurements. The WR/ER ratio after 3 days is measured to be ~400. The WR/ER ratio after 10 years is estimated to be ~ 64 that is suitable for long-term binary data storage.

In comparison, we fabricated an untreated pristine MoS_2 FET and its transfer characteristics exhibits a mild hysteresis, as shown in Figure 5.2. This mild hysteresis was attributed to the charging/discharging processes associated with the charge-trapping sites at the MoS_2/SiO_2 interface [64]. As indicated by the previous work, such charge-trapping sites can retain trapped charges for relatively short time durations (trapping time constants (τ) range from 30 to 500 s) [64], not suitable for data storage. We subsequently measured the transfer characteristics of a MoS_2 FET treated with water vapor by using an atomic layer deposition (ALD) tool (see Section 5.2.2 for more details on this treatment process). As shown in Figure 5.3 (a), this moisture-treated FET exhibits a much more prominent I_{DS}-V_G hysteresis as compared to the untreated FET. Such a large hysteresis was attributed to the high density of moisture-induced charge traps, and it motivated us to characterize the retention properties of trapped charges in this moisture-treated FET. Figure 5.3 (b) shows I_{DS}-t curves of the potential binary data states of this moisture-treated FET. After the application of ±100 V V_G pulses, the I_{DS} values of "write" and "erase" states quickly relaxed to almost the same value after ~ 2000s. The device transfer characteristics imply that although the water molecules adsorbed on MoS_2 FETs can result in a prominent hysteresis, the charge-trapping times of such hysteresis and data states are too short to enable any practical data storage applications.

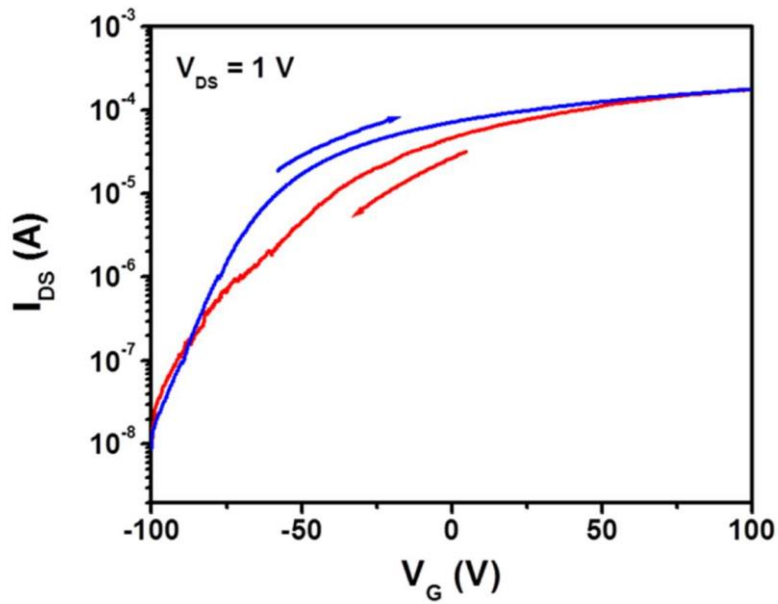


Figure 5.2 Transfer curves (I_{DS}-V_G curves acquired along two different V_G sweep directions with a sweep rate of 10 V/s) of an untreated pristine MoS_2 FET that exhibits a relative weak hysteretic behavior.

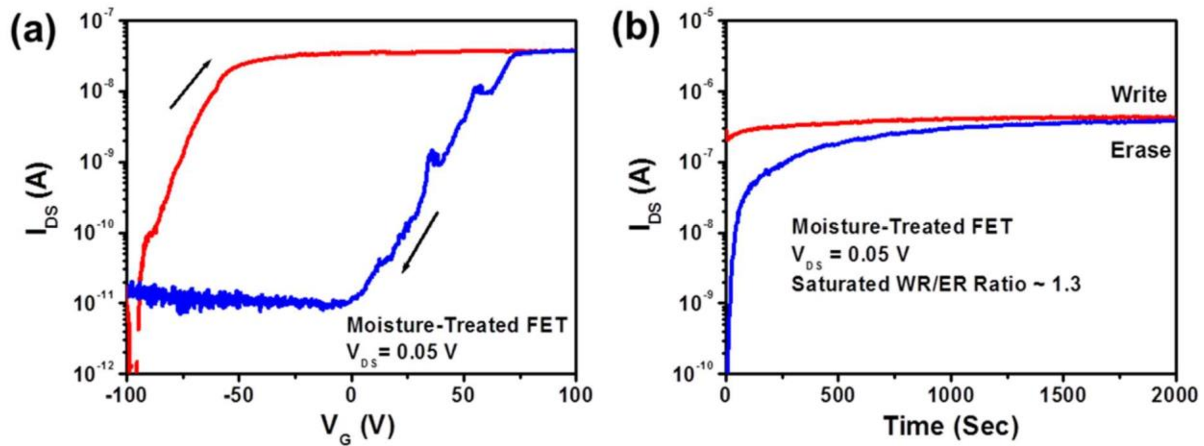


Figure 5.3 Transfer curves (I_{DS}-V_G curves acquired with a V_G sweep rate of 10 V/s) (a) and retention characteristic curves (I_{DS}-t curves) of potential binary data states ("Write" and "Erase") (b) of a MoS_2 FET treated with water vapor by using an ALD tool. Here, I_{DS}-t curves were measured with $V_G = 0$ and $V_{DS} = 50$ mV.

In contrast to the untreated and moisture-treated MoS_2 FETs, all plasma-treated FETs exhibit well-differentiated binary data states with excellent retention properties. For example, Figure 5.1 (c) and Figure 5.1 (d) display transfer and retention characteristics of an O_2 plasma-treated FET (*i.e.*, the one shown in Figure 5.1 (b)), respectively. This memory FET exhibit a high WR/ER ratio (*i.e.*, I_{WR}/I_{ER}) that was measured to be ~10^3 after a 1-hour retention test and ~400 after a 3-day retention test. Based on the 3-day retention test data plotted in Figure 5.1 (d), the WR/ER ratio after 10 years is estimated to be ~ 64 that can still enable an unambiguous reading of distinguishable I_{DS} values for "write" and "erase" states. Figure 5.4 shows the transfer and retention characteristics of exemplary CF_4 and CHF_3 plasma-treated MoS_2 memory FETs. CF_4 and CHF_3 plasma-treated FETs typically exhibit relatively lower WR/ER ratios (10 to 100 after 2000s retention tests) in comparison with those of O_2 plasma-treated ones (100 to 1,500 after 2000s retention tests). These characterizations indicate that plasma-induced (especially, O_2 plasma-induced) charge-trapping levels in MoS_2 can retain trapped charges for a much longer time and are suitable for long-term data storage applications, in comparison with the traps at MoS_2/SiO_2 interfaces and moisture-induced traps.

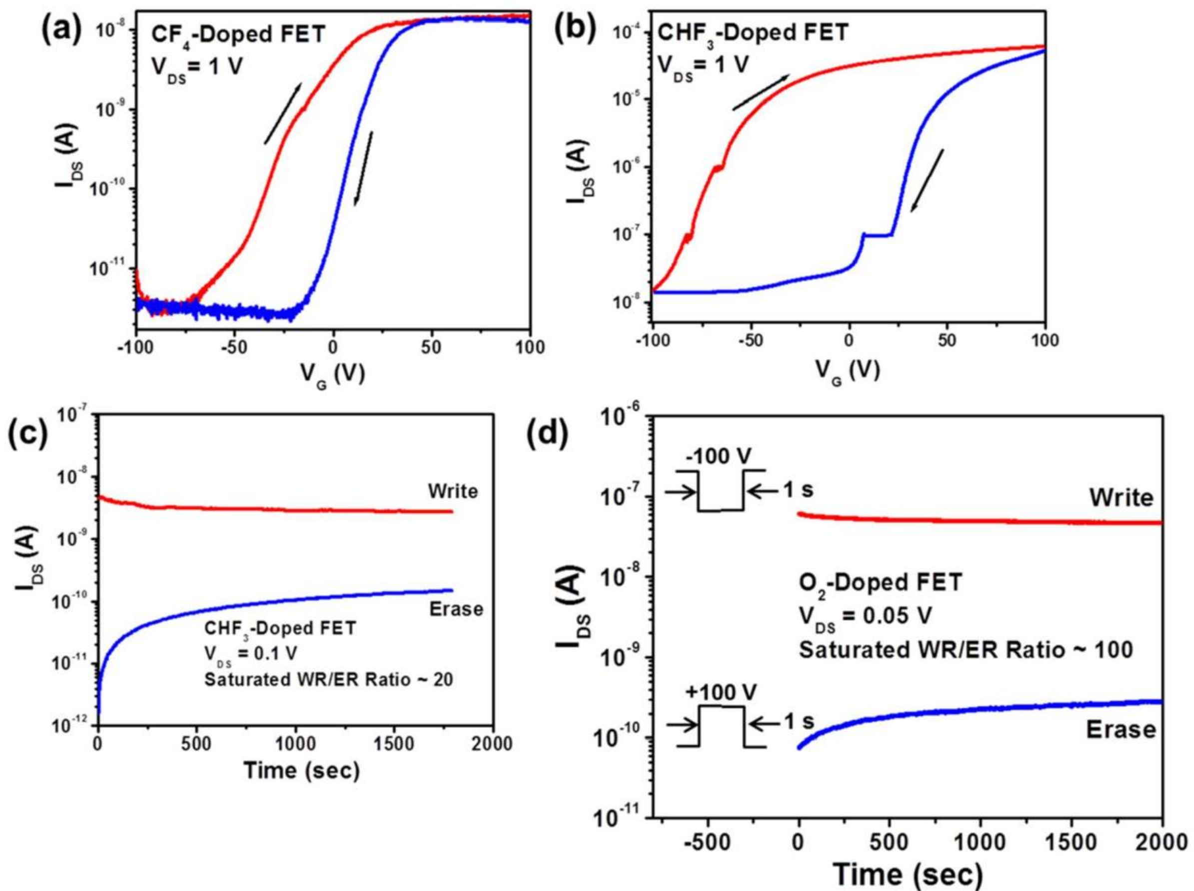


Figure 5.4. Transfer curves (I_{DS}-V_G curves acquired with a V_G sweep rate of 10 V/s) of MoS_2 FETs treated with (a) CF_4 and (b) CHF_3 plasmas, respectively. Retention characteristic curves (I_{DS}-t curves) of binary data states ("Write" and "Erase") of MoS_2 FETs treated with (c) CHF_3 and (d) O_2 plasmas, respectively. Here, all I_{DS}-t curves were measured with $V_G = 0$ and $V_{DS} = 0.1$ V.

The MoS_2 FETs with O_2 plasma-treatment were further tested to demonstrate multibit storage capability. To obtain an n-bit/FET storage capability, a memory FET needs to have at least 2^n reliable data levels. For example, the same FET shown in Figure 5.1 (d) was used for realizing 2-bit storage that needs 4 data levels. Figure 5.5 (a) sketches four V_G signals used for configuring the memory FET into 4 data states ("00", "01", "10", "11"). Here, the signals labeled with "00"

and "11" are exactly the same ±100 V, 1s V_G pulse signals used for setting the FET into binary "erase" (now as "00") and "write" (now as "11") states, respectively. The V_G signal for setting the "01" ("10") state is a dual-pulse signal that consists of one -100V (+100V), 1s pulse (V_{G1}) immediately followed with another +75V (-75V), 1s pulse (V_{G2}). Here, the 1st pulse (V_{G1}) is used to assure that any previously trapped charged carriers with the same polarity as that of the targeted new ones are completely eliminated. The 2nd pulse (V_{G2}) sets the FET with a new charging state. Figure 5.5 (b) shows the 3-day retention test data of 4 data levels. Based on the extrapolated I_{DS}-t curves (solid lines in log scales) shown in Figure 5.5 (b), these 4 data states are anticipated to be still distinguishable after 10 years. Therefore, this O_2 plasma-treated MoS_2 FET can serve as a 2-bit memory cell with a year-scale data storage capability.

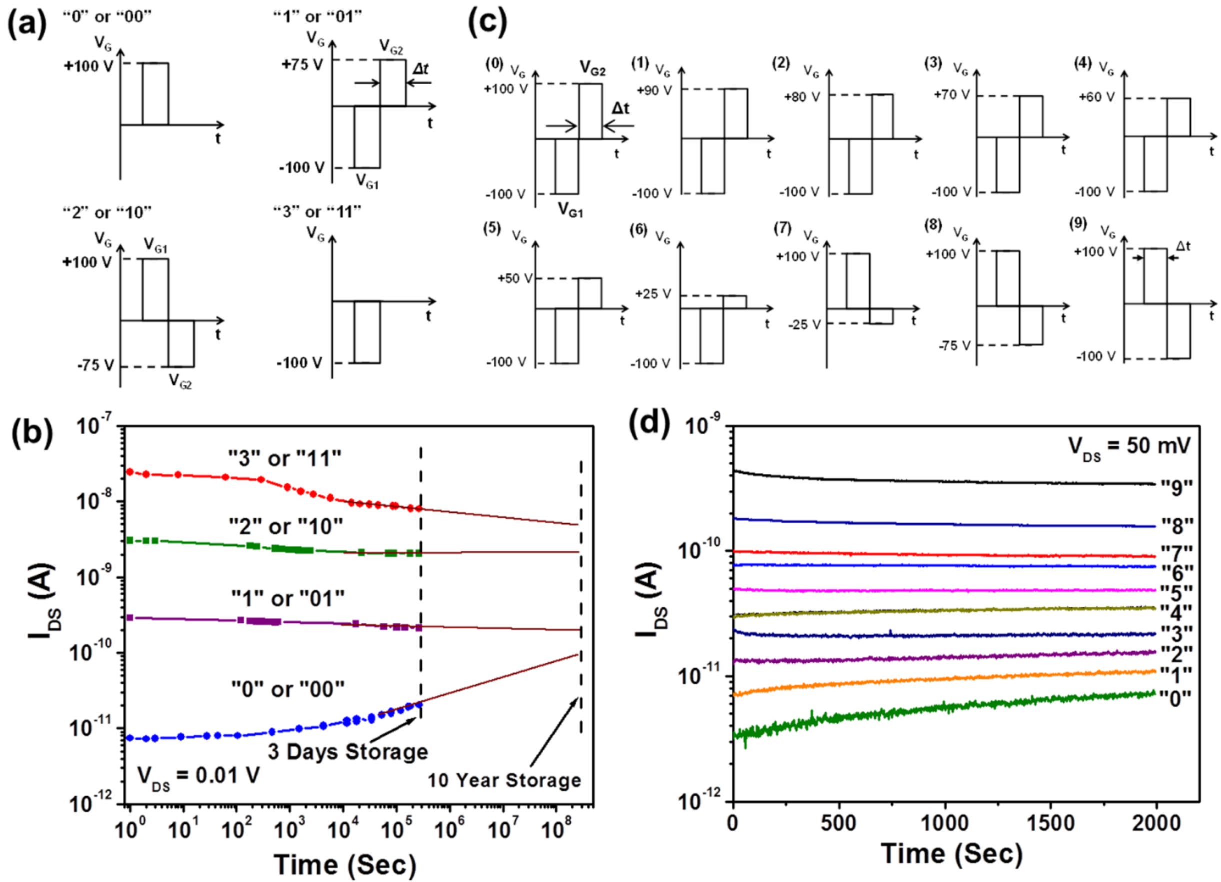


Figure 5.5 (a) The V_G signals used for programming the memory FET (the one shown in Fig. 1) into 4 data states ("00", "01", "10", "11", *i.e.*, a 2-bit memory). (b) Retention characteristics of 4 data states recorded for 3 days. For these retention measurements, V_{DS}= 0.01 V, V_G= 0 V. It is estimated that these 4 data states can be well discernible within 10 years since the initial applications of programming V_G signals. (c) The V_G signals for programming another plasma-treated MoS_2 memory FET into 10 data states. (d) Retention characteristics of 10 well-discernible data states recorded for 2000 s. For these 10 retention measurements, V_{DS} = 0.05 V, V_G = 0 V.

Using the dual-pulse V_G signals sketched in Figure 5.5 (c), another O_2 plasma-treated FET was programmed into 10 stable data states ("0" to "9"). The 2nd pulses (V_{G2}) of these signals have different polarities and amplitudes, which can result in different amounts of positive/negative charges trapped in the FET and generate multiple data levels. Figure 5.5 (d) shows the retention

behaviors of these 10 data levels for 2000 s. Based on the retention test data, it is estimated that these 10 data levels are distinguishable within day-scale time durations after the initial setting (see Figure 5.6). Thus, such a memory FET exhibits 3-bit (*i.e.,* 8 data levels) storage capability and can be used for electronic applications requiring hour- or day-scale data storage functionalities, such as disposable electronic tags and buffer memories for displays.

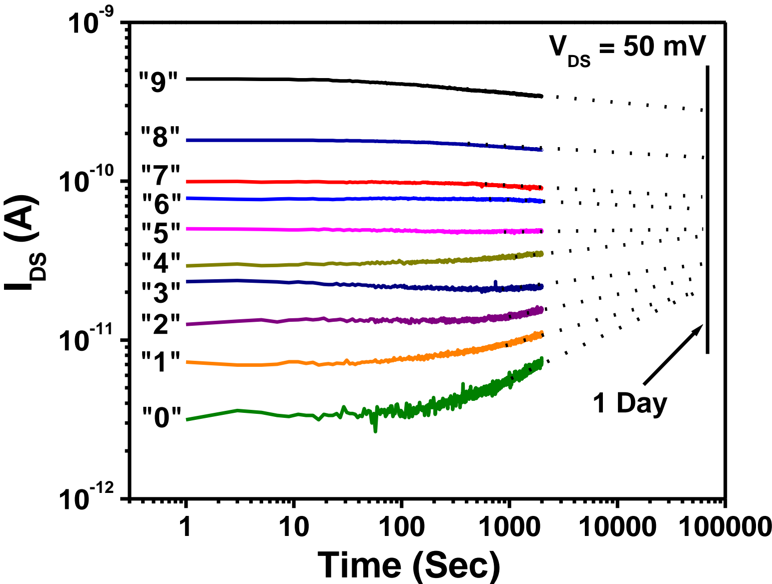


Figure 5.6 Retention characteristics of 10 data states recorded for 2000 s, which are estimated to be well discernible within hour- or day-scale time durations after the initial setting. For these 10 retention measurements, $V_{DS} = 0.05$ V, $V_G = 0$ V.

To further evaluate the endurance property of all created memory states, an O_2 plasma-treated FET was periodically programmed into 8 data states by repeatedly applying 8 dual-pulse V_G signals (*i.e.*, “0” to “1” to “2” … to “7” then repeat), as indicated in Figure 5.7 (a). When the FET was switched into a data state, its current transfer characteristic curve (*i.e.*, I_{DS}-V_G curve for V_G = -

10 to 10 V; V_{DS} = 50 mV) was recorded. Figure 5.7 (a) shows the transfer curves corresponding to 8 data states that were recorded during the first 10 programming cycles. Figure 5.7 (b) plots I_{DS} values (measured under V_G = 0 V, V_{DS} = 50 mV) of 8 data states recorded for 100 cycles, which indicates that such plasma-induced multibit memory states have a good endurance property.

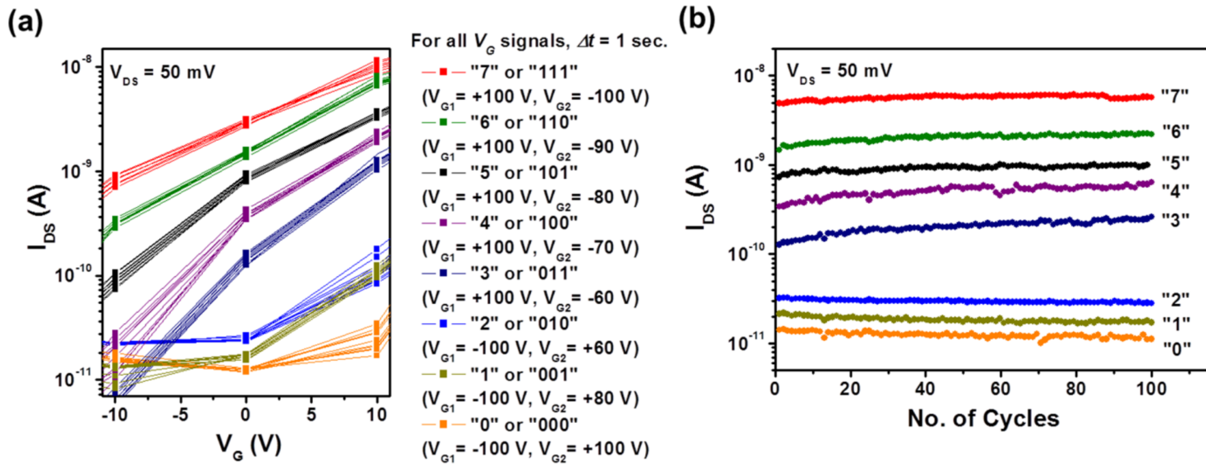


Figure 5.7 Switching endurance characteristics of a MoS_2 memory FET: (a) Transfer curves (I_{DS}-V_G curves) corresponding to 8 data states measured for 10 sequential cycles; (b) data levels (I_{DS} values measured at V_{DS}= 0.05 V, V_G= 0 V after the applications of programming V_G signals) recorded for 100 sequential cycles (for each endurance characterization cycle, the memory FET is sequentially programmed into "000" to "111" states, demonstrating a repeatable 3-bit memory capability).

To investigate the effect of the V_G pulse duration (Δt) on the correspondingly induced data states, as shown in Figure 5.8 (a), we measured the retention curves of the binary data levels of an O_2 plasma-treated FET (L ~ 2 μm, W ~ 5 μm) after it was set by applying ±100V V_G pulses with different time durations ranging from 10 ms to 1 s. Figure 5.8 (a) shows that the I_{DS} value of "Write" state exhibits a weak dependence on Δt, whereas the I_{DS} value of "Erase" state highly depends on Δt, therefore resulting in a strong dependence of the WR/ER ratio on Δt. When Δt is

reduced from 1s to 10 ms, the WR/ER ratio drops from ~100 to 15. This suggests that a long pulse duration (Δt > 1s) may be needed to fully charge (or discharge) all plasma-induced charge-trapping states in a microscale size FET. Assuming that the capacitance associated with plasma-induced charge-trapping states is proportional to the total MoS_2 surface area treated with plasma, the required memory setting time is anticipated to be scaled down with reduction of the total plasma-treated area (*e.g.*, using the selected-area plasma treatment). Figure 5.8 (b) illustrates a MoS_2 memory FET with a selected area treated with plasma. Here, the selected area is a line with a nanoscale width across the whole FET channel. Figure 5.8 (c) shows a zoomed (in-lens mode) scanning electron microscope (SEM) image of a MoS_2 FET surface with a selected area (*i.e.*, 46 nm wide line region) treated with O_2 plasma. Figure 5.8 (d) displays the retention curves of binary data levels of this memory FET after it was set by applying ±100V V_G pulses with different time durations ranging from 10 ms to 1 s. Although this FET has the same total channel area (*i.e.*, L ~ 2 μm, W ~ 5 μm) as that of the blank-treated FET shown in Figure 5.8 (a), both its "Write" and "Erase" I_{DS} values as well as WR/ER ratio exhibit a weak dependence on Δt values. This result indicates that, comparing to the transistor with a blank plasma treatment, a much smaller capacitance of plasma-induced charge-trapping states can be formed by the selected-area plasma treatment, which will result in a faster memory setting speed and still maintain reasonably good WR/ER ratios (40 to 100) suitable for practical data storage applications.

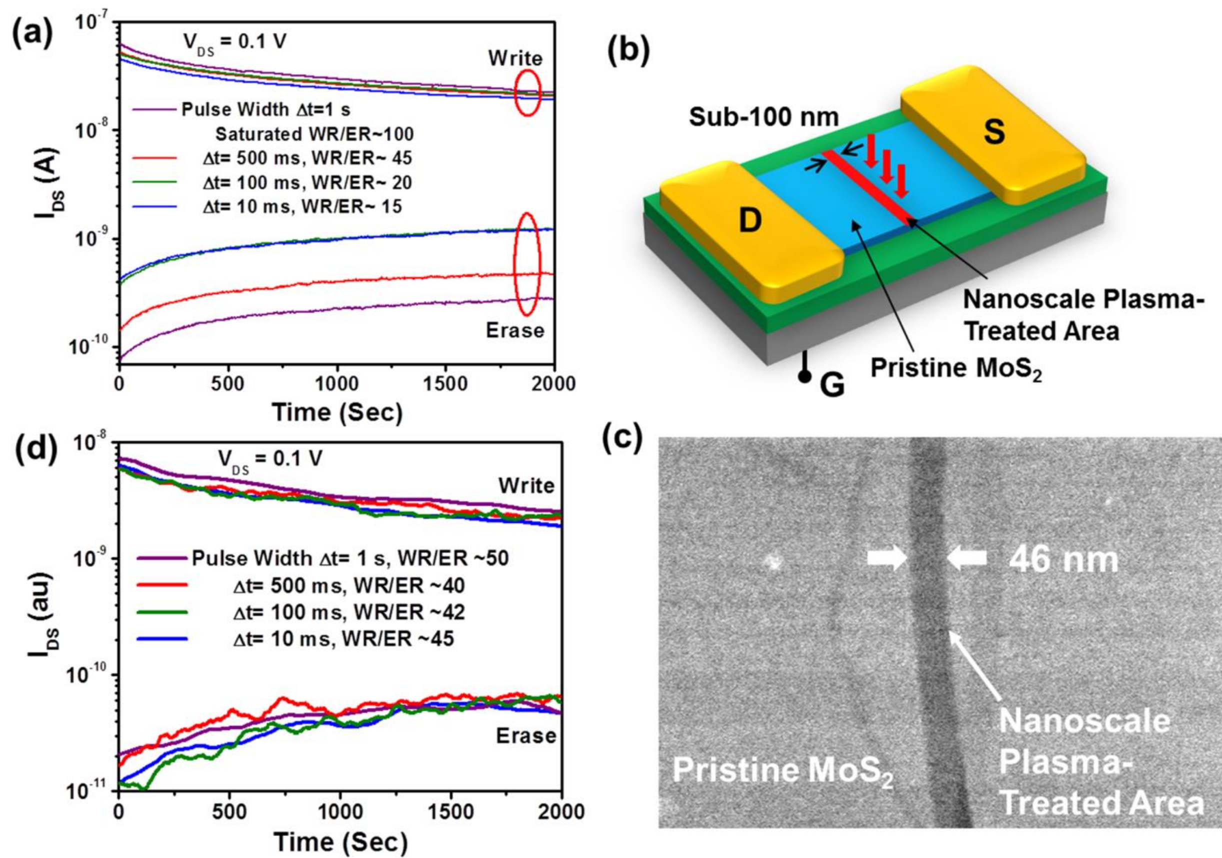


Figure 5.8 (a) Retention characteristics of the binary data states in a microscale memory FET (channel length: ~ 5 μm, width: ~ 10 μm), which were measured after the device was programmed by ±100 pulses with various pulse durations (Δt = 10 ms, 100 ms, 500 ms, and 1 s). (b) Illustration of a MoS_2 memory FET fabricated by using selected-area plasma treatment. Here, the plasma-treated region is a sub-100 nm wide nanoline across the pristine MoS_2 channel. (c) SEM image of a 46 nm wide plasma-treated line region across a pristine MoS_2 FET channel. (d) Retention characteristics of the binary data states in the MoS_2 memory FET shown in (c), which were measured after the device was programmed by ±100 pulses with various pulse durations.

5.3.2 Hypothesized Physics Mechanism for MoS_2 Memory FET

For the further exploration of the in-depth mechanism responsible for the observed memory capability, MoS_2 surfaces treated with O_2 plasma were inspected by using scanning electron microscopy (SEM). The SEM image in Figure 5.9 (a) shows that the O_2 plasma-treated MoS_2 surface exhibits a nanoscale roughness with average period of ~ 10 nm. Such a roughness, in contrast with the flat surface of a pristine MoS_2 sample, is attributed to the plasma-induced doping of external atoms, which can induce a significant expansion of the MoS_2 layers and let these layers ripple up and down [107]. This ripple effect is expected to partially exfoliate the plasma-doped top layers from the undoped pristine MoS_2 layers and form charge-trapping sites slightly isolated from the FET channel, as illustrated in Figure 5.9 (b). The gap size between such charge-trapping sites and the undoped MoS_2 channel is estimated to be in the order of the average period of the ripple features in the top layers (*i.e.*, 5-10 nm). This gap may serve as a tunneling/blocking barrier layer for retaining trapped charges and switching the memory states. Based on this analysis, we hypothesize a possible write/erase mechanism to explain the memory capability of plasma-treated MoS_2 FETs. Figure 5.9 (c) illustrates the hypothesized band structure (*i.e.*, the density of states (DOS) function) of a plasma-treated MoS_2 FET. The untreated (or pristine) MoS_2 layers (*i.e.*, the FET channel region) have a typical band structure of lightly doped semiconductors with a relatively low density of impurity states in the bandgap, whereas the plasma-treated top layers are expected to exhibit a rich of plasma-induced localized trapping states in the bandgap. It is also assumed that these trapping states are distributed over a broad energy range in the bandgap and they are likely to be a mixture of donor-type, acceptor-type, and isoelectronic deep-level traps. Such a large variety and broad energy distribution of plasma-induced traps are hypothesized based

on the fact that energetic plasma species, similar to electron irradiation, can generate a broad variety of defect configurations in MoS_2 layers, including sulfur vacancies, substitutional donor/acceptor defects, adatoms with charge, and isoelectronic impurities [7, 97, 107, 115]. Therefore, the plasma-treated MoS_2 top layers may serve as an ambipolar memory charging layer. At the initial neutral state, the net charge in the plasma-treated layers is assumed to be close to zero (*i.e.*, all donor-type traps are occupied with electrons, and all acceptor-type traps are vacant). To obtain an "erase" ("write") state, a positive (negative) V_G pulse is applied. In this case, the Fermi level is elevated (lowered) and the conduction (valence) band of untreated layers (*i.e.*, the FET channel) is populated with electrons (holes). These electrons (holes) have a high probability to tunnel through the barrier and are injected into the conduction (valence) band of the plasma-treated top layers. The injected electrons (holes) may quickly relax to the localized trapping states with the lower energies. When the V_G is set back to zero, the trapped electrons (holes) could be retained in the top layers for a long storage time, because of the existence of a barrier layer between plasma-treated and untreated layers as well as the lack of target states in the bandgap of untreated layers that can effectively prevent electrons (holes) to tunnel back from trapped states to the FET channel. This model also implies that the V_G pulse amplitude could modulate the total amount of charged carriers that are injected into the charge-trapping states in plasma-treated MoS_2 layers. Such trapping states, very likely different from the discrete trap levels in conventional memory FETs with floating gates, are distributed over a broad energy range and could accommodate different amounts of injected carriers with different polarities, therefore resulting in multiple data levels (*i.e.*, multiple I_{DS} values). Such a hypothesized model can preliminarily explain the observed multibit data storage capability. In addition, as implied by this model, the electrons (holes) trapped at

relatively high-energy states that are close to the conduction (valence) band could easily tunnel back to the FET channel and result in a slow relaxation of I_{DS} values. The higher V_G pulse could induce the trapping of more charged carriers in such high-energy states and result in a more prominent relaxation of I_{DS} values. This model implies that the data states with the highest or the lowest I_{DS} values/conductance, typically configured by ±100V V_G pulses, exhibit more prominent relaxation characteristics than other intermediate data states between them, which is consistent with our previous observation in the retention tests (*e.g.*, see Figures 5.5 (b) and (d)).

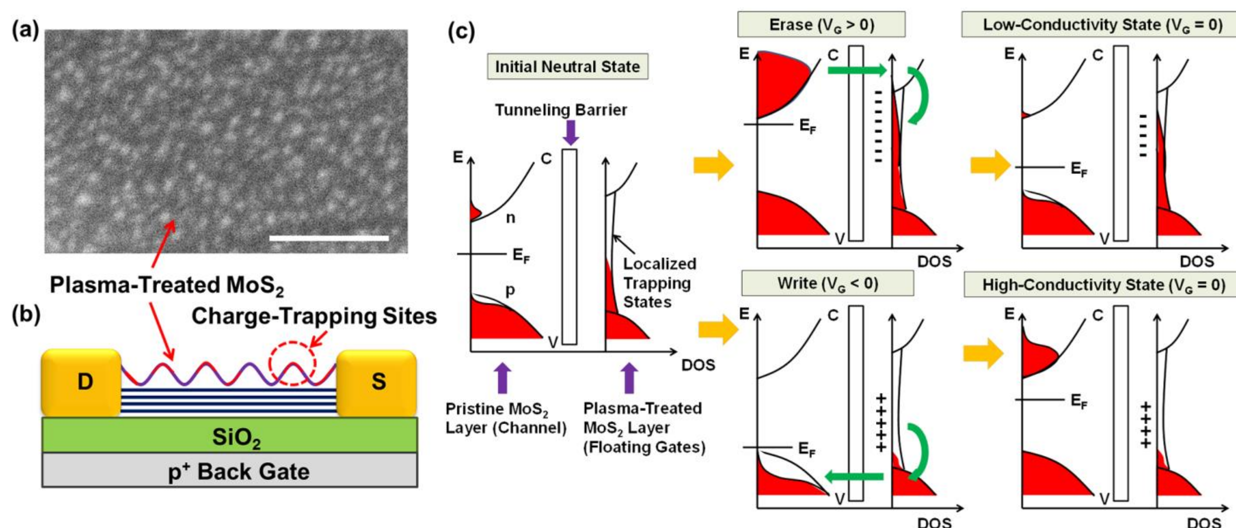


Figure 5.9 (a) SEM image of an O_2 plasma-treated MoS_2 surface that features nanoscale roughness features (the scale bar is 100 nm). (b) Cross-sectional illustration of a MoS_2 memory FET treated with plasma. The top few MoS_2 layers become rough because of the doping of plasma species. Part of the treated layers may be mechanically separated and electrically insulated from the intact bottom layers, and therefore can serve as a non-volatile charge-trapping layer (similar to the floating gate in a regular flash memory). The plasma-enhance gap between this charge-trapping layer and the intact MoS_2 channel can serve as a tunneling barrier layer. (c) Hypothesized write/erase schemes of plasma-treated MoS_2 memory FETs.

5.3.3 Kelvin Force Microscope (KFM) Imaging of Contact Potential on MoS_2 FET Surface

To further support our model and verify that plasma-treated MoS_2 layers can indeed serve as memory charging layers, the contact potential (or work function) difference (V_{CPD}) between V_G-modulated MoS_2 FET surfaces and the KFM tip was measured by using a Kelvin force microscope (KFM, Veeco NanoMan Dimension V system equipped with Pt/Ir-coated tips with tip radius R~ 20nm and resonant frequency f_0~ 75kHz). Figure 5.10 (a) shows the OM of an O_2 plasma-treated MoS_2 FET, in which the dashed box denotes the KFM-imaged area. Figure 5.10 (b) displays two KFM images that were captured after the FET was configured by applying a -100V, 1s V_G pulse and a +100V, 1s V_G pulse, respectively. The scanlines denoted by the solid lines are accordingly plotted in Figure 5.10 (c). Figures 5.10 (b) and (c) explicitly show that the polarity switching of the applied V_G pulse can accordingly switch the V_{CPD} polarity on the MoS_2 surface but does not change the V_{CPD} on the SiO_2 surface. Here, the V_{CPD} value on the MoS_2 surface is directly associated with the electrostatic interaction between the trapped charge in the top MoS_2 layers and the KFM tip [116, 117]. It should be noted that the charge trapped at other interfaces (*e.g.*, MoS_2/SiO_2 and Si/SiO_2 interfaces) can hardly affect the V_{CPD} value on the MoS_2 surface because of the screening effect of multilayer MoS_2 channels (the electric-field screening length in MoS_2 is 3-5 nm; the thickness of our FET channels is 20-30 nm) [117]. Therefore, the KFM result is consistent with our hypothesized model, indicating that the charge trapping states in plasma-treated top MoS_2 layers enable the ambipolar charge retention and gate modulation of the memory states observed in our MoS_2 FETs.

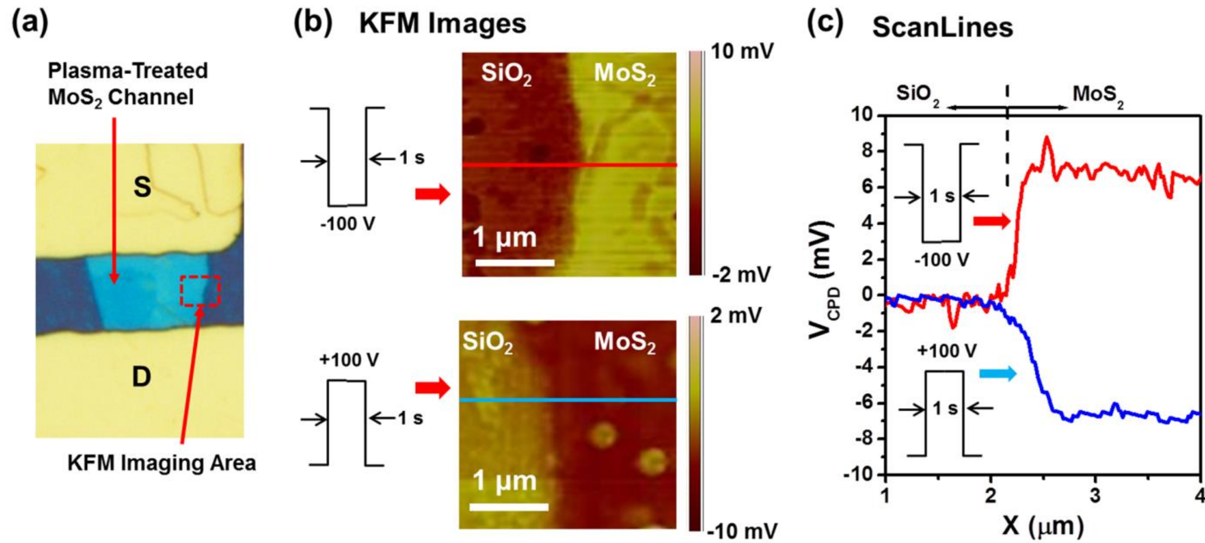


Figure 5.10 (a) Optical image of a plasma-treated MoS_2 memory FET used for KFM measurements. The dashed box indicates the region for KFM measurements. (b) KFM images of the MoS_2 channel after programmed by -100 V 1s (top) and +100 V 1 s (bottom) pulses. (c) KFM scanlines showing the V_{CPD} values of the MoS_2 channel programmed by -100 V 1s (red line) and +100 V 1 s (blue line) pulses.

5.3.4 Device-to-Device Consistency for MoS_2 Memory FETs

Finally, we evaluated the device-to-device consistency in our MoS_2 memory FETs. Although it is possible to create reliable individual memory FETs and observe durable multibit memory states in our experiments, our current FETs still exhibit prominent device-to-device variations in WR/ER ratios (*i.e.,* the absolute dynamic range of I_{DS} values for possible memory states), I_{DS} values for specific memory states (or data levels), and on/off ratios of initial FETs. Such variations are attributed to our current poor control of the geometry parameters of MoS_2 channels (*i.e.,* width, length, and thickness parameters of MoS_2 FET channels) and the fabrication introduced unexpected impurities. In particular, different lateral pattern shapes of MoS_2 channels can result in

different channel conductance (or I_{DS}) values, different MoS_2 thicknesses can result in different on/off and WR/ER ratios, and unexpected impurities introduced by the fabrication processes could modify the DOS profile of charge-trapping states in plasma-treated MoS_2 layers, resulting in an observable variation in the ratios of I_{DS} values for multiple data levels. These technical issues need to be addressed to ultimately enable the implementation of our MoS_2 memory FETs into large-area memory cell array architectures. With the current rapid development of 2D materials technologies, these problems are expected to be solved in the near future through developing new nanomanufacturing processes capable of producing MoS_2 FET array patterns with high uniformity in both feature dimensions and doping profiles.

For the further justification of our anticipation, we characterized five memory FETs that were fabricated in the same batch and were expected to have very similar doping profiles in their MoS_2 channels. All five devices have very close MoS_2 channel thicknesses (20 to 25 nm) and lengths (~5 μm), but very different channel widths (2-10 μm). To eliminate the effect of lateral pattern shapes on the memory data levels, we used the average conductivity (σ) values, instead of I_{DS} values, of MoS_2 channels to denote the memory states. Figure 5.11 plots the 2-bit data levels of these five memory FETs, which were measured after the FETs were set by the V_G signals listed in Figure 5.5 (a). Here, these FETs exhibit a reasonably good uniformity and consistency in all plasma-induced data levels. This experimental result implies that it is highly possible to fabricate large arrays of plasma-treated MoS_2 memory FETs with a high uniformity at all registered data levels *via* carefully unifying the processing conditions and device geometries.

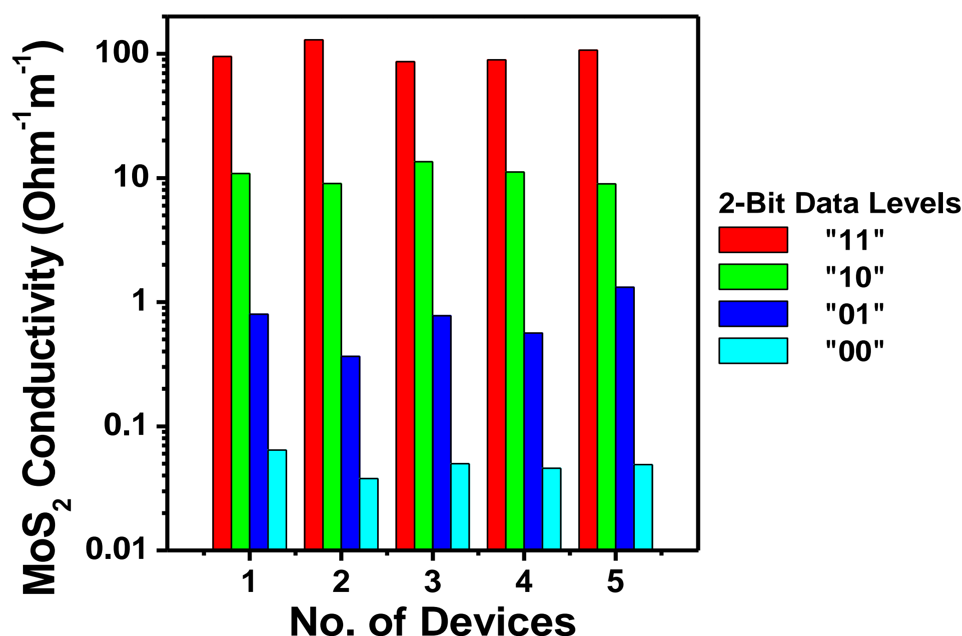


Figure 5.11 Two-bit data levels (*i.e.,* "00", "01", "10", "11" states) of five O_2 plasma-treated MoS_2 memory FETs fabricated in the same batch. Note that here the data levels are denoted by the conductivity of MoS_2 FET channels instead of I_{DS} values, which exhibit a reasonably good device-to-device uniformity and consistence.

5.4 Summary

In summary, we dramatically found that the plasma-treated MoS_2 FETs can provide multibit memory solutions with a year-scale 2bit/cell (or day-scale 3bit/cell) storage capability. The KFM results suggest that such a data storage capability is attributed to the plasma-induced separation of the top MoS_2 layers from the underlying pristine layers, which spontaneously forms a memory FET structure bearing an ambipolar charging layer coupled with the FET channel through a tunneling barrier. Such multibit memories exhibit a unique combination of excellent

retention/endurance characteristics, extremely simple structures, and low fabrication costs. Our work also shows that the programming speed of such memories can be improved by using nanoscale-area plasma treatments. This work greatly leverages the unique structural property of MoS_2 and other emerging 2D layered materials for nanoelectronic applications. The presented device structures and fabrication methods could be potentially developed into a low cost, upscalable memory solution for making high-performance cost-effective storage electronic products such as electronic labels, digital newspapers, and disposable tags.

Chapter 6

Summary and Future Work

6.1 Summary of Dissertation

The work in my dissertation successfully advanced nanofabrication technologies and device physics for memory applications based on atomically layered materials. The first part of my dissertation presents a nanoimprint/nanoprint-based method for fabricating TMDC-based (*e.g.*, MoS_2, WSe_2) field-effect transistors. In this process, the imprint TMDC pillar stamp is firstly made using conventional photolithography. The fabricated stamp and the polymer-coated SiO_2 substrate are subsequently imprinted together through a pair of jig plates in a vacuum oven and separated in a home-made roller tool *via* applying shear. The successful shear exfoliation of TMDC structures is identified by Raman spectroscopy. In addition, field effect transistors (FETs) made from produced multilayer MoS_2 flakes exhibit very consistent performance with high on/off ratios in the range of 10^5 -10^7. The characterization data measured from these FETs show that produced MoS_2 flakes have a high uniformity of electronic properties.

The second part of my dissertation presents a novel plasma-assisted doping technology for modulating the electronic properties of layered semiconductor materials such as TMDCs. Taking MoS_2 as an exemplary TMDC under study, *via* plasma doping, we have demonstrated *p*-type MoS_2 transistors that can be complementary to pristine *n*-type MoS_2 transistors, potentially enabling applications in CMOS circuits. Moreover, *via* applying plasma doping for selected areas, we have created 2D diodes with high rectification degrees (*i.e.*, forward/reverse current ratios up to 10^4 within a range of $V = \pm 1$ to $\pm 2V$) and a superior long-term stability at room temperature.

The third part of my dissertation presents a study on the abnormal charge-trapping and memory characteristics of few-layer WSe_2 transistors. We find that multiple charge-trapping states with large extrema spacing, long retention time, and quasi-analog tunability can be excited in the transistors made from mechanically-exfoliated few-layer WSe_2 flakes. Such unique charge-trapping characteristics of WSe_2 transistors are attributed to the exfoliation-induced interlayer deformation on the cleaved surfaces of few-layer WSe_2 flakes, which can spontaneously form ambipolar charge-trapping sites. Furthermore, our work has demonstrated that the charge-trapping states excited in multiple transistors could be calibrated into consistent multi-bit data storage levels for making working memories.

The fourth part of my dissertation presents an innovative device application of MoS_2 in making floating-gate-free, non-volatile, multi-bit memory FETs, which has a unique combination of excellent retention/endurance characterisitcs, simple device structures and extremely low fabrication cost. MoS_2-based memory FETs were fabricated using our plasma-assisted doping technology discussed in the second part. Using such memory FETs, we have demonstrated highly reliable binary and 2 bit (*i.e.*, 4 data levels) data states with a potential for year-scale data storage,

as well as 3 bit (*i.e.*, 8 data levels) data states at least suitable for day-scale data storage. This multi-bit memory capability is attributed to plasma-doping-induced deformation features in the MoS_2 layers very close to the cleaved surface, which could form an ambipolar charging layer interfacing the underlying transistor channel through a tunneling barrier. This structure could enable the nonvolatile retention of charged carriers as well as the reversible modulation of polarity and amount of the trapped charge, ultimately resulting in multiple memory states with a broad range of binding energies.

These presented works provide nanofabrication and material processing solutions for making nanoelectronic devices based on emerging layered semiconductors, which can be generally utilized for making a broad range of functional devices based on various layered materials. Especially, the plasma doping method demonstrated in my research holds the potential to be further developed into an industrial material processing technology for precisely tailoring the band structures of TMDCs to achieve desirable characteristics for various device applications. In addition, the obtained device physics knowledge associated with MoS_2 and WSe_2-based multi-bit charge memory states is anticipated to greatly leverage the unique electronic and structural properties of layered semiconductors for scalable data storage and emerging analog computing applications.

6.2 Future Work

Our work shows that multiple charge-trapping states with large extrema spacing, long retention time, and quasi-analog tunability can be excited in the transistors made from mechanically-exfoliated few-layer WSe_2 flakes or plasma-doped MoS_2 flakes. Such charge-

trapping states could be further studied for making multi-bit or quasi-analog-tunable memory devices for emerging neuromorphic and analog-computing device applications. Due to the intrinsic nanoscale dimensions and superior electronic properties, these layered semiconductor materials could be investigated and exploited for device applications which emulate the functions of synapses and neurons with good plasticity, analog memory and spike signal processing capability. Furthermore, these electronic devices made from TMDC structures could be studied for making neuromorphic circuits, which could potentially be scaled up to emulate biological neural networks with parallel signal processing and low energy consumption.

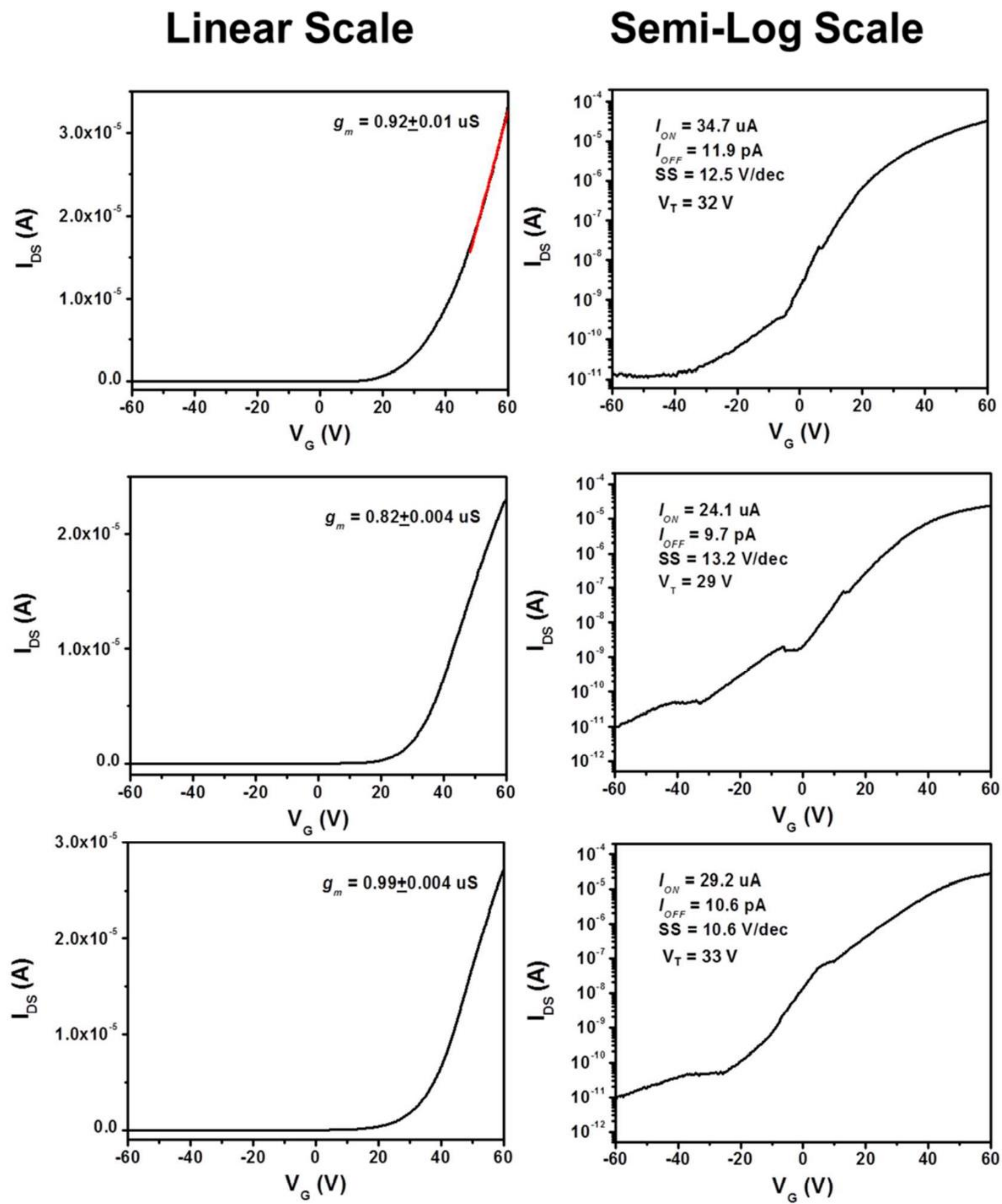
Another natural progression of our work would be to extend the application of our nanofabrication technology (*e.g.,* nanoimprint assisted shear exfoliation and plasma doping) to regular TMDCs as well as TMDC heterostructures. In our research, we frequently take MoS_2 and WSe_2 as exemplary TMDCs, as they share the similar structure properties with most atomically layered semiconductors. To generalize these fabrication methods developed based on MoS_2 and WSe_2 and apply them on other TMDCs, future work could focus on the process optimization with more experimental testing. In addition, for some practical device applications such as photovoltaics, diode and high electron mobility transistor (HEMT), TMDC heterostructures are highly desired. We expect our nanoimprint assisted fabrication method to be able to produce TMDC heterostructure via stacking different exfoliated TMDC flakes. Especially for array-to-array stacking, one area of study that could be performed is to improve the alignment accuracy and alignment efficiency. Another possible solution to produce heterostructure is to apply our plasma doping method to modify top TMDC layers, creating a junction in vertical direction. For this

process, future study will pursue the precise control of plasma dosage as well as doping depth, which determines the TMDC heterostructure dimensions.

Appendices

Appendix A

Transfer Characteristics of 45 NASE-Produced MoS_2 Field-Effect Transistors (FETs)



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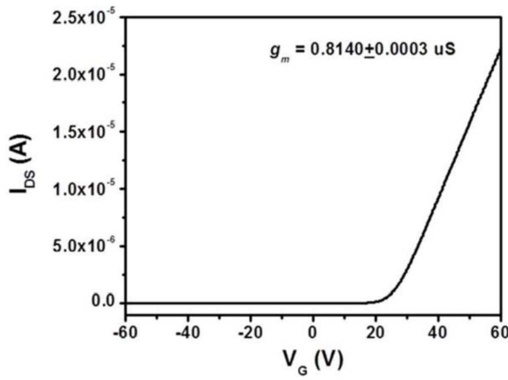

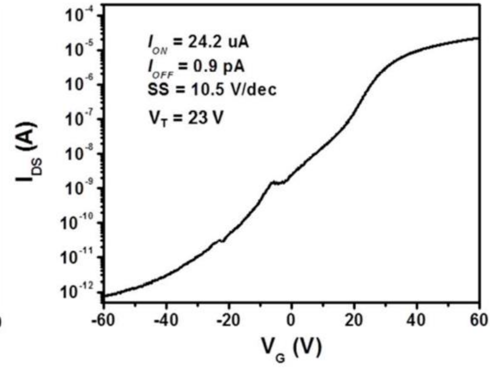

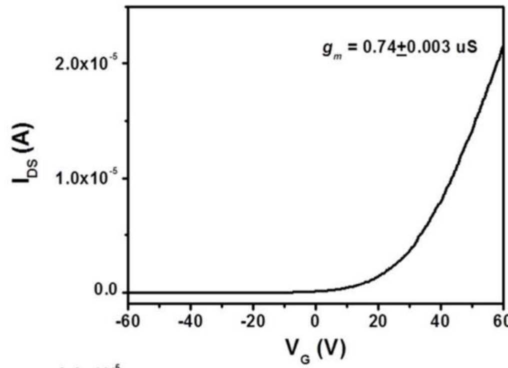

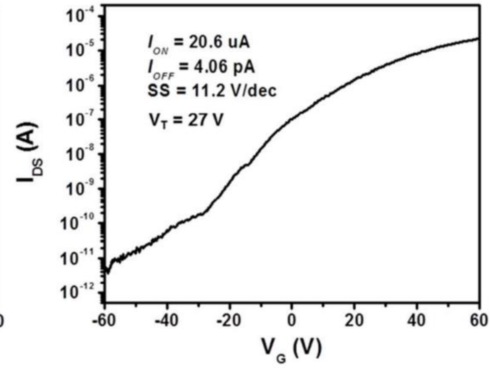

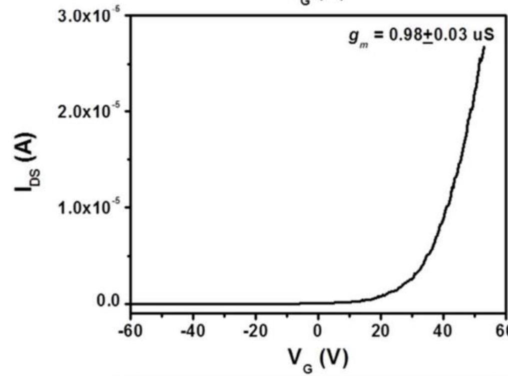

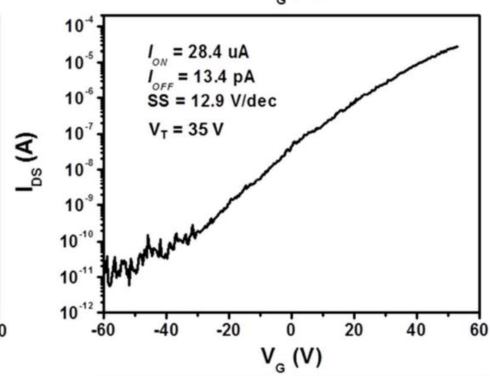

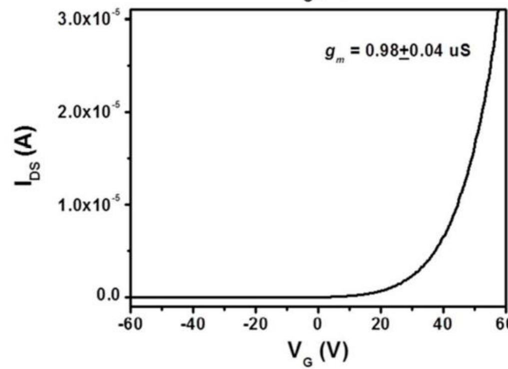

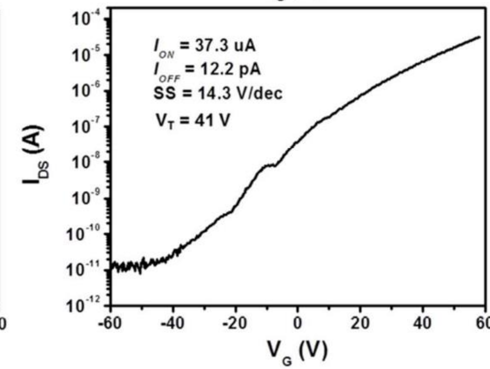

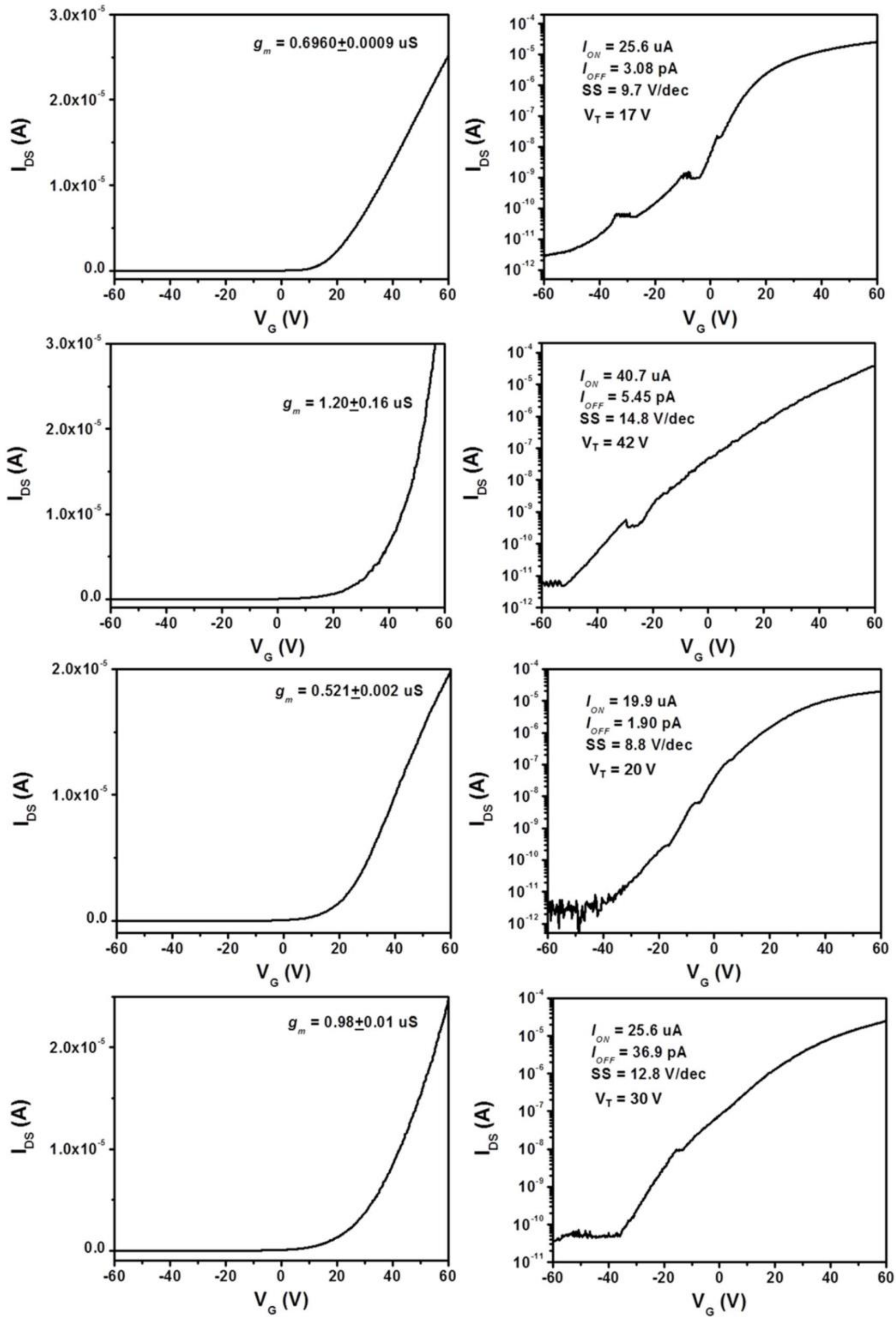
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I_ON = 25.6 uA
I_OFF = 3.08 pA
SS = 9.7 V/dec
V_T = 17 V
g_m = 1.20±0.16 uS
I_ON = 40.7 uA
I_OFF = 5.45 pA
SS = 14.8 V/dec
V_T = 42 V
g_m = 0.521±0.002 uS
I_ON = 19.9 uA
I_OFF = 1.90 pA
SS = 8.8 V/dec
V_T = 20 V
g_m = 0.98±0.01 uS
I_ON = 25.6 uA
I_OFF = 36.9 pA
SS = 12.8 V/dec
V_T = 30 V
I_DS (A)
V_G (V)

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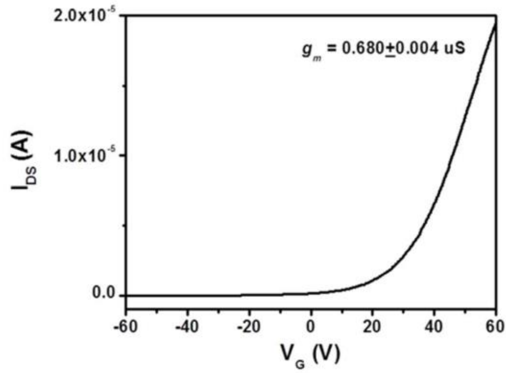

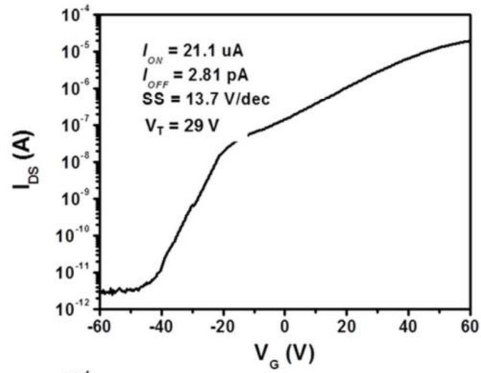

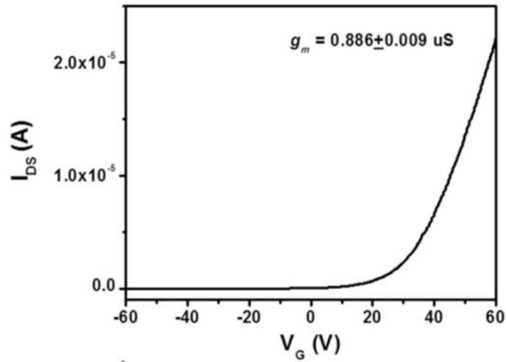

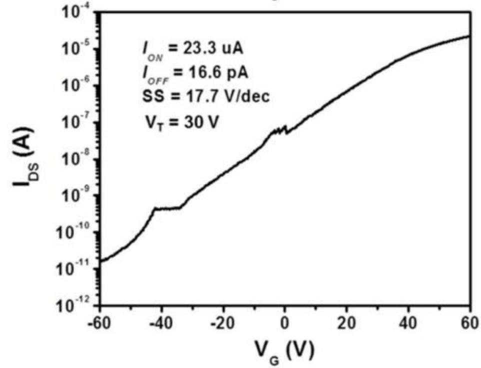

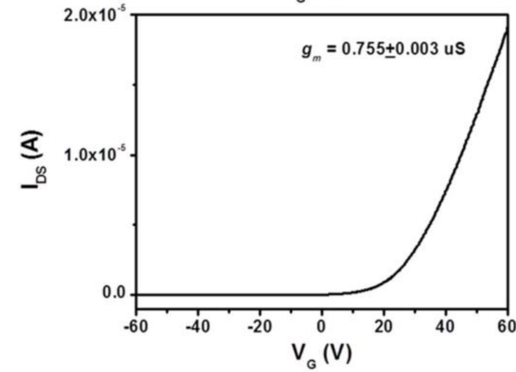

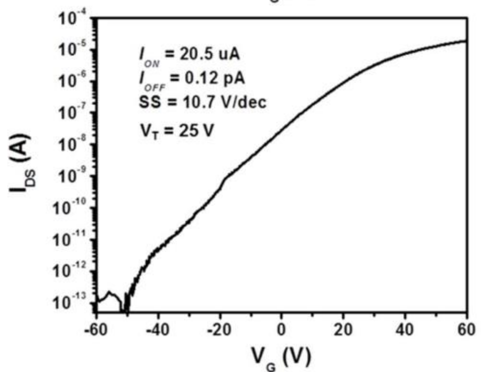

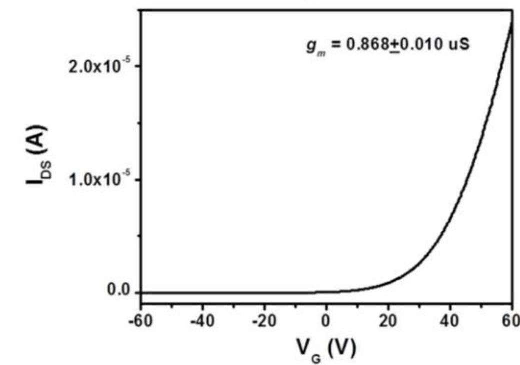

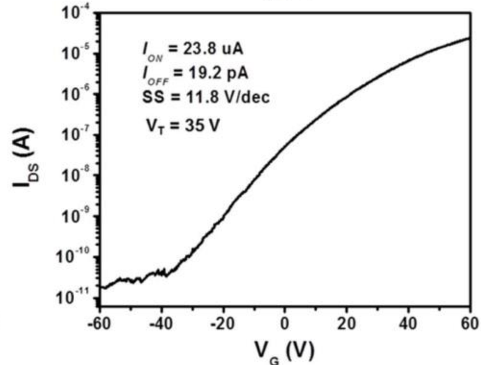

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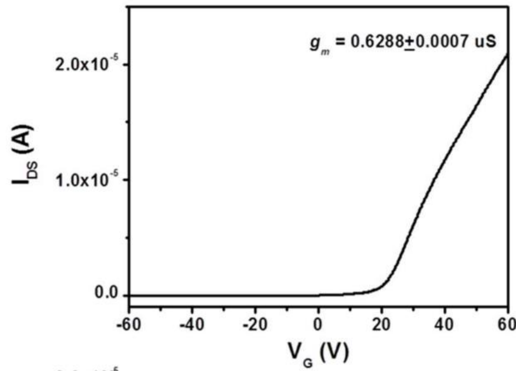

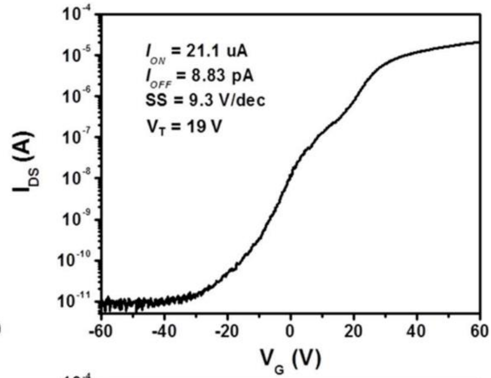

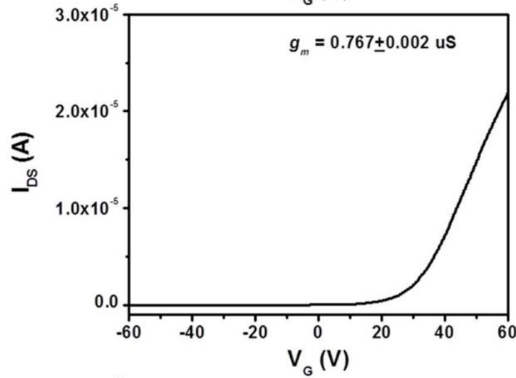

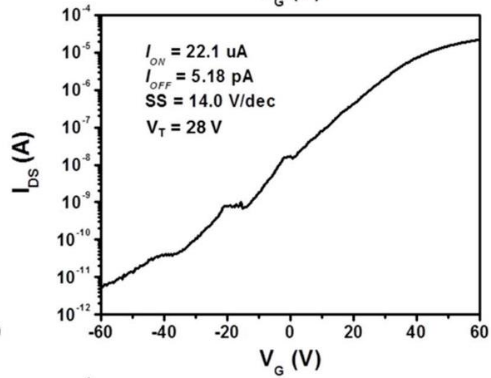

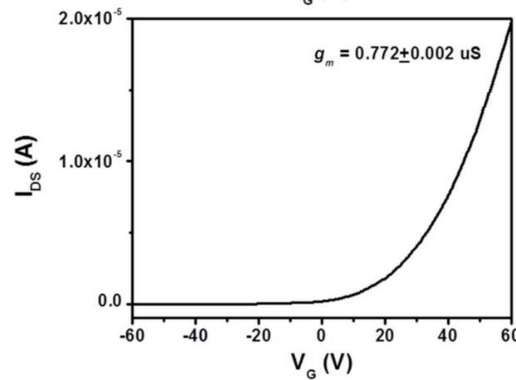

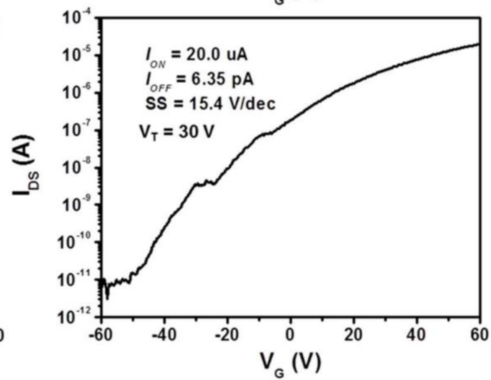

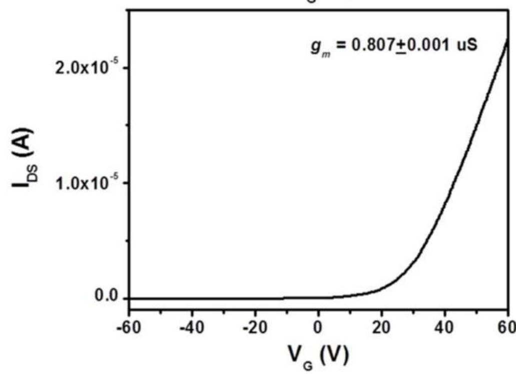

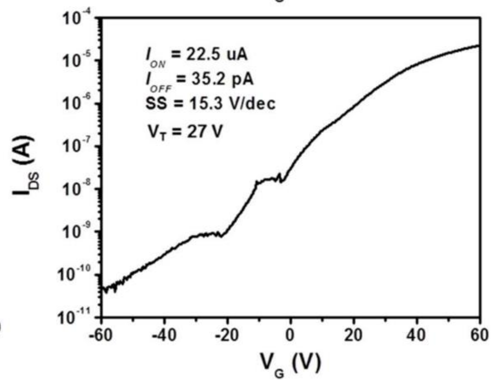

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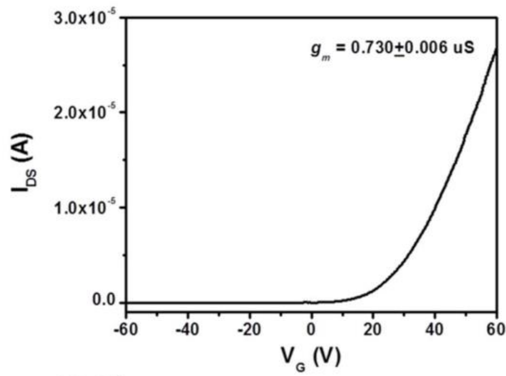
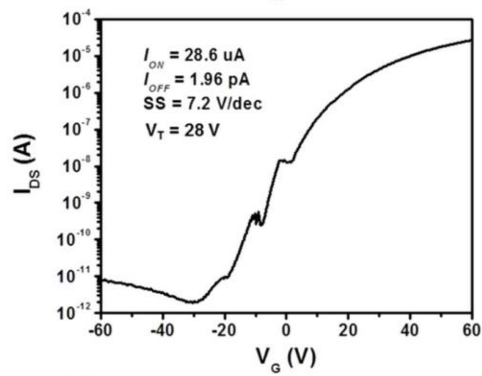
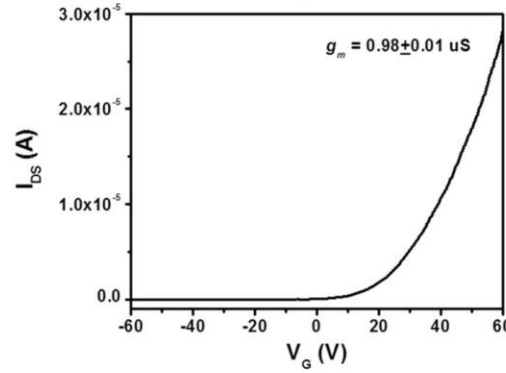
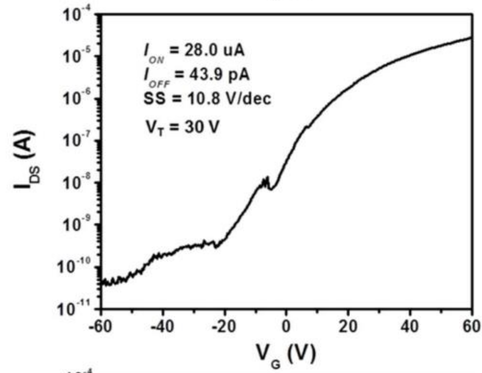
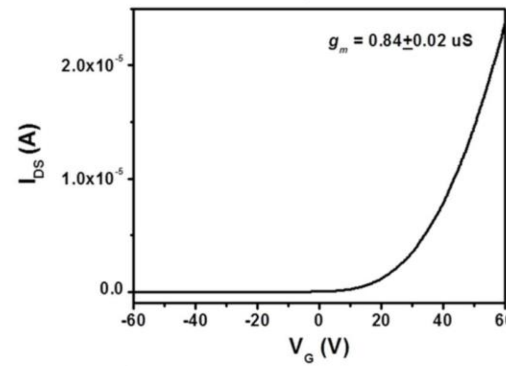
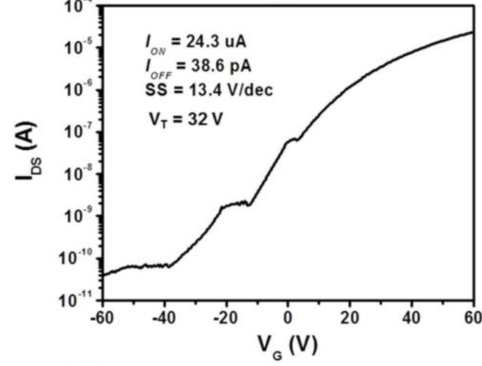


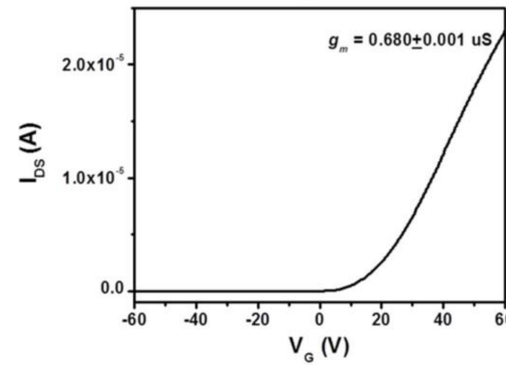


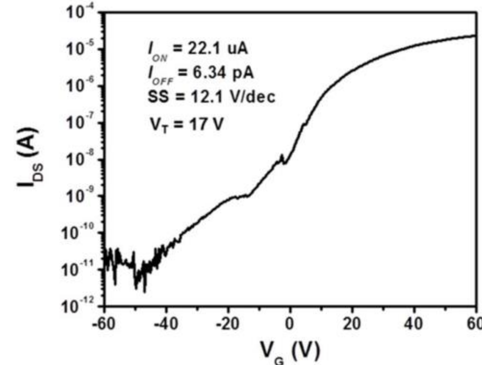


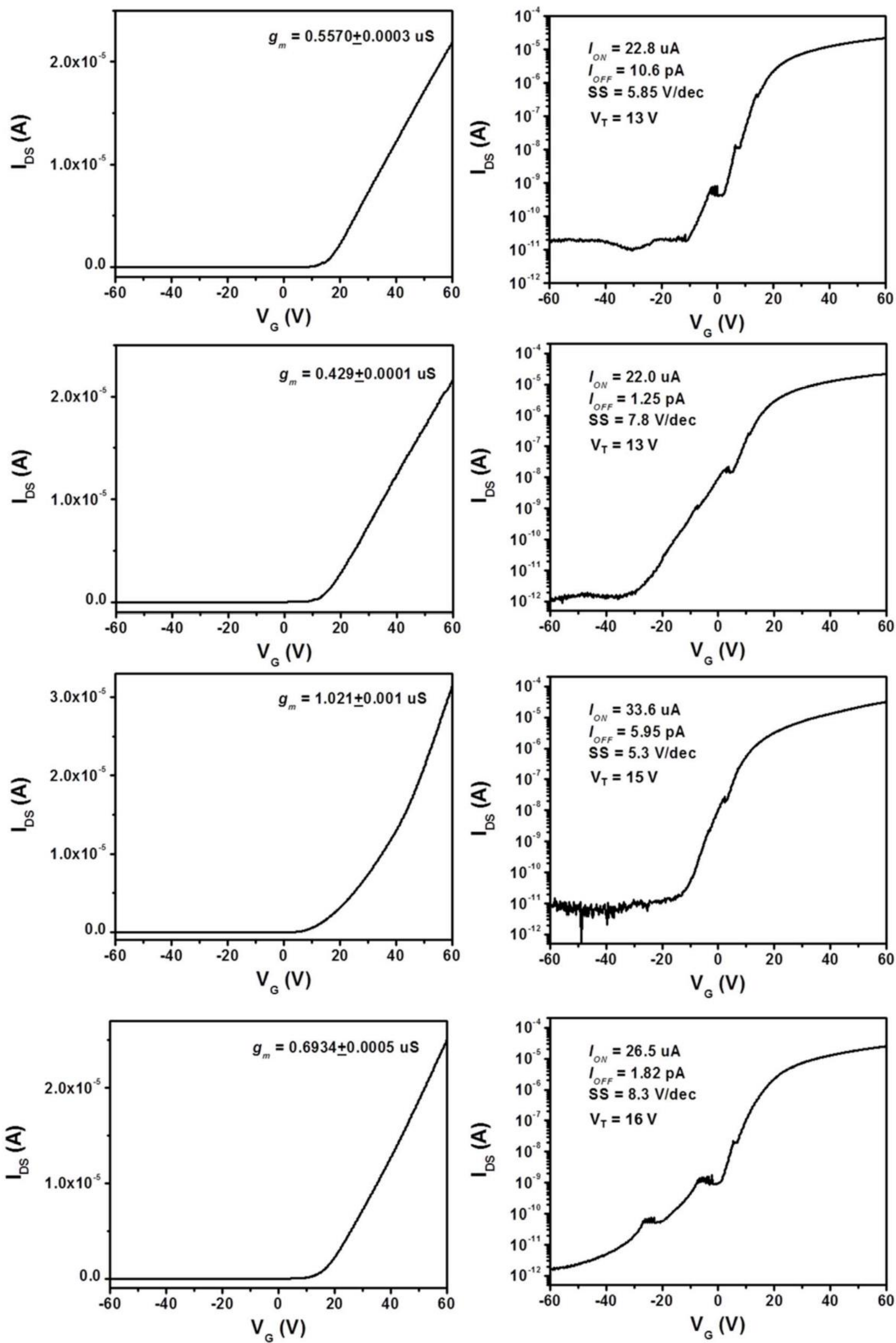




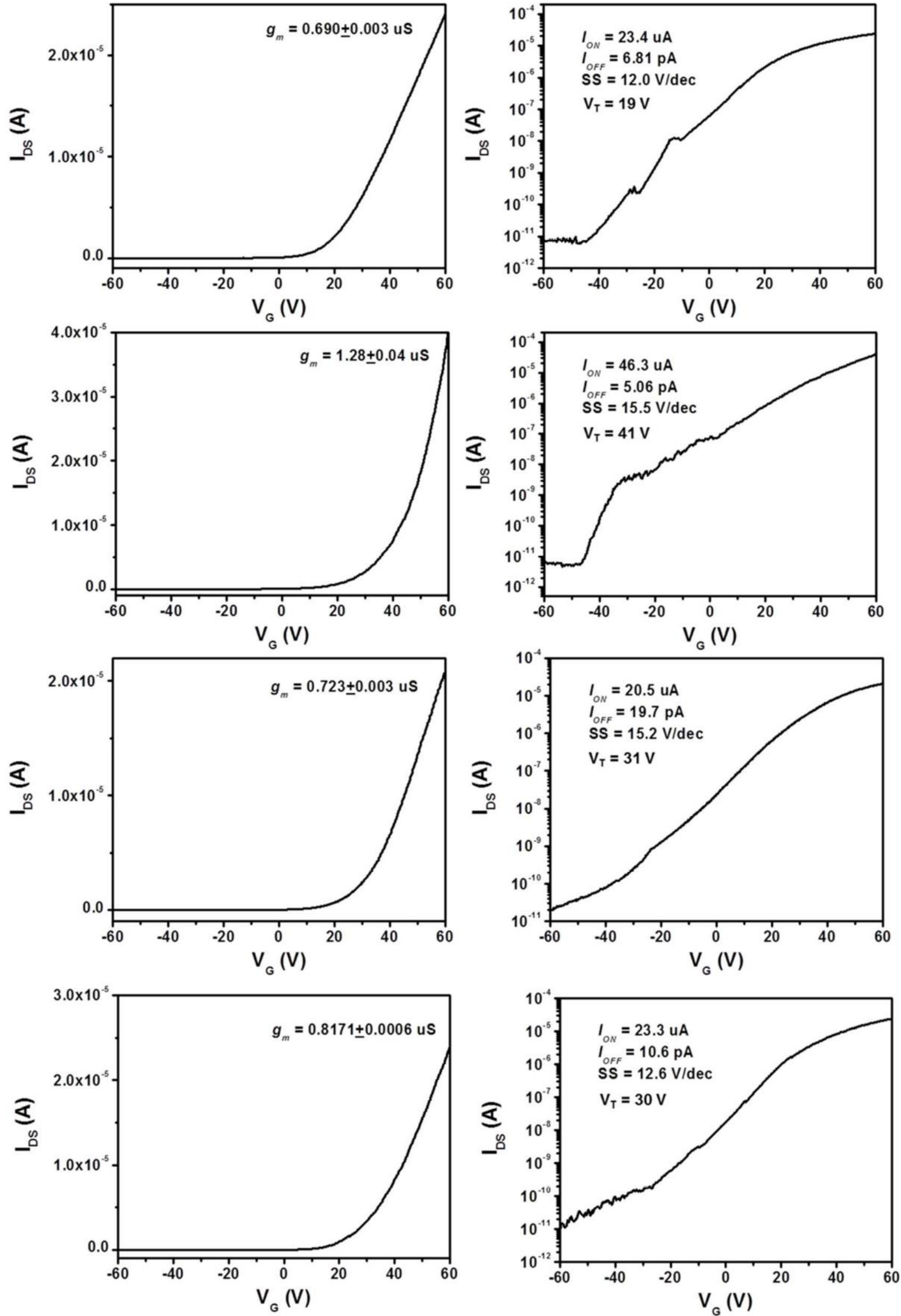








Linear Scale
Semi-Log Scale
g_m = 0.5570±0.0003 uS
I_ON = 22.8 uA
I_OFF = 10.6 pA
SS = 5.85 V/dec
V_T = 13 V
g_m = 0.429±0.0001 uS
I_ON = 22.0 uA
I_OFF = 1.25 pA
SS = 7.8 V/dec
V_T = 13 V
g_m = 1.021±0.001 uS
I_ON = 33.6 uA
I_OFF = 5.95 pA
SS = 5.3 V/dec
V_T = 15 V
g_m = 0.6934±0.0005 uS
I_ON = 26.5 uA
I_OFF = 1.82 pA
SS = 8.3 V/dec
V_T = 16 V
I_DS (A)
V_G (V)



Linear Scale
Semi-Log Scale
g_m = 0.690±0.003 uS
I_ON = 23.4 uA
I_OFF = 6.81 pA
SS = 12.0 V/dec
V_T = 19 V
g_m = 1.28±0.04 uS
I_ON = 46.3 uA
I_OFF = 5.06 pA
SS = 15.5 V/dec
V_T = 41 V
g_m = 0.723±0.003 uS
I_ON = 20.5 uA
I_OFF = 19.7 pA
SS = 15.2 V/dec
V_T = 31 V
g_m = 0.8171±0.0006 uS
I_ON = 23.3 uA
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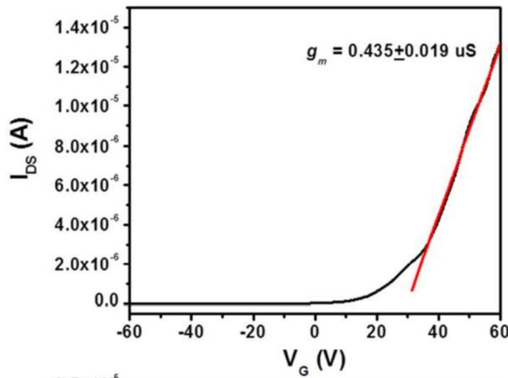
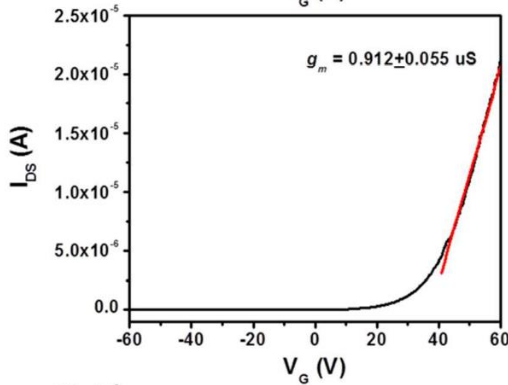
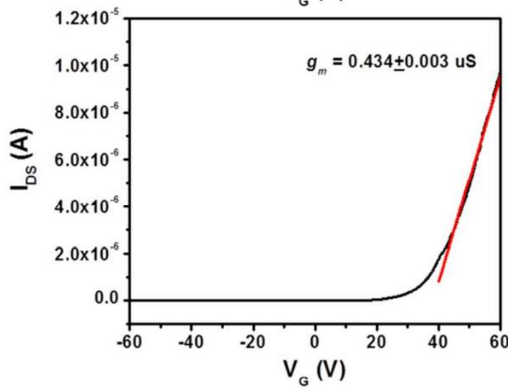
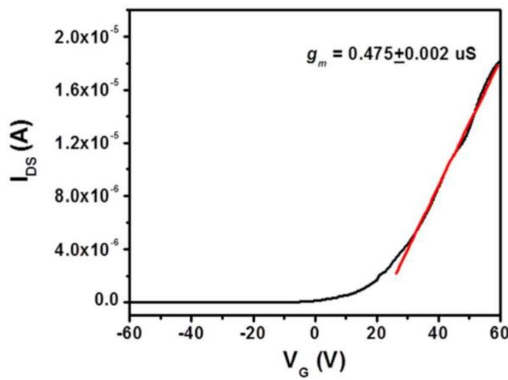
V_T = 30 V
I_DS (A)
V_G (V)

Linear Scale

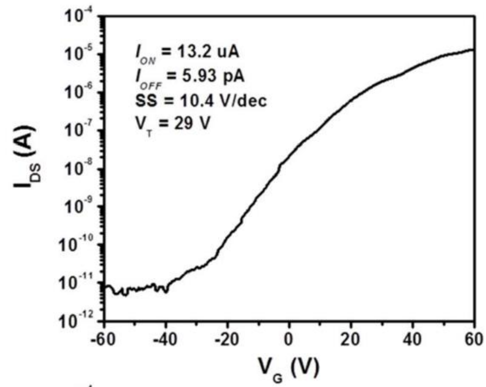


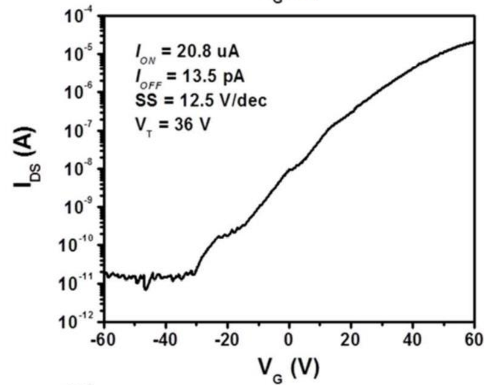


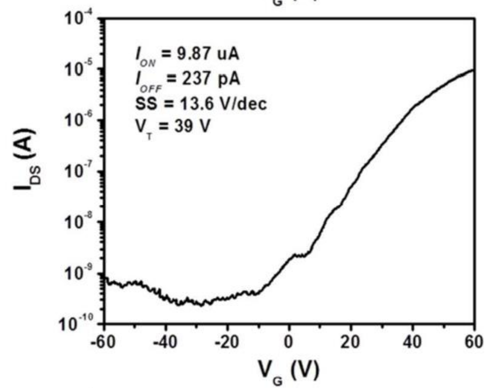


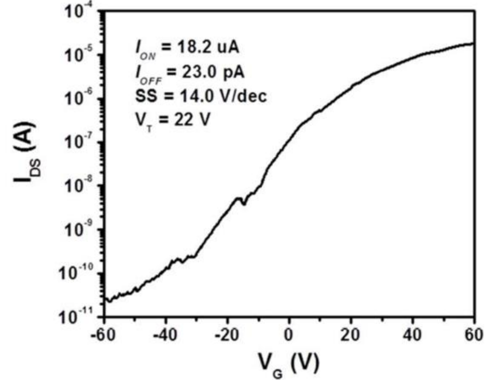


Semi-Log Scale

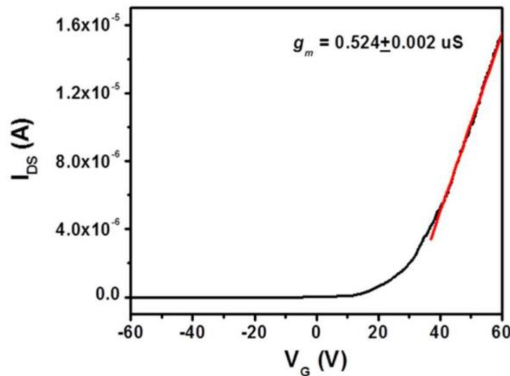


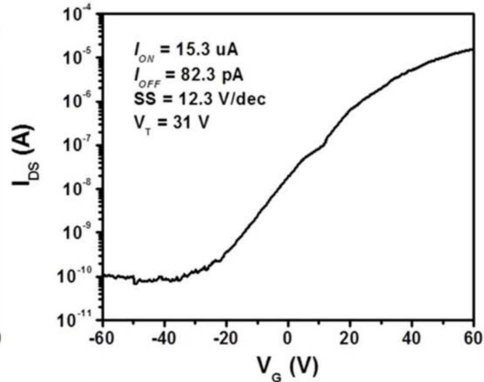


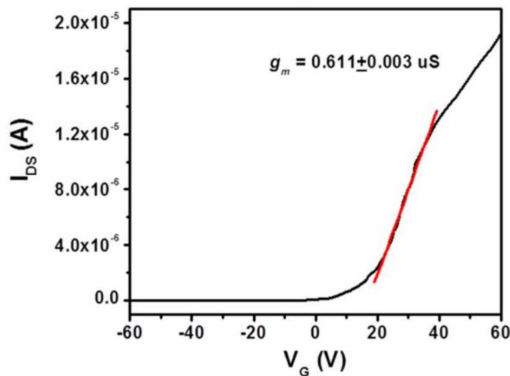


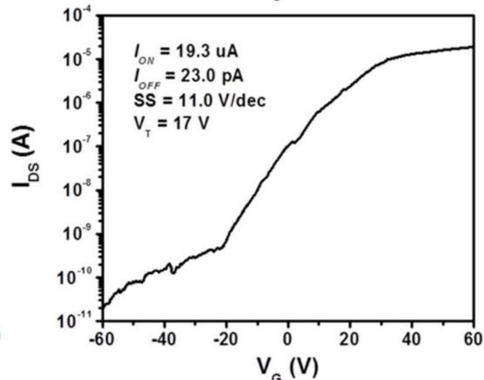


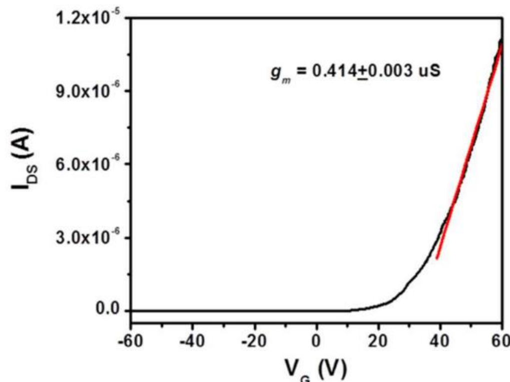
Linear Scale | **Semi-Log Scale**

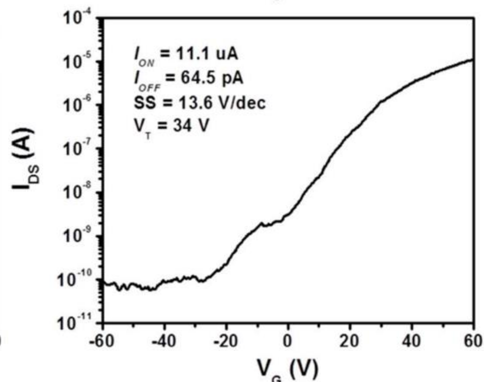


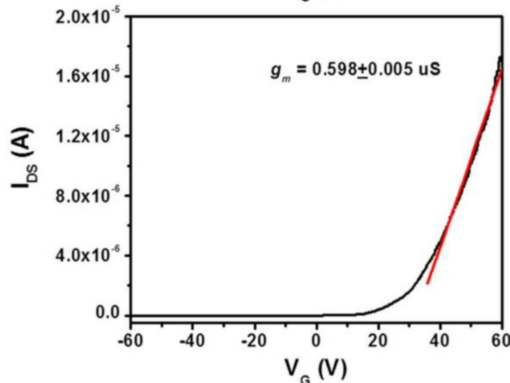


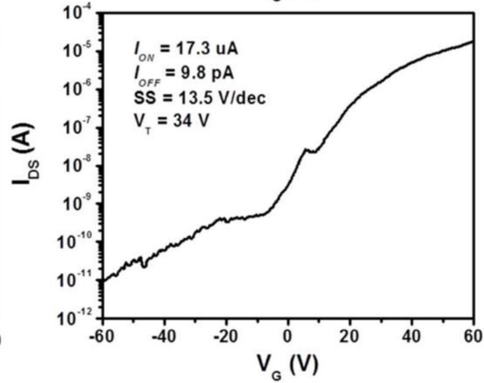




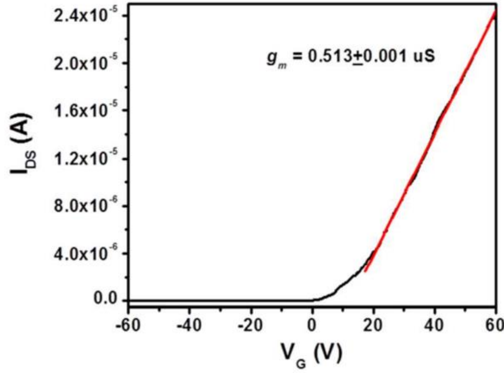


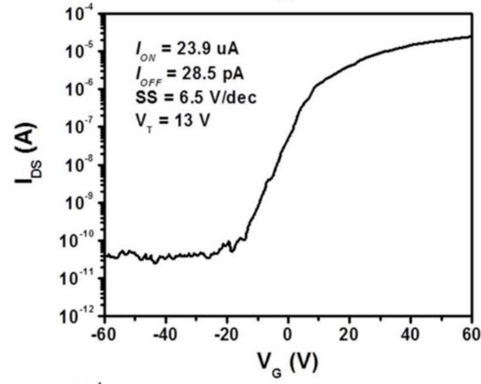


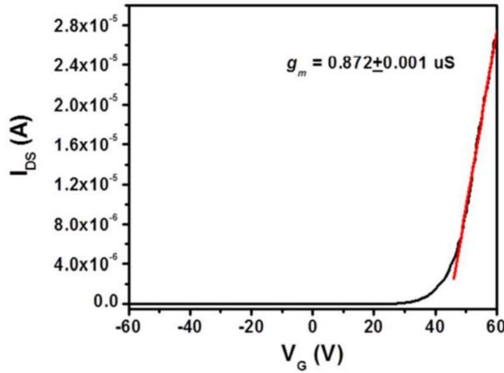


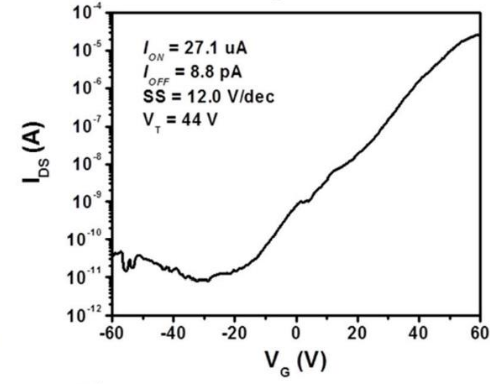


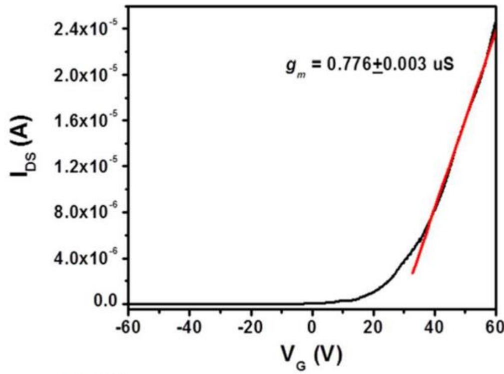
Linear Scale **Semi-Log Scale**

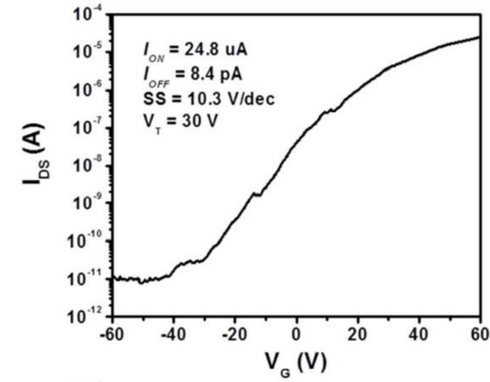


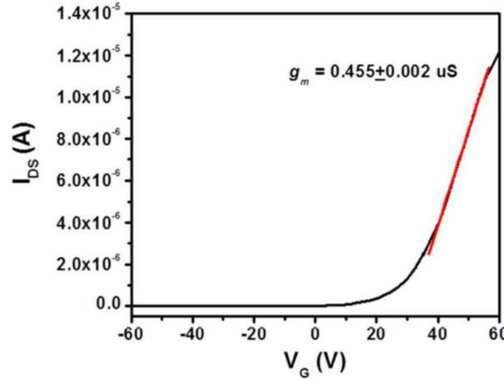


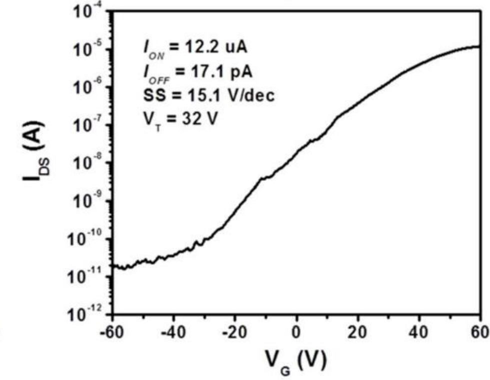












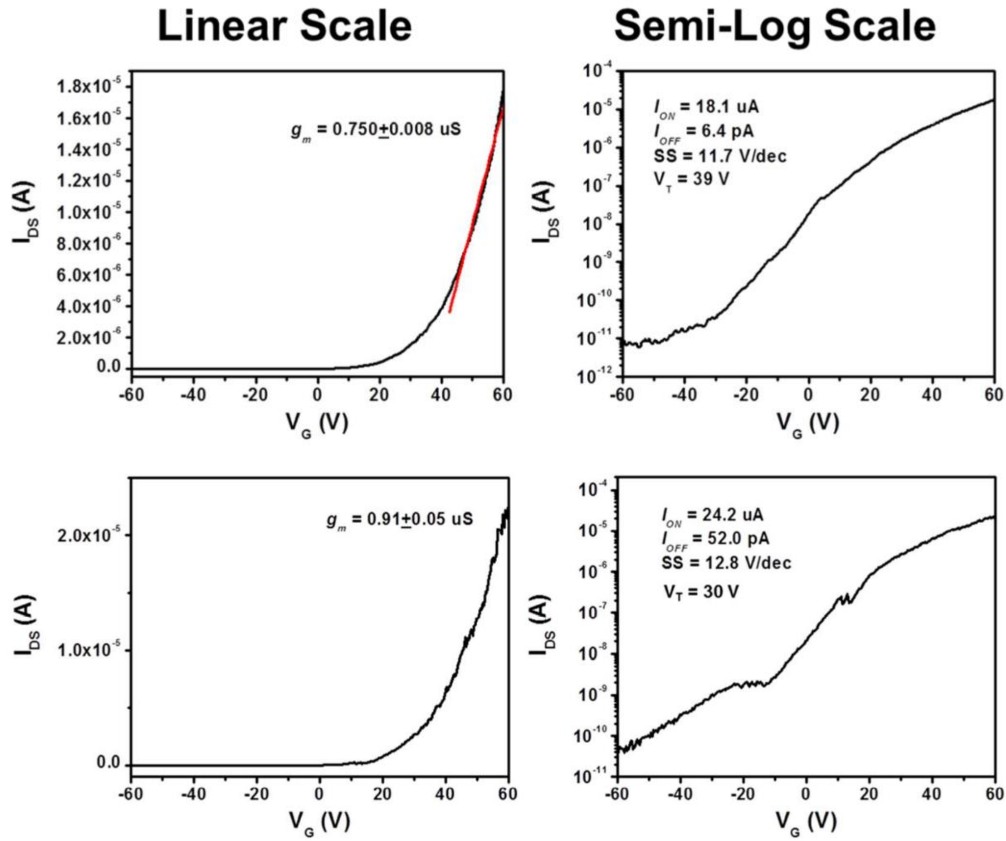


Figure A.1 Transfer characteristics of 45 back-gated field-effect transistors (FETs), which were made from the multilayer MoS_2 flakes (thickness ~20 nm) produced in a NASE process. For all FETs, the channel width and length are 15 and 10 µm, respectively; the back gate dielectric is 300 nm SiO_2 + residual PS (estimated to be thinner than 5 nm).

Appendix B

Discussion on Relationship between Flake Rigidity and Required Vertical Pressure

In our lab-made setup, two mechanical loads mainly contribute to the shear exfoliation of MoS_2 flakes: (1) a shear load generated by the roller and (2) a uniform pressure load generated by the vertical stage. The MoS_2 stamp is imprinted into the fixing layer on the substrate. The shear load is basically applied to the MoS_2 stamp in order to overcome the interlayer bond strength between MoS_2 flakes and subsequently slide one flake relative to the other, whereas the uniform pressure load is mainly responsible for avoiding the ripple formation in the MoS_2 flakes during the shear exfoliation process.

Ripples in the MoS_2 flakes that are induced by the shear load may lead to either crumpling the printed MoS_2 flakes or failing in the exfoliation of the MoS_2 flakes. To focus on the physical insight, here we simplify the system and apply a beam bulking model shown in Figure B.1.

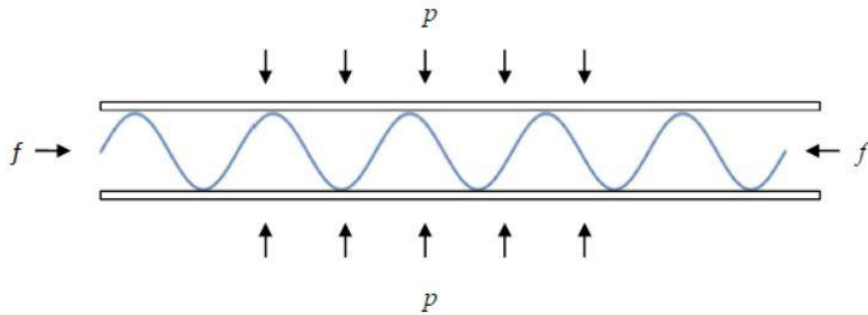


Figure B.1 The beam bulking model for analyzing the ripple formation in a NASE-produced MoS_2 flake.

The force f is the required shear load to cause exfoliation, which scales with the bond strength between layers. This shear load is passed to the layer of analysis by the edge of the fixing layer, which stops any motion of the part imprinted in the fixing layer. The pressure P is the applied pressure to suppress the ripple formation due to force f. The linear perturbation analysis is performed by considering a ripple of the form

$$v(x) = A\sin(\frac{2\pi x}{\lambda})$$

where A is the ripple amplitude and λ is the ripple wavelength. The free energy of the system per unit wavelength, g, is given by the bending energy of the layer and the potential of the applied force,

$$\lambda g = \int_0^\lambda \frac{EI}{2}(\frac{d^2v}{dx^2})^2 dx - f\int_0^\lambda \frac{1}{2}(\frac{dv}{dx})^2 dx - 2A(-p)\lambda$$

where the first term is the bending energy, where E is Young's modulus and I is the second moment of area scaling with t^4, where t is the flake thickness. The second term is the potential from f, where $\int_0^\lambda \frac{1}{2}(\frac{dv}{dx})^2 dx$ describes the shrinkage of length in the x direction due to the perturbation. The last term is the potential from p.

Substituting $v(x)$ into the above equation, we obtain

$$g = \frac{1}{4}(EI(\frac{2\pi}{\lambda})^4 - f(\frac{2\pi}{\lambda})^2)A^2 + 2pA$$

Take $\partial g/\partial\lambda = 0$ and $\partial g/\partial A = 0$, we obtain

$$p = \frac{f^2}{16EI}$$

Therefore, a TMDC material with a higher stiffness (*EI*) requires a smaller pressure for avoiding the ripple formation, while a TMDC material with larger interlayer bond strength requires a higher pressure for avoiding the ripple formation.

Appendix C

Setup Parameters for Density Functional Theory (DFT) Computation

Based on Format of ABINIT Code

To express the hexagonal lattice of a WSe_2 layer, the angles in degrees (parameter: angdeg) are set as 90 90 120.

To express the types of different atoms in WSe_2 layers, the number of the types of involved atoms (parameter: ntypat) is set to 2, and the types of atoms (parameter: typat) are set to 1 2 2 1 2 2.

To express the specific atoms in WSe_2 layers, the nuclear charges for two types of pseudopotentials are given in order as 74, 34.

To express the bilayer system, the numbers of atoms (parameter: natom) are set to 6, 3.

To determine segmentation of the reciprocal space, the K point boundaries (parameter: kptbounds) are set as below:

```
0      0      0      #gamma
1/3    1/3    0      #k
1/2    0      0      #M
1      1      1      #gamma
```

To total number of electronic bands (parameter: nband), *i.e.*, occupied and possibly unoccupied bands, for which the corresponding wavefunctions are computed along with eigenvalues, is set to 32.

To include the van der Waals exchange-correlation functional module, Parameter: vdw_cx is set to 1.

To control the self-consistency of the computation, the integer for self-consistent-field (SCF) cycles (parameter: iscf) is set to -2, which permits the computation of the eigenvalues of occupied and unoccupied states at arbitrary *k* states in the fixed self-consistent potential produced by the integration grid of *k* points. The maximal number of SCF cycles (parameter: nstep) is set to 60.

To evaluate the total energy convergence needed for obtaining reliable computation results, the Maximal kinetic energy cut-off (parameter: ecut), the unit cell lattice vector scaling (parameter: acell), and the number of grid points for K point generation (parameter: ngkpt) are tested independently to reach the minimum value of the total energy of the system. The final values are ecut = 28, Hartree, acell = 6.4 6.4 50 in Bohr, and ngkpt = 8 8 8.

To conduct the process of crystal relaxation, the distance between two twisted/displaced WSe_2 layers is calculated and expressed by the vectors of atom positions in Cartesian coordinates (parameter: xcart).

To express the relative displacement and rotation between two twisted WSe_2 layers, the Cartesian coordinates (parameter: xcart) of the individual atoms in a primitive cell are listed as below:

3.2000000000E+00 1.8475208614E+00 2.9796577439E+00

0 -1.3583012686E-

0 6.0951981795E+

2.8779558941E+00 1.8334601120E+00 1.7979657744E+01

6.2268009809 0.2718680021E+00 1.4864169870E+01

6.2268009809 0.2718680021E+00 2.1095198179E+01

By default, Parameter: xcart is given in terms of Bohr atomic units (1 Bohr=0.5291772108 Angstroms).

The Z-axis coordinates of individual atoms are initially based on the lattice parameters provided by the published reference [118], and they are finally determined by the relaxation results when the total energy of the system reaches the minimum value.

The X and Y-axis coordinates of individual atoms are also based on the lattice parameters provided by the same reference [118], with an interlayer rotation angle of 5°.

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