Theoretical investigation of the count rate capabilities of in-pixel amplifiers for photon counting arrays based on polycrystalline silicon TFTs

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ABSTRACT

Purpose:

Photon counting arrays (PCAs), capable of measuring the spectral information of individual x-ray photons and recording that information digitally, provide a number of advantages compared to conventional, energy-integrating active matrix flat-panel imagers – such as reducing the undesirable effects of electronic readout noise and Swank noise. While contemporary PCAs are based on crystalline silicon, our group has been examining the use of polycrystalline silicon (poly-Si, a semiconductor material better-suited for the manufacture of large-area devices) for such arrays. In this study, a theoretical investigation of the front-end amplifiers of array pixels incorporating photon counting circuits is described – building upon circuit simulation techniques developed in a previous study. Results for amplifier circuit designs corresponding to prototype PCAs currently under development, as well as for hypothetical circuit designs identified in the study, are reported. In the simulations, performance metrics (such as signal gain, linearity of signal response, and energy resolution) as well as various measures of count rate are determined.

Methods:

The simulations employed various input energy distributions (i.e., a 72 kVp spectrum as well as monoenergetic x rays) in order to determine circuit performance. To make the results representative of the properties of poly-Si, the simulations incorporated transistor characteristics that were empirically obtained from test devices. Optimal operating conditions for the circuits were determined by applying criteria to the performance metrics and identifying which conditions minimized settling time. Once the optimal operating conditions were identified, trains of input pulses simulating x-ray flux were used to determine two measures of count rate corresponding to dead time losses of 10% and 30% (referred to as CR_{10} and CR_{30}, respectively).

Results:

The best performing prototype amplifier design (implemented at a pixel pitch of 1 mm) exhibited CR_{10} and CR_{30} values (expressed in counts per second per pixel) of 8.4 and 21.6 kcps/pixel, respectively. A hypothetical amplifier design was derived by modifying transistor, resistor, and capacitor elements of the prototype amplifier designs. This hypothetical design (implemented at a pitch of 1 mm) exhibited CR_{10} and CR_{30} values of 154 and 381 kcps/pixel, respectively. When implemented at a pitch of 0.25 mm, the performance of that design increased to 210 and 491 kcps/pixel, respectively (corresponding to counts per second per unit area of 3.4 and 7.9 Mcps/mm^2).

Conclusions:

The simulation methodology described in this paper represents a useful tool for identifying promising designs for the amplifier component of photon counting arrays, as well as evaluating the analog signal and noise performance of those designs. The results obtained from the current study support the hypothesis that large-area, photon counting arrays based on poly-Si transistors can provide clinically useful count rates. Encouraged by these early results, further development of the methodology to assist in the identification and evaluation of even more promising designs, along with development and empirical characterization of prototype designs, is planned.

Key words: photon counting arrays, count rate, polycrystalline silicon thin-film transistors, circuit simulations, medical x-ray imaging

I. Introduction

In the 120 years following Roentgen's seminal discovery of x rays, x-ray image sensors have continued to evolve into ever more valuable tools for medical screening, diagnosis and intervention, as well as for radiotherapy treatment guidance. The most common form of x-ray imaging is energy-integration whereby the total energy deposited by the incident beam is collected to form one or more projection images (e.g., for radiography or fluoroscopy) or a volumetric image set (e.g., for digital breast tomosynthesis or cone-beam CT). Currently, such imaging is commonly performed with active matrix flat-panel imagers (AMFPIs). An AMFPI is based on a "backplane" coupled to some form of x-ray converter material such as CsI:Tl (which generates x-ray induced signal in the form of optical photons) or a-Se (which generates signal in the form of electron-hole pairs). The backplane consists of a 2D array of pixels containing circuits made of hydrogenated amorphous silicon (a-Si:H).[1,2] This thin-film semiconductor material is notable by virtue of the fact that it lends itself to the creation of large-area, monolithic devices of a size commensurate with that of human anatomy – with current arrays as large as ~43×43 cm[2,3]. Devices made from a-Si:H also exhibit a very high degree of radiation damage resistance [4,5] and each array pixel typically consists of a single thin-film transistor (TFT) connected to some form of pixel storage capacitor. When x-rays are delivered during an image frame, the total energy absorbed in each pixel is integrated and stored in the pixel capacitor – and later read out via addressing lines to produce an output image.

A different form of x-ray imaging, called photon counting, uses far more complex in-pixel circuitry to measure and record information about the amount of signal generated in the converter by each interacting x ray (referred to as an *event*). In the case of a relatively simple pixel circuit, the x-ray

induced signal is amplified, shaped, compared to a threshold (whose value is set by the user) and, depending on the outcome of that comparison, the tally in a digital counter of events for that pixel is incremented by one unit. Increasingly complex pixel circuits can include more thresholds and counters. Highly specialized features can also be introduced such as the ability to sense, and partially compensate for occurrences in which signal from a single event is deposited across several adjacent pixels.[6-8]

Photon counting detectors offer a number of advantages.[9-11] By virtue of the nature of their binary recording of events per pixel, photon counting detectors offer the potential to diminish the contrast-reducing effects caused by electronic readout noise and Swank noise [12] in energy-integration detectors. This binary nature can help to overcome another problem with energy-integrating detectors – that lower energy x rays provide higher contrast but less signal per event than higher energy x rays, reducing overall image contrast.[10] In addition, multiple thresholds and counters in the pixel circuit allow events to be separated into multiple bins based on signal size – providing a degree of separation of the spectral components of the x-ray beam transmitted through the patient. Such advantages and capabilities offer the possibility of dose reduction.[10,13] Features such as those discussed above have been incorporated into photon counting detectors for mammography and conventional (i.e., fan-beam) CT to facilitate advanced imaging techniques such as dual-energy imaging,[14] material decomposition in CT [15,16] and K-edge imaging.[17,18]

While a large-area, monolithic, photon counting imager that also demonstrates high radiation damage resistance would be desirable, this will require development of a backplane containing the necessary photon-counting pixel circuits, which is the focus of this paper. Outside of the scope of the present study but also essential, is an x-ray converter offering suitably high x-ray quantum efficiency and sensitivity, and sufficiently prompt signal response time. Converters based on cadmium telluride (CdTe) or cadmium zinc telluride (CZT) have such favorable properties and are used in photon counting detectors for CT. Presently, while CZT detectors are relatively small in size and costly, methods to reduce defects and improve purity (problems which constrain the size and contribute toward the expense of large-size, detector-grade crystals) are under investigation.[19-21] Other efforts to develop converters for photon-counting, based on materials which lend themselves to large area deposition (i.e., a-Se and poly-perovskite), have been reported.[22-24]

Given its demonstrated role in enabling the creation of large area, monolithic AMFPI backplanes, a-Si:H would be a candidate for photon counting circuits. Unfortunately, a-Si:H has electron and hole

mobilities that are simply too low (~1 and 10^{-2} cm^2/V-s, respectively) to allow creation of the complex circuitry required for photon counting circuits. Although contemporary photon counting imager technologies [14,15,18,25-37] employ crystalline silicon (c-Si), which has electron and hole mobilities of ~1000 cm^2/V-s, c-Si is not well-suited to fabrication of very large-area, monolithic arrays and is relatively susceptible to radiation damage. An alternative to both of these materials is polycrystalline silicon (poly-Si) produced through low-temperature, laser-annealing techniques.[38] This form of poly-Si, which has been extensively developed for the display industry, utilizes a thin-film process that allows the creation of large-area devices. The material also exhibits good radiation damage resistance [39] and provides electron and hole mobilities on the order of 100 cm^2/V-s – two and four orders of magnitude greater than those of a-Si:H, respectively, and within an order of magnitude of that of c-Si.

For these reasons, our group has been examining the possibility of photon counting arrays (PCAs) based on poly-Si TFTs. In the spirit of exploring the potential development of poly-Si photon counting arrays for use at fluoroscopic and radiographic x-ray energies, a number of early prototype poly-Si PCAs have been designed and fabricated,[40] and are currently undergoing characterization. A pixel pitch of 1 mm was chosen to reduce the number of challenges in the design of these initial prototype arrays.[41] The pixel circuit architecture of these prototype arrays is comprised of the four components schematically illustrated in Fig. 1: an amplifier, comparator, clock generator, and counter – with several designs for each component. A recent theoretical study investigated photon counting metrics such as energy resolution and count rate for the components used in those prototype arrays.[41] That study also performed an initial exploration of the minimum pixel pitch that could be achieved for such arrays. Count rate, in particular, is an important metric since it determines the capability of PCA circuits to handle the x-ray fluence encountered in a given application. For example, the estimated input x-ray flux for radiographic and fluoroscopic procedures (expressed in units of counts per second [cps] per unit detection area) is in the range of 1 to 50 Mcps/mm^2.[42] In the previous theoretical study, the highest count rates of the latter three components of the circuit design (i.e., the comparator, clock generator, and counter) were determined to be sufficient for these procedures, although the count rate of the amplifier component was not examined. The amplifier, however, is of definite interest since, as the first component in the signal chain, the degree to which its count rate performance can be maximized influences design decisions affecting subsequent pixel circuit components.

In the present study, the count rate capabilities of amplifiers suitable for PCA pixel circuits, based on poly-Si TFTs, are investigated at x-ray energies representative of those encountered in radiography and

fluoroscopy. To this end, circuit simulation was used to estimate count rate for amplifier circuits in photon counting pixels and used to explore the effects of a wide range of circuit design variables on amplifier count rate.

II. Methods

IIa. Overview

Circuit simulations were performed to examine the count rate performance of the amplifier circuit designs incorporated in the pixels of the previously mentioned prototype poly-Si photon counting arrays.[40] In addition, hypothetical variations of those prototype amplifier designs that provide higher count rates, while maintaining or improving signal gain, linearity of signal response and energy resolution, were identified and investigated.

The simulations employed the Eldo SPICE circuit simulation software package (Mentor Graphics, OR). In the simulations, the transistors were modeled using version 2 of the RPI poly-Si TFT model [43] and, to make the results representative of the properties of low-temperature poly-Si, the model card parameters required for the TFT model were the same empirically-determined values used for the "standard" transistors in the earlier theoretical study [41] – including electron and hole mobilities of 134.5 and 78.1 cm^2/V-s, respectively.

In the present study, each signal input to an amplifier circuit was assumed to be generated by an x ray depositing all of its energy in a direct detection x-ray converter in the form of a 500 µm thick CZT detector – equivalent to the assumption of perfect quantum efficiency and ignoring all detector effects except photoelectric absorption.[41] The energy distribution of these x rays was assumed to take one of three forms: 70 keV monoenergetic x rays, 1 to 200 keV monoenergetic x rays, and an x-ray spectrum (obtained from a 72 kVp beam with a W target and 21 mm of Al filtration) giving the same half-value-layer as the RQA5 spectrum in IEC 61267. This spectrum is representative of the type of x-ray energy distribution encountered in radiographic and fluoroscopic applications. The assumed CZT thickness of 500 µm is sufficient to convert ~92% of the incident radiation for the 72 kVp spectrum [44] – an efficiency comparable to that offered by other types of converters used in various forms of projection x-ray imaging. Each signal input to the amplifier circuit took the form of an *input pulse* with a height corresponding to an x-ray energy sampled from one of these distributions – resulting in the generation of an *amplifier output response*.

IIb. Determination of Energy Resolution

Energy resolution for a given amplifier circuit design was calculated in the manner reported in reference 41 using the equation:

$$\Delta E = \frac{E_{noise} \times 2.35}{E_{in}} \times 100\% \qquad\qquad [1]$$

where E_{in} is the energy of the input x ray (70 keV). For a given amplifier design, E_{noise} is the equivalent input noise of that design, in units of keV, and is calculated through division of E_{in} by the signal-to-noise ratio of the amplifier. The signal-to-noise ratio of the amplifier is calculated by dividing the amplifier output response by the intrinsic noise associated with the TFTs present in that circuit. The noise contribution from each TFT was obtained through simulations (performed in the frequency domain) employing the following equation for the noise power spectral density associated with TFT flicker noise:

$$S_{v-flicker}(f) = \frac{k_f}{C_{ox}^2 WLf}. \qquad (V^2/Hz) \qquad\qquad [2]$$

In this equation, k_f is the flicker noise constant (empirically determined to be 4.5×10^{-25} and 7.6×10^{-25} C^2/m^2 for n-type and p-type TFTs, respectively), C_{ox} is the gate oxide capacitance (0.345 fF/µm^2), W and L are the width and length dimensions of the TFT gate, and f is frequency in Hz.[41]

The amplifier output response used in the calculation of energy resolution was the signal response of the amplifier circuit to an input pulse corresponding to a 70 keV x ray. Circuit simulations of signal response were performed in the temporal domain – as described in the next section.

IIc. Determination of Count Rate and Energy Response Profile

In the earlier theoretical study,[41] the signal response of the amplifier was examined via circuit simulations performed in the frequency domain. However, detailed investigation of the count rate performance of amplifier circuit designs necessitates examination of signal response over time. For that reason, all simulations of signal response in this study were performed in the temporal domain using the adaptive time step feature of the Eldo package. In addition, knowledge of the amplifier output response as a function of incident x-ray energy is also required and was obtained through 200 simulations. In each of those simulations, a single input pulse corresponding to a 1 to 200 keV monoenergetic x ray was used to obtain an output response. The resulting plot of amplifier output response versus incident x-ray energy constitutes the calibration curve used to set the threshold in the determination of count rate.

In order to quantify the count rate capabilities for a given amplifier circuit, trains of pulses were input to the circuit and detailed information generated by the simulations about the response of the circuit to that input was extracted and analyzed. (This is the equivalent of empirically probing the signal operation of an actual amplifier circuit, then performing off-line analysis of the measured data.)

A total of 10,000 current pulses, randomly generated over a time period, formed the input pulse train. The input pulses (each having a 20 ns rise time and an 80 ns fall time)[45] had a pulse height distribution that corresponded to the 72 kVp spectrum. In the simulations, the input flux for this pulse train (expressed in counts per second per pixel) was varied from 1 to 2000 kcps/pixel by varying the time period over which the 10,000 pulses were input to the amplifier circuit from 10 s to 5 ms.

Once the simulations described above were performed, the count rate for a given amplifier circuit was determined by taking the ratio of the number of times the amplifier output response exceeded a selected voltage level to the duration of the input pulse train (i.e., 5 ms to 10 s). Using the calibration curve, that voltage level was chosen to correspond to an energy threshold of 19.5 keV – so as to allow the entire 72 kVp spectrum (which has a minimum x-ray energy of ~20 keV) to contribute to the count rate.

From the values of count rate obtained from the simulations, two specific measures of count rate were determined for each amplifier circuit design. The measures are referred to as CR_{10} and CR_{30} and correspond to the rates obtained when 10% and 30% of the input flux fail to be counted due to dead time loss. (Dead time refers to the time period after one or more input pulses when the amplifier circuit observes the next input pulse as part of the last detected pulse due to pulse pile-up.)[46]

The simulation methodology described above was also used to determine *energy response profiles* for each amplifier circuit design – providing a means to visualize how accurately a given design reproduces the input energy distribution. Energy response profiles were determined for two input energy distributions – the 72 kVp spectrum and 70 keV monoenergetic x rays. For a given input energy distribution, the energy response profiles were obtained through simulations in which the energy threshold applied to the amplifier output response was increased in 1 keV steps from 19.5 up to 199.5 keV. For a given threshold, the number of times the amplifier output response exceeded that threshold was tallied. A histogram of the differences of the tallies for consecutive thresholds formed the energy response profile.

IId. Definition of Performance Metrics and Optimal Operating Conditions

Simulations were performed to investigate the following *performance metrics* of the various amplifier circuit designs examined in this study: (i) the magnitude of the amplifier output response generated by an input pulse corresponding to a 70 keV x ray; (ii) the degree of non-linearity of the amplifier output response over the input signal range of interest in this study (i.e., from 20 to 100 keV); (iii) the energy resolution; and (iv) the *settling time* of that circuit in response to an input pulse corresponding to a 70 keV x ray. Following the convention described in reference 47, non-linearity was calculated by finding the maximum deviation of the amplifier output response from a straight line connecting the amplifier output response at 20 keV to the response at 100 keV. For a given case, the degree of non-linearity is expressed as a percentage and was calculated by dividing the maximum deviation from that line by the maximum value of the line (i.e., by the response at 100 keV). Energy resolution was determined using the methodology described in Sec. IIb. In addition, settling time is defined as the time required after an input pulse for the amplifier output response to essentially return to its baseline condition – i.e., return to and stay within 1% of its peak – as illustrated in Fig. 2. Shorter settling times are generally associated with higher count rates since they allow the amplifier circuit to resolve more input pulses.

For a given amplifier circuit design, performance metrics (i) through (iv) and, ultimately, count rate, are strongly affected by the values of the bias voltages applied to each amplifier stage. The values of these voltages (V_{AGC}, V_B and V_{CG}, shown in Fig. 3e) are collectively referred to as the *operating conditions* of the circuit. In the study, these voltage values were systematically varied so as to identify the *optimal operating conditions* – defined as that set of values which minimized settling time as well as satisfied a pair of criteria related to performance metrics (i) and (ii). For the first criterion, in order to ensure that the amplifier output response is sufficiently large so as to be well above the noise floor of the subsequent component in the pixel circuit (i.e., the comparator), a minimum response of 1.25 V was required – consistent with a similar criterion used in the earlier theoretical study of prototype amplifier designs.[41] For the second criterion, the deviation of the amplifier output response from linear behavior was required to be no larger than 10%.

IIe. Amplifier Designs

The names and technical descriptions of the amplifier circuit designs examined in this study are summarized in Table I and the circuit diagrams for those designs, all of which employ a 3-stage architecture, are illustrated in Fig. 3.

Designs SPC1-amp1 and SPC1-amp2 are 1st order and 2nd order bandpass circuit designs that correspond to the prototype amplifier designs [40] and are illustrated in Figs. 3a and 3b, respectively. Design New-amp-a is a hypothetical, 3rd order bandpass variation of the first two circuit designs and is illustrated in Fig. 3c. These three designs were assumed to be incorporated in a pixel with a pitch of 1 mm – i.e., the same as that of the prototype arrays.[40] Design New-amp-b also corresponds to the circuit diagram in Fig. 3c, but was assumed to be incorporated in a pixel with a pitch of 0.25 mm – resulting in a decrease in C_1, the capacitance of the CZT detector (see Fig. 3d). The choice of this pitch was motivated by a previous study which estimated that, through layout optimization as well as progressive improvement in the manufacture of poly-Si circuits, the pixel pitch of the prototype arrays could potentially be reduced to 0.25 mm.[41] This pitch approaches those used in radiographic and fluoroscopic applications.

The transistor dimensions, resistance values and capacitance values corresponding to the various TFTs, resistors and capacitors appearing in the circuit diagrams of Fig. 3 are given in Table II. In the case of SPC1-amp1 and SPC1-amp2, these values are the nominal specifications used in the design and layout of those prototype amplifier designs. The values of parasitic capacitance C_P appearing in the table are estimates based on the area of overlap between the CZT detector and underlying metal wires in the pixel circuit, as well as the dielectric constant and assumed thickness of the passivation layer that separates the detector and wires. In the case of New-amp-a and New-amp-b, the values appearing in the table for these hypothetical amplifier designs were determined as described in the next section.

III. Results

IIIa. Simulation Results for Performance Metrics

Table III shows the values of the optimal operating conditions for SPC1-amp1 and SPC1-amp2, identified through simulations, along with the corresponding values of performance metrics. In the simulations, V_{AGC} was varied from 0 to 6 V in 0.1 V steps, V_B was varied from 0 to 6 V in 0.25 V steps, and V_{CG} was varied from 0 to 8 V in 0.5 V steps. The resulting values of optimal operating conditions, along with the corresponding values of performance metrics, are shown in Table III. For both prototype amplifier designs, the resulting value for amplifier output response is well above the required minimum of 1.25 V while the degree of non-linearity is slightly below the upper limit of 10%. Interestingly, while SPC1-amp1 is seen to exhibit better energy resolution, SPC1-amp2 demonstrates better settling time.

In the spirit of exploring the degree to which reductions in settling time could be achieved compared to those reported above for SPC1-amp1 and SPC1-amp2, a variety of alternative amplifier circuit designs were explored. Starting from those prototype amplifier designs (and maintaining a pixel pitch of 1 mm), this exploration involved modification of the transistor dimensions, of the resistance and capacitance of the circuit elements, and of the configuration of the feedback loop. For each variation of design examined, the optimal operating conditions were determined using the same methodology employed for SPC1-amp1 and SPC1-amp2.

A promising design identified in this exploration (referred to as New-amp-a) is the circuit shown in Fig. 3c – the circuit element values for which are given in Table II. New-amp-a differs from the prototype amplifier designs by virtue of a change in dimension for transistor M_1, the removal of resistor R_2 and capacitor C_5, and a change in the configuration of the feedback loop. Specifically, the new feedback loop is comprised solely of a resistor (R_3) with significantly lower resistance values than the R_3 resistors employed in the prototype designs.

The values of the optimal operating conditions, along with the corresponding values of performance metrics, for New-amp-a are shown in Table III. Results are also shown for New-amp-b, the same circuit implemented at a pixel pitch of 0.25 mm, the circuit element values for which are given in Table II.

In Table III, the optimal values for V_{AGC}, V_B and V_{CG} for hypothetical amplifier designs New-amp-a and New-amp-b are all well within the range of values examined in the simulations – as is also the case for the prototype amplifier designs SPC1-amp1 and SPC1-amp2. Compared to the prototype designs, the amplifier output response of the hypothetical designs is seen to be very similar and the degree of non-linearity is seen to be generally better. Furthermore, New-amp-a and New-amp-b exhibit significantly better energy resolution and shorter settling times than SPC1-amp1 and SPC1-amp2 – largely due to the new feedback loop. For example, the improvement in energy resolution is partially a result of the changed frequency bandwidth, now spanning fewer decades, exhibited by the hypothetical designs which causes a reduction in flicker noise (as expected from Eq. [2]). Note that, compared to New-amp-a, New-amp-b has a smaller C_1 capacitance that results in a larger signal at the input of the amplifier for the same input pulse, further improving the energy resolution of that design. Finally, the improved settling time of the hypothetical designs reflects more rapid dissipation of amplifier output response after an input pulse is applied.

The operating conditions shown in Table III were also used to obtain the results reported in the next section.

IIIb. Simulation Results Related to Count Rate

Count rates obtained from the simulations of the prototype amplifier designs and hypothetical amplifier designs are shown in Fig. 4 as a function of input flux. When input flux is low, each of the amplifier circuits is able to resolve every input pulse – as seen from the close overlap of the count rate curves with the dashed line representing ideal behavior. As input flux increases, SPC1-amp1 and SPC1-amp2 are seen to deviate from the dashed line (due to dead time loss) at considerably lower input fluxes than New-amp-a and New-amp-b – an expected outcome given the improvement in settling time reported for the hypothetical designs in Table III.

A summary of results obtained for count rates with 10% and 30% dead time loss (CR_{10} and CR_{30}, respectively) is shown in Table IV. For each of the four amplifier circuit designs, the values reported for CR_{30} are ~2 to 2.5 times higher than that for CR_{10}. As expected, for a given measure of count rate, the count rate values for the four designs are roughly correlated with the settling times reported in Table III – a correlation which validates the selection of minimum settling time in the determination of optimal operating conditions. (Note that settling time, which is depicted in Fig. 2, only represents the ideal amount of time desired between input pulses in the pulse train – since that amount of time would allow the amplifier output to almost completely return to its baseline value. However, input pulses spaced closer together in time can still be resolved by the amplifier – albeit with some degradation in energy resolution.) In addition, for both measures of count rate, New-amp-a and New-amp-b exhibit much higher values than SPC1-amp1 and SPC1-amp2 by a factor of ~20 to 30 – a result that can be largely attributed to the new feedback loop. Furthermore, New-amp-b exhibits higher count rates than New-amp-a due to its smaller input capacitance C_1 – which allows for the selection of optimal operating conditions with a faster, more favorable settling time.

The resulting energy response profiles for each of the four amplifier circuit designs are shown in Figs. 5 and 6. In each figure, results are shown for four input fluxes: 1, 10, 100 and 1000 kcps/pixel. Figure 5 corresponds to results obtained with the 72 kVp spectrum. For SPC1-amp1 (which had a CR_{10} value of 5.03 kcps/pixel), when the input flux is 1 kcps/pixel, the energy response profile largely overlaps with the input energy distribution – demonstrating good fidelity. However, as input flux increases, the energy response profiles increasingly deviate from the input energy distribution – reflecting the progressive

inability of the SPC1-amp1 circuit to unambiguously resolve, or correctly identify the energy of, input pulses that are more closely spaced in time. The same pattern of behavior is exhibited by each of the other amplifier circuit designs – with significant deviations from the input energy distribution becoming apparent at progressively higher input fluxes for SPC1-amp2, followed by New-amp-a and then New-amp-b. Note that the area under the curve for the input energy distribution is 10,000 counts – corresponding to the number of pulses used in the simulation. By comparison, for all amplifier circuit designs, while the area under the curve for the energy response profile is ~10,000 counts at lower input fluxes, the area decreases at higher input flux values – approaching a lower limit of 1 count due to progressively greater degrees of dead time loss.

Figure 6 corresponds to results obtained with 70 keV monoenergetic x rays. While the figure exhibits behaviors similar to those observed in Fig. 5, it more clearly illustrates how the energy response profiles change as a function of input flux. For all designs, as input flux increases, the number of counts below or above 70 keV increases due to pulse pile-up (at least until the input flux is so high that dead time losses result in only a small fraction of pulses being resolved). Interestingly, compared to New-amp-a and New-amp-b, SPC1-amp1 and SPC1-amp2 more strongly shift the monoenergetic, 70 keV input energy towards lower energies. This is a result of the prototype amplifier designs providing an amplifier output response that more severely undershoots compared to that provided by the hypothetical amplifier designs. An example of undershoot appears in Fig. 2 where the amplifier output response falls below the initial baseline value – affecting subsequent pulses that start during the undershoot.

IV. Discussion and Conclusions

Circuit simulations have been employed to investigate the potential performance of amplifier circuit designs based on thin-film, poly-Si transistors for use in large-area, monolithic photon counting arrays. The simulations enabled detailed examination of energy resolution and count rate for existing prototype amplifier designs (SPC1-amp1 and SPC1-amp2), as well as for a pair of hypothetical amplifier designs (New-amp-a and New-amp-b) offering a number of advantages.

Compared to SPC1-amp1 and SPC1-amp2, the number and dimensions of the circuit elements (i.e., the resistors, capacitors and transistors) in New-amp-a and New-amp-b have been reduced. This simplification allows the New-amp-b design to fit in a pixel pitch of 0.25 mm (after shrinkage of the comparator, clock generator and counter components through the improvements in poly-Si circuit manufacture described in reference 41).

A second advantage is that the significant increase in count rate capability offered by New-amp-a (which is over an order of magnitude greater than that of the prototype amplifier designs) approaches the rates associated with radiographic and fluoroscopic imaging applications. For example, the CR_{10} value for New-amp-a (which was implemented at a pixel pitch of 1 mm) is within an order of magnitude of the range of count rates associated with radiography and fluoroscopy (1 to 50 Mcps/mm^2). Moreover, New-amp-b (which corresponds to implementation of the amplifier circuit design of New-amp-a at a pitch of 0.25 mm) not only provides further improvement in the count rate per pixel, but also corresponds to a CR_{10} value of 3.4 Mcps/mm^2 – a highly encouraging result.

Further improvement of amplifier performance may be possible. In particular, while the hypothetical amplifier designs examined in this study were limited to the same folded cascode architecture as the prototype amplifier designs, exploration of alternative amplifier architectures may lead to further improvements in count rate. For example, while the three stages for a given design were identical (i.e., employed circuits with identical transistor dimensions), expanding the exploration of designs to account for different transistor dimensions for each stage may lead to new circuit designs exhibiting even higher count rates. A second example would be employing a mix of amplifier architectures for each stage (other than the folded cascode) to achieve higher count rates.

A simplifying assumption used in this study – that the input energy distributions presented to the amplifier circuits were given by the incident x-ray energy spectra – was chosen so as to result in simpler and easier to interpret energy response profiles such as those shown in Figs. 5 and 6. While not accounting for more realistic absorbed energy distributions is believed to have had relatively little effect upon the count rate results, extending the study to do so (as well as to account for effects such as detector shot noise) would produce more realistic energy response profiles – allowing, for example, the degree to which the amplifier reproduces interesting features of the absorbed energy distribution, such as k-edges, to be studied as a function of input flux.

In the examination of energy resolution, the simulation of noise was performed in the frequency domain – based on a framework developed in a previous study.[41] As a result, while the flicker noise contribution from transistors in the circuits was accounted for, the contribution from transistor thermal noise (which will become a dominant noise source at sufficiently high frequencies) was not. However, the designs of the amplifier circuits examined in the study (combined with the operational conditions of

those circuits) are such that the contribution of thermal noise is relatively minor – as demonstrated through analytical calculations presented in Appendix A.

Future work could improve the accuracy of the energy resolution simulations by performing the noise simulations using more sophisticated poly-Si TFT noise models in the temporal domain (similar to the methodology described in reference 48). In addition, simulating noise in the temporal domain would enable the examination of energy resolution as a function of input flux – since energy resolution generally decreases when input flux increases, as can be seen in Fig. 6. Such simulations would also allow quantification of the proportion of energy resolution loss that is due to intrinsic noise or due to pulse pile-up – providing valuable insight that is not easily obtainable through empirical measurements.

In summary, the simulation methodology employed in this study provides a powerful means for identifying new amplifier designs that offer improved performance. The encouraging results obtained from simulations of the hypothetical amplifier designs reported in this paper support the hypothesis that poly-Si -based, large-area photon counting arrays that exhibit clinically useful count rates are feasible. Use of simulation techniques to further improve the energy resolution and count rate of the amplifier component, as well as to characterize and improve the other components (i.e., comparator, clock-generator, and counter) of photon counting pixels for large area arrays is planned. Finally, it is interesting to note that, while the design of the other pixel circuit components (i.e., the comparator, clock generator and counter) for a given application will depend on requirements associated with that application (e.g., pixel pitch, number of thresholds and counters, counter bit depth, etc.), those circuit designs will also be influenced by the performance and signal output characteristics of the front-end amplifier component.

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Disclosures of Conflict

The authors have no conflicts to disclose.

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Appendix A:

Estimates of the relative contribution of the TFT thermal noise based on analytic calculations

The frequency domain circuit simulations performed in this study, which facilitate relatively straight-forward computation of TFT flicker noise, account for the complexity of the shape of the response of the circuit in frequency space. Estimates of the relative importance of the TFT thermal noise contribution were obtained from the analytic calculations described below.

The power spectral density for the flicker noise contribution of a transistor, in units of V^2/Hz, is:

$$S_{v-flicker}(f) = \frac{k_f}{C_{ox}^2 WLf}. \qquad [A1]$$

This equation was introduced as Eq. [2] in the main text (along with a description of its parameters) and is repeated here for convenience. The power spectral density for the thermal noise contribution of a transistor,[47] in units of V^2/Hz, is:

$$S_{v-thermal} = \frac{8}{3} k_B T \frac{1}{g_m}$$
[A2]

In Eq. [A2], g_m is the transconductance of the TFT (which varies for each TFT in a design as a function of operating conditions), k_B is the Boltzmann constant (1.38×10^{-23} J/K) and T is temperature (298 K).

Integration of Eqs. [A1] and [A2] was used to provide estimates of noise for each TFT in each of the amplifier circuit designs. For a given TFT in a given design, the integration limits were determined through frequency domain simulations of the folded cascode circuit at that design's optimal operating conditions using the methodology outlined in reference 41 – yielding a pair of frequencies, f_{lo} and f_{hi}, at which the gain of that TFT (referred to the output of the folded cascode circuit) is $1/\sqrt{2}$ of its maximum value, known as the 3 dB points. Those simulations also provide the value of g_m for the TFT. With these values, taking the integral of Eq. [A1] provides an expression for an estimate of the flicker noise in units of Volt:

$$\sigma_{v-flicker} = \sqrt{\frac{k_f}{C_{ox}^2 WL} ln\left(\frac{f_{hi}}{f_{lo}}\right)},$$
[A3]

while taking the integral of Eq. [A2] provides an expression for an estimate of the thermal noise in units of Volt:

$$\sigma_{v-thermal} = \sqrt{\frac{8}{3} k_B T \frac{1}{g_m} (f_{hi} - f_{lo})}.$$
[A4]

Each of the four amplifier circuit designs examined in the study has three folded cascode stages and each stage consists of four TFTs: M_1, M_2, M_3 and M_4, as shown in Fig. 3. (When present in a circuit, the M_5 and M_6 TFTs did not contribute significantly to the noise.[41]) Due to the effect that the gain of each subsequent cascading stage has on noise from the previous stage or stages, the noise associated with the first stage was found to be, by far, the dominant contributor of noise – rendering the noise contribution of the second and third stages negligible.

Using Eqs. [A3] and [A4], the noise contribution due to flicker noise and thermal noise for each transistor of the first stage of all four amplifier circuit designs was examined. For all transistors, flicker noise was found to be significantly (2.7 to 25.7 times) larger than thermal noise.

Since, for a given transistor, the combined flicker and thermal noise is given by:

$$\sigma_{v-total} = \sqrt{\sigma^2_{v-flicker} + \sigma^2_{v-thermal}}\,, \hspace{2cm} \text{[A5]}$$

the combined noise increases by only 0.1% to 6.6% compared to flicker noise alone – demonstrating the relatively minor contribution of thermal noise.

Figure 1. Schematic diagram of the pixel circuit architecture of the photon counting arrays under development by the authors. The amplifier component serves to magnify the x-ray induced signal to the level required to allow proper operation of the subsequent comparator component. The comparator component generates an output if the input signal exceeds a user-defined threshold. That output signal is shaped by the clock generator component into pulses that cause the counter component to increment its tally by one. Note that the figure also includes the number of TFTs per component for the various circuit designs incorporated in our early prototype poly-Si PCAs.

Figure 2. Schematic illustration of the concept of settling time. The solid curve represents the amplifier output response to an input pulse corresponding to an interacting x ray. Note that the dashed vertical line on the left corresponds to the introduction of an input pulse. See main text for further details.

Figure 3. Circuit diagrams for the amplifier circuit designs described in Table I: (a) SPC1-amp1, (b) SPC1-amp2, and (c) New-amp-a and New-amp-b. In these diagrams, transistors are labeled M_1 to M_6, capacitors are labeled C_1 to C_5 and C_P, and resistors are labeled R_1 to R_3. Other circuits depicted in the figure include: (d) the circuit corresponding to the circle symbol at the input to each of the designs; and (e) a folded cascode circuit corresponding to the triangle symbols in each of the designs. Note that I is the current source for the input pulses, C_1 is the capacitance of the CZT detector, C_P is a parasitic capacitance, V_{AGC}, V_B and V_{CG} are bias voltages, and V_{DD} is a power rail (which is set to 8 V in the study).

Figure 4. Count rate as a function of input flux for the four amplifier circuit designs. For each design, results are plotted up to that value of input flux beyond which less than 2% of the flux is resolved. The solid lines are drawn to guide the eye while the dashed line corresponds to the ideal of a one-to-one correlation of count rate and input flux.

Figure 5. Energy response profiles for the four amplifier circuit designs. For each design, results are shown for input flux values ranging from 1 to 1000 kcps/pixel. For a given design and flux, the grey and black lines in a graph represent the input energy distribution (corresponding to the 72 kVp spectrum) and the resulting energy response profile, respectively. Note that counts are plotted for a bin size of 1 keV. See main text for further details.

Figure 6. Energy response profiles for the four amplifier circuit designs – following the same conventions used in Fig. 5 – but where the input energy distribution corresponds to 70 keV monoenergetic x rays.

Table I: Design name, circuit description and pixel pitch for each of the amplifier circuit designs examined in this study.

Design Name	Circuit Description	Pixel Pitch
SPC1-amp1	3-stage, 1st order bandpass	1 mm
SPC1-amp2	3-stage, 2nd order bandpass	1 mm
New-amp-a	3-stage, 3rd order bandpass	1 mm
New-amp-b	3-stage, 3rd order bandpass	0.25 mm

Table II. Transistor width/length dimensions, as well as the resistance and capacitance of the other circuit elements, for the various amplifier circuit designs examined in this study. The symbols for the circuit elements listed in the table correspond to those appearing in Fig. 3. Instances where a particular circuit element is not present in a given design are denoted by "n/a". Note that the design specifications for New-amp-a and New-amp-b are identical, except for the value of the input detector capacitance C_1.

	SPC1-amp1	SPC1-amp2	New-amp-a	New-amp-b
Transistor dimensions (µm/µm)				
M_1	50/10	50/10	50/5	50/5
M_2	10/10	10/10	10/10	10/10
M_3	20/10	20/10	20/10	20/10
M_4	20/10	20/10	20/10	20/10
M_5	10/10	6/6	n/a	n/a
M_6	10/10	n/a	n/a	n/a
Resistor values (MΩ)				
R_1	200	200	10	10
R_2	10	10	n/a	n/a
R_3	200	200	15	15

Capacitor values (fF)

C_P	100	100	100	100
C_1	195	195	195	12
C_2	500	500	500	500
C_3	100	100	n/a	n/a
C_4	100	n/a	n/a	n/a
C_5	10	10	n/a	n/a

Table III. Summary of the values for the optimal operating conditions (columns 2 to 4) identified for each amplifier circuit design examined in this study – along with the values of the corresponding performance metrics (columns 5 to 8).
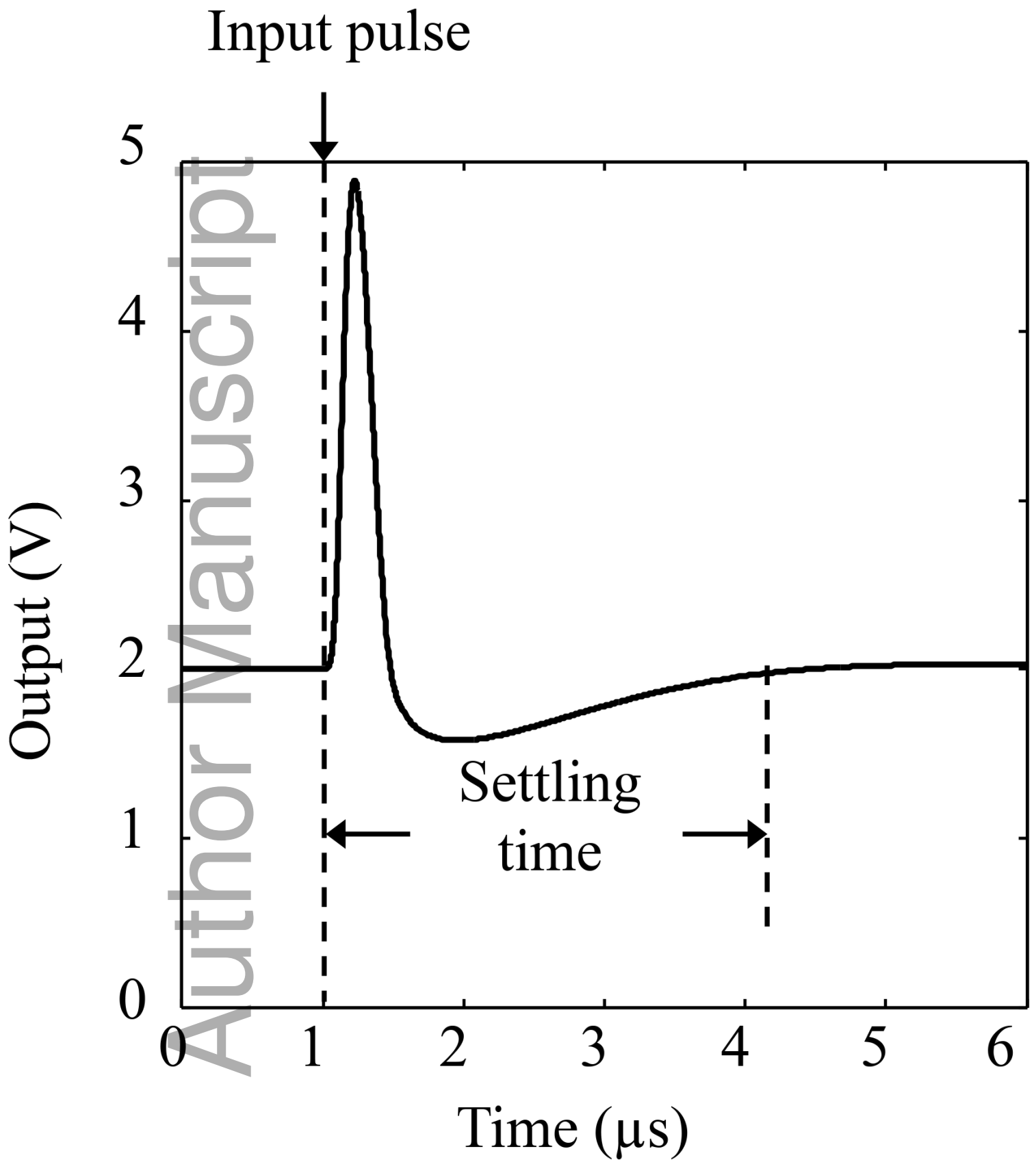
	V_{AGC}	V_B	V_{CG}	Amplifier Output Response	Non-Linearity	Energy Resolution	Settling Time
SPC1-amp1	2.0 V	5.75 V	4.5 V	2.7 V	7.51%	6.78%	143 µs
SPC1-amp2	2.1 V	3.50 V	1.0 V	2.8 V	9.23%	14.9%	53.3 µs
New-amp-a	2.7 V	2.75 V	3.5 V	2.9 V	5.34%	5.88%	5.56 µs
New-amp-b	3.4 V	1.50 V	3.0 V	2.9 V	8.11%	2.76%	3.11 µs

Table IV. Results for the two measures of count rate (CR_{10} and CR_{30}) for each amplifier circuit design. See text for further details.

	CR_{10}	CR_{30}
	(kcps/pixel)	(kcps/pixel)
SPC1-amp1	5.03	13.9
SPC1-amp2	8.36	21.6
New-amp-a	154	381
New-amp-b	210	491

Amplifier (13-16 TFTs) → Comparator (7-9 TFTs) → Clock generator (30-40 TFTs) → Counter (116-164 TFTs)
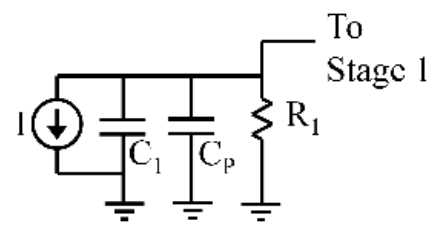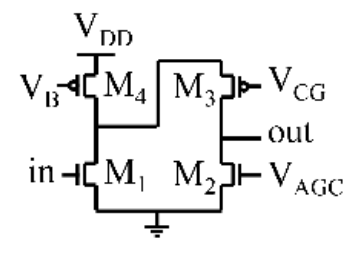
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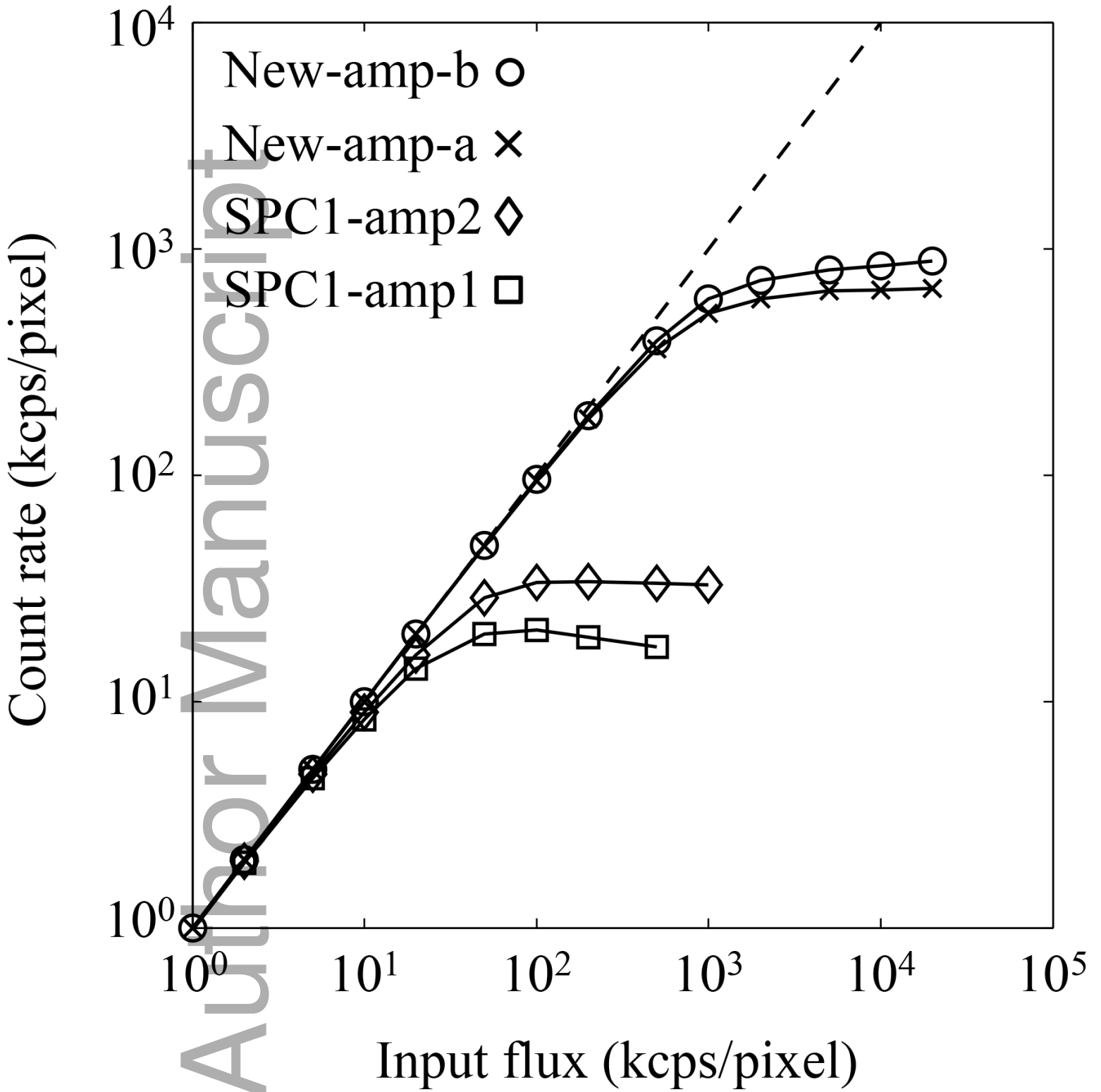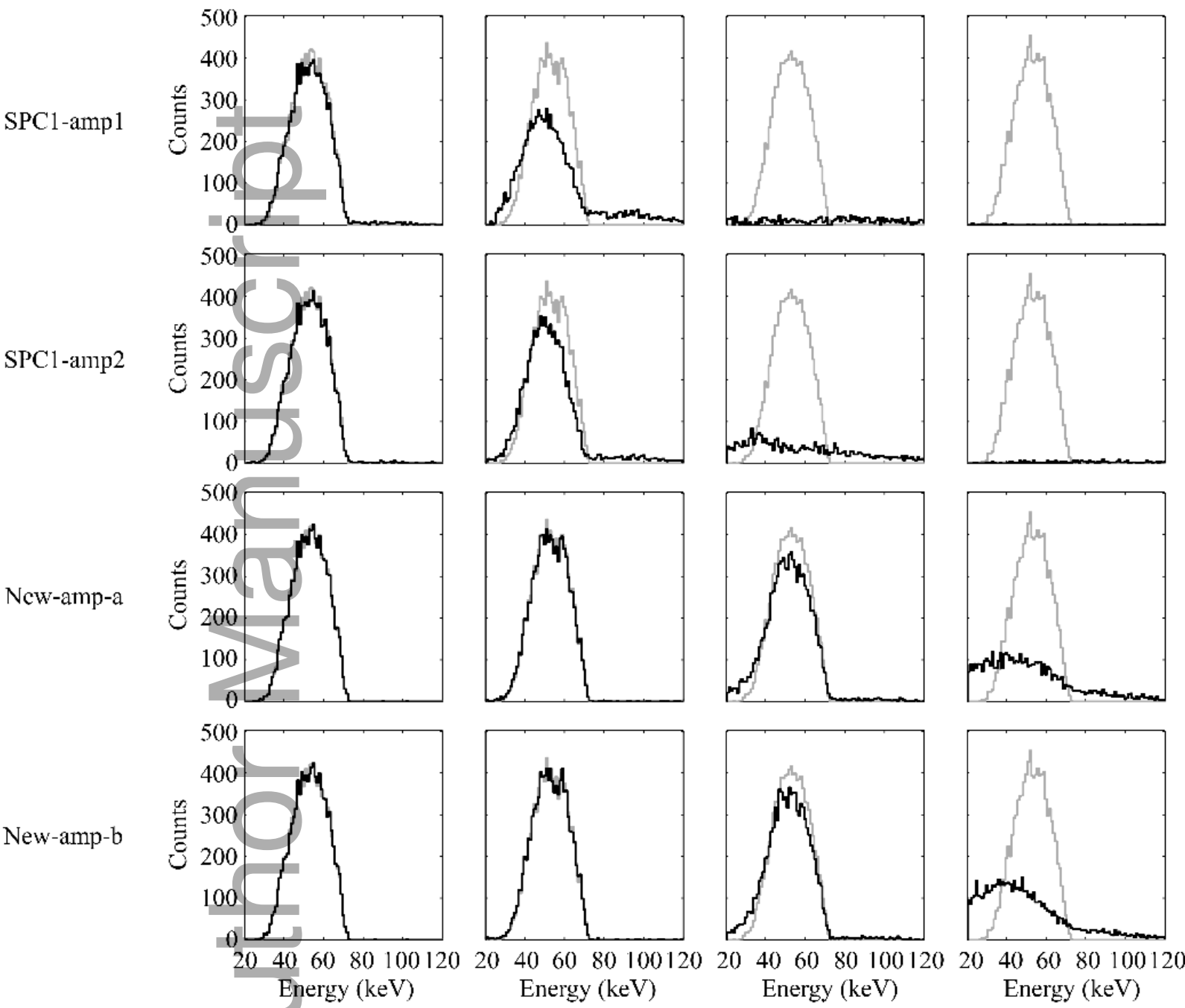
(a)

(b)

(c)

Stage 1   Stage 2   Stage 3
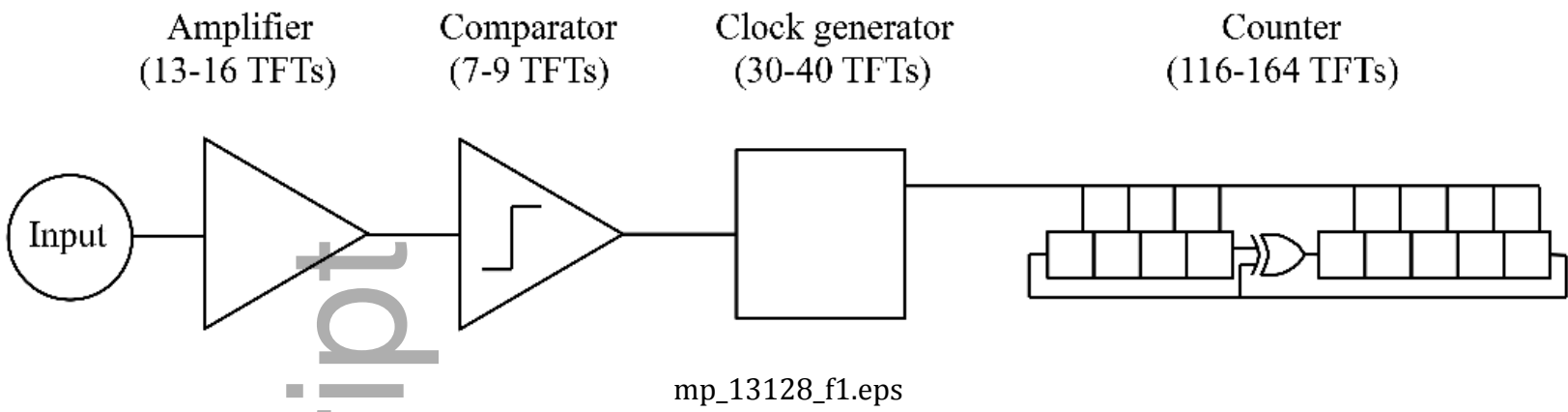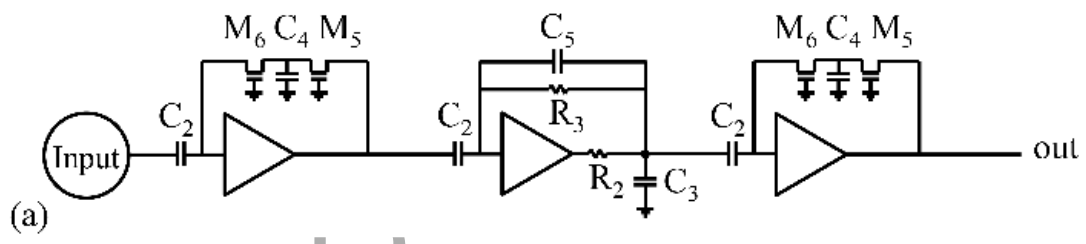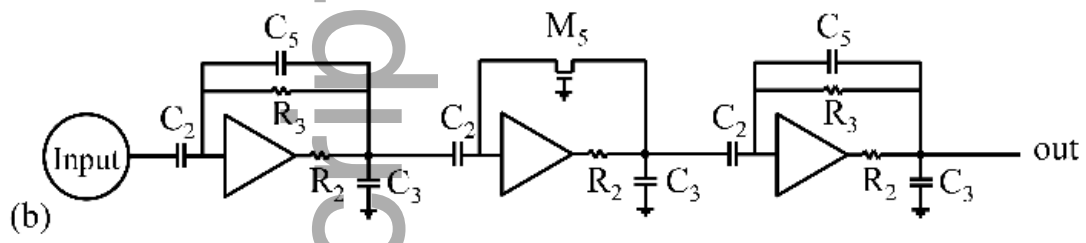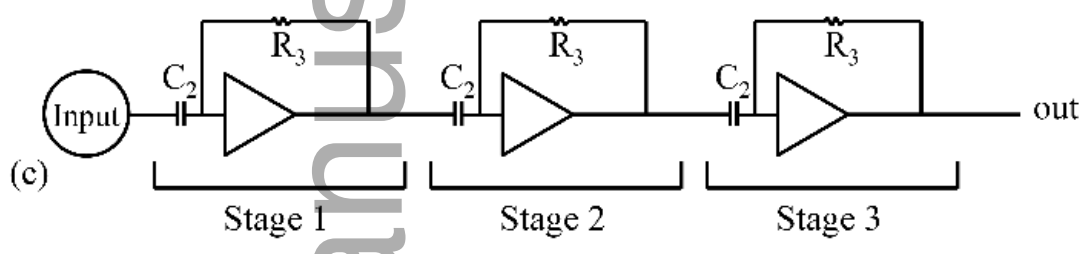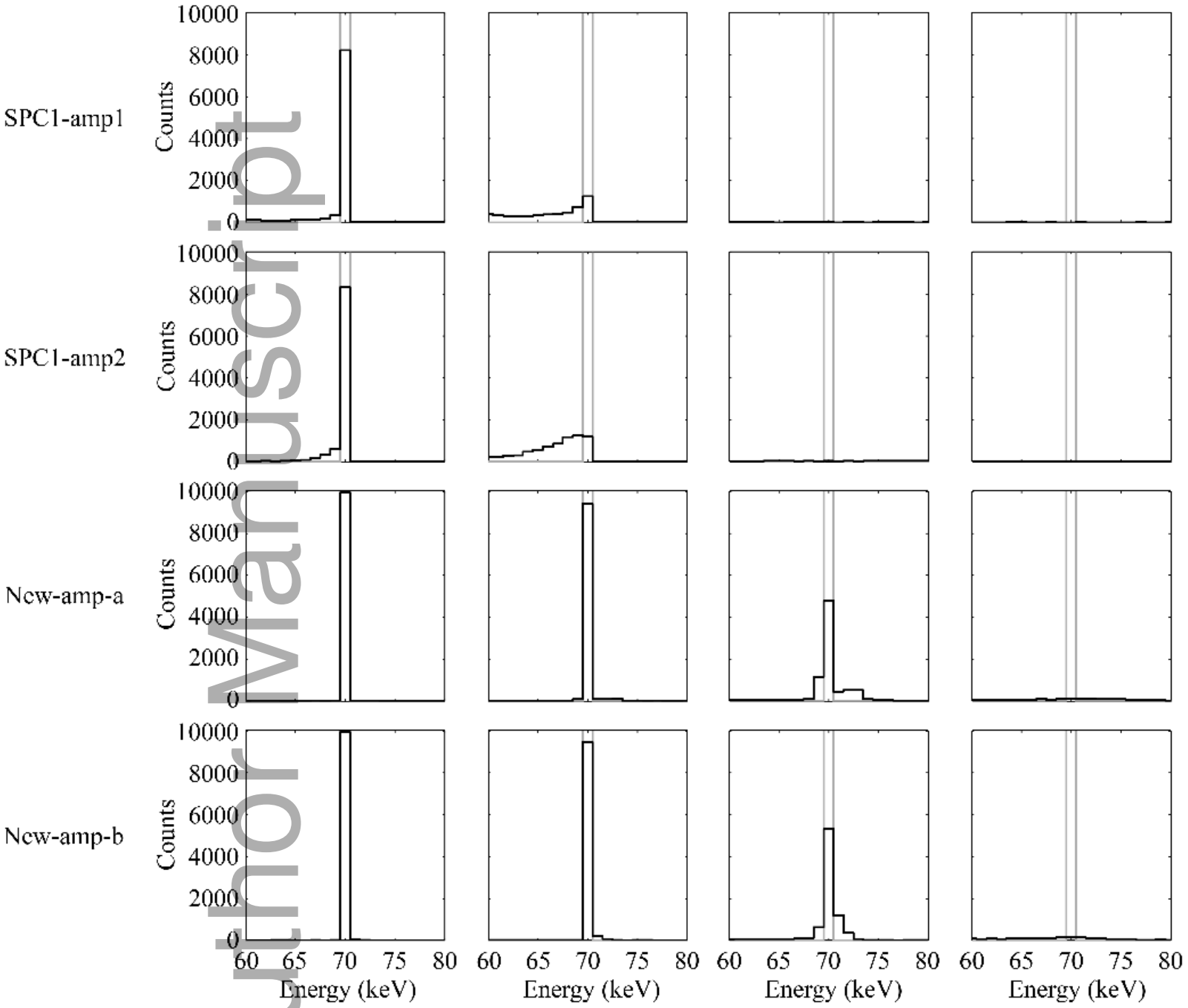
(d) Input circuit

(e) Folded cascode circuit

mp_13128_f3.eps

mp_13128_f4.eps

Input flux: 1 kcps/pixel   10 kcps/pixel   100 kcps/pixel   1000 kcps/pixel

SPC1-amp1

SPC1-amp2

Ncw-amp-a

New-amp-b

Energy (keV)   Energy (keV)   Energy (keV)   Energy (keV)

mp_13128_f5.eps

mp_13128_f6.eps