A CMOS Digital Beamforming Receiver

by

Sunmin Jang

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in the University of Michigan
2018

Doctoral Committee:

Professor Michael P. Flynn, Chair
Professor Zhong He
Assistant Professor Hun-Seok Kim
Associate Professor Zhengya Zhang

Sunmin Jang

smjang@umich.edu

ORCID iD: 0000-0002-0706-9786

Acknowledgements

Over the past five years I have received lots of support and encouragement from a number of individuals. First, I want to thank my family and my parents in Korea. My wife, Seunghyun Kim, has been very supportive taking care of Ian Jang for her busy husband. I also want to thank my son, Ian Jang, for distracting me when I was under pressure and stress. I would like to thank my parents Seongjae Jang and Kiheung Yoo for their unconditional support.

Prof. Flynn has been a very generous and kind advisor. I have lots of respect for him in both technical and personal aspects. I appreciate his support, valuable advices, and jokes. Jaehun Jeong is a great mentor who taught me not only technical material but also how to survive in grad school. I was lucky to work with Rundao Lu, who is an amazingly hard-working guy. Fred N. Buhler is a very nice friend who has helped my writings several times. I also thank Daniel Weyer for his cynical jokes. I thank Seungjong Lee for teaching me analog techniques. I am grateful that I became a friend with Eunseong Moon, the nicest guy in the world. It was great to spend weekends with Junghoon Kim, Minhwa Jang, Wonjin Choi, Hanjin Lim, and their kids. I want to thank Lamsol Woo and Sungwook Yoon for being my best friends from the middle school.

Finally, I thank Jeongsong Cultural Foundation for supporting my master's study, and the Samsung scholarship for supporting my Ph.D. study.

Table of Contents

List of Tables

List of Figures

List of Abbreviations

ADC	Analog-to-digital converter
BB	Baseband
BSP	Bit stream processing
CMOS	Complementary metal-oxide semiconductor
CT	Continuous-time
CTBPDSM	Continuous-time band-pass delta-sigma modulator
CWM	Complex weight multiplication
DAC	Digital-to-analog converter
DDC	Digital down-conversion
DSP	Digital signal processing
DT	Discrete-time
dB	Decibel
ENOB	Effective number of bit
FF	Feedforward
FPGA	Field programmable gate array
HPF	High pass filter
HZ	Half-clock-delayed return-to-zero
IC	Integrated circuit
IF	Intermediate frequency
IIT	Impulse-invariant transformation
IL-BSP	Interleaved bit stream processing

LPF	Low pass filter
MIMO	Multiple input and multiple output
MUX	Multiplexer
NTF	Noise transfer function
NMOS	N-type metal-oxide-semiconductor
PCB	Printed circuit board
PMOS	P-type metal-oxide-semiconductor
PSD	Power spectral density
QFN	Quad-flat no-leads
RF	Radio frequency
RZ	Return-to-zero
SFDR	Spurious-free dynamic range
SNDR	Signal to noise-plus-distortion ratio
SNR	Signal to noise ratio

Abstract

As the demand for high speed communication is increasing, emerging wireless techniques seek to utilize unoccupied frequency ranges, such as the mm-wave range. Due to high path loss for higher carrier frequencies, beamforming is an essential technology for mm-wave communication. Compared to analog beamforming, digital beamforming provides multiple simultaneous beams without an SNR penalty, is more accurate, enables faster steering, and provides full access to each element. Despite these advantages, digital beamforming has been limited by high power consumption, large die area, and the need for large numbers of analog-to-digital converters. Furthermore, beam squinting errors and ADC non-linearity limit the use of large digital beamforming arrays. We address these limitations.

First, we address the power and area challenge by combining Interleaved Bit Stream Processing (IL-BSP) with power and area efficient Continuous-Time Band-Pass Delta-Sigma Modulators (CTBPDSMs). Compared to conventional DSP, IL-BSP reduces both power and area by 80%. Furthermore, the new CTBPDSM architecture reduces ADC area by 67% and the energy per conversion by 43% compared to previous work.

Second, we introduce the first integrated digital true-time-delay digital beamforming receiver to resolve the beam squinting. True-time-delay beamforming eliminates squinting, making it an ideal choice for large-array wide-bandwidth applications.

Third, we present a new current-steering DAC architecture that provides a constant output impedance to improve ADC linearity. This significantly reduces distortion, leading to an SFDR improvement of 13.7 dB from the array.

Finally, we provide analysis to show that the ADC power consumption of a digital beamformer is comparable to that of the ADC power for an analog beamformer.

To summarize, we present a prototype phased array and a prototype timed array, both with 16 elements, 4 independent beams, a 1 GHz center frequency, and a 100 MHz bandwidth. Both the phased array and timed array achieve nearly ideal conventional and adaptive beam patterns, including beam tapering and adaptive nulling. With an 11.2 dB array gain, the phased array achieves a 58.5 dB SNDR over a 100 MHz bandwidth, while consuming 312 mW and occupying 0.22 mm^2. The timed array achieves an EVM better than -37 dB for 5 MBd QAM-256 and QAM-512, occupies only 0.29 mm^2, and consumes 453 mW.

Chapter 1 Introduction

1.1. Digital Beamforming and 5G

Emerging wireless systems such as 5G will use mm-wave bands to support more users and deliver higher data rates [1]. However, mm-wave systems face severe link-budget challenges due to high path losses and the lower diffraction of mm-wave signals [2], [3]. Large-array beamforming is an essential technology to make up for the reduced link budgets with array gain and to establish reliable wireless connections through the use of MIMO algorithms.

Digital beamforming (DBF) has several advantages over analog beamforming (ABF) including accurate beam patterns, multiple receive beams without SNR penalty, adaptive interference suppression, simplified calibration, and the flexibility of fully configurable beam shapes [4]. Seamless generation of multiple simultaneous beams in DBF allows us to exploit MIMO techniques for improved reliability and higher data rates. For example, transmit diversity improves resistance to multipath fading by receiving a single data stream via multiple beams [5]. Spatial multiplexing, in which different data streams are received through different beams, can also achieve higher data rates or further reduce the SNR requirement of the receiver [6]. However, digital beamforming has been limited in practice by high power consumption and large die area [7].

1.2. Phased Array and Timed Array

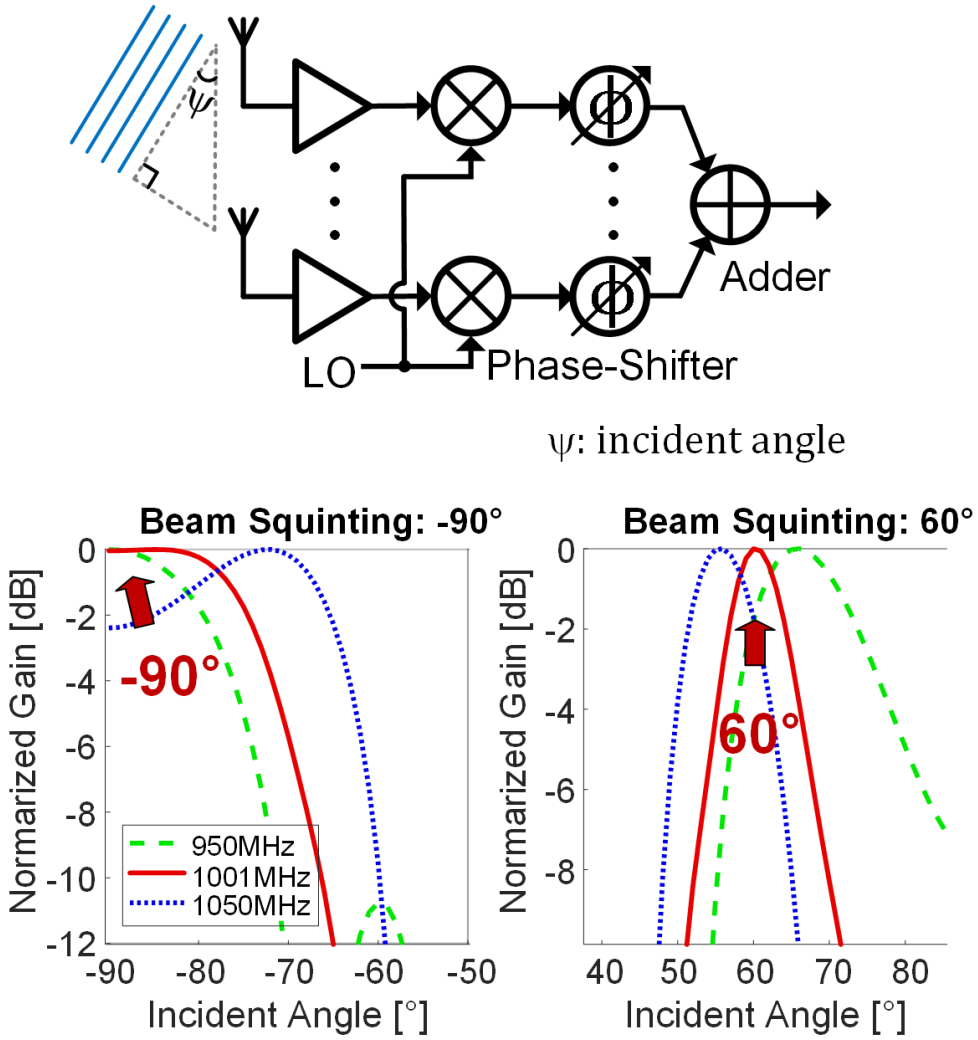

Figure 1. (top) System architecture of a conventional phase-shift beamformer and (bottom) beam squinting errors of a 16-element, 1 GHz IF, a 100 MHz BW beamformer.

Current integrated beamformers approximate time delay by phase-shift. This allows size and power efficiency [8], [9], but it is limited by inaccurate beam steering away from the central frequency - a phenomenon known as squinting [10]. Figure 1 shows the high-level architecture of a baseband phased array, together with beam-squinting errors for a 1 GHz, 16-element, 100 MHz bandwidth phased array. Notice that the central frequency (solid red) is steered accurately, but the beam squinting error can be as large as 18° for frequencies $\pm$50 MHz from the center frequency.

Implementations of true-time-delay arrays are quite limited. RF true-time-delay beamformers replace phase-shifters with RF delay lines, but are limited to a few hundred picoseconds of time delay and suffer from delay variation over the input bandwidth [11].

1.3. ADC Power Comparison for Digital and Analog Beamforming

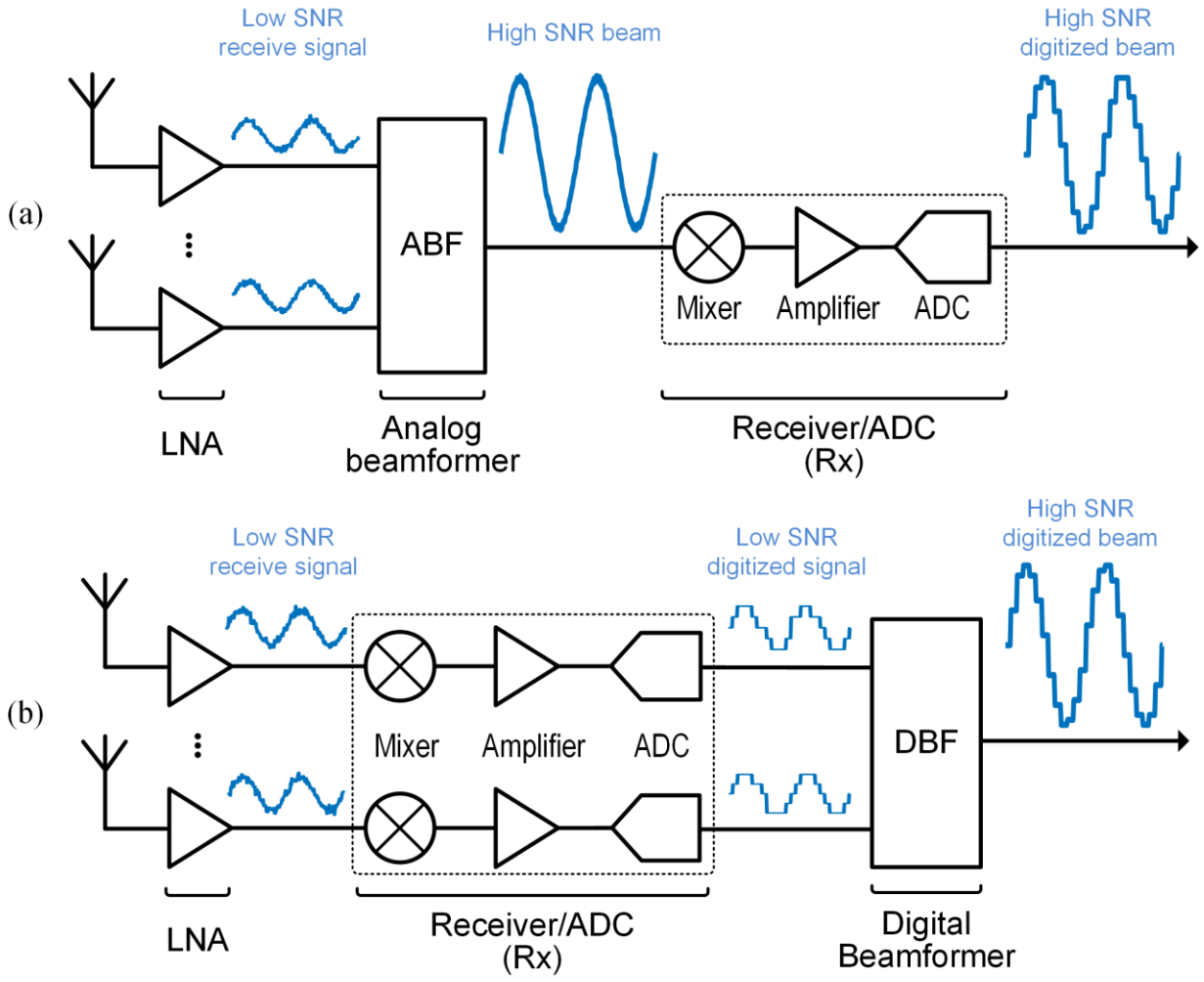

Figure 2. System architectures of (a) analog and (b) digital beamforming.

Although digital beamforming requires a large number of ADCs, if the ADCs are noise limited then the total ADC power for digital and analog beamforming is comparable.

1.3.1. Thermal Noise Limited

Although a large number of ADCs are required for DBF, the array gain in DBF greatly relaxes the ADC SNR requirement. Further, if we assume that the ADCs are thermal noise limited, then the total ADC power is the same for both cases.

ABF necessitates high ADC SNR to quantize the high SNR beam since beamforming is performed prior to the ADC ((a)). Although DBF necessitates several ADCs, the SNR requirement of a single ADC can be greatly relaxed, as the lower SNR signals from the individual ADCs combine to generate a high SNR beam ((b)). The SNR requirement of the ADCs in ABF and in N-element DBF is expressed as

$$\mathrm{SNR_{ABF}} = \mathrm{SNR_{target}}, \tag{1}$$

$$\mathrm{SNR_{DBF}} = \frac{\mathrm{SNR_{target}}}{\mathrm{N}}, \tag{2}$$

where $\mathrm{SNR_{target}}$ is the SNR requirement of the system, $\mathrm{SNR_{ABF}}$ is the SNR requirement of the single ADC in ABF, and $\mathrm{SNR_{DBF}}$ is the SNR requirement of one of the ADCs in DBF. As shown in (1) and (2), $\mathrm{SNR_{DBF}}$ is N times lower than $\mathrm{SNR_{ABF}}$, as N-element DBF exploits a digital array gain of N (Receive signals from channels constructively interfere to generate $\mathrm{N^2}$ times higher signal power, and uncorrelated noise from channels produce N times greater noise power).

With the assumption that the ADCs in DBF and ABF have the same Schreier figure of merit (FoM), the total power consumption of the ADCs in ABF and DBF can be represented as

$$\mathrm{P_{ABF}} = \frac{\mathrm{SNR_{ABF}} * \mathrm{BW}}{\mathrm{FoM_s}} \tag{3}$$

$$\mathrm{P_{DBF}} = \frac{\mathrm{SNR_{DBF}} * \mathrm{BW}}{\mathrm{FoM_s}} * \mathrm{N}, \tag{4}$$

where P_{ABF} is the power consumption of the ADC in ABF and P_{DBF} is the power consumption of all ADCs in DBF. As SNR_{DBF} is N times lower than SNR_{ABF}, the total power consumption of all the ADCs in DBF is the same as the single ADC power consumption in ABF, when the ADCs are limited by thermal noise.

1.3.2. Interference Limited

When a beamformer receives M interfering signals, the total received input power of an ADC can be represented as $(\sum_{m=1}^{M} I_m) + S$, where I_m is the m^{th} interference power and S is the signal power. In this case, the SNR requirement of the ADC becomes $10\log_{10}((\sum_{m=1}^{M}\frac{I_m}{S}) + 1)$ dB higher. For example, when we have one interferer that sends the exact same power as the signal transmitter at the same distance, the SNR requirement of the ADC in a digital beamformer increase by 3.01 dB (0.5 bit ENOB). The SNR requirement for an analog beamformer does not increase by as much because the interference is attenuated. If the m^{th} interference is attenuated by N_mdB, the SNR requirement of an ADC in an analog beamformer increases by $10\log_{10}((\sum_{m=1}^{M}\frac{I_m}{s}10^{-\frac{N_m}{10}}) + 1)$ dB, which is lower than for digital beamforming [4].

1.4. Thesis Outline

In this paper, we present two prototype digital beamforming receivers. The first prototype is a 16-element, 1 GHz IF, 100 MHz BW digital phase-shift beamformer. This is the largest single-chip digital beamforming phased array among published works. The prototype uses interleaved bit stream processing (IL-BSP) to reduce both power and area, based on bit stream processing (BSP) introduced in [9]. The second prototype is a true-time-delay digital beamformer. As the first

integrated true-time-delay digital beamformer IC, this work addresses the problem of beam squinting and ADC nonlinearity.

This paper is organized as follows. Chapter 2 presents the architecture of the continuous-time band-pass delta-sigma modulator (CTBPDSM). Chapter 3 provides a mathematical explanation of phased arrays and baseband true-time-delay arrays. Chapter 4 details the implementation of the prototype digital beamformers. Chapter 5 and Chapter 6 present the system architectures and measurement results of the prototype-I phased array and prototype-II true-time-delay array. Chapter 7 suggests possible future work. Finally, Chapter 8 concludes this thesis.

Chapter 2 Continuous-Time Band-Pass Delta Sigma Modulator[1]

2.1. System Architecture

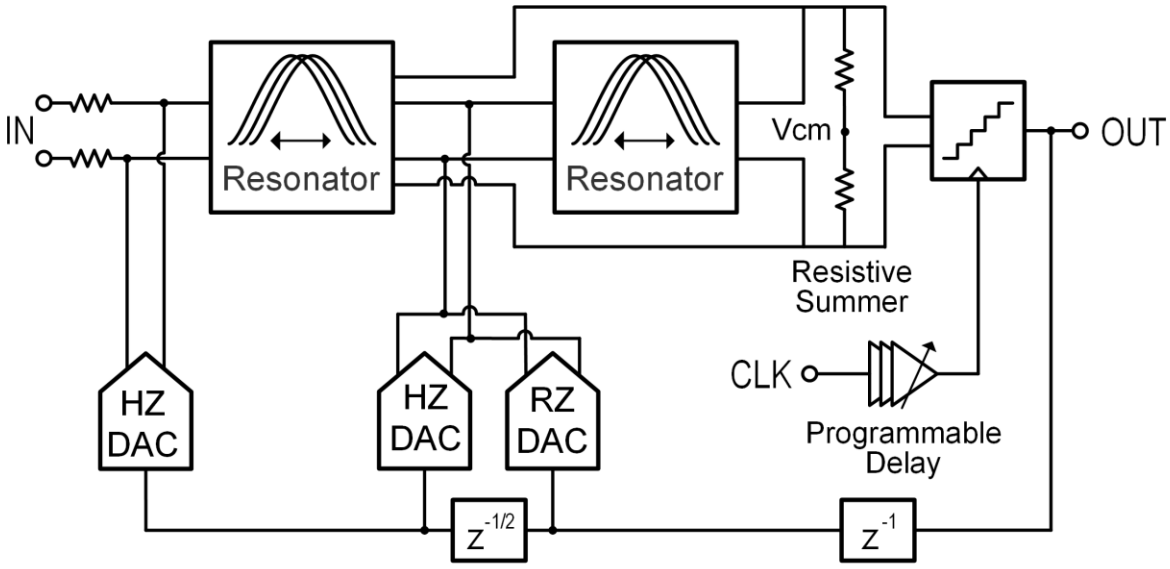

Figure 3. 4th order Continuous-Time Band-Pass Delta-Sigma Modulator.

The ADC area and power consumption have a huge bearing on the die area and power consumption of the entire beamformer. We choose a Continuous-Time Band-Pass Delta-Sigma Modulator (CTBPDSM) for its energy efficiency and small size. Furthermore, a CTBPDSM is easy to drive, resilient to aliasing, and is very attractive for digitizing IF signals. At the system level, we take advantage of the signal processing gain of the large ADC array to improve the SNR of the overall beamformer. Since noise and random mismatch errors are uncorrelated, the prototype-I phased array benefits from a near-ideal 11.2 dB array SNR improvement.

[1] The design of continuous-time band-pass delta-sigma modulator was in collaboration with Jaehun Jeong.

The fourth-order CTBPDSM in Figure 3 uses compact single op-amp RC resonators instead of bulky LC-tank resonators [12] to save power and area. The resonator center frequency is tuned with 3-bit trim capacitors. To further reduce power and area, we use a passive summer instead of power-hungry trans-impedance amplifier (TIA) in front of the quantizer. Thanks to the passive summer, the ADC consumes 20% less power and occupies 10% less area. The 4GS/s 5-level quantizer is on-chip offset calibrated so it presents a very small capacitive load (0.2 fF) to the summer. The quantizer sampling time is digitally adjusted by a 3b tunable delay to ensure loop stability. The op-amps use a 3-stage nested Gm-C structure which gives a good tradeoff between bandwidth and gain.

2.2. Advantages of a Continuous Time Modulator over a Discrete-Time Low-Pass Nyquist ADC

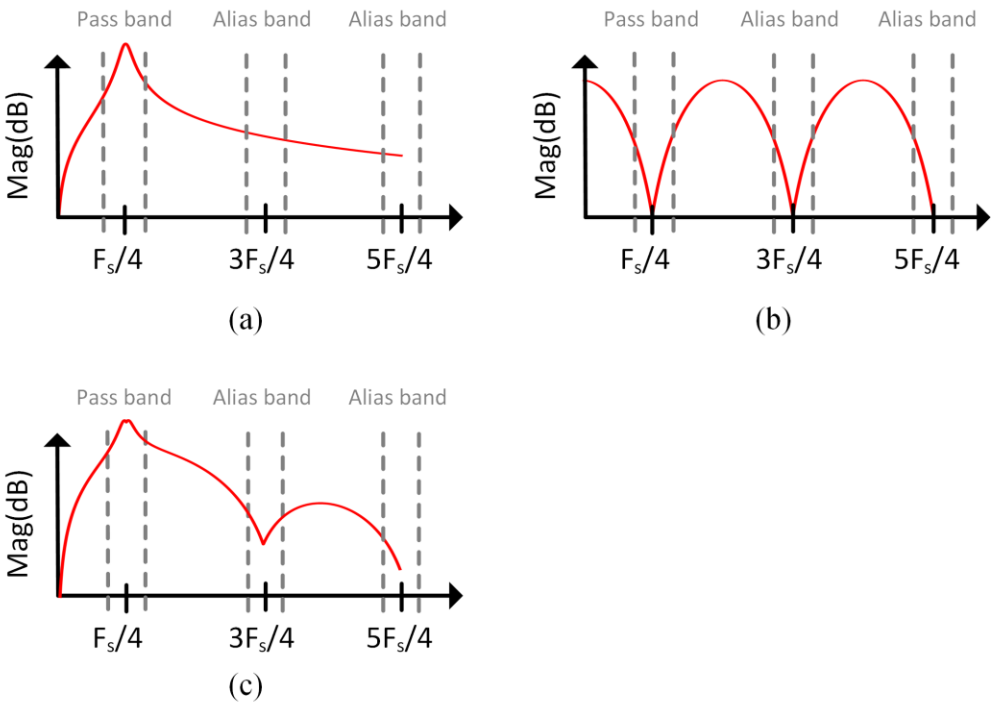

Figure 4. Frequency domain representations of (a) the resonator, (b) the noise transfer function, and (c) the signal transfer function of the CTPBDSM.

Continuous-time band-pass delta-sigma modulators have several advantages. A continuous-time modulator has inherent anti-alias filtering. As discussed in [13], the noise transfer function (NTF) of the 4th order CTBPDSM in Figure 3 can be expressed as

$$\mathrm{NTF}(z) = \frac{1}{1 - \mathrm{L}(z)}, \tag{5}$$

where L(z) is the discrete time transfer function from the quantizer output, through the feedback DACs and the resonators, back to the quantizer input. The NTF is expressed in the z-domain because the quantization noise is sampled by the quantizer. The signal transfer function (STF) of the modulator can be expressed as

$$\mathrm{STF}(s,z) = \frac{\mathrm{G}(s)}{1 - \mathrm{L}(z)} \tag{6}$$

$$= \mathrm{G}(s)\mathrm{NTF}(z), \tag{7}$$

where G(s) is the transfer function of the feed-forward path. As $s = j2\pi f$ and $z = e^{j2\pi f/f_s}$, (7) can be rewritten as

$$\mathrm{STF}(f) = \mathrm{G}(j2\pi f)\mathrm{NTF}\left(e^{j2\pi f/f_s}\right). \tag{8}$$

Figure 4 shows the frequency domain representations of $\mathrm{G}(j2\pi f)$, $\mathrm{NTF}\left(e^{j2\pi f/f_s}\right)$, and $\mathrm{STF}(f)$. Although the NTF has zeros in the pass-band (Figure 4(a)), the poles of the resonators (Figure 4(a)) cancel the NTF zeros, making a reasonably flat STF gain. On the other hand, the STF gain in the alias bands is much lower because there are no resonator poles (Figure 4(c)). Therefore, interference in the alias bands is attenuated, which greatly relaxes anti-alias filtering requirements.

Another advantage of the band-pass modulator approach is that digital mixing does not suffer from I/Q mismatch, mixer noise, DC offset, and flicker noise. Band-pass digitization also halves the number of required ADCs because the quadrature signals share an ADC. On the other hand, two low-pass modulators would be required to digitize I and Q analog signals.

2.3. Implementation

Emerging standards require relatively wide ADC bandwidths for high data rates. The 4th order CTBPDSM achieves a 100 MHz bandwidth with a 4 GHz sampling rate and an OSR of 20. Furthermore, small-area and low-power consumption are critical as DBF has a large number of ADCs. We reduce power and area with various techniques including 1) digital array gain, 2) redesign of the feedback DACs, 3) a passive summer, 4) a compact RC based resonator, 5) a 3-stage nested Gm-C opamp, and 6) a constant output impedance feedback DAC.

2.3.1. Digital Array Gain

We exploit the high digital array gain to lower the SNR requirement of the individual ADCs. An advantage of DBF is that it performs highly accurate digital down-conversion, and complex weight multiplication, so that array gain is close to the theoretical limit. Our prototype-I 16 element beamformer (see Chapter 5.3.) benefits from a near-ideal 11.2 dB array gain, which significantly lowers the SNR requirement of the individual ADCs.

2.3.2. Elimination of the First Return-to-zero DAC

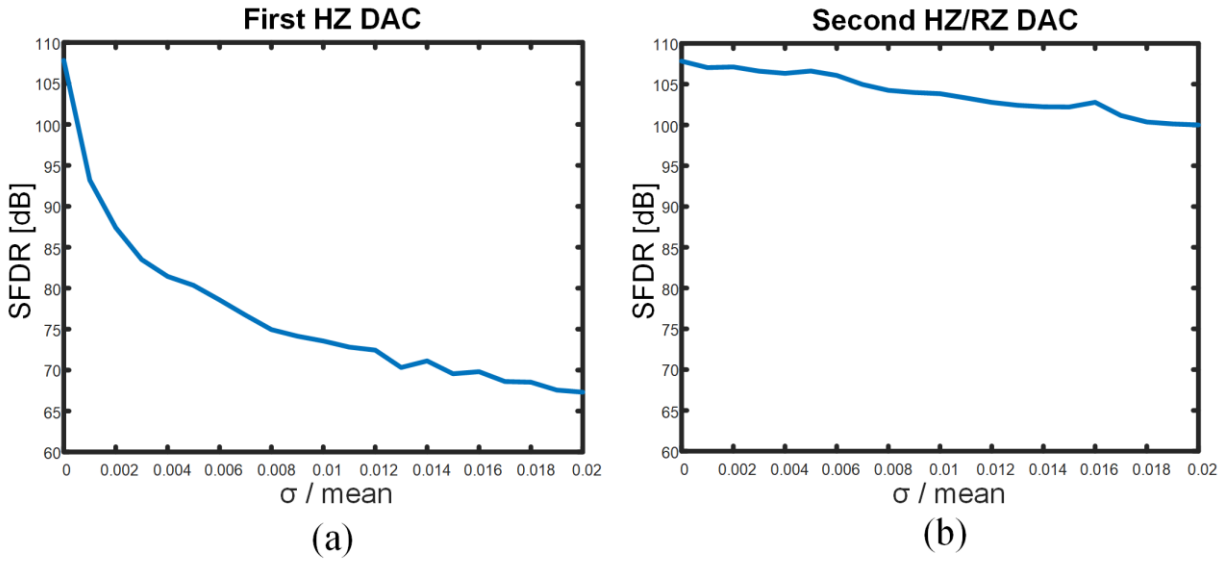

Figure 5. Effect of mismatch (a) in the first-stage DAC and (b) in the second-stage DAC on the SFDR of the modulator.

We modify the DAC feedback to further save power and area [12]. Conventionally, a continuous-time band-pass modulator requires a pair of feedback DACs, consisting of a Return-to-Zero (RZ) DAC and a Half-clock-delayed return-to-Zero (HZ) DAC for each resonator to perfectly transform a discrete-time modulator into a continuous-time modulator. Based on the calculations in [14], the current of the first-stage RZ DAC is made much smaller than the current of the first-stage HZ DAC. Due to the small current of the first-stage RZ DAC, proper tuning of the second-stage DACs can remove the need for the first-stage RZ DAC, reducing system noise and power consumption.

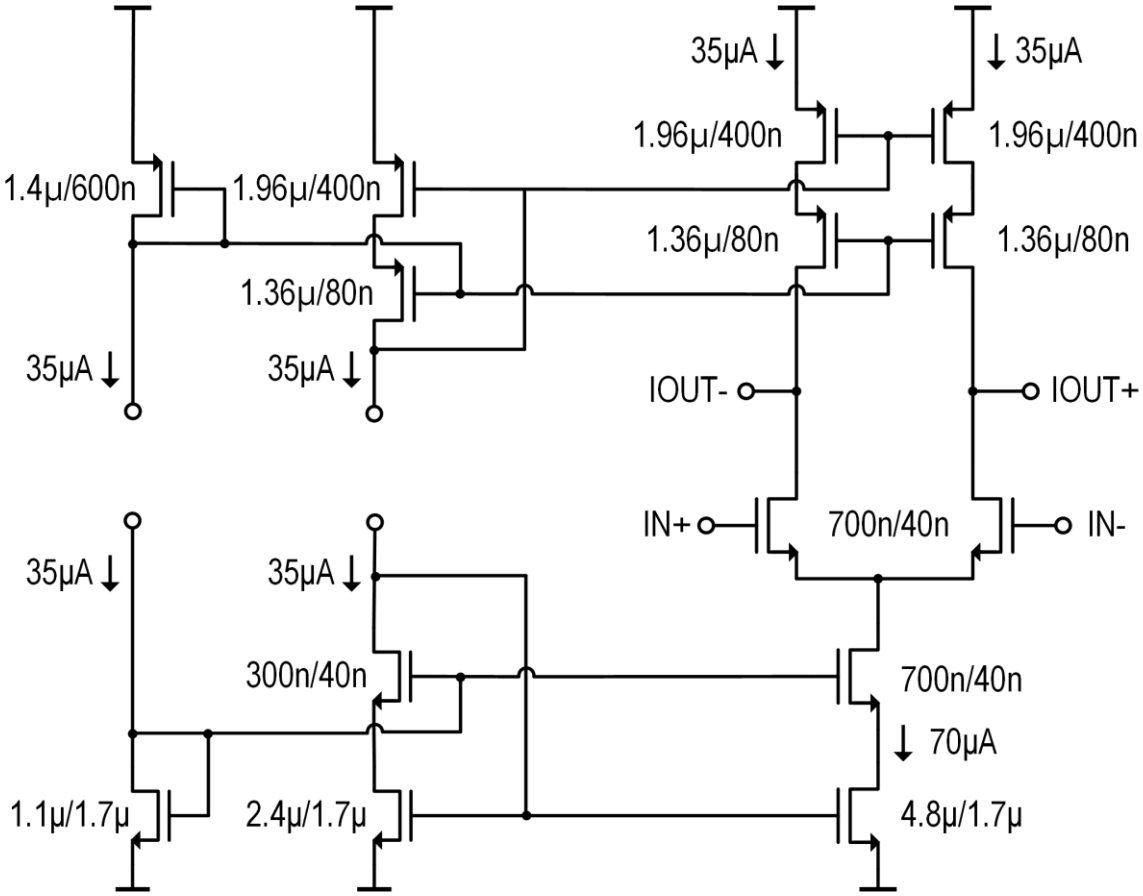

Figure 6. Schematic of the first-stage RZ DAC.

The SFDR of the CTPBDSM is limited by the mismatch of the first-stage DAC, as the first resonator attenuates the non-linearity of the second-stage DACs (Figure 5). The average output current of the first-stage DAC is 70 µA, and its standard deviation is 1.4 µA. The measured SFDR of the modulator is 66 dB and a schematic of the first-stage RZ DAC is shown in Figure 6.

2.3.3. Passive Summer

A passive summer further reduces power and area. We replace the power-hungry active TIA (trans-impedance amplifier) used in [9] with a resistive summer that adds the output current of the first resonator with the output current of the second resonator. Consequently, the CTBPDSM consumes 20% less power and occupies 10% less area.

2.3.4. High Intermediate Frequency (IF)

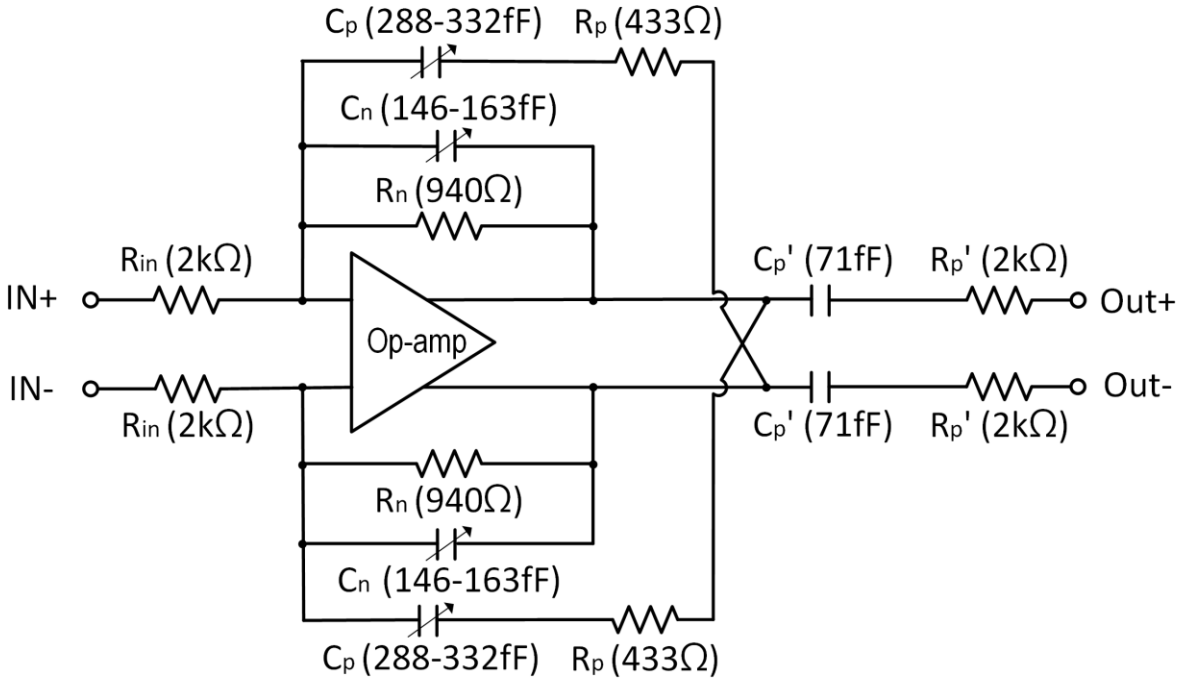

Figure 7. RC based single op-amp resonator.

The single op-amp based RC resonator in Figure 7 is used instead of a bulky LC-tank resonator. As discussed in [12], the resonator transfer function T(s) and center frequency w_0 are

$$T(s) = \frac{w_o s}{s^2 + w_o^2}, \tag{9}$$

$$w_0 = \frac{1}{2R_p C_p}, \tag{10}$$

when $C_p = 2C_n$ and $R_n = 2R_p$. As indicated by (10), the center frequency is inversely proportional to R_p and C_p. The high IF frequency of 1 GHz, allows the use of smaller resistors and capacitors to reduce the area of the resonators. As a result, the resonator size is only 0.003 mm^2 and the CTBPDSM occupies 0.01 mm^2. To account for PVT variation, the resonator center frequency is tuned with a 3-bit trim of C_p and C_n (Figure 7).

2.3.5. 3-stage Nested Gm-C Op-amp

Compared to switched-capacitor based discrete-time modulators, continuous-time modulators have relaxed op-amp bandwidth constraints [13]. We use the 3-stage cascaded G_m-C structure in Figure 8 which gives a good tradeoff between gain and bandwidth [15]. The first resonator op-amp consumes 5.4 mW and provides 13.22 GHz unity gain bandwidth, 71 dB DC gain with 100 fF load capacitance (i.e. the input capacitance of the second resonator).

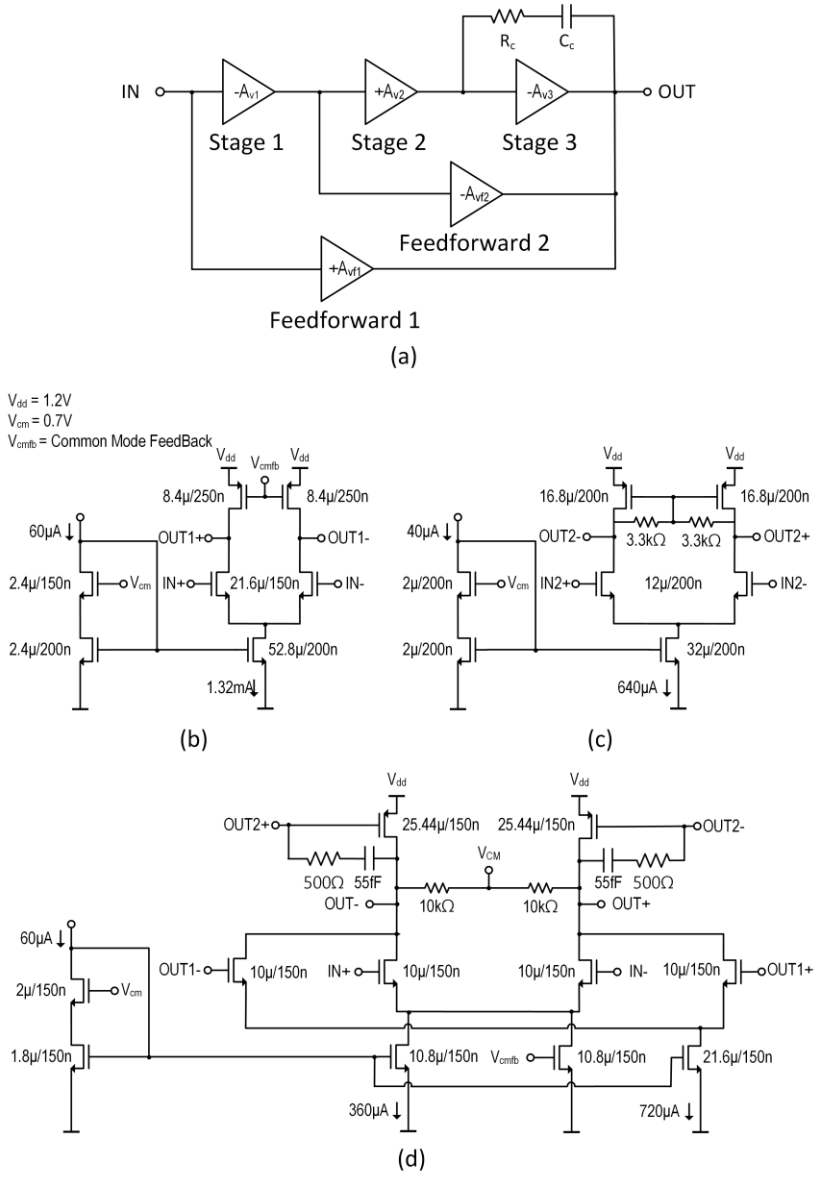

Figure 8. (a) 3-stage nested Gm-C operational amplifier, schematic of (b) stage 1, (c) stage 2, and (d) stage 3 with feedforward amplifiers.

2.3.6. Constant Output Impedance Feedback DAC[2]

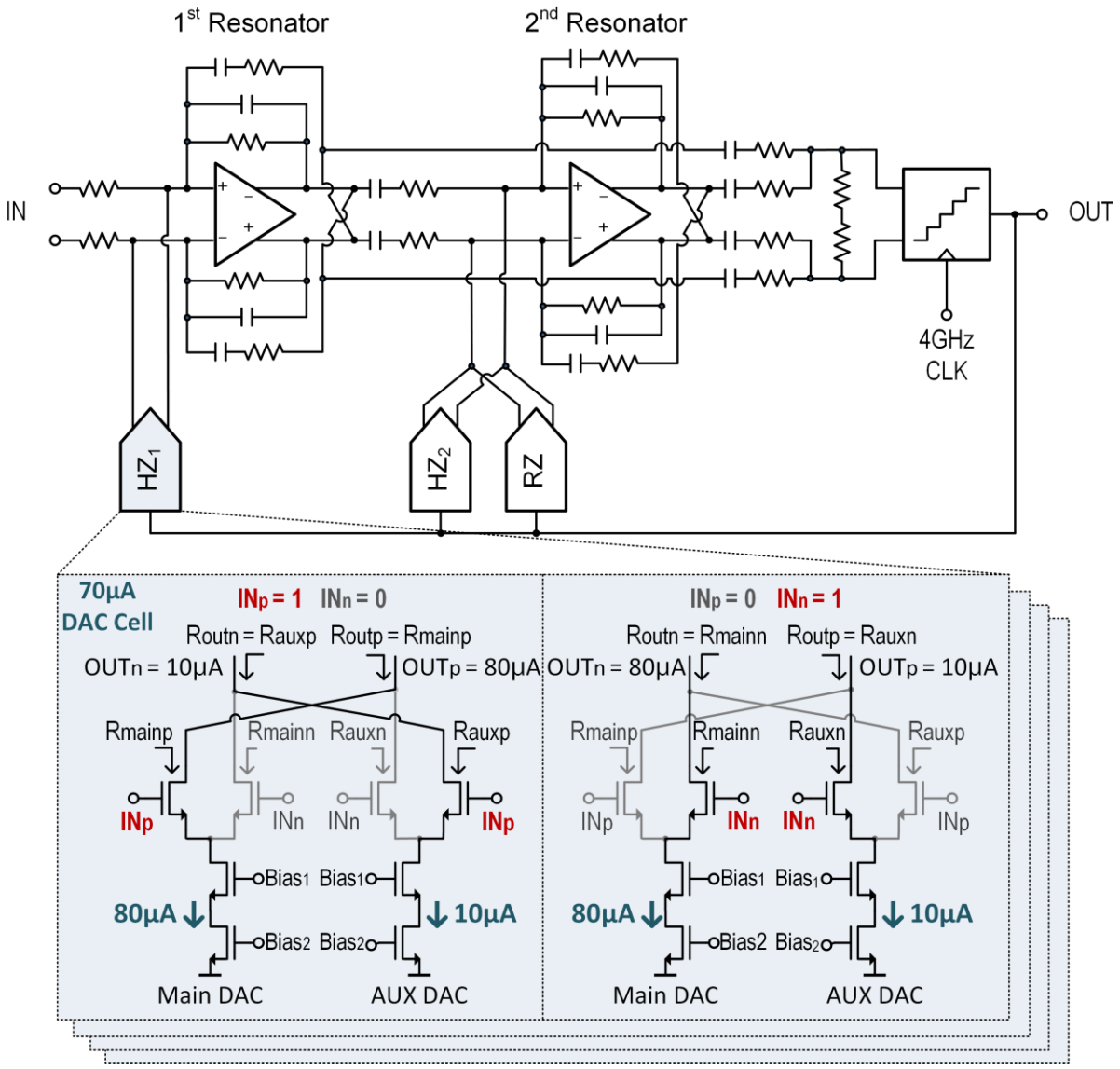

Figure 9. Continuous-time band-pass delta-sigma modulator and a constant output impedance current steering DAC cell.

A big advantage of large arrays is that the array gain improves SNR and also attenuates uncorrelated errors (e.g. DAC transistor matching errors in the ADCs). However, the array cannot improve systematic non-linearity and therefore this limits the overall SNDR and SFDR of the beamformer. We address the dominant systematic nonlinearity of code dependent loading in the

[2] The new DAC design was in collaboration with Rundao Lu.

feedback DAC with a new DAC structure. Figure 9 shows the CTBPDSM and DAC. The output impedance of a conventional current steering DAC is correlated with its input code. We introduce an auxiliary DAC to maintain a constant output impedance regardless of the input signal. As shown in Figure 9, the input to the 10 µA auxiliary DAC is the opposite of the 80 µA main DAC, forcing one of the DACs to sink current at all times. This simple scheme eliminates the correlation between the output impedance and the input code and therefore improves SFDR of the ADC by 6 dB.

2.4. Comparison with State-of-the-Art

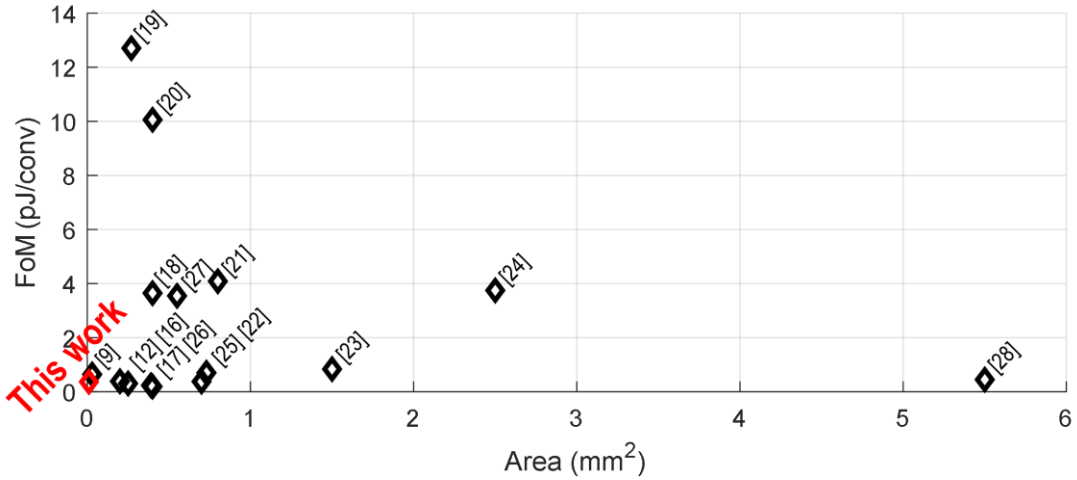

Figure 10. Area and FoM comparison between the CTBPDSM in this work and other state-of-the-art CTBPDSMs.

Figure 10 compares the area and Walden FoM [29] of this ADC with other state-of-the-art CTPBDMs. In addition to having the smallest area (0.01 mm^2) the prototype has one of the best FoMs (365 fJ/conv). Compared to [9], the prototype has a 5 times higher bandwidth (100 MHz) and a 4 times higher center frequency (1 GHz), while using 43% less energy per conversion.

Chapter 3 Mathematical Analysis

3.1. Phased Array

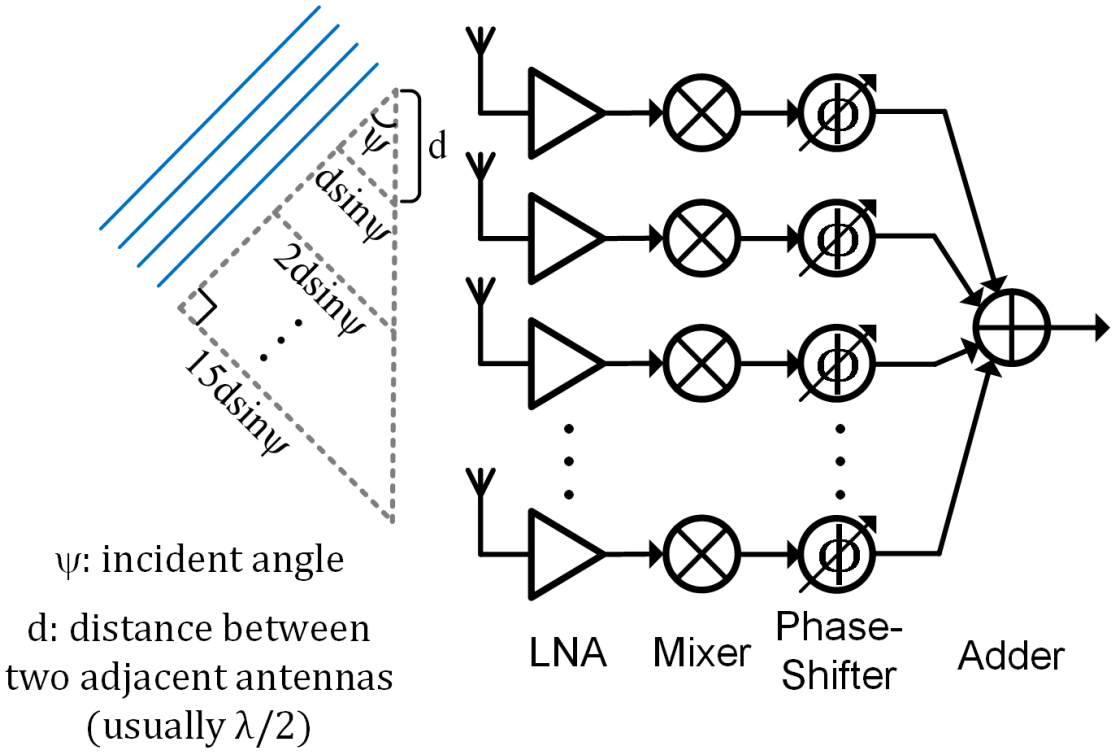

Figure 11. A conventional phased array with 16 elements, 1 GHz center frequency, and 100 MHz bandwidth.

Phased arrays mimic time delay with phase-shifting and are widely used for narrowband applications [30], [31]. To understand the principle of phase-shift beamforming, we consider the 16-element, 1 GHz carrier, 100 MHz bandwidth phased array shown in Figure 11. For a given angle, the propagation delay between the first element and the k^{th} element is,

$$\tau_k = (k-1) \times \frac{d \times \sin\psi}{c}, \tag{11}$$

where τ_k is the time delay difference, k is the element number, d is the distance between two adjacent antennas, ψ is the steered angle, and c is the speed of light. For most phased arrays, $d = \lambda/2$ is chosen as a good tradeoff between 3-dB beam width and number of grating lobes [32]. As $c = \lambda f_c$, (11) is equivalent to:

$$\tau_k = (k-1) \times \frac{\sin\psi}{2f_c} \tag{12}$$

By defining $\tau = \frac{\sin\psi}{2f_c}$, (12) can be simplified to:

$$\tau_k = (k-1) \times \tau. \tag{13}$$

When a phased array is receiving a narrowband sine wave signal centered at f_c, the k^{th} element receives a signal $R_k(t)$ which is

$$R_k(t) = \cos((f_c + \Delta f)(t - \tau_k)) \tag{14}$$

$$= \cos\big((f_c + \Delta f)t - (f_c + \Delta f)\tau_k\big). \tag{15}$$

For narrowband signals, we can simplify (15) with the following approximation which is often called the narrowband assumption:

$$f_c + \Delta f \approx f_c \tag{16}$$

Using the narrowband assumption, we simplify (15) to:

$$R_k(t) \approx \cos((f_c + \Delta f)t - f_c\tau_k). \tag{17}$$

One can eliminate the k-dependent term $-f_c\tau_k$ in (17) by phase-shifting the signal by

$$f_c\tau_k = f_c \times (k-1) \times \tau, \tag{18}$$

and get:

$$f_c\tau_k = f_c \times (k-1) \times \tau, \tag{19}$$

In this way, after phase-shifting we recover the same signal from all the array elements. Because the noise in each element is independent from each other, the addition of the phase-shifted signals ($R_k^{'}$) results in a higher overall SNR.

3.1.1. Limitations of Phased Arrays

Since phased arrays are simpler to implement than timed arrays, they are more widely used. However, the operation of phased arrays is based on the narrowband assumption, which means they produce errors when used in high bandwidth applications. Specifically, they suffer from beam squinting error in the spatial domain, and array ISI in the time domain.

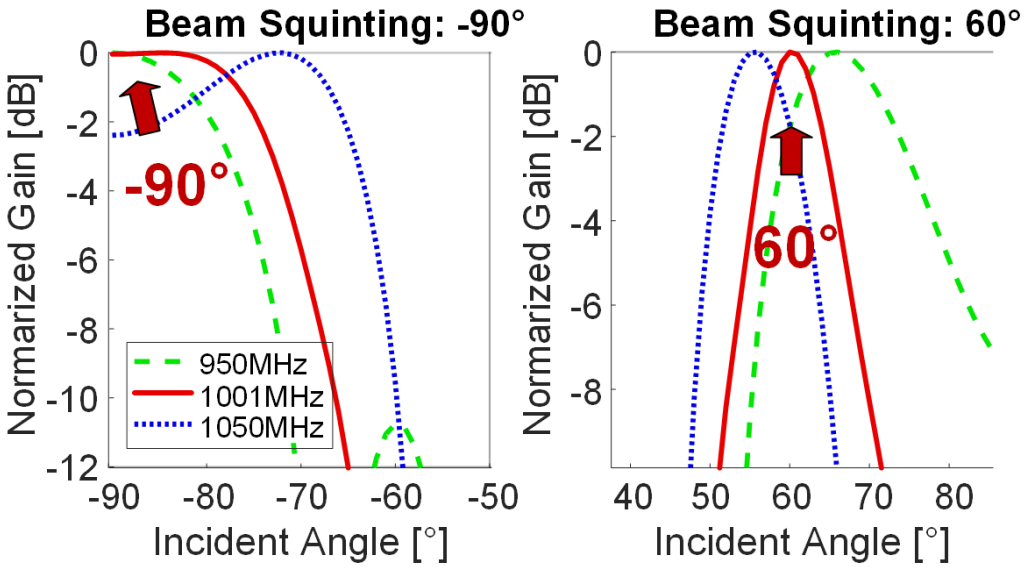

Figure 12. Beam squinting errors for the phased array in Figure 11.

Beam squinting due to the narrowband approximation can be observed in the spatial domain. For example, Figure 12 shows beam squinting errors for a 16 element, 1 GHz center frequency, 100 MHz BW beamformer. As shown in the figure, the narrowband approximation causes the direction of the beam to depend on the frequency. To get a sense of how much beam squinting error occurs for phased arrays, [33] estimates the error as:

$$\Delta\theta = -\frac{\tan\theta_0}{f_c}\Delta f, \tag{20}$$

where $\Delta\theta$ is the squinting error, θ_0 is the steered angle, f_c is the carrier frequency, and Δf is the offset frequency. Although the squinting error in (20) is not dependent on the array size, large arrays suffer more than small arrays because the 3-dB beam width is narrower for large arrays. For the beamformer in Figure 11 that has a 1 GHz center frequency and a $\pm$50 MHz bandwidth, the estimated error for a 60° steered beam is $\pm$5°, which matches the plot in Figure 12. This squinting error is larger than the $\pm$4° 3-dB beam width for a 16-element linear array.

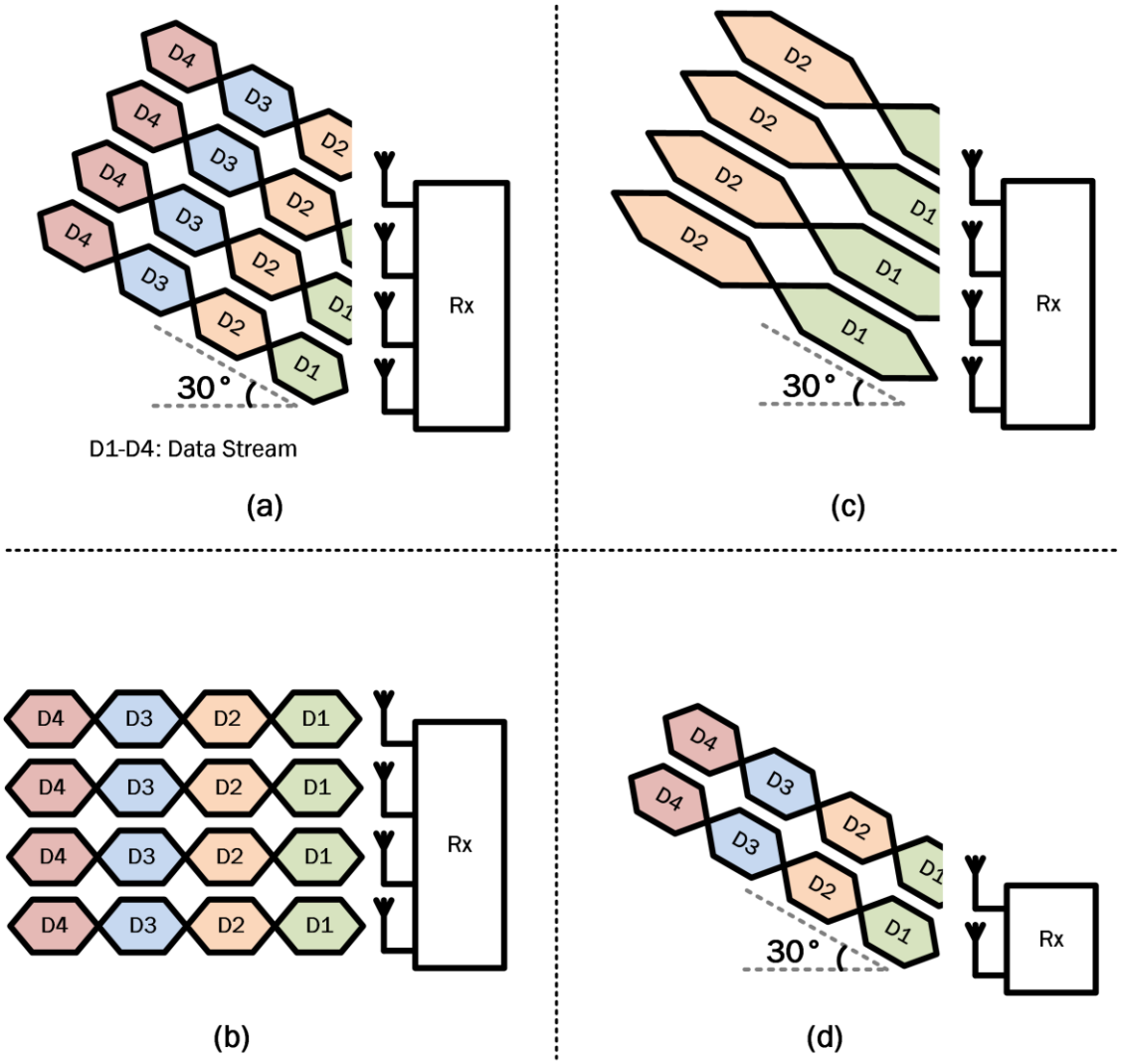

Figure 13. (a) An example of an intersymbol interference and why it is less likely to occur when the array has (b) a low data rate, (c) a small steered angle, and (d) a small array size.

The narrowband assumption is only valid when the propagation delay to the elements can be approximated with a constant phase-shift over the signal bandwidth [32]. When the propagation delay is large, phased arrays suffer from array ISI, which causes some array elements to receive different data symbols than others. For example, Figure 13(a) shows a 4-element phased array steered at 30°. In the figure, D1-D4 represent data symbols. Antenna 1 is receiving D2 while the other antennas are receiving D1. Since D1 and D2 are independent, D2 is merely a distortion of D1, and the performance of the array degrades after beamforming. This phenomenon is called array ISI because a subsequent symbol (D2) interferes with the current symbol (D1).

The array ISI is not severe when the array has a low data rate (Figure 13(b)), small size (Figure 13(c)) or a small, steered angle (Figure 13(d)). This is because the low data rate reduces the symbol period, and smaller steered angles or small array sizes increase the maximum propagation delay. However, emerging communication standards require high data rates and large arrays, making array ISI a serious limitation.

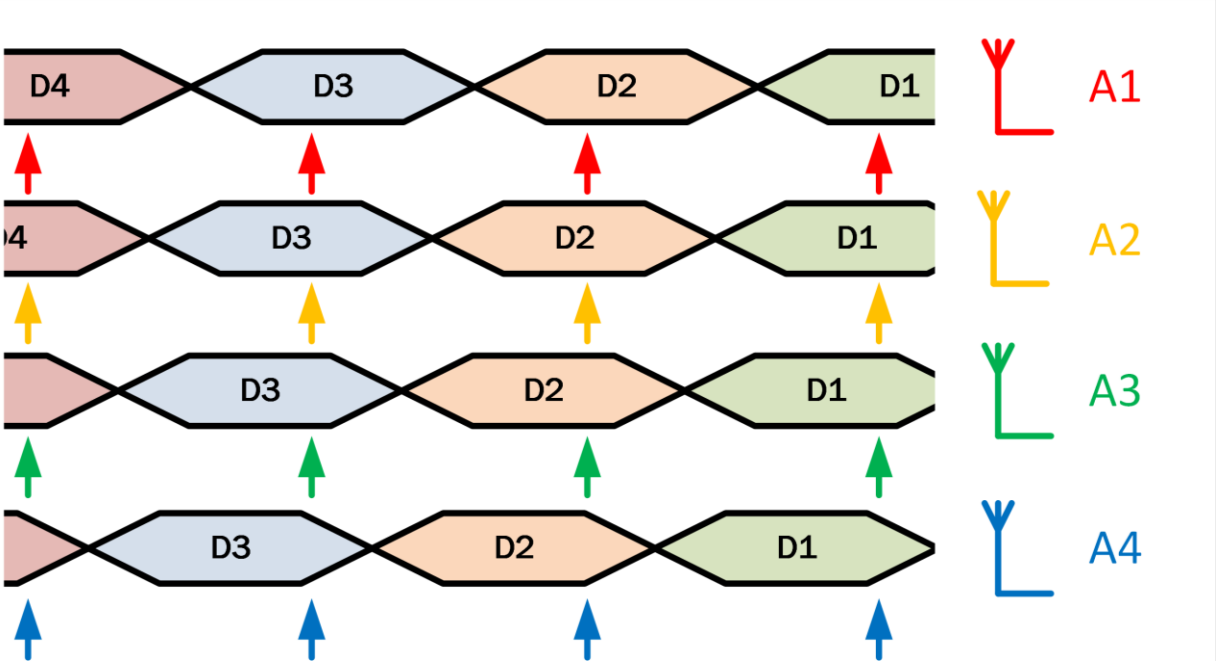

Figure 14. A 4-element uniform linear array without the array inter-symbol interference.

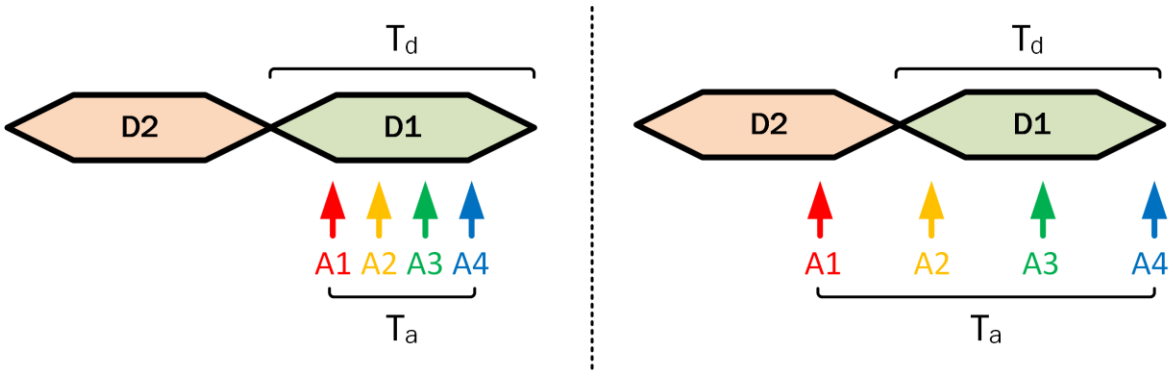

Figure 15. A simplified diagram (left) without and (right) with array inter-symbol interference.

Figure 14 gives an example of an array without the array ISI. In Figure 15(left), a simplified representation of Figure 14 with a single data stream is depicted. T_d is the symbol period, which is inversely proportional to the signal's bandwidth, and T_a is the maximum propagation delay difference across the array. In Figure 15(right), the array experiences array ISI as A1 receives D2 while A2-A4 receive D1. The array cannot avoid the array ISI when T_a is larger than T_d [32]. Therefore, the array needs to satisfy

$$T_d \gg T_a, \tag{21}$$

Based on (12), T_a can be expressed as follow for an array size of N and $\psi = 90°$.

$$T_a = (N-1) \times \frac{1}{2f_c} \tag{22}$$

T_d, the symbol period, can be expressed as follow for a double sideband signal such as QAM.

$$T_d = \frac{2}{BW} \tag{23}$$

where BW is the instantaneous bandwidth. With (22) and (23), (21) is equal to

$$\frac{2}{BW} \gg (N-1) \times \frac{1}{2f_c}. \tag{24}$$

This can be re-written as:

$$N \ll \frac{4f_c}{BW} + 1. \tag{25}$$

With (38), a maximum array size without the array ISI can be calculated. For example, the array size of a uniform linear array with a 1 GHz carrier frequency and 100 MHz bandwidth needs to be much smaller than 41 elements to avoid array ISI.

3.2. RF Timed Arrays

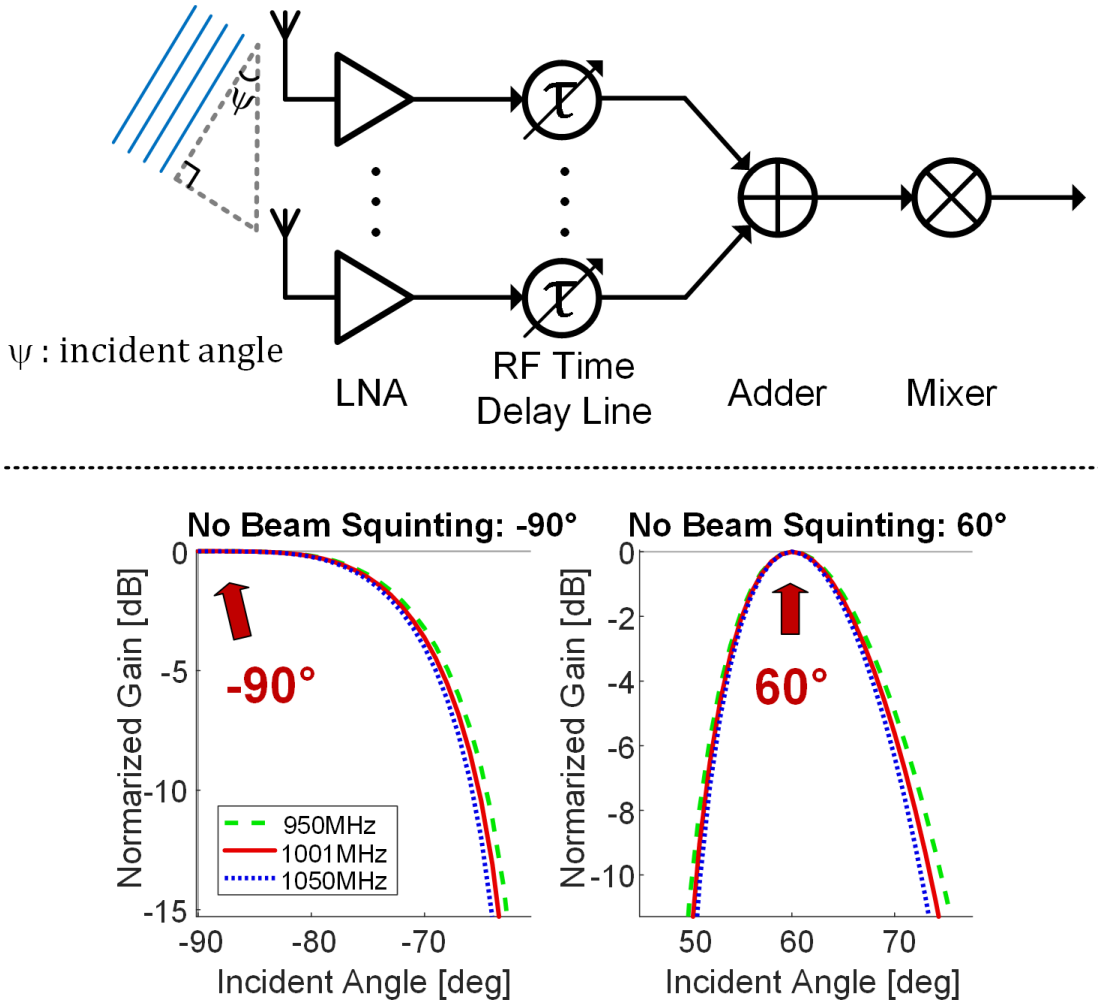

Figure 16. A system architecture of RF timed arrays and simulated beam patterns showing no squinting errors for 16 elements, 1 GHz center frequency, and a 100 MHz bandwidth.

By introducing time delay in the RF domain (Figure 16), RF timed arrays [34], [35] attempt to address the problems we discussed in 3.1.1. As shown in Figure 16(bottom), RF timed arrays eliminate beam squinting errors, however, they have their own set of challenges.

3.2.1. Limitations of RF Timed Arrays

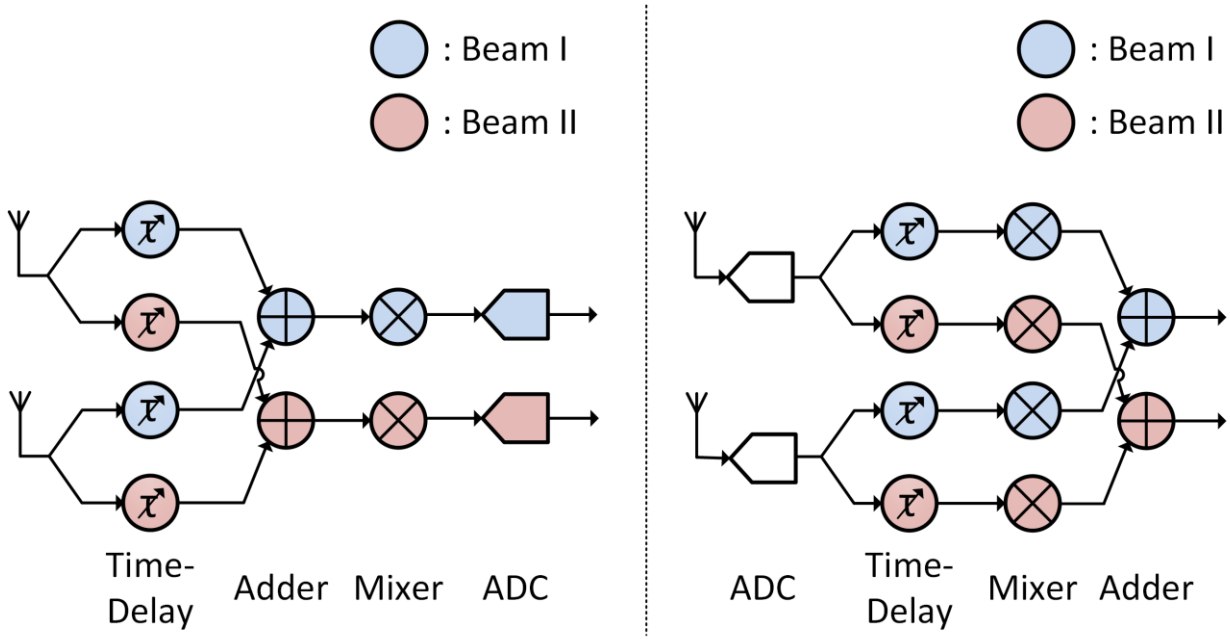

Figure 17. Multi-beam architecture examples for (left) RF beamforming and (right) digital beamforming.

The major challenge in the implementation of true-time-delay blocks lies in the small, chip area requirements [32]. For example, the transmission line (TL) based switched delay line introduced in [36] occupies 0.2 mm^2 per element because 1 mm of TL provides only 10 ps of delay. LC-based artificial TLs reduce area, but often suffer more than a 10% delay variation over the frequency range [37]. Inductor-less, RC-based all-pass filters have also been used in area reduction, but the resulting designs are still quite large. For example, [34] and [35] occupy 0.6 mm^2, 0.07 mm^2 per element, respectively. Furthermore, they can only support a single beam. Figure 17 compares multi-beam array architectures between RF and digital beamformers. For RF beamforming to be able to generate multiple beams, the SNR must decrease as the signal is split in the RF domain and signal power is lost. For example, in Figure 17(left), SNR decreases by 3 dB as the signal is split in two. In general, SNR decreases by 10 log M dB, where M is the number of beams. In contrast, as shown in Figure 17(right), digital beamforming can produce multiple

beams without any SNR penalties, as the signal is not split until after digitization [38]. In addition, TL-based time delay units are lossy. For example, [36] has 1 dB loss per mm. RC-based, all-pass filters also have high power consumption since high bandwidth, active amplifiers are used to implement the RF time delay. For example, [34] and [35] consume 52 mW, and 90 mW per element, respectively. RF time delay cells also have limited carrier frequency range; the time delay cells in [34] and [35] only operate up to 2.5 GHz, which is far below the mm-wave frequency. TL delay cells also suffer from PVT variation and require calibration. Finally, RF true-time-delay beamformers are not suitable for large array applications, due to their limited time delay range, which is 1.7 ns in [34] and 550 ps in [35]. For a 1 GHz center frequency, when the array elements are spaced by $\frac{\lambda}{2}$, they are 15 cm apart. It takes 500 ps for an electromagnetic wave to travel 15 cm. Thus, for a 1 GHz carrier, the maximum array size with a maximum time delay cell of 1.7 ns in [34] is limited to 4 elements. Furthermore, [35] can sonly support 2 element arrays for a 1 GHz carrier frequency with its 550 ps maximum time delay.

3.3. Baseband True-Time-Delay

As discussed in 3.1.1. and 3.2.1. , phased arrays and RF timed arrays have limitations such as beam squinting error, array ISI, high power consumption, and beam number. Baseband true-time-delay beamforming not only addresses these challenges, but also allows for digital beamforming, which is highly accurate, fast, and able to generate multiple beams. However, baseband timed array is complicated because baseband time delay is not equivalent to RF time delay.

3.3.1. The Problem with using Baseband Time Delay Alone

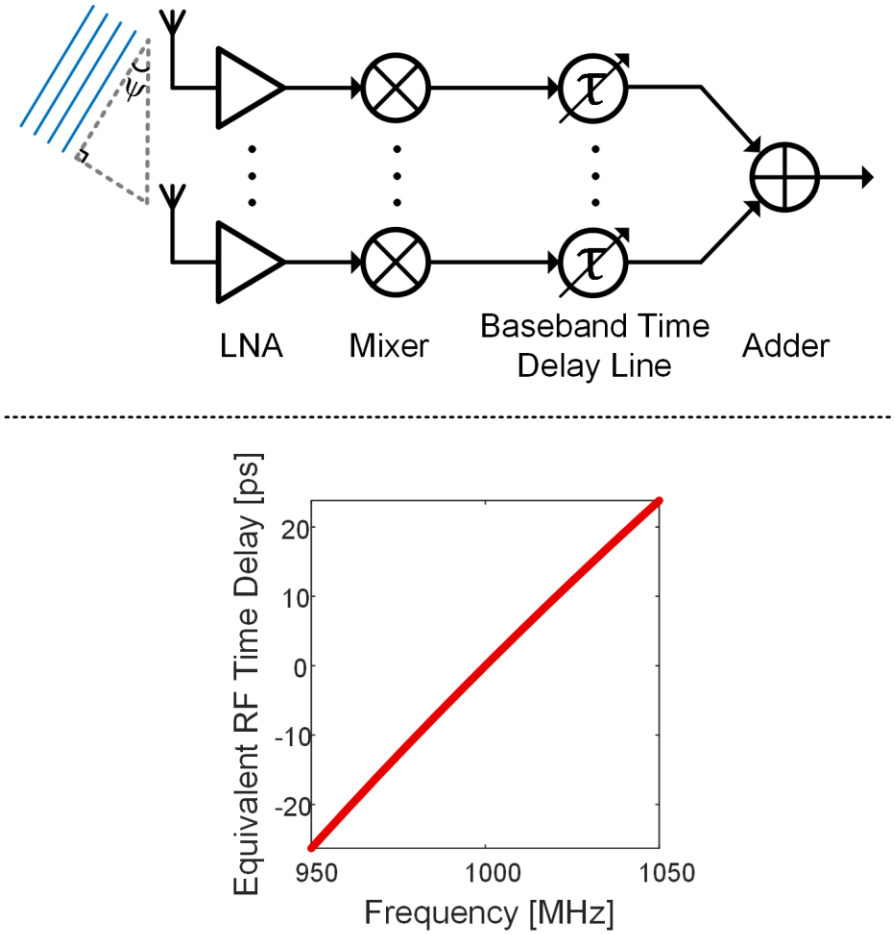

Figure 18. (top) System architecture of an array with baseband time delay alone and (bottom) equivalent RF time delay at 1 GHz for a baseband 500 ps time delay over ±50 MHz bandwidth.

To understand why baseband time delay alone does not give a true RF time delay, we must consider an array with baseband time delay alone in Figure 18(top). After down-conversion, the array obtains a low-frequency sine wave signal (I_{bb}) described below.

$$I_{bb} = \sin(\omega_{bb} t), \tag{26}$$

where bb stands for baseband. If we time delay I_{bb} by τ_d,

$$I_{bb}' = \sin(\omega_{bb}(t - \tau_d)) \tag{27}$$

$$= \sin(\omega_{bb} t - \omega_{bb}\tau_d). \tag{28}$$

Up-converting this signal by mixing with an LO signal, we get

$$I_{rf} = \sin((\omega_{bb} + \omega_{LO})t - \omega_{bb}\tau_d) \tag{29}$$

$$= \sin\left((\omega_{bb} + \omega_{LO})(t - \frac{\omega_{bb}}{\omega_{bb} + \omega_{LO}}\tau_d)\right). \tag{30}$$

As a result, Figure 18 shows that a baseband time delay τ_d corresponds to a RF time delay of $\frac{\omega_{bb}}{\omega_{bb}+\omega_{LO}}\tau_d$, which is much smaller than the baseband time delay τ_d but is also dependent on the baseband frequency ω_{bb}. To illustrate the problem with baseband time delay, Figure 18(bottom) shows the equivalent RF time delay for a 500 ps baseband time delay over a $\pm$50 MHz bandwidth centered at 1 GHz. In particular, for a DC signal ($\omega_{bb} = 0$), the equivalent RF time delay is always 0. A DC signal has a constant output voltage and does not change over time. Therefore, shifting or delaying a DC signal in the time domain does not result in a change in output value.

3.3.2. Combination of Baseband Time Delay and Phase-Shifting

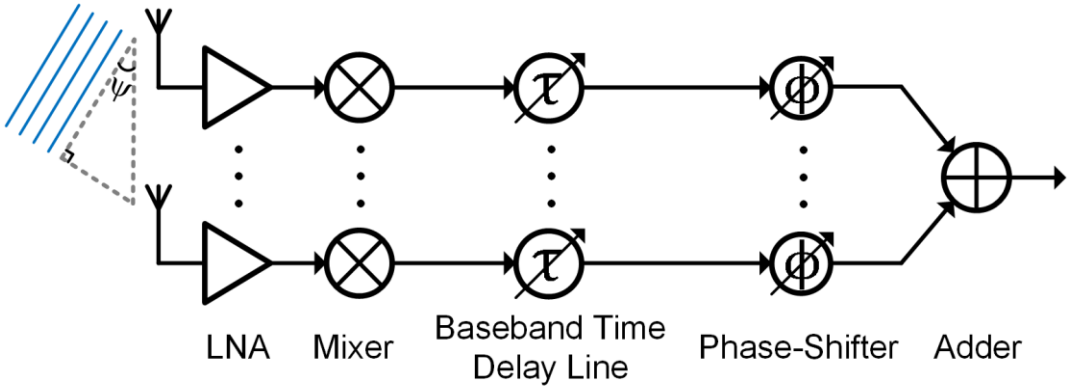

Figure 19. System architecture of a baseband true-time-delay beamformer.

A baseband beamforming technique introduced in 1992 solves the squinting and array ISI problems for acoustic beamforming [39]. By combining phase-shifting and time delay in the baseband (Figure 19), we can eliminate squinting. To understand this, we reformulate (30) to obtain

$$I_{rf} = \sin\left((\omega_{bb} + \omega_{LO})(t - \tau_d + \frac{\omega_{LO}}{\omega_{bb} + \omega_{LO}}\tau_d)\right) \quad (31)$$

$$= \sin((\omega_{bb} + \omega_{LO})(t - \tau_d) + \omega_{LO}\tau_d) \quad (32)$$

By introducing a phase-shift of $-\omega_{LO}\tau_d$ in (32), we get

$$I_{rf} = \sin((\omega_{bb} + \omega_{LO})(t - \tau_d)). \quad (33)$$

(41) shows that an RF time delay of τ_d can be achieved by time delaying a baseband signal by τ_d and phase-shifting the signal by $-\omega_{LO}\tau_d$, which is independent to the baseband signal frequency ω_{bb}. Regardless of the baseband frequency, an equivalent RF time delay τ_d can be achieved.

As we discussed in 3.1. , the k^{th} element in an array has a propagation delay of $-\tau_k$. To achieve an RF time delay of $-\tau_k$, we need to introduce a phase-shift of $\omega_{LO}\tau_k$ and a time delay of $-\tau_k$. For quadrature signals, phase-shifting can be achieved by multiplying the signals with a rotation matrix. Therefore, baseband true-time-delay operation for quadrature signals can be expressed in a matrix form as followed,

$$\begin{bmatrix} I_k(t) \\ Q_k(t) \end{bmatrix} = \begin{bmatrix} \cos(\omega_c\tau_k) & -\sin(\omega_c\tau_k) \\ \sin(\omega_c\tau_k) & \cos(\omega_c\tau_k) \end{bmatrix} \begin{bmatrix} I(t + \tau_k) \\ Q(t + \tau_k) \end{bmatrix} \quad (34)$$

where I_k and Q_k are the down-converted k^{th} quadrature signals. If we include the down-converting operation,

$$R_k(t) = [\cos(\omega_c t) \quad -\sin(\omega_c t)] \begin{bmatrix} \cos(\omega_c\tau_k) & -\sin(\omega_c\tau_k) \\ \sin(\omega_c\tau_k) & \cos(\omega_c\tau_k) \end{bmatrix} \begin{bmatrix} I(t + \tau_k) \\ Q(t + \tau_k) \end{bmatrix}, \quad (35)$$

where $R_k(t)$ is the received signal at the k^{th} element, and ω_c is the carrier frequency. This expression has the form:

$$R_k = \text{Carrier} \times \text{Phase-Shift} \times \text{Delayed Baseband} \quad (36)$$

We also note that for a narrowband signal, $-\tau_k$ is negligible and (35) becomes conventional phased array beamforming.

Chapter 4 Implementation

4.1. Bit Stream Processing (BSP)

Bit stream processing (BSP) was first proposed by Wong [40]. The idea is to replace power-hungry digital multipliers, with power and area efficient multiplexers, by using delta-sigma modulators. As an example, let us consider a delta-sigma modulator that generates a 1-bit bit stream as in Figure 20. When the bit stream is multiplied by a constant multiplicand (M in Figure 20), the product results in a 2-level signal (M or 0). This multiplication can be performed with a 2:1 MUX as shown in Figure 20 by selecting either M or 0. The combination of bit stream processing and delta-sigma modulators significantly reduces both power and area of DBF [9].

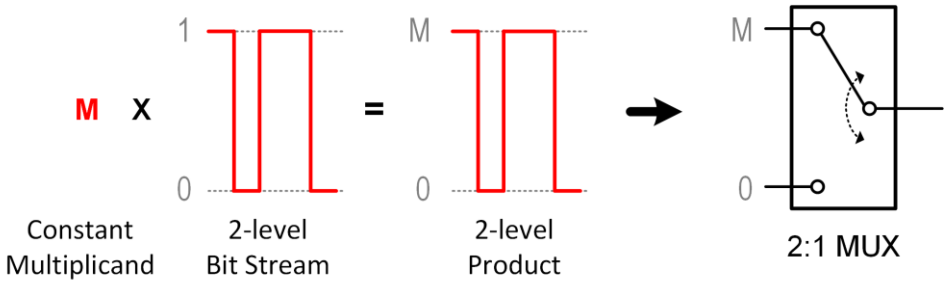

Figure 20. Example of multiplication in Bit Stream Processing (BSP) with a 2-level bit stream.

To understand bit stream beamforming, we first consider a more conventional digital beamformer architecture with conventional DSP and low-pass delta-sigma modulators as shown in Figure 21(a). Analog mixers down-mix the receive signals and then low-pass delta-sigma modulators convert the down-mixed signals to bit streams. Decimators convert the bit streams to low-sample-rate high-resolution digital signals. Phase-shifting through digital multiplication and finally, addition of the phase-shifted signals generates a beam.

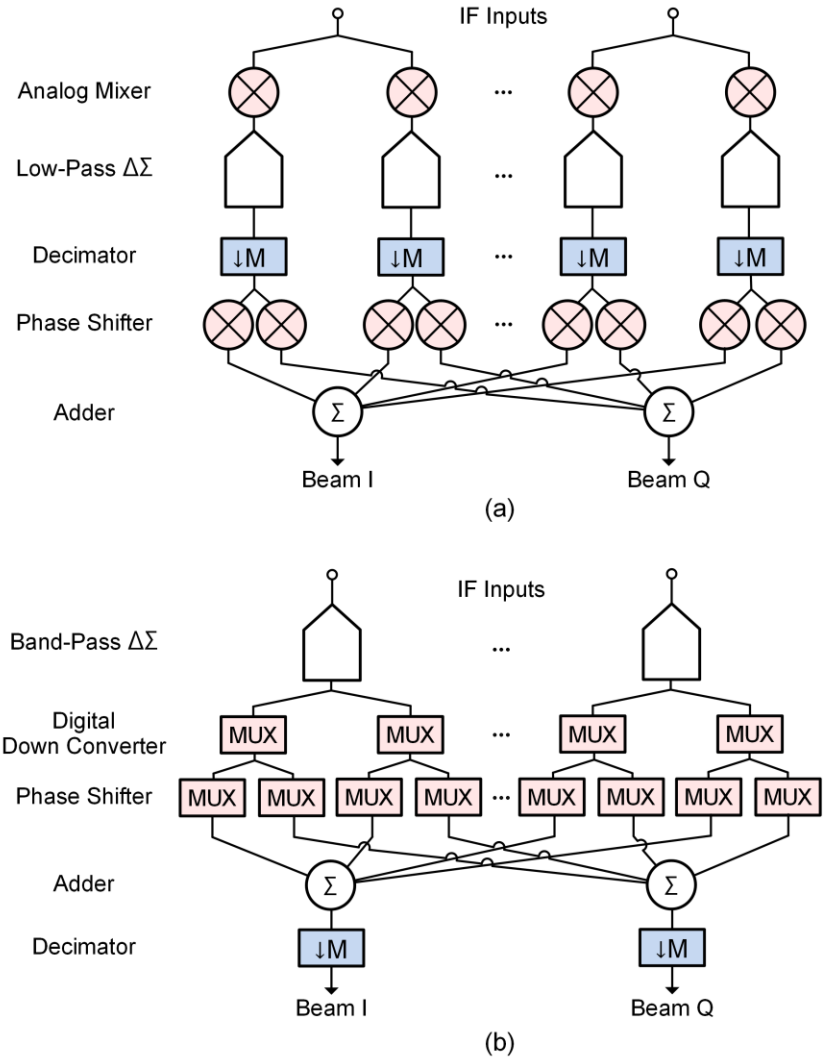

Figure 21. Digital beamformers in (a) DSP and (b) BSP implementations.

In contrast, BSP implements high-speed digital multiplication with simple multiplexers (MUX) operating directly on the low-resolution bit streams from band-pass ADCs (Figure 21(b)), removing the need for a power and area-hungry digital multipliers and decimator in each channel [9]. A BSP digital down-converter (DDC) directly down-converts the bit stream from IF to base-band, by multiplying the bit stream with a digital local oscillator (LO) signal. The low resolution quantizer in the CTBPDSM generates the 5-level (-2, -1, 0, 1, 2) bit stream. A sampling frequency 4 times higher than the LO frequency results in a sampled LO signal represented by three levels (-1, 0, 1) as shown in Figure 22(a). In [9], this multiplication operation is implemented with a 3:1

MUX using the three-level LO as the MUX select. The product of the multiplication between the 3-level LO and the 5-level bit stream remains a 5-level signal.

Complex weight multiplication (CWM) can be expressed in a matrix form as:

$$\begin{bmatrix} I_k' \\ Q_k' \end{bmatrix} = \begin{bmatrix} \cos(k\theta) & \sin(k\theta) \\ -\sin(k\theta) & \cos(k\theta) \end{bmatrix} \begin{bmatrix} I_k \\ Q_k \end{bmatrix} \tag{37}$$

$$\theta = 2\pi f_c \frac{d\sin\psi}{c}, \tag{38}$$

where I_k and Q_k are the down-converted signals from the k^{th} element, I_k' and Q_k' are the phase-shifted outputs, and the θ is a constant phase for a given incident angle (ψ)and center frequency (f_c) as represented in (38). Because multiplication in CWM scales the bit stream with a weight ($\cos(k\theta)$ or $\sin(k\theta)$) it is efficiently implemented with a 5:1 MUX with the bit stream as the MUX select (Figure 22(b)).

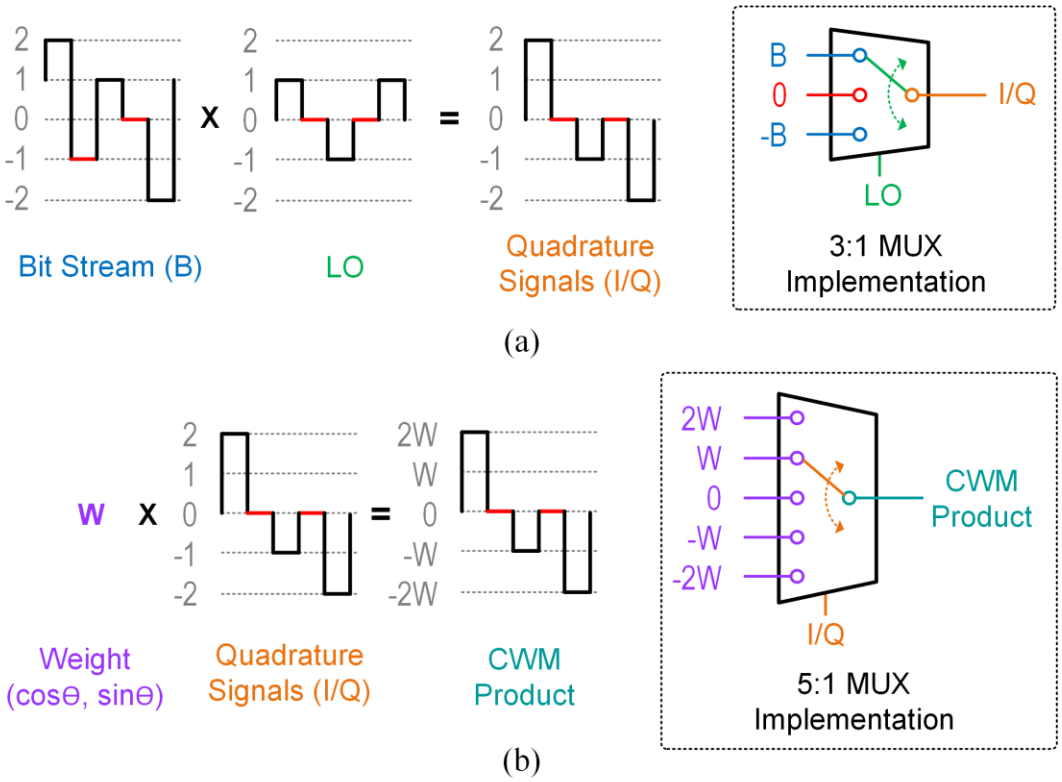

Figure 22. MUX-based (a) digital down-conversion and (b) complex weight multiplication (CWM) implementation in BSP.

An important advantage of BSP is the reduced number of decimators. As shown in Figure 22(a), in the DSP approach each antenna element requires a decimator, however, with BSP there is only one decimator per beam (Figure 22(b)). This is an advantage because a high-speed decimator requires extensive high-speed addition, which consumes a significant amount of power. It is shown in [9] that the decimation filters consume 87% of the DBF power in a conventional DSP implementation. Thanks to the reduced number of decimators and MUX-based multiplication, the 8-element 2-beam digital beamformer in [9] reduces power consumption by 64% and area by 68% compared to a conventional DSP implementation.

4.2. Interleaved Bit Stream Processing (IL-BSP)

The ADC in this work digitizes the received signals at 4 GS/s for a 100 MHz bandwidth. This also requires the digital circuitry to run at 4 GHz, which is challenging for the BSP MUX logic and especially challenging for the decimators. While the adders in the decimators have input bit-widths more than 20-bit, 40 nm CMOS can only perform an 8-10 bits addition in one clock cycle with 40 ps of setup and hold time [41]. To address this challenge, we introduce Interleaved BSP (IL-BSP) to halve the clock rate and reduce both power and area significantly.

IL-BSP performs a two-stage decimation with an initial decimation by 2 at the digital down conversion, to reduce the subsequent digital processing rate to 2 GHz. As we will see, this initial decimation by 2 is very efficient because it takes advantage of the nulls in the noise transfer of the band-pass modulator, and also exploits a nearly free two-stage CIC (Cascaded Integrated Comb) filter in the digital down conversion to baseband I and Q signals. After this 2x decimation, complex weight multiplication, summation and final decimation of the beam signals run at 2 GHz.

The initial decimation by 2 takes advantage of the fortuitous aliasing of noise shaping nulls

in the band-pass modulator. For band-pass modulators, the center frequency is chosen to be one fourth of the sampling frequency to facilitate efficient digital down-conversion. With this ratio of center and sampling frequencies, the sampled LO waveforms can be represented by -1, 0 and 1, so that DDC can be implemented with simple MUXes.

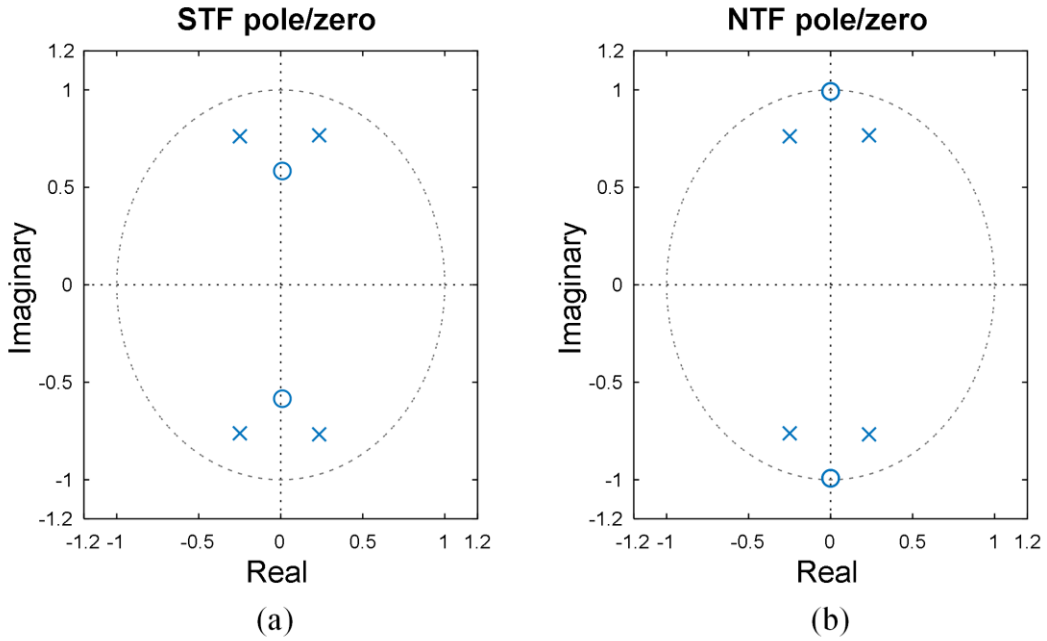

Figure 23. (a) STF and (b) NTF pole/zero placement of the 4th order band-pass delta-sigma modulator.

To understand the decimation process, we first consider the NTF of the band-pass modulator and the corresponding down-mixed NTF. Figure 23 shows the pole and zero placement for the 4th order band-pass modulator in this work. Because the NTF zeros of the band-pass modulator occur in complex conjugate pairs, the NTF of the 4th order band-pass modulator has two zeros at 1/4 F_s and two more zeros at 3/4 F_s (Figure 23(b)) [42].

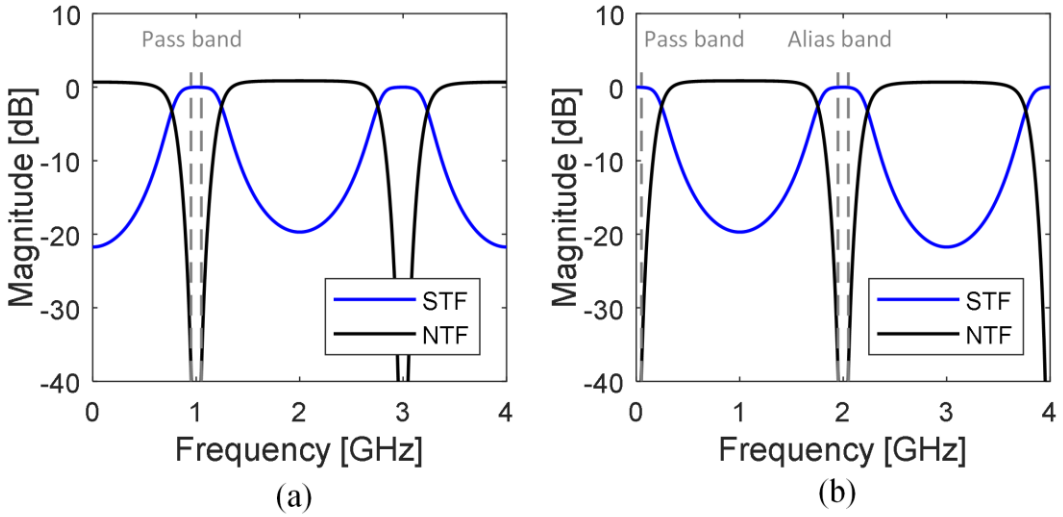

Figure 24. Frequency domain representation of (a) quantization noise from the 4th order band-pass ΔΣ, and (b) after down-mixing.

Therefore, the 4th order band-pass modulator shapes quantization noise from 1/4 F_s and 3/4 F_s with a -40 dB/decade slope as shown in Figure 24(a). Down mixing of the band-pass NTF with the 1/4 F_s LO leads to the NTF in Figure 24(b), with noise shaping nulls at DC, $F_s/2$ and F_s. Down-sampling by 2 to a sampling rate of $F_s/2$ takes advantage of the fact that the noise null at $F_s/2$ aliases onto the signal of interest.

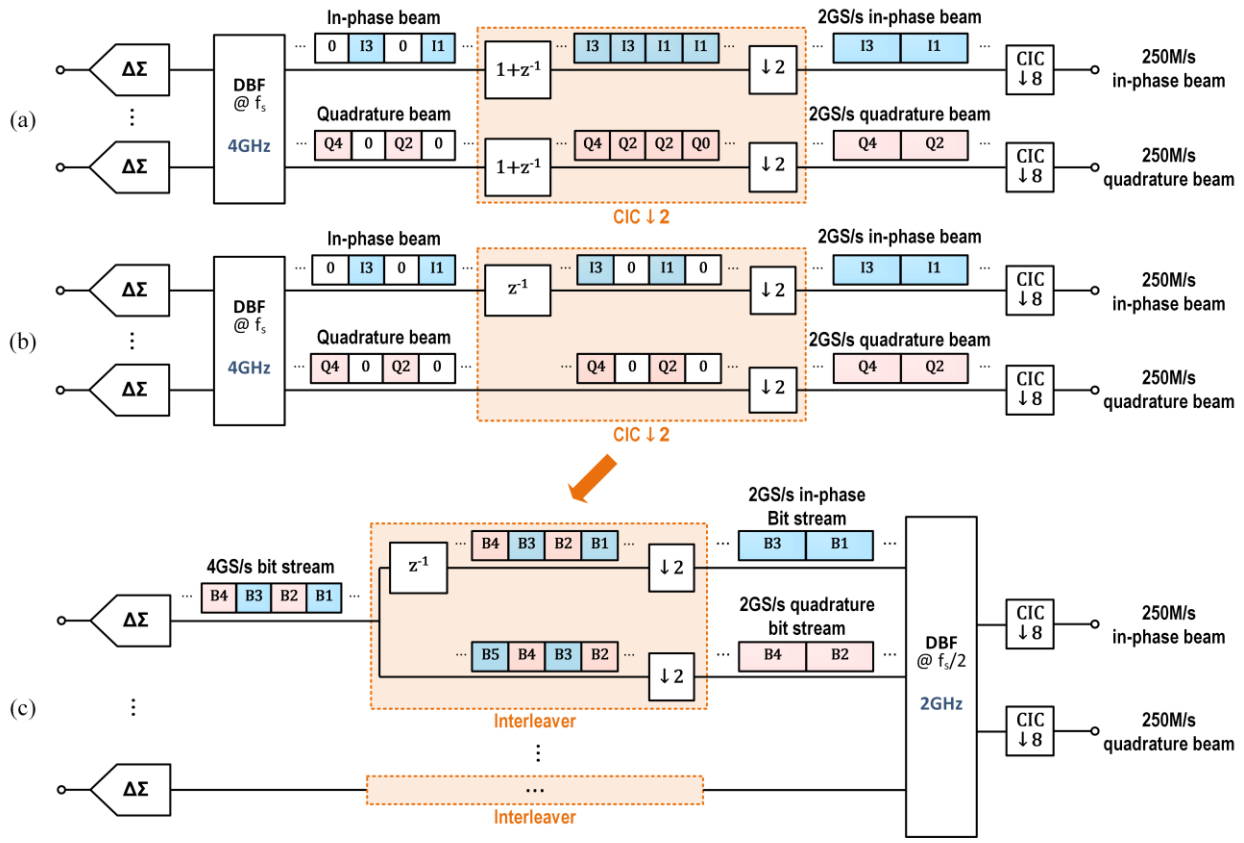

Figure 25. (a) A 2-stage CIC filter and (b) an equivalent implementation of the filter following a bit stream processing DBP block. (c) Interleaved bit stream processing DBF with an interleaver in front of the DBF block.

A low-cost two-tap CIC filter takes advantage of the 0's in the LO sequence to further minimize any aliasing artifacts associated with down mixing. This allows the down-mixing to baseband I and Q, and the down-sampling by 2, to be combined in an elegant way. The transfer function of a 1st order CIC decimation filter is expressed as follows:

$$H(z) = \frac{1 - z^{-2}}{1 - z^{-1}} = 1 + z^{-1}. \tag{39}$$

We begin by considering a 1st order CIC decimation filter and a 2x decimator placed after the digital down conversion and DBF to generate half rate I and Q signals (Figure 25(a)). Because every other LO value is always zero (see Figure 25(a)), every other I/Q value and every other I/Q beam value are also zero. Due to these zero values, the CIC filter block $(1 + z^{-1})$ repeats each value twice and the subsequent down-sampler simply samples one of these repeated values to

produce a 2 GS/s beam. More efficiently, the approach in Figure 25(b), simplifies the filter and decimator with a digital delay (z^{-1}) to produce the same I/Q beams with reduced circuit complexity.

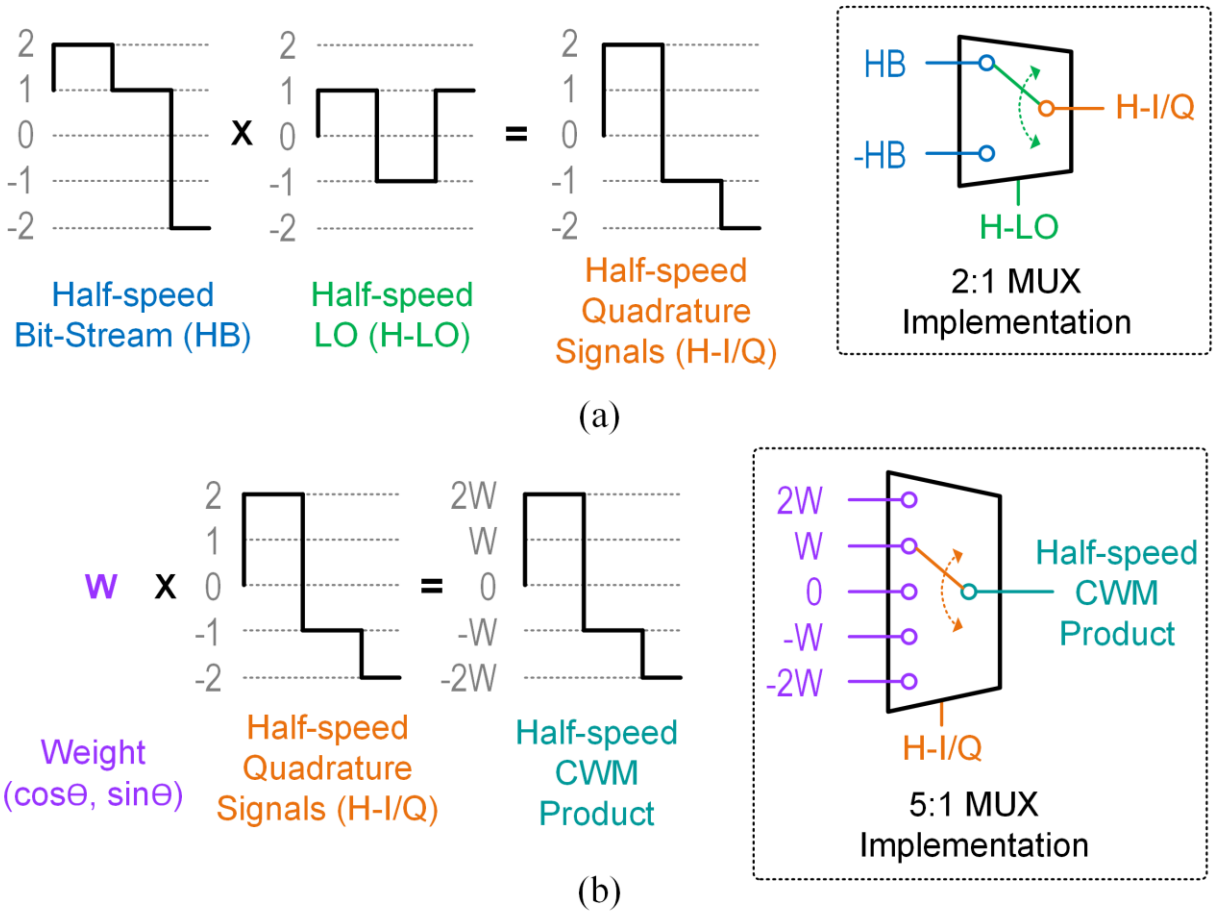

Figure 26. MUX-based (a) digital down-converting and (b) complex weight multiplication implementation in interleaved bit stream processing.

IL-BSP (Figure 25(c)) moves the digital delay and the 2x down samplers of Figure 25(b) to the front of the DBF block. The combination of the digital delay and down samplers acts as an interleaver that outputs the even-numbered data as I, and the odd-numbered data as Q. The interleaver allows the digital beamformer to run at half speed without losing any performance or accuracy (Figure 26). Removing the zeros means ignoring all zero value LO inputs to the DDC.

Therefore, DDC is implemented with a 2:1 MUX, driven by the LO values, simplifying circuit implementation and reducing power consumption.

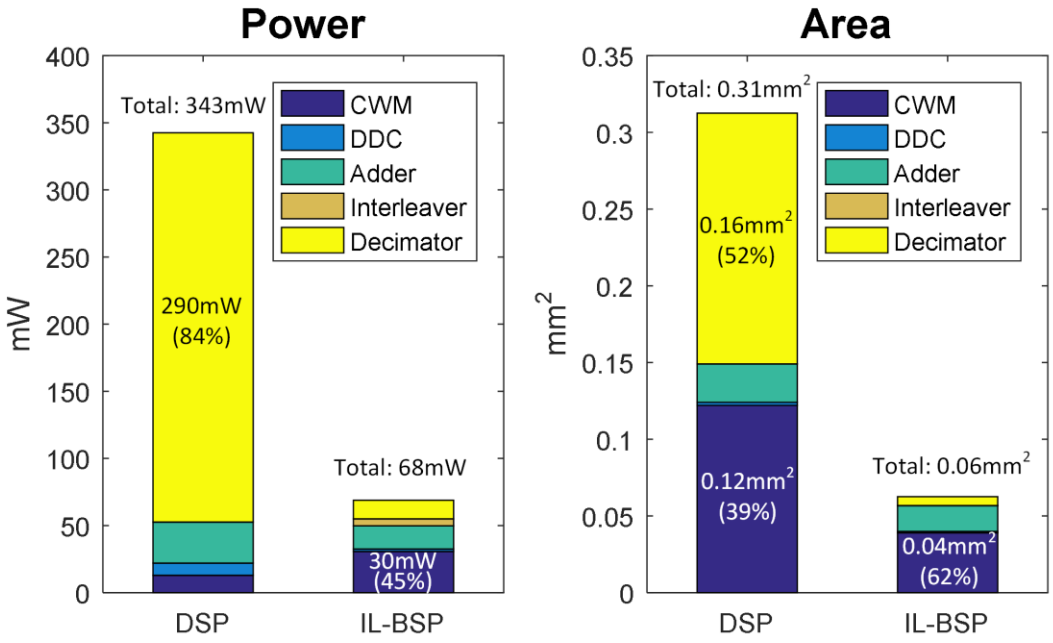

Figure 27. Power and area comparison between DSP and IL-BSP.

Figure 27 compares power and area of 16-element 4-beam 1GHz-IF digital beamformers implemented with a conventional DSP approach and with the IL-BSP approach. The 16 decimators in DSP consume 84% of the total digital power and occupy 52% of the total area. Although the DDC and CWM in IL-BSP dissipate a comparable amount of power to DDC and CWM in DSP, the IL-BSP decimators only consume 14 mW, which is far lower than 290 mW for the DSP decimators. Moreover, MUX-based multiplication in IL-BSP reduces the area of CWM by 68%. Consequently, IL-BSP reduces both power and area by 80% compared to a conventional DSP implementation. The entire IL-BSP digital beamformer with 16 elements and 4 beams consumes only 68 mW and occupies 0.0625 mm^2.

4.3. True-Time-Delay Digital Beamformer

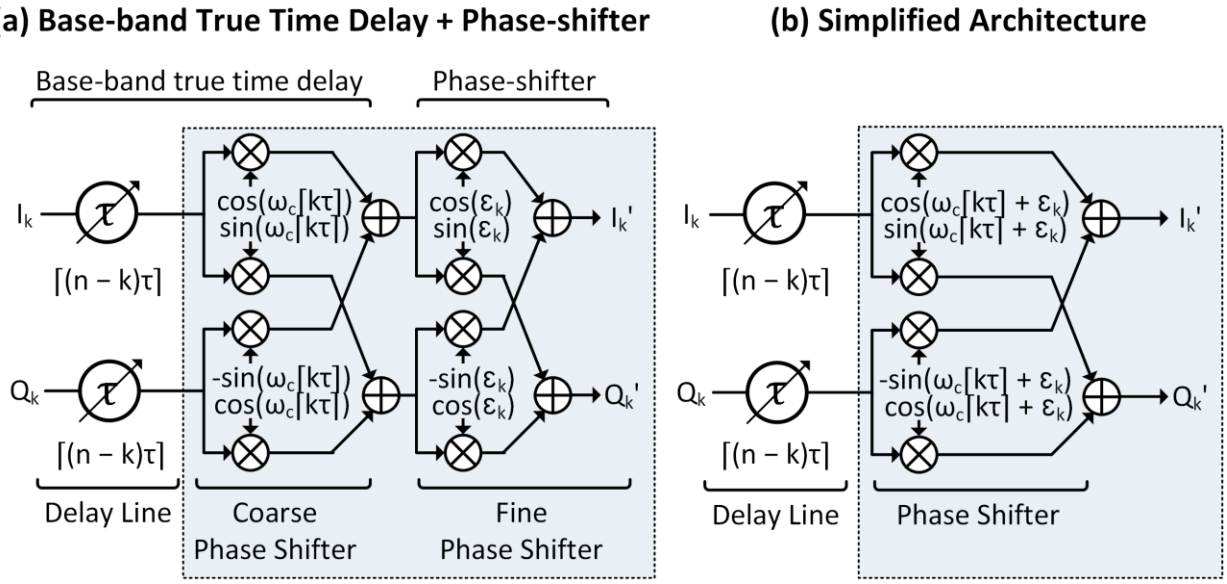

Figure 28. A hybrid digital beamforming architecture combining true-time-delay and phase-shifting.

As discussed in 3.3.2. , a base-band true-time-delay beamformer requires a time delay by $-k\tau$ and a phase-shift by $\omega_c k\tau$. In practice, a causal system cannot implement a negative time delay $-k\tau$. We add a constant time delay $n\tau$ to each element, making all the delays, $(n-k)\tau$, positive. Also, the resolution of the time delay is limited by the rate of the digital stream. In our system, the digital time delay has a resolution of 500 ps. Thus, instead of the ideal time delay of $(n-k)\tau$, where n is the array size, we delay by the closest number of digital increments, which we denote by $\lceil(n-k)\tau\rceil$. This shift differs from the ideal time delay by a small amount. To compensate for this small missing delay we introduce a small phase-shift ε_k (Figure 28(a)).

This hybrid approach combines the advantages of true-time-delay with the simplicity of compact size phase-shifting. This phase-shift combines with the phase-shift of $\omega_c\lceil k\tau\rceil$ to give a total phase-shift of $\omega_c\lceil k\tau\rceil + \varepsilon_k$. In our digital pipeline, we reduce to baseband, then delay by $\lceil(n-k)\tau\rceil$ increments, and shift phase by $\omega_c\lceil k\tau\rceil + \varepsilon_k$ (Figure 28(b)). This trading of a small time delay error for a small phase doesn't introduce any noticeable squinting.

Chapter 5 Prototype-I (Phased Array)

5.1. System Architecture

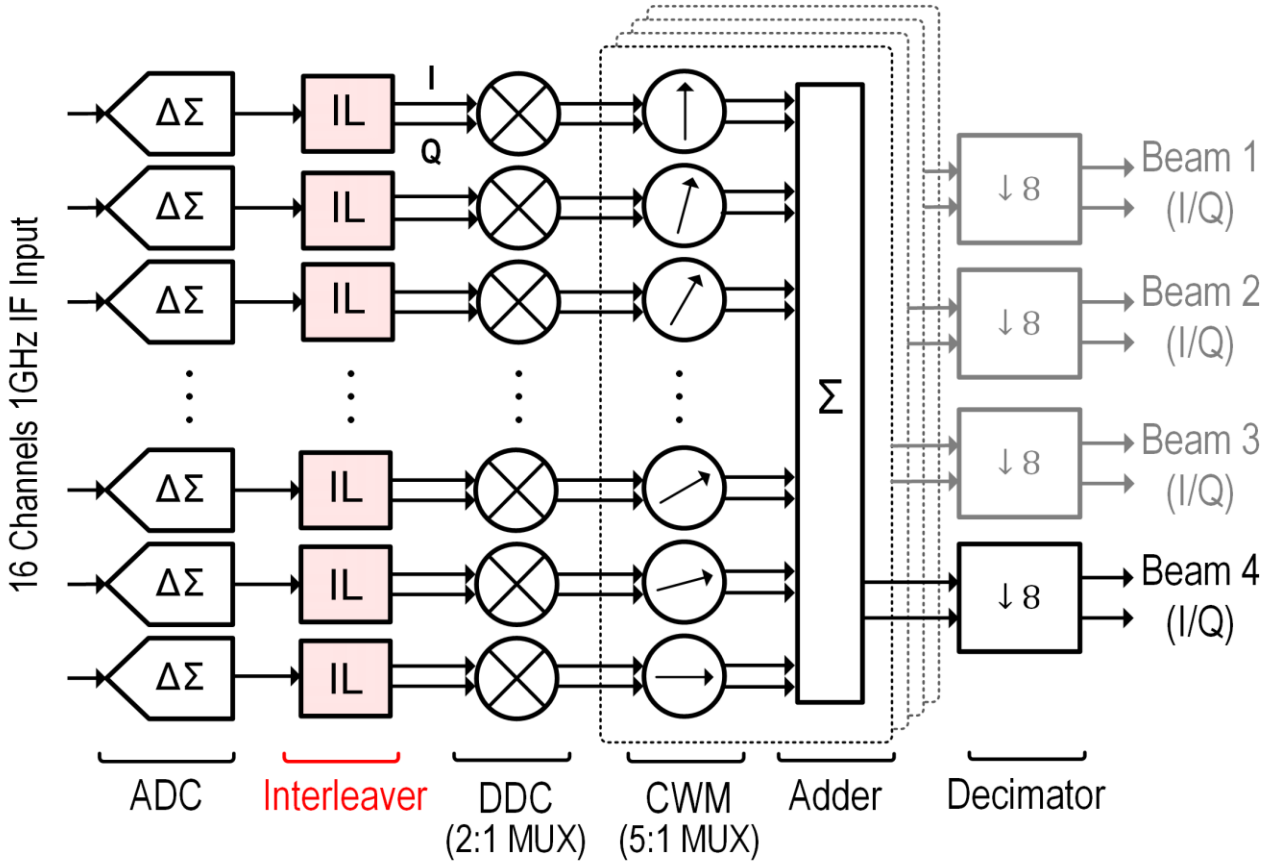

Figure 29. System architecture of the prototype digital beamformer.

As shown in Figure 29, the 16-element 100 MHz bandwidth digital beamformer generates 4 simultaneous beams. The 16 CTBPDSMs digitize the 16 1 GHz IF inputs to create 4 GS/s 5-level bit streams. The interleavers halve the data rate by interleaving the digitized bit streams into 2 GS/s quadrature signals. The 2:1 MUX-based DDCs down-convert the quadrature signals to base-band without adding noise or mismatch. The CWMs shift phase of the down-converted

signals with complex weights set by 6-bit registers, resulting in a 0.02° main beam direction resolution. After phase-shifting, the adder creates 2 GS/s quadrature beams. Finally, the decimators produce 13-bit 125 MS/s quadrature beams. The prototype digital beamformer has 4 sets of 16 CWMs, adders, and decimators, to produce 4 independent simultaneous beams for MIMO.

5.2. Measurements[3]

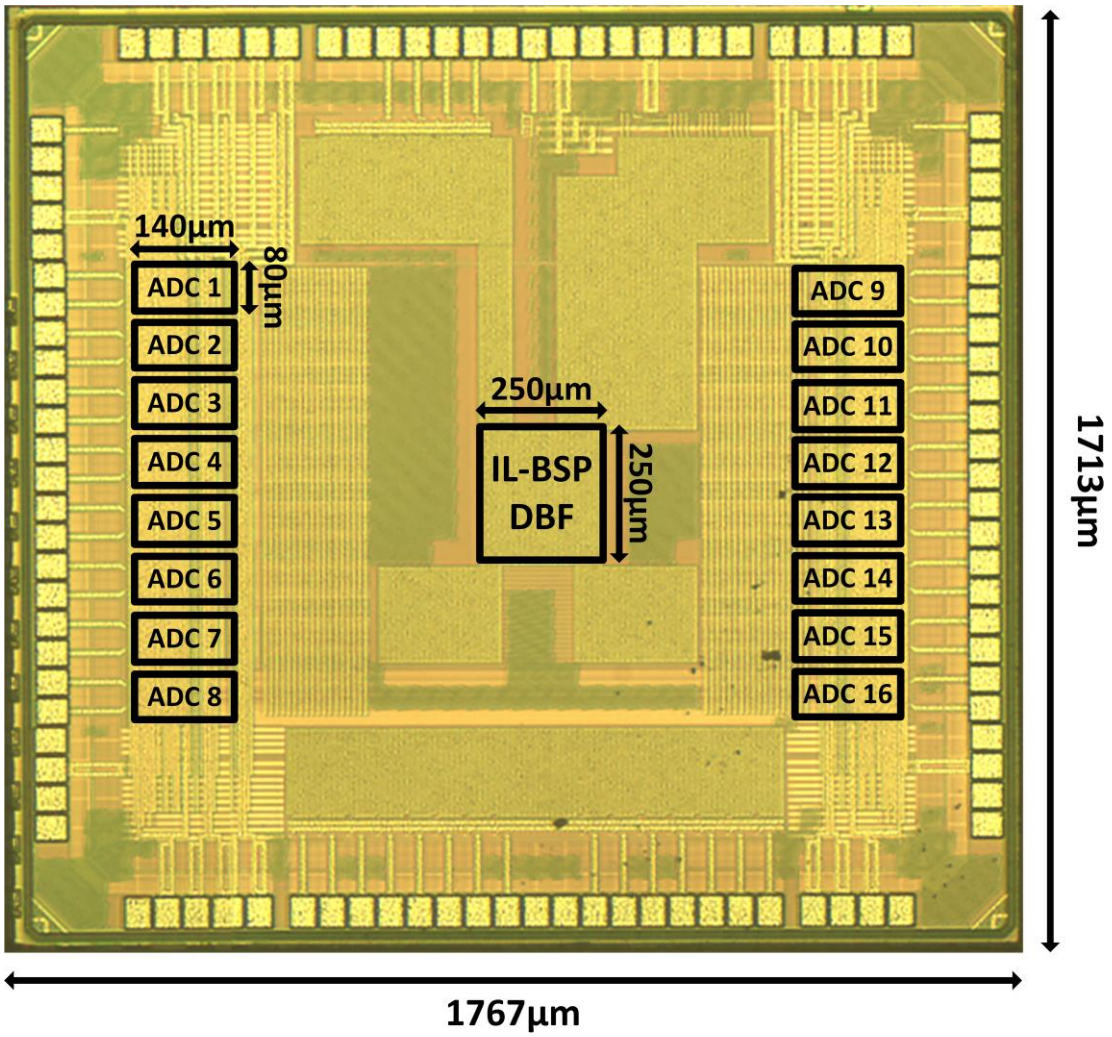

Figure 30. Die micrograph (0.24 mm^2 of active area in 40 nm CMOS).

[3] The measurements were made in collaboration with Rundao Lu.

Figure 30 shows a die micrograph of the prototype 16-element digital beamformer. The prototype is fabricated in 10-metal 40 nm CMOS and packaged in an 88-lead QFN package. It occupies a core area of 0.24 mm^2, including the 16 CTBPDSMs and the DBF circuitry.

5.2.1. Wireless Test

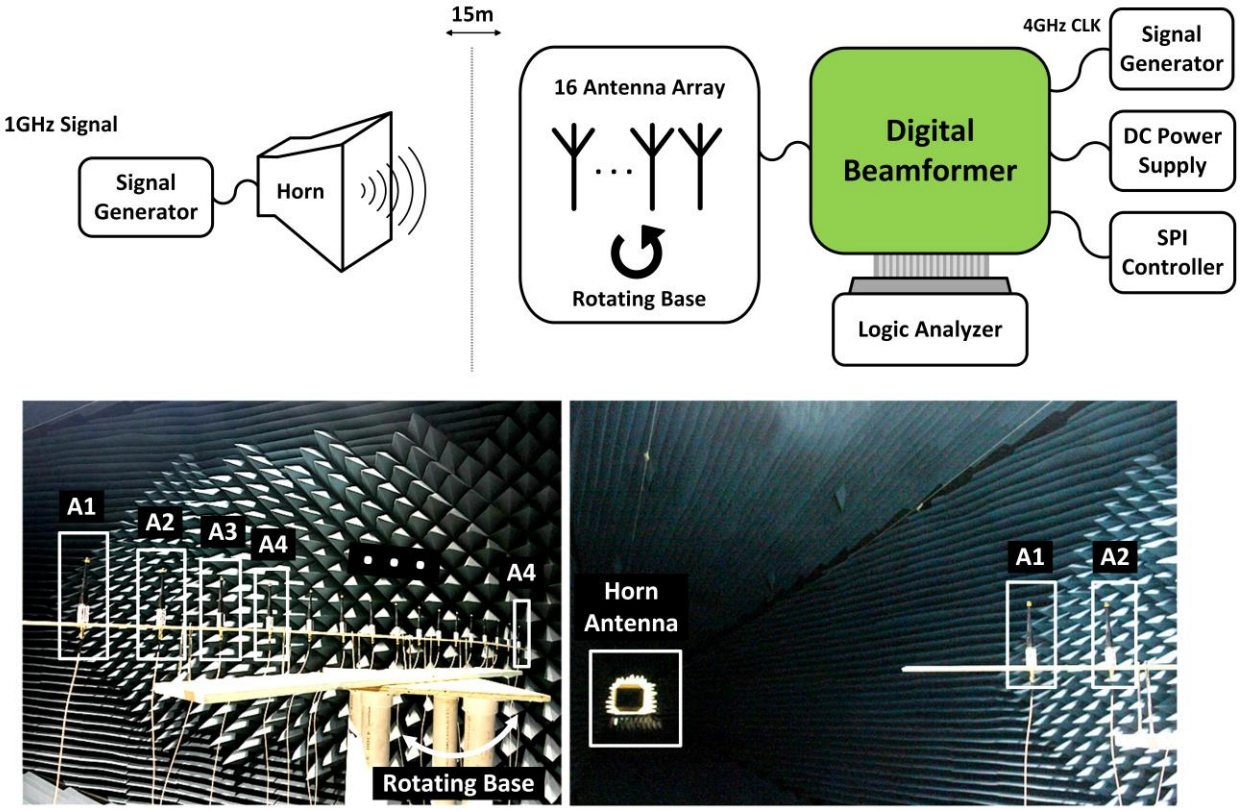

Figure 31. (top) Anechoic chamber test setup and (bottom) pictures showing 16 quarter-wave whip antennas (A1-A16), spaced at λ/2 (15 cm) increments on a rotating base.

The resistive input and continuous time operation allow the prototype device to be directly connected to a linear array of 16 quarter-wave whip antennas, spaced at λ/2 increments, without external LNAs. The 16-element antenna array is placed on a rotating base in an anechoic chamber to measure azimuth beam patterns (Figure 31). A horn antenna with antenna gain of 15 dBi

transmits a 15 dBm 1.006 GHz continuous wave signal from a distance of 15 m. An array of whip antennas each with an antenna gain of 1.3 dBi receives the -25 dBm signal.

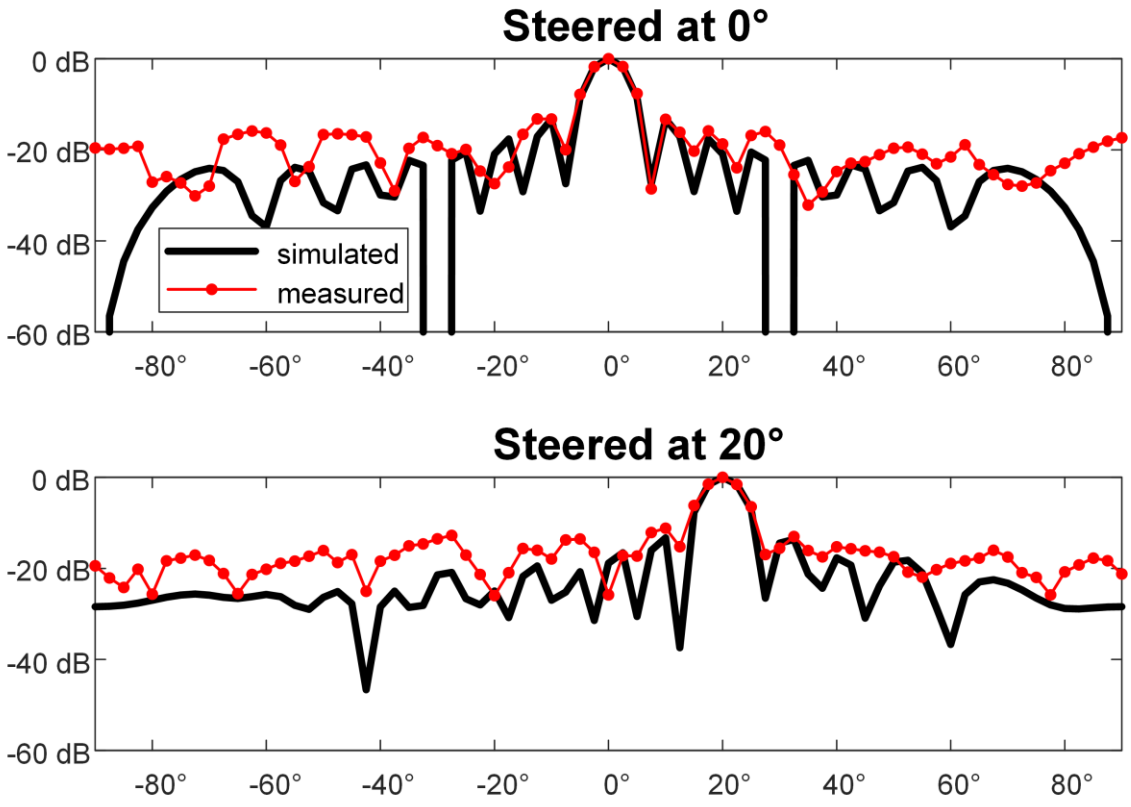

Figure 32. Measured and simulated beam patterns of wireless test for 0° and 20° steered angles (input frequency: 1.006 GHz).

Beam patterns are measured over incidence angles from -90° to 90° with a step size of 2.5°. This wireless test is performed without an RF front-end. The RF signal is fed directly into the resistive input of the continuous-time ADCs. The ADC noise figure is 26 dB. Figure 32 shows the measured beam patterns overlaid on ideal beam patterns in the log domain. The beam patterns are normalized. Ideally, the receiver is expected to achieve 55.4 dB SNR. The outer antennas of the 2.25 m antenna array receive significant echoes because they are outside of the 1 m quite zone of the anechoic chamber, resulting in some discrepancy between the ideal and measured patterns. Moreover, echoes and return loss from the 2 m long antenna cables also cause measurement errors.

5.2.2. Wired Test

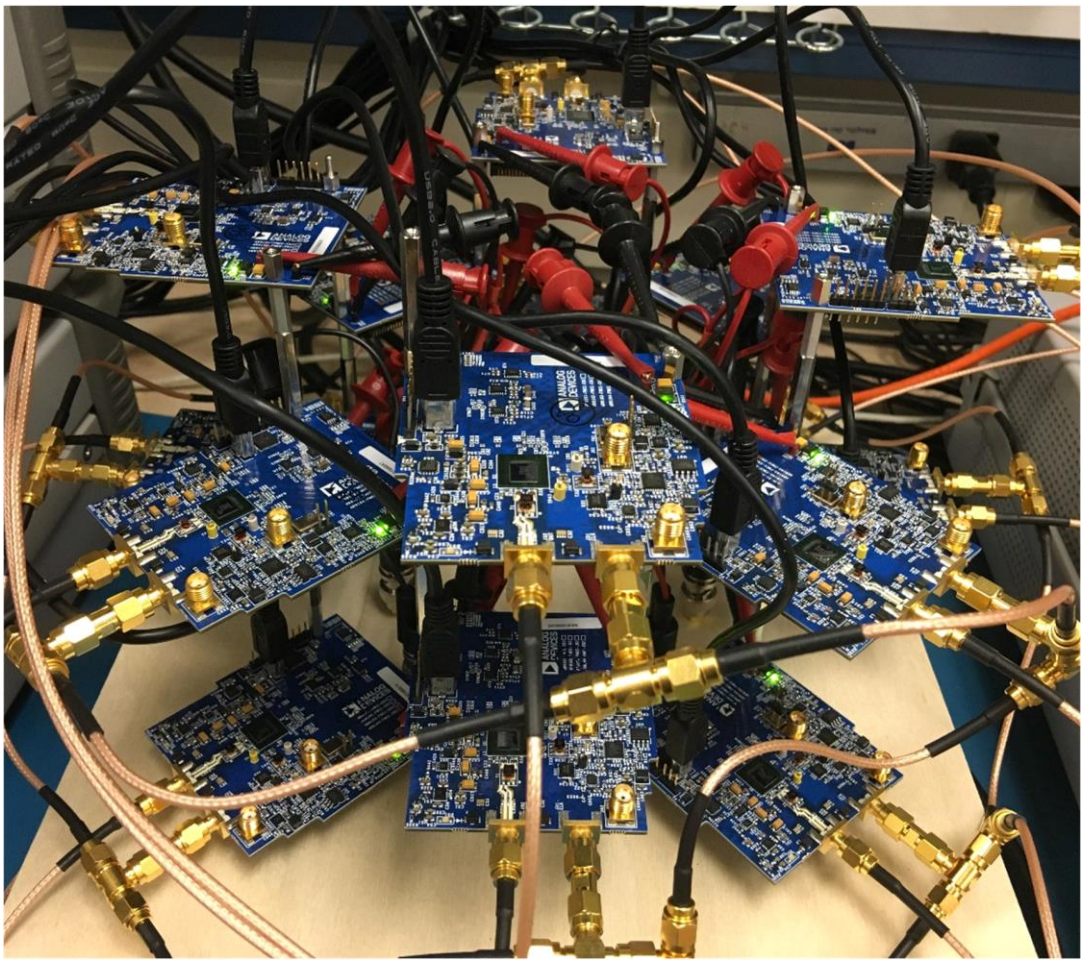

Figure 33. 16 AD9164 DDS boards generate 16 synchronized 1 GHz signals.[4]

To measure beam patterns without the non-idealities of the anechoic chamber, we generate an array of 16 poly-phase input 1 GHz signals with 16 high-performance direct digital synthesizers (DDSs) shown in Figure 33.

[4] This DDS beam-pattern generation system was design and implemented by Rundao Lu and Justin Correll.

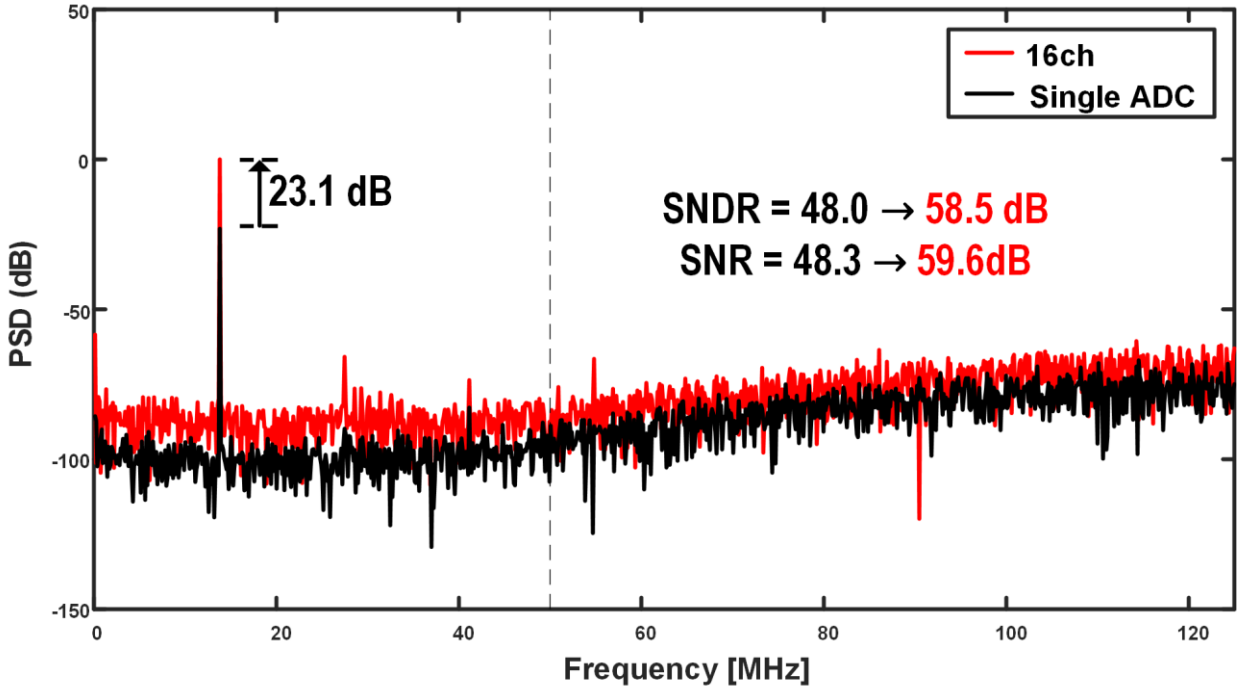

Figure 34. Measured power spectral density of a single CTBPDSM and overall 16-element beamformer (input frequency: 1.013 GHz).

As shown in Figure 34 the average measured single ADC SNDR over a 100 MHz bandwidth is 48.0 dB. The overall 16-element array achieves a measured SNDR of 58.5 dB which corresponds to a 10.5 dB improvement from the array. The measured array gain is 11.2 B, with 59.6 dB SNR from the entire array.

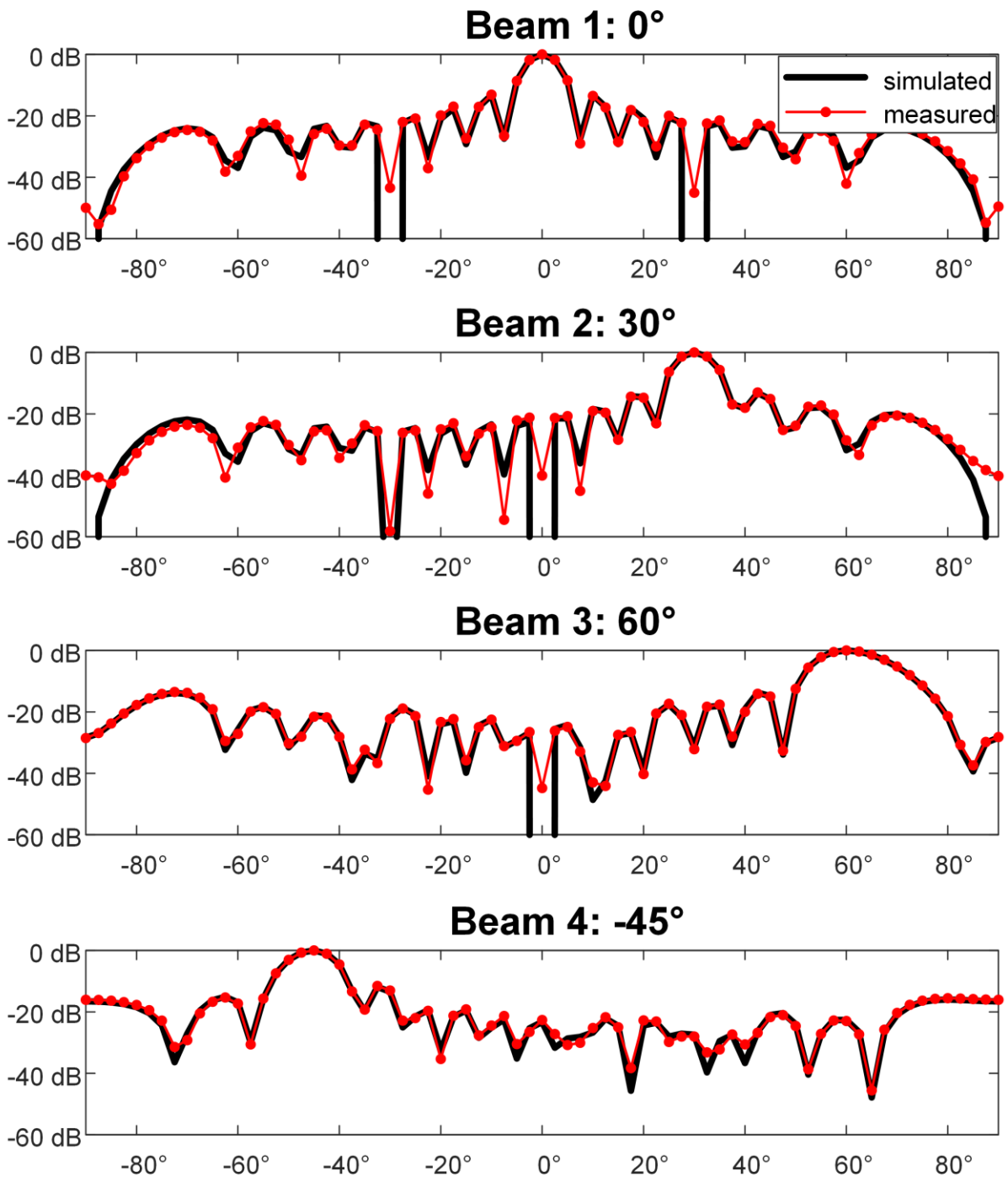

Figure 35. Measured and simulated 4 independent simultaneous beams steered at different angles (input frequency: 994 MHz).

Figure 35 shows four measured simultaneous independent beam patterns with different incident angles (0°, 30°, 60°, and -45°). The measured beam patterns are near-ideal, with a half-power beam width of 10°-15° for a +/- 60° incident angle range.

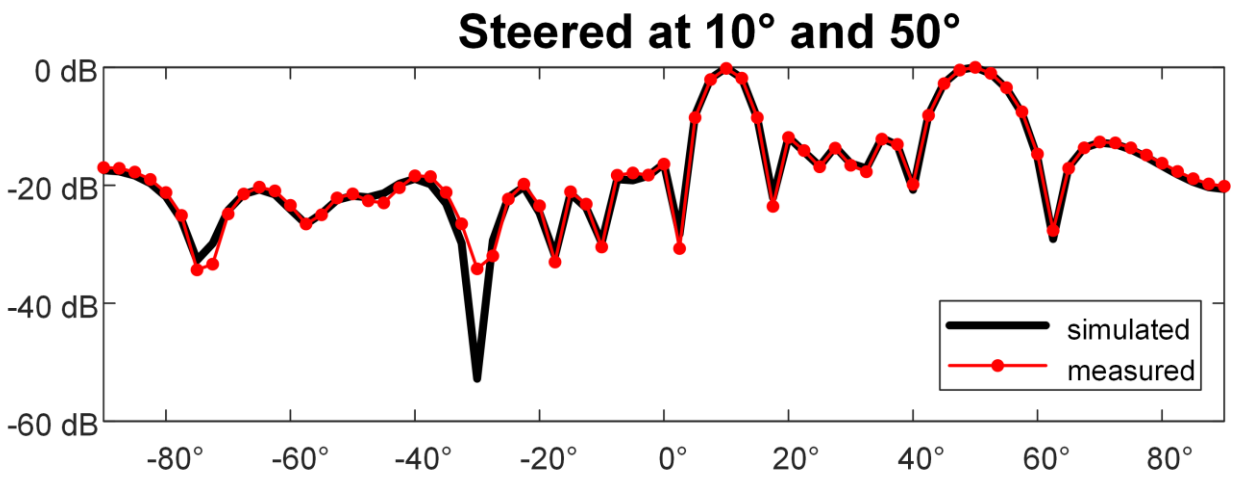

Figure 36. Beam patterns with two main lobes (input frequency: 1.006 GHz).

IL-BSP also enables enhanced beamforming with multiple main lobes. As shown in Figure 36, IL-BSP is programmed to produce a two-main-lobe beam pattern by averaging complex weights for two different single main lobe beam patterns as represented in (40) and (41).

$$\cos\theta_{1+2} = \frac{\cos\theta_1 + \cos\theta_2}{2} \tag{40}$$

$$\sin\theta_{1+2} = \frac{\sin\theta_1 + \sin\theta_2}{2} \tag{41}$$

Theoretically, ABF can also achieve these beam patterns, however, hardware errors including channel mismatch limit the performance in practice [4]. The prototype digital beamformer has measured beam patterns which are almost ideal for two incident angles 10°/50°.

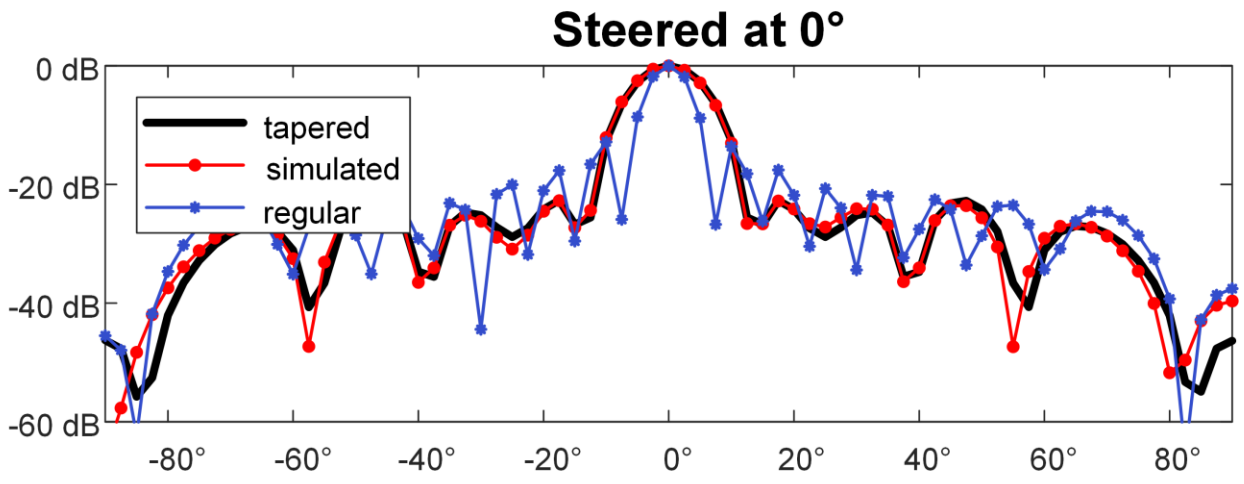

Figure 37. Measured tapered beam patterns (input frequency: 1.006 GHz).

Figure 37 depicts measured tapered beam patterns with suppressed side lobes. This adaptive beamforming is performed by applying a Chebyshev window to the complex weights. The measured beam pattern for 0° incident angle has side-lobes lower than -22.7 dB.

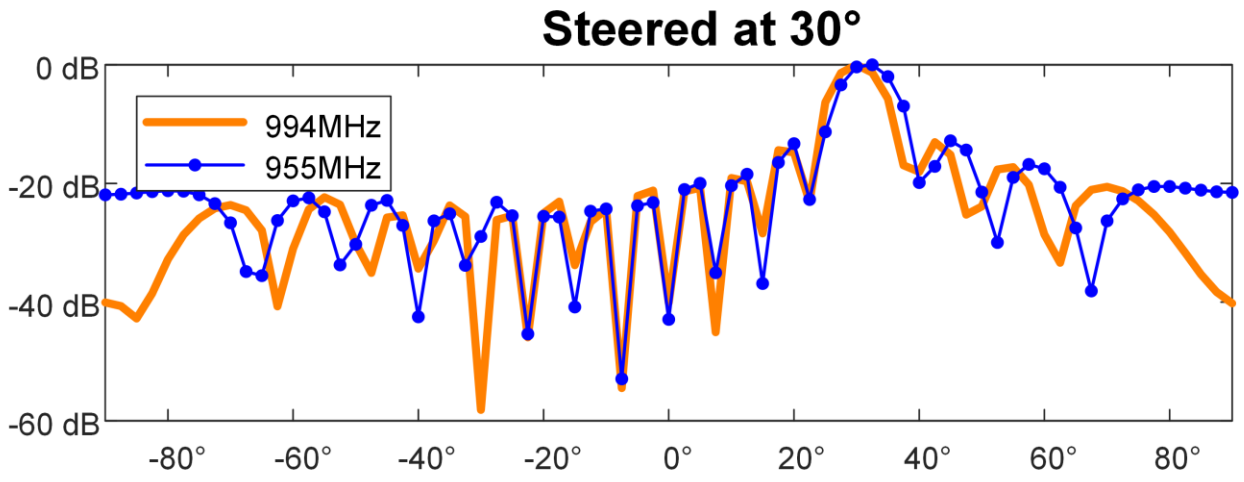

Figure 38. Measured beam patterns over +/- 50 MHz bandwidth (input frequency: 994 MHz and 955 MHz).

Figure 38 shows the variation of the beam patterns over the +/- 50 MHz input bandwidth to measure beam squinting (direction) error. The beam squinting error for a beamformer with ideal phase-shifters can be approximated as:

$$\Delta\Theta = -\frac{\tan\Theta_0}{f_0}\Delta f, \tag{42}$$

where $\Delta\Theta$ is the squinting error, Θ_0 is the main beam direction, f_0 is the center frequency, and Δf is the frequency offset of the input signals [33]. When a beamformer is steered at 30°, the theoretical beam squinting error for -45 MHz off-center frequency is 1.5°. The beam pattern in Figure 38 has a 2.5° squinting error, which is the closest number to the theoretical error for a measurement angle step size of 2.5°.

5.3. Performance Summary and Comparison

Table I. Prototype-I Phased Array Performance Summary and Comparsion

	THIS WORK	**J. Jeong JSSC 2016** [9]	**F. Angiolini DATE 2017** [43]	**H. Aliakbarian EuCAP 2010** [44]
Application	RF Communication	RF Communication	Ultrasound Imaging	Satellite
Integration	ADC + DDC + DBF	ADC + DDC + DBF	DBF	DBF
Center Frequency [GHz]	1.0	0.26	0.004	-
Bandwidth [MHz]	100	20	-	-
# of Elements	16	8	1024	2
# of Beams	4	2	1	1
Array SNR [dB]	59.6	-	-	-
Array SNDR [dB]	58.5	63.3	-	-
SNR improvement [dB]	11.2	-	-	-
SNDR improvement [dB]	10.5	8.9	-	-
Total Power [mW]	312	124	5000	500
DBF Power [mW]	68	19	5000	500
Active Area [mm^2]	0.22	0.28	-	-
Technology	40 nm	65 nm	FPGA	FPGA

Table I compares the digital beamformer prototype IC with the state-of-the-art. The digital beamformer in this work has twice as many beams and elements as [9], which is the most for a published digital beamformer. The prototype consumes 312 mW (16 CTBPDSMs: 244 mW, DBF:

68 mW), and has a 11.2 dB array gain, which is 2.3 dB higher than [8]. It occupies 0.24 mm^2 (16 CTBPDSMs: 0.18 mm^2, DBF: 0.06 mm^2) of active area, which is 21% smaller than [9].

Chapter 6 Prototype-II (Timed Array)

6.1. System Architecture

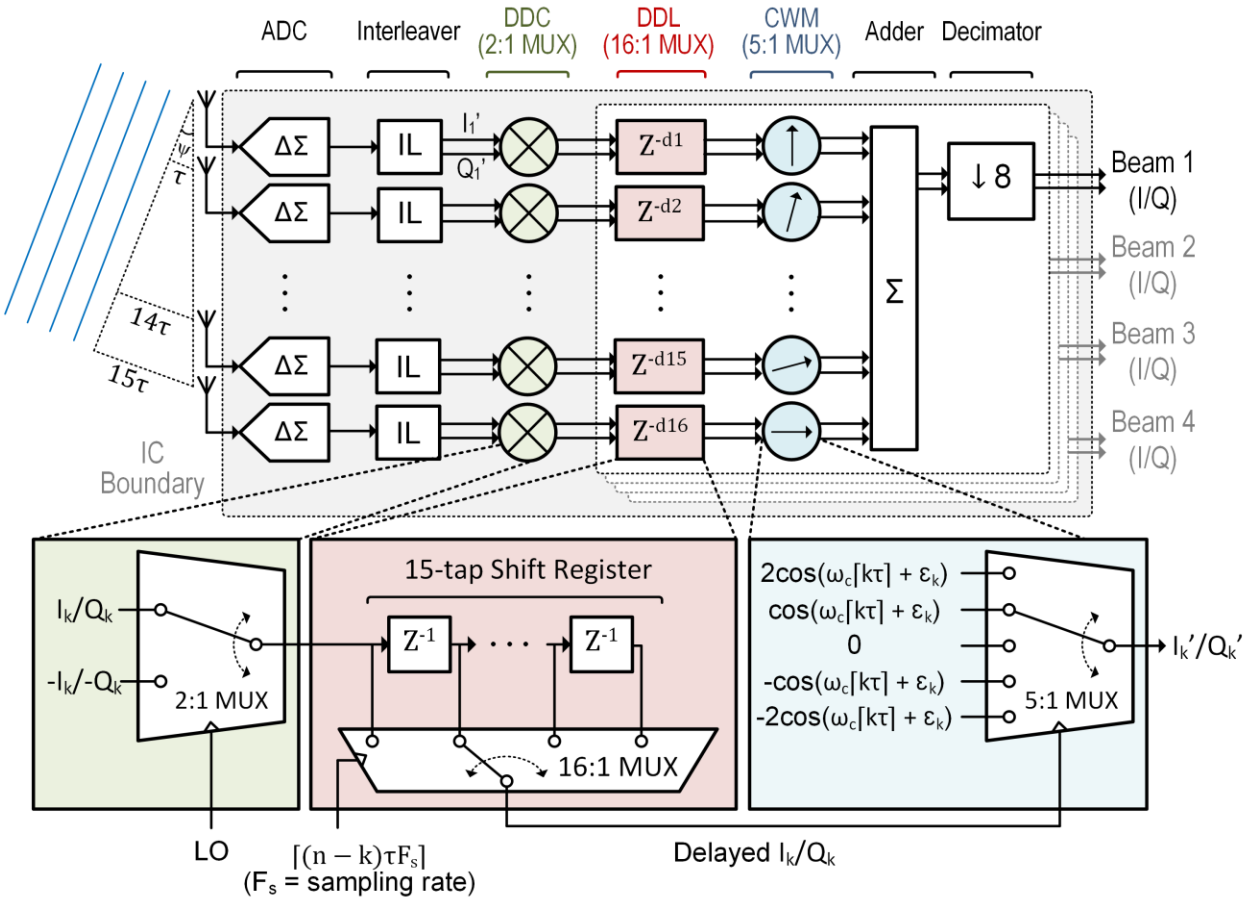

Figure 39. System architecture of the true-time-delay interleaved bit stream processing (IL-BSP) digital beamformer.

We build on the interleaved bit stream processing approach in [8] to efficiently implement this true-time-delay technique. [8] uses an array of continuous time band-pass delta-sigma modulators (CTBPDSMs) to directly digitize high-IF signals, and implements phase-shifting with bit stream processing (BSP). A disadvantage of the approach in [8] is that it is limited to

conventional phase-shift beamforming. In this work, we take advantage of the fast sample rate of the CTBPDSMs to facilitate high-resolution digital time delay.

As shown in Figure 39, 16 band-pass modulators generate 4 GS/s 5-level digital bit streams. Interleavers produce 2 GS/s quadrature I and Q signals. A digital down converter (DDC) down converts the digitized band-pass signal to baseband with a 2:1 MUX, using the 2-level (1 and -1) digital LO as the MUX select. The 16-level digital delay line (DDL) delays the signal with a 500 ps delay resolution from 0-7500 ps. Next, a 5:1 MUX, using the delayed quadrature signal as the MUX-select performs complex weight multiplication (CWM). Finally, the combined signals are decimated to 250 MS/s. Four copies of this processing produce four simultaneous independent beams.

6.2. Measurements

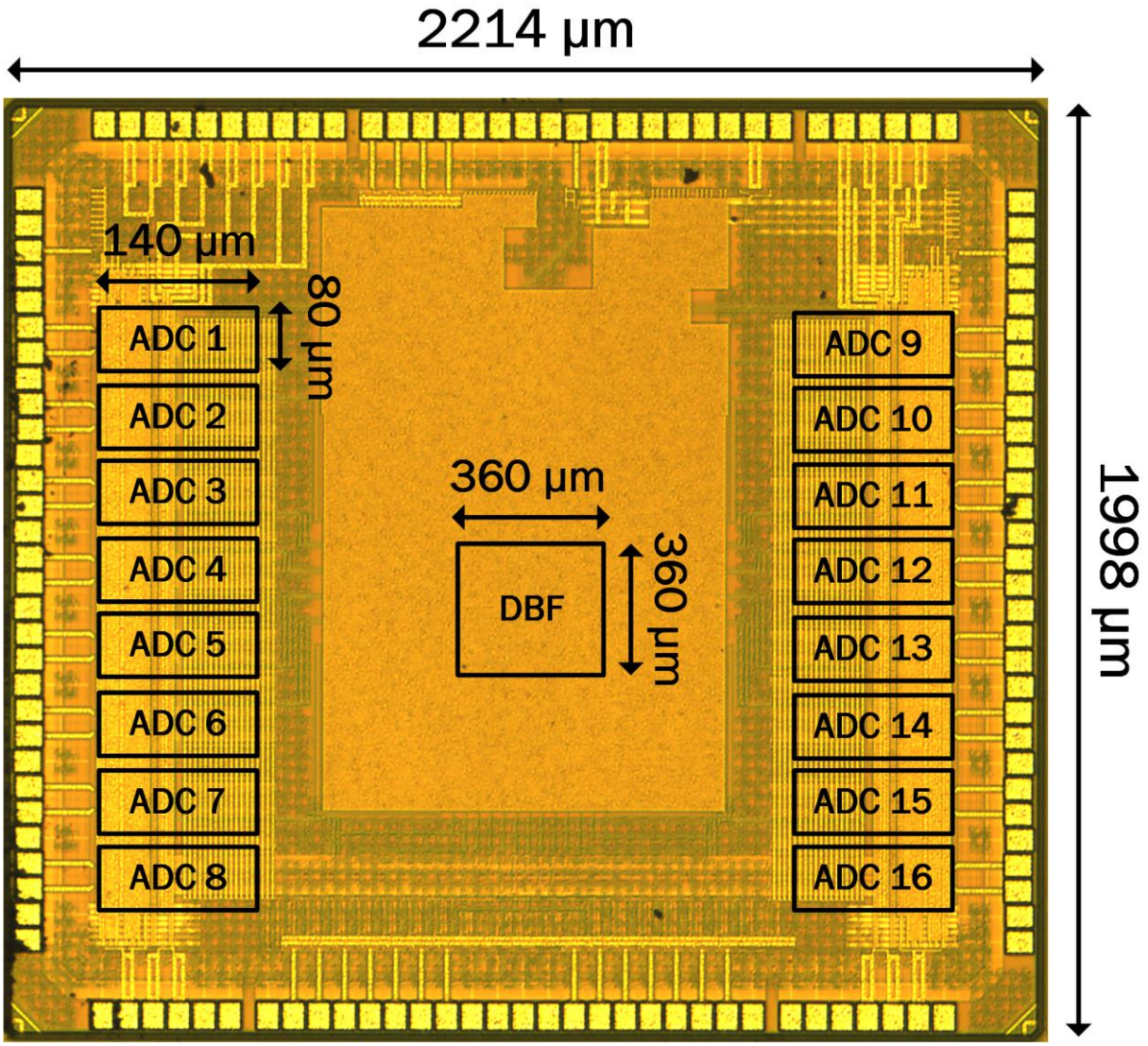

Figure 40. Die Micrograph (2.214 × 1.998 mm^2).

As shown in Figure 40, the prototype 16-element true-time-delay digital beamformer has 8 ADCs on each side of the chip and the true-time-delay digital beamformer block in the middle. The prototype is fabricated in 10-metal 40 nm CMOS and packaged in an 88-lead QFN package. The 16 modulators and the DBF circuitry occupy a core area of 0.29 mm^2.

6.2.1. Power Spectral Density Plot and Constellation Diagram

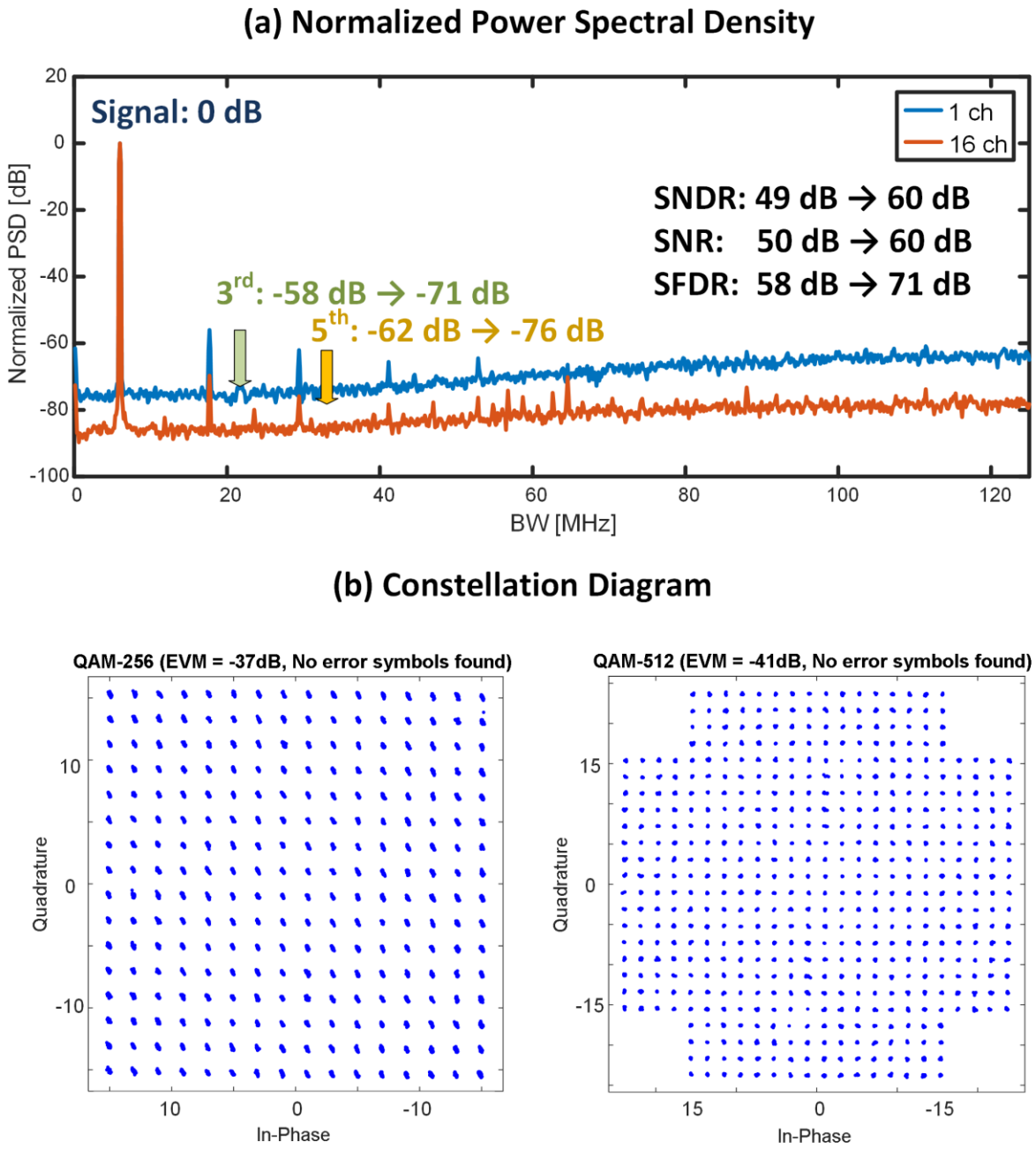

Figure 41. (a) Normalized measured power spectral density plot for a single channel and entire array and (b) measured QAM-256/512 constellation for 16-element array.

Figure 41(a) compares the power spectral density of a single element to that of the entire array. The measured SNR, SNDR and SFDR for the 16-element array are 60 dB, 60 dB and 71 dB, respectively. Array SNDR, SFDR improve by 11 dB, 14 dB, respectively, compared to a single

element. Connecting directly to an antenna without an RF frontend, the measured NF for a single element is 26 dB. The measured EVM is less than -37 dB and no bit errors are observed in 8000 symbols for 5 MBd QAM-256 and QAM-512 (Figure 41(b)).

6.2.2. Beam Pattern

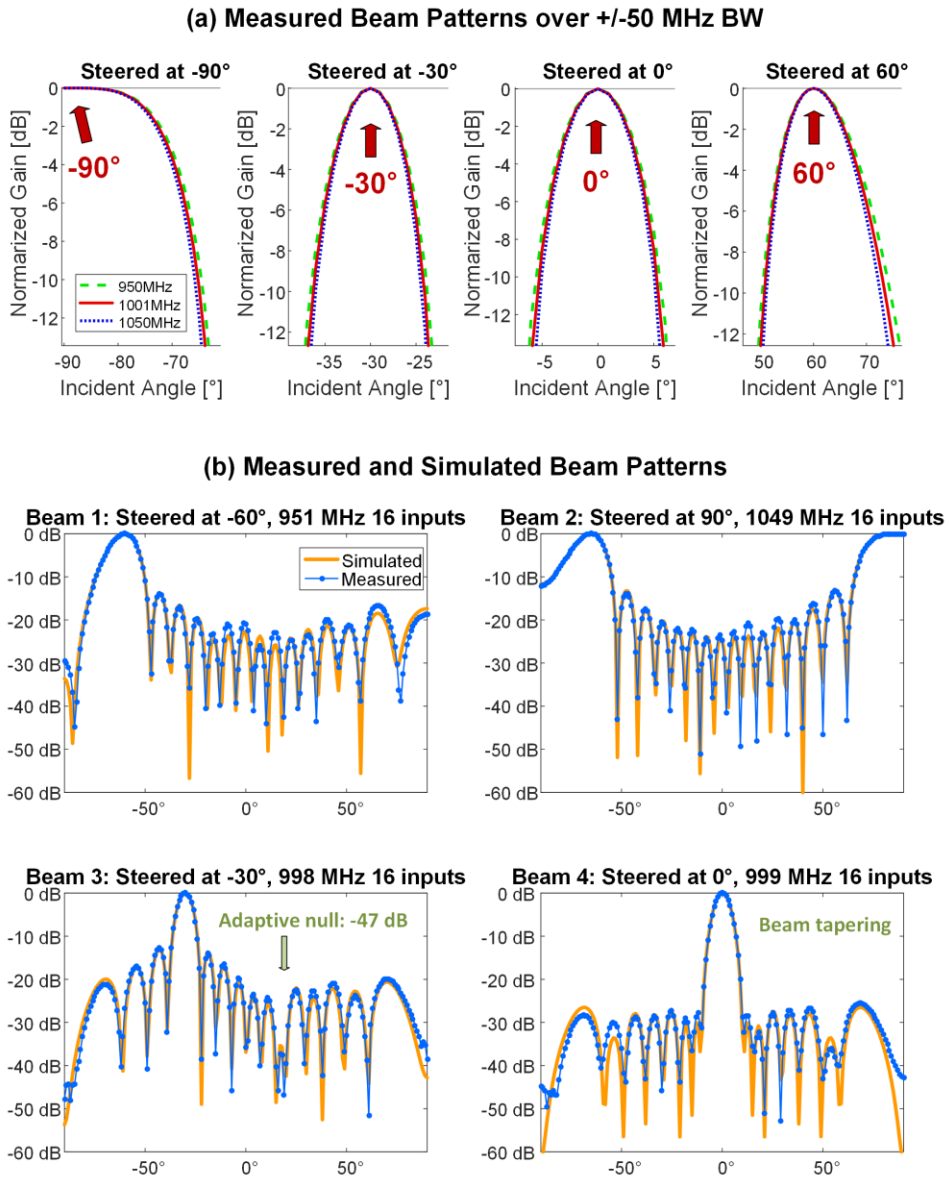

Figure 42. (a) Measured beam patterns over +/- 50 MHz have no beam squinting error and (b) measured beam patterns are near identical to the ideal ones.

Figure 42(a) shows the measured beam patterns for input signals over the +/- 50 MHz input bandwidth from 1 GHz. With a measurement step size of 1°, the true-time-delay digital beamforming shows negligible squinting error. Furthermore, the measured 4-simultaneous beam patterns are almost identical to the simulated beam patterns (Figure 42(b)). In these tests, beam 1 and 2 are programmed to steer the beam direction to -60° and 90°, respectively. The beam 3 and 4 demonstrate null steering and tapering. In contrast to RF/analog time delay arrays which require additional variable gain amplifiers for adaptive beamforming, the high-resolution CWM with 10-bit coefficients facilitates adaptive null steering and tapering without additional circuitry. Beam 3 is programmed to have a main beam at -30° and a null at 20° while beam 4 has tapered coefficients to suppress sidelobes to less than -25 dB.

6.2.3. Interference Test[5]

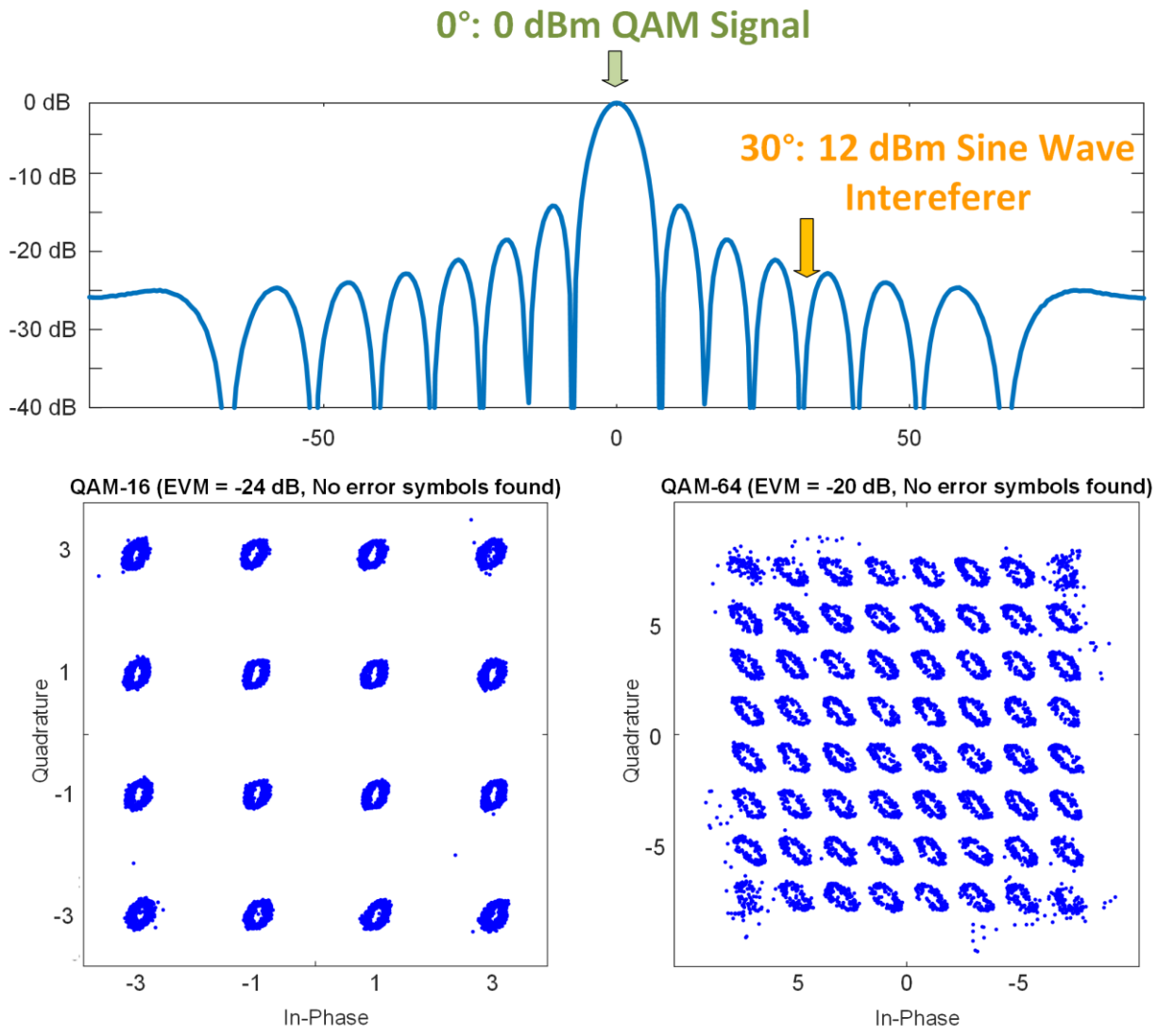

Figure 43. Measured QAM constellations for 16-element array transmitted at 5 MBd with a large interference at 30°.

Figure 43 shows measured QAM-16 and QAM-64 constellation diagrams in the presence of an in-band large interferer at a null. The power of the desired signal is 0 dBm and the interference is 12 dBm. Although the power of the interference is 12 dB higher than the desired

[5] The QAM interference test was in collaboration with Rundao Lu.

QAM signal, measured EVM is better than -20 dB for QAM-64 (-24 dB for QAM-16) and no error symbols are found in 8000 symbols.

6.3. Performance Summary and Comparison

Table II. Prototype-II Timed Array Performance Summary and Comparsion

	This Work	[8]	[9]
# of Elements	16	16	8
# of Beams	4	4	2
Delay Implementation	True-time-delay	Phase-shifting	Phase-shifting
Bandwidth [MHz]	100	100	20
Array SNDR [dB]	60	59	63
Time Delay Range [ps]	0 - 7500	-	-
ADC Power [mW]	16	15	13
DBF Power [mW]	196	68	19
Total Power [mW]	453	312	124
Active Area [mm^2]	0.29	0.22	0.28
Phase-shifter Resolution [bit]	10	6	10
Technology	40 nm CMOS	40 nm CMOS	65 nm CMOS

Table II summarizes the performance of the first digital true-time-delay beamformer IC and compares it with state-of-the-art DBF ICs. The digital beamforming receiver supports 16 elements and generates four independent simultaneous beams with 100 MHz bandwidth and consumes 28 mW per element.

Chapter 7 Future Work

In this thesis we present a digital phased array and a digital timed array both with 16 elements, large bandwidth (100 MHz), and a 1 GHz center frequency. Although our work significantly contributes to the field of digital beamforming, there is still some skepticism and some doubts on the practicality of digital beamforming. The following suggestions can be considered to implement and further improve the performance and flexibility of digital beamforming:

- A wider bandwidth (i.e. 800 MHz) is desirable to fulfil 5G requirements.
- To prove its feasibility as a 5G receiver, requires the implementation of an mm-wave front-end, including an LNA and mixer.
- A full duplex transceiver design including an on-chip circulator, PA, and PLL to prove the possibility of a complete system-level-integrated digital-beamforming SoC.
- In practice, beamforming receivers need to scan for the desired transmitter. Implementation of the direction of arrival algorithms (DOA) such as Periodogram, MUSIC, SAMV can be considered.
- An automated gain and phase calibration algorithm is required for a practical application.
- Multi-chip digital beamforming is a fascinating research area. Potential challenges include local oscillator (LO) signal distribution and phase offset calibration.
- One of the biggest challenges of digital beamforming is the lack of spatial interference rejection in RF domain. A solution for this issue would be a game changer.

Chapter 8 Conclusion

Key contributions of the prototype-I phased array include power and area reduction through interleaved bit stream processing, design and verification of the largest integrated digital phased array, and the design of a power- and area-efficient 100 MHz-bandwidth band-pass ADC. The prototype-II timed array contributes to digital beamforming by implementing the first integrated true-time-delay digital beamformer, and improving ADC linearity through a newly introduced constant-output-impedance current-steering feedback DAC.

This work addresses the challenges of power, area, squinting, and distortion. We expand the complexity and performance of digital beamforming with interleaved bit stream processing, true-time-delay technique, and efficient band-pass delta-sigma ADCs. The prototype-I beamformer, a digital phased array with a 1 GHz center frequency, a 100 MHz bandwidth, and 16 elements, generates 4 simultaneous beams for MIMO. IL-BSP consumes 80% less power and occupies 80% less area compared to a conventional DSP implementation. The CTBPDSMs in this work have 5 times higher bandwidth, 4 times higher center frequency, yet require 1/3 area and 43% less energy per conversion than the ADCs presented in previous work. The prototype-I beamformer achieves a 11.2 dB array gain in SNR and consumes only 20mW/element. The prototype-II beamformer, true-time-delay digital array, also has a 1 GHz center frequency, a 100 MHz bandwidth, and supports 16 elements, and 4 simultaneous beams. The prototype IC achieves 11 dB SNDR improvement and consumes only 28 mW/element. A new feedback DAC technique reduces distortion in the ADCs so that a large array can better benefit from the array SNR gain. Thanks to digital beamforming and accurate analog to digital conversion, the measured beam

patterns, including single main lobe beam, two main lobes beam, tapered beam, and adaptive nulling beam are nearly ideal, which is challenging for analog/RF beamformers. The prototype-II timed array including the 16 CTPBDMs occupies only 0.29 mm^2 and consumes 453 mW.

Bibliography

[1] M. Shafi and et al., "5G: A tutorial overview of standards, trials, challenges, deployment, and practice," *IEEE Journal on Selected Areas in Communications,* vol. 35, no. 6, pp. 1201-1221, 2017.

[2] F. W. Vook, A. Ghosh and T. A. Thomas, "MIMO and beamforming solutions for 5G technology," in *2014 IEEE MTT-S International Microwave Symposium*, Tampa, 2014.

[3] O. E. Ayach, S. Rajagopal, S. Abu-Surra, Z. Pi and R. W. Heath, "Spatially sparse precoding in millimeter wave MIMO systems," *IEEE Transactions on Wireless Communications*, vol. 13, no. 3, pp. 1499-1513, 2014.

[4] S. H. Talisa, K. W. O'Haver, T. M. Comberiate, M. D. Sharp and O. F. Somerlock, "Benefits of Digital Phased Array Radars," *Proceedings of the IEEE,* vol. 104, no. 3, pp. 530-543, 2016.

[5] A. Lozano and N. Jindal, "Transmit diversity vs. spatial multiplexing in modern MIMO systems," *IEEE Transactions on Wireless Communications,* vol. 9, no. 1, pp. 186-197, 2010.

[6] R. W. Heath and A. J. Paulraj, "Switching between diversity and multiplexing in MIMO systems," *IEEE Transactions on Communications,* vol. 53, no. 6, pp. 962-968, 2005.

[7] P. K. Bailleul, "A new era in elemental digital beamforming for spaceborne communications phased arrays," *Proceedings of the IEEE,* vol. 104, no. 3, pp. 623-632, 2016.

[8] S. Jang, J. Jeong, R. Lu and M. P. Flynn, "A 16-element 4-beam 1GHz-IF 100MHz-bandwidth Interleaved Bit-Stream digital beamformer in 40nm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 53, no. 5, pp. 1302-1312, 2018.

[9] J. Jeong, N. Collins and M. P. Flynn, "A 260 MHz IF sampling bit-stream processing digital beamformer with an integrated array of continuous-time band-pass ΔΣ modulators," *IEEE Journal of Solid-State Circuits,* vol. 51, no. 5, pp. 1168 - 1176, 2016.

[10] R. Rotman, M. Tur and L. Yaron, "True time delay in phased arrays," *Proceedings of the IEEE,* vol. 104, no. 3, pp. 504-518, 2016.

[11] J. D. Roderick, H. Krishnaswamy, K. Newton and H. Hashemi, "A 4-bit ultra-wideband beamformer with 4ps true time delay resolution," in *Proceedings of the IEEE 2005 Custom Integrated Circuits Conference*, San Jose, 2005.

[12] H. Chae, J. Jeong, G. Manganaro and M. P. Flynn, "A 12 mW low power continuous-time bandpass ΔΣ modulator with 58 dB SNDR and 24 MHz bandwidth at 200 MHz IF," *IEEE Journal of Solid-State Circuits,* vol. 49, no. 2, pp. 405-415, 2014.

[13] R. Schreier and G. C. Temes, "Implementation considerations for ADCs," in *Understanding delta-sigma data converters*, Wiley-IEEE press, 2005, pp. 205-218.

[14] O. Shoaei and W. M. Snelgrove, "A multi-feedback design for LC band-pass delta-sigma modulators," in *1995 IEEE International Symposium on Circuits and Systems*, Seattle, 1995.

[15] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 48, no. 9, pp. 1041-1056, 2001.

[16] H. Chae and M. P. Flynn, "A 69 dB SNDR, 25 MHz BW, 800MS/s continuous-time band-pass delta sigma modulator using a duty-cycle-controlled DAC for low power and reconfigurability," *IEEE Journal fo Solid-State Circuits,* vol. 51, no. 3, pp. 649-659, March 2016.

[17] J. Harrison and et al., "An LC band-pass ΔΣ ADC with 70dB SNDR over 20MHz bandwidth using CMOS DACs," in *2012 IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2012.

[18] J. Ryckaert and et al., "A 6.1 GS/s 52.8 mW 43 dB DR 80 MHz bandwidth 2.4 GHz RF band-pass ΔΣ ADC in 40 nm CMOS," in *2010 IEEE Radio Frequency Integrated Circuits Symposium*, Anaheim, CA, 2010.

[19] N. Beilleau and et al., "A 1.3V 26mW 3.2GS/s undersampled LC band-pass ΣΔ ADC for a SDR ISM-band receiver in 130nm CMOS," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, Boston, MA, 2009.

[20] E. Martens and et al., "RF-to-Baseband digitization in 40 nm CMOS with RF band-pass ΔΣ modulator and polyphase decimation filter," *IEEE Journal of Solid-State Circuits,* vol. 47, no. 4, pp. 990-1002, April 2012.

[21] J. Ryckaert, "A 2.4 GHz low-power sixth-order RF band-pass converter in CMOS," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 11, pp. 2873-2880, Nov. 2009.

[22] J. Zhang and et al., "A 54.4-mW 4th-order quadrature band-pass CT ΣΔ modulator with 33-MHz BW and 10-bit ENOB for a GNSS receiver," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Phoenix, AZ, 2015.

[23] C. Y. Ho and et al., "A quadrature band-pass continuous-time delta-sigma modulator for a tri-mode GSM-EDGE/UMTS/DVB-T receiver," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 11, pp. 2571-2582, 2011.

[24] C. Y. Ly, "A sixth-order 200 MHz IF band-pass sigma-delta modulator with over 68 dB SNDR in 10 MHz bandwidth," *IEEE Journal of Solid-State Circuits,* vol. 45, no. 6, pp. 1122-1136, June 2010.

[25] S. B. Kim, "A 2.7 mW, 90.3 dB DR continuous-time quadrature band-pass sigma-delta modulator for GSM/EDGE low-IF Receiver in 0.25 μm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 3, pp. 891-900, 2009.

[26] Y. Xu, "A 5-/20-MHz BW reconfigurable quadrature band-pass CT delta sigma ADC with antipole-splitting opamp and digital I / Q calibration," *IEEE Transactions on Very Large Scale Integration (VLSI),* vol. 24, no. 1, pp. 243-255, Jan. 2016.

[27] P. M. Chopp and A. A. Hamoui, "A 1-V 13-mW single-path frequency-translating delta sigma modulator with 55-dB SNDR and 4-MHz bandwidth at 225 MHz," *IEEE Journal of Solid-State Circuits,* vol. 48, no. 2, pp. 473-486, Feb. 2013.

[28] H. Shibata and et al., "A DC-to-1 GHz tunable RF delta sigma ADC achieving DR = 74 dB and BW = 150 MHz at f0 = 450 MHz using 550 mW," *IEEE Journal of Solid-State Circuits,* vol. 47, no. 12, pp. 2888-2897, Dec. 2012.

[29] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications,* vol. 17, no. 4, pp. 539-550, 1999.

[30] K. Khalaf and et al., "A 60-GHz 8-way phased-array front-end with T/R switching and calibration-free beamsteering in 28-nm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 53, no. 7, pp. 2001-2011, July 2018.

[31] B. Sadhu and et al., "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 12, pp. 3373-3391, Dec 2017.

[32] H. Hashemi, T. Chu and J. Roderick, "Integrated true-time-delay-based ultra-wideband array processing," *IEEE Communications Magazine,* vol. vol. 46, no. no. 9, pp. pp. 162-172, September 2008.

[33] S. K. Garakoui, E. A. Klumperink, B. Nauta and F. E. V. Vilet, "Phased-array antenna beam squinting related to frequency dependency of delay circuits," in *2011 European Radar Conference (EuRAD)*, Manchester, 2011.

[34] I. Mondal and N. Krishnapura, "A 2-GHz bandwidth, 0.25–1.7 ns true-time-delay element using a variable-order all-pass filter architecture in 0.13 µm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 8, pp. 2180-2193, Aug. 2017.

[35] S. K. Garakoui, E. A. M. Klumperink, B. Nauta and F. E. v. Vliet, "Compact cascadable gm-C all-pass true time delay cell with reduced delay variation over frequency," *IEEE Journal of Solid-State Circuits,* vol. 50, no. 3, pp. 693-703, March 2015.

[36] T. Chu and H. Hashemi, "A true time-delay-based bandpass multi-beam array at mm-waves supporting instantaneously wide bandwidths," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, 2010.

[37] M. Q, D. Leenaerts and R. Madhmoudi, "A 12ps true-time-delay phase shifter with 6.6% delay variation at 20–40GHz," in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Seattle, WA, 2013.

[38] S. H. Talisa, K. W. O'Haver, T. M. Comberiate, M. D. Sharp and O. F. Somerlock, "Benefits of digital phased array radars," *Proceedings of the IEEE*, vol. 104, no. 3, pp. 530-543, 2016.

[39] D. C. M. Horvat, "True time-delay bandpass beamforming," *IEEE Journal of Oceanic Engineering*, vol. 17, no. 2, pp. 185-192, 1992.

[40] P.W. Wong and R. M. Gray, "FIR filters with sigma-delta modulation encoding," *IEEE Transactions on Acoustics, Speech and Signal Processing*, vol. 38, no. 6, pp. 970-990, Jun. 1990.

[41] I. Levi and et al., "High speed dual mode logic carry look ahead adder," in *IEEE International Symposium on Circuits and Systems*, Seoul, 2012.

[42] R. Schreier and G. C. Temes, "Band-pass and quadrature delta sigma modulation," in *Understanding delta-sigma data converters*, Wiley-IEEE Press, 2005, pp. 141-142.

[43] F. Angiolini and et al., "1024-Channel 3D ultrasound digital beamformer in a single 5W FPGA," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Lausanne, 2017.

[44] H. Aliakbarian and et al., "Analogue versus digital for baseband beam steerable array used for LEO satellite applications," in *2010 Proceedings of the Fourth European Conference on Antennas and Propagation (EuCAP)*, Barcelona, 2010.