Design of Digital FMCW Chirp Synthesizer PLLs

Using Continuous-Time Delta-Sigma Time-to-Digital Converters

by

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ABSTRACT

Radar applications for driver assistance systems and autonomous vehicles have spurred the development of frequency-modulated continuous-wave (FMCW) radar. Continuous signal transmission and high operation frequencies in the K- and W-bands enable radar systems with low power consumption and small form factors. The radar performance depends on high-quality signal sources for chirp generation to ensure accurate and reliable target detection, requiring chirp synthesizers that offer fast frequency settling and low phase noise. Fractional-N phase locked loops (PLLs) are an effective tool for synthesis of FMCW waveform profiles, and advances in CMOS technology have enabled high-performance single-chip CMOS synthesizers for FMCW radar.

Design approaches for FMCW chirp synthesizer PLLs need to address the conflicting requirements of fast settling and low close-in phase noise. While integrated PLLs can be implemented as analog or digital PLLs, analog PLLs still dominate for high frequencies. Digital PLLs offer greater programmability and area efficiency than their analog counterparts, but rely on high-resolution time-to-digital converters (TDCs) for low close-in phase noise. Performance limitations of conventional TDCs remain a roadblock for achieving low phase noise with high-frequency digital PLLs. This shortcoming of digital PLLs becomes even more pronounced with wide loop bandwidths as required for FMCW radar. To address this problem, this work presents digital FMCW chirp synthesizer PLLs using continuous-time delta-sigma TDCs.

After a discussion of the requirements for PLL-based FMCW chirp synthesizers, this dissertation focuses on digital fractional-N PLL designs based on noise-shaping TDCs that leverage state-of-the-art delta-sigma modulator techniques to achieve low close-in phase noise in

wide-bandwidth digital PLLs. First, an analysis of the PLL bandwidth and chirp linearity studies the design requirements for chirp synthesizer PLLs. Based on a model of a complete radar system, the analysis examines the impact of the PLL bandwidth on the radar performance. The modeling approach allows for a straightforward study of the radar accuracy and reliability as functions of the chirp parameters and the PLL configuration.

Next, an 18-to-22GHz chirp synthesizer PLL that produces a 25-segment chirp for a 240GHz FMCW radar application is described. This synthesizer design adapts an existing third-order noise-shaping TDC design. A 65nm CMOS prototype achieves a measured close-in phase noise of -88dBc/Hz at 100kHz offset for wide PLL bandwidths and consumes 39.6mW. The prototype drives a radar testbed to demonstrate the effectiveness of the synthesizer design in a complete radar system.

Finally, a second-order noise-shaping TDC based on a fourth-order bandpass delta-sigma modulator is introduced. This bandpass delta-sigma TDC leverages the high resolution of a bandpass delta-sigma modulator by sampling a sinusoidal PLL reference and applies digital down-conversion to achieve low TDC noise in the frequency band of interest. Based on the bandpass delta-sigma TDC, a 38GHz digital FMCW chirp synthesizer PLL is designed. The feedback divider applies phase interpolation with a phase rotation scheme to ensure the effectiveness of the low TDC noise. A prototype PLL, fabricated in 40nm CMOS, achieves a measured close-in phase noise of -85dBc/Hz at 100kHz offset for wide loop bandwidths >1MHz and consumes 68mW. It effectively generates fast (500MHz/55μs) and precise (824kHz rms frequency error) triangular chirps for FMCW radar. The bandpass delta-sigma TDC achieves a measured integrated rms noise of 325fs in a 1MHz bandwidth.

CHAPTER 1 Introduction

Although radar was originally developed for the military during World War II, modern radar technology finds widespread use in numerous civil applications ranging from traffic security and vehicular navigation to surveillance systems and weather forecasting. Over the past decade, automotive radar applications for driver assistance systems and autonomous vehicles have been driving demand for high-performance radar-sensor technology [1]. Due to their robustness against environmental conditions such as light and weather, radar sensors can complement other sensor technologies to accurately capture the environment of the vehicle or can even be the sensory system of choice when it comes to triggering a real-time response to certain traffic scenarios. Mid-range and long-range automotive radar typically rely on frequency-modulated continuous-wave (FMCW) radar while operating at tens of GHz, enabling power-efficient radar systems with small form factors. High-frequency FMCW radar can therefore meet the increasing demand for low-cost, compact and light-weight radar solutions and motivates research on fully-integrated FMCW waveform synthesizers [2]–[8] and single-chip FMCW radar transceivers [9]–[11].

1.1 FMCW Radar

The term RADAR is an acronym for “Radio Detection And Ranging” and refers to technology and electronic equipment that uses radio waves to detect objects [12], [13]. The transmitter of a radar system generates electromagnetic signals, which are emitted by a transmit antenna. The signal waves travel through space, are reflected at an object, and a small portion of

the reflected energy returns to the radar and is picked up by a receive antenna. From the properties of the received signal such as frequency, time delay and signal power, the radar can then provide information about the detected object, e.g. distance, height, speed and direction.

Depending on the used radar technology, radar systems can be classified as pulse radars or continuous-wave (CW) radars. A pulse radar periodically transmits short pulses with high pulse power and turns off between the transmission pulses while it receives the echo signals. The pulse repetition frequency and the duty cycles of the radar pulses are important performance parameters of such a radar system. Since the echo signal must be received before the transmission of the next radar pulse to unambiguously determine the range of the target, the pulse repetition frequency sets a limit to the so-called maximum unambiguous range. Moreover, a pulse radar relies on a short pulse duration, i.e. a small duty cycle, to achieve a short minimal detection range and a small range resolution.

In contrast to a pulse radar, a CW radar continuously transmits and receives radar signals, offering lower power consumption. By monitoring the frequency difference between the transmit and receive signals caused by the Doppler effect, the velocity of a target can be determined. Due to the continuous radar operation, potential leakage of the transmitted signal power into the receiver is a challenge with CW radar. Classic run-time measurements as with pulse radars, i.e. measurements of the elapsed time as the signal pulses travel to an object and back to the radar, are not possible with CW radars. Therefore, the range of a detected object cannot be determined.

Frequency-modulated continuous-wave (FMCW) radar is a special type of CW radar where the operating frequency of the continuously transmitted radar signal is modulated during the measurement. This modification introduces a time reference for range measurement and FMCW radar can thus determine both the range and velocity of the detected object. The frequency of an

FMCW radar signal is generally linearly modulated and the linear ramps of the waveform profile are referred to as chirps. A very common FMCW waveform profile is a triangular profile featuring up-chirps and down-chirps, as shown in Figure 1.1.

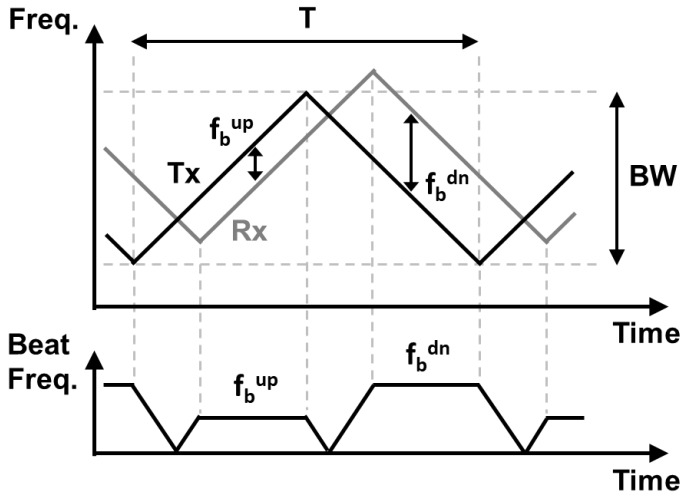


Figure 1.1. FMCW radar waveforms for a triangular waveform profile

Due to the signal roundtrip to the target and back to the radar, there is a propagation delay between the transmitted signal (Tx) and the received signal (Rx). The resulting offset frequency between the two signals is called beat frequency and is a measure of the range of the detected object. In addition, if the object is moving relative to the radar, the frequency of the received waveform profile exhibits a Doppler shift, resulting in different beat frequencies for the up- and down-chirps. Producing two distinct beat frequencies, an FMCW radar using a triangular waveform profile allows a simultaneous and unambiguous determination of both the range and velocity of the object. Range and velocity can be calculated as

$$R = \frac{c\,T}{4\,BW} \cdot \frac{f_b^{up} + f_b^{dn}}{2} \tag{1.1}$$

$$v = \frac{c}{2\,f_c} \cdot \frac{f_b^{up} - f_b^{dn}}{2} \tag{1.2}$$

where BW denotes the modulation bandwidth, T is the waveform period, f_b^{up} and f_b^{dn} are the beat frequencies for up- and down-chirps, respectively, f_c is the center frequency of the waveform and c is the speed of light [10].

High resolution in the range and velocity measurements is critical to the radar performance. Assuming perfectly linear chirps, range resolution and velocity resolution are defined as [10]

$$\Delta R = \frac{c}{2\,BW} \tag{1.3}$$

$$\Delta v = \frac{c}{2\,f_c\,T} \tag{1.4}$$

Accordingly, a fine range resolution requires a large modulation bandwidth while a longer waveform period improves the velocity resolution.

A block diagram of a complete FMCW radar is shown in Figure 1.2. The chirp synthesizer generates the desired FMCW waveform profile and a power amplifier feeds the synthesizer output to a transmit antenna. The received signal is mixed with the synthesizer output to obtain the beat frequency. An analog-to-digital converter (ADC) digitizes the resulting baseband signal. A DSP unit performs an FFT on the digitized baseband signal to determine the beat frequency and calculate distance and velocity of the detected object.

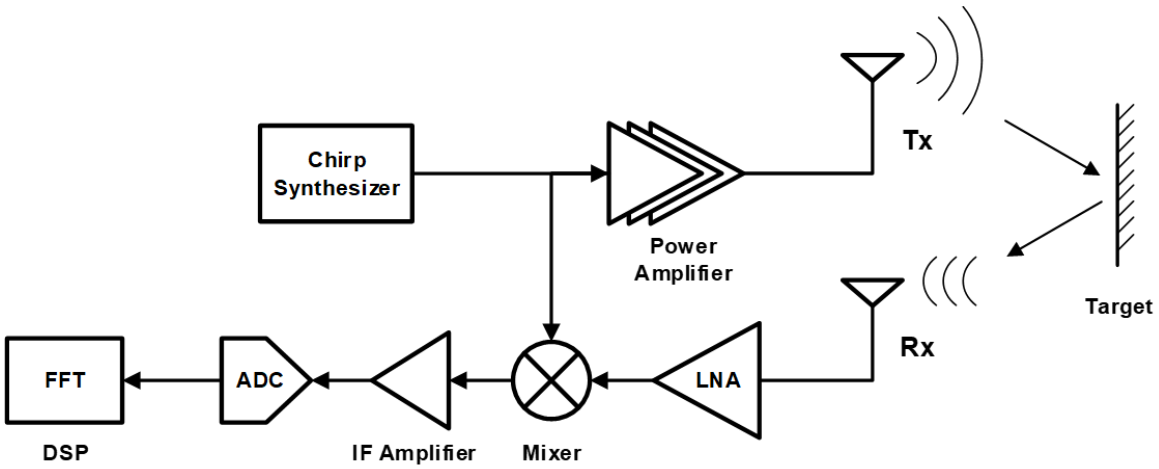


Figure 1.2. Block schematic of an FMCW radar system

Phase locked loops (PLLs) can be used to effectively generate linear chirps and PLL-based chirp synthesis has been widely adopted to implement fully-integrated FMCW chirp generation [2]–[11]. The performance and capabilities of the PLL play a crucial role for the overall performance of the FMCW radar, translating to challenging and partly conflicting requirements for the design of the PLL. The research presented in this dissertation focuses on design approaches for digital fractional-N PLLs that address these challenges.

1.2 PLL Design for FMCW Chirp Synthesis

The principle of FMCW radar assumes perfectly linear chirps to determine range and velocity of detected targets. A high-accuracy FMCW radar requires the chirp synthesizer to produce chirps with high linearity so that the beat frequencies are an accurate representation of the target parameters [14]. Linear chirps can effectively be generated with a fractional-N PLL by digitally modulating the division ratio of the feedback divider, as illustrated in Figure 1.3. This common approach to modulating the PLL output frequency is also known as one-point modulation as the modulation signal is injected at only one point of the feedback loop. The modulation signal controls the effective PLL division ratio according to the parameters of the chirp profile to be generated. To obtain highly linear chirps, the PLL must be able to follow the modulation signal and thus exhibit fast settling behavior. Fast settling of the PLL output frequency translates to a wide loop bandwidth of the PLL, making it an essential characteristic of a chirp synthesizer PLL.

Beside high accuracy, reliable target detection is another important aspect of the radar performance. An FMCW radar uses the transmit signal generated by the synthesizer PLL to down-convert the receive signal. For slow to moderate-speed chirps, the resulting baseband signal falls into the close-in phase noise region of the PLL (Figure 1.4). To reliably detect a target, a certain

signal-to-noise ratio must be given at the mixer output, i.e. the signal power of the beat frequency associated with the target must rise above the phase noise level by a certain amount. Low close-in phase noise is therefore imperative to ensure high detection sensitivity of the radar. Furthermore, detection reliability can be improved by generating fast chirps because this results in higher beat frequencies for the same radar scenario and potentially pushes them out of the 1/f noise and up towards lower phase noise (Figure 1.4), increasing the baseband signal-to-noise ratio as well. Faster chirps, however, require fast PLL settling and thus again a wide loop bandwidth.

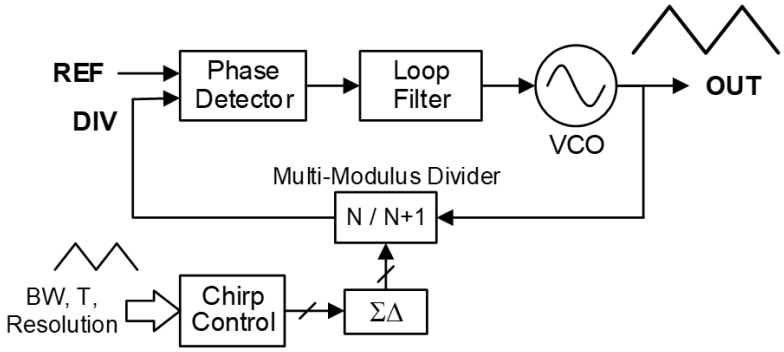


Figure 1.3. Chirp generation based on feedback modulation in a fractional-N PLL

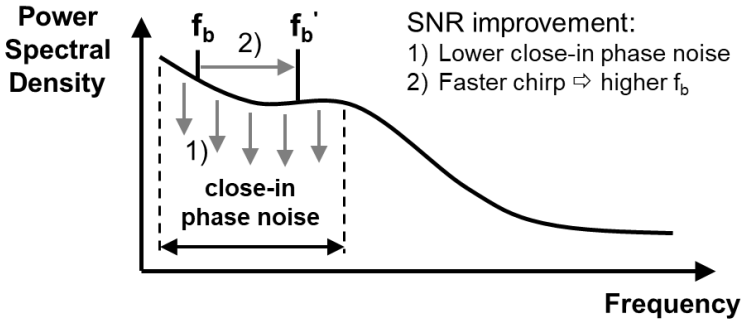


Figure 1.4. Effect of lower close-in phase noise and faster chirps on detection reliability

Unfortunately, achieving low close-in phase noise with wide PLL bandwidths presents a fundamental design trade-off with conventional PLLs – a wide loop bandwidth allows more noise from the phase detector to contribute to the output phase noise of the PLL and comes at the penalty

of increased close-in phase noise. This design conflict becomes even more challenging with digital PLLs as these rely on high-resolution time-to-digital converters (TDCs) for low close-in phase noise. Conventional PLL designs that offer low phase noise are typically restricted to slow settling [15]. PLL techniques that attempt to break the trade-off between phase noise and settling speed such as two-point modulation have been demonstrated [3], [6], [7], but come at the cost of other undesirable effects such as loop gain mismatch and require calibration.

While high-frequency synthesizers can basically be implemented as analog or digital PLLs, analog implementations still dominate for high frequencies [5], [10], [11], [15], [16]. Digital PLLs promise several advantages such as greater programmability and flexibility, area efficiency as well as easier portability between technology nodes. However, digital PLLs suffer from performance limitations of conventional TDCs, poor time resolution and linearity in particular, and from shortcomings of digitally-controlled oscillators (DCOs) such as their tuning resolution [17]. Low TDC time-resolution severely limits the close-in phase noise performance of a digital PLL. This bottleneck becomes even more pronounced with a wide PLL bandwidth as required for FMCW radar because more TDC noise contributes to the PLL output phase noise. This dissertation presents approaches to TDC design that enable low close-in phase noise with wide loop bandwidths in high-frequency digital PLLs.

1.3 Research Contributions

Radar applications in the mm-wave range such as automotive radar require high-quality frequency synthesizers offering low phase noise and fast settling. Digital PLLs are appealing for these applications as they promise greater flexibility and area efficiency. However, performance limitations of conventional TDCs remain a major roadblock for the adoption of high-frequency

digital PLLs. To address this issue, this research introduces a novel approach to time-to-digital conversion that leverages the properties of a continuous-time ΔΣ modulator.

As a starting point of this work, an analysis based on a model of a complete FMCW radar with a PLL-based chirp synthesizer examines the impact of the PLL bandwidth and chirp linearity on the overall radar performance. The upper and lower bounds of the PLL bandwidth are quantified for a given application scenario. This analysis provides design guidance by studying the accuracy and reliability of the radar as functions of the chirp parameters and the PLL configuration.

Next, a digital chirp synthesizer PLL covering an output frequency range from 18 to 22GHz and producing a 25-segment chirp is designed in 65nm CMOS to feed a 240GHz FMCW radar system. This PLL adapts the noise-shaping TDC design presented in [4], which consists of a conventional analog phase detector front-end, i.e. a conventional combination of a phase-frequency detector (PFD) and a charge pump, followed by a continuous-time 3^{rd}-order ΔΣ modulator. A prototype synthesizer achieves low close-in phase noise of -88dBc/Hz at 100kHz offset for wide PLL bandwidths. Experimental results of a radar testbed demonstrate that the synthesizer can effectively drive an FMCW radar system.

The main body of work introduces a noise-shaping TDC based on a continuous-time bandpass ΔΣ modulator (BPDSM). The novel bandpass ΔΣ TDC (BPDSTDC) leverages the high resolution in the center bandwidth of a BPDSM gained from oversampling and noise-shaping to achieve low TDC noise. It digitizes a sinusoidal reference while using the PLL feedback signal as a sampling clock, and applies digital down-conversion to provide the captured phase information as a dc value. By combining a BPDSM with explicit down-conversion in the digital domain, the BPDSTDC avoids low-frequency TDC noise contamination, makes efficient use of the BPDSM bandwidth and has an extended phase detection range, thus offering several advantages over

conventional ADC-based time-to-digital conversion. Based on the BPDSTDC, a digital FMCW chirp synthesizer PLL with an output frequency range from 36.3 to 38.2GHz is presented [2]. To ensure low close-in phase noise with fractional-N operation, the PLL design reduces fractional-N ΔΣ divider noise by using a feedback divider with a phase interpolator to emulate divider ratios with a small divider ratio step size. The BPDSTDC achieves low integrated noise of $325fs_{rms}$ in a 1MHz bandwidth and enables low close-in phase noise of -85dBc/Hz at 100kHz offset for wide PLL bandwidths >1MHz in a 40nm CMOS prototype. The prototype PLL includes on-chip control logic to generate fast and precise triangular chirps for FMCW radar applications.

1.4 Outline of the Dissertation

This dissertation is organized as follows. Chapter 2 summarizes PLL fundamentals and reviews basic analog and digital PLL implementations. Furthermore, conventional TDC designs are discussed and an overview of state-of-the-art high-frequency PLLs and fully-integrated chirp synthesizer PLLs is provided. Chapter 3 discusses the impact of the loop bandwidth of an FMCW chirp synthesizer PLL on the radar performance with an analysis supported by simulation results. Chapter 4 describes a 20GHz FMCW chirp synthesizer with a 3^{rd}-order noise-shaping TDC. Background information about the application is provided and stand-alone measurement results of a 65nm CMOS prototype as well as test results of a radar testbed are presented. Chapter 5 describes a 38GHz FMCW chirp synthesizer PLL with a bandpass ΔΣ TDC. Discussions include the operating principle and advantages of the TDC design as well as implementation details of the synthesizer architecture and individual PLL components. In addition, measurements of a 40nm CMOS prototype are presented. Chapter 6 concludes the dissertation and suggests future work.

CHAPTER 2 Review and Background Information

The research presented in this dissertation addresses the design of high-frequency digital chirp synthesizer PLLs for FMCW radar and focuses on novel noise-shaping time-to-digital conversion techniques. In this chapter, fundamentals of PLLs and basic PLL design concepts are reviewed. Moreover, a discussion of conventional TDC design techniques is provided. The chapter concludes with an overview of state-of-the-art high-frequency and chirp synthesizers PLLs.

2.1 Overview of Phase Locked Loops

Integrated PLLs find widespread use as signal sources in numerous applications and are indispensable components in modern RF communication systems. Accordingly, standard literature on RF IC design covers basic PLL principles in detail [18], [19] and thorough theoretical phase noise analyses have been developed [20]. In contrast to integer-N PLLs, fractional-N PLLs allow a fine resolution of the PLL output frequency as required for many applications, e.g. FMCW radar. While PLLs have traditionally been implemented as analog PLLs, digital PLL designs promise to overcome the drawbacks of their analog counterparts.

2.1.1 Fundamental PLL Architecture and Operation

A PLL is essentially a feedback control system that acts on phase and synchronizes the phase (and with it the frequency) of its output to a reference [21]. The schematic in Figure 2.1 shows the basic architecture and core components of a PLL. The voltage-controlled oscillator

(VCO) generates a high-frequency signal whose frequency is proportional to the tuning voltage at the VCO input. The frequency divider forms the feedback path of the loop and divides the VCO output frequency, producing an output signal whose frequency is equal to (or during start-up at least close to) the reference frequency of the PLL. The phase detector (PD) processes the reference clock and the feedback signal (i.e. divider output) and measures the phase difference between the two signals. The PD output can have different forms depending on the implementation of the PD and PLL, e.g. current pulses of a charge pump in an analog PLL or digital output words of a TDC in a digital PLL. Finally, the loop filter stabilizes the feedback loop, smoothing the PD output and providing the tuning voltage for the VCO.

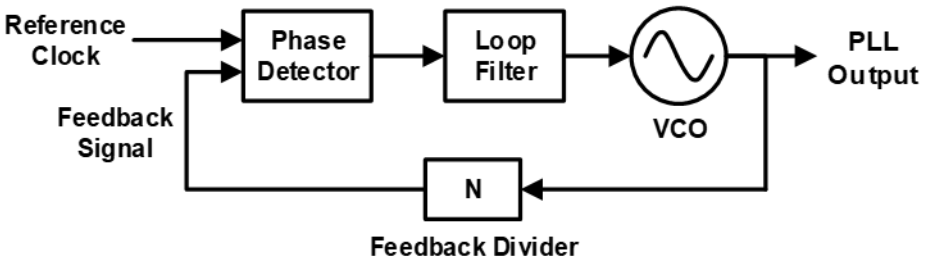


Figure 2.1. Basic PLL architecture with core components

Assuming the VCO tuning voltage has settled to a level such that the frequencies of reference and feedback are equal, e.g. after power-up of the PLL, the PLL is locked and the output frequency is given as $F_{out} = N \cdot F_{ref}$, where N is the division ratio of the feedback divider. In this case, the PLL output phase is locked to the reference phase because the negative feedback of the loop drives the phase difference between reference clock and feedback signal to zero. An analysis of the noise contributions in a PLL shows that noise sources associated with the reference node contribute to the output phase noise of the PLL while being subject to a low-pass transfer characteristic. In contrast, VCO phase noise is subject to a high-pass transfer characteristic. Consequently, high-frequency phase noise of the VCO reaches the PLL output unfiltered and

determines the output phase noise at high frequency offsets while low-frequency phase noise of the VCO is suppressed by the PLL. At low frequency offsets, the phase noise performance of the PLL depends on the PD noise, reference noise and divider noise. The PLL bandwidth marks the cut-off frequency of the PLL transfer characteristic. For a higher bandwidth, more VCO phase noise is suppressed, but more reference and PD noise passes through to the PLL output. The PLL bandwidth must be chosen appropriately according to the requirements of the respective application. The bandwidth of PLLs used as local oscillators in RF transceivers is typically set to minimize the PLL output jitter while chirp synthesizer PLLs for FMCW radar must offer fast frequency settling, which translates to wide PLL bandwidths.

2.1.2 Integer-N and Fractional-N PLLs

Keeping the reference frequency constant, the output frequency of a PLL can be changed by changing the division ratio N. The feedback divider is essentially a digital counter, as it counts the oscillation cycles of the VCO and produces one cycle per N VCO cycles at its output. The divider can be made programmable so that a digital control word can be used to set the division ratio. Since the division ratio is restricted to integer values, the output frequency resolution of an integer-N PLL is limited by the reference frequency. However, many applications depend on a fine frequency resolution. For example, RF communication systems must be tuned to narrow frequency bands for channel selection. FMCW radars require a continuously tunable frequency in theory, traversing a continuous chirp profile. Reducing the reference frequency to achieve a finer resolution is usually not an option because the reference frequency must be significantly higher than the PLL bandwidth (factor of ≈10) to ensure sufficient suppression of reference spurs in the PLL output spectrum [18]. Typical values for the PLL bandwidth are a few hundred kilohertz to

suppress low-frequency VCO phase noise. For fast chirp generation, high PLL agility requires wide bandwidths in the megahertz range, thus limiting the frequency resolution of an integer-N PLL to a few megahertz, which is unacceptably coarse for the accuracy requirements of an FMCW radar.

A fractional-N PLL implements fractional division ratios to achieve a fine resolution of its output frequency. The problem of limited frequency resolution with integer-N PLLs can be solved by switching the division ratio of the programmable divider between different integer values in such a fashion that the average value is equal to the desired fractional value. This type of averaging is commonly implemented by a ΔΣ modulator that controls the programmable divider [22]. The ΔΣ modulator produces a stream of coarsely quantized digital output words based on a high precision digital input value, while the low-frequency average of the output is equal to the high precision input. The noise transfer characteristic of the ΔΣ modulator suppresses quantization noise at low frequencies at the expense of increased high-frequency noise, i.e. the quantization noise is shaped to high frequencies. Like the reference noise and the PD noise, the ΔΣ divider noise introduced into the loop by the modulator is low-pass filtered. Therefore, the high-frequency ΔΣ noise is filtered out and does not affect the phase noise performance of the PLL if the loop bandwidth can be assumed not to be too wide. Modulating the programmable divider by means of ΔΣ modulation allows almost arbitrary fractional division ratios, resulting in very fine PLL frequency resolution.

2.1.3 Analog and Digital PLLs

Traditional PLLs are implemented as analog PLLs and feature a PFD with a charge pump followed by an analog loop filter. A block diagram of an analog fractional-N PLL implementation

is shown in Figure 2.2. The PFD measures the phase difference between reference and feedback signals and produces voltage pulses at its UP or DOWN outputs. The location of the pulses can be interpreted as the sign of the phase difference, i.e. if the pulse appears at the UP (or DOWN) output, then the reference signal (or the feedback signal) leads. The widths of the pulses are a measure of the absolute phase difference. The charge pump converts the PFD pulses to current pulses, which are then filtered and smoothed by the loop filter. Such analog PLL implementations rely on analog-intensive circuits for phase detection and filtering, making the PLL design more sensitive to PVT variations and reducing design portability between technology nodes. Moreover, analog PLLs offer limited reconfigurability of the loop parameters, i.e. adjustments of the charge pump current and the loop filter settings, and the analog loop filter typically consumes a large area due to the sizes of the capacitors.

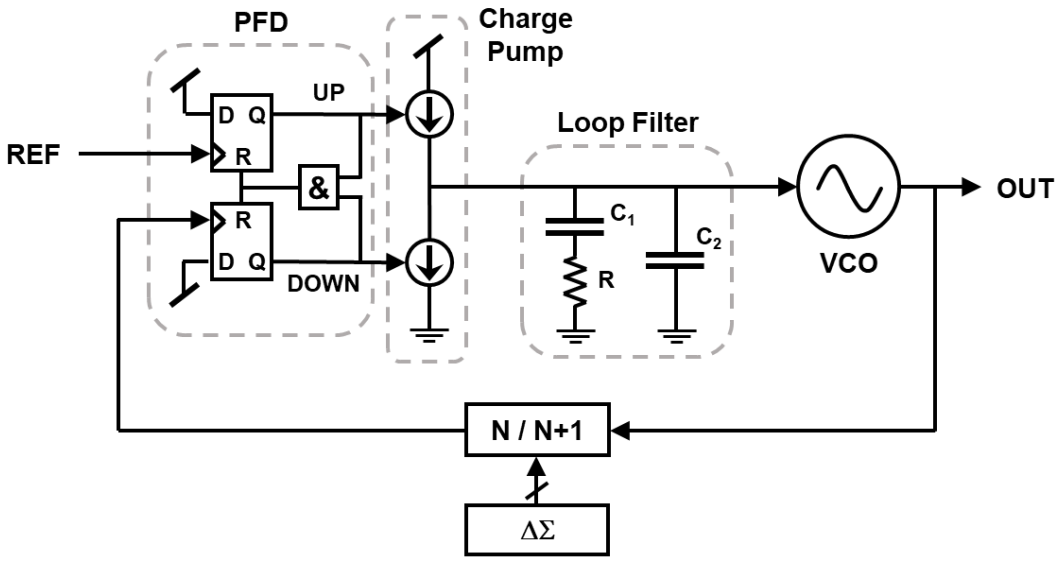


Figure 2.2. Conventional analog fractional-N PLL

Digital implementations of PLLs promise to overcome these shortcomings of analog PLLs. A basic digital fractional-N PLL architecture with core components is shown in Figure 2.3. Digital PLLs use digital loop filters and can therefore offer better area efficiency and greater

programmability regarding the settings of the loop dynamics. Since the loop filter processes digital inputs, digital PLLs depend on phase detection techniques that provide digital output words as measures of the phase difference between the reference and feedback signals. Measuring the phase alignment or, in other words, the time between the edges of the input signals and converting it to the digital domain, these types of phase detectors are referred to as time-to-digital converters (TDCs). Low close-in phase noise of digital PLLs depends on accurate phase detection and thus requires low quantization noise, or high time resolution, in the TDC. This design challenge must be given even more attention if wide-loop-bandwidth PLLs are desired, e.g. for FMCW chirp synthesis, because a wider loop bandwidth allows more TDC noise to contribute to the PLL output phase noise. An additional challenge of digital PLL design is the implementation of oscillators whose output frequency can be tuned digitally by a control word produced by the digital loop filter. Such a digitally-controlled oscillator (DCO) can be implemented by combining a high resolution digital-to-analog converter (DAC) with a conventional VCO [2], [6], or in a more digital fashion by tuning the oscillator frequency using digitally-controlled capacitive tuning banks [7], [17].

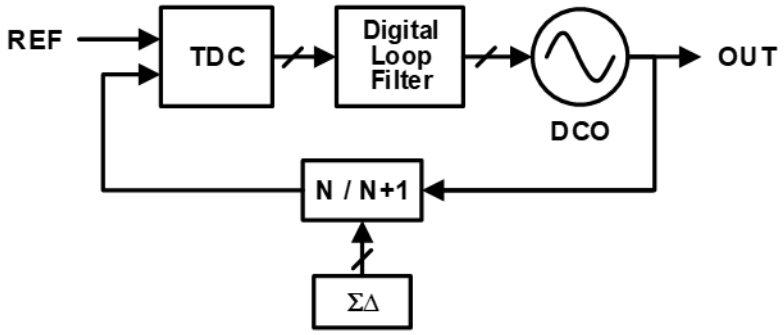


Figure 2.3. Digital fractional-N PLL architecture

2.2 Conventional TDC Design

A well-known, yet very simple TDC architecture is a delay-line TDC [23], as shown in Figure 2.4. The input signal passes through a chain of unit delay elements, e.g. inverters. The delay chain essentially quantizes time and is sampled by flip-flops, which are triggered by the TDC clock. The thermometer code obtained from combining the flip-flop outputs indicates the time difference between the edges of the input and the TDC clock. If compared with ADCs, this approach is analogous to a flash ADC, which uses a resistor ladder to quantize a reference voltage range and a series of comparators to compare the input voltage to the reference voltages.

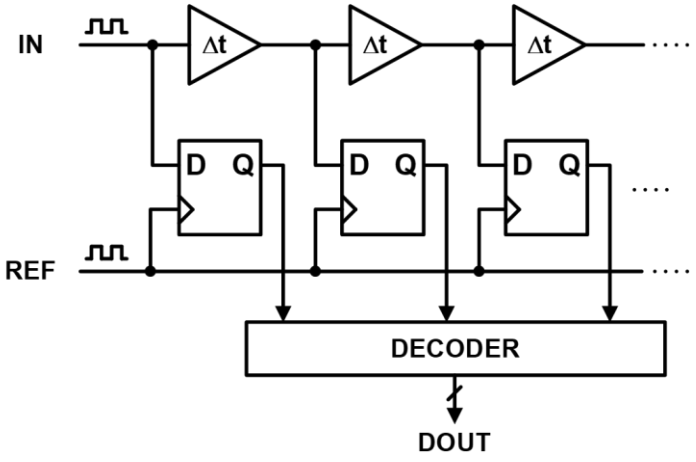


Figure 2.4. Delay-line time-to-digital converter

Although a delay-line TDC represents a very direct approach to time-to-digital conversion, its performance has several limitations. First, the time resolution of a delay-line TDC is limited by a single gate delay, which is in the range of several picoseconds and too coarse to enable low close-in phase noise in high-frequency PLLs. Second, the TDC linearity suffers from gate delay mismatch. Consequently, PVT variations affect both resolution and linearity of the TDC and cause the full-scale range of the TDC to vary. Since delay mismatches and random jitter accumulate along the delay chain, it is desirable to keep the delay chain short, but this limits the TDC range.

Several alternative TDC architectures have been demonstrated that mitigate or overcome the limitations of a basic delay-line TDC. A looped TDC increases the full-scale range of a delay-line TDC by using a delay line that forms a loop [24]. The input signal can pass through the delay line loop several times and, in principle, the TDC can measure time intervals of arbitrary length. This type of TDC is therefore relatively area-efficient, but the layout of the loop inevitably introduces systematic non-linearity. Instead of measuring the complete time difference with full TDC resolution, a hierarchical or two-step TDC uses a first TDC stage to coarsely quantize the input time difference and then feeds the residue into a second TDC stage with fine resolution [25]. This approach reduces area and power consumption compared to a basic delay-line TDC, but it is very challenging to implement due to mismatch and latency introduced by the coupling paths between the two TDC stages. To achieve sub-gate delay resolution, a Vernier TDC uses delay lines for both the input signal and the TDC clock, with the unit delay elements in the clock line having a different delay than those in the input line [26]. As a result, the time difference between the two different delay elements determines the TDC resolution. However, a Vernier TDC uses twice the number of delay elements, which increases mismatch and area consumption. A local passive interpolation TDC does not rely on two different unit delays but interpolates the signal edges at consecutive delay elements by means of resistor ladder segments [27]. These segments are tapped to obtain additional intermediate signal transitions, allowing fine sub-gate delay resolution. Another approach to achieve fine resolution is time amplification, usually applied in a two-stage TDC [28]. The time difference being the residue of a coarse quantization stage is enlarged by a time amplifier before being injected into a fine quantization stage. Linearity and noise of the time amplifier critically affect the TDC performance. Finally, noise-shaping TDCs have been demonstrated to enable sub-gate delay resolution. Noise shaping in a TDC can be implemented by

reusing information about the quantization error from the previous measurement in the next one. As an example, a gated-ring-oscillator TDC samples and freezes the states of a gated looped delay line in every measurement step before releasing them at the beginning of the next measurement interval and thus effectively accomplishes first order noise shaping [29].

2.3 State-of-the-Art High-Frequency and Chirp Synthesizer PLLs

Advances in silicon technology have made fully-integrated high-frequency chirp synthesizer PLLs possible, and an increasing demand for compact and low-cost high-frequency FMCW radars have fueled research efforts in this area. In general, high-frequency (>20GHz) PLLs are still predominately analog [15], [16]. Accordingly, early fully-integrated CMOS chirp synthesizers [10], [11] as well as more recent works [5] are based on analog PLL implementations. Although digital PLLs promise greater flexibility and area efficiency, performance limitations related to the TDC and the DCO hinder the adoption of high-frequency digital PLLs. Hybrid PLL designs combine the advantages of analog and digital PLLs at the cost of increased design complexity [30]. A mixed-mode chirp synthesizer architecture using mostly digital blocks has been demonstrated, but suffers from poor close-in phase noise [8]. More recently, mm-wave all-digital PLLs have been introduced, but fail to achieve low close-in phase noise [7], or depend on extensive calibration [17]. Two-point modulation has become a popular design approach for chirp synthesizer PLLs to overcome the fundamental design trade-off between wide PLL bandwidth and low close-in phase noise [3], [6], [7]. However, these designs rely on calibration as they must account for potential gain and timing mismatch between the two modulation paths.

CHAPTER 3 Analysis of PLL Bandwidth and Chirp Linearity for PLL-based FMCW Chirp Synthesis

The accuracy and reliability of an FMCW radar depends on the generation of highly linear chirps. This chapter presents an analysis of the PLL bandwidth and chirp linearity based on a Simulink model of a complete radar system. The model incorporates a detailed model of a fractional-N chirp synthesizer PLL and considers design aspects of the DSP back-end as well. The analysis examines the impact of the PLL bandwidth on the radar performance and quantifies the upper and lower bounds of the PLL bandwidth.

3.1 PLL Bandwidth Optimization

FMCW radar is based on the premise that the frequency chirps are perfectly linear so that the beat frequencies accurately represent the parameters of the detected targets. An optimized PLL bandwidth is key to achieving high chirp linearity. The PLL division ratio (Figure 1.3) approximates the chirp profile with a stair-like signal. This modulation is discrete in time and output value. The PLL bandwidth must be large enough for the PLL to follow the trajectory of the ideal linear chirp profile, requiring a bandwidth far greater than the chirp modulation frequency. At the same time, PLL settling must not be so fast that the PLL output frequency follows the stepped modulation signal too closely. This requires a PLL bandwidth less than the stepping rate of the modulation signal. Consequently, an optimized loop bandwidth satisfies the following inequalities:

$$\frac{1}{T} \ll BW_{PLL} < \frac{2^{lin} - 1}{T/2} \tag{3.1}$$

Here, T denotes the period of a triangular FMCW chirp profile. The modulation signal is assumed to comprise 2^{lin} output quantization levels, and the stepping rate is described as a function of the chirp resolution denoted by lin in bits. The following analysis quantifies the inequalities in (3.1) and examines the impact of the PLL bandwidth on the detection reliability and accuracy. Although general guidelines can be given regarding the design of an FMCW chirp synthesizer PLL, it is hard to evaluate synthesizer performance and provide design guidance without a specific application scenario. The analysis assumes the well-known 77GHz standard for long-range automotive radar (LRAR) to examine PLL requirements and evaluate radar performance. The methodology presented in this chapter can be easily applied to other scenarios.

3.2 Model and Simulation Setup

In preparation for the PLL bandwidth analysis, a simple phase-domain model of an analog type-II PLL (Figure 3.1) is used to first determine the PLL configuration (charge pump current, loop filter component values) for different bandwidths extending from 100kHz to 10MHz. The chosen PLL settings ensure loop stability with 60° phase margin. As an example, Figure 3.2 shows the magnitude and phase of the loop gain for a loop bandwidth of 1MHz. Throughout the analysis, a 500MHz PLL reference, a 77GHz PLL output in accordance with the LRAR scenario, and a VCO gain of 1GHz/V are assumed.

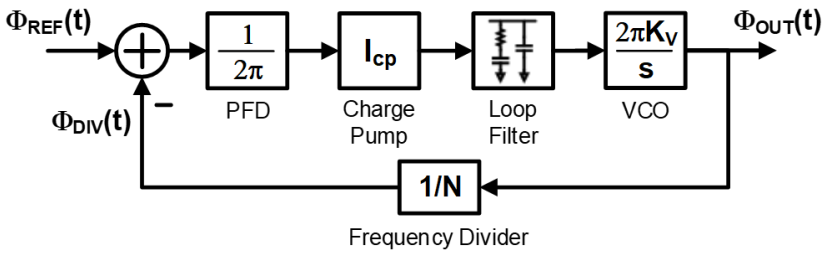


Figure 3.1. Phase-domain PLL model

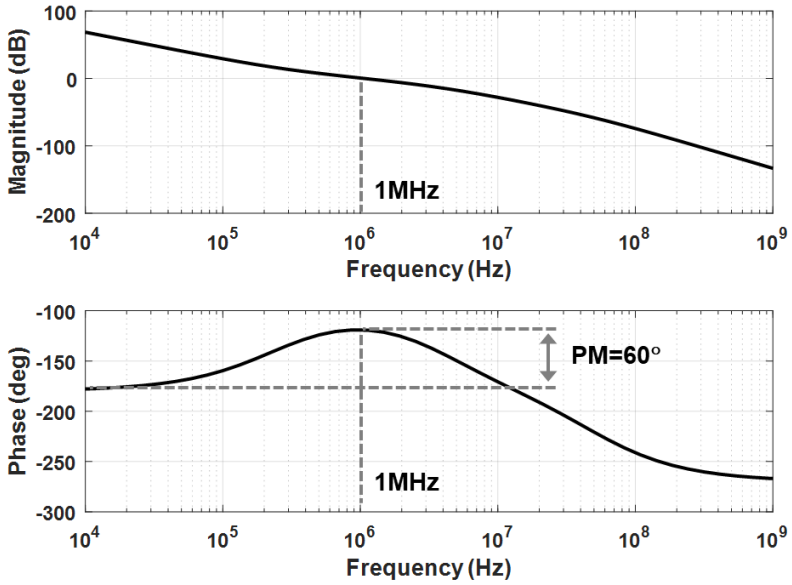


Figure 3.2. Bode plot of loop gain for a 1MHz loop bandwidth

A time-domain model of a fractional-N PLL for chirp generation simulations would result in long simulation times because the PLL output period and the chirp modulation period differ by orders of magnitude. The Simulink-based synthesizer model developed for this analysis (Figure 3.3) operates in the phase/frequency domain instead, allowing fast simulation. The output signal of the model represents the PLL output frequency. Reference phase and feedback phase are obtained by integrating the constant reference frequency and the feedback frequency, respectively. A zero-order-hold element in the forward path models the update of the charge pump output at reference rate. In a similar manner, a zero-order-hold element samples a continuous chirp

waveform signal in the time and value domains to produce a stair-like modulation signal with the desired stepping rate.

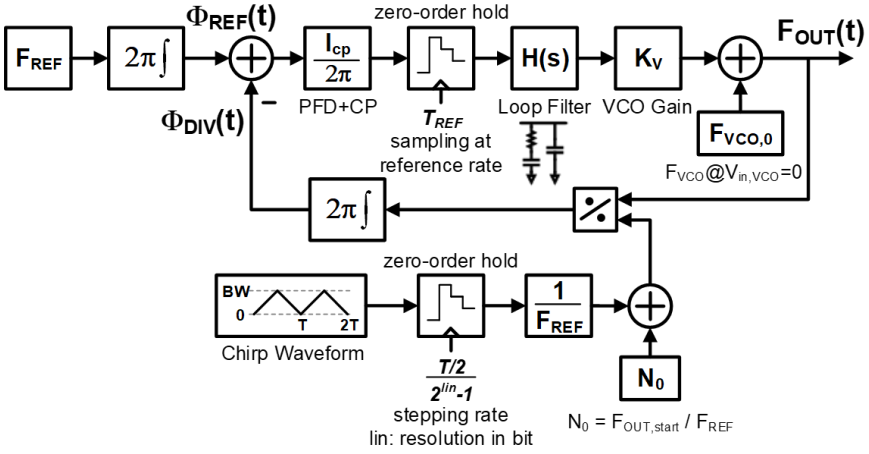


Figure 3.3. Phase/Frequency model of an FMCW chirp synthesizer PLL

The synthesizer model is employed as a subsystem in a Simulink-based FMCW radar system model (Figure 3.4). The system model uses a delay block to model the roundtrip propagation delay of the radar signal and adds a frequency shift to account for a Doppler effect due to a moving target. The mixing operation in the receive path is modeled by subtracting the receive frequency signal from the synthesizer output, resulting in a signal that represents the beat frequency. To reflect the baseband processing of a real transceiver system, an oscillator block generates a signal with its instantaneous frequency being equal to the obtained beat frequency. An ideal quantizer converts the baseband signal to the digital domain before an FFT is performed on the signal.

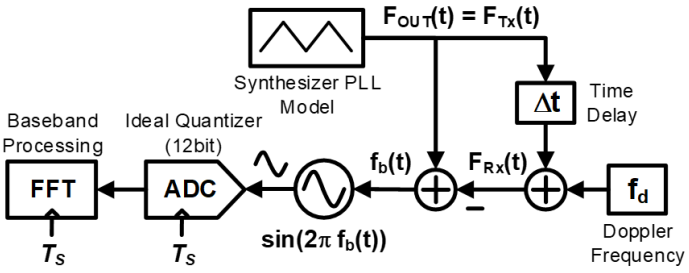


Figure 3.4. Model of an FMCW radar system with chirp synthesizer model

3.3 Approach for Result Evaluation

As a part of the analysis, the chirp modulation period T is modified to implement varying chirp slopes. $T_{S,FFT} = N/F_S$ denotes the time required to collect N data points for an N-point FFT with sample rate $F_S = 1/T_S$. $T_{S,FFT}$ should be as large as possible (ideally equal to the chirp duration $T/2$) to achieve best beat-frequency resolution. Therefore, F_S is adapted to the modulation period used in each case. Since the largest linearity errors of a triangular chirp occur at the turnaround points, time gating can be applied to block these non-linear portions of the chirp from being processed by the FFT [14]. Accordingly, $T_{S,FFT} = m \cdot T/2$, where m denotes the time gating factor ($m < 1$). The minimum resolvable beat frequency is then given as[1]

$$\Delta f_b = \frac{F_S}{N} = \frac{1}{T_{S,FFT}} = \frac{2}{m \cdot T} \tag{3.2}$$

Using (1.1) and (1.3), the minimum resolvable range resolution can be obtained from (3.2) as

$$\Delta R = \frac{c\,T}{4\,BW} \cdot \Delta f_b = \frac{1}{m} \cdot \frac{c}{2\,BW} = \frac{1}{m} \cdot \Delta R_{ideal} \tag{3.3}$$

Clearly, time gating somewhat coarsens the range resolution for the sake of better effective chirp linearity. For this analysis, $m = 90\%$ to process only the inner 90% of each chirp ramp. Regarding the number of FFT points, N, a large enough N is used to ensure the unambiguous detection of the maximum beat frequencies by satisfying the Nyquist criterion $F_S > 2\,f_{b\_max}$. With $F_S = N/T_{S,FFT}$ and $T_{S,FFT} = m \cdot T/2$, (1.1) can be used to reformulate this inequality as

$$N > m \cdot \frac{4\,BW}{c} \cdot R_{max} \tag{3.4}$$

[1] The frequency resolution can be improved by using interpolation between FFT bins [31].

A modulation bandwidth of 500MHz is used in the analysis, which, according to (1.3), offers an appropriate range resolution of 0.3m for the LRAR scenario. Assuming a realistic maximum target range of 200m, this work uses $N = 2^{11} = 2048$.

Before trying to quantify (3.1), it is instructive to take a look at the generated chirp waveforms in Figure 3.5 for optimized and non-optimized PLL bandwidths. If the PLL bandwidth is too small (Figure 3.5(a)), the generated chirps clearly show poor linearity, impeding accurate detection. If the PLL bandwidth is too large (Figure 3.5(c)), the output waveform follows the stair-like modulation signal too closely and the associated non-linearity results in spurious peaks in the FFT spectrum, increasing the risk of detection of ghost targets. An optimized PLL bandwidth (Figure 3.5(b)) offers the best chirp linearity.

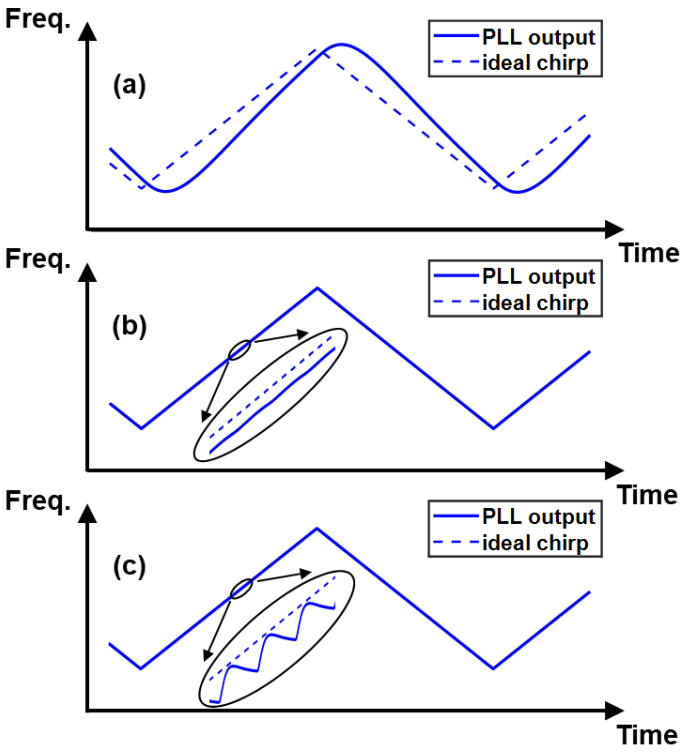


Figure 3.5. Simulated synthesizer output waveforms for too small PLL bandwidth (a), optimized PLL bandwidth (b), and too large PLL bandwidth (c)

If the radar utilizes the beat frequencies resulting from both up- and down-chirps to calculate the target velocity using (1.2), the velocity resolution required for the application scenario dictates the minimum modulation period of the triangular chirp, as stated by (1.4). For the LRAR scenario, Δv = 5km/h is assumed as a sufficient performance parameter, corresponding to a modulation period of 1.4ms. This is to be considered a slow modulation signal and does not present a challenge to the left half of (3.1). However, the PLL bandwidth must be small enough and combined with a sufficiently large number of quantization levels in the modulation signal to ensure that the right half of (3.1) is satisfied. In Section 3.4 , the presented analysis quantifies the right half of (3.1), using a long modulation period of 2ms. Section 3.5 then focuses on fast modulation signals.

3.4 Generation of Slow Chirps

A rather low PLL bandwidth and a large resolution of the stair-like modulation signal are critical for the radar performance if slow chirps are generated. This scenario is the subject of the first part of this analysis. Too large a PLL bandwidth can significantly degrade the chirp linearity, as can be seen in Figure 3.5(c). The observed non-linearity in the output waveform translates to spurious peaks in the FFT spectrum [32]. As an example, Figure 3.6 shows the simulated FFT spectra for the radar system model of Figure 3.4 for a PLL bandwidth of 1MHz and two different chirp modulation stepping rates. For a stepping rate of 1MS/s, the right half of (3.1) is not sufficiently satisfied, and as a result, there are numerous spurious peaks in the spectrum (Figure 3.6(a)), degrading the spurious-free dynamic range (SFDR) to be only 18dB. In contrast, a stepping rate of about 8 times the PLL bandwidth greatly reduces the spur levels and yields a high SFDR of 77dB (Figure 3.6(b)). If the stepping rate is increased even further, spurious peaks due to chirp

non-linearity eventually disappear altogether and the SFDR approaches an upper limit of around 95dB.

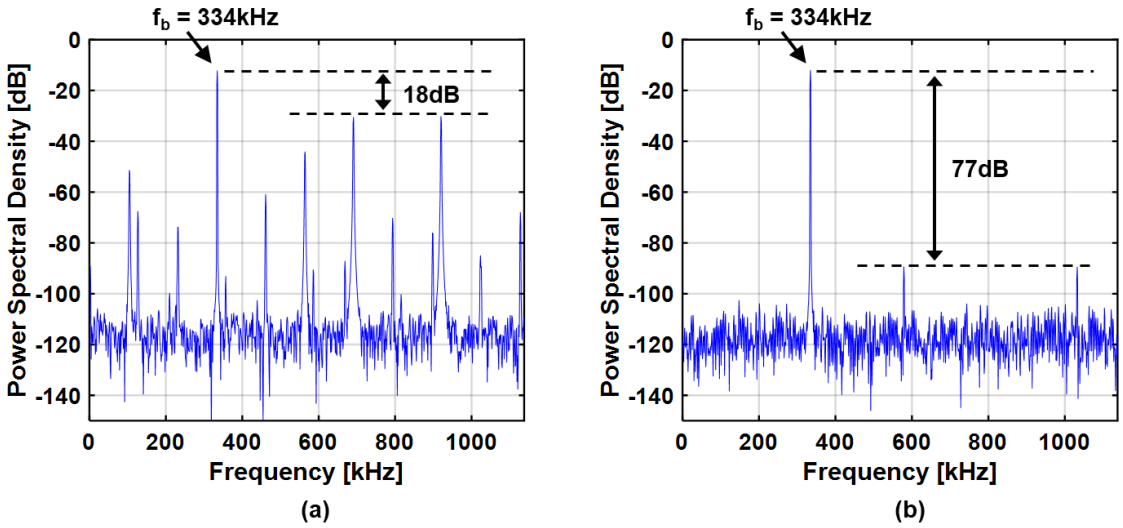


Figure 3.6. FFT spectra for BW_{PLL} = 1MHz, T = 2ms, R = 100m, v = 0km/h, and stepping rates of 1.0MS/s (10bit resolution) (a) and 8.2MS/s (13bit resolution) (b)

For a given FMCW radar system and application scenario, the receive signal power depends on the radar cross section (RCS) of the target as well as on the target range. According to the RCS diagram in [1], the RCS can vary up to about 30dB around the rear of a car. Moreover, if a target range from 80m to 150m is assumed, the receive signal power varies up to an additional 11dB. Because of this combined receive-power variation of more than 40dB, a minimum SFDR margin is required in this analysis to distinguish beat frequencies from spurious peaks. In the following, an SFDR margin of 45dB is used and associated with sufficient chirp linearity.

The PLL bandwidth is swept from 100kHz to 10MHz and the modulation signal resolution from 9 bits to 14 bits, while the chirp bandwidth is 500MHz and the modulation period is 2ms. In all these cases, the radar model correctly resolves the target range (R = 100m) within ΔR = 0.3m and the target velocity (v = 10km/h) within Δv = 5km/h. Simulation results in Figure 3.7 show the FFT SFDR as a function of the PLL bandwidth for varying modulation resolution, i.e. different

stepping rates. For a given PLL bandwidth, the SFDR is significantly worse for lower modulation resolution because the PLL output follows the stair-like modulation signal more closely. The SFDR decreases for the same reason if the PLL bandwidth is increased and the modulation resolution is kept constant. For lower resolutions, however, the SFDR levels off at high PLL bandwidths because there is no significant degradation in chirp linearity beyond a certain PLL bandwidth anymore. Also, the SFDR is upper-limited by the noise floor. No noteworthy spurs appear in this case and the upper limit of the SFDR is approximately 95dB.

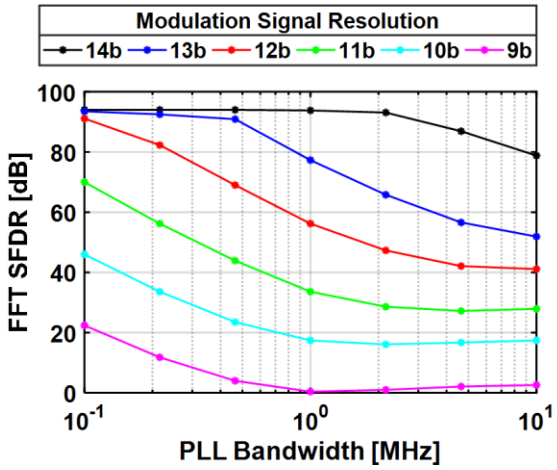


Figure 3.7. SFDR in FFT spectrum as a function of PLL bandwidth and chirp modulation resolution for T = 2ms

The above results provide guidance for the optimal choices for the PLL bandwidth and modulation resolution. In general, SFDR is best with low PLL bandwidths for slow chirp modulation. However, it should be taken into account that the beat frequency is only about 300kHz in the given scenario, and it is advisable to choose a PLL bandwidth larger than that to limit VCO noise. With a lower PLL bandwidth, the close-in phase noise of the PLL may be too high as too much VCO noise contributes to the PLL output phase noise. Figure 3.7 suggests that a PLL bandwidth of around 1MHz and a modulation resolution of at least 12bit (which corresponds to a stepping rate of 4.1MS/s with T = 2ms) are an appropriate design choice for the given scenario.

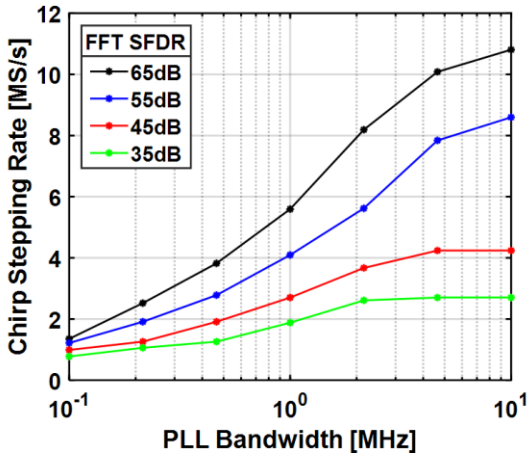


Figure 3.8. PLL bandwidth vs. stepping rate characteristic for constant SFDRs and T = 2ms

A similar perspective is provided by Figure 3.8, which illustrates the relationship between PLL bandwidth and chirp stepping rate for constant SFDR values. Again it can be seen that a higher PLL bandwidth requires a higher stepping rate for the same SFDR, i.e. to maintain the chirp linearity, and that the SFDR results tend to level off for high PLL bandwidths. Taking 45dB as the minimum required SFDR, it can be concluded that a chirp stepping rate exceeding the PLL bandwidth by a factor of 3 to 6 sufficiently satisfies the right half of (3.1) for the given scenario. As pointed out above, the close-in phase noise performance of the synthesizer must be taken into account as, in practice, this may set a lower bound for the PLL bandwidth.

3.5 Generation of Fast Chirps

The second part of this analysis examines the radar performance in the case of fast chirps and focuses on the left half of (3.1). Fast FMCW chirps result in higher beat frequencies that are potentially located outside the close-in phase noise region of the synthesizer. However, considering (1.4), a triangular chirp radar cannot provide reasonable velocity resolution with fast chirps, and one must resort to different approaches for velocity estimation. For this reason, only

the accuracy of the range detection is considered here as the radar model is used to generate fast chirps and evaluate the radar performance. Again, a modulation bandwidth of 500MHz and a target range of 100m are used. Since the results for the target range are not affected by the target velocity, the target velocity is set to zero. The rms linearity frequency error is calculated from the difference between the synthesizer output waveform and an ideal linear fit while the vicinity of the turnaround points is discarded, and the chirp non-linearity is expressed as a percentage of the chirp modulation bandwidth [14].

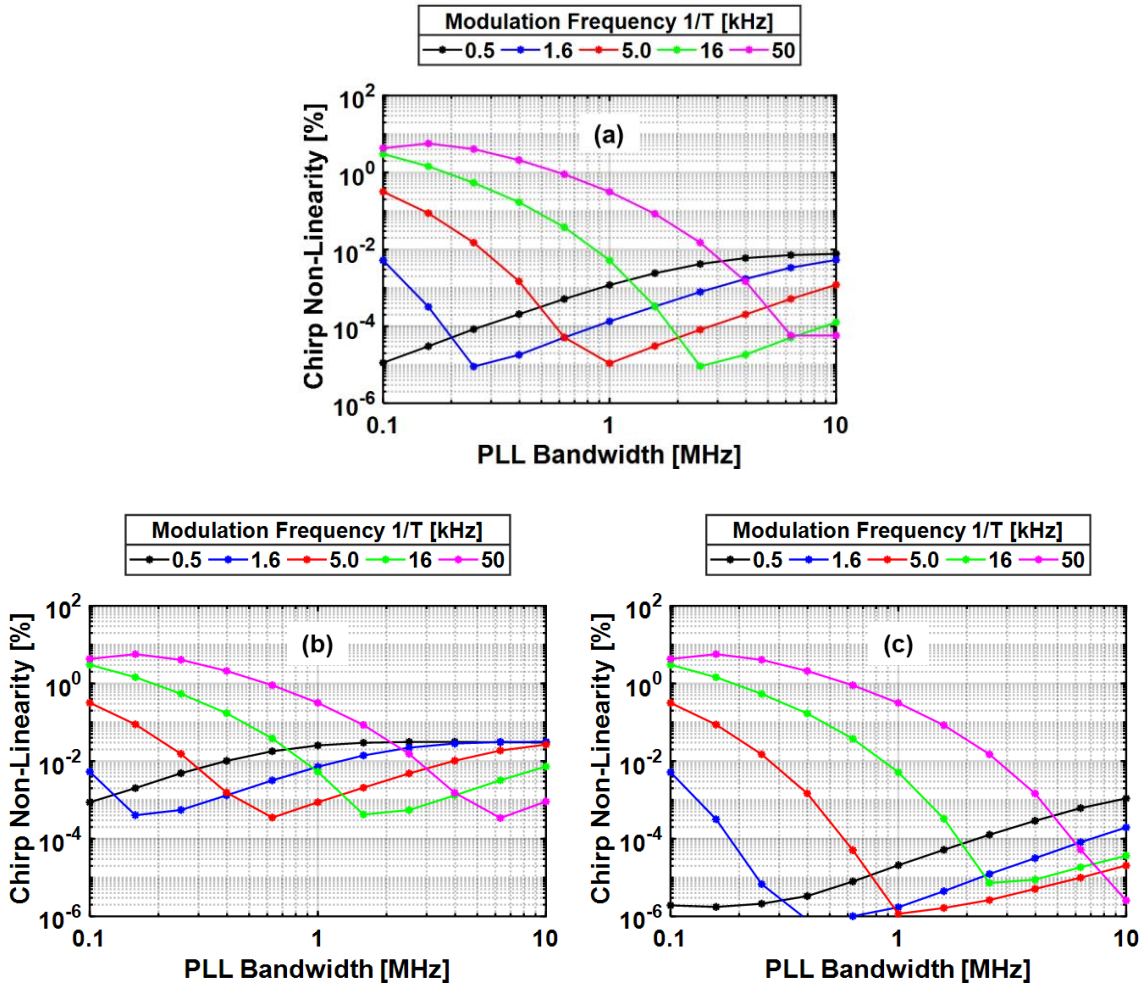


Figure 3.9. Chirp non-linearity as a function of PLL bandwidth and modulation frequency for a modulation resolution of 12bit (a), 10bit (b), and 14bit (c)

Figure 3.9 shows the chirp non-linearity for varying PLL bandwidths and chirp modulation frequencies. Clearly, fast chirp modulation combined with a low PLL bandwidth results in poor chirp linearity because the PLL is not fast enough to follow the trajectory of the ideal chirp profile (Figure 3.5(a)). Moreover, the chirp linearity degrades as the PLL bandwidth becomes very large, increasing the tendency of the PLL to approximate the stair-like modulation signal. Consequently, there is an optimum bandwidth that minimizes the chirp non-linearity. As (3.1) suggests, this optimum bandwidth increases with the chirp modulation frequency. Comparing the plots in Figure 3.9, one can also observe an increase in the optimum PLL bandwidth with the modulation resolution. In addition, the minimum chirp non-linearity greatly improves with the modulation resolution, suggesting the use of a very high stepping rate. However, this result may not accurately reflect a real design scenario as the modeled radar system is noiseless for the sake of simplicity. Also, it should be noted that the best linearity results suggested by Figure 3.9(c) exceed the chirp linearity typically required in practice.

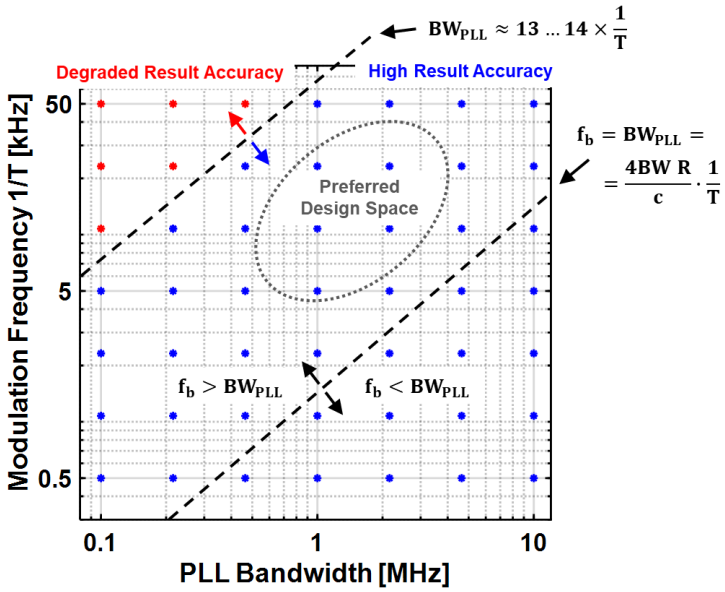


Figure 3.10. Result accuracy in the modulation frequency vs. PLL bandwidth design plane for a 500MHz chirp bandwidth and R = 100m

As the detection accuracy of the radar is evaluated, one half of the modulation frequency vs. PLL bandwidth plane can be identified that provides a degraded result accuracy (Figure 3.10), i.e. the detected target range deviates from the actual range of 100m by more than the range resolution of 0.3m. In this half-plane of the entire design space, the chirp modulation is too fast for the given PLL bandwidth, resulting in poor chirp linearity and beat frequencies that do not accurately represent the target range. The red dots in Figure 3.10 mark individual simulated range results with degraded result accuracy. In contrast, the blue dots mark range results that are within the range resolution. From the boundary of the two half-planes, the left half of inequality (3.1) can be quantified. Accordingly, (3.1) is sufficiently satisfied if the PLL bandwidth exceeds the modulation frequency by a factor of at least 14. For larger factors, however, more reliable results can be expected. At the same time, the PLL bandwidth should be chosen smaller than the beat frequency expected for the given LRAR scenario to take advantage of the fact that fast chirps result in beat frequencies outside the close-in phase noise. With this in mind, a recommended or preferred design space can be defined in the plane in Figure 3.10 that offers both accurate detection results and high beat frequencies. Also, this design space is placed around the 1-to-2MHz bandwidth range as a compromise between sufficient VCO noise suppression and uncommonly large PLL bandwidths.

CHAPTER 4 A 20GHz Digital 25-Segment Chirp Synthesizer using a Third-Order Noise-Shaping TDC

This chapter presents a 20GHz chirp synthesizer designed to drive a 240GHz FMCW radar. The synthesizer is based on a digital fractional-N PLL architecture[2] that features a 3rd-order noise-shaping TDC to enable fast frequency settling with low close-in phase noise [4]. The fabricated prototype includes programmable on-chip chirp generation logic to generate a segmented sawtooth chirp profile suitable for electronic beam steering. Stand-alone measurements of the synthesizer IC are performed and the synthesizer is also used as a signal source in a testbed that models a complete FMCW radar system.

4.1 Application Background

Advances in CMOS technology have paved the way for a new generation of integrated radar solutions as single-chip radars operating in the mm-wave range become feasible. These developments have motivated research on fully-integrated radar transceivers over the past decade. Moreover, the high operating frequencies allow the use of relatively small antenna arrays. The possibility of compact, light-weight and power-efficient radars opens new application areas such as indoor mapping and navigation radars mounted on flyers or crawlers. With these types of applications in mind, a 20GHz chirp synthesizer is designed as a signal source for a 240GHz FMCW radar system for Micro-Autonomous System Technologies (MAST) [33].

[2] The PLL architecture including the 3rd-order noise-shaping TDC is a direct adaptation of the work in [4].

An overview of the MAST radar architecture is given in Figure 4.1. The 20GHz PLL drives a multiplier chain consisting of two frequency doublers and a frequency tripler to generate transmitter output frequencies around 240GHz. The transmitter feeds a frequency scanning antenna array to cover a specified field of view by applying electronic beam steering. The received signal is mixed with the transmit signal generated by the multiplier chain to down-convert it to baseband. Finally, baseband processing extracts the beat frequencies and determines the properties of the detected targets.

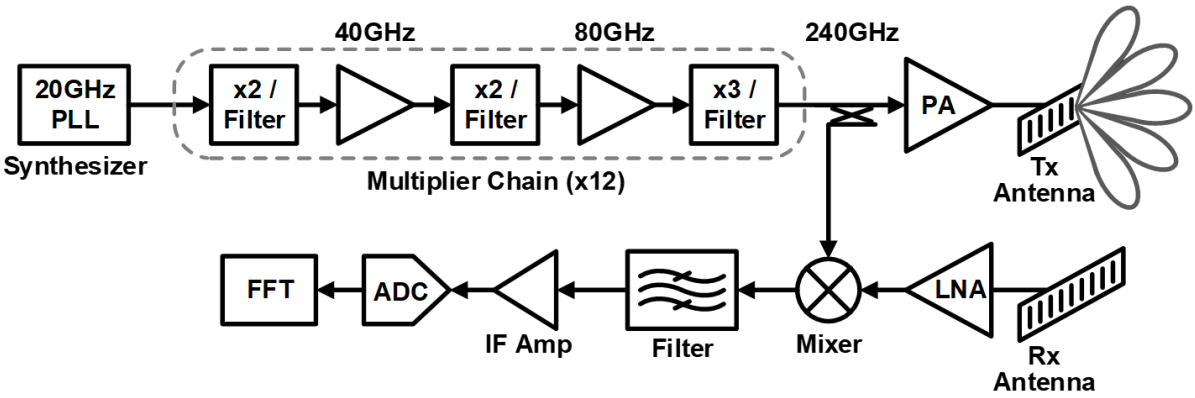


Figure 4.1. MAST 240GHz radar architecture

The MAST 240GHz radar is specified to cover a 50° field of view by applying electronic beam steering and using a 2° beam width. For this purpose, the transmitter is required to provide a chirp signal with a sawtooth profile consisting of individual 25 segments, as shown in Figure 4.2. The complete chirp frame is traversed periodically every 33.25ms. Each chirp segment is traversed in 1.33ms, has a bandwidth of 400MHz to satisfy to specified range resolution and is followed by a 200MHz jump to the next segment. The complete chirp extends over a bandwidth of 25×600MHz = 15GHz, ranging from 230GHz to 245GHz.

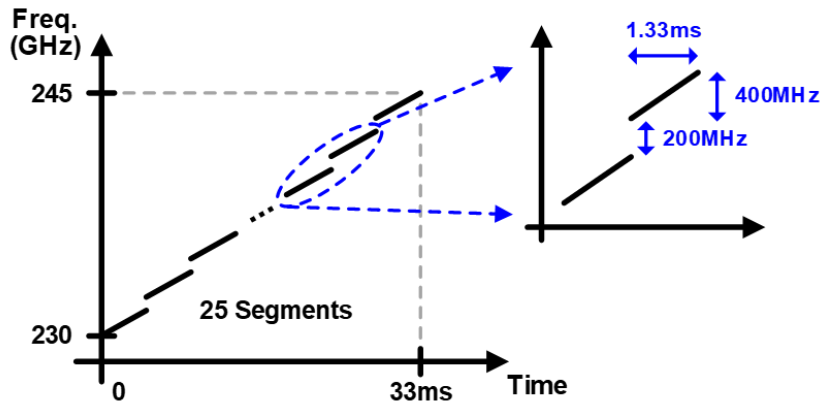


Figure 4.2. Chirp profile of transmitter output for MAST radar

The performance of the MAST 240GHz radar system crucially depends on the performance of the 20GHz chirp synthesizer, which must be capable of fast and accurate chirp generation while also offering sufficient programmability. As pointed out in Chapter 1, a chirp synthesizer PLL for FMCW radar must produce chirps with high linearity to ensure sufficient accuracy of the radar. A particularity of the chirp profile specified for the MAST radar is the fact that the beam steering requires the PLL output frequency to jump from segment to segment as the complete chirp profile is traversed. The PLL unlocks and relocks as its output frequency transitions between the segments or reaches the end of the chirp frame and returns to the starting frequency. The quality of the generated beams therefore depends on a short locking time of the PLL. The PLL design for the MAST radar targets a settling time of less than 5μs, translating to a PLL bandwidth greater than 1MHz. At the same time, the PLL output must be characterized by low close-in phase noise for the radar to meet sensitivity requirements. Finally, to simplify the operation of the radar, the synthesizer needs to incorporate chirp generation logic on-chip. From the specifications of the chirp profile given above, the synthesizer must generate a signal whose frequency is ramped up from 19.166GHz to 20.416GHz over 33.25ms. The ramp recurs periodically and consists of 25 ramp segments, with each segment having a linear chirp of 33.33MHz over 1.33ms and a jump of

16.67MHz to the next ramp segment. To satisfy the stated requirements, the 20GHz synthesizer presented in this chapter is based on a digital fractional-N PLL architecture with a high-resolution continuous-time ΔΣ TDC. This design approach enables a high PLL bandwidth to achieve the required settling speed while offering low close-in phase noise. To allow flexible chirp generation, the synthesizer incorporates programmable on-chip chirp control logic.

4.2 Implementation of Noise-Shaping TDC

The vast majority of high-frequency PLLs are still implemented as analog PLLs. Achieving low quantization noise with conventional TDCs remains a serious bottleneck for the close-in phase noise performance of high-frequency digital PLLs, especially if a wide loop bandwidth is desired. The digital 20GHz PLL described in this chapter uses a noise-shaping TDC that has been proven to overcome this limitation [4]. The TDC architecture implements a two-step approach to time-to-digital conversion (Figure 4.3). The first stage of the TDC is a conventional PFD with charge pump to take advantage of the high accuracy offered by this common analog approach to phase detection. The first TDC stage measures the phase difference between input signal and TDC clock and provides a result in the form of a differential pulse-width-modulated output current signal. The measured phase difference is given in the dc component (or average value) of the signal. The second stage of the TDC is a continuous-time ΔΣ modulator and converts the charge pump current pulses to the digital domain. Since the modulator is clocked by the same signal as the PFD, the TDC has a high oversampling ratio of $f_S/(2f_B)$, where f_S and f_B denote the TDC clock frequency and the TDC bandwidth, respectively. The modulator retains the high accuracy of the first TDC stage by shaping the quantization noise to high frequencies, resulting in low quantization noise in the frequency band of interest $[0, f_B]$. Essentially, the continuous-time modulator extracts the

average value of the analog pulsed-current input, which represents the measure of the phase difference, and then digitizes it while high-pass filtering the quantization noise, thus achieving low TDC noise in the band of interest. The shaped out-of-band noise of the TDC is eventually low-pass filtered by the PLL.

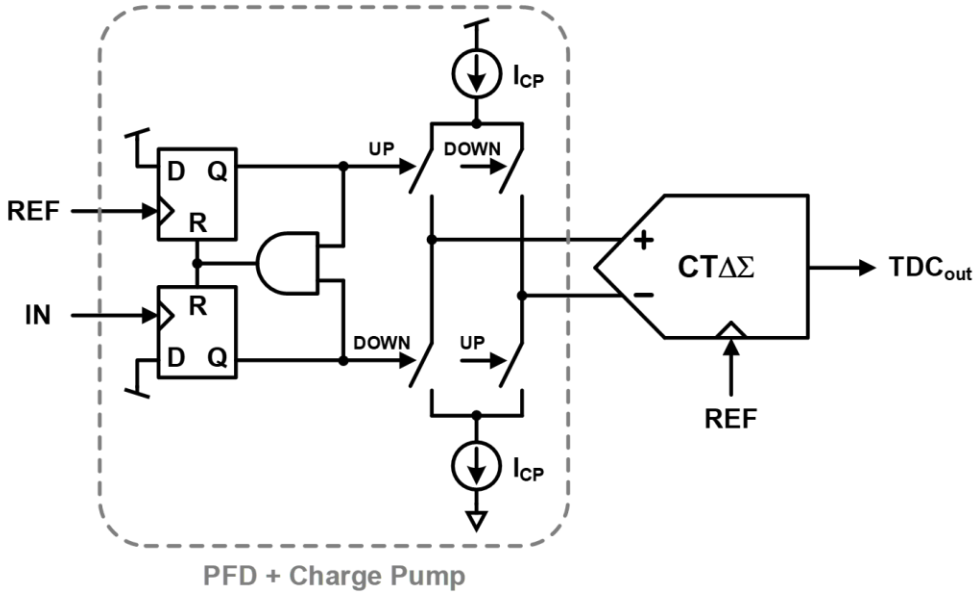


Figure 4.3. Two-step architecture of noise-shaping TDC [4]

A schematic of the continuous-time ΔΣ modulator is shown in Figure 4.4. The modulator is implemented as a 3rd-order modulator to achieve high TDC resolution in the band of interest and to avoid idle tones. A single-bit quantizer digitizes the output of the modulator loop filter. During fractional-N operation of the PLL, the PFD output is zero on average, but can deviate from zero significantly in individual reference cycles. Since a single-bit quantizer is inherently linear, the quantizer helps avoid spurs in the PLL output spectrum and ensures stable loop dynamics. In addition, the ΔΣ modulator is designed as a distributed-feedback architecture to avoid peaking in the signal transfer function, which also improves the spur performance of the PLL.

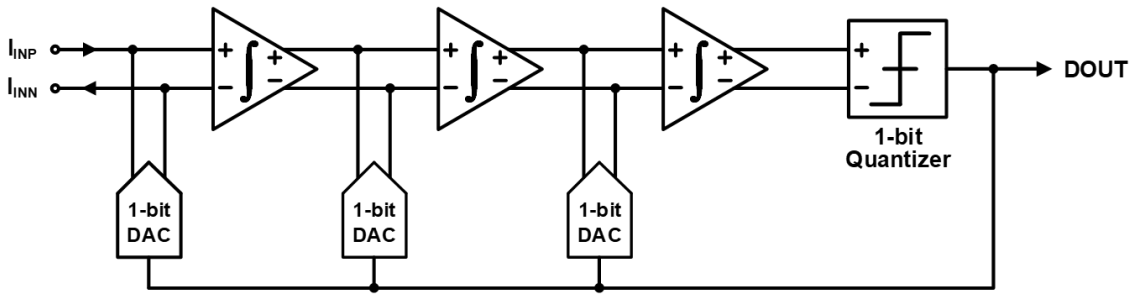


Figure 4.4. Continuous-time 3rd-order feedback architecture of ΔΣ modulator [4]

4.3 Synthesizer Architecture

The 20GHz chirp synthesizer is implemented as a type-II fractional-N PLL [4]. It uses an external 250MHz reference and provides both a 20GHz output and a divided-down 5GHz output. A block schematic of the PLL is shown in Figure 4.5.

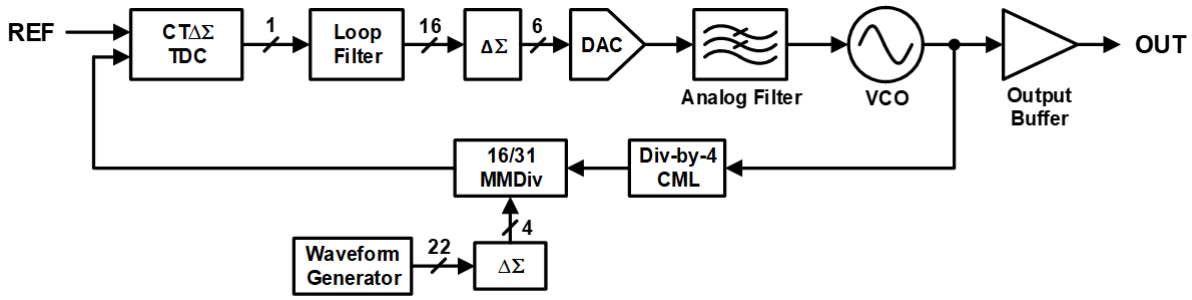


Figure 4.5. Block schematic of the 20GHz chirp synthesizer

The digital loop filter consists of an accumulator and a digital filter stage introducing a pole-zero pair to stabilize the loop. The loop filter parameters (accumulator gain, pole and zero locations) are programmable and allow easy modification of the loop dynamics. In particular, the accumulator gain can be considered a convenient tuning knob to adjust the loop bandwidth. In each reference cycle, the accumulator increases or decreases its value by the accumulator gain, depending on the 1-bit TDC output. The loop filter output is converted to the analog domain by a resistor-ladder digital-to-analog converter (DAC), filtered by a 2nd-order low pass filter and

delivered to the VCO tuning node. The upper and lower DAC reference voltages determine the available voltage range for the VCO tuning range and thereby the available VCO output frequency range and the effective VCO gain. The feedback divider consists of a divide-by-four current-mode logic (CML) stage and a 16-to-31 multi-modulus divider. A 2^{nd}-order $\Delta\Sigma$ modulator with a 22-bit input generates the 4-bit control words for the programmable divider to enable fractional-N operation needed for high frequency resolution. Finally, a programmable on-chip chirp generation logic unit provides the 22-bit control words for the frequency division. To allow reconfigurability with regard to the linearity and bandwidth of the generated chirp profile, the programmable chirp parameters include the number of PLL division ratio steps, i.e. the number of frequency levels, within each of the 25 ramp segments, and the frequency step size between adjacent levels in a ramp segment. Additionally, an internal counter variable sets the update rate of the PLL output frequency, allowing adjustments of the ramp period.

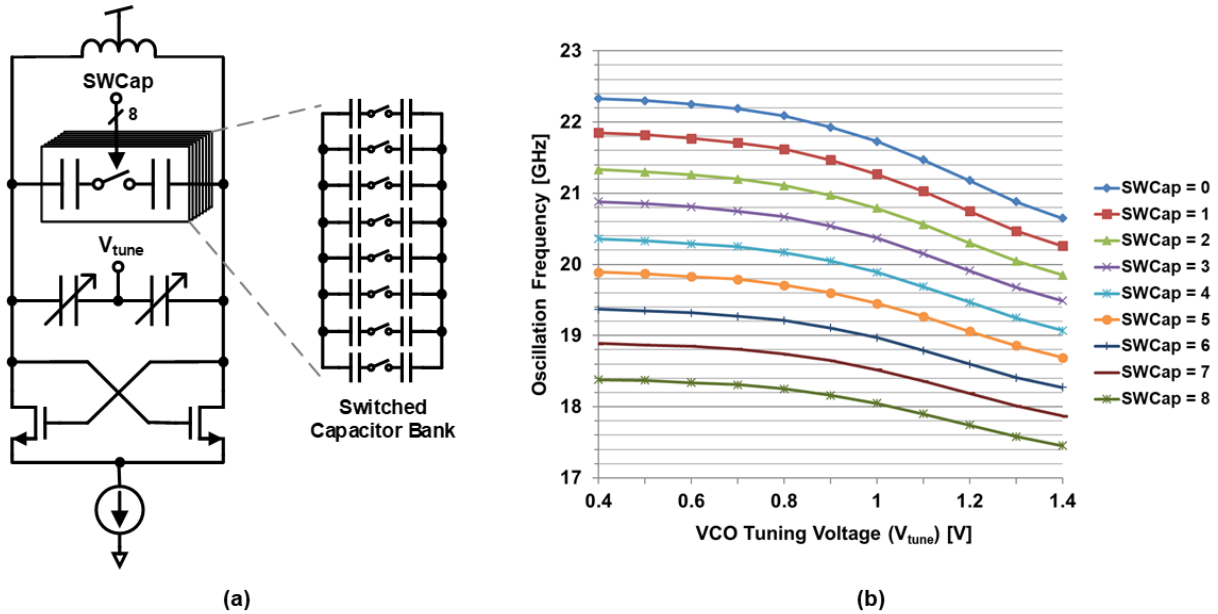


Figure 4.6. VCO schematic (a) and measured frequency tuning characteristic (b)

The VCO circuit schematic is shown in Figure 4.6(a). The VCO operating point is set by the tail current source, and the capacitance in the LC-tank is made up of the varactors and a switched capacitor tuning bank. Fine tuning of the VCO oscillation frequency is accomplished by changing the voltage across the varactors. To cover the wide frequency range required for the MAST radar application, the capacitor bank in the VCO consists of eight switch units for coarse tuning. The individual capacitance values in the switch units are chosen small enough so that the adjacent frequency tuning curves corresponding to different capacitor bank settings overlap and the VCO covers a continuous frequency range from 19.1GHz to 20.4GHz. The measured VCO tuning curves for all possible capacitor bank settings are shown in Figure 4.6(b).

4.4 Measurement Results

The MAST 20GHz chirp synthesizer is fabricated in 65nm CMOS. A die micrograph is shown in Figure 4.7. The die measures 1mm x 1mm and the active area is 0.53mm^2. The fabricated chip is wire-bonded in a 28-pin QFN package and soldered on a PCB suitable for measurements of high-frequency signals. In addition to stand-alone measurements of the synthesizer, the effectiveness of the synthesizer is verified in a test setup that models a complete FMCW radar system.

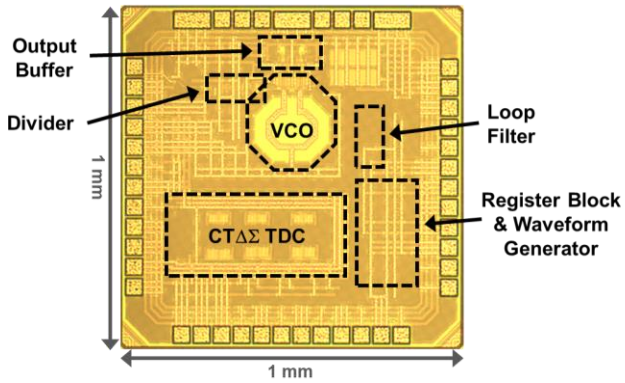
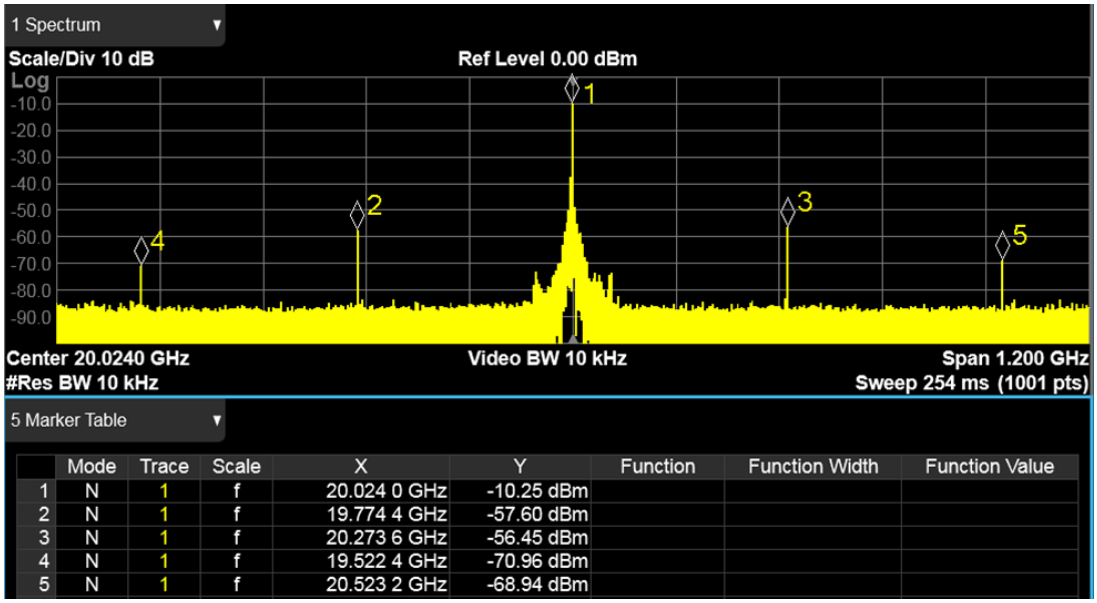


Figure 4.7. Die micrograph of the MAST 20GHz chirp synthesizer prototype

4.4.1 Synthesizer Measurements

All testing is performed using a Keysight N5183A as a reference source and a low-noise reference voltage board to provide the supply and reference voltages. The PLL output spectrum and phase noise are measured with a Keysight N9010A. The synthesizer IC consumes a total power of 39.6mW from a 1.2V supply. The power consumption of the TDC is 8.4mW, while the divider and output buffer combined consume 28.8mW. The remaining power of 2.4mW is consumed by the loop filter and the chirp generation logic. Due to the capacitor banks in the VCO, the PLL offers a wide output frequency range from 17.9GHz to 22.1GHz and thus covers the specified range from 19.1GHz to 20.4GHz. Moreover, the 22-bit resolution of the ΔΣ modulator for the fractional-N divider translates to a fine output frequency resolution of 4kHz. Figure 4.8 shows the output spectrum for a 20.0GHz output. The measured reference spurs are at -45dBc.



	Mode	Trace	Scale	X	Y	Function	Function Width	Function Value
1	N	1	f	20.024 0 GHz	-10.25 dBm			
2	N	1	f	19.774 4 GHz	-57.60 dBm			
3	N	1	f	20.273 6 GHz	-56.45 dBm			
4	N	1	f	19.522 4 GHz	-70.96 dBm			
5	N	1	f	20.523 2 GHz	-68.94 dBm			

Figure 4.8. Measured PLL output spectrum at 20GHz

The synthesizer achieves a low measured close-in phase noise of -88dBc/Hz at 100kHz offset with a wide loop bandwidth (>1MHz) and fast settling (<10μs). The corresponding phase

noise plot is shown in Figure 4.9. Due to the nonlinear VCO gain, which can clearly be seen from the curvature of the tuning curves in Figure 4.6(b), the loop gain of the PLL changes as the PLL output frequency traverses the specified chirp profile. This results in varying phase noise performance and potential loop instability if the loop gain is too high. Therefore, the loop gain is chosen such that optimal performance and stability are ensured across the entire output frequency range from 19.1 GHz to 20.4GHz. In this case, the measured close-in phase noise is -83dBc/Hz at 100kHz offset for a 20.0GHz output.

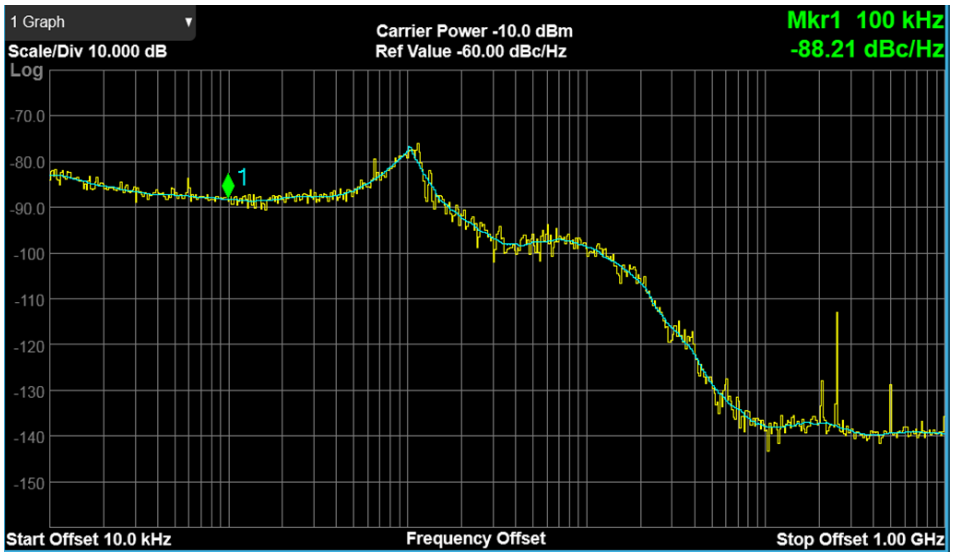


Figure 4.9. Measured phase noise at 20GHz

For the synthesizer to generate the desired frequency chirp consisting of 25 segments and covering a range from 19.166GHz to 20.416GHz, the on-chip chirp generation logic computes and updates the division ratio of the PLL accordingly. It must be reprogrammed upon power-up to guarantee proper chirp generation. Most importantly, a suitable setting for the capacitor tuning bank in the VCO must be assigned to each of the 25 ramp segments so that the PLL can reliably produce the frequency range of the respective ramp segment. As a result, the chirp generation logic changes the capacitor bank setting three times during certain jumps between ramp segments as the

synthesizer output frequency traverses the entire chirp profile. Proper and successful chirp generation can be seen from the measured output spectrum (Figure 4.10). The 25 columns in the spectrum correspond to the 25 ramp segments and the gaps in between indicate the frequency jumps. The chirp generation logic provides two synchronization signals: One goes high upon completion of each ramp segment and the other one goes high upon completion of the entire chirp frame.

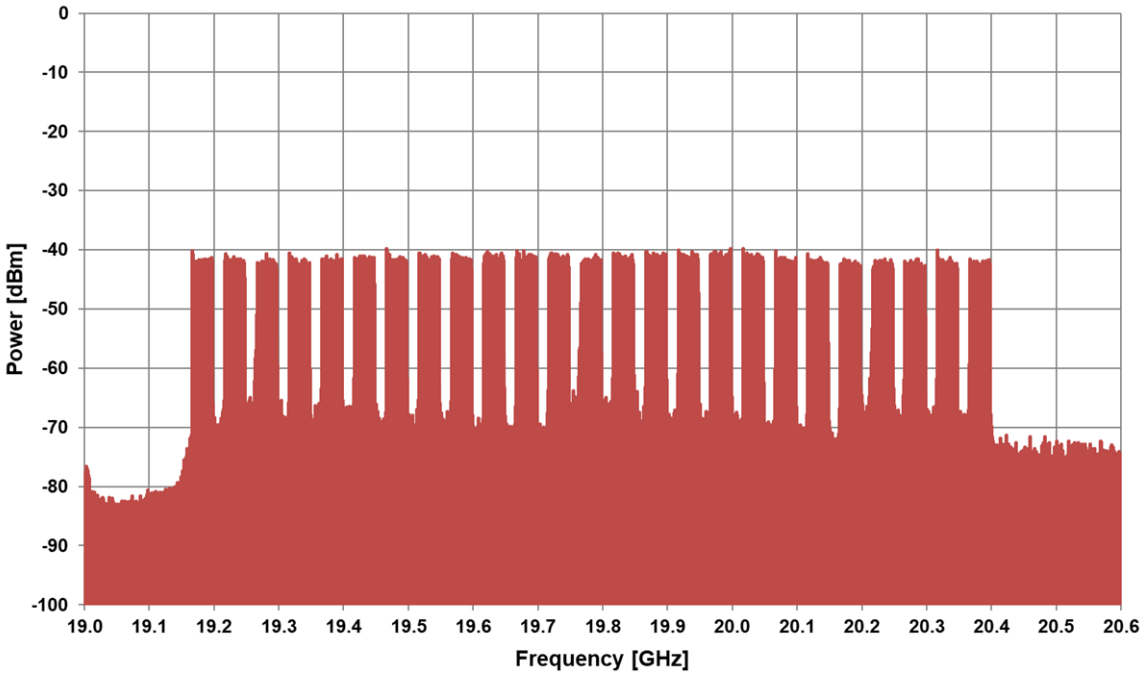


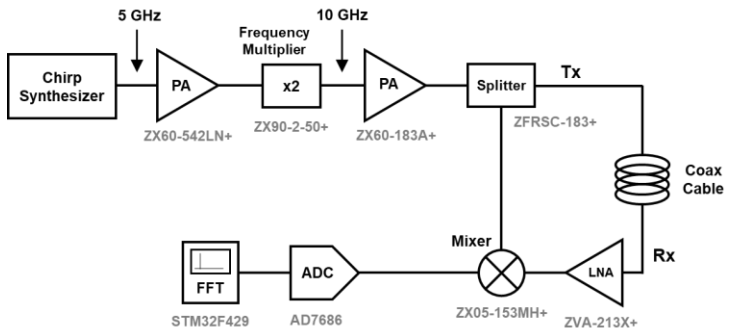
Figure 4.10. Synthesizer output spectrum showing 25-segment chirp

4.4.2 Radar Testbed

In addition to the stand-alone measurements described above, the synthesizer IC is used to drive a complete end-to-end radar testbed[3] that serves as an experimental test setup to verify the effectiveness of the synthesizer design in an FMCW radar system. The testbed generates a 10GHz

[3] The testbed setup and result analysis were contributed to by Lu Jie. He selected and configured the components for the digital baseband processing (ADC, microcontroller).

sawtooth chirp profile and models a complete radar transceiver including chirp synthesizer, transmitter chain, transmission channel, receiver and digital baseband processing. The 5GHz divided-down output of the synthesizer IC serves as the signal source of the testbed and commercially available, discrete components implement the transmitter and receiver chains as well as the DSP back-end. A block schematic of the testbed is shown in Figure 4.11 and pictures of the actual setup are shown in Figure 4.12.



PA (ZX60-542LN+)	24 dB Gain
Doubler (ZX90-2-50+)	12 dB Conv. Loss
PA (ZX60-183A+)	29dB Gain
Splitter (ZFRSC-183+)	6 dB Total Loss
LNA (ZVA-213+)	26 dB Gain 3.0 dB NF
Mixer (ZX05-153MH+)	8.5 dB Conv. Loss

Figure 4.11. Block schematic of the radar testbed and component performance data

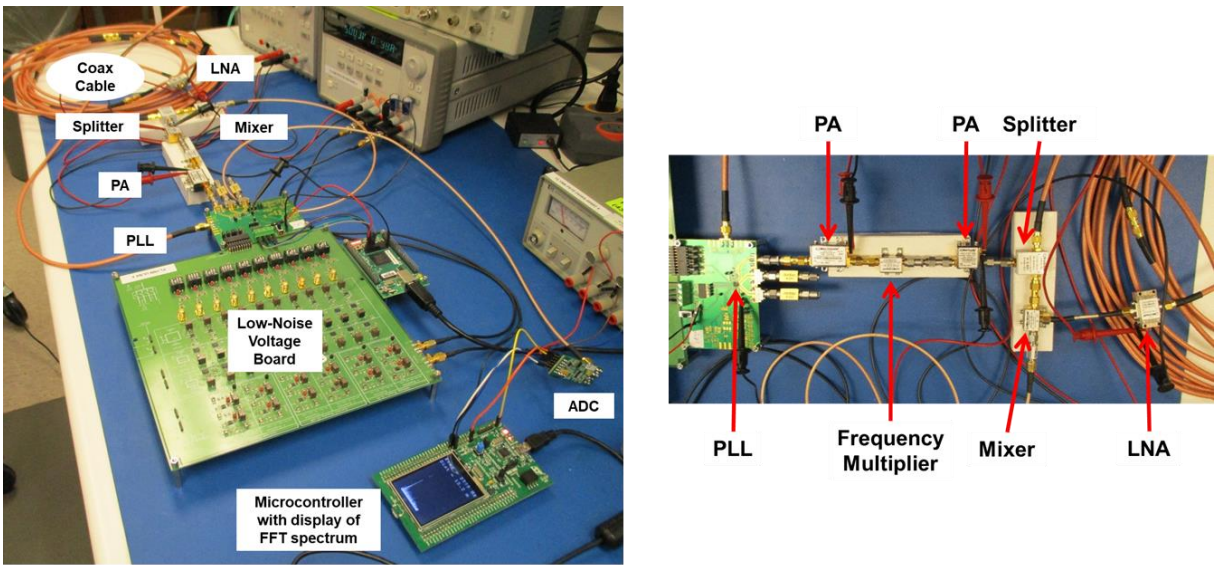


Figure 4.12. Radar testbed (a) and close-up view of the transmit and receive paths (b)

The transmitter chain comprises two power amplifiers, a frequency multiplier and a splitter to amplify the synthesizer output signal, double its frequency to 10GHz and provide it to the mixer and transmission channel. The latter is realized by a long coaxial cable to model the propagation delay of the radar signal on its path to the target and back. MiniCircuits components are used to implement the transmitter chain and receiver front-end. An overview of their performance characteristics at 10GHz is included in Figure 4.11. Moreover, the baseband signal is digitized by an AD7686 from Analog Devices. It features a sample rate of 500kSps and 16-bit nominal resolution. Finally, the testbed uses an STM32F429I Discovery Board from STMicroelectronics for FFT processing, range calculation and result display. The STM32F429 microcontroller can provide FFT results in real-time, and the FFT and range results can be readily displayed on the LCD interface of the board.

As a case study, the synthesizer is configured to generate a sawtooth chirp with a bandwidth of 200MHz, a period of 2.7ms and 12-bit linearity. The power spectrum of the chirp is shown in Figure 4.13. The recorded baseband signal at the output of the mixer reveals proper operation of the testbed (Figure 4.14).

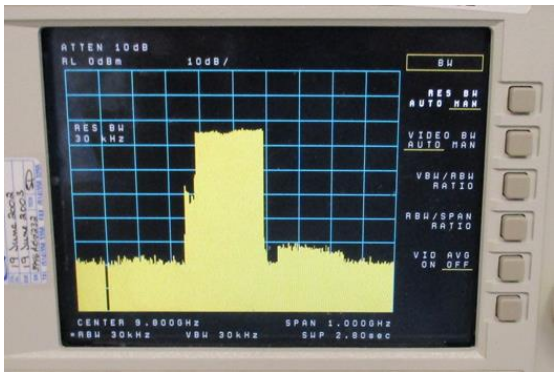


Figure 4.13. Chirp spectrum for radar testbed

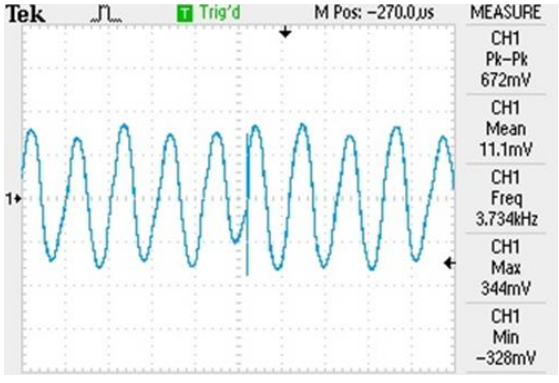


Figure 4.14. Baseband signal at mixer output

The microcontroller is programmed to acquire a series of 256 samples from the ADC over 2.7ms, which is equal to the chirp period. It computes the FFT and finds the maximum frequency

bin. The FFT spectrum is then fitted to a sinc function around this bin and a more accurate beat frequency is determined through interpolation to improve the range resolution [31]. Based on the given chirp parameters, the controller calculates the target range that would result in the same signal delay as provided by the coaxial cable in the testbed. FFT spectrum, detected beat frequency and calculated range can be observed on the LCD display of the controller (Figure 4.15). After the data sampling period of 2.7ms, the data processing takes about 2.5ms. Therefore, the described algorithm is repeated about every 5ms. During this process, LCD display refresh and data transmission occur in parallel. The implemented algorithm is verified by comparing the detected beat frequency with the signal frequency at the output of the mixer.

Figure 4.15. Microcontroller display showing beat frequency, range and FFT spectrum

The results obtained from the radar testbed confirm the effectiveness of the implemented radar configuration. In particular, if the length of the coaxial cable between the transmitter and the receiver is changed to model the effect of different propagation delays of the radar signal, the displayed beat frequency and range update as expected and correctly reflect the changes in the propagation delay. The 20GHz chirp synthesizer can successfully drive a radar system to provide reliable results, showing that the described PLL design can effectively be applied in an FMCW radar.

4.5 Conclusion

A 20GHz chirp synthesizer PLL is designed to be used as a signal source for a 240GHz FMCW radar application. The specifications of the application require the synthesizer to generate a sawtooth chirp consisting of 25 continuous chirp segments with frequency jumps between the segments. To meet the settling speed and phase noise requirements, the synthesizer is implemented as a digital fractional-N PLL using a 3^{rd}-order noise-shaping TDC. The TDC architecture uses a conventional PFD with charge pump to enable high-accuracy phase detection and leverages the noise-shaping characteristic of a continuous-time $\Delta\Sigma$ modulator to convert the phase information to the digital domain while retaining the high accuracy of its analog phase detector front-end. Due to the low TDC noise at low frequencies, the PLL achieves low close-in phase noise with wide loop bandwidths. The synthesizer design incorporates on-chip chirp generation logic that modulates the division ratio of the PLL to produce the specified chirp profile. The synthesizer IC is fabricated in 65nm CMOS, consumes 39.6mW and covers a wide frequency range from 17.9GHz to 22.1GHz. The measured close-in phase noise is -88dBc/Hz at 100kHz offset for a wide loop bandwidth (>1MHz). Experiments with a radar testbed that models a complete FMCW radar show that the chirp synthesizer IC can effectively drive an FMCW radar system.

CHAPTER 5 A 38GHz Digital Fractional-N FMCW Chirp Synthesizer PLL with a Continuous-Time Bandpass ΔΣ TDC

While conventional TDCs rely on gate delays for time discretization, the noise-shaping TDC in the synthesizer presented in the previous chapter is based on a conventional analog phase detection technique – a PFD with charge pump – and combines it with a ΔΣ modulator to convert the phase information to the digital domain. Similarly, the design approach presented in [34] uses a successive-approximation-register (SAR) ADC to digitize the output of a charge pump. Both approaches leverage the high resolution offered by the respective data converter types to achieve high TDC resolution, but depend on an analog-intensive phase detector design to precede the data converter. As a promising and more direct approach to ADC-based time-to-digital conversion, digital PLL architectures can be designed to use an ADC that samples the edges of a signal and directly digitizes the phase information in the voltage-domain.

This chapter introduces a noise-shaping TDC that uses a continuous-time bandpass ΔΣ modulator to capture and digitize the phase difference between the reference and feedback signals of a PLL. This bandpass ΔΣ TDC leverages the noise-shaping characteristic of the bandpass ΔΣ modulator and combines the modulator with a digital down-conversion scheme to achieve low noise in the frequency band of interest. A 38GHz digital fractional-N synthesizer PLL for FMCW radar based on this TDC is presented. The PLL is fabricated in 40nm CMOS and measurements of a prototype IC demonstrate that the bandpass ΔΣ TDC enables low close-in phase noise in a wide-bandwidth high-frequency digital PLL.

5.1 ADC-based Time-to-Digital Conversion in PLLs

The basic principle of ADC-based time-to-digital conversion is to capture the time difference between two signals in the voltage-domain and digitize the time information with an ADC. The time-to-voltage conversion step, which is accomplished by a sampling operation, assumes relatively slow signal edges of the sampled signal so that the voltage samples accurately represent the time difference between sampled and sampling signal. The application of this principle is demonstrated in digital PLL implementations such as [35] and [36], which are both sub-sampling PLLs. In [35], a buffer turns the DCO output waveform into charging and discharging waveforms characteristic of an RC unit, and the ADC sub-samples the buffered version of the DCO output. In contrast, the ADC-based TDC in [36] sub-samples the DCO output using a bootstrap sample-and-hold circuit, and takes advantage of the inherent linearity of the sinusoidal DCO output waveform near its zero crossings to achieve high TDC linearity. A simplified block schematic of the PLL in [36] including reference and output frequencies as well as an illustration of the conversion principle are shown in Figure 5.1.

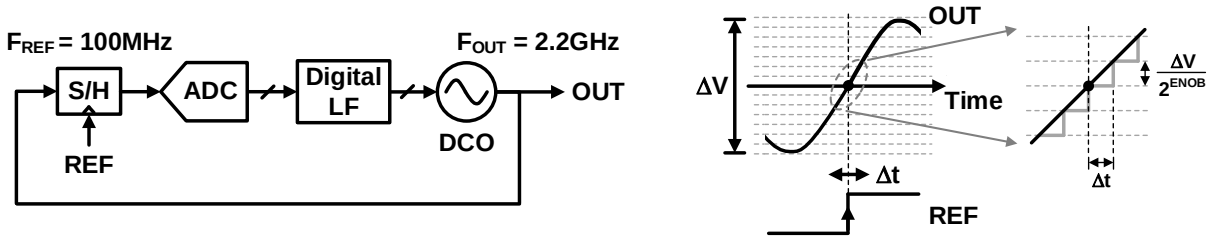


Figure 5.1. Digital sub-sampling PLL with ADC-based TDC [36] and conversion principle of an ADC-based TDC

The rising edges of the reference clock coincide with zero crossings of the DCO output if this sub-sampling PLL is locked. The time resolution of the ADC-based TDC can be estimated by a linear approximation of the sinusoidal DCO waveform at the zero crossing. If the sinusoid is assumed to cover the full input range of the ADC, the voltage-domain can be divided into small

discrete intervals of $\Delta V = 2A/2^{ENOB}$, where A is the amplitude of the sinusoid and $ENOB$ is the effective number of bits of the ADC. The slope of the linear approximation at the zero crossing is a function of the amplitude of the sinusoid as well as its frequency, subsequently denoted as the TDC input frequency f_{in}, and can be calculated as $m = 2\pi f_{in} A$. Since the discrete voltage intervals ΔV correspond to discrete steps Δt in the time-domain, the effective time resolution of the ADC-based TDC is given as

$$\Delta t_{res,TDC} = \frac{\Delta V}{m} = \frac{1}{\pi \cdot f_{in} \cdot 2^{ENOB}} \tag{5.1}$$

As intuitively expected, the TDC resolution increases with the ADC resolution. Additionally, the presence of f_{in} in the denominator indicates that a steeper slope of the input edges improves the TDC resolution as well. This effect is exploited in [36], where a voltage amplifier is placed between the sample-and-hold circuit and the ADC to enhance the resolution.

The above observations show that an ADC-based TDC is a promising approach to achieve high time resolution with good linearity. However, the approaches in [35] and [36] are restricted to lower RF frequencies and not practical for mm-wave PLLs because of the very high sampling speed that would be necessary to track a high-frequency DCO output waveform.

5.2 PLL Reference Sampling and Phase Digitization

Instead of sampling the DCO output, a high-frequency digital PLL can incorporate ADC-based time-to-digital conversion in the fashion shown in Figure 5.2. This digital PLL architecture includes a feedback divider to divide the DCO output frequency down to the reference frequency. The shown approach assumes a sinusoidal reference waveform, which is a low-frequency signal and can easily be sampled by an ADC. The PLL feedback signal clocks the ADC, i.e. it triggers

the sampling and digitization of the reference signal in the ADC. Since the reference and feedback have equal frequency if the PLL is locked, the digital output of the ADC is a measure of the phase alignment (or time difference) between the two signals.

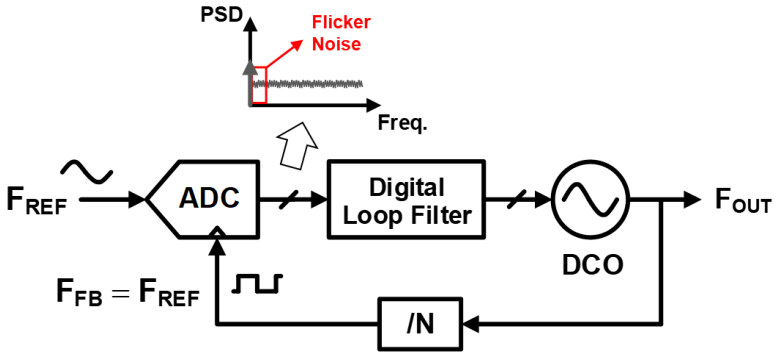


Figure 5.2. Digital PLL with reference-sampling ADC

5.2.1 Shortcomings of Direct ADC-based Phase Digitization

Although the approach in Figure 5.2 works in principle, it has a few shortcomings and drawbacks. First, this type of ADC-based TDC relies on implicit down-conversion to provide a digital dc output representing the measured phase difference. The dc value at the ADC output is a result of the reference signal being sampled by a clock signal (the PLL feedback signal) of equal frequency. This causes noise sources close to dc, primarily flicker noise, to appear in the band of interest near dc at the TDC output and interfere with the phase-difference measurement. Phase detection techniques in conventional analog and digital PLLs equally rely on implicit down-conversion and their performance is therefore affected by low-frequency noise as well.

Second, the ADC must have a large bandwidth extending beyond the reference frequency so that it is fast enough to track the edges of the reference sinusoid. Frequencies of a few hundred megahertz are not uncommon for references of high-frequency PLLs. The large ADC bandwidths

required in these cases make it almost prohibitive to employ a conventional Nyquist-type ADC for direct phase digitization.

Third, the useful phase detection range of the ADC-based TDC in Figure 5.2 is only $\pm\pi/2$, which can be seen from the waveform in Figure 5.1. The phase detection characteristic corresponds to the sine waveform and is monotonic only if the phase difference between reference and feedback is within $\pi/2$. Therefore, the reference-sampling ADC-based TDC cannot serve as a frequency detector and its narrow phase detection range makes an additional loop for frequency acquisition indispensable to ensure PLL locking upon start-up.

5.2.2 Reference Digitization with Digital Down-Conversion

The TDC architecture presented in this chapter avoids low-frequency noise contamination of the phase measurement and offers an extended phase detection range by digitizing a sinusoidal reference at a rate that is an integer multiple of the reference frequency before down-converting it in the digital domain. This principle is illustrated in Figure 5.3. Instead of relying on implicit down-conversion to output a dc value, the ADC treats the sinusoidal reference as an analog signal and samples it at four times the reference frequency. The ADC output is a digitized version of the reference which holds the information about the phase alignment between reference and feedback. The frequency ratio is chosen to be four because this greatly simplifies the implementation of the digital down-conversion (DDC). The digital version of a sine sampled four times per period can be represented by the sequence (+1,0,-1,0) and thus the ADC output is digitally down-converted by simply periodically multiplying the output bitstream by a (+1,0,-1,0) sequence. At the same time, DDC upconverts low-frequency noise present in the ADC output. Therefore, flicker noise

does not appear in the band of interest near dc at the TDC output and does not affect the accuracy of the phase measurement.

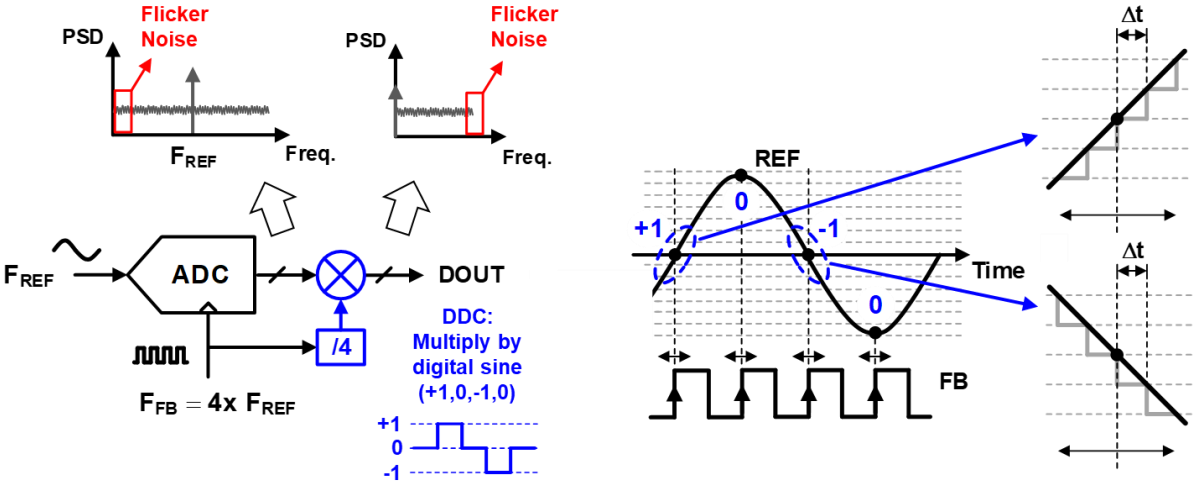


Figure 5.3. ADC-based TDC with digital down-conversion

As suggested by the reference and feedback waveforms in Figure 5.3, the feedback edges coincide with the zero crossings and peak values of the reference sinusoid when the PLL is locked with $F_{FB} = 4 \times F_{REF}$. DDC retains the samples at the zero crossings by multiplying by ±1, while discarding the samples at the peak values. As a result, the shown ADC-based TDC with DDC has an effective sample rate of twice the reference rate.

Figure 5.4 compares the phase transfer characteristic of the ADC-based TDC with DDC with those of a conventional PFD and an ADC sampling a sinusoidal reference at reference rate. While the ADC-based TDC with DDC has a limited phase detection range and cannot be used as a frequency detector, the fact that its sampling rate is four times the reference frequency results in a useful phase detection range of ±2π of the feedback phase, as opposed to ±π/2 with a simple reference-sampling ADC. For this reason, the 38GHz chirp synthesizer PLL described later in this chapter exhibits robust locking behavior and does not require an additional loop for frequency acquisition.

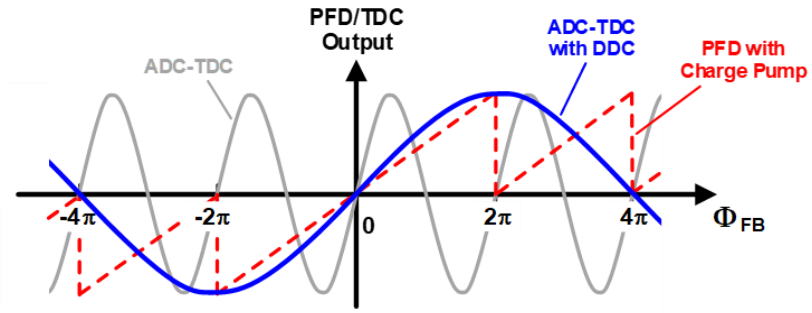


Figure 5.4. Comparison of PFD/TDC phase transfer characteristics

One design challenge that is not relaxed by DDC is the required ADC bandwidth. If compared to a simple reference-sampling ADC, the ADC-based TDC with DDC is advantageous in terms of low-frequency noise and phase detection range, but the ADC bandwidth must still extend beyond the reference frequency so that the ADC can track the reference waveform. At this point, it must be noted that the above discussions assume a Nyquist-type ADC, which is also suggested by the flat quantization noise spectra in Figure 5.2 and Figure 5.3. However, for an ADC-based TDC with DDC to achieve low output noise in the band of interest near dc, the quantization noise of the ADC does not have to be low across the whole spectrum as shown in Figure 5.3, but only in a frequency band around the reference frequency. Efficient use of the data converter bandwidth is possible if the data converter exhibits low quantization noise in a limited band around a center frequency. An established data conversion technique that provides this type of quantization noise characteristic is bandpass ΔΣ modulation, making it obvious and appealing to employ a bandpass ΔΣ modulator (BPDSM) in an ADC-based TDC with DDC. The following section provides a brief review of bandpass ΔΣ modulation.

5.3 Continuous-Time Bandpass ΔΣ Modulation

ΔΣ modulators take advantage of the principles of oversampling and noise-shaping to achieve high resolution in a specified frequency band, typically at low frequencies near dc. They are most commonly implemented as feedback topologies with a loop filter and a low-resolution quantizer in the forward path, and a DAC feedback network. Due to the feedback, the quantizer produces a bitstream that drives the loop filter input to zero. As a result of this digitization scheme, the average of the modulator output bitstream matches the analog input while, unlike with Nyquist-rate ADCs, there is no one-to-one correspondence between input and output values. A ΔΣ modulator oversamples its input with a certain oversampling ratio (OSR), which is defined as $f_S/(2f_B)$, where f_S and f_B denote the sampling rate and modulator bandwidth, respectively. Since f_S is much larger than the Nyquist sampling rate of $2f_B$, the quantization noise of the modulator is spread over a wider frequency spectrum, thus increasing the signal-to-noise ratio in the band of interest. The loop filter of the modulator determines the transfer characteristics, which are mathematically described by the signal transfer function (STF) and the noise transfer function (NTF). Most ΔΣ modulators are designed to have a low-pass characteristic, meaning that the STF passes low frequencies whereas the NTF is high-pass. In these cases, the quantization noise is shaped to high frequencies and suppressed at low frequencies, resulting in high resolution in a frequency band near dc.

In contrast to a low-pass ΔΣ modulator, a BPDSM does not achieve high resolution in a band near dc, but in a narrow band of width f_B around a center frequency f_0. A continuous-time single-loop feedback architecture of a BPDSM along with a general output spectrum is shown in Figure 5.5. The loop filter of a BPDSM uses a resonator circuit, which has a passband characteristic with a center frequency f_0. The resulting STF and NTF are described by a passband and a stopband

transfer function, respectively. A BPDSM achieves high resolution in the narrow center band by oversampling the center bandwidth and shaping the quantization noise out of band to low and high frequencies. It still offers a high OSR because f_S is much larger that f_B, but f_0 is a considerable fraction of f_S. Typically, $f_0 = f_S/4$, as is also the case in this work. BPDSMs are attractive for RF receiver systems as they can be used for IF digitization in direct conversion receivers to simplify the receiver architecture, and increasing center frequencies make BPDSMs suitable as receivers by themselves [37]. In this work, a BPDSM is used in a TDC to digitize a sinusoidal PLL reference and measure the phase difference between modulator input and clock signal because it allows efficient use of its bandwidth.

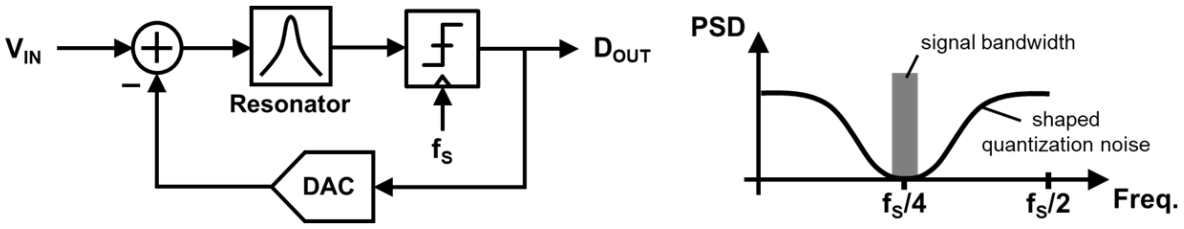


Figure 5.5. Continuous-time bandpass ΔΣ modulator and output spectrum

For the bandpass ΔΣ TDC presented in this chapter, a continuous-time BPDSM implementation is chosen as it brings an additional feature desirable for this application. While the sampling operation in discrete-time ΔΣ modulators occurs at the modulator input, continuous-time ΔΣ modulators have a continuous-time loop filter and the sampling occurs at the quantizer. The input signal first passes the loop filter, which acts as an anti-aliasing filter, suppressing out-of-band frequency components. This inherent anti-aliasing filtering is beneficial to the TDC because the BPDSM removes potential distortion present in the PLL reference waveform, which is assumed to be a pure tone.

5.4 Bandpass ΔΣ TDC

Replacing the generic Nyquist-type ADC in the ADC-based TDC from Figure 5.3 with a BPDSM results in the proposed bandpass ΔΣ TDC (BPDSTDC) (Figure 5.6). This TDC is the key component in the digital synthesizer architecture described in the following section. The PLL reference frequency assumes the role of the BPDSM center frequency. To measure the phase difference between reference and feedback signals, the PLL feedback clocks the BPDSTDC at four times the reference frequency ($F_{FB} = 4{\times}F_{REF}$). Not only does this design choice simplify the implementation of the DDC, but it also results in the very common frequency ratio $f_0 = f_S/4$ for the BPDSM.

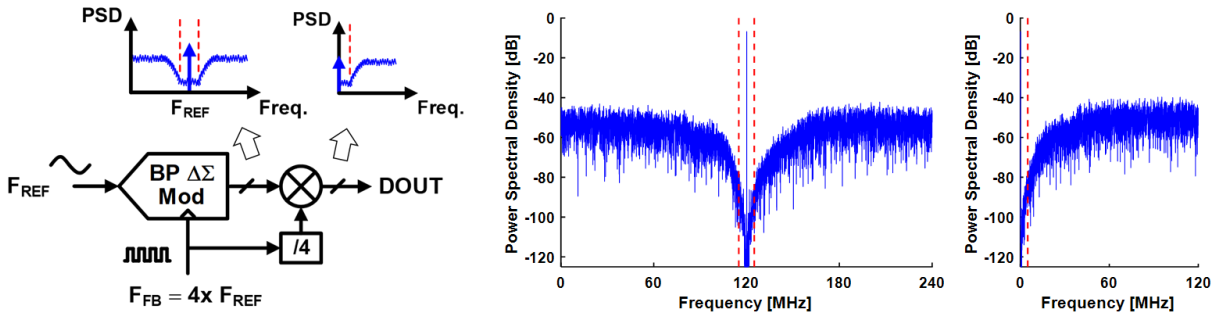


Figure 5.6. Bandpass ΔΣ TDC and simulated noise spectra before and after digital down-conversion

For $F_{FB} = 4{\times}F_{REF}$, the BPDSM output is a digitized version of the sinusoidal reference and contains the phase difference information. The output spectrum shows low quantization noise in a two-sided band around the reference frequency and increased noise elsewhere. DDC down-converts the reference frequency component to dc, giving the desired phase information at the BPDSTDC output. At the same time, DDC transforms this noise spectrum to that one of a low-pass ΔΣ modulator, i.e. low quantization noise in a band near dc and increased noise at high frequencies. The BPDSTDC therefore achieves high resolution in the band of interest near dc. Its increased out-of-band noise is eventually filtered out by the low-pass characteristic of the PLL.

Figure 5.6 also shows the simulated output spectra before and after DDC obtained from a model of the BPDSM implementation used in this work. Since the two-sided BPDSM band translates to a BPDSTDC band of half that width near dc, the required passband bandwidth of the BPDSM needs to be only twice the targeted PLL bandwidth. This again emphasizes the fact that the BPDSTDC makes efficient use of the narrow bandwidth of a BPDSM.

5.5 Synthesizer Architecture

The proposed BPDSTDC is used in a 38GHz fractional-N PLL for FMCW chirp synthesis. A block schematic of the 38GHz synthesizer is shown in Figure 5.7. The BPDSTDC uses the feedback signal to sample a sinusoidal 120MHz reference and the PLL locks with a feedback frequency of 480MHz. The TDC measures and digitizes the phase difference between reference and feedback signals while shaping the quantization noise to higher frequencies, and produces a 5-level digital output stream. The BPDSM in the TDC has a bandwidth of 5MHz around the center frequency of 120MHz, which translates to a TDC bandwidth of 2.5MHz. This provides sufficient margin for PLL bandwidths >1MHz.

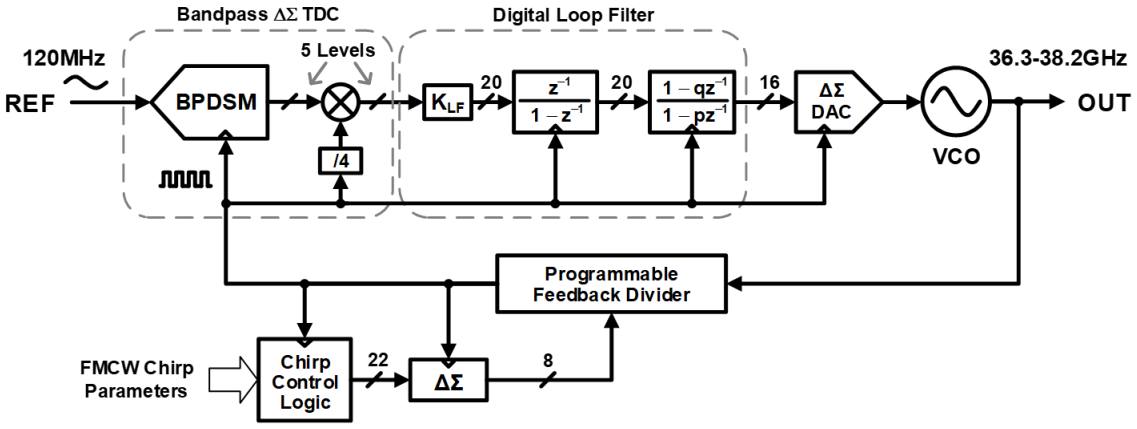


Figure 5.7. Block schematic of the 38GHz chirp synthesizer

The TDC output feeds to the digital loop filter of the PLL, which incorporates a digital accumulator to implement a type-II PLL. In each update cycle, the accumulator multiplies its gain K_{LF} by the TDC output value (-2,-1,0,+1,+2) and adds it to the previous accumulator value. K_{LF} represents the loop filter gain and serves as a convenient tuning knob to adjust the PLL bandwidth. In this work, K_{LF} is chosen such that loop stability is ensured with a small phase margin to obtain high PLL agility for chirp generation. The digital filter that follows the accumulator introduces a zero at 170kHz and a pole at 3.8MHz to stabilize the loop.

A 1st-order ΔΣ DAC converts the loop filter output to the analog domain and provides it to the tuning node of the VCO. The DAC consists of a 1st-order digital ΔΣ modulator to reduce the data bit width from 16 bit to 6 bit, and a 6-bit resistor-ladder DAC. The reference voltages of the resistor ladder are used to adjust the available VCO output frequency range and the effective VCO gain. In addition, two RC-filter units with cutoff frequencies at 12 MHz smooth the DAC output and filter the shaped noise of the 1st-order modulator. The analog 2nd-order filter in the DAC combines with the low-pass characteristic of the accumulator in the digital loop filter to provide sufficient suppression of the 2nd-order-shaped TDC quantization noise.

Due to the absence of an external reference having a frequency equal to the effective TDC rate of $2\times F_{REF}$, the PLL feedback signal does not only clock the BPDSTDC, but it is also used to clock the digital filter and the ΔΣ DAC. As is the case with the DDC, the operation of the loop filter and the DAC is not compromised by the jitter and ΔΣ divider noise present in the feedback clock. The timing variation of the clock edges is taken into account as clock uncertainty during digital synthesis. Technically, the loop filter and ΔΣ DAC should be clocked at $2\times F_{REF}$, which is the effective TDC rate. A clock at $2\times F_{REF}$ can easily be provided by dividing the PLL feedback signal by two. In this case, the loop filter processes only those TDC output values that are not

automatically zero due to the DDC. In other words, the digital loop filter considers only those output words of the BPDSM that are multiplied by +1 or -1 by the DDC. However, it is desirable to update the VCO tuning voltage as often as possible for best PLL phase noise performance. Therefore, the loop filter and the ΔΣ DAC are clocked at the full rate of $4\times F_{REF}$, even though every other input to the loop filter is zero. This approach is verified during testing of the prototype by switching the clock rate of the loop filter between $2\times F_{REF}$ and $4\times F_{REF}$.

A design challenge arises from the fact that the BPDSTDC is used in a fractional-N PLL. The feedback signal of the PLL serves as the BPDSTDC clock, but also carries the fractional-N ΔΣ quantization noise. Phase noise simulations of the PLL suggest that the output spectrum of the BPDSM convolves with the ΔΣ noise of the fractional-N divider – an event that is independent of the data converter type in the TDC, but due to the TDC treating the reference as an analog signal and sampling it at $4\times F_{REF}$. As a result, the ΔΣ divider noise may determine and limit the close-in phase noise of the PLL if it is too high, making a fine TDC resolution ineffective. Two measures are taken in the PLL design to avoid this: First, a 2nd-order ΔΣ modulator having an NTF with a maximum out-of-band gain of only 1.2 controls the fractional-N division. This reduces the maximum ΔΣ noise level, limiting the number of possible modulator outputs to only two for most input words. Second, and more importantly, a programmable feedback divider that implements divider ratios with a small step size of 1/4 reduces the fractional-N quantization noise, as illustrated in Figure 5.8. Simulations with very high TDC resolution show that each doubling of the divider ratio resolution improves the close-in phase noise of the PLL by 6dB. For the expected noise performance of the BPDSTDC, a divider ratio step size of 1/4 proves to lower the fractional-N ΔΣ noise by a sufficient amount. The following section describes the architecture and operation of the feedback divider in detail.

Finally, on-chip chirp control logic completes the synthesizer architecture. It produces the input words for the 2nd-order ΔΣ modulator to modulate the PLL division ratio and generate the desired triangular FMCW chirp profile.

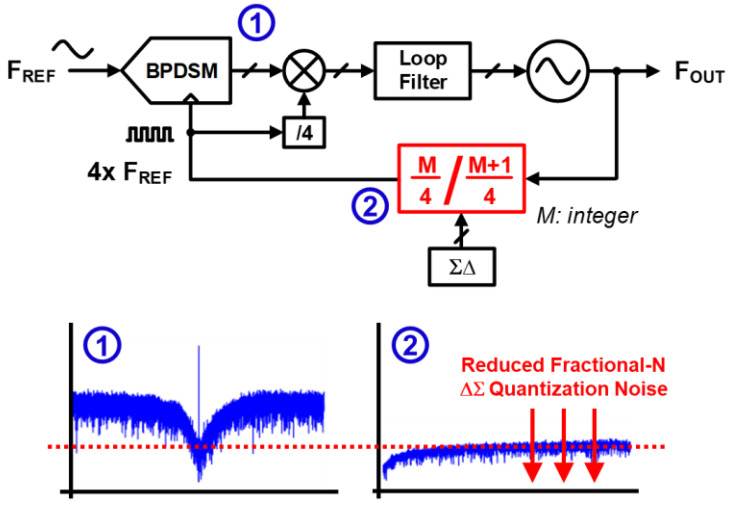


Figure 5.8. Reduced fractional-N ΔΣ quantization noise due to divider ratio step size of 1/4

5.6 Feedback Divider Design

The feedback divider of the PLL makes use of phase interpolation and a phase switching (or phase rotation) scheme to enable programmable division with fine divider ratio steps of 1/4. The basic principle of phase rotation is to have several phases available and to switch a different phase to the divider output in each divider cycle. In this design, the selected phase lags the previous output phase so that the next signal edge at the divider output is delayed after the phase rotation step. This way, different effective divider ratios are emulated, which depend on the size of the phase steps.

A block diagram of the divider architecture is shown in Figure 5.9. A high-speed current-mode logic (CML) pre-scaler consisting of two divide-by-two stages divides the VCO output down to a frequency that is manageable for CMOS logic. Since the CML divider stages are differential

and implemented with two latches, each stage generates four phases from two input phases. Due to the high power consumption of CML, only two CML divider stages are used and the four output phases of the second stage are tapped, giving four phases after division by four. Next, two differential CML-to-CMOS converters amplify the signal swings to CMOS levels. A divide-by-two CMOS divider stage consisting of two parallel divider stages provides eight output phases. Resetting the CMOS divider latches ensures the correct sequence of the output phases.

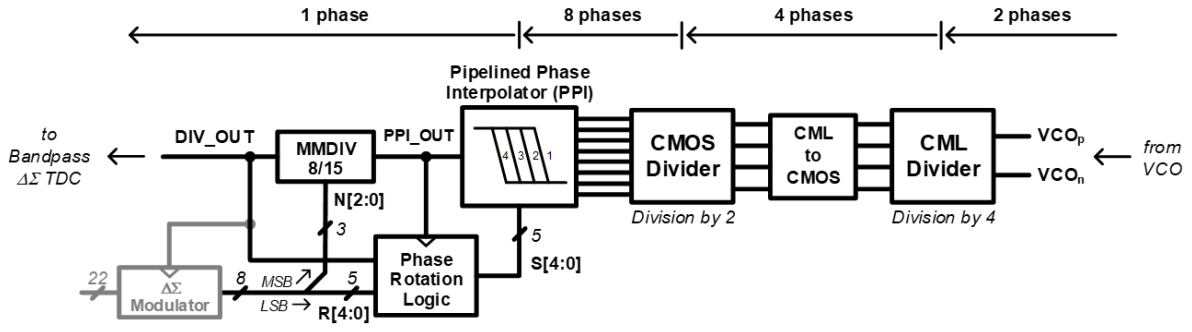


Figure 5.9. Feedback divider architecture

Since eight phases are available after division by eight, phase rotation at this point would emulate division ratios with a step size of one. For this reason, phase interpolation is applied to quadruple the number of available phases to 32. After division by eight, this results in the desired divider resolution of 8/32 = 1/4. The placement of the pipelined phase interpolator (PPI) at this point in the divider chain is a compromise between PPI design complexity (number of input phases) and PPI operating speed (signal frequency of PPI input). An 8-to-15 multi-modulus divider (MMDIV) follows the PPI to divide the PPI output frequency down to $4\times F_{REF}$. Since the BPDSM design in the TDC assumes a 50%-duty-cycle clock, additional logic is included in the MMDIV to ensure a 50%-duty-cycle divider output.

The phase switching in the PPI is controlled by the output variable *S[4:0]* of the phase rotation logic. The implementation of the phase rotation logic is shown in Figure 5.10. The input

word *R[4:0]* specifies the size of the phase rotation step performed in each divider cycle. Since the PPI is followed by another divider stage, the MMDIV, the phase rotation logic is designed to observe *DIV_OUT* and perform only one complete phase rotation step per divider output cycle. This ensures that the divider resolution of 1/4 is retained for the entire divider chain. Moreover, the logic breaks a phase rotation step down into several (up to four) smaller steps to avoid large single phase steps in the PPI that would result in additional edges at the MMDIV input and an incorrect total division ratio. Based on *R[4:0]*, a decoder provides four phase step addends (*PSA_1*, *PSA_2*, *PSA_3*, *PSA_4*) that specify the sizes of the four individual phase steps, according to the truth table given in Table 5-1. To further ensure a duty cycle of (or at least close to) 50% in *DIV_OUT*, the phase rotation logic splits the four steps equally between the high and low sections of *DIV_OUT*. The counter variable *SEL[1:0]* controls the selection of the phase step addend to be added to *S[4:0]* and enables the addition at the desired instants as well as the decoding of the addends. The timing diagram in Figure 5.11 illustrates the operation of the phase rotation logic with the instants of the phase steps highlighted for a complete divider output cycle. As an example, Figure 5.12 shows a phase rotation scenario for a total division ratio of 78 of the feedback divider.

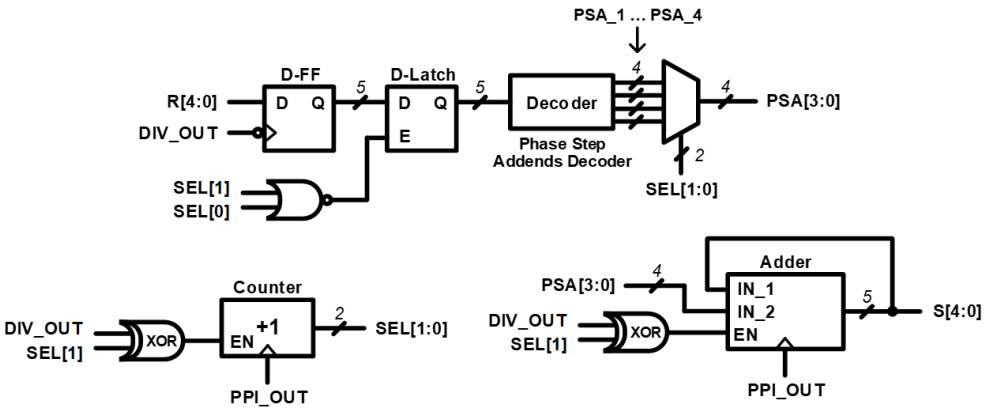


Figure 5.10. Implementation of the phase rotation logic

R[4:0]	*PSA_1*	*PSA_2*	*PSA_3*	*PSA_4*
0 = 0 + 0 + 0 + 0	0	0	0	0
1 = 1 + 0 + 0 + 0	1	0	0	0
2 = 1 + 0 + 1 + 0	1	0	1	0
3 = 1 + 1 + 1 + 0	1	1	1	0
4 = 1 + 1 + 1 + 1	1	1	1	1
5 = 2 + 1 + 1 + 1	2	1	1	1
6 = 2 + 1 + 2 + 1	2	1	2	1
7 = 2 + 2 + 2 + 1	2	2	2	1
8 = 2 + 2 + 2 + 2	2	2	2	2
⋮	⋮	⋮	⋮	⋮
31 = 8 + 8 + 8 + 7	8	8	8	7

Table 5-1. Truth table for phase step addends decoder

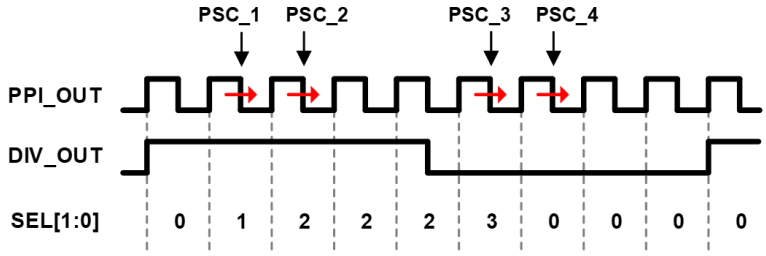


Figure 5.11. Operation principle of the phase rotation with phase step instants highlighted for a MMDIV division ratio of 9

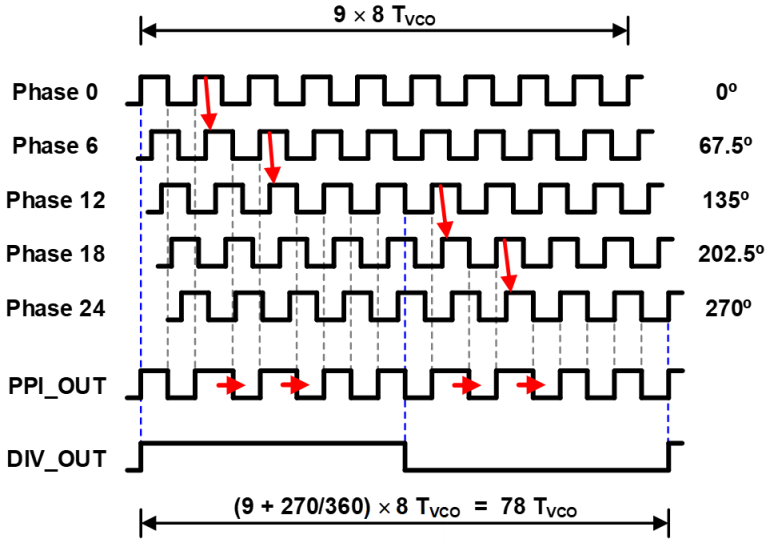


Figure 5.12. Phase rotation scenario for a total effective divider ratio of 78

5.7 Circuit Implementation

Key components of the 38GHz chirp synthesizer PLL include the BPDSM, which enables high resolution of the BPDSTDC, the VCO, the high-speed divider stages, and the PPI, which is essential to implement the fine divider ratio step size. This section covers implementation details of those key components.

5.7.1 Bandpass ΔΣ Modulator

The BPDSM is implemented as a 4^{th}-order continuous-time modulator to obtain 2^{nd}-order noise shaping in the BPDSTDC. A block schematic of the BPDSM is shown in Figure 5.13. Since the input signal passes the continuous-time loop filter of the modulator and signal sampling occurs at the quantizer, the continuous-time modulator architecture offers inherent anti-aliasing, which suppresses distortion in the sinusoidal PLL reference. The distributed-feedback architecture of the modulator employs single-opamp resonators (Figure 5.14) to reduce area and power consumption [38]. Since these types of resonators offer only one injection point for the feedback signal, which is at the resonator input, return-to-zero (RZ) and half-clock-delayed return-to-zero (HZ) DACs are used to implement the loop transfer function and stabilize the modulator. Two DACs (RZ and HZ) are needed per resonator if the modulator architecture does not include any feed-forward paths. In [38], two feed-forward paths are introduced so that only one DAC per resonator is required. This reduces the input-referred noise of the modulator, but the direct path from the input to the quantizer degrades the anti-aliasing effect. The BPDSM in this work uses a single feed-forward path around the second resonator [39]. This still allows the omission of the RZ DAC at the modulator input for the benefit of reduced input-referred noise, which results in a lower noise floor in the modulator

passband. At the same time, the anti-aliasing is retained as the input passes through the first resonator.

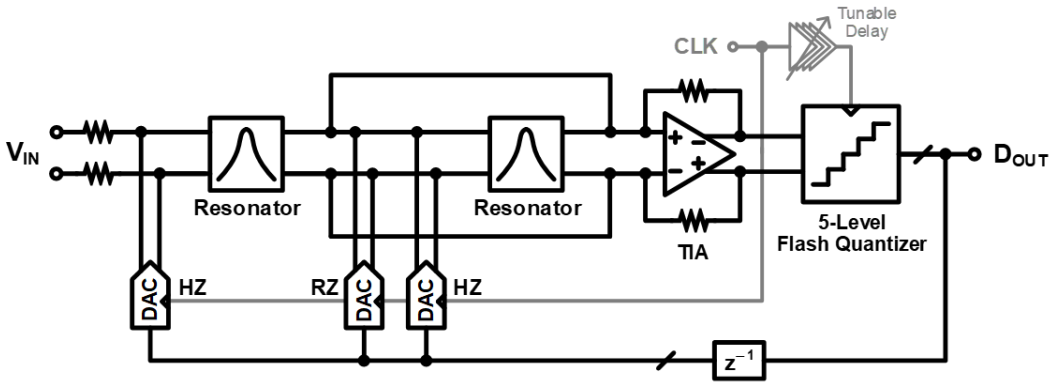


Figure 5.13. Implementation of the bandpass ΔΣ modulator

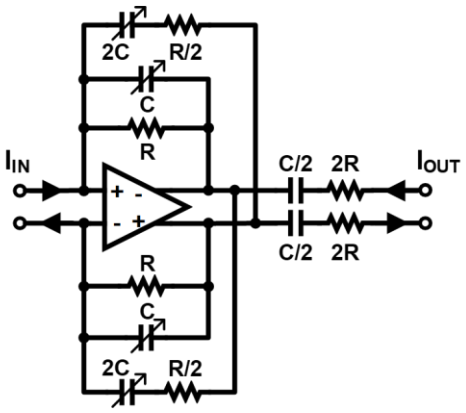


Figure 5.14. Single-opamp resonator

For the application of the BPDSM in the BPDSTDC, quantization noise suppression around F_{REF} is crucial, requiring the center frequency of the resonators to be at F_{REF}. The single-opamp resonators implement the biquadratic transfer function $H_r(s) = 0.5 \cdot \omega_0 \cdot s/(s^2 + {\omega_0}^2)$, where the center frequency $\omega_0 = 1/(RC)$, and the resonator quality factor Q is infinite. However, process variations and mismatch in the passive resonator components lead to a shift of the center frequency and degrade Q. Therefore, capacitive tuning banks are added to the resonators to adjust the center frequency and maximize Q.

A transconductance amplifier sums the output currents of the resonators, and its output voltage is digitized by a 5-level flash quantizer. The thermometer code generated by the quantizer controls the feedback DACs and is processed by subsequent logic that implements the DDC of the BPDSTDC. The feedback DACs are implemented as current steering DACs, each consisting of four unit current cells. Additional measures such as dynamic element matching to account for the DAC non-linearity are not considered in the BPDSM design because the modulator input frequency is exactly one fourth of the sampling frequency when the PLL is locked. Therefore, harmonics of the input frequency fold down to dc or onto the fundamental and do not appear in the output spectrum of the PLL.

5.7.2 Voltage-Controlled Oscillator

The high-frequency PLL output is generated by a supply-biased push-pull LC-VCO. A circuit schematic of the VCO as well as the measured frequency tuning characteristic for a 1.2V supply are shown in Figure 5.15. The VCO design omits capacitive tuning banks in favor of a higher tank quality factor. Resistors are placed at the drain terminals of the active devices to reduce the 1/f-noise corner frequency [40]. The measured tuning range of the VCO extends from 36.2GHz to 38.2GHz for a 1.2V supply. A reduced tuning range is used in the PLL by adjusting the reference voltages of the resistor ladder in the preceding $\Delta\Sigma$ DAC.

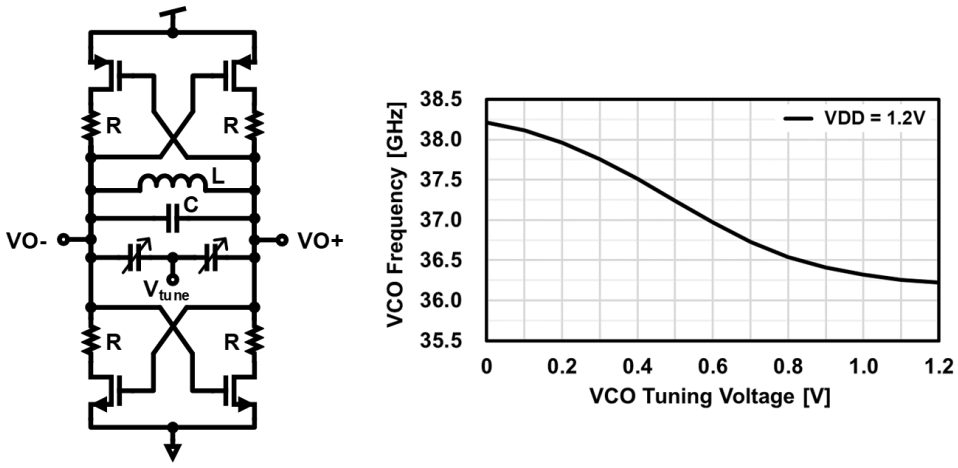


Figure 5.15. VCO implementation and measured VCO tuning characteristic

5.7.3 High-Speed Divider Stages

A high-speed (CML) divider stage (Figure 5.16(a)) divides the VCO output by four before the divided-down signal is converted to CMOS levels. The CML divider consists of two divide-by-two CML divider units, each of which is formed by two differential latches. In the first unit, the outputs of only one latch are connected to the subsequent divider stage. In the second unit, the outputs of both latches are tabbed to obtain four output phases.

After conversion to CMOS, a CMOS divider stage (Figure 5.16(b)) processes the four phases and divides the frequency by two while producing eight output phases. The CMOS divider consists of two divider units operating in parallel, where each unit is formed by two differential CMOS latches, in analogy to the CML divider units. By tabbing all four CMOS latches, eight output phases are obtained. Since the correct sequence of the eight phases is not guaranteed upon start-up, the latches include reset switches to reset the CMOS divider stage.

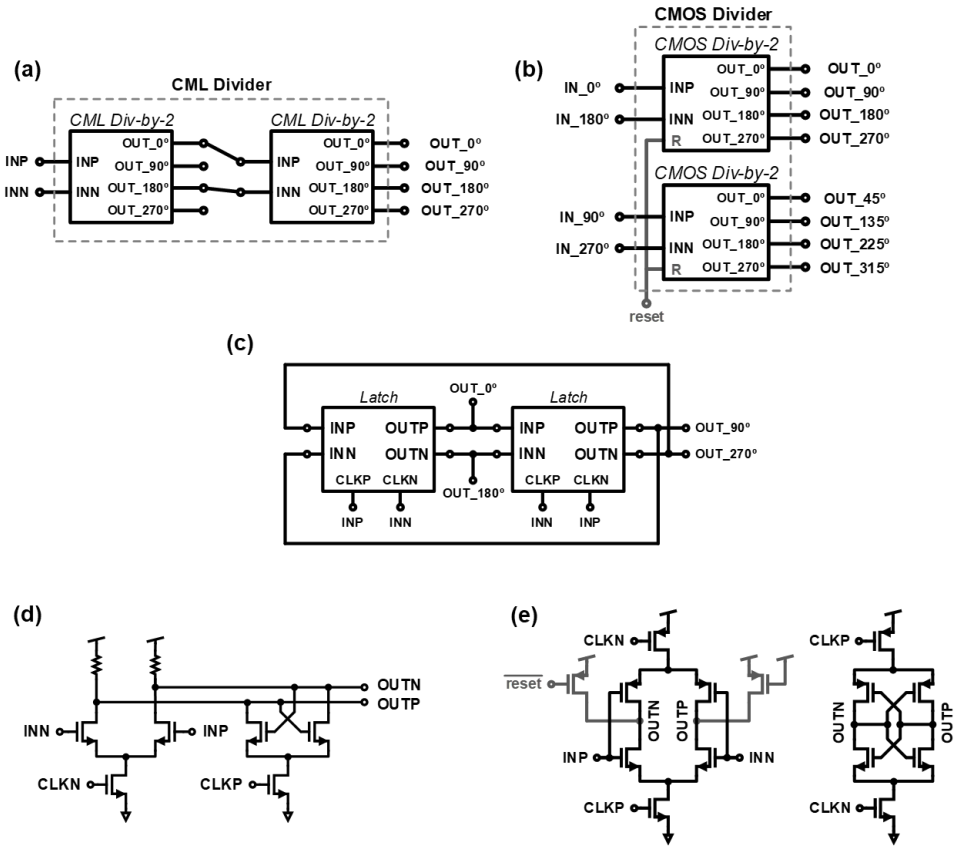


Figure 5.16. CML divider (a), CMOS divider (b), Divide-by-2 unit (same topology for CML divider and CMOS divider) (c), CML latch (d), and CMOS latch (e)

5.7.4 Pipelined Phase Interpolator

The feedback divider of the PLL incorporates a PPI to increase the number of available phases and emulate a fine divider ratio step size by applying a phase rotation scheme. A block schematic of the PPI is shown in Figure 5.17. The pipelined PI topology becomes apparent in the alternating sequence of switch units and phase interpolator (PI) units, which takes into account that only one phase needs to be available at the PI output in any given switching cycle [41]. This type of PI implementation reduces design complexity and saves power and area. At the PPI input, an 8-to-2 switching network selects two adjacent phases from the eight input phases and feeds them to the first PI unit. The PI unit forwards both phases and generates a third intermediate phase.

A 3-to-2 switch selects two adjacent phases from the three output phases of the first PI unit and feeds them to a second PI unit. A 2-to-1 multiplexer switches the first forwarded phase or the intermediate phase of the second PI unit to the PPI output. This way, the PPI quadruples the number of phases selectable at the PPI output to 32. The control bits of the PPI switches select the PPI output phase and are set and updated by the phase rotation logic.

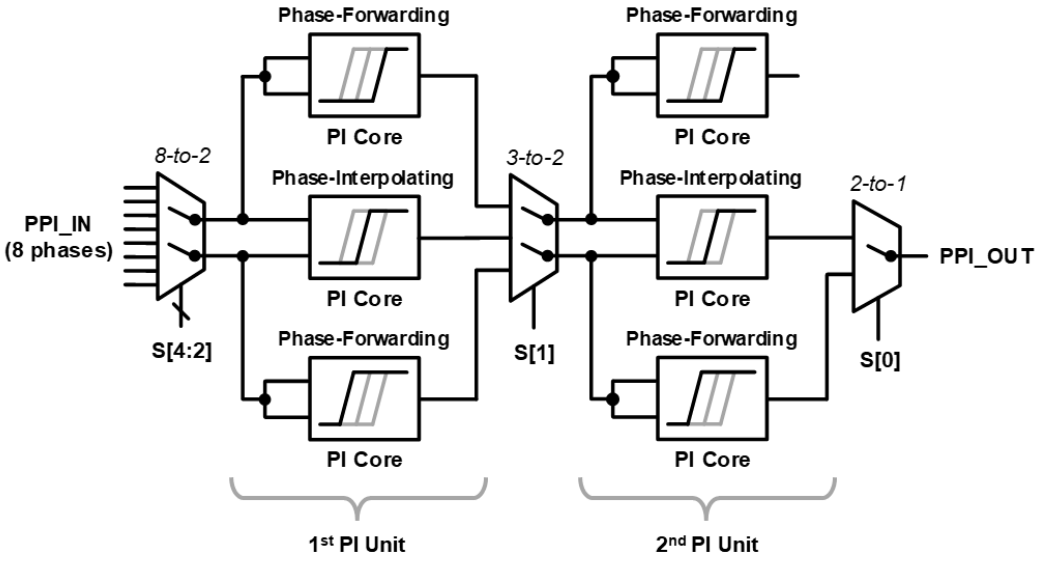


Figure 5.17. Pipelined phase interpolator

Each PI unit consists of three PI core circuits, two of which operate in phase-forwarding mode, while the third interpolates the two input phases. The PI core circuit is shown in Figure 5.18 along with a timing diagram that illustrates the operation of the phase-interpolating PI core. The charging and discharging currents in both branches of the PI core circuit are limited by current sources of equal currents to ensure linear phase interpolation. In addition, the logic gates at the PI core inputs avoid short-circuit currents between the edges of the input phases to improve PI linearity [41]. Dummy gates are used at the PI core inputs so that both inputs present the same load.

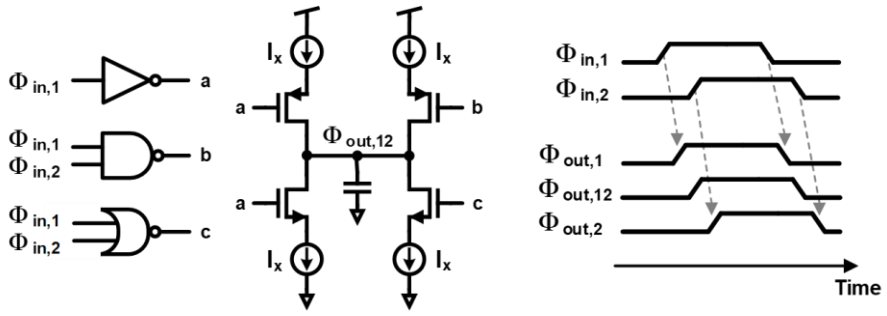


Figure 5.18. Phase interpolator core circuit with timing diagram

5.8 Measurement Results

The 38GHz chirp synthesizer PLL is fabricated in 40nm CMOS. The prototype IC measures 1.0mm x 1.2mm and includes additional digital circuitry for reconfiguration and debugging. A die photo is shown in Figure 5.19. The IC is wire-bonded in a 32-pin QFN package and placed with the high-frequency output pads very close to the package pins to minimize bond wire lengths. Triple bonding is used for these pads to further reduce the effective bond wire inductance. The QFN package is soldered on a 4-layer PCB with Rogers 4350B as the top dielectric and 50Ω transmission lines for the high-frequency differential outputs. A balun on the PCB converts the external PLL reference signal from single-ended to differential, as required for the BPDSTDC input. Two low-phase-noise signal generators (R&S SGS100A, Keysight N5183A) provide the PLL reference and an external TDC clock, respectively, and phase noise measurements are performed with a Keysight N9030B. In addition, the generated FMCW chirps are recorded with an R&S FSW43. The measurement setup for the chirp synthesizer is shown in Figure 5.20.

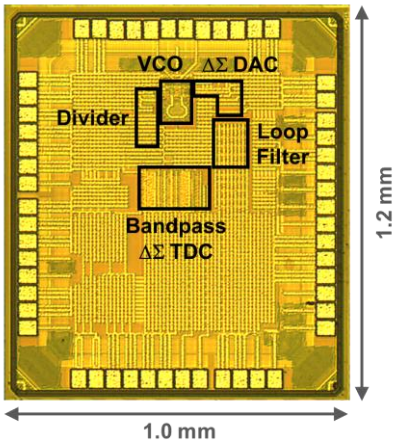


Figure 5.19. Die micrograph of the 38GHz chirp synthesizer prototype

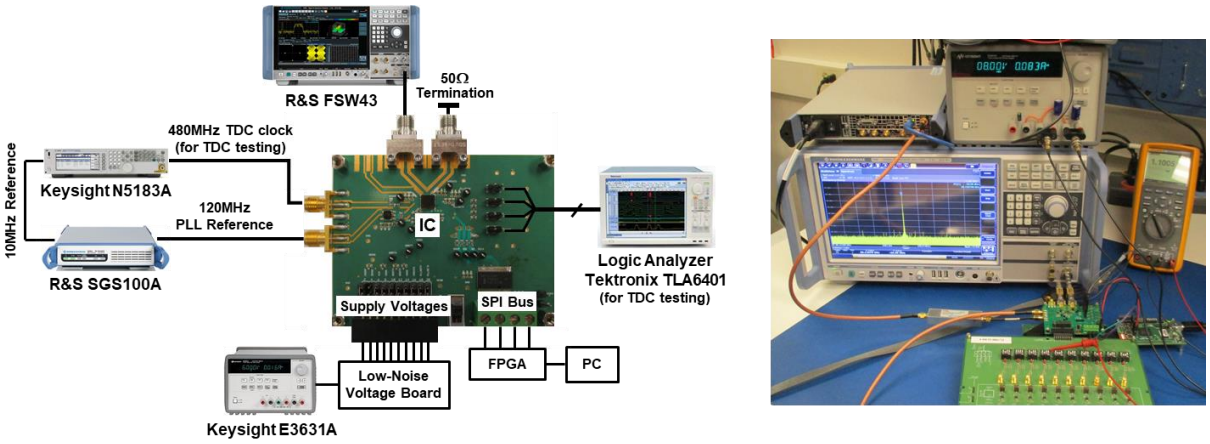


Figure 5.20. Measurement setup for the 38GHz chirp synthesizer

5.8.1 TDC Measurements

The BPDSTDC occupies 0.02mm^2 and consumes 8.4mW from a 1.1V supply. To characterize the BPDSM and verify its configuration, stand-alone measurements of the BPDSM with a 120MHz input and an external 480MHz clock are performed. Based on the measured BPDSM output spectra, the resonators in the BPDSM are tuned to center the quantization noise suppression around the center frequency of 120MHz. In addition, the input amplitude is successively increased during measurements until the BPDSM output saturates to determine the

maximum (full-scale) input. Both steps ensure maximum BPDSM resolution in the center band, resulting in maximum TDC resolution. For a full-scale input, the measured BPDSM resolution is 63dB SNDR or 10.2b ENOB for a 5MHz bandwidth around 120MHz (Figure 5.21). (For a 2MHz bandwidth, the measured resolution is 66dB SNDR or 10.7b ENOB.) According to equation (5.1), the estimated TDC resolution is 1.1ps in a 2.5MHz bandwidth (0.8ps in a 1MHz bandwidth). A flat noise floor is visible in the center band, indicating that the BPDSM resolution is limited by thermal noise. Noise simulations of the BPDSM suggest that the first resonator is the dominant contributor of thermal noise in this BPDSM design.

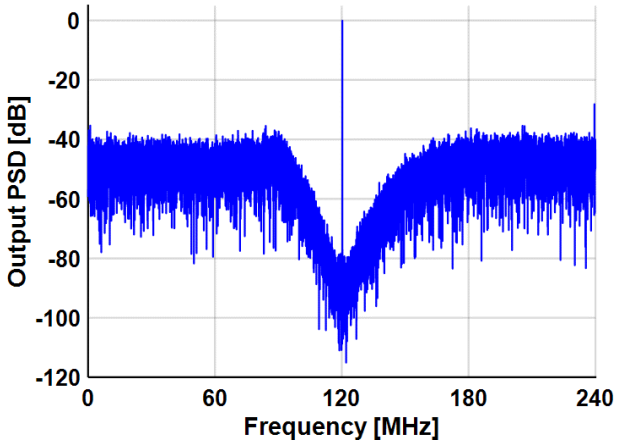


Figure 5.21. Measured output spectrum of the bandpass ΔΣ modulator for a full-scale input

To characterize the BPDSTDC, a phase-modulated clock is applied to the BPDSM. The BPDSM output data is recorded and the DDC is performed as part of the data post-processing. To account for the effective TDC sampling frequency of 240MHz, DDC considers every other output word and multiplies them alternately by +1 and -1. The clock signal source generating the phase modulation (PM) offers limited PM linearity and the PM amplitude is chosen as large as possible without observing harmonics in the TDC output spectrum. Figure 5.22 shows the output spectra obtained with $33ps_{pp}$ phase deviation for 100kHz PM and 1MHz PM, respectively. The spectra show a flat noise profile up to about 2.5MHz, confirming the targeted TDC bandwidth, and reveal

2^{nd}-order noise shaping, which is evident in the 40dB per decade increase in quantization noise at high frequencies. In a 1MHz bandwidth, the measured integrated noise of the TDC is $325fs_{rms}$ and $352fs_{rms}$, respectively ($515fs_{rms}$ and $565fs_{rms}$ in a 2.5MHz bandwidth). This corresponds to a TDC resolution of 1.2ps in a 1MHz bandwidth (1.9ps in a 2.5MHz bandwidth), in good agreement with the above estimate based on the BPDSM resolution. Table 5-2 compares the BPDSTDC with state-of-the-art noise-shaping TDCs.

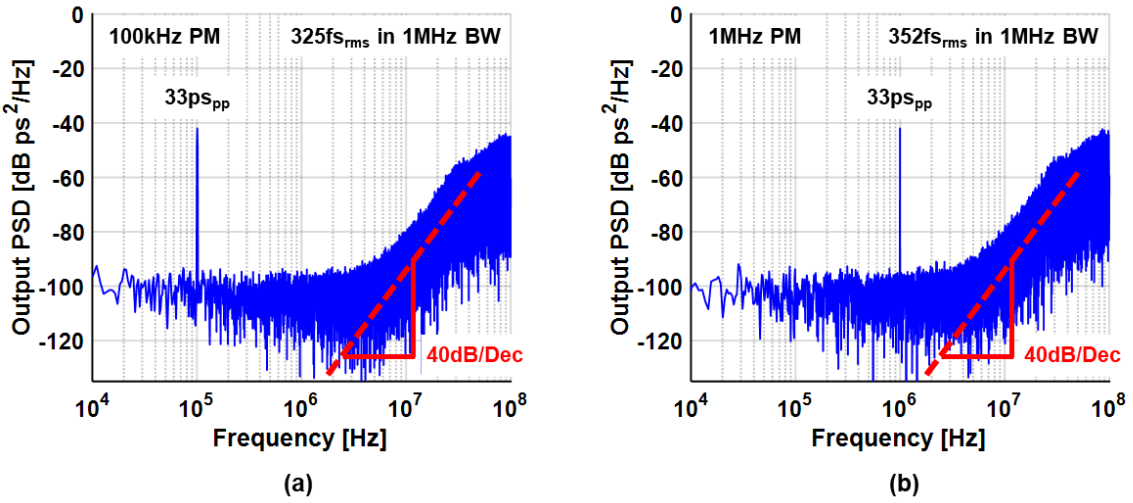


Figure 5.22. Measured output spectra of the bandpass ΔΣ TDC for 100kHz PM (a) and 1MHz PM (b)

	This work	JSSC'18 Dayanik [4]	RFIC'15 Wu [42]	CICC'13 Yu [43]	ISSCC'12 Elshazly [44]
TDC Type	CTΔΣ	PFD/CP + CTΔΣ	Flash-ΔΣ	GSRO	SRO
Technology [nm]	40	65	40	65	90
Supply Voltage [V]	1.1	1.2	1.1	--	1.0
Power [mW]	8.4	8.4	1.32	6.55	2
Area [mm^2]	0.02	0.055	0.08	0.05	0.02
Integrated Noise [fs_{rms}]	325*	182	103	148	315
Bandwidth [MHz]	2.5	1	1.25	4	1
Sampling Rate [MS/s]	240	250	50	400	500

* In a 1MHz bandwidth

Table 5-2. TDC performance comparison with state-of-the-art noise-shaping TDCs

5.8.2 Synthesizer Measurements

The synthesizer occupies 0.18mm^2 and consumes a total power of 68mW. The power consumption distribution is shown in Figure 5.23. Since simulations suggest robust PLL locking, the PLL is implemented without an additional loop for frequency acquisition upon start-up. Experiments confirm the robust locking behavior seen in simulations. In addition to the simulated PLL locking with a full-scale sinusoidal PLL reference, Figure 5.24 also shows the simulated locking behavior with a square-wave reference of same amplitude, revealing the benefit of the inherent filtering offered by the BPDSTDC.

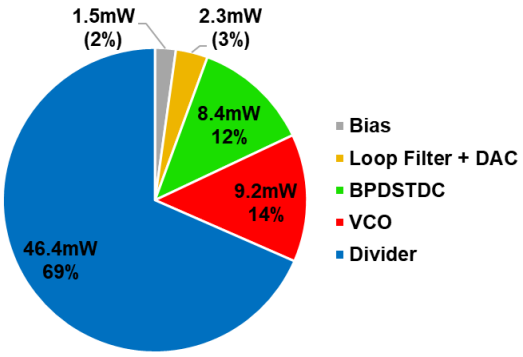


Figure 5.23. Power consumption distribution of the synthesizer prototype

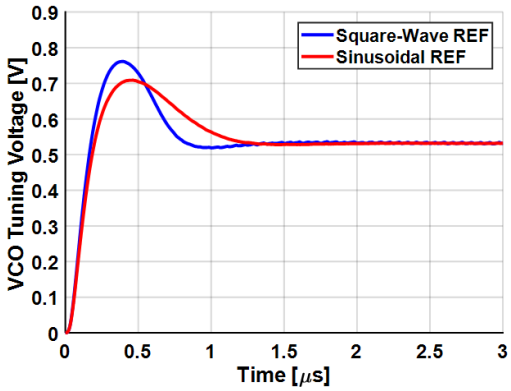


Figure 5.24. Simulated PLL locking with a full-scale sinusoidal reference and a square-wave reference of same amplitude

The PLL output covers a frequency range from 36.3 to 38.2GHz. The measured output spectrum for a 38.1GHz output is shown in Figure 5.25. The spurious performance of the PLL is limited by phase mismatch in the feedback divider and the measured spurs are below -55dBc. These spurs have no significant impact on the radar performance because their locations vary as the output frequency is modulated.

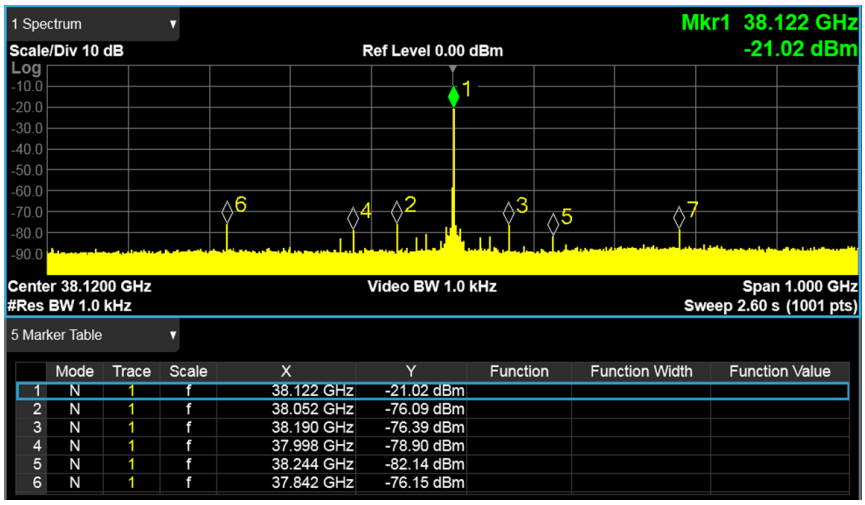


Figure 5.25. Measured PLL output spectrum at 38.1GHz

To verify the measured close-in phase noise, the theoretical close-in phase noise of a conventional PLL can be calculated from the measured TDC performance as [45]

$$L = \frac{(2\pi)^2}{12} \cdot \left(\frac{\Delta t_{res,TDC}}{T_{VCO}}\right)^2 \cdot \frac{1}{F_{REF}{}^*} \tag{5.2}$$

where $\Delta t_{res,TDC}$ is the effective TDC resolution in a specified bandwidth, T_{VCO} is the VCO oscillation period and $F_{REF}{}^* = F_{REF}/OSR$ is the reference frequency normalized to the OSR of the TDC. In this case, F_{REF} is the effective TDC sampling frequency of 240MHz and a TDC bandwidth of 1MHz is used, giving $OSR = 240$. Equation (5.2) assumes that the close-in phase noise is solely limited by the TDC noise. For $F_{VCO} = 38GHz$ and $\Delta t_{res,TDC} = 1.2ps$, the calculated phase noise is -82dBc/Hz.

The loop filter gain K_{LF} is changed between phase noise measurements to adjust the PLL bandwidth. The measured phase noise for a wide PLL bandwidth >1MHz is shown in Figure 5.26(a). Phase noise peaking around 1MHz offset is due to peaking in the loop transfer function as the PLL is configured to have a wide bandwidth with low phase margin for high PLL agility. The PLL achieves a measured phase noise of -85dBc/Hz at 100kHz offset, corresponding to a

normalized phase noise of -216dBc/Hz^2. These results are obtained if the loop filter and the ΔΣ DAC are clocked at 480MHz. However, if both components are clocked at the effective TDC sampling frequency of 240MHz as suggested in Section 5.5 , the measured close-in phase noise is degraded by about 2dB and in excellent agreement with the theoretical phase noise calculated above. Furthermore, the measured phase noise profile for a low PLL bandwidth <1MHz is shown in Figure 5.26(b). In this case, there is no phase noise peaking and the close-in phase noise is increased as less VCO noise is suppressed.

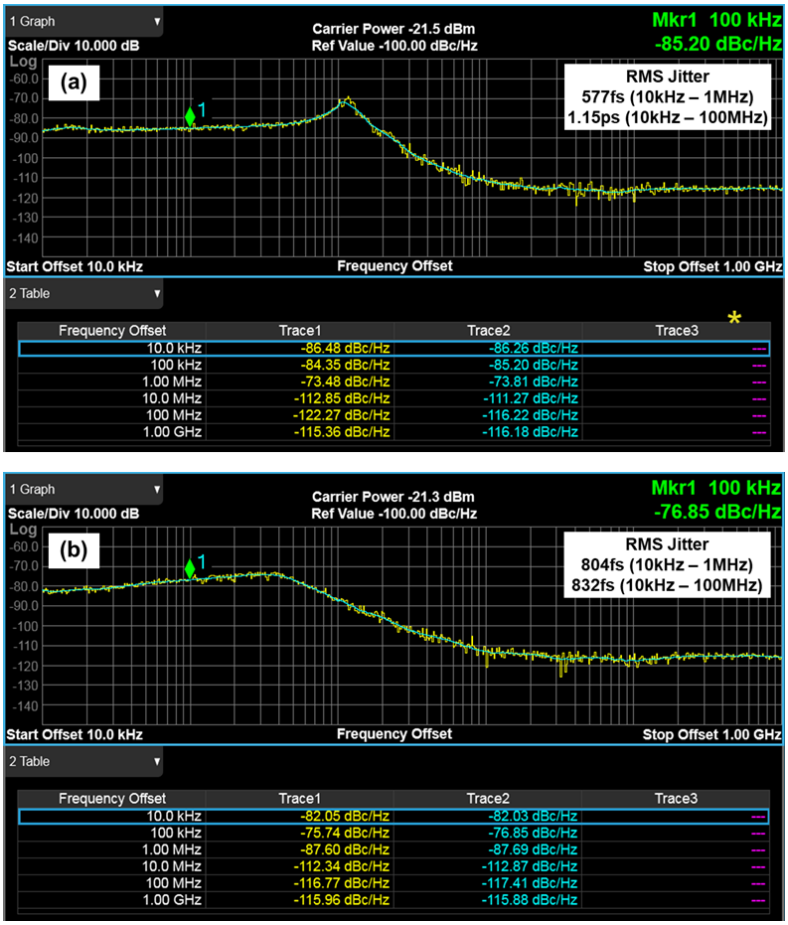


Figure 5.26. Measured PLL output phase noise for a wide PLL bandwidth >1MHz (a) and a low PLL bandwidth <1MHz (b)

To verify the quality of the generated FMCW chirps, the on-chip chirp control logic is enabled and configured such that the digital modulation signal has 10-bit linearity and the PLL generates triangular chirps with a 500MHz bandwidth from 37.65 to 38.15GHz. Figure 5.27 shows the synthesizer output spectrum, revealing the chirp bandwidth and turn-around frequencies. The modulation period is modified during measurements to record the instantaneous output frequency and frequency error for different chirp slopes. The recorded profile of a fast chirp (9.1MHz/µs slope) and the measured error, i.e. the frequency deviation from an ideal chirp, are shown in Figure 5.28(a). Due to the nonlinear VCO gain, the loop gain of the PLL and with it the PLL bandwidth change as the PLL output traverses the chirp profile, resulting in different peak errors at the upper and lower turn-around points (TAPs). The measured rms frequency error excluding the TAPs is 824kHz. The recorded profile and frequency error of a slow chirp (1.0MHz/µs) is shown in Figure 5.28(b), and Table 5-3 lists the measured frequency errors for different chirp slopes. Table 5-4 compares the 38GHz synthesizer with state-of-the-art CMOS FMCW chirp synthesizer PLLs.

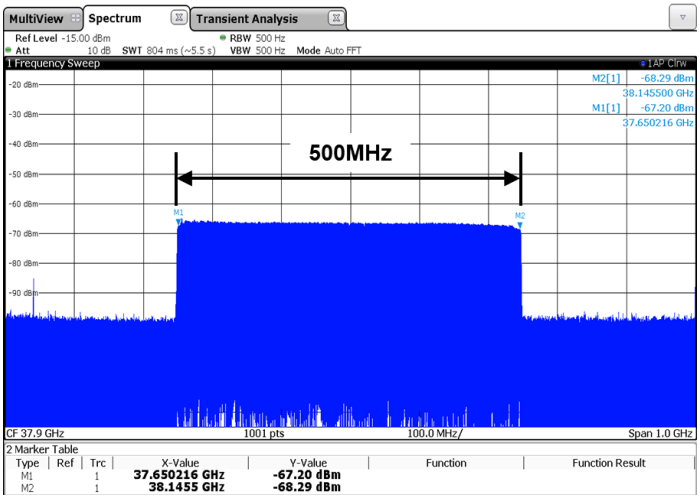


Figure 5.27. Measured FMCW chirp spectrum

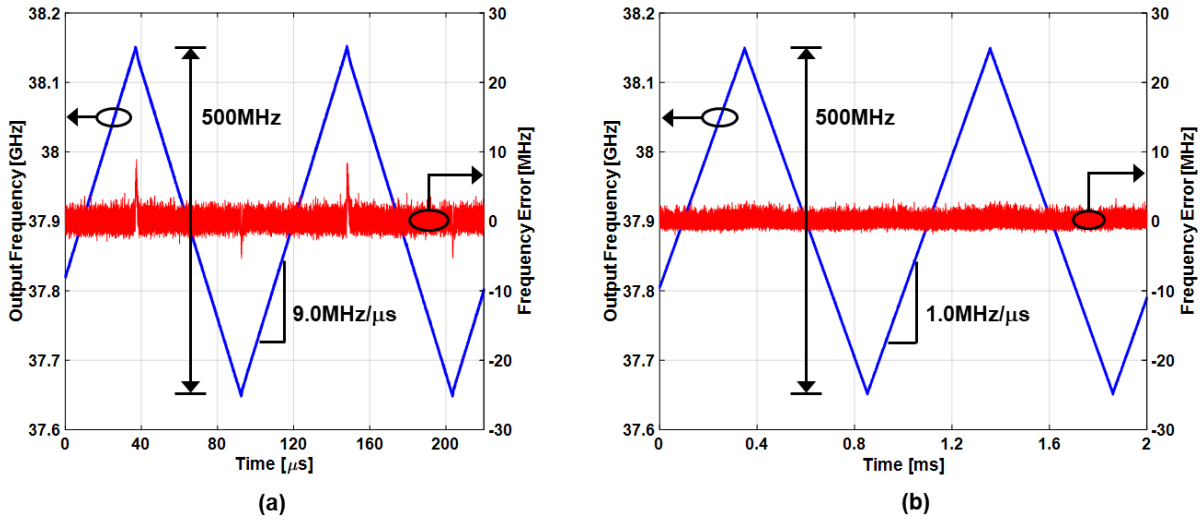


Figure 5.28. Measured FMCW chirp and frequency error for a fast chirp (a) and a slow chirp (b)

Modulation Period	0.11ms	0.20ms	0.50ms	1.0ms
RMS Frequency Error (w/o TAPs)	824kHz	692kHz	640kHz	589kHz
Peak Frequency Error	8.9MHz	6.8MHz	4.0MHz	3.3MHz

Table 5-3. Measured frequency errors for a 500MHz chirp bandwidth

	This work	ISSCC'18 Cherniak [3]	ISSCC'16 Yeo [6]	JSSC'14 Wu [7]	ISSCC'11 Sakurai [8]	JSSC'10 Lee [10]	JSSC'10 Mitomo [11]
PLL Architecture	Digital Frac-N	Digital TPM**	Digital TPM**	Digital TPM**	Mixed-Mode	Analog Frac-N	Analog Int-N +DDFS
TDC Type	CTΔΣ	Bang-bang PD	Linear	Delay Chain	Delay Chain	--	--
Technology [nm]	40	65	65	65	65	65	90
Supply [V]	0.9/1.1/1.2	--	1.2	1.2	1.2	1.2	1.2
Power [mW]	68	19.7	14.8	48	152	73	101
Area [mm^2]	0.18	0.48	0.18	0.48	1.7	0.16***	0.63***
Frequency range [GHz]	36.3-38.2	20.4–24.6	8.4-9.4	56.4-63.4	82.1-83.8	75.6-76.3	78.1-78.8
Ref. frequency [MHz]	120	52	277	10-100	26	700	77
Spur level [dBc]	-55	-58	--	-74	--	-40	--
Phase Noise @100kHz [dBc/Hz]	-85	-89	-102	-72	-52	-88	-68
Normalized Phase Noise @100kHz [dBc/Hz^2] *	-216	-219	-216	-207	-196	-217	-207
Chirp period [μs]	50-2000	1.2 - 315	5 - 220	420-8200	2000-10000	1000-1500	500
Chirp slope [MHz/μs]	9.1	173	32.63	4.76	1.5	0.97	2.46
RMS freq. error [MHz]	0.82	0.11	1.9	0.38	0.18	0.3	1.05

* Phase Noise – 20log(Division Ratio) – 10log(F_{REF})
** Two-Point Modulation
*** Estimated from die micrograph

Table 5-4. Comparison of the 38GHz synthesizer with state-of-the-art CMOS FMCW chirp synthesizer PLLs

5.9 Conclusion

A digital 38GHz chirp synthesizer PLL for FMCW radar is implemented with a noise-shaping TDC based on a BPDSM. Overcoming the shortcomings of other ADC-based phase digitization techniques, the presented TDC design uses a BPDSM to sample a sinusoidal PLL reference and digitize the phase information. Since the BPDSTDC samples the reference at four times the reference rate and applies DDC, flicker noise does not interfere with the phase-difference measurement and the TDC offers an extended phase detection range, resulting in robust PLL locking. The BPDSTDC makes efficient use of the BPDSM bandwidth and leverages the high resolution of the BPDSM to enable low close-in phase noise for wide loop bandwidths in a high-frequency digital PLL. The chirp synthesizer PLL is implemented as a type-II fractional-N PLL with on-chip control logic for chirp generation. Since the PLL feedback signal clocks the BPDSTDC and carries the fractional-N $\Delta\Sigma$ noise, fractional-N division in the PLL is based on phase interpolation and a phase rotation scheme to reduce the fractional-N quantization noise and ensure that the TDC noise determines the close-in phase noise of the PLL. A prototype IC is fabricated in 40nm CMOS, occupies an area of 0.18mm^2 and consumes 68mW. The PLL achieves a measured close-in phase noise of -85dBc/Hz and a normalized phase noise of -216dBc/Hz^2 at 100kHz offset for wide loop bandwidths >1MHz. Chirp measurements confirm that the synthesizer effectively generates fast and precise triangular FMCW chirps.

CHAPTER 6 Conclusion and Future Work

FMCW radar applications depend on fast-settling and low-phase-noise frequency synthesizers for chirp generation. Digital fractional-N PLLs are attractive for FMCW chirp generation as they offer flexibility and area efficiency, but require high-performance TDCs. This dissertation investigates the requirements for PLL-based FMCW chirp synthesis and focuses on the design of digital FMCW chirp synthesizer PLLs using noise-shaping TDCs based on continuous-time ΔΣ modulators. The contributions of this work are an analysis of the PLL bandwidth and chirp linearity to provide general guidance for the synthesizer design, a digital chirp synthesizer with a proven noise-shaping TDC as well as an experimental setup to verify the effectiveness of the synthesizer, and a novel bandpass ΔΣ TDC employed in a digital fractional-N PLL architecture for FMCW chirp synthesis.

The analysis examines the impact of the PLL bandwidth and chirp linearity on the overall radar performance. Based on a model of a complete radar system including a PLL-based chirp synthesizer, the presented approach allows for a straightforward study of the radar accuracy and reliability as functions of the chirp parameters and the PLL configuration. An exemplary analysis for a long-range automotive radar scenario provides design guidance for both slow and fast chirp modulation.

The first synthesizer design is a 20GHz digital fractional-N PLL intended for a 240GHz FMCW radar application and uses an existing noise-shaping TDC design that is based on a third-order ΔΣ modulator. A prototype fabricated in 65nm CMOS achieves a measured close-in phase

noise of -88dBc/Hz at 100kHz offset with wide PLL bandwidths while consuming 39.6mW, and effectively generates a 25-segment frequency ramp ranging from 19.1 to 20.4GHz. Experiments with a radar testbed confirm the effectiveness of the synthesizer design in a complete FMCW radar system.

The second synthesizer is implemented as a 38GHz digital fractional-N PLL and features a bandpass ΔΣ TDC that measures phase by sampling a sinusoidal reference. The novel TDC design combines a fourth-order bandpass ΔΣ modulator with digital down-conversion to achieve low noise in the frequency band of interest while offering an extended phase detection range. Phase interpolation and the application of phase rotation in the feedback divider ensure low PLL output phase noise during fractional-N operation. A prototype fabricated in 40nm CMOS achieves a measured close-in phase noise of -85dBc/Hz at 100kHz offset for wide loop bandwidths >1MHz while consuming 68mW, and generates fast (500MHz/55μs) and precise (824kHz$_{rms}$ frequency error) triangular chirps.

Items of future work are suggested in the following list and pertain to the digital chirp synthesizer PLL design using the novel bandpass ΔΣ TDC as described in Chapter 5. Potential improvements for better system performance include:

- Improved resolution of the bandpass ΔΣ modulator by lowering the thermal noise level and increasing the number of quantizer levels to increase the TDC resolution and thus improve the close-in phase noise of the PLL
- Reduced phase mismatch in the feedback divider by revising the phase generation and calibrating the phase interpolation to reduce the spur levels in the PLL output

- Revision of the divider architecture to reduce the power consumption while retaining the fine divider ratio step size
- Development of a noise cancellation scheme for the fractional-N $\Delta\Sigma$ divider noise
- Implementation of a loop filter architecture having a proportional path in addition to the existing integral path to avoid phase noise peaking
- Linearization of the VCO gain to ensure a constant PLL bandwidth and achieve optimum chirp linearity across the output frequency range of the chirp synthesizer

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