A High-Yield Microfabrication Process for Sapphire Substrate Pressure Sensors with Low Parasitic Capacitances and 200°C Tolerance

by

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ABSTRACT

Microelectromechanical systems (MEMS) can offer many benefits over conventional sensor assembly, especially as the desire for smaller and more effective instrumentation escalates in demand. While many industries continually strive for improved sensing capabilities, those invested in natural gas and oil extraction have a particular interest in miniaturized pressure sensing systems. These sensors need to operate autonomously in harsh environment (50 MPa, 125°C) fissures (≤1 cm) with at least 10-bit pressure resolution (≤0.05 MPa).

The primary focus of this report is the development of a surface micromachining process to fabricate high performance capacitive pressures sensors, utilizing dielectric substrates to enable extremely low offset and parasitic capacitances and temperature coefficients. In contrast to conventional bulk silicon micromachining methods that use various kinds of etch stops such as electrochemical or dopant selective, dry additive processes are utilized to reduce manufacturing complexity, cost, and material consumption and have gained favor in recent years as the tools have matured.

The fabricated devices must meet both pressure sensing and dimensional scaling requirements with a full-scale range of ≥50 MPa, resolution of ≤50 kPa (>20 fF/MPa with a system resolution of 1 fF/code), and size of $\leq 2\times 1\times 0.5$ mm^3. In order to meet these goals while maximizing yield, particular attention has been given to the interplay between equipment limitations and device design. Process and design features have been refined over four process generations that together lead to a capacitance response of >450 fF/MPa over 50 MPa, provide a yield of >80%, permit an extreme span (>1000×) of full-scale range designs, and allow automated

system assembly. Devices have been tested at pressures and temperatures of up to ≥50 MPa and 200°C, representing downhole environments, demonstrating <7.0 kPa (<1 psi) resolution. Devices designed to operate over a much lower full-scale range of <50 kPa (≤350 Torr), representing biomedical applications, have been tested and demonstrate a resolution of <80 Pa (<0.6 Torr).

Sensor response and design have been validated in the primary use-case of autonomous microsystem integration. The system circuity includes a microcontroller, capacitance-to-digital converter, temperature sensor, photodiode, and battery. The readout electronics and sensor are mounted onto a flexible PCB, packaged into stainless steel or ceramic shells, sealed with silicone epoxy to permit pressure transmission while providing environmental protection, and measure $<9 \times 9 \times 7$ mm^3 in size. The systems have been successfully field tested in a brine well.

While the capacitive pressure sensors have been developed primarily for active microsystems, there may be situations where a wired connection to the readout circuitry is not possible. A passive wireless pressure monitoring system utilizing short-range inductive coupling has been developed to evaluate the performance of the sapphire substrate sensors for this use-case. The passive sensing element consists of the capacitive pressure sensor and an inductor, packaged in a 3D printed biocompatible housing measuring ø12 x 24 mm^3. Pressure monitoring within the GI tract has been targeted; an *in situ* resolution of 1.6 kPa (12 Torr) at 6 cm has been achieved through conductive saline. A practical application of the sensor has been demonstrated *in vivo*, having been ingested and successfully interrogated in a canine model to monitor stomach pressure for over two days.

CHAPTER 1: Introduction

1.1 Motivation

Representing one of the greatest successes of the microsensor industry, pressure sensors have been produced for applications ranging from industrial and automotive to biomedical and healthcare [Gia06] and contributed sales of over 1.5 billion in 2017 [Yol18]. Pressure sensor microfabrication can employ more matured processes such as bulk silicon micromachining with various kinds of etch stops such as electrochemical [Klo89] and dopant selective [Zha94], or high temperature deposition methods such as low-pressure chemical vapor deposition (LPCVD) [Cho92]. In contrast to these techniques, dry additive processes use smaller quantities of chemicals and have gained favor in recent years as plasma-based manufacturing tools have come to maturity [Jae98]. Lower temperature plasma processes have historically had high defect densities and could not be successfully used without meticulous substrate cleanliness and preparation, which can be nearly impossible in non-industry-level laboratories, or densified with a high temperature (≥900°C) anneal step [Bat87]. LPCVD also involves temperatures upwards of 800°C while simultaneously using large quantities of chemical reagents in a furnace environment. This effort utilizes the technological advances in plasma-enhanced chemical vapor deposition (PECVD) [Siv13] to deposit high quality dielectric films to define the diaphragm while allowing for a reduction in manufacturing complexity, cost, and material consumption.

The primary goal for these sensors is microsystem integration to record pressure data in downhole environments for natural gas and oil exploration, in which commercial systems cannot reach or have insufficient imaging resolution. Therefore, the process must be able to meet the

necessary system-level requirements of size (≤2 × 1 × 0.5 mm^3), full-scale range (≥50 MPa), resolution (≥10-bit: ≤50 kPa (<7.0 psi); ≥20 fF/MPa (≥0.15 fF/psi) @ 1 fF/code system resolution), and temperature (≥125°C) with minimal offset capacitance (to increase system capacitance resolution) to successfully operate in these harsh environments.

Downhole Data Collection Background:

One of the most widely used data collection systems for borehole drilling is wireline logging, in which sensors are attached to a wireline cable (used for transporting equipment along a well shaft, measuring approximately 10 cm in diameter) and lowered into the borehole (approximately 15 cm in diameter), collecting data as the sensors travel down the shaft, illustrated in Fig. 1.1. One specific wireline pressure sensor from Schlumberger is the PressureXpress XPT-C [Sch15]. It is capable of recording pressures up to 55 MPa (8,000 psi) with an accuracy of 35 kPa (5 psi), measures 10 cm in diameter, 6.5 m long, and weighs approximately 200 kg. However, this method has the obvious disadvantage of only being able to provide data in the immediate vicinity of the wireline, as the sensors are quite large and require direct mounting to a wireline.

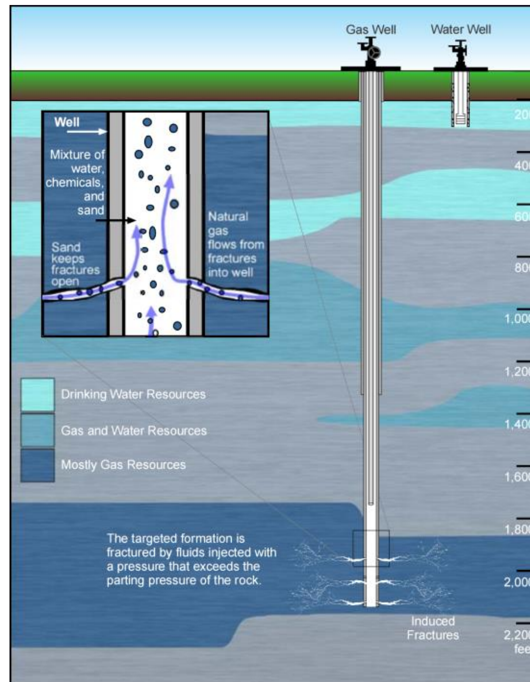

Fig. 1.1: Conventional well illustration utilizing wireline logging, duplicated from [Epa11].

In contrast to direct wireline sensing, wireless detection methods can be employed to image the area between boreholes. Cross-well electromagnetic emitters and receivers are lowered into adjacent wells and electromagnetic waves are transmitted between them, illustrated in Fig. 1.2. However, this technique has a limited resolution of ≈6 meters for nominal inter-well spacing [Sch06], is easily affected by environmental noise, and cannot be utilized on more modern, non-conventional (horizontally drilled) wells, as illustrated in Fig. 1.3.

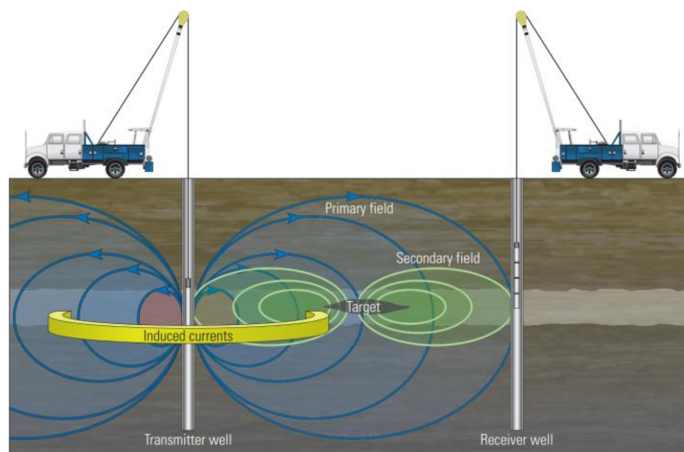

Fig. 1.2: Illustration of electromagnetic cross-well imaging, possible only in conventional (vertical) boreholes duplicated from [Sch09].

Microsystem Sensor Integration:

In order to gather a more complete picture of the downhole environment, borehole illumination methods capable of sensing outside the main well are required in general, but particularly in situations where cross-well imaging is not a viable option, such as in modern, non-conventional (horizontally drilled) boreholes. One possible solution is to use small autonomous microsystems which can freely flow in cm-scale borehole fractures, collecting data and recording location as they flow, then being recollected and interrogated after they are pumped back out of the well, illustrated in Fig. 1.3. While many considerations must be accounted for in the complete system [Li17], the sensing element itself has many requirements, including a sufficiently small form factor to fit within such a microsystem (with estimated maximum dimensions measuring $\leq 2 \times 1 \times 0.5$ mm^3), a capacitive output for the on-board electronic interface circuitry, minimal power consumption due to inherent reduced power capacity [Gia83], sufficient full-scale range (≥50 MPa), survivability of harsh environments (≥125°C), adequate capacitance response to allow for the desired resolution with the electronics (≥20 fF/MPa @ 1 fF/code for ≤50 kPa/code (≤7.0 psi/code), and small enough offset capacitance (C_0) to remain within the usable full-scale capacitance range of the C-to-D circuitry (<45 pF). However, there is a notable lack of miniaturized sensing elements (including both commercialized and those in academic research) capable of withstanding these harsh downhole environments while simultaneously meeting all of the necessary requirements for microsystem integration to record data in borehole fractures where wireline logging cannot reach and electromagnetic imaging cannot resolve. This sensor absence is a primary motivating factor for the design of a robust microfabrication process with which custom capacitive pressure sensors can be created.

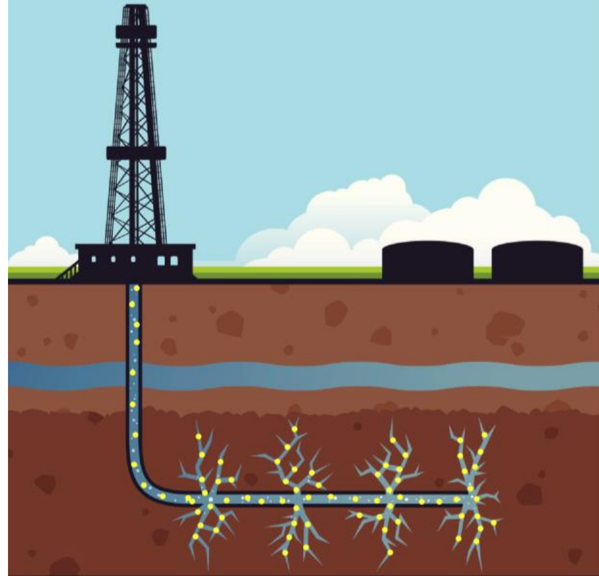

Fig. 1.3: Illustration of free-flowing distributed autonomous microsystems (illustrated with yellow dots) in a non-conventional borehole post-fracture [Hyd13].

Passive Wireless Sensing:

In addition to an active wired system integration approach, the development of a wireless system could offer sensing in even harsher conditions. A completely passive sensor removes the need for the most temperature sensitive system components (typically the battery and electronics) to withstand the harsh environment [Fon02]. When the capacitive pressure sensor is combined with a fixed inductor, it creates an LC resonator, resulting in a pressure-dependent resonant frequency, which can be monitored with an external inductor antenna, illustrated in Fig. 1.4. While the antenna and required excitation and readout electronics still needs to be placed relatively close to the sensing element (to maximize coupling between sensor and antenna coil), they can be more securely packaged, as a pressure feed through and direct sensor connection are no longer required.

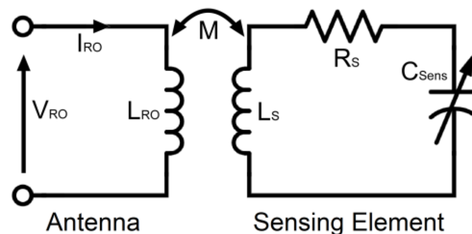

Fig. 1.4: Equivalent circuit of electrical model for an LC-resonant sensing element inductively coupled to an external readout antenna/inductor.

1.2 Pressure Sensor Background

Microfabricated pressure sensors that have been explored utilize a variety of transduction approaches including piezoresistive [Sam73], capacitive [San80], resonant-beam [Ike90], servo-controlled tunneling [Yeh94], pirani [Cho97], and microplasma discharge [Eun14]. Most commercialized pressure sensors utilize bulk silicon micromachined piezoresistive devices, as the technology has matured to a high level of understanding. The limitations of these devices are well known and include limited dimensional scaling, reduced full-scale output (~2% for typical devices), relatively large power budgets [Cha87], and large temperature coefficients [Kan82], making them unsuitable for high temperature applications. In comparison, capacitive pressure sensing devices tend to provide superior sensitivity and scalability, as well as lower noise, power consumption [Gia83], and temperature coefficients [Wan97]. However, they still face challenges such as reduced full-scale ranges [Par03], small absolute changes [Lee82], and difficulty in system integration [Ji92]. Some shortcomings can be overcome with enhanced readout circuitry [Cra90], but others, such as high offset capacitances and reduced full-scale range, simply cannot be electronically compensated (especially when size and power-budgets are of concern) without sacrificing other desired system characteristics.

Importance of Reducing the Offset Capacitance:

The susceptibility of capacitance-to-digital converters to large parasitic and offset capacitances [Pue90] is perhaps the largest challenge in both sensor design and system integration. As the offset capacitance is increased, the ultimate resolution of the circuitry generally decreases, causing a drop in system pressure resolution for the same capacitance response. There are many capacitance-to-digital-converter (CDC) architectures available, such as impedance metering [Lot99], dual-slope [Tan12], passive wireless telemetry [Tak04], and switched capacitor charge integration [Par83].

Impedance metering utilizes two AM modulator and demodulators in order to better reject any common mode signals, can customize the bandwidth and nominal (C_0) capacitance, and is quite accurate, offering a resolution as low as 42 aF. However, it is limited in dynamic range to ≈±1% of the chosen nominal capacitance before a high degree of non-linearity compromises accuracy. The dual-slope CDC design can be made to operate on very low power, but it often has a large nominal capacitance that must be charged for each reading, making it difficult to achieve sufficient resolution with small capacitance sensors with high energy efficiency. State-of-the-art designs offer resolutions of ≈10 fF/code over a full-scale range of 15-30 pF [Oh15]. If a passive wireless approach utilizing inductive coupling is used, a frequency dependent capacitance change can be created. However, the frequency response is directly related to the sensing element's total capacitance, and larger offsets will have a direct (negative) impact on the pressure-dependent frequency response, reducing the system resolution [Deh02].

Perhaps the most widely used architecture, though, is the switched capacitor charge integrator, illustrated in Fig. 1.5. It is a relatively simple circuit, offers an output voltage directly proportional to the capacitance change, and permits differential sensing in order to eliminate any parasitic capacitance common to both the sensor and a reference capacitor [Chu85]. As with most other CDC's, though, the absolute value of the sensed capacitance is limited by several factors. The steady state output voltage (equation 1.1) increases as the sensor capacitance rises; however, this output voltage is limited by the output limits of the op-amp driving the charge integrator and cannot increase to arbitrarily large voltages. To accommodate larger offset capacitances, C_{Ref} can be increased, but this will consume more power, increase the noise, and reduce output bandwidth, as larger capacitors will now need to be charged up each reading [Kaa09]. Larger capacitances can also be accommodated by increasing C_F, but this will decrease system resolution, as the output

voltage will become less sensitive to changes in the sensor. Conversely, the input voltage, V_p, can be adjusted to trade resolution for range without any changes to the circuit hardware. Even with these limitations, commercially available charge integrators can deliver a bandwidth of up to 1 kHz and a resolution of 1 fF/code over a full-scale range of 0-45 pF at <500 μW of power [Sil11].

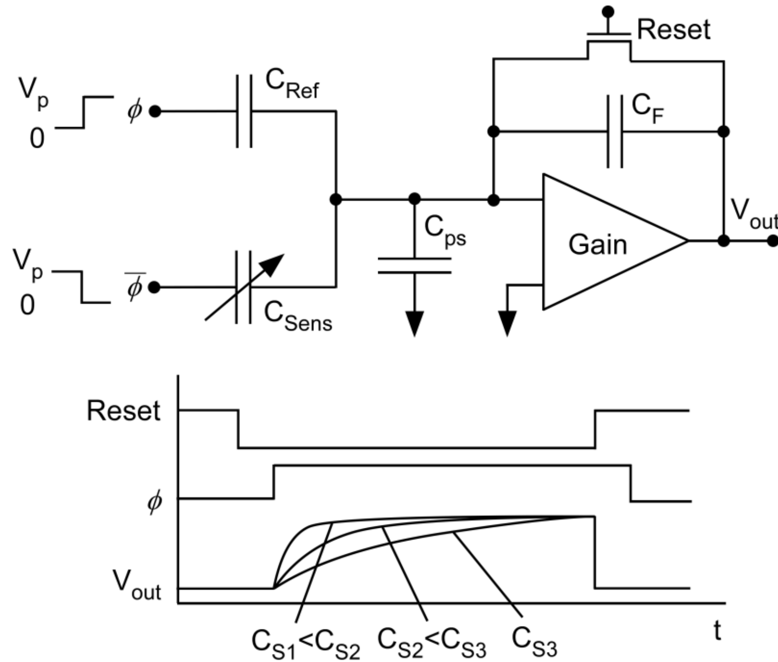

Fig. 1.5: Switched capacitor charge integrator circuit and operating voltage waveforms [Gia06].

$$V_{out} = \frac{V_p(C_{Sens} - C_{Ref})}{C_F} \tag{1.1}$$

One way to reduce a major source of offset and parasitic capacitances is with the use of insulating dielectric substrates [Cho92]. Research into dielectric substrate sensors has been focused primarily on conventional bulk silicon micromachining with the dissolved wafer process (DWP), utilizing anodic bonding of glass substrates and silicon diaphragms [Gia92]. However, it requires relatively large anchor sites for bonding [Cha01] and a lengthy bulk silicon dissolution. A benchmarking table of dielectric substrate sensors is given in Table 1.1.

Table 1.1: Comparison of capacitive pressure sensors utilizing dielectric substrates

Ref.	C_0 [pF]	Full-scale Range [kPa]	Diaphragm Size [mm]	TCO [ppm/°C]	T. Resp. [fF/°C]	Max. Temp.	Mask Steps
Cho92	6.0	1.5	2.1 × 2.1	841	4.55	200°C	6
Cha88	0.5	70	0.3 × 0.55	-3071	-1.55	50°C	4
Par00	3.75	1500	ø2.0	405	1.36	300°C	3
Cha01	8.34	13.3	6 || ø1.0	3900	32.5	70°C	8

Extended full-scale range capacitive pressure sensors have been previously investigated using a variety of substrate materials, but none have been able to achieve a sufficient range, resolution, and/or size. Silicon carbide (Si-C) substrate sensors have been investigated for their extremely high temperature tolerance, but have been limited in full-scale range [Che08, Jin11]. One sensor utilizing a flexible PET substrate was able to achieve a full-scale range of 18 MPa but at the cost of increasing the size to over 1600 mm^2 [Nar12]. A summary is given in Table 1.2.

Table 1.2: Comparison of capacitive pressure sensors with extended full-scale range

Ref.	Substrate	Size [mm^2]	C_0 [pF]	Range [MPa]	Max. Temp.	Avg. Response	Resolution (1 fF/code)	Resolution [bits]
Che08	Si-C	4.5×4.5	8.3	5	300°C	0.6 fF/kPa	1.65 kPa	11.6
Jin11	Si-C	30×20	9.8	5	500°C	0.2 fF/kPa	4.34 kPa	10.2
Nar12	PET	40×40	26	18	20°C	0.6 fF/kPa	1.65 kPa	13.4

Commercial Pressure Sensors:

While commercialized capacitive pressure sensors may not be as advanced as those in academic research, they are worth examination to explore what is possible using fully matured technology which must balance both performance and yield. One commercial pressure sensor that meets the necessary output and size requirements for microsystem integration is a capacitive MEMS sensor by Murata (SCB10H-B250) [Mur13], which measures $1.4 \times 1.4 \times 0.85$ mm^3, has a single crystal silicon diaphragm, average capacitance response of 2.6 fF/kPa (resolution of 0.40 kPa (0.05 psi) assuming readout electronics resolution of 1 fF/code), but a full-scale range of only 2.5 MPa (360 psi), eliminating it as a usable device for downhole applications.

Another commercial capacitive pressure sensor is the E8.0T [Mic08] produced by Microfab of Germany. It is fabricated on a dielectric fused silica substrate with a polysilicon diaphragm, measures $1.2 \times 0.6 \times 0.5$ mm^3, and has a capacitance response of 13.1 fF/kPa (resolution of 0.077 kPa (0.01 psi) at 1 fF/code); however, this comes at the cost of an even further reduced full-scale range of 0.8 MPa (115 psi), rendering it unfit for downhole applications.

A larger commercial capacitive MEMS pressure sensor capable of reading pressure to the full 50 MPa full-scale range is currently in development by Openfield™ Technology. It consists of both sensor and readout electronics in a self-contained package measuring ø8 × 14 mm. It can operate up to 125°C and 100 MPa (14,500 psi), and is capable of sensing pressure with an accuracy of 10.3 kPa (1.5 psi) when the proprietary electronics are used. It can also be integrated into a flowable "Smart ball" for harsh environmental sensing which has an outer diameter of ø50.8 mm [Ope13]. Due to the sensing element and protective packaging's relatively large size, though, it cannot fit into the centimeter scale openings created by the fracturing method of gas and oil extraction. Sensor summary given in Table 1.3 and Fig. 1.6.

Table 1.3: Commercial capacitive pressure sensor range and resolution comparison

Ref.	Size [mm^2]	C_0 [pF]	Range [MPa]	Max. Temp.	Avg. Cap. Response	Resolution (1 fF/code)	Resolution [bits]
Mur13	1.4 × 1.4	7.3	2.5	125°C	2.64 fF/kPa	0.40 kPa	12.7
Mic08	1.2 × 0.6	9.8	0.8	50°C	13.1 fF/kPa	0.08 kPa	13.7
Ope13	ø8 × 14	50	100	125°C	---	10.3 kPa	13.2

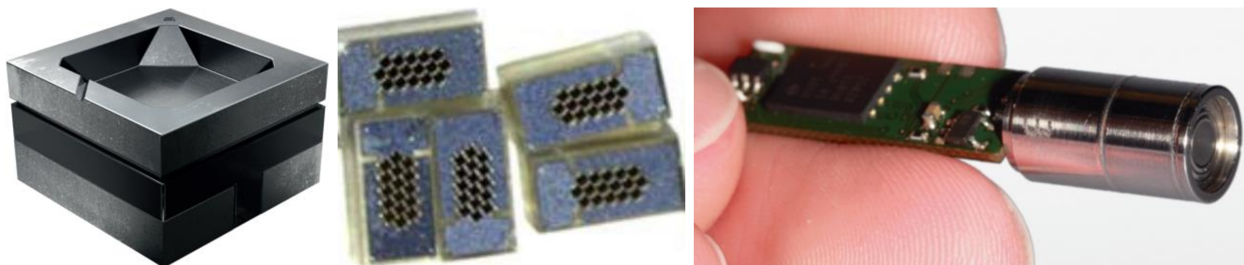

Fig. 1.6: Optical images of the Murata [Mur13], Microfab [Mic08], and Openfield [Ope13] pressure sensors, left to right.

A comparison all sensors described above to the Sapphire18 pressure sensors is given in Table 1.4. Additionally, a plot comparing the ratio of the full-scale capacitance change to the offset capacitance against sensor size is shown in Fig. 1.7. It can be seen that the ø100 µm Sapphire18 devices show both the largest dynamic range and ratio of full-scale output capacitance change to offset capacitance (>6.0), achieving this in a device volume of <1.0 mm^3.

Table 1.4: Commercial capacitive pressure sensor range and resolution comparison

Ref.	Size [mm^3]	C_0 [pF]	Cap. Rsp. [fF/kPa]	Sensitivity [ppm/kPa]	Range [MPa]	Resol. [kPa] (1 fF/code)	Resol. [bits]	TCO [ppm/°C]
Cho92	2.2	6.0	4575	762k	0.001	0.0002	12.6	841
Cha88	0.15	0.5	5.47	10.9k	0.04	0.183	7.8	-3071
Par00	0.17	3.75	1.50	400	1.5	0.67	11.1	405
Cha01	3.0	8.34	231.4	27.7k	0.01	0.004	11.2	3900
Che08	20	8.3	0.61	73	5.0	1.65	11.6	-
Jin11	1200	8.0	0.23	29	5.0	4.34	10.2	-
Nar12	1600	26	0.61	23	18	1.65	13.4	-
Mur13	1.67	7.3	2.64	362	2.5	0.40	12.7	560
Mic08	0.6	9.8	13.1	1340	0.8	0.08	13.7	-
Ope13	700	50	0.10	2	100	10.3	13.2	-
18C100	**0.7**	**3.6**	**0.45**	**125**	**50**	**2.22**	**14.5**	**420**

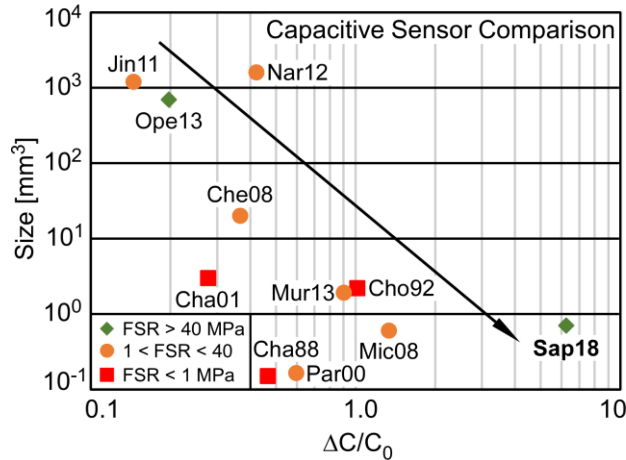

Fig. 1.7: Comparison of capacitive sensor size and ratio of full-scale capacitance change (ΔC) to offset capacitance (C_0).

1.3 Focus of this Work

Sapphire Substrate Process Design:

A surface micromachining process utilizing dielectric sapphire substrates was investigated in an effort to reduce parasitic and offset capacitances and temperature dependency, while focusing on improving sensor performance and yield. Additionally, efforts addressing system-level integration of the pressure sensors into autonomous microsystems were made, setting specific device size, full-scale range, and maximum temperature requirements. These sensors were packaged into custom microsystems and tested in both laboratory and field environments.

Process Scalability and Throughput Improvements:

With the successful fabrication of high yield, low parasitic capacitance sapphire substrate pressure sensors and their integration into microsystems, effort focusing on process modification for large scale system integration to address integration deficiencies was studied. Process improvements which allowed for increased scalability (including commercial die singulation and automated PCB assembly) were integrated into the process.

Process Refinement for Full-scale Range Enhancement:

Further process enhancement was completed by co-designing devices and process parameters which allowed for sensor designs with an extreme span (>1000×) of full-scale range designs by altering only the sensor diameter. Devices have been tested at pressures and temperatures of up to ≥50 MPa (7,250 psi) and 200°C, representing downhole environments, demonstrating <7.0 kPa (<1 psi) resolution. Devices designed to operate over a much lower full-scale range of ≤50 kPa (≤350 Torr), representing biomedical applications, have been tested and demonstrate a resolution of <80 Pa (<0.6 Torr).

Passive Wireless Pressure Sensing:

While the capacitive pressure sensors have been developed primarily for active microsystems, there may be situations where a wired connection to the readout circuitry is not possible. A passive wireless pressure monitoring system utilizing short-range inductive coupling has been developed to evaluate the performance of the sapphire substrate sensors in this use-case. Pressure monitoring within the GI tract has been targeted; an *in situ* resolution of 1.6 kPa (12 Torr) at an interrogation range of 6 cm and has been achieved through conductive saline. A practical application of the sensor has been demonstrated *in vivo*, being ingested and successfully interrogated in a canine model to monitor stomach pressure for over two days.

Research Goals:

1. Develop a surface micromachining fabrication process for capacitive pressure sensors. Utilize dielectric substrates to minimize parasitic and offset capacitances and temperature coefficients. Identify and address limitations that constrain yield and performance, focusing on interactions between equipment configurations, process integration, and sensor design.
   1.1. Utilize dry, low temperature (≤400°C) fabrication techniques and tools to permit a reduction in chemical waste and fabrication cost, where possible.
2. Design capacitive pressure sensors which can accomplish sensing in downhole environments for natural gas and oil exploration that can meet system level requirements for full-scale range (≥50 MPa, ≥7,250 psi), temperature (≥125°C), resolution (≤10 bit: <50 kPa (<7 psi) @ 1 fF/code system resolution), and sensor size (≤$2 \times 1 \times 0.5$ mm^3).
3. Further enhance process by co-designing devices and parameters to permit sensor designs with an extreme span (>1000x) of full-scale range options while simultaneously improving upon the system integrability and singulation throughput. Fabricate devices on the same

wafer (by altering only sensor diameter) that demonstrate a full-scale range as high as ≥50 MPa (≥7,250 psi) while providing <7.0 kPa (<1 psi) resolution (representing downhole environments) to as low as ≤50 kPa (≤350 Torr) while providing <130 Pa (<1.0 Torr) resolution (representing biomedical applications).

4. Evaluate the sapphire substrate capacitive pressure sensor in a passive wireless pressure sensing system utilizing short-range inductive coupling to assess a use-case in which wired connection to a readout circuit is not possible.

    4.1. Use the reduced full-scale range sensors to monitoring pressure within the GI tract. Design this system to meet desired size (ø12 x 24 mm^3), resolution (≤130 Pa, ≤1 Torr), readout bandwidth (64 Hz), and interrogation range (≥10 cm) targets. Test the system in both controlled *in situ* (conductive saline) and *in vivo* (beagle canine model) environments.

1.4 Organization of Thesis

This thesis is divided into six chapters. Chapter 1 gives an introduction including literature reviews on pressure sensors and harsh downhole environmental sensing requirements.

Chapter 2 describes an initial investigation into a dielectric sapphire substrate surface microfabrication process, addressing both yield limiting fabrication and fundamental design issues encountered. Two iterations were completed, termed Sapphire15 and Sapphire16. The Sapphire15 process was able to achieve a diaphragm yield of >85% for all device diameters. The Sapphire16 process was designed to increase the capacitance response, managing to do so by over an order of magnitude. The TCO of these devices was measured to be less than 300 ppm/°C up to 200°C. The pressure sensors were demonstrated to be operational within custom microsystem units at pressures up to 50 MPa (7,250 psi) and temperatures up to 125°C.

Chapter 3 describes the continued investigation of sapphire substrate pressure sensors (Sapphire17), focusing on both yield and capacitance response enhancements that reduced the effectiveness of the Sapphire15/16 processes. The final singulated device yield was increased to >80% while simultaneously doubling the average sensitivity of the single diaphragm ø100 μm devices (63,000 ppm/MPa in Sapphire16 to 133,000 ppm/MPa in Sapphire17). Sensors were integrated into microsystems and tested in a brine well borehole to a depth of 1.3 km and successfully recorded environmental conditions reaching 12 MPa (1,750 psi) and 70°C.

Chapter 4 covers process improvements for increasing the capacitance response, scalability, and functionality by identifying process parameters for wide full-scale range capability, addressing sensor pad metallurgy to permit the use of high throughput commercial sensor mounting, and improving quality of die singulation with industrial facilities. Devices were created allowing for commercial singulation and automated PCB attachment while improving the resolution to <7.0 kPa (<1.0 psi) up to 50 MPa (7,250 psi) when integrated into the microsystem. Utilizing the same process parameters, sensors delivering a full-scale range of ≤50 kPa (≤350 Torr) providing <80 Pa (<0.6 Torr) resolution were fabricated. Device yield was better than 95% for the large full-scale range sensors.

Chapter 5 covers an evaluation of the capacitive pressure sensor in a passive wireless pressure sensing system (utilizing short range inductive coupling) to assess a use-case where a wired connection to the readout circuit may not be possible. Monitoring pressure within the GI tract was targeted, with size, resolution, interrogation range, and bandwidth set as primary goals. The system was limited by resistive losses in the pressure sensor. This shortcoming was mitigated by the use of a parallel dummy capacitor to reduce the equivalent series resistance of the passive element, trading a reduced frequency response for an improved quality factor and range. An *in situ*

(conductive saline environment) range and resolution of 6 cm and 1.6 kPa (12 Torr) over 35 kPa (263 Torr) was achieved. The sensor was evaluated in a practical application, successfully monitoring GI tract pressure *in vivo* in a canine model for two days.

Chapter 6 summarizes the findings and contributions of this work, and proposes future work for a further improvement of the passive sensing system described in Chapter 5, as well as a potential active system for dramatically improved sensing capabilities within the GI tract.

Appendices outline additional investigations of process development for RF MEMS switches and describe work on a first generation silicon substrate process, where multiple unaddressed microfabrication issues resulted in low diaphragm yield (≈25%), poor performance, high temperature coefficient offsets (≈25,000 ppm/°C), and large parasitic capacitances.

CHAPTER 2: Dielectric Substrate Surface Micromachining Process

This chapter describes the initial investigation of a dielectric sapphire substrate, surface micromachining process utilized to fabricate high performance capacitive pressure sensors with extremely low parasitic capacitance and temperature coefficients. The device diaphragms consist of dry plasma deposited dielectrics. Sensor electrodes are electrically insulated in order to permit over pressure protection and touch mode operation to extend full-scale range. Sensitivity and yield improvements are realized by overcoming fundamental process challenges, giving particular attention to the interplay between equipment limitations and device design. Average sensitivity of ø100 μm diameter sensors was demonstrated to be greater than 55,000 ppm/MPa up to 50 MPa (11 fF/MPa, C_0 ≈200 fF) and TCO was measured to be less than 300 ppm/°C up to 200°C. Successful device integration into custom microsystems was demonstrated, accurately tracking applied pressures and temperatures of up to 50 MPa and 125°C. Section 2.1 presents previous work which utilized dielectric substrates and surface micromachining to fabricate capacitive pressure sensors. Sections 2.2, 2.3, and 2.4 cover the proposed fabrication approach, FEA modeling, and process modifications implemented to increase device yield and sensitivity. Experimental results of fabricated devices are given in Section 2.5.

2.1 Dielectric Substrate and Surface Micromachining Process Overview

Utilizing dielectric substrates to reduce parasitic and offset capacitances has been previously explored, primarily through bulk silicon micromachining and the dissolved wafer process [Cha88]. However, this method requires dual wafer alignment and anodic bonding of silicon and glass, followed by dopant-selective bulk silicon dissolution in ethylene diamine and

pyrocatechol (EDP). As microfabrication techniques have evolved over the past three decades, though, the use of single wafer, dry surface micromachining processes have become more favored [Jae98] in order to reduce fabrication time, chemical waste, and cost.

One surface micromachining approach in which dielectric diaphragms were fabricated utilized sacrificial polysilicon to define diaphragm dimensions, silicon dioxide and silicon nitride structural materials, and achieved hermetic sealing with atomic layer deposition (ALD) Al_2O_3 [An14]. With the addition of embedded metal electrodes, microdischarge-based [Luo15] and capacitive (Appendix B) pressure sensors could be realized. However, these processes employed conductive silicon substrates with through-wafer lead transfer for size reduction, resulting in both high parasitic capacitances and temperature coefficients (25,000 ppm/°C).

2.2 Sapphire Substrate Surface Micromachining Process

This work describes a microfabrication process that successfully combines dielectric substrates with dry surface micromachining methods to fabricate pressure sensors with no conductive structural materials (Fig. 1.1), effectively eliminating any parasitic capacitances and permitting an extreme reduction in both offset capacitance and temperature dependence. This was accomplished through in-depth process development and modification of the silicon substrate surface micromachining process outlined above (and detailed in Appendix B) to address previously unresolved yield and response limiting issues while also focusing on incorporating design features required for microsystem integration.

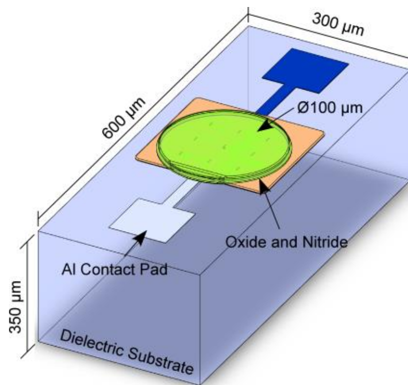

Fig. 2.1: (a) Model of the pressure sensor on a sapphire substrate.

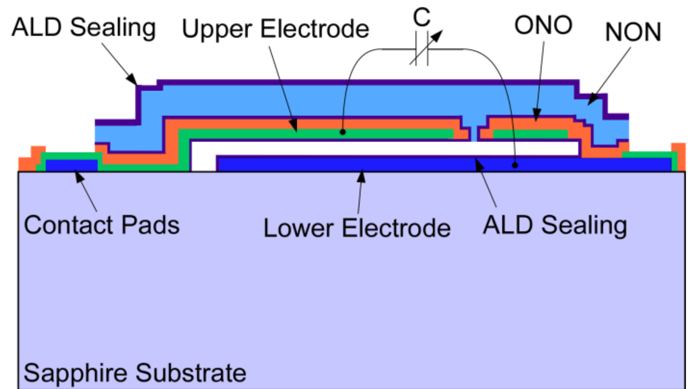

Fig. 2.1: (b) Cross section of the capacitive pressure sensor on a sapphire substrate.

The first major process adaptation was the switch to a dielectric substrate. There are many options available, but the three most common are fused silica, borosilicate, and sapphire. While any non-conductive substrate would permit a reduction in stray capacitances (in comparison to conductive substrates), the thermal expansion coefficient difference between the substrate and diaphragm materials must be considered in order to reduce temperature dependency. The primary material of the sensor diaphragm is silicon nitride, with an estimated thermal coefficient of expansion (TCE) of approximately 5 ppm/°C; fused silica has a TCE of ≈0.5 ppm/°C, borosilicate ≈3.0 ppm/°C, and sapphire ≈6.0 ppm/°C [Gad01]. Due to the relatively large thermal expansion difference between fused silica and nitride, it was not chosen. While borosilicate is a relatively close TCE match, there were concerns of sodium ion contamination in the deposition tools. This left sapphire, which is both a good TCE match to nitride and extremely inert, presenting no concerns of tool contamination and offering enhanced harsh environment survivability.

The second major revision was the removal of the thru-wafer isolation trenches, necessitating the use of front side contact pads; this has a great impact on the offset and parasitic capacitances worth quantitatively exploring. The simulated active C_0 of the 3 µm gap, ø100 µm diameter silicon substrate device (Fig. B.1) was less than 25 fF; however, the large parallel plate capacitors resulting from through-wafer lead transfer exhibited an additional (simulated) nominal

C_0 of ≈400 fF, not including any fringe parasitic capacitances coupled to the conductive substrate sidewalls. While utilizing front side contact pads will slightly increase the device volume (from a theoretical minimum of ≈0.005 mm^3 to ≈0.010 mm^3), the final sensor designs would still be much smaller than the electronics, battery, and packaging (measuring ≈$9 \times 9 \times 7$ mm^3) and any conductive sidewall incurred parasitic capacitances are eliminated.

This initial dielectric sapphire substrate, surface micromachining process consists of 5-mask lithographic microfabrication steps. Two major versions of the process sequence were completed and evaluated, designated Sapphire15 and Sapphire16. The final version of Sapphire15 (Fig. 2.2) was the culmination of a series of progressive improvements to yield problems that ultimately resulted in a diaphragm yield >85%. The Sapphire16 process (Fig. 2.3) resulted from the initiation of new steps to enhance performance. While Sapphire16 did not achieve the same yield as Sapphire15, the device capacitance response was improved by over an order of magnitude.

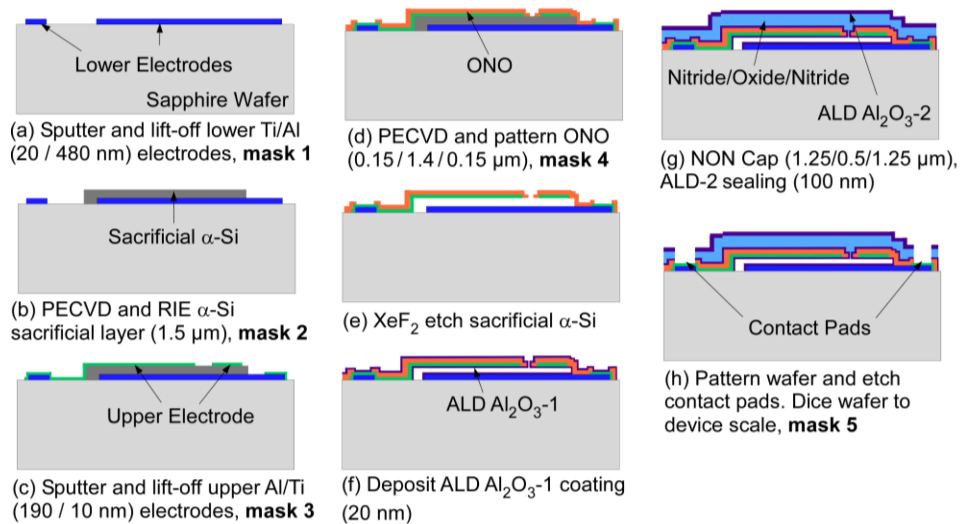

Fig. 2.2: Process sequence for the Sapphire15 high-yield process.

<u>Sapphire15 Process Description:</u> The first step of this process is to define the lower electrodes using evaporation and liftoff of a titanium/aluminum stack, where Ti is utilized as an adhesion promoter. The sacrificial layer for diaphragm diameter and inter-electrode cavity gap is

formed with a 1.5 μm-thick layer of Plasma-Enhanced Chemical Vapor Deposition (PECVD) low stress amorphous silicon (α-Si), which is patterned with an isotropic dry etch. The upper electrode is defined using sputtering and lift-off for conformal step coverage over the α-Si. Then, a stack of PECVD ONO (oxide-nitride-oxide, 0.15 μm/1.4 μm/0.15 μm) is deposited to form the diaphragm, and patterned with etchant access slots. The sacrificial α-Si layer is etched by gas phase XeF_2, which provides isotropic etching and high selectivity to other exposed materials (oxide, Al_2O_3, and aluminum). Atomic layer deposition (ALD) of Al_2O_3 is used to insulate the electrodes and permit touch mode operation to extend the full-scale range. (The concept of touch mode operation exploits the fact that the substrate provides a natural over-pressure stop that can prevent rupture of the diaphragm [Ko96].) The sealing of the etchant access slots and diaphragm is performed by a second stack of PECVD nitride and oxide, followed by ALD of Al_2O_3 to create a hermetic sealing of the diaphragm (as PECVD materials can be slightly porous) [An14].

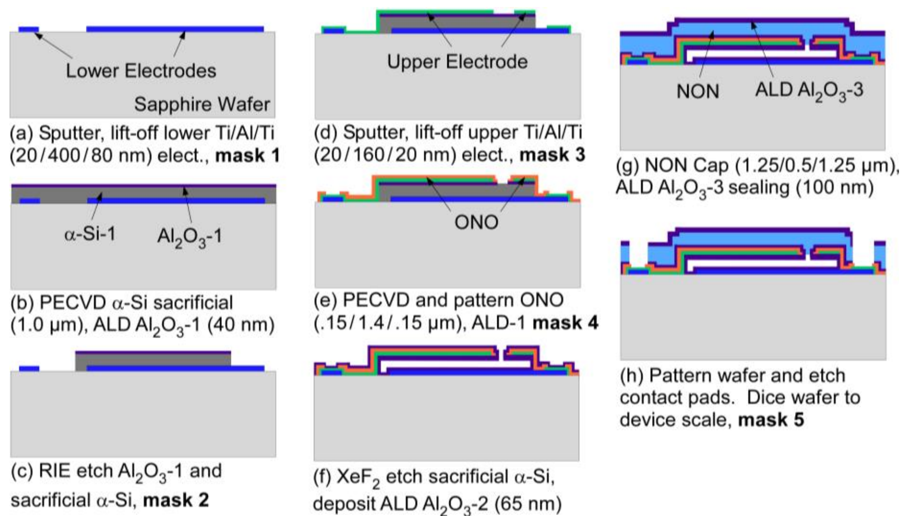

Fig. 2.3: Process sequence for the high sensitivity Sapphire16 process.

Sapphire16 Process Description: The Sapphire16 process is similar to the Sapphire15 process, but differs in three major aspects: (1) the use of Ti barrier layers between the Al electrodes and the α-Si sacrificial layer; (2) the nominal inter-electrode cavity gap, reduced from 1.5 μm to 1.0 μm; and (3) the inter-electrode layer of ALD Al_2O_3 insulation, which was previously deposited

after the sacrificial etch, is now supplemented by another layer of Al_2O_3 after the α-Si deposition. The Ti barrier layers allow the cavity surface roughness to be substantially reduced by eliminating the Al spiking that occurs as a consequence of inter-diffusion between Al and α-Si. The reduction in the thickness of the sacrificial α-Si layer is intended to compensate for a loss of capacitance response due to the slight increase in diaphragm thickness required to increase yield after the XeF_2 release. In an effort to correct non-uniform ALD Al_2O_3 deposition in the cavity, an additional layer of ALD Al_2O_3 was deposited after the α-Si and prior to the upper electrode deposition.

2.3 Sapphire15 and Sapphire16 Fabrication Modifications and Results

Fabrication results at important points of the process sequence and solutions to encountered problems are highlighted below.

Mask 1: Lower Electrode

The Sapphire15 and Sapphire16 processes begin with deposition and definition of the lower electrode directly onto a sapphire substrate. To define the lower electrode, evaporation and liftoff were used in both Sapphire15 and Sapphire16. The metal stack of the lower electrode for the Sapphire15 was simply a Ti/Al layer, where the Ti layer served as an adhesion promoter between the sapphire substrate and the Al electrode, causing the Al electrode and α-Si sacrificial layer to be in direct contact. Because the highest process temperature encountered after the α-Si deposition (and before its removal) was 400°C, Al spiking was considered to be non-relevant, as the eutectic temperature between pure Al and single crystal silicon is ≈577°C [Han58]. However, it was empirically observed after the XeF_2 etch in Sapphire15 that Al spiking had occurred (Fig. 2.4). This is thought to be due to the lower quality and presence of impurities in the α-Si [Yan07], which allowed the aluminum and silicon to inter-diffuse at significant rates [Ans69] even at the relatively low temperature of 400°C [Jae02].

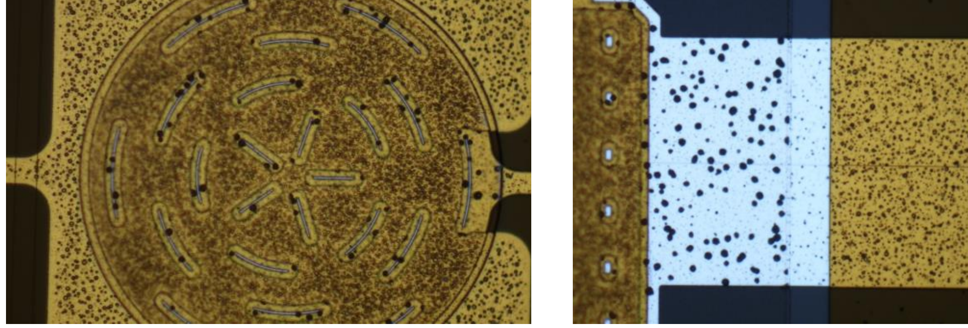

Fig. 2.4: Al spiking (large black dots) can be seen under an unsealed released sensor cavity (left) and exposed (right) on a test structure with no ONO capping deposited over the α-Si layer.

The Al spiking resulted in undesired surface roughness inside the cavity, which caused shorting and reduced capacitance response when the devices were under applied pressure. When operating in touch mode, the insulating ALD Al_2O_3 layer ideally prevented inter-electrode shorting; however, the topography of the Al spikes and the deposition conditions of the ALD Al_2O_3 prevented the Al spikes from being properly insulated. When devices did not short out, the output signal was greatly reduced, as the spikes prevented the diaphragms from moving downward, resulting in a chamber air gap set by the height of the spikes.

This was corrected in the Sapphire16 process with a two-fold approach: preventing the Al spikes from being formed by using Ti barrier layers between the Al electrodes and the α-Si sacrificial layer, and inserting an additional layer of ALD Al_2O_3 insulation beneath the upper electrode metal. The Ti layer thickness required was determined by the consumption rate of Ti at both the Al and α-Si at the interfaces [Nic81]. These rate relationships are given in equations (2.1) and (2.2), where *k* is Boltzmann's constant and *T* is temperature in Kelvin.

$$\text{Al/Ti Reaction Rate: } 1.5x10^{15} exp\left(\frac{-1.85\ eV}{kT}\right) \left[\text{Å}^2/_{sec}\right] \quad (2.1)$$

$$\text{Si/Ti Reaction Rate: } 4.0x10^{9} exp\left(\frac{-1.3\ eV}{kT}\right) \left[\text{Å}^2/_{sec}\right] \quad (2.2)$$

As the Si, Ti, and Al interact, they diffuse into each other, forming the compounds $SiTi_2$ and $TiAl_3$. The lower electrode is exposed to an elevated temperature (400°C) for approximately

45 minutes (including the substrate heating time for PECVD ONO depositions), causing the Ti/α-Si interface to create a layer of $SiTi_2$ approximately 5 nm thick, whereas the Ti/Al interface forms a layer of $TiAl_3$ approximately 35 nm thick. Using a 2x safety factor and assuming that all growth of these interfacial layers occurs into the Ti layer (the worst case scenario), the lower electrode Ti barrier must be at least approximately 80 nm thick to prevent any unwanted surface roughness from occurring on the metal surface. Whereas the upper electrode is also exposed to the elevated temperatures, in the Sapphire16 process it is insulated from the α-Si by a layer of ALD Al_2O_3, and does not require an additional barrier.

It should be noted that the interaction at the Ti/α-Si interface is substantially slower, accounting for only ≈10% of the consumed Ti. It was shown experimentally that the interaction of Ti and α-Si does not result in substantial increased surface roughness, even with the non-zero interaction predicted. Evaporated Ti/Al/Ti lower electrode and α-Si layers were defined (with areas of the lower electrode both covered and uncovered by the α-Si) on a dummy wafer and then subjected to 400°C for 60 minutes in a thermal oven to simulate the deposition temperature cycling encountered during the PECVD of the ONO diaphragm. The α-Si was then removed using XeF_2 and root mean square (R_q) surface roughness measurements were taken on the electrode surfaces. As shown Table 2.1, there was only a slight increase (≈1.5 nm) in roughness at the Ti/α-Si interface and negligible change in the roughness of the bare Ti capped electrode.

Table 2.1: RMS (R_q) Surface Roughness Measurements

Electrode (as deposited)	Ti/α-Si Interface (post 400°C, α-Si removed)	Electrode (post 400°C, open field)
69 Å	85 Å	63 Å

Electrode ALD Insulation

Initially, a 20 nm ALD Al_2O_3 electrode insulation was deposited after the XeF_2 sacrificial etch. This allowed *in situ* insulation of the electrodes for touch mode operation without the need

for an extra lithography step. However, in order for Al_2O_3 to coat the electrodes, ALD precursor gases needed to enter through the small etchant access slits ($0.8 \times 5.0\ \mu m^2$) and react inside the thin chamber (1.5 µm). This small slit and chamber gap increased the impedance of the precursor gas flow, resulting in incomplete ALD electrode coating, causing yield loss due to device shorting in touch mode. This also resulted in an uneven and inconsistent deposition of ALD on the electrodes, causing the touch mode capacitance response to deviate from the ideal simulation.

In the transition from Sapphire15 to Sapphire16, to increase the repeatability of the inter-electrode insulation, the ALD Al_2O_3 deposition step was initially moved from after the XeF_2 etch (deposited *in situ* inside the released cavity) to directly after the definition lower electrode (on an open field) to a thickness of 40 nm. This would not increase the thickness of the Al_2O_3 between the electrodes when in touch mode, as the upper electrode would now be uninsulated. However, this layer of ALD was found to severely compromise the adhesion of the α-Si sacrificial layer. In order to maintain low stress and prevent crystallization, the α-Si is deposited at 250°C; the PECVD of the dielectric diaphragm layers is performed at 400°C to increase uniformity and film quality. This increase in temperature, combined with the ultra-smooth and inert layer of ALD Al_2O_3, caused the α-Si to delaminate and bubble, Fig. 2.5.

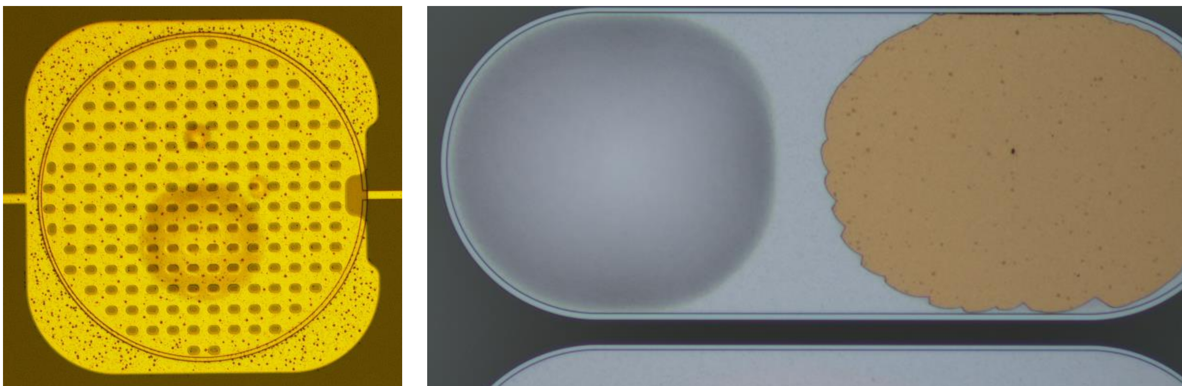

Fig. 2.5: α-Si delamination from underlying ALD Al_2O_3 after temperature cycling to 400°C.

In an attempt to correct for this delamination problem, the ALD Al_2O_3 insulation layer was deposited immediately after the α-Si deposition (immediately followed by a thin (10 nm) layer of Ti to promote adhesion between the ALD Al_2O_3 and the upper Ti/Al electrode). The placement of the ALD Al_2O_3 insulation at this step in the process had the added benefit of not requiring the use of an extra lithography step, as the masking step previously used to solely define the α-Si could be used to define both the ALD Al_2O_3 sealing and α-Si simultaneously.

Once the fabrication was completed, though, it was found that the devices would become electrically shorted under applied pressure (and remain shorted after pressure release). This failure mechanism was likely due to inadequate adhesion of the ALD Al_2O_3 to the diaphragm "ceiling". When pressure was applied, the ALD would delaminate and pull part of the upper electrode with it, causing it to touch the uninsulated lower electrode. Due to the nature of ALD Al_2O_3, it has very good adhesion to materials it is deposited onto (as it is "grown" in a two-step process directly on the material surface), but most materials have very poor adhesion when deposited onto ALD (due to its extremely smooth and non-reactive surface) [Puu05]. Because the ALD was deposited onto the α-Si (which is later removed to define the sensor cavity) and the upper electrode and dielectric diaphragm materials were deposited onto the ALD, which left a weakly attached upper electrode and ALD layer that was prone to failing under the strain of diaphragm deflection.

To correct for this failure mode in the Sapphire16 process, a second layer of ALD was deposited immediately after the XeF_2 etch of the α-Si to more securely attach the initial ALD and upper electrode to the diaphragm, as well as to provide further electrode insulation for the lower electrode to prevent any more shorting of devices. While this resulted in uneven electrode insulation, it allowed for the devices to yield without shorting under applied pressure and could be accurately modeled as a linear gradient of ALD thickness in the matching simulations.

Mask 2: α-Si Sacrificial Layer

The sacrificial α-Si layer was initially defined using DRIE, resulting in vertical sidewalls and several adverse side effects. Even when highly conformal sputtering was used to define the upper electrode, a disconnect was found to occur in the lead due to the limited step coverage on the vertical α-Si. Secondly, the relatively tall sidewall tended to accumulate photoresist at the bottom corner, exacerbating the disconnect problem if undeveloped residual photoresist remained on the wafer prior to metallization. Sharp inner diaphragm edges are also undesirable for device operation, as a smoother transition from a sloped sidewall can reduce the local stress concentration and avoid device failure due to cracking of the diaphragm during operation.

A custom isotropic RIE etch was created by tuning the fluorine/oxygen gas mixture ratio, plasma chamber pressure, and electrode bias in a parallel plate RIE system. The most important factor in determining the sidewall sloping (degree of isotropy in the etch) is the $O_2/(CF_4 + O_2)$ ratio [Mog78]. As the O_2 concentration increases, the etch rate first increases and then decreases beyond a certain ratio. This is due to the fact that with increased oxygen, a $Si_xO_yF_z$ film (etching inhibitor) forms on the surface of the silicon, causing the concentration of the fluorine atom (etching species) to dilute (as it is used in to form the $Si_xO_yF_z$ film). This fluorine dilution encourages isotropic etching, as the vertical etching rate is reduced, allowing more time for the α-Si to be etched laterally. Increased chamber pressure decreases the mean free path of the ions in the plasma, resulting in a loss of ion directionality, further increasing the isotropy.

The baseline parameters for the characterization were CF_4 at 40 sccm, O_2 at 2 sccm, 80 W power and 100 mTorr chamber pressure. The first parameter tested was the CF_4/O_2 ratio, as it appeared to be the most critical parameter for creating an isotropic etch, however, as the O_2 concentration increased, the etch rate of the photoresist mask was also significantly increased,

resulting in total mask etch before the silicon etch was completed. The final etching parameters were 10% O_2 (CF_4 42 sccm / O_2 4.7 sccm) with a 150 mTorr chamber pressure at 80 W power. The final sidewall profile can be seen in Fig. 2.6, with an undercut width that is similar to the thickness of the α-Si layer. Due to the isotropic etch, the drawn dimension of the α-Si layer must be larger than the fabricated diameter; this was taken into account with a modified mask.

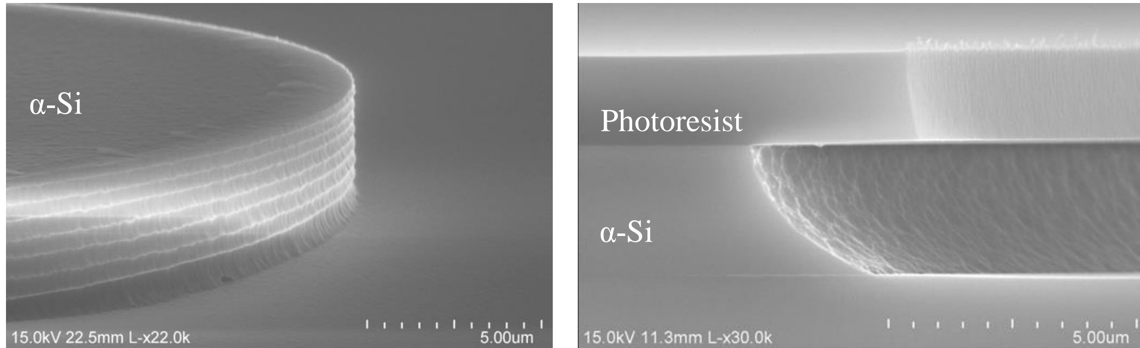

Fig. 2.6: α-Si definition with DRIE (left) and isotropic RIE (right).

<u>Mask 3: Upper Electrode</u>

Initially, the upper electrode was defined with image reversal and lift-off. However, the sputtered metal provided sufficient coverage of the photoresist sidewalls such that metal "ears" were formed after lift-off. Traditionally, liftoff patterning is performed with non-conformal evaporation to prevent PR sidewall metallization. In order to obtain adequate α-Si step coverage, though, sputtering was necessary (and even then, an isotropic etch for sloped sidewalls was required to ensure a reliable connection). Due to the conformal nature of sputtering metallization, the metal coated the sidewall of the PR, leading to unwanted metal roughness at the edges of the PR after lift-off. Instead of image reversal, lift-off-resist (LOR) and thickly spun on PR (SPR 220 3.0 at 2000 rpm for 4 μm thickness) was used to obtain much deeper undercut to prevent the sputtered metal from depositing on the sidewalls, allowing for a gently sloping metallization profile. SEM micrographs of the "ear" formation due to sidewall metallization and the corrected metallization with LOR can be seen in Fig. 2.7.

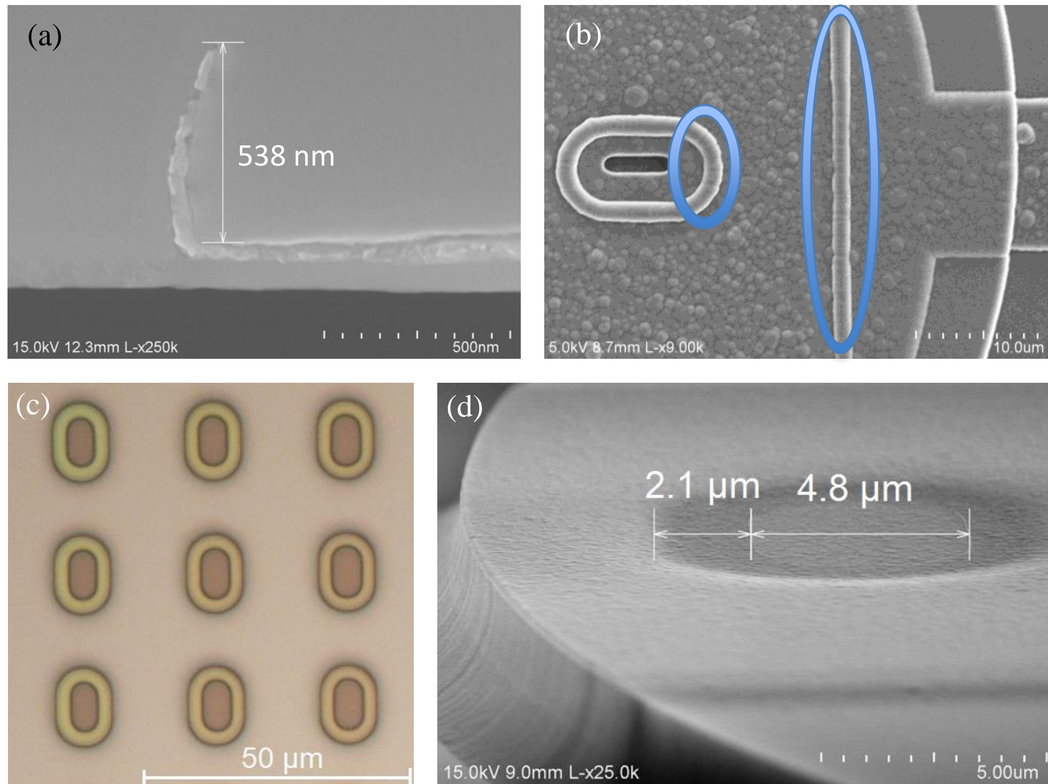

Fig. 2.7: (a) Metal "ear" formation with sputtering and image reversal (post ONO deposition) cross section, (b) top view. (c) Deeply undercut LOR and (d) corrected metallization profile.

Mask 4: ONO Diaphragm and Etchant Access Hole Definition

It was found that the diaphragm release and sealing were the source of many yield limiting issues, leading to device failure from layer delamination at elevated temperatures, diaphragm cracking due to mechanical forces during tool pumping, and shear forces of the capping dielectrics.

As Sapphire15 was being developed, the first step before processing began was the re-characterization of film stress in the α-Si, oxide, and nitride layers, as not only did the substrate change from silicon (CTE ≈3.5 ppm/K) to sapphire (CTE ≈6.0 ppm/K), but a new PECVD tool (Applied Materials Precision 5000) with better reliability was used. It offered an extra parameter (shower head / susceptor height) that could be modified to adjust the stress levels. Through a modification of both the susceptor height and applied RF power, the silicon nitride stress could be tuned from highly compressive (-300 MPa) to low tensile stress (80 MPa) without adjusting the

temperature and gas flow mixtures. This resulted in a higher quality layer of silicon nitride closer to the stoichiometric ratio of Si_3N_4 than possible with the older PECVD tool, in which the temperature and gas mixtures needed to be substantially altered in order to achieve a stable low stress recipe. The final recipe was a chamber pressure of 4.5 Torr, 250 W RF power (reduced from 415 W), susceptor height of 500 mils (reduced from 600 mils), SiH_4 flow of 180 sccm, N_2 flow of 2000 sccm, and NH_3 flow of 55 sccm. With a less silicon rich film (compared to the original nitride film used), it is attacked far less by XeF_2, leading to more reliable diaphragm creation.

The oxide stress was measured at -122 MPa compressive on sapphire, but its recipe (chamber pressure of 2.8 Torr, RF power of 125 W, showerhead spacing of 350 mils, SiH_4 flow of 54 sccm, and N_2O flow of 1200 sccm) was not modified, as this is a sufficiently modest value and only thin layers are used as protection for the nitride during the XeF_2 etch and stress balancing of the overall diaphragm. Careful control and monitoring of the stresses in all diaphragm layers is important, as large tensile stress values can severely compromise capacitance response and cause fractures at stress concentrations along the etchant access slits, whereas compressive stress can cause large diaphragms to buckle after release.

The next step is the release of the diaphragm structures with XeF_2 gas. However, they were very fragile, measuring only 1.1 µm thick and perforated with etchant access slits, resulting in a low yield of larger diaphragms after the XeF_2 etch. The small hydraulic diameter of the slits resulted in a large flow resistance for the gas that is purged during the process cycles of the XeF_2 etch tool. During these pump-purge cycles, a valve opens to an evacuated pipe, causing the chamber pressure to drop from 750 Torr to 50 Torr over less than 100 milliseconds. This negative impulse pressure caused the diaphragms to balloon outward past their breaking point, Fig. 2.8.

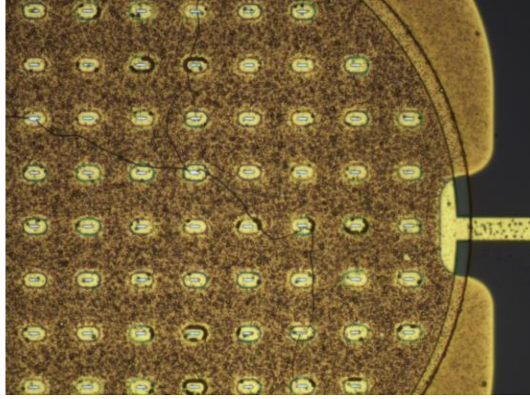
Fig. 2.8: Hairline fractures in an early version of a Sapphire15 process ø300 μm diameter device after being released.

Two fabrication changes and a tool modification were implemented to reduce this failure mode. Fabrication changes included thickening the ONO diaphragm and elongating the etchant access slits. As the stiffness of a diaphragm is proportional to the cube of its thickness (derived in equations (2.3-2.5), [Gia06]), by increasing it from 1.1 μm to 1.7 μm, the stiffness of this unsealed diaphragm during the XeF_2 etch was increased by nearly 270%, but the impact on the final device was a stiffness increase of less than 30% (diaphragm thickness increase from 4.6 μm to 5.0 μm). To improve the capacitance response due to the stiffness increase, the inter-electrode gap (α-Si thickness) was reduced to 1.0 μm in Sapphire16.

$$d_{center} = \frac{3 * \Delta P * (1 - \nu^2) * a^4}{16 * E * h^3} \tag{2.3}$$

$$stiffness, k = \frac{force}{deflection} = \frac{16 * (sensor\ area) * E * h^3}{3 * (1 - \nu^2) * a^4} \tag{2.4}$$

$$\frac{k_2}{k_1} = \frac{(h_2)^3}{(h_1)^3} \tag{2.5}$$

The second solution was to increase the length of the etchant access slots. While the width cannot be increased (resulting in additional PECVD deposition into the cavity), the length can be increased without causing any deposition to occur in the cavity during sealing. By extending the slots to ≈20 μm in length on larger diameter devices, the hydraulic resistance and outward ballooning effect was reduced. The modified etchant access holes can be seen in Fig. 2.9.

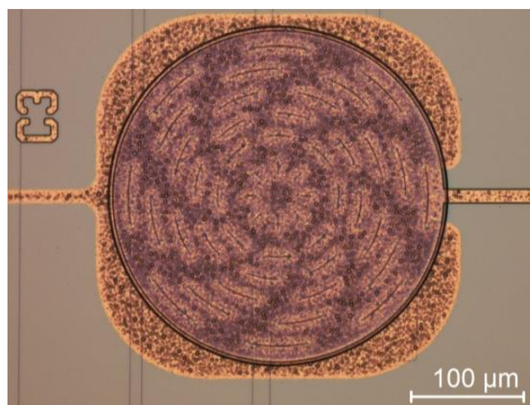

Fig. 2.9: Modified etchant access slits in a Sapphire15 ø300 μm diameter device.

The final correction was a tool modification, accomplished by installing a needle valve on the evacuation pipe closest to the etch chamber. This reduced the initial pressure drop to only 150 Torr (e.g. dropping from 750 Torr to 600 Torr) while the needle valve allowed for the slow evacuation of the remaining chamber pressure. These changes allowed all of the devices, regardless of diameter size, to remain intact after the XeF_2 etch.

After the diaphragms were released, they were sealed with PECVD dielectric. Initially, this was done with a single layer of nitride. While it had a relatively low characterized stress value, the shear force from a thick (3.0 μm) layer caused the larger diaphragms to peel up along the edges before sealing could be completed, shown in Fig. 2.10.

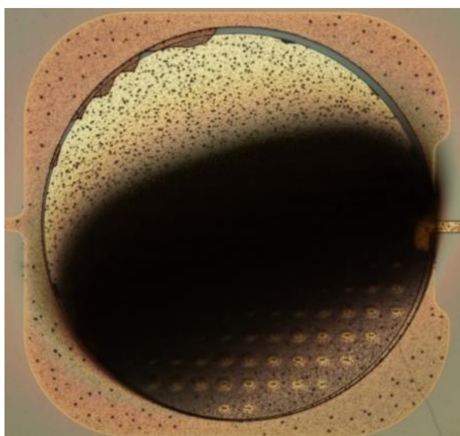

Fig. 2.10: Peeling and delamination of a ø300 μm diaphragm after 3.0 μm nitride deposition.

The shear stress was reduced by using a stress compensated nitride/oxide/nitride (NON) stack to seal the diaphragms. This interleaved oxide layer balanced the stress build-up of the nitride, preventing diaphragm delamination. When this final change was made in the Sapphire15 process, all device diaphragms ≥ø200 µm diameter had a yield of 85% while all ø100 µm diameter diaphragms had a yield of nearly 100%.

Mask 5: Contact Pad Definition

The final lithography step removes the deposited dielectrics from the contact pads. The wafer was patterned and dry etched with a transformer coupled plasma (TCP) reactive ion etch (RIE) LAM Research 9400 tool. The recipe was designed to etch both silicon dioxide and nitride at similar rates (measured at 2050 Å/min for PECVD silicon dioxide and 1750 Å/min for PECVD silicon nitride) using a C_4F_8 and SF_6 gas mixture of 45 sccm and 13.5 sccm, respectively.

The devices were then diced to the device level using conventional singulation methods. The standard dicing recipe resulted in large chipping and device loss when cutting through sapphire wafers. While the dicing streets between the devices provided a minimum of 250 µm of clearance, the dicing blade cut a channel approximately 230 µm wide with chipping extending up to an additional 75 µm, resulting in a necessary dicing street width of ≈400 µm. This amount of chipping was seen when the dicing recipe used a feed rate of 1 mm/s with 5 passes measuring between 3 mil - 6 mil and a blade spin speed of 24k rpm. The chipping can be seen in Fig. 2.11.

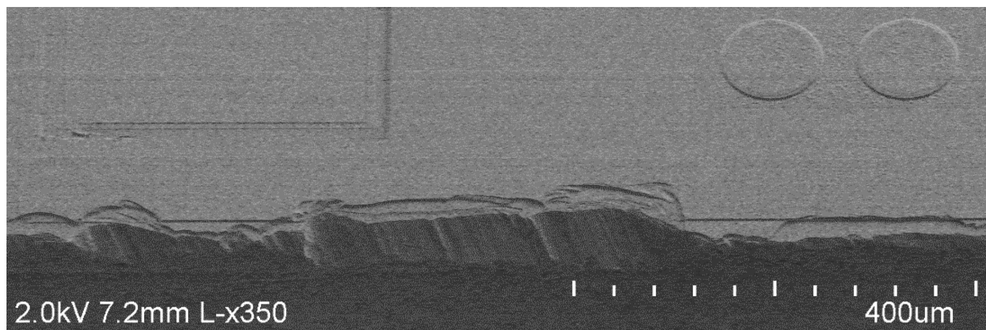

Fig. 2.11: Chipping and delamination of the devices caused by the dicing process.

To reduce the chipping to a minimum, the feed rate was reduced to 0.5 mm/s and the number of passes was increased to 8 measuring between 1 and 5 mil per cut. The spin speed of the blade had negligible impact on chipping. While this did increase the time required to dice the devices, it reduced the chipping to ≈20 µm, allowing for a much higher yield of singulated devices.

When all of these changes were implemented, the Sapphire15 process run showed a diaphragm yield of over 85%, but with a low capacitance response due to the cavity roughness. When fabrication changes were made to improve the response (resulting in a 10x increase), the yield lowered due to electrode delamination and device shorting.

Selected final devices are shown in the following figures, which compare Sapphire15 and Sapphire16. Fig. 2.12 shows SEM and optical micrographs of 4C100 devices from the Sapphire15 and Sapphire16 runs with improving surface roughness. Figures 2.13 and 2.14 show fully fabricated devices highlighting the improvement between Sapphire15 and Sapphire16 of the ø200 µm and ø300 µm devices. Fig. 2.15 shows a device diced to the size required for integration into the microsystems on a US penny.

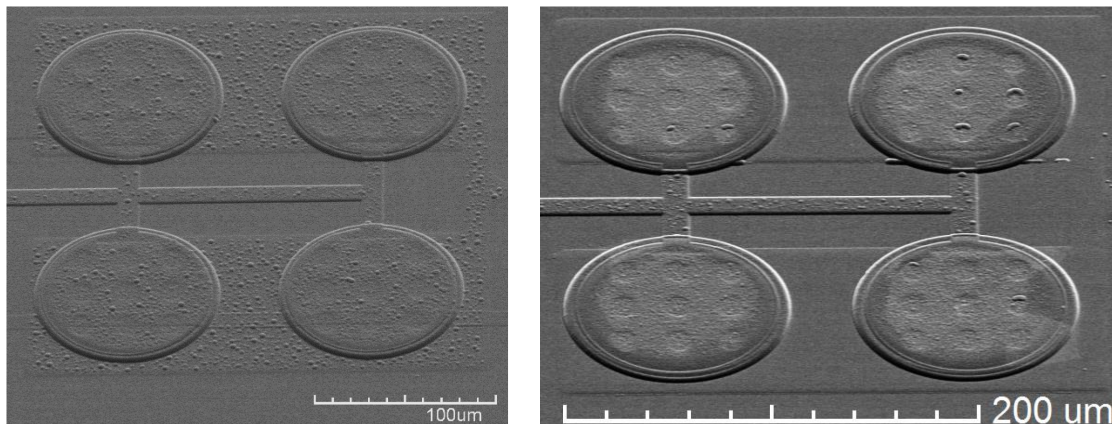

Fig. 2.12: (a) Fabricated 4C100 device (4 parallel connected ø100 µm devices); Sapphire15 showing surface roughness (left) and Sapphire16 (right).

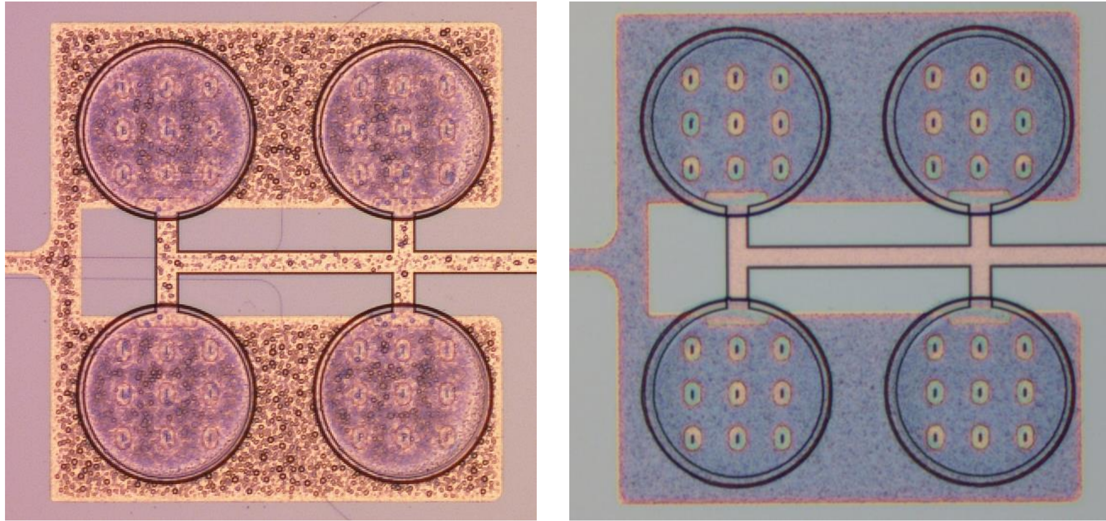

Fig. 2.12: (b) Fabricated 4C100 device (4 parallel connected ø100 µm devices) showing reduction of the surface roughness from the Sapphire15 (left) to the Sapphire16 (right).

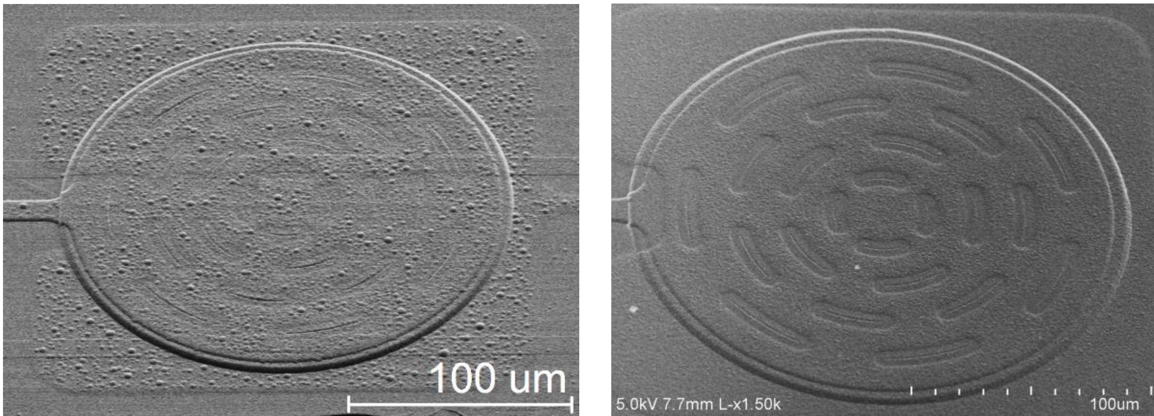

Fig. 2.13: Fabricated C200 (ø200 µm device) showing reduction of surface roughness from the Sapphire15 (left) to the Sapphire16 (right).

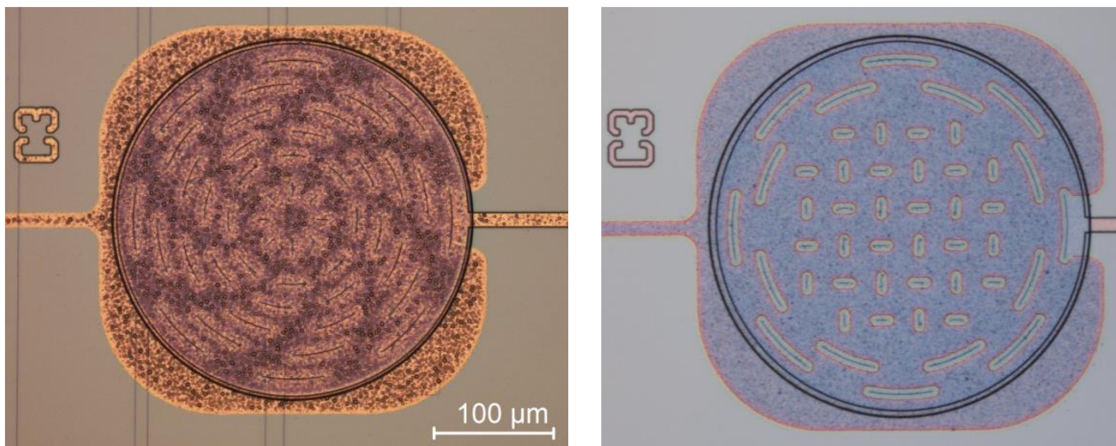

Fig. 2.14: Fabricated C300 (ø300 µm device) showing reduction of the surface roughness from the Sapphire15 (left) to the Sapphire16 (right).

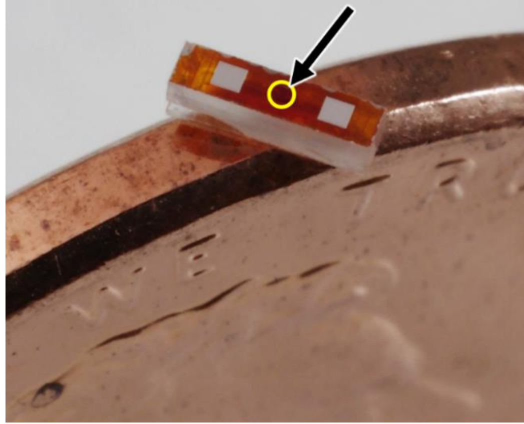

Fig. 2.15: Macro view of diced C100 device on a US penny. Actual device is circled in yellow; large contact pads are only for prototype testing and can be reduced as necessary.

2.4 FEA Simulation: Modeling the Capacitance Response

In order to accurately model the responses of the fabricated sensors, simulations were completed with COMSOL Multiphysics® 4.4, which allows for touch mode operation simulation with a dielectric insulation layer present [Wan99]. The Electro-mechanics module provided a dedicated interface for simultaneously determining diaphragm deflection (mechanical) and capacitance (electrical) response of the sensor. Simulated touch mode operation is permitted by limiting the diaphragm deflection with a distributed contact force on the boundary of the insulated lower electrode. When the diaphragm deflects beyond the defined inter-electrode gap, this contact force stops the diaphragm, illustrated in Fig. 2.16 (a) and (b).

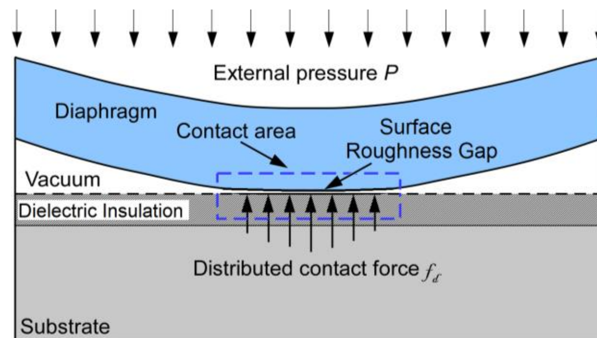

Fig. 2.16: (a) Cross-sectional illustration showing diaphragm deflection, non-ideal roughness air gap, and contact force allowing for touch mode simulation [Luo15].

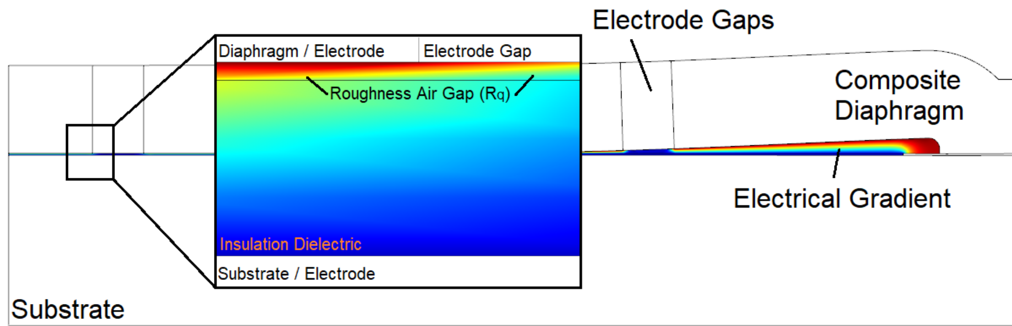

Fig. 2.16: (b) Cross-sectional illustration showing deformed diaphragm under applied pressure and the electrode potential gradient.

In order to expedite simulation time, the diaphragm was modeled as a single composite layer using as accurate geometry as possible. As a major requirement of the sensors is to measure up to 50 MPa (7,250 psi) of pressure, it must at least be able to withstand and survive this pressure. When 50 MPa is applied to a ø100 µm diaphragm, the maximum stress that occurs on the sidewall edge is ≈1.5 GPa, assuming a semi-ideal corner. The diaphragm consists of silicon nitride (Ultimate Tensile Strength ≈6 GPa), silicon dioxide (UTS ≈2 GPa) and aluminum oxide (UTS ≈3 GPa) [Gad01], all of which can survive this theoretical maximum stress during operation.

Additionally, the restoring force of the diaphragm should be adequate to prevent stiction to the substrate when operated at high pressures. Due to the stiff nature of the ø100 µm diaphragms, they have a simulated spring constant of ≈50 kN/meter. When deflected by 50 MPa of pressure, this results in a restoring force of ≈50 mN (assuming a 1 µm chamber gap and diaphragm deflection). During full deflection, approximately 50% of the diaphragm area is in contact with the substrate (≈4000 µm^2), resulting in an equivalent restoring pressure of over 10 MPa. While stiction pressures for silicon nitride and aluminum oxide have not been published, the published minimum restoring pressure for polysilicon / polysilicon interfaces is stated to be between 1-10 kPa [Bha01], more than 1000x smaller than the estimated restoring pressure.

However, the electrical modeling is more difficult, as a large number of non-idealities needed to be integrated with the simulation model in order to find a matching response. These

included an effective value for the diaphragm's Young's modulus, E, (approximated as a single composite layer to reduce simulation run-time), deposited layer thicknesses (affecting the inter-electrode cavity gap, g, and diaphragm thickness, h), radial variations in the thickness of the dielectric electrode insulation, upper electrode area (reduced due to etchant access slit geometry), and RMS surface roughness, R_q, (approximated as a constant air gap between the lower boundary of the upper electrode and upper boundary of the dielectric electrode insulation). Due to the large number of required matching parameters, though, it is nearly impossible to predict the exact expected result prior to fabrication, as small changes in these values can dramatically impact the final capacitance response. Using estimated nominal values listed in Table 2.2, the expected change in capacitance for a ø100 µm device is approximately 450 fF. However, the parameters have some uncertainty, due to variations in the deposited thickness (g, h), lithography (electrode area), physical nature of the layers (E), and/or surface roughness (R_q). Estimated changes in these values (excluding the major roughness error due to Al spiking) are given in Table 2.2, and the estimated change in capacitance response (over 50 MPa of applied pressure) from the maximum to the minimum (holding the other parameters constant) is listed. If all parameters are shifted to their maximum/minimum, the response can vary from as high as 1200 fF to as low as 200 fF.

Table 2.2: Major parameters required to fit the capacitance response.

Parameter	Nominal	Est. Variation	Var. Range	ΔC_{50MPa}
Inter-electrode Gap (g)	1.0 µm	±5%	0.95 – 1.05	±10 fF
Diaphragm thickness (h)	5.0 µm	±5%	4.75 – 5.25	±20 fF
Electrode Area	6000 µm^2	±5%	5700 – 6300	±50 fF
Young's Modulus (E)	120 GPa	±33%	80 – 160	±60 fF
Roughness (R_q)	20 nm	±75%	5 – 40	±250 fF

2.5 Experimental Results

Capacitive pressure sensors with diaphragms measuring ø100 µm, ø200 µm, and ø300 µm were tested in an oil environment. Each diced device is first mounted to a prototype printed circuit board using conductive silver epoxy. The prototype board is then soldered to a 6-pin electrical connector, inserted into a high pressure test chamber, and fixed in place by the chamber cover, shown in Fig. 2.17. Pressure was applied with a manual hydraulic pump and monitored by a pressure gauge in between the pump and pressure chamber. The capacitance was read out through an HP 4284A LCR meter, calibrated with terminals open and shorted prior to measurement.

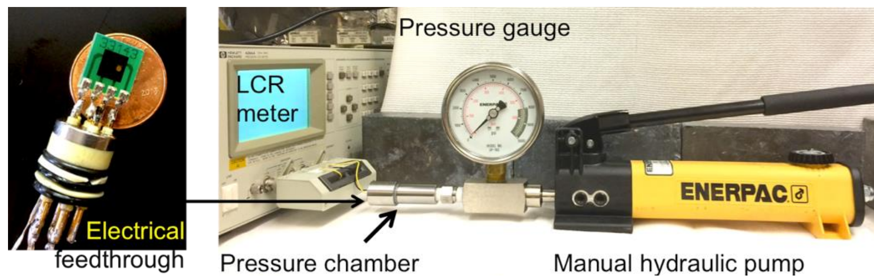

Fig. 2.17: Experimental setup for measuring the capacitive pressure sensors.

An overview of measured results of the Sapphire15 (high yield) process is provided first. It is apparent in the Sapphire15 devices that the cavity roughness due to aluminum spiking caused a significant reduction in the capacitance response, with spiking modeled to extend as high as 320 nm (approximated as an air gap of this thickness between the electrodes).

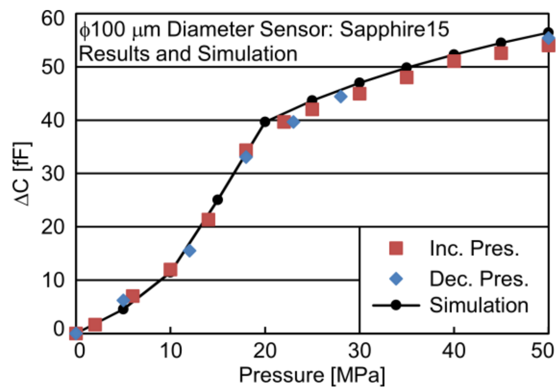

Fig. 2.18: Sapphire15: Response of ø100 µm device. Capacitance change in response to applied oil pressure. Each data point is average of ≈10 readings. Matching simulation parameters: Spiking roughness: 220 nm (@r=0) 320 nm (for r ≥20 µm), h=5 µm; g=1.5 µm; E: 160 GPa; upper electrode openings: 3 µm wide rings spaced every 15 µm.

The response of the ø200 µm diameter device (Fig. 2.19) shows improved performance, but this is due simply to the four fold increase in surface area and slightly reduced chamber roughness. Because the aluminum spiking is inconsistent, the roughness from device to device varied. This tested device had a modeled roughness of only 150 to 250 nm in height, allowing for a larger capacitance response. This device enters touch mode around 1 MPa, but shows a significant taper after 5 MPa. Unlike the ø100 µm devices which show a change in capacitance response as they enter touch mode, the larger devices show a taper once the diaphragms have nearly fully deflected into touch mode, and only a small area around the perimeter continues to deflect. For this device, the region of high capacitance response between 0 and 5 MPa show ≈85 fF/MPa, while the tapering region between 5 and 25 MPa reduces to ≈22 fF/MPa.

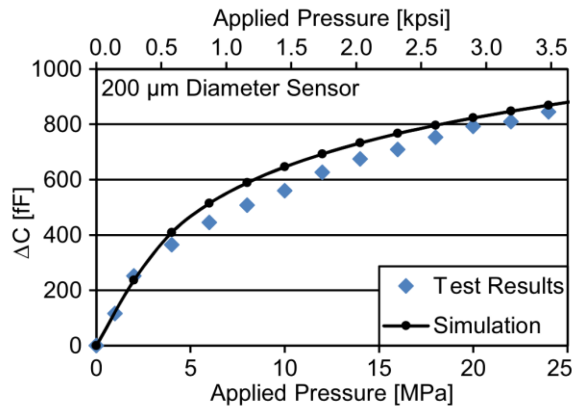

Fig. 2.19: Sapphire15: A ø200 µm device with cavity roughness due to Al spiking. Capacitance change in response to applied oil pressure. Each data point is the average of ≈10 readings. Matching sim. parameters: roughness: 150 nm (@r=0) tapered to 250 nm (r ≥20 µm); h=5 µm, g=1.5 µm; E: 160 GPa; upper electrode openings: 7 µm wide rings, spaced every 30 µm.

The ø300 µm diameter sensor was tested at a much lower pressure range (up to 0.7 MPa (100 psi) applied pressure) and shows a sharp change between touch and non-touch mode sensitivities, likely due to large spiking in the cavity, which was modeled to taper from 160 to 280 nm, shown in Fig. 2.20. As the low full-scale range sensor diaphragms are very compliant, once they enter touch mode, they conform to the surface very quickly and show a nearly complete shunting of the capacitance change rather than a longer taper as seen in other devices.

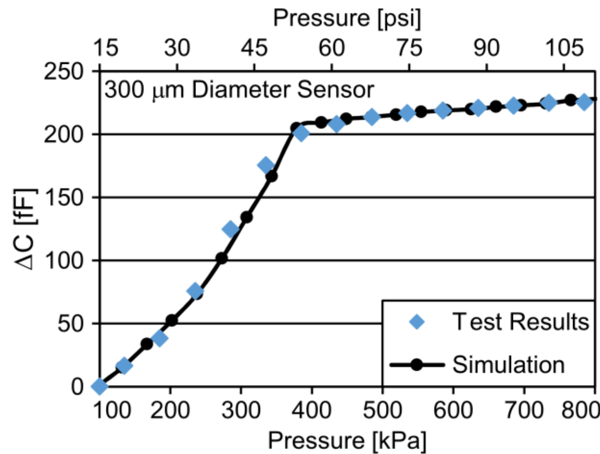

Fig. 2.20: Sapphire15: A ø300 µm device with cavity roughness due to Al spiking. Capacitance change in response to applied oil pressure. Each data point is the average of ≈10 readings. The simulation parameters used to match the test results: Spiking roughness: 160 nm (@r=0) tapered to 280 nm (for r ≥60 µm); h=5 µm; g=1.5 µm; E: 160 GPa; upper electrode openings: 10 µm wide rings, spaced every 30 µm.

Sapphire16 Experimental Results:

Measured results from the Sapphire16 (high performance) process are shown below. Fig. 2.21 shows the response from a single ø100 µm device while Fig. 2.22 shows the response of 4 parallel connected ø100 µm devices and a comparison to the Sapphire15 iteration response, both with 50 MPa of applied pressure. It is evident that the change in capacitance between the two Sapphire16 devices is not exactly in the ratio of 1:4 as would be in an ideal case. This is due to the non-uniformity of the ALD deposited inside the thin cavity, which can greatly alter the capacitance response and entrance pressure of the devices into touch mode, causing uncontrolled variances from device to device. While this is non-ideal from a system integration standpoint, the Sapphire15 and Sapphire16 fabrication runs were used to prove the capacitance response, yield, low C_0, and improved TCO of the dielectric substrate process.

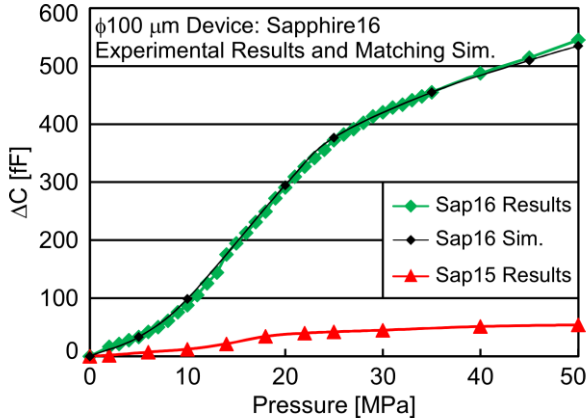

Fig. 2.21: Sapphire16: One ø100 µm device (C100) response. Capacitance change in response to applied pressure. Each data point is the average of ≈10 readings. Matching simulation parameters: ALD: linear taper of 95 nm (@r=0) to 40 nm (@ r=50 µm); g=1.0 µm; E: 110 GPa; RMS roughness R_q=35 nm; upper electrode openings: 3 µm wide rings spaced every 15 µm.

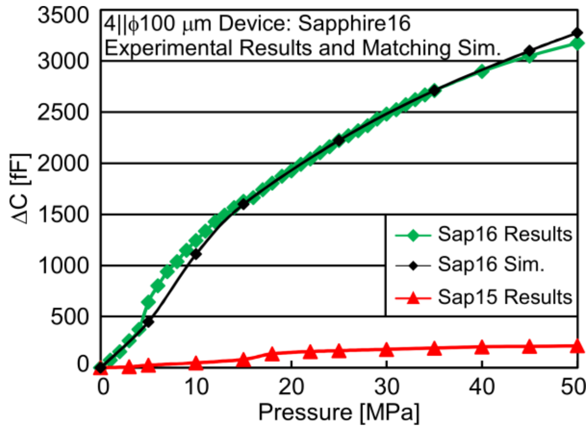

Fig. 2.22: Sapphire16: Four parallel-connected ø100 µm device (4C100) response. Capacitance change in response to applied pressure. Each data point is the average of ≈10 readings. Matching simulation parameters: ALD: linear taper of 65 nm (@r=0) to 20 nm (@ r=50 µm); g=1.0 µm; E: 110 GPa; R_q=35 nm; upper electrode openings: 3 µm wide rings every 15 µm.

2.5.1 TCO Measurement: Sapphire16

The temperature coefficient of offset (TCO, equation 2.6) of the ø100 µm Sapphire16 device was tested without attachment to the prototype PCB, as it was only rated for 100°C, preventing testing beyond this range. Due to the wire-bonding attachment of the sensor the PCB, it also added a large amount of parasitic capacitance. The PCB was eliminated by attaching wire leads directly to the sensor contact pads. However, in order to correct for any TCO parasitic offset, the TCO of the wire leads attached to a dummy device were obtained first. This parasitic TCO was then subtracted from the TCO of the real device to obtain the isolated TCO of the sensor.

$$TCO \equiv \frac{\Delta C}{C_0 \Delta T} \tag{2.6}$$

The capacitance values were obtained with the HP 4284A precision LCR meter used in the pressure testing. In order to ensure a uniform sensor temperature, fine grit sand was placed in a

glass bowl and heated with a hot plate. The sensor was then placed approximately 2 cm below the surface of the sand and two thermocouples were placed adjacent to the buried sensor. The C_0 of the dummy and sensor were recorded as the temperature was risen and lowered from room temperature to 200°C. Response measurements are shown in Fig. 2.23 and 2.24.

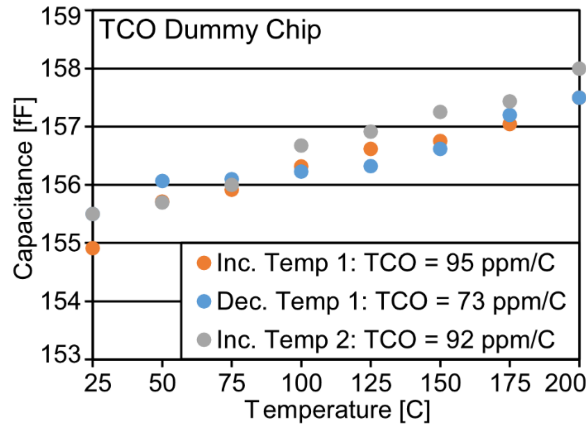

Fig. 2.23: Temperature dependence of the capacitance of dummy chip and wire leads.

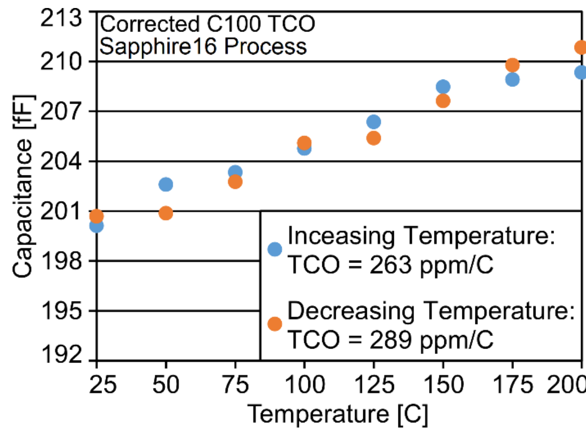

Fig. 2.24: Corrected temperature-dependent offset of ø100 µm device.

The main component contributing to the TCO of the sensor is the mismatch between the thermal expansion coefficients of the diaphragm layers and substrate. In capacitive pressure sensors with non-vacuum cavities, the expansion of the cavity gasses can be a major contributing factor, adding an additional two orders of magnitude to the TCO [Lee82], but due to the vacuum sealing nature of the capping PECVD nitride and ALD, this sensor cavity is at near-vacuum. Using thermal expansion coefficients obtained from both experimental data and references [Hua06] for

the oxide [Rie88], aluminum, ALD Al_2O_3 [Kim08], and low-stress nitride [Mar04], the diaphragms average weighted thermal coefficient of expansion (TCE) is approximately 5.6 ppm/°C while the sapphire wafers have a TCE of approximately 5.9 ppm/°C (parallel to the C-plane). This close thermal expansion match (along with vacuum cavity sealing) helps contribute to the low TCO of these devices.

While the temperature coefficient of sensitivity (TCS) was not measured, the C vs. P curve was obtained at room temperature from the temperature cycled device after it was cooled, showing a fully functional, nearly unchanged response after being brought to 200°C, shown in Fig. 2.25.

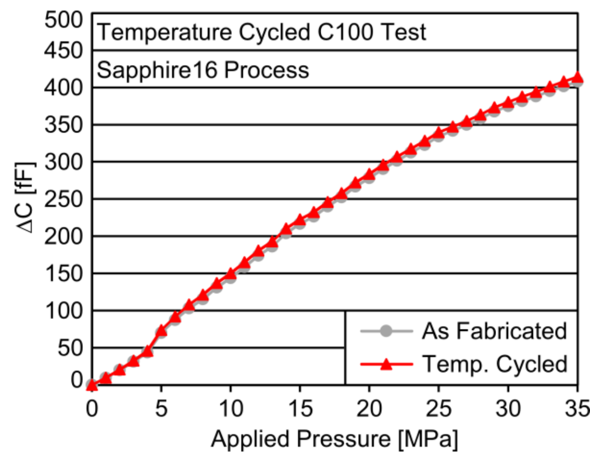

Fig. 2.25: C vs. P response of temperature cycled ø100 µm device. The pressure response is nearly identical before and after being temperature cycled to 200°C.

2.5.2 Microsystem Integration Test Results: Sapphire15

Through a collaborative effort[1], a custom microsystem was designed and assembled to verify the pressure sensor response in its primary use-case of data logging in high-temperature, high-pressure subsurface environments that can be encountered in hydraulic fracturing wellbores. Its system components were commercial off-the-shelf to enable rapid prototyping, consisting primarily of an MCU (Silicon Labs C8051F990), solar cell (Clare CPC1822), LED indicators for optical data transfer, and miniature rechargeable lithium battery (Seiko Instr. MS412FE) [Cho17].

[1] The microsystem design, assembly, and testing was performed primarily by Yu Sui, Yushu Ma, Ryan Meredith, Tao Li, Andy Trickey-Glassman, Neeharika Vellaluru, and Wenching Tsai.

The MCU was responsible for functional control, data storage and communication, system power management, temperature monitoring, and capacitance-to-digital conversion (with a resolution of 1 fF/code up to an absolute capacitance of 45 pF). During system operation, the system took temperature and capacitance measurements every 2 minutes. The system components were integrated onto a flexible polyimide PCB, which was folded and placed into a stainless steel or ceramic package ($8.9 \times 8.9 \times 6.85$ mm^3). The integrated sensor and PCB were then completely sealed in the shell with a deformable epoxy (such as PDMS), which allowed pressure transmission while protecting the system from direct exposure to the environment, shown in Fig. 2.26.

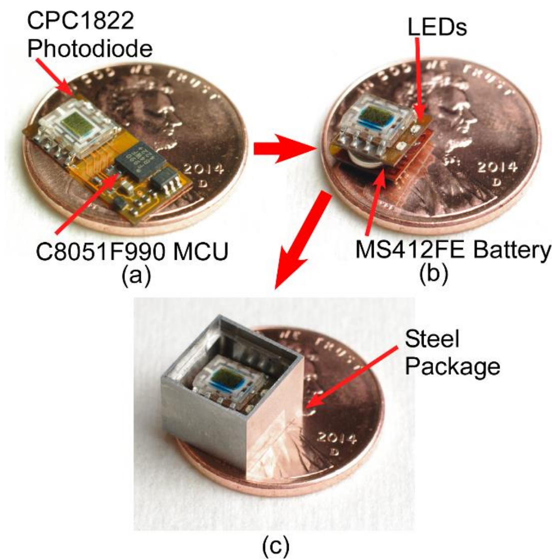

Fig. 2.26: (a) Photo of flexible polyimide PCB before assembly. (b) Photo of the folded electronics stack. (c) Photo of the prototype microsystem in a stainless steel package [Li17].

The first test of the sensors in the custom microsystem used a Sapphire15 4C100 device (four parallel connected ø100 μm devices). It was pressure tested up to 50 MPa at room temperature, Fig. 2.27. The pressure was applied using a hydraulic pump with a pressure transducer from TE Connectivity than can read up to 69 MPa (10,000 psi). The pressure cycle was a linear ramp up to 50 MPa over one hour with a hold 20 minutes at 50 MPa. The discretization issue is due to the MCU being incorrectly programmed; the system is capable of resolving 1 fF.

It should be noted that the total capacitance change was 256 fF. In the previous test of a Sapphire15 iteration C100 device (a singular ø100 µm device, shown in Fig. 2.18), the total capacitance change was 57 fF, which is approximately ¼ of the capacitance change, as would be expected. However, the response is more linear than that of the individually tested Sapphire15 C100 device response, believed to be due to the parallelization of the diaphragms and inconsistent cavity roughness. Because the aluminum spiking is relatively random in its roughness height, it is likely that each sensor in the 4C100 device entered touch mode at a slightly different pressure, leading to a more linear response, as the high capacitance response peak in the transition region would be spread out.

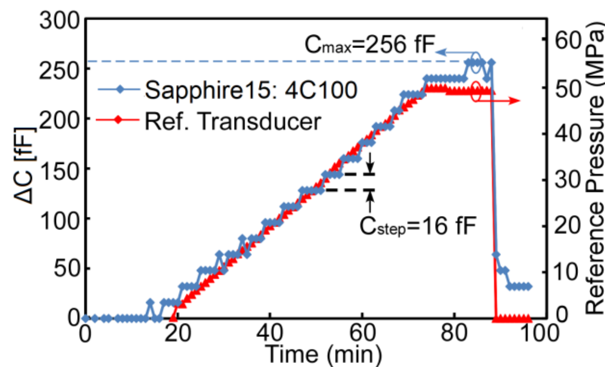

Fig. 2.27: Sapphire15: C vs. P response of a 4C100 (4 parallel connected ø100 µm devices) integrated with the microsystem. The discretization errors were due to a correctable software error, causing a large ΔC_{min} to be used.

2.5.3 Microsystem Integration Test Results: Sapphire16

To lab test the Sapphire16 devices, a 4C100 device (four parallel connected ø100 µm devices) was packaged and tested with the microsystem in the same manner as the Sapphire15 device described above. Compared to the 4C100 test shown in Fig. 2.22, the results (Fig. 2.28) are quite similar, showing an entrance into touch mode around 5 MPa, an increasing but tapering response in touch mode, and a ΔC of ≈3.5 pF at 50 MPa. Again, differences in sensor response are due to inconsistent ALD coverage, causing variances in electrode spacing when in touch mode, resulting in different responses curves.

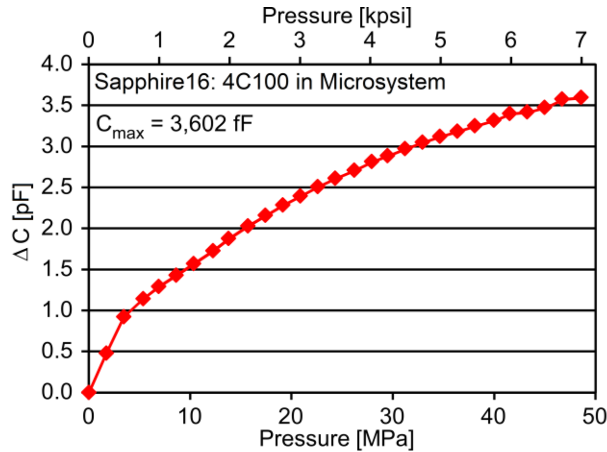

Fig. 2.28: Sapphire16: C vs. P response of a Sapphire16 4C100 (four parallel ø100 μm devices) integrated with the microsystem. The discretization errors seen in the Sapphire15 test have been eliminated and the results are similar to the non-integrated device tests, Fig. 2.22.

More Sapphire16 sensors were integrated with microsystems and tested at RTI International in North Carolina using equipment that could apply both high pressure and temperature to the system. The test shown in Fig. 2.29 is that of a Sapphire16 C100 device integrated into a microsystem with a maximum pressure and temperature of 50 MPa (7,250 psi) and 125°C applied over the course of 90 minutes. The interpreted pressure of Fig. 2.29 (c) was calculated by using the linear relationship between the capacitance and pressure of Fig. 2.29 (b). Because the capacitance response is not completely linear, there are minor errors in the interpreted pressure data of Fig. 2.29 (c).

A drift in the output capacitance when held at pressure and temperature can also be observed. This is likely due to a further compression of the sealing epoxy and the commercial electronics being operated outside of their maximum temperature range. With further investigation into the effects of the microsystem, this drift can potentially be corrected for.

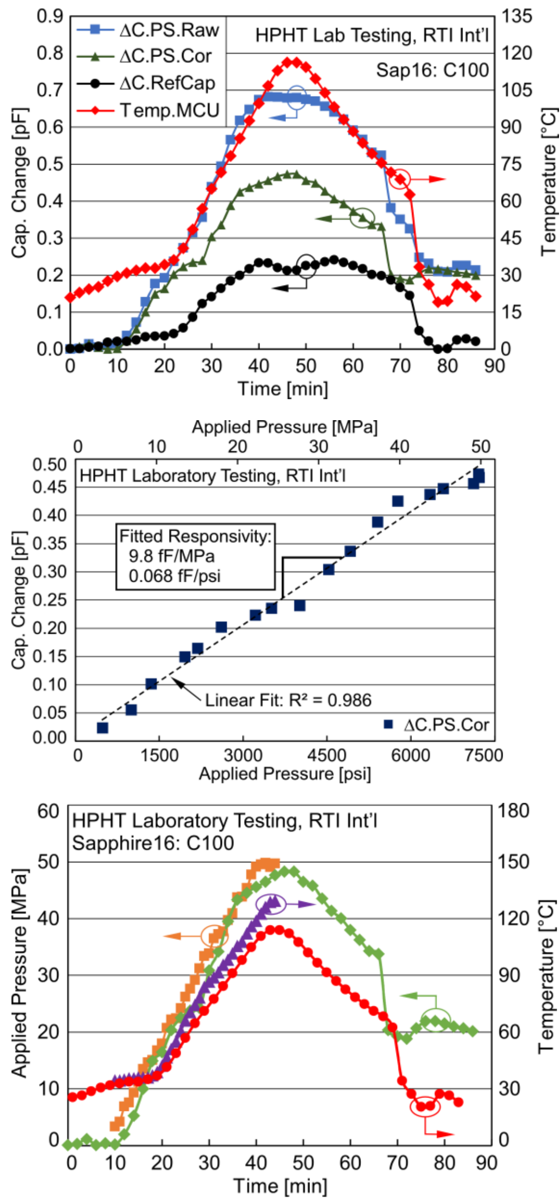

Fig. 2.29: (a) Sensor data captured with the microsystem when a pressure and temperature ramp was applied (as shown in Fig. 3.29: (c)). A reference capacitor is used to correct for the readout circuitry drift at high temperatures. The corrected AEC sensor capacitance is then obtained by subtracting the reference capacitor data from the raw sensor data.

Fig. 2.29: (b) The pressure response of a Sapphire16 ø100 µm sensing element. While this curve is more linear than the lab tested sensor, this increased linearity is presumably caused by the combined effects of pressure attenuation through several millimeters of protective epoxy and the read-out circuitry operating at temperatures above its certified limits.

Fig. 2.29: (c) Using the linear fit of the pressure response from Fig. 3.29: (b), the interpreted pressure and temperature were calculated and plotted. Machine applied temperature and pressure are plotted for comparison (test equipment stopped recording data after 45 minutes).

This test shows that these sensors are capable of recording pressure for up to 90 minutes at a simultaneous applied pressure of 50 MPa (7,250 psi) and 125°C, albeit with readout drift due to the first generation of system integration using prototype electronics and integration methods. While there was some variability between from sensor to sensor, it was thought that these variances were caused by non-uniform inter-electrode sealing of the ALD, which is corrected in the Sapphire17 iteration.

2.6 Discussion and Summary of Sapphire15 and Sapphire16 Results

An investigation into a dielectric sapphire substrate, 5-mask microfabrication process for capacitive pressure sensors was conducted. Many fabrication challenges were investigated and addressed, bringing the diaphragm yield up to ≥85% for all device diameters in the Sapphire15 process, and demonstrating the ability to solve numerous yield limiting challenges by focusing on the interactions between equipment configurations and limitations and sensor design. The TCO of the Sapphire16 devices was measured to be less than 300 ppm/°C up to 200°C, including parasitic effects that may result from the test set-up. There was very little change in the response after being brought to 200°C. The pressure sensors were demonstrated to be operational within microsystems at pressures up to 50 MPa (7,250 psi) and temperatures up to 125°C.

It should be noted that the smallest sapphire substrate capacitive pressure sensor had a diaphragm of ø100 µm, with a total potential minimum volume of ≈0.011 mm^3. Because the final dimension of the sensor was determined by the microsystem integration requirements (primarily contact pad size and spacing for placement onto the flexible PCB), there was no size difference between the final fabricated sensors. The active sensor-diaphragm area was <0.01 mm^2 (0.7% total sensor area) for the C100 ø100 µm device and <0.04 mm^2 (2.8% total sensor area) for the 4C100 4||ø100 µm device. With such a small active device area, the final sensor could theoretically be reduced in size to accommodate a 0.4×0.4 mm^2 size requirements for sub-millimeter packages [Ma14] with no loss in capacitance response.

CHAPTER 3: Process Improvements for Sensitivity and Yield

While many fabrication improvements were made in the Sapphire15 and Sapphire16 process, culminating in a diaphragm yield of over 85% and capacitance response improvement of nearly an order of magnitude, these goals were not met simultaneously; the final high response fabrication run (Sapphire16) suffered from low yield due primarily to delamination of the ALD electrode insulation, resulting in yield loss due to shorting when operated at high pressure. By carefully tracking down the cause of these yield limiting issues, a combined high-yield / high-sensitivity fabrication process was created.

The Sapphire17 process consisted of 6-mask lithographic microfabrication steps starting with a dielectric sapphire wafer, as shown in Fig. 3.1 and 3.2. This process was used to make sensors that were integrated into microsystems tested in laboratory settings at Pau, France, and in brine well borehole field tests in Vauvert, France.

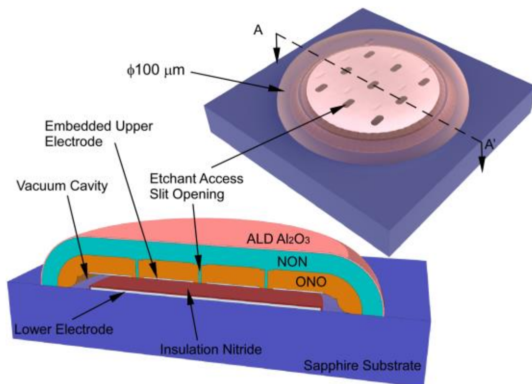

Fig. 3.1: (a) Schematic of a capacitive pressure sensor on a sapphire substrate

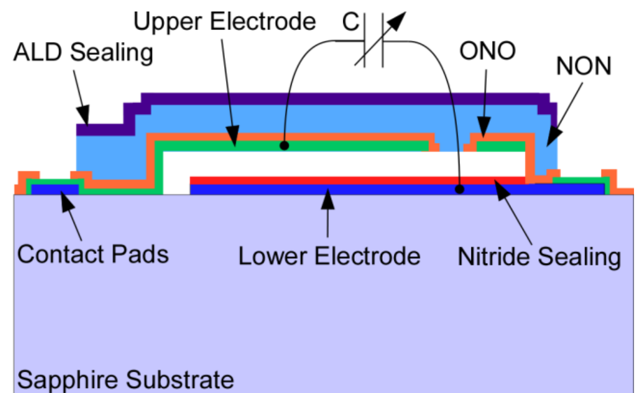

Fig. 3.1: (b) Cross section of the capacitive pressure sensor on a sapphire substrate

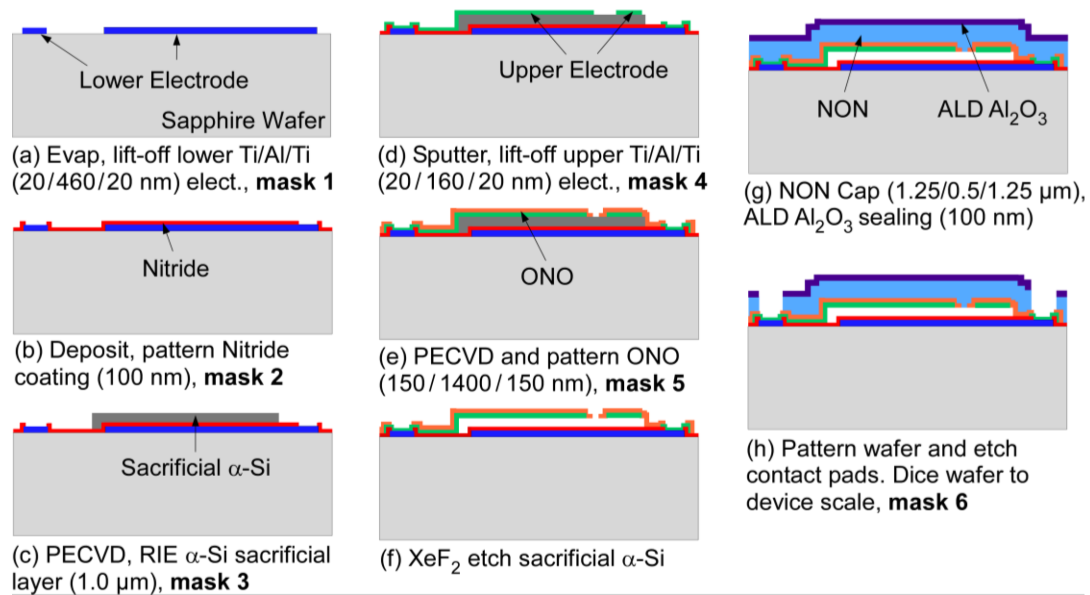

Fig. 3.2: Process sequence for the Sapphire17 high-yield/high-sensitivity process.

Sapphire17 Process Description:

The Sapphire17 process is similar to the Sapphire15 and Sapphire16 processes, but with one major alteration – silicon nitride replaced ALD Al_2O_3 as the electrode insulation layer. Due to the issues with the ALD causing delamination and poor electrode coverage when deposited inside the cavity, it was decided that insulating the lower electrode with a high quality nitride would provide the best results in terms of cavity roughness and device response repeatability, as variances in electrode insulation thicknesses would be reduced.

3.1 Sapphire17 Fabrication Modifications and Improvements

Fabrication results at important points of the process sequence and solutions to all encountered problems are highlighted below.

Mask 1: Lower Ti/Al/Ti Electrodes

The Sapphire17 process begins with the deposition and definition of the lower electrode Ti/Al/Ti stack using evaporation and liftoff. The titanium layers are used as adhesion promoters between the aluminum and sapphire as well as between the aluminum and insulation nitride. To

ensure proper device sensitivity and yield, the two most critical aspects of the lower electrode are the insulation of the aluminum from the α-Si (to prevent aluminum spiking) and the reduction of the surface roughness (to increase touch mode capacitance response by reducing non-ideal electrode separation in touch mode). By using an adhesion layer of Ti and an insulation layer of silicon nitride between the aluminum and α-Si, the possibility of aluminum spiking is eliminated. To ensure a minimal surface roughness of the metal electrode, the minimal chamber vacuum (<1 μTorr) and a low deposition rate (~4 Å/s) were used [Bor12], resulting in a measured root mean square surface roughness of <5 nm.

Mask 2: Silicon Nitride Electrode Insulation

The Sapphire15 and Sapphire16 processes used Atomic Layer Deposition (ALD) of Al_2O_3 to insulate the electrodes, but resulted in unreliable electrode coverage, causing both inconsistent device response and yield loss from layer delamination and device shorting when in touch mode operation. For the Sapphire17 iteration, a 100 nm layer of silicon nitride (Si_3N_4) was instead used for electrical insulation. This was the most suitable replacement material for electrode insulation, as it has a similar dielectric constant (ε_r) to ALD Al_2O_3 (7.5 for Si_3N_4 [Ma98] vs. 9.1 for Al_2O_3 [Bie03]) and can be deposited with a very low roughness using PECVD [Ami16], (<5 nm verified experimentally), allowing for similar ideal touch mode response. While this does add one masking step, it proved to completely eliminate all issues with adhesion and shorting, as the α-Si proved to have superb adhesion to the nitride and the upper electrode and was no longer deposited onto the inert ALD, but rather the surface of the α-Si. With the insulation layer being deposited on the open field of the wafer with only the lower electrode patterned, it ensured that the touch mode response was as consistent as possible, being limited in thickness variations due only to the limitations of the PECVD tool.

Mask 3: α-Si Sacrificial Layer

With the adhesion issue of the α-Si solved by the use of silicon nitride as a lower electrode insulation layer, the same low stress PECVD amorphous silicon (α-Si) defined with sloping sidewalls was used to define the diaphragm diameter and inter-electrode gap.

Mask 4: Upper Electrode

A Ti/Al/Ti stack is sputtered and defined with lift-off using lift-off resist (LOR) as was done in the Sapphire15 and Sapphire16 iteration. The Ti and Al sputtering recipes were tuned for minimal stress (≈30 MPa compressive) by adjusting the RF power and sputtering pressure.

Mask 5: PECVD Dielectric Diaphragm Definition and Sealing

A PECVD stack of low stress oxide/nitride/oxide (ONO) was used to define the initial diaphragm, where the oxide layers were used for balancing the nitride stress and protecting the nitride during the XeF_2 sacrificial etch. The etchant access slots in the ONO stack were defined with a dry plasma RIE etch. The underlying α-Si was then etched using XeF_2 to release the diaphragm. Using a second dielectric stack of nitride/oxide/nitride (NON), the etchant access slits were sealed, followed by a final sealing layer of ALD Al_2O_3 for hermeticity.

Because many of the yield limiting issues encountered in the Sapphire15/16 iterations (e.g. aluminum spiking surface roughness, electrode delamination, diaphragm cracking) were solved, all effort on the dielectric diaphragms could be focused on stress and thickness *control*. Because these parameters are of vital importance for sensor yield and capacitance response, they were tuned for optimal values and re-measured before each deposition to ensure no tool drift had occurred. The stress of the silicon dioxide was measured at -122±7 MPa with a cross wafer thickness non-uniformity of less than 2.0% (±2 nm when deposited to a thickness of 150 nm) while the nitride

was measured at 81±4 MPa with a cross wafer thickness non-uniformity of less than 1.6% (±11 nm when deposited to a thickness of 1400 nm).

Using well controlled recipes (combined with re-checking and re-tuning layers before each deposition), these diaphragms were created with well controlled stress (46±5 MPa, weighted sum) and high capacitance response while maintaining diaphragm yield in excess of 90%.

One final sensitivity-limiting issue encountered (occurring only with sensors whose diameters were ≥200 µm) was the deposition of PECVD into the cavity through the etchant access slits during diaphragm sealing. Due to the larger sensor cavity volume, PECVD could more easily deposit though the etchant access slots, resulting in ridges under each slot, as shown in Fig. 3.3. This re-entrant PECVD constrained diaphragm deflection under externally applied pressure, diminishing the total output signal. By further exploring the limitations of the lithography tools available, thinner etchant access slits could be used in future iterations to reduce the amount of reentrant PECVD for more consistent responses on larger devices.

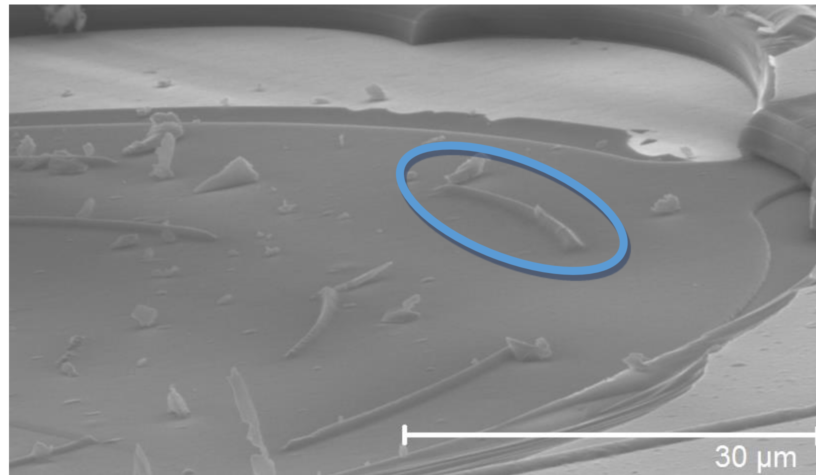

Fig. 3.3: SEM micrograph of PECVD ridges deposited inside the sensor cavity. The sensor diaphragm has been removed. Each ridge is approximately 300 nm in height.

Mask 6: Contact Pad Definition

The final masking layer was used to open the contact pads by removing the PECVD layers. The wafer was patterned and dry etched. Following the contact pad opening, the devices were diced to the device level using a custom dicing recipe designed to minimize chipping developed in the Sapphire16 process. By using a slower feed rate and cut depth, the chipping could be reduced to ≈25 µm, allowing for an improved final yield.

The total combined fabrication improvements in the Sapphire17 fabrication process included using a silicon nitride insulation on the lower electrode to improve the surface roughness and α-Si adhesion, enhanced stress and thickness control of the PECVD dielectric diaphragm layers for increased diaphragm yield, and improved dicing, allowing for even further improved device yield and capacitance response. When all of these improvements were combined in the final Sapphire17 fabrication run, a fully fabricated and diced device yield of >80% was achieved while not only maintaining, but also improving, the capacitance response nearly two-fold from the Sapphire16 iteration of the ø100 µm devices. Selected device photos and SEM micrographs of the Sapphire17 iteration devices are shown below.

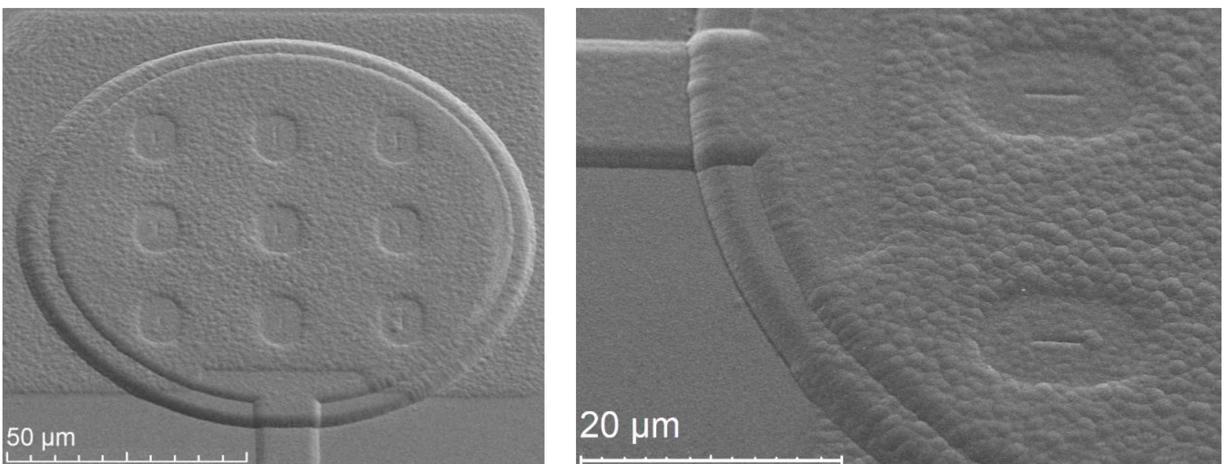

Fig. 3.4: SEM Image of a fabricated C100 device (singular ø100 µm diaphragm) and close up SEM image showing sealed etchant access slits and lower electrode routing.

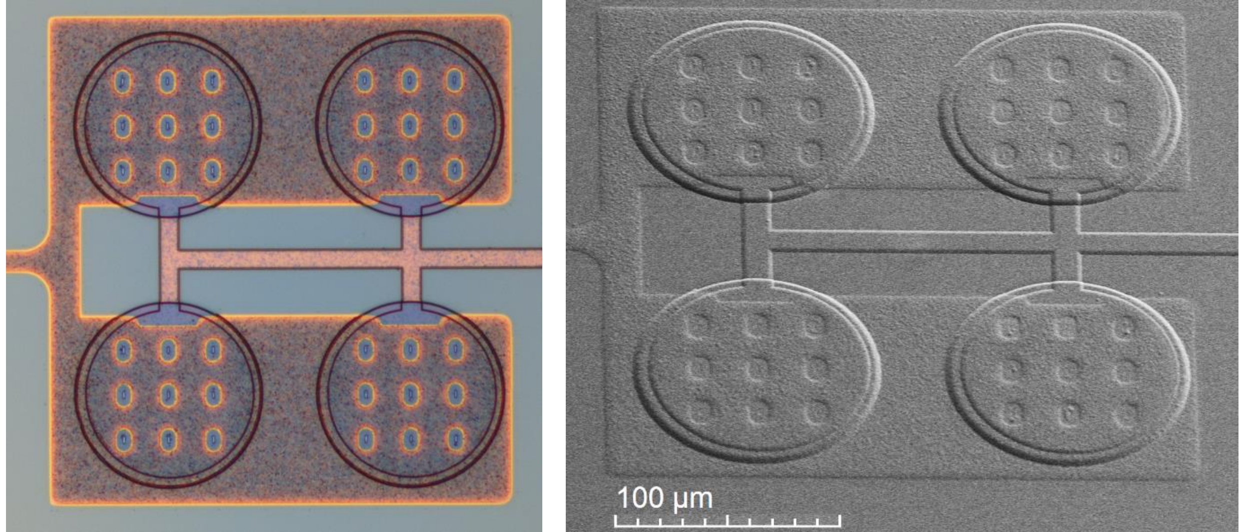

Fig. 3.5: Optical image (left) and SEM micrograph (right) of a fabricated 4C100 device (4 parallel connected ø100 µm diaphragms).

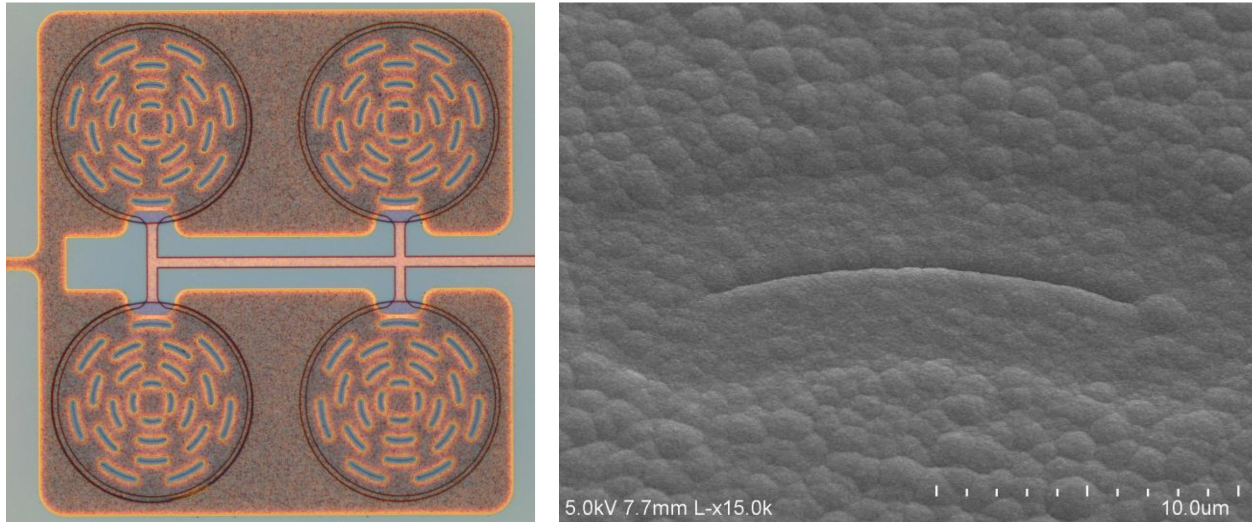

Fig. 3.6: Optical image (left) of a fabricated 4C200 device (4 parallel connected ø200 µm diaphragms) and SEM micrograph (right) of a sealed etchant access slit on a C200 device.

3.2 Experimental Results and Matching Simulations

Capacitive pressure sensors with diaphragms measuring ø100 µm and ø200 µm were tested in an oil environment in the same manner as Sapphire15 and sapphire16 (using the test set-up shown in Fig. 2.17). An overview of measured results of the Sapphire17 process and comparison to the previous iterations is provided. Fig. 3.7 shows the sensor development of the ø100 µm device over the course of the Sapphire15, Sapphire16, and Sapphire17 iterations, showing an

improvement of over 18 fold from Sapphire15 to Sapphire17 and nearly two fold from Sapphire16 to Sapphire17. Fig. 3.8 shows the capacitance response improvement of the 4C100 device with similar capacitance response improvements to the single diaphragm C100 device.

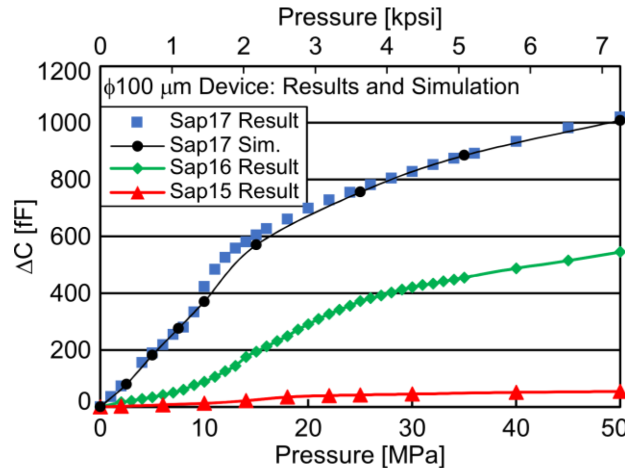

Fig. 3.7: One ø100 µm device (C100) with comparison to previous iterations. Capacitance change in response to applied oil pressure. Sapphire17 simulation parameters matching the test results: Insulation nitride: 75 nm, h=5 µm; g=1.0 µm; E: 100 GPa; RMS Roughness R_q=15 nm; upper electrode openings: 3 µm wide rings spaced every 15 µm.

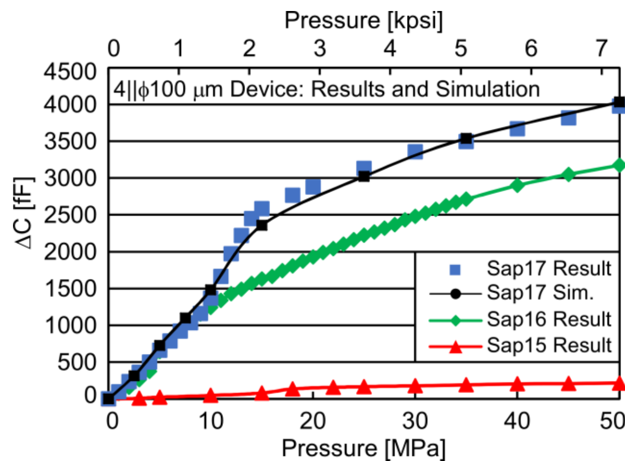

Fig. 3.8: Four parallel-connected ø100 µm devices (4C100) with comparison to previous iterations. Capacitance change in response to applied oil pressure. Sapphire17 simulation parameters are the same as the C100 device, Fig. 3.7, with simulation results multiplied by 4.

As described in the previous section, the change in capacitance between the Sapphire16 C100 and 4C100 devices is not exactly in the ratio of 1:4 as would be in an ideal case, due to the non-uniformity of the ALD being deposited inside the chamber. However, in the Sapphire17 iteration, the ALD is replaced with silicon nitride deposited immediately after the lower electrode

definition, minimizing the variation between sensors as a much more uniform layer can be produced. The difference between the C100 and 4C100 sensors at 50 MPa is only ~25 fF (when the 4C100 sensor response is normalized to the C100 response), but these sensor differences can be attributed to the minor variation in material properties as deposited with the PECVD tools.

The C200 devices were also tested, with results shown in Fig. 3.9. An improvement of the C200 devices was achieved in Sapphire17; however, due to reentrant PECVD in the larger diameter devices, responses were variable from device to device.

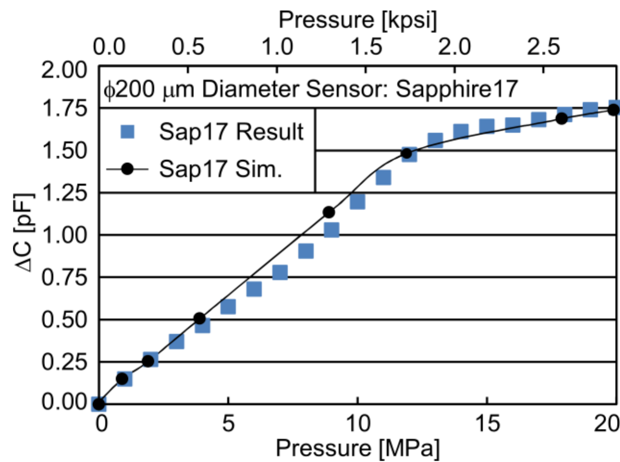

Fig. 3.9: ø200 μm device (C200). Capacitance change in response to applied oil pressure. The simulation parameters used to match the test results: Nitride: 100 nm; h=5.2 μm, g=1.0 μm; E: 100 GPa; R_q=65 nm upper electrode openings: 7 μm wide rings, spaced every 30 μm.

Sapphire17 Theoretical System Resolution:

The Sapphire17 devices can also be integrated with the microsystem. Table 3.1 compares the theoretical resolutions of integrated Sapphire15, Sapphire16, and Sapphire17 ø100 μm devices for a more practical comparison of the improvements in the fabrication process.

Table 3.1: Sensitivity and estimated pressure resolution comparison for ø100 µm devices for the Sapphire15, Sapphire16, and Sapphire17 processes

Microsystem Circuitry Resolution (ΔC_{min}): 1 fF/code						
	Sensitivity, C_0 = 200 fF		Resolution, **C100**		Resolution, **4C100**	
	[fF/MPa]	[ppm/MPa]	[kPa]	[psi]	[kPa]	[psi]
Non-touch (Sapphire15)	2.00	10,000	500	72.5	130	18
Touch (Sapphire15)	0.57	2,833	1800	256	44	64
Non-touch (Sapphire16)	23.45	117,250	40	6.2	10.7	1.55
Touch (Sapphire16)	17.25	86,250	60	8.4	14.5	2.1
Non-touch (Sapphire17)	42.50	211,250	24	3.4	5.9	0.85
Touch (Sapphire17)	14.38	71,900	69	10.1	17.4	2.53

While the touch mode sensitivity of the best Sapphire16 device was higher than the Sapphire17 devices (due to the higher relative permittivity of the ALD electrode seal), there was significant variation in capacitance response from device to device in the Sapphire16 devices. It should also be noted that the average capacitance response of the Sapphire16 iteration was only 12.6 fF/MPa (63,000 ppm/MPa), whereas the Sapphire17 average capacitance response was 26.6 fF/MPa (133,000 ppm/MPa).

3.3 Microsystem Integration Test Results

To experimentally verify sensors at the system level, Sapphire17 devices were integrated into microsystems and tested in both laboratory and field settings[2] in Pau and Vauvert, France, respectively. The field tests were conducted by microsystem attachment to a cable and lowered into a brine well to a depth of 1.3 km. This simultaneously increased both the pressure and

[2] Thanks to John Richard Ordonez-Varela for his help organizing the off-site laboratory and field tests.

temperature. A temperature invariant reference capacitor was again integrated with the microsystem so that the offset and drift due to the electronics could be removed.

Results from a 60 minute lab test are shown in Fig. 3.11 and results of a 3.5-hour duration field test are given in Fig. 3.12. For the field test, commercial sensors (Openfield Technology [Ope13], also attached to the cable) were used to independently verify the pressure and temperature in the oil well. The maximum pressure and temperature were 12 MPa and 70°C. When compared to the non-integrated lab tested sensor (Fig. 3.8), the total capacitance change of the integrated sensor (Fig. 3.11 (b)) over 12 MPa was approximately equal. The pressure response curves for both tests are very similar, being nearly linear in the non-touch mode region (0-12 MPa).

The lab tested sensor (which used a 4C100 (4||ø100 µm diaphragms) device) was capable of resolving 5.5 kPa (0.8 psi) in the non-touch mode (capacitance response of 173 fF/MPa, 1.2 fF/psi) and a resolution of 19.3 kPa (2.8 psi) in touch mode (response of 51.4 fF/MPa, 0.36 fF/psi). The field tested sensor (using a C100 device, single ø100 µm diaphragm) remained in the non-touch regime and was capable of resolving 32.4 kPa (4.7 psi), with a capacitance response of 31.0 fF/MPa (0.21 fF/psi).

Fig. 3.10. Image of brine well (left) and wireline cable (right) used for field testing.

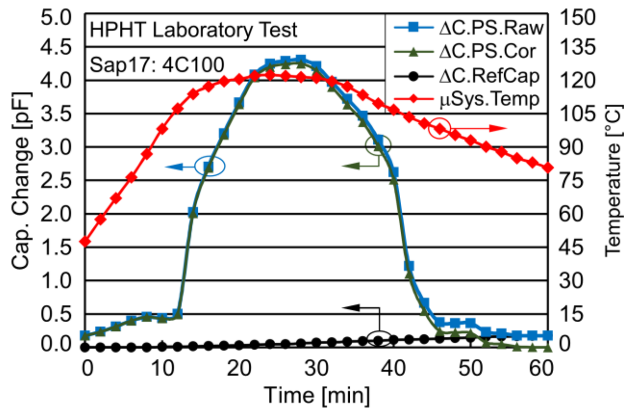

Fig. 3.11: (a) Embedded Sapphire17 4C100 sensor data captured with the microsystem. System was tested in a HPHT testing tool for 60 minutes. A reference capacitor is used to remove the capacitance drift of the C-to-D converter due to temperature.

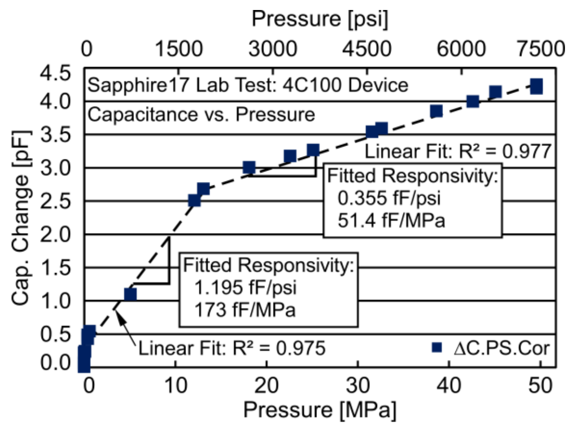

Fig. 3.11: (b) The pressure response of the Sapphire17 4C100 sensing element. Even when embedded into the microsystem, a response similar to the non-integrated devices (Fig. 3.8) is obtained, with entrance into touch mode at ≈12 MPa.

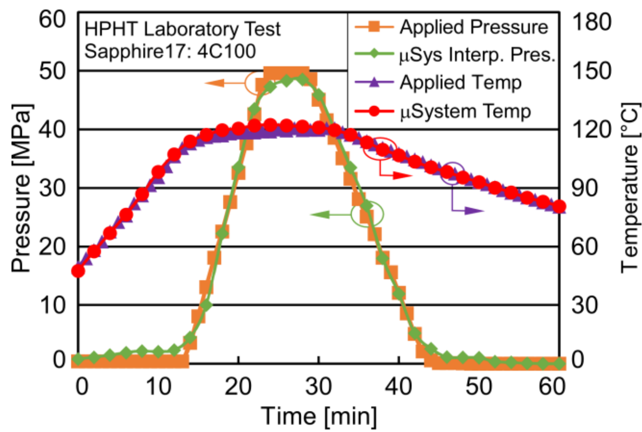

Fig. 3.11: (c) Using the dual linear fit of the pressure response from Fig. 3.11: (b), the interpreted pressure and temperature were calculated and plotted. The data recorded by the tool are plotted for comparison as well. It can be seen that the match between the microsystem data and tool data is very close.

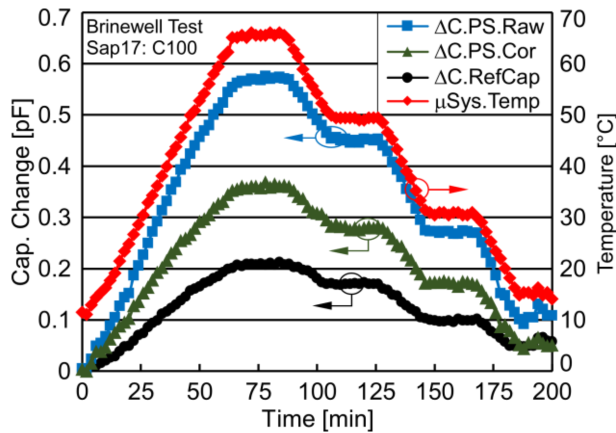

Fig. 3.12: (a) Embedded sensor data captured with the microsystem and Sapphire17 sensor (C100) when the system was lowered into a brine well to a depth of 1.3 kilometers and then raised in steps. An embedded reference capacitor was used to correct for the readout circuitry drift at high temperatures. The corrected sensor response was obtained by subtracting the reference capacitor data from the raw sensor data.

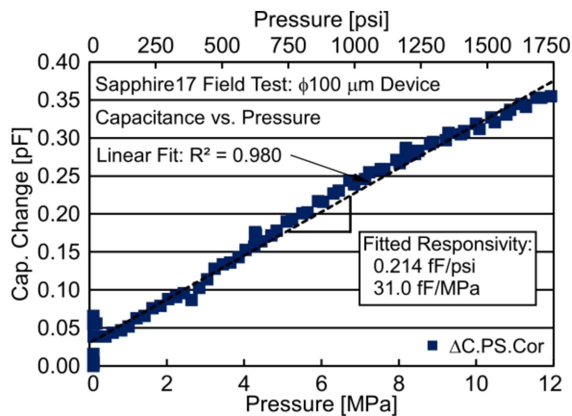

Fig. 3.12: (b) The pressure response of the Sapphire17 C100 sensing element. Even at a depth of 1.3 km, the pressure never rose above 12 MPa, allowing the sensor to remain in the quasi-linear non-touch mode. (Matching the lab tested sensors, Fig. 3.7.)

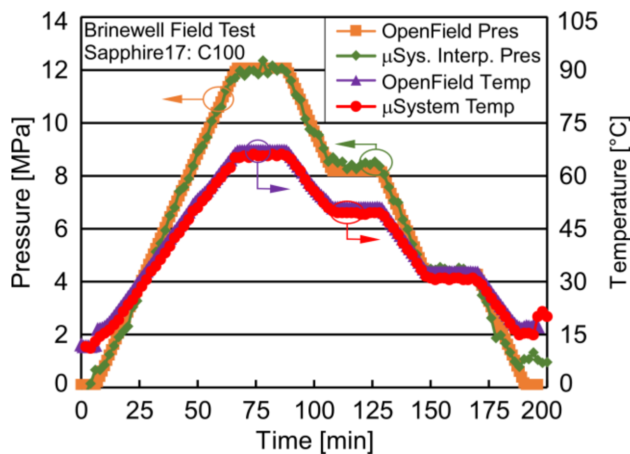

Fig. 3.12: (c) Using the linear fit of the pressure response from Fig. 3.12: (b), the interpreted pressure was calculated and plotted. The Openfield (commercial sensor) data are plotted for comparison as well.

These system tests prove that not only can the sensors accurately track pressure changes in a lab setting up to 50 MPa and 125°C, but also in a practical field environment outside of a controlled laboratory setting. The only error encountered was a slight drift in the capacitance output over the duration of the test. The use of a reference capacitor was able to extract and correct for the temperature offset of the commercial CDC (thought to be due primarily to a temperature

dependency of the comparator in the SAR or in the C-to-V conversion at the front end of the CDC [Sau81], with secondary effects from the thermal expansion [Gia06] of the steel package, sealing epoxy, and silver-epoxy bonded connections). However, a small amount of uncertainty and hysteresis can still be seen in the corrected capacitance readout, and is thought to be influenced from a number of effects including operation of the electronics at an elevated temperature, epoxy compression and hysteresis, and changing parasitic capacitances from the silver epoxy attachment of the sensor to the PCB.

3.4 Discussion and Summary of Sapphire17 Results

Sapphire17 continued the investigation of sapphire substrate pressure sensors, focusing on both yield and sensitivity improvements. By altering the electrode insulation method, monitoring the surface roughness, controlling the dielectric diaphragm stresses, and refining a conventional dicing method, the final device yield was increased to >80% while simultaneously doubling the sensitivity (63,000 ppm/MPa in Sapphire16 to 133,000 ppm/MPa in Sapphire17) of the high full-scale range (ø100 µm) sensors. The Sapphire17 sensors were integrated into the microsystems and tested at Pau and Vauvert, France in both laboratory (simultaneous 50 MPa and 125°C) and field borehole settings (non-laboratory) to a depth of 1.3 km in a brine well with a simultaneous pressure and temperature of 12 MPa (1,750 psi) and 70°C. The parallelism that allowed for high capacitance response over a wide operating range without loading the capacitance-to-digital readout electronics was due to the great reduction in the parasitic capacitances allowed by the dielectric substrate and small offset capacitance of the sensor as well as the high diaphragm yield.

CHAPTER 4: Full-scale Range and Throughput Enhancements

4.1 Sapphire18 Process Modifications and Improvements

With a more mature understanding of the sapphire process, refinements to further enhance the system integrability, throughput, and full-scale range are investigated. Microsystem sensor integration in the Sapphire15/16/17 iterations involved manual attachment to the PCB with conductive epoxy, which was tedious and easily resulted in failed systems with inaccurate contact pad alignment; automated assembly with commercial placement and soldering systems could greatly reduce these issues. Device singulation (dicing) was laborious with available equipment, as a slow feed rate and low cut depth were required to reduce yield loss; commercial singulation is desired. Additionally, the sensor parameters can be refined (using the fitted Sapphire17 simulations as a baseline) to find a single set of process parameters which could permit the concurrent fabrication of sensors with wide full-scale ranges in both downhole environments (≥50 MPa, 7,250 psi) to biomedical applications (≤50 kPa, 350 Torr).

Therefore, the work for the Sapphire18 process can be summarized as follows: (1) address sensor pad metallurgy to permit the use of automated assembly by meeting commercial sensor bonding/soldering requirements; (2) investigate options for improving die singulation throughput with commercial facilities; and (3) co-design of devices and process parameters to allow extreme full-scale range customization such that a singular set of process parameters can be used to fabricate sensors for operation in environments ranging from harsh downhole (≥50 MPa, 7,250 psi) to biomedical (≤50 kPa, 350 Torr) while maintaining system resolution, device size, and offset capacitance requirements.

4.1.1 Automated Sensor Integration

In order to remove the hand-assembled aspect of the microsystems, commercial sensor mounting during the microsystem's PCB assembly is preferable. Commercial PCB vendors were contacted to determine the sensor size and contact pad metallurgy requirements for automated mounting. The minimum sensor size that the pick and place assembly machine can handle is approximately 0.6×0.3 mm^2. The contact pads need to be 300×300 µm^2 (as the contact pads on the current PCB layout are 350×350 µm^2) with a nickel/gold stack for proper solder wetting. These requirements are summarized in Table 4.1, and were added to the fabrication flow and implemented in the Sapphire18 process. A liftoff process was utilized to deposit the Ni/Au on the contact pads, allowing for the new metallurgy without an additional lithographic step.

Table 4.1: Post-processing requirements

	AllFlex	**FlexPCB**
Minimum Device Size	0.6 x 0.3 mm^2	0.6 x 0.3 mm^2
Contact Pad Size	300×300 µm^2	300×300 µm^2
Exposed Pad Metal	Gold/Tin	Gold/Tin
Contact Pad Metal Stack	Gold/Tin on nickel	Gold/Tin on nickel
Metal Stack Thickness	250 nm Au / 500 nm Ni	250 nm Au / 500 nm Ni

4.1.2 Die Singulation and Separation

While the fabrication of the wafers is completed entirely within the U of M LNF Cleanroom, device singulation still proved to be a cumbersome task, taking many hours to dice just a small portion of the wafer due to the sapphire substrate, which the dicing tool was not designed to handle. In order to expedite the dicing of an entire wafer, commercial dicing companies were assessed to determine their ability to compensate for limited in-house capabilities.

Commercial dicing companies were sent sapphire wafer samples for testing. Conventional dicing (Advotech, Tempe, AZ) resulted in a kerf width of ≈140 µm and average chipping of ≈65 µm, Fig. 4.1 (a). If a dicing street width of ≈300 µm is used, the kerf width and any potential chipping would be accounted for, allowing for little to no yield loss during device singulation.

While laser dicing can be gentler, allowing for a yield increase and reduced kerf, issues were encountered stemming from the transparent nature of the substrate for the services that were utilized (Optec Systems, Greenville, SC). Laser reflection caused the devices to be burned from below and vaporized material was re-deposited onto the top of the sensor, causing destruction of the devices, shown in Fig. 4.1 (b). Due to these issues, the conventional dicing approach was used.

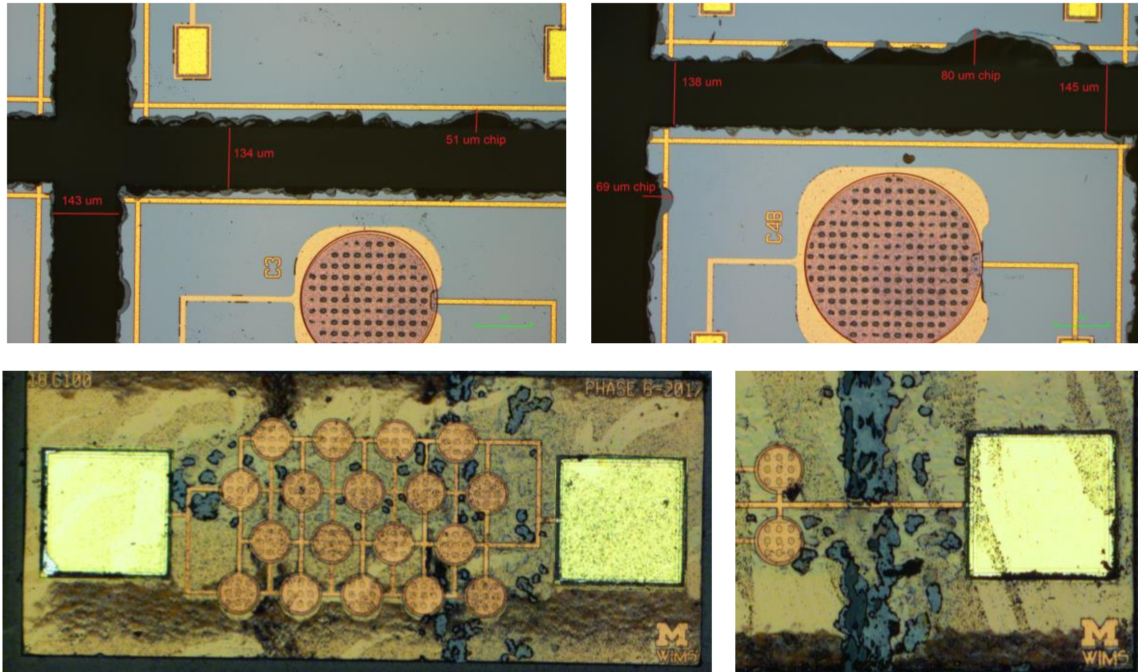

Fig. 4.1: (a, top) Conventional dicing with kerf width of ≈140 µm and chipping of ≈65 µm. (b, bottom) Laser diced sample with device destruction due to internal wafer laser reflection.

4.1.3 Sensor Dimension Refinement

The final major change to the fabrication process was to refine the sensor dimensions (inter-electrode gap, diaphragm diameter, and diaphragm thickness) such that sensors with full-scale ranges extending beyond 50 MPa (7,250 psi) while maintaining ≤50 kPa (7.0 psi) resolution (in a system with 1 fF/code resolution) and below 50 kPa (350 Torr) while maintaining ≤130 Pa (1 Torr) resolution (in the same microsystem) can be created with the same device size and on the same wafer by changing only the diaphragm diameter (a change made at the mask level, requiring no additional lithographic steps). The first set of simulations focus solely on refining the

high pressure and large full-scale range pressure sensors, followed by the refining of the reduced full-scale range pressure sensors. A compromise between these two sets of parameters is then found for use in the final Sapphire18 process.

<u>50 MPa full-scale range sensor refinement study:</u>

Fabrication design constraints were set based on previous experience with fabrication limitations. An inter-electrode gap of no less than 200 nm (any smaller risks diaphragms buckling into the lower electrode during diaphragm sealing) and no greater than 1000 nm (any thicker will necessitate an unreasonably large diaphragm diameter for the reduced full-scale devices, lowering the yield), a diameter of no less than 40 μm (smaller diameters result in very small absolute capacitive changes) and no greater than 160 μm (which can no longer achieve a full-scale range of ≥50 MPa), and a diaphragm thickness of approximately 4.5 μm (as a balance between stiffer diaphragms for larger full-scale range and flexibility for the reduced full-scale range).

Minimum manufacturable diaphragm thickness:

The minimum diaphragm thickness is set by three factors: 1) the minimum ONO thickness to permit structurally sound structures after the XeF_2 release (≈2.0 μm), 2) the minimum NON thickness to seal the etchant access slits (≈1.3 μm), and 3) the ALD Al_2O_3 required to hermetically seal the diaphragm (100 nm). This results in a minimum diaphragm thickness of ≈3.5 μm (including electrode metal). If improved lithography and etching capabilities are utilized, diaphragm thickness can be reduced even further. Thinner etchant access slits defined in the ONO would permit a reduction in the PECVD NON thickness required to successfully seal the slits. For example, if it were possible to reduce etchant access slit width to 0.1 μm and XeF_2 etch parameters could be adjusted to completely remove the sacrificial material through these slits, the NON thickness could be reduced to ≈0.25 μm, permitting a diaphragm thickness of ≈2.5 μm.

Table 4.2: Simulated parameter ranges for ≥50 MPa full-scale range sensor designs

	Minimum	**Maximum**
Inter-electrode Gap	200 nm	1000 nm
Diaphragm Diameter	40 μm	160 μm
Diaphragm Thickness	3.5 μm	6.5 μm

Simulations were run (using the fitted simulation parameters of the Sapphire17 process, Insulation nitride: 75 nm, E: 100 GPa; RMS Roughness R_q=15 nm; upper electrode openings: 3 μm wide rings spaced every 15 μm) to determine both the full-scale range and average capacitance response for varying sensor designs. The full-scale range was determined by the sensors entrance into its saturation region, which results in a tapering slope and diminishing resolution. This was estimated by comparing the instantaneous capacitance response to the average capacitance response – once it had dropped below 33% of the average response, it was said to have reached its full-scale range. Table 4.3 illustrates the full-scale ranges of devices with varying inter-electrode gaps and diameters. It can be seen that as the gap increases and diameter decreases, the full-scale range tends to increase, as would be expected (due to a larger electrode travel distance before saturation and a stiffer diaphragm). Areas highlighted in green indicate a full-scale range of greater than or equal to 50 MPa, while red indicate less than 50 MPa. What becomes immediately clear is that a diameter of ≈100 μm or less is required for this pressure range. With a 130 μm diameter, the maximum full-scale range is 40 MPa with a 1000 nm inter-electrode gap; using such a large gap would require unreasonably large diameters for the reduced full-scale range devices.

Table 4.3: Heat map showing full-scale range as a function of diameter and inter-electrode gap

Gap / Diam.	ø40 μm	ø70 μm	ø100 μm	ø130 μm	ø160 μm
200 nm	60	50	30	20	10
400 nm	65	55	50	25	15
600 nm	>70	>70	55	30	25
800 nm	>70	>70	65	35	30
1000 nm	>70	>70	>70	40	30

Color Key
Range <50 MPa
Range ≥50 MPa

The next area of interest is the device capacitance response, as a higher average response will improve the overall system resolution that can be achieved. The heat map in Table 4.4 shows the average response (over the allowable full-scale range given in Table 4.3), identifying the optimum sensor design as a ø100 µm diameter with an inter-electrode gap of 400-800 nm. Devices with a larger diameter and/or smaller inter-electrode gap have insufficient full-scale range while smaller diameters have small absolute responses, leading to a reduced capacitance response even with small inter-electrode gaps.

Table 4.4: Heat map illustrating average capacitance response (over full-scale range as given in Table 4.3) as a function of diameter and cavity gap

Gap / Diam.	ø40 µm	ø70 µm	ø100 µm	ø130 µm	ø160 µm
200 nm	0.5	5.4	15.6	36.5	60.9
400 nm	0.5	5.5	16.3	31.1	61.9
600 nm	0.5	5.8	17.2	35.0	66.9
800 nm	0.4	4.1	17.5	36.8	65.0
1000 nm	0.3	2.9	15.9	38.7	63.9

Color Key
Range <50 MPa or Resp. <2 fF/MPa
Resp. <4 fF/MPa
Resp. <8 fF/MPa
Resp. >16 fF/MPa

Reduced full-scale range sensor refinement study:

Using the same approach as above, simulations with varying inter-electrode gap and diameter were completed. The same inter-electrode gap limitation was set, but a larger maximum diameter of no greater than ø250 µm was used, as larger (and more fragile) devices have historically had a higher chance of diaphragm failure during sealing and singulation. It can be seen in the Table 4.5 heat map that as the diameter increases and gap decreases, the average capacitance response (over a 50 kPa (350 Torr) range) tends to increase. Due to the relatively small full-scale range of these sensors (in comparison to the designs above), all have a full-scale range of >50 kPa (350 Torr). While there is no isolated peak as with the high full-scale range sensors, it is clear that using larger inter-electrode gaps requires the use of larger diameters and that a 200 nm - 400 nm inter-electrode gap is preferable for the consistent higher responses required for increasing resolution to an acceptable level.

Table 4.5: Heat map illustrating average capacitance response as a function of diameter and cavity gap for reduced full-scale range sensor designs

Gap / Diam.	ø175µm	ø200µm	ø225µm	ø250µm
200 nm	0.55	1.33	1.38	1.70
400 nm	0.54	0.96	1.91	2.08
600 nm	0.16	0.88	1.05	2.12
800 nm	0.05	0.45	1.12	1.13
1000 nm	0.01	0.22	0.66	0.72

Resp. [fF/Torr]	Resol. [Torr]
R≤0.2	R≥5
0.2<R≤0.67	5>R≥1.5
0.67<R≤1.33	1.5>R≥0.75
R>1.33	R<0.75

By simulating a large number of variable parameters, two sets of favored parameters for both types of sensors were found – a ø100 µm diameter, 400-800 nm inter-electrode gap for the high pressure sensors and a ≤400 nm gap and ≥ø200 µm diameter for the reduced full-scale pressure sensors. Using a compromise in the inter-electrode gap of ≈450 nm, it is possible to create sensors for both full-scale ranges that have a minimal reduction in capacitance response, allowing sensor designs to be created to fit specific needs extending from biomedical (≤50 kPa, 350 Torr) to harsh downhole (≥50 MPa, 7,250 psi) environments while also maintaining the specified system resolutions. The process (labeled Sapphire18.0 due to its untested nature) and parameters are given in Table 4.6 and Fig. 4.2.

Table 4.6: Chosen Parameters for Sapphire18.0 Process

Design parameter	**Sapphire18.0**	**Sapphire17**
Lower electrode	400 nm	500 nm
Insulation nitride	100 nm	100 nm
α-Si (inter-electrode gap)	450 nm	1000 nm
Upper electrode	200 nm	200 nm
ONO	150 / 1400 / 150 nm	150 / 1400 / 150 nm
NON	1100 / 400 / 1100 nm	1250 / 500 / 1250 nm
ALD	100 nm	100 nm

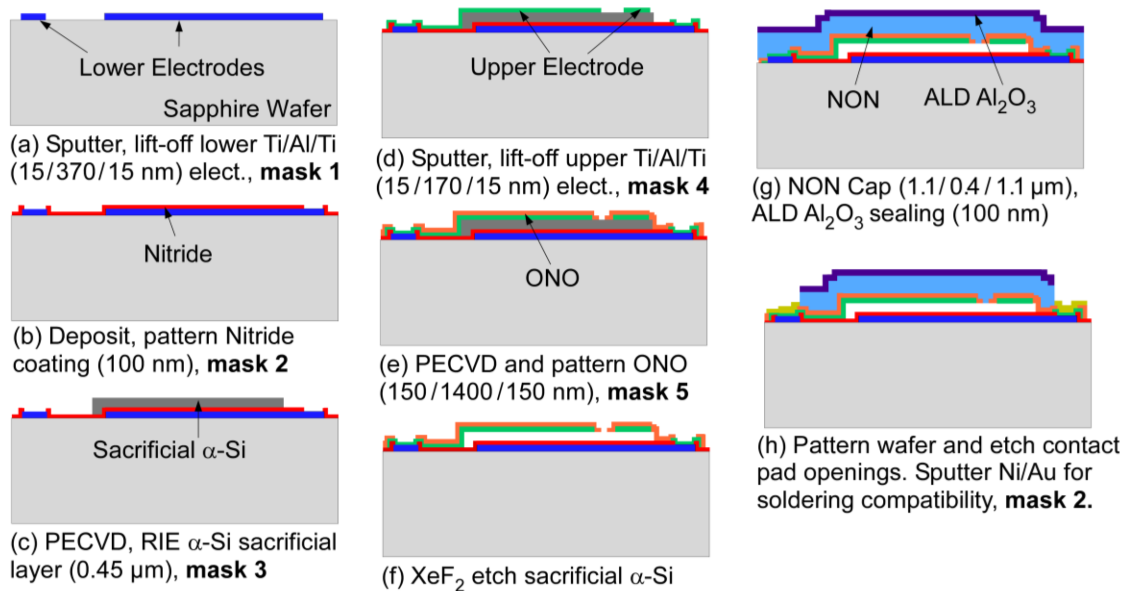

Fig. 4.2: Process sequence for the Sapphire18.0 high-yield/sensitivity/throughput flow.

Sapphire18.0 enhancement summary:

In order to increase throughput and system integrability, commercial conventional device singulation and automated PCB assembly will be employed. By utilizing 300 μm wide dicing streets to accommodate for the observed kerf width and average chipping as seen in the sample in Fig. 4.1, yield loss can be minimized and device singulation can be improved over in-house capabilities. An additional metallization of nickel and gold will be deposited onto the sensor contact pads, allowing for commercial attachment to the system PCB for improved reliability. Using the same lithographic masking step for both contact pad opening and lift-off deposition of the Ni/Au, automated mounting requirements can be met without an additional lithographic step.

Sensor parameters were thoroughly simulated and refined such that a singular process can fabricate devices with full-scale ranges beyond 50 MPa (7,250 psi) and below 50 kPa (350 Torr) (while maintaining high capacitance response and yield) by changing only the sensor diameter.

4.2 Sapphire18.0 Process Challenges

In order to test the throughput and refinement process modifications, a short loop experiment was performed using the proposed Sapphire18.0 parameters to ensure the changes to the inter-electrode gap and diaphragm thickness would not have any unforeseen consequences which may limit yield, capacitance response, or both.

While no device failures were observed during fabrication or dicing, once the fabricated devices were probed, it was found that the C_0 of the devices was much higher than expected. In order to examine the root cause in more detail, devices were cleaved and cross-section SEM micrographs were taken. It was found that the diaphragms had buckled into the insulated lower electrode. However, the buckling of the diaphragms was not due to poor stress control of the thin films (each film had been re-tested for stress values immediately prior to deposition), but rather the re-heating of the released diaphragms to 400°C during the NON sealing (step (g) in Fig. 4.2), as explained below.

In the fabrication process, the 200 nm upper electrode and 1700 nm "pre-diaphragm" of ONO are deposited onto the 450 nm sacrificial layer of α-Si (Fig. 4.2, step e). After etching thin etchant access slits, XeF_2 gas is used to etch the α-Si and free the diaphragms (Fig. 4.2, step f). The stress of the aluminum electrode, silicon dioxide, and silicon nitride were characterized to be low stress (-40 MPa, -120 MPa, and 80 MPa, respectively) with an overall target stress of approximately 50 MPa tensile so as to prevent buckling with a compressive diaphragm and delamination with high stress. However, these stress values are only valid for room temperature; stress is directly proportional to temperature and thermal expansion coefficients [Hua06] due to the dielectric layer's amorphous nature. The NON PECVD capping step is completed at 400°C, which causes the ONO PECVD layers to return to zero stress while the aluminum becomes highly compressive, resulting in a bowing of the thin diaphragms, simulation shown in Fig. 4.3.

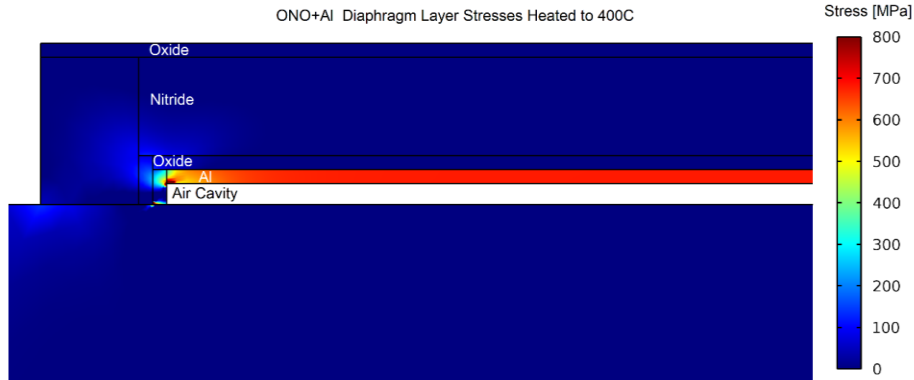

Fig. 4.3: Cross section of interface stress when ONO diaphragm is heated to 400°C

This issue went unnoticed in the previous iterations, as the inter-electrode gap was sufficiently large to prevent the diaphragm from bowing into the substrate during the NON capping. In the Sapphire18.0 process, though, this bowing is captured and becomes permanent by the small amount of re-entrant PECVD "gluing" the diaphragm to the substrate during the deposition, causing an immobilization the diaphragms and higher C_0, shown in Fig. 4.4.

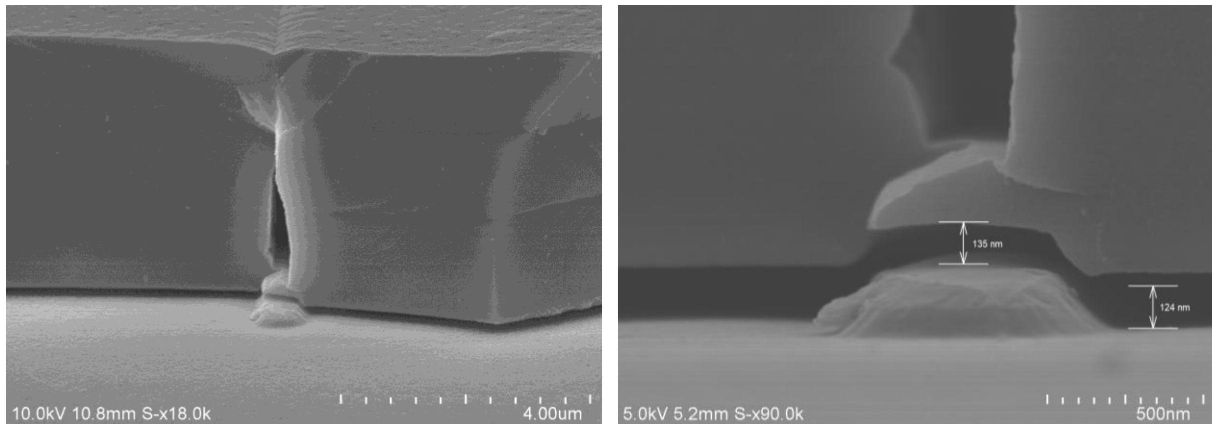

Fig. 4.4: (a) Cross section of etchant access slit. When diaphragm is bowed into substrate during NON sealing, re-entrant PECVD deposits on bottom of slit sidewall and substrate, effectively "gluing" it into place (diaphragm was "freed" during cross-section cleaving).

Another issue discovered in the SEM cross-section micrographs was unremoved α-Si. Because the inter-electrode gap was reduced, the effective etch rate of the XeF_2 on the α-Si was reduced due to a higher flow resistance of the gas entering and exiting the diaphragm cavity. This was corrected by using a longer etch time to allow the XeF_2 gas to travel further into the cavity, as well as a higher XeF_2 gas pressure to alleviate any saturation effect inside the cavity.

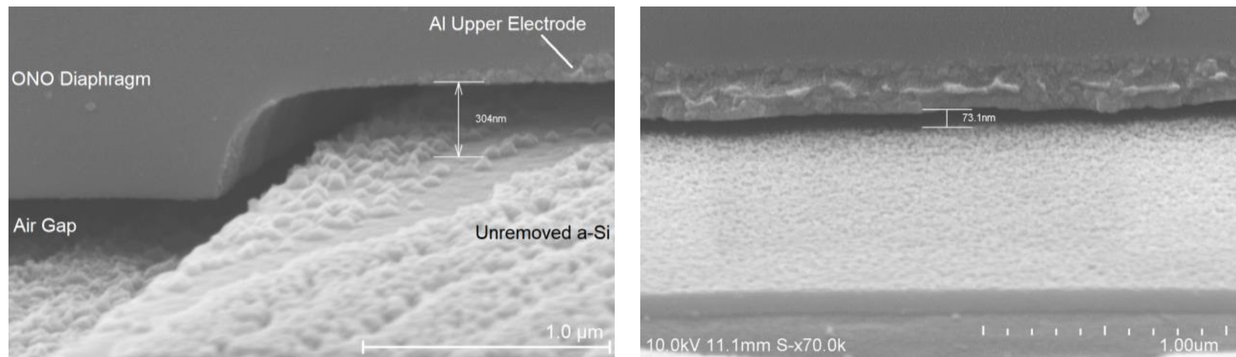

Fig. 4.4: (b) Cross section showing reduced chamber gap of ≈300 nm near device edge (left) and ≈73 nm near device center (right) due to diaphragm bowing as well as a rough lower electrode from incompletely removed α-Si.

<u>Sapphire18 Process Corrections:</u>

In order to prevent the diaphragms from bowing into the substrate during the 400°C NON capping, two changes were made to the process – 1) the upper electrode was modified to include perforations and the outer perimeter was removed to lessen its impact on the diaphragm bending, and 2) the ONO layer was thickened to stiffen it and reduce the bending (while simultaneously reducing the thickness of the NON to maintain a 4.5 µm diaphragm thickness).

<u>Diaphragm Deflection Reduction: Upper Electrode Modifications</u>

Simulations (assuming a ø100 µm diaphragm) with perforations (2 µm wide rings spaced every 10 µm) in the upper electrode and outer 10 µm edge of the electrode removed were shown to alleviate the stress and greatly lessen the bowing of the diaphragm when brought to 400°C, reduced the bending to less than 120 nm, shown in Fig. 4.5.

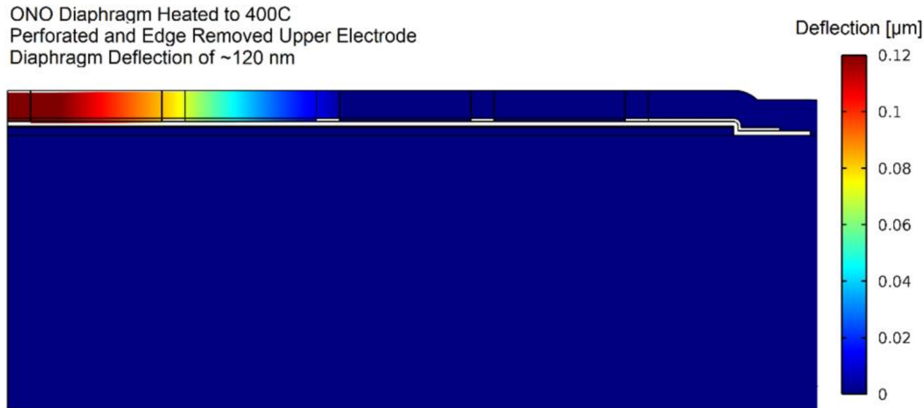

Fig. 4.5: Diaphragm with perforations and outer 10 µm rim removed in the upper electrode resulting in a center deflection of only 120 nm at 400°C.

While removing the outer rim of the electrode theoretically reduced the capacitance response of the sensors, once the sensors are in touch mode, the majority of the capacitance change is due to the central portion of the diaphragm coming into contact with the insulated lower electrode, resulting in a only a minor decrease in capacitance response.

Diaphragm Deflection Reduction Methods: ONO Thickness Increase

The second method used to reduce the deflection of the diaphragm was to increase the thickness of the ONO from 1.7 µm to 2.3 µm. This will stiffen the diaphragm and reduce the impact of the compressive upper electrode. The capping NON thickness can be reduced to as low as 1.25 µm, as the SEM cross sections show that the slits are sealed after ~1.0 µm of PECVD. A NON thickness of 2.0 µm will maintain a safety factor of 2 to ensure complete sealing of all slits while proving the desired overall thickness of 4.5 µm. When this 2.3 µm thick ONO and edge excluded upper electrode are combined, the bending is reduced even further to less than 90 nm, as shown in Fig. 4.6. When these modifications are simulated on a ø200 µm diameter device (with the outer rim removal being proportional to diameter increase – e.g. removing the outer 20 µm rim), the deformation is still limited to approximately 150 nm, allowing for a gap of 300 nm during NON capping.

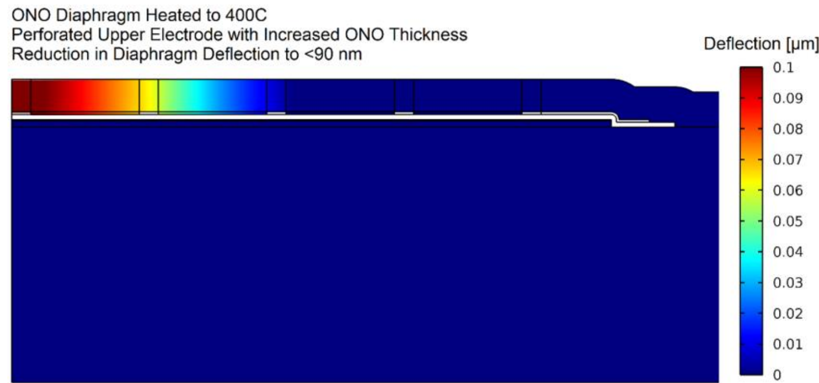

Fig. 4.6: Diaphragm with thicker ONO (increased to 2.3 µm from 1.7 µm) perforations and outer 10 µm rim removed in the upper electrode resulting in a deflection of less than 90 nm.

Sapphire18 Sensor Designs:

With the process issues solved and refined design parameters found, sensor designs were created to meet the system requirements for the large full-scale range (≥50 MPa), high-performance (≤50 kPa (≤7.0 psi) resolution) and for the reduced full-scale range (≤50 kPa) sensors (≤130 Pa (≤1 Torr) resolution). Due to the greatly reduced C_0 and high diaphragm yield afforded by the Sapphire18 process, a near-arbitrary number of diaphragms (within the boundaries of the sensor size) can be parallelized without great impact on the sensor C_0 or device yield (from individually fractured diaphragms resulting in device loss).

≥50 MPa Full-scale Range Designs:

Three designs were created using the optimum sensor diameter of ø100 µm, with a single diaphragm, four parallel diaphragm, and 18 parallel diaphragm design, each serving a purpose. The single diaphragm sensor (C100) is able to meet the minimum system requirements of ≤50 kPa (≤7.0 psi) resolution with the minimum possible active area (<0.025 mm^2) and C_0 (<250 fF). Additionally, it will provide a device with which to better characterize the process, as well as an "insurance" on sensor yield, (should the diaphragm yield be lower than desired). The four parallel diaphragm sensor (4C100) is able to deliver a higher average system resolution while still providing a high probability of sensor yield. The final design consists of 18 parallel ø100 µm

diaphragms (18C100), filling in the entire available sensor area. While this will have the highest active area (≈0.3 mm^2), C_0 (≈4.0 pF), and (theoretically) lowest sensor yield, it will also provide the highest average resolution (3.5 kPa, 0.5 psi) over the full-scale range of ≥50 MPa (≥7,250 psi) with no increase in final sensor size ($1.8 \times 0.8 \times 0.5$ mm^3).

Reduced Full-scale Range Designs:

Two designs were created for the reduced full-scale sensors. From past experience in the fabrication, as the diaphragm diameter increases, the simulated capacitance response and yield deviate from ideal (primarily due to increased inter-cavity surface roughness and increased diaphragm fragility). The first device (8C200) consists of 8 parallelized ø200 µm diaphragms (in order to utilize the entire available sensor area), allowing a theoretical resolution of 20 Pa (0.15 Torr), ensuring that the goal of 130 Pa (1 Torr) resolution will be met.

The second design (12C160) is a more conservative array of ø160 µm diaphragms. A single diaphragm has a simulated average capacitance response of 0.75 fF/kPa (0.1 fF/Torr). However, because they are smaller, 12 diaphragms can be parallelized on a single 1.8×0.8 mm^2 device, allowing for an average capacitance response of 9.0 fF/kPa (1.2 fF/Torr) and resolution of 110 Pa (0.8 Torr) at 1 fF/code, meeting the required specification of 130 Pa (<1 Torr) resolution. While this has a lower safety margin in terms of resolution, the diaphragms are smaller and should allow for increased yield.

Sapphire18 Process Summary:

The total combined fabrication improvements in the Sapphire18 fabrication process included addressing sensor pad metallurgy to permit the use of automated PCB assembly, utilizing commercial die singulation to increase throughput, increasing XeF_2 etch time and pressure to ensure complete removal of sacrificial α-Si, modifying upper electrode topology and ONO

thickness to prevent diaphragm deformation during NON capping, and refining the inter-electrode gap to allow a wide range of potential full-scale ranges. A singular process was used to create sensors (by changing only the sensor diameter) capable of operating with a full-scale range of ≥50 MPa (7,250 psi) and ≤50 kPa (350 Torr) while still maintaining high capacitance response over their respective full-scale range.

When all of these improvements were combined in the final Sapphire18 fabrication run, a fully fabricated and diced device yield of >95% for the large full-scale range sensors and >80% for the reduced full-scale range sensors was achieved (with yield loss due to diaphragm fracture during device singulation as the primary failure mode) while not only maintaining, but also improving, the capacitance response over 30% from the Sapphire17 iteration of the ø100 μm devices. It should be noted that the diaphragm yield prior to device singulation was nearly 100%. Yield loss due to dicing occurred when larger chips caused the PECVD to crack, destroying devices. Larger diaphragm devices are more fragile and susceptible to destruction with smaller chips, hence the larger yield loss. Selected device photos and SEM micrographs of the Sapphire18 iteration devices are shown below. The final Sapphrie18 process is given in Fig. 4.7.

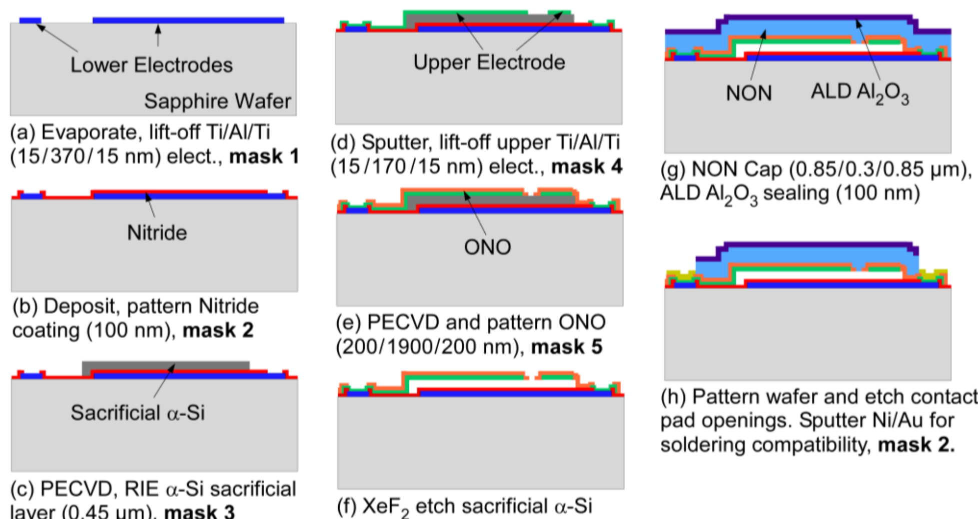

Fig. 4.7: Sapphire18 process used for the high-yield/high-sensitivity/high-throughput flow.

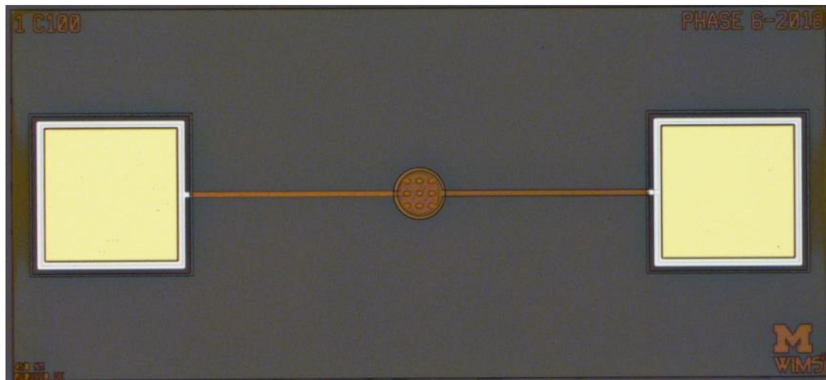

Fig. 4.8: Optical image of full C100 device showing Ni/Au metallurgy on contact pads.

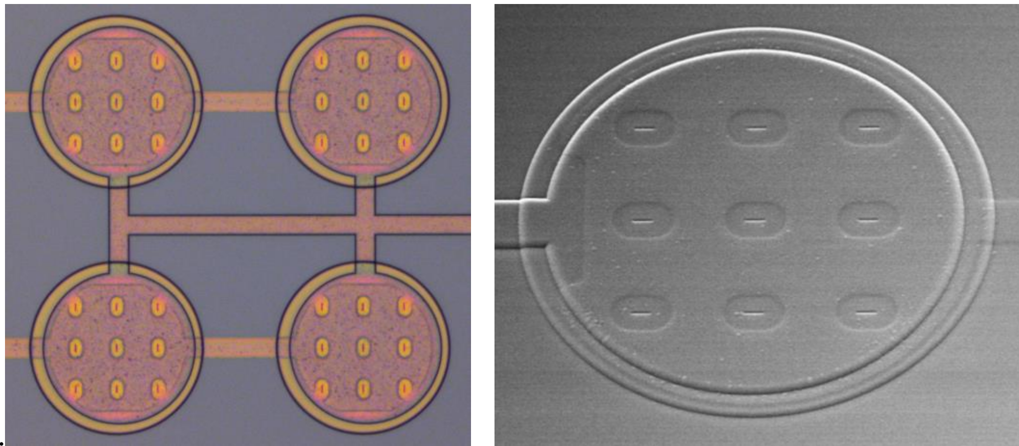

Fig. 4.9: 4 parallel ø100 µm diaphragms and SEM micrograph of ø100 µm diaphragm.

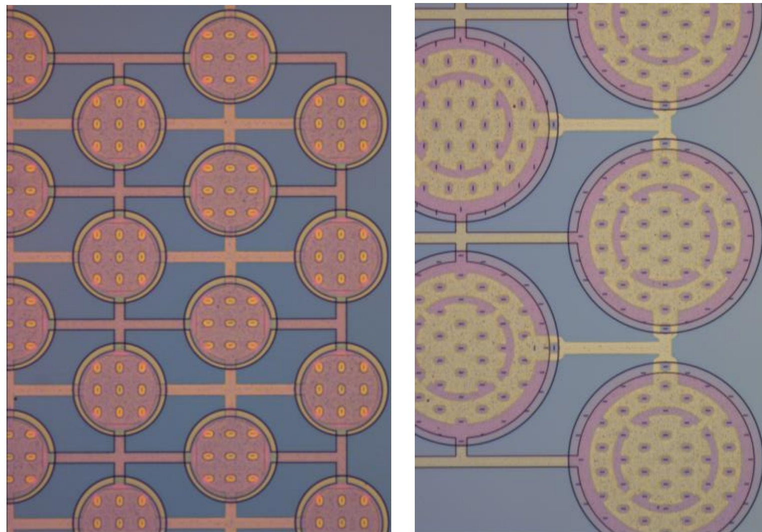

Fig. 4.10: Optical image of parallelized diaphragms. 18C100 device (ø100 µm) and 8C200 (ø200 µm) showing removed outer perimeter and inner perforation of upper electrode.

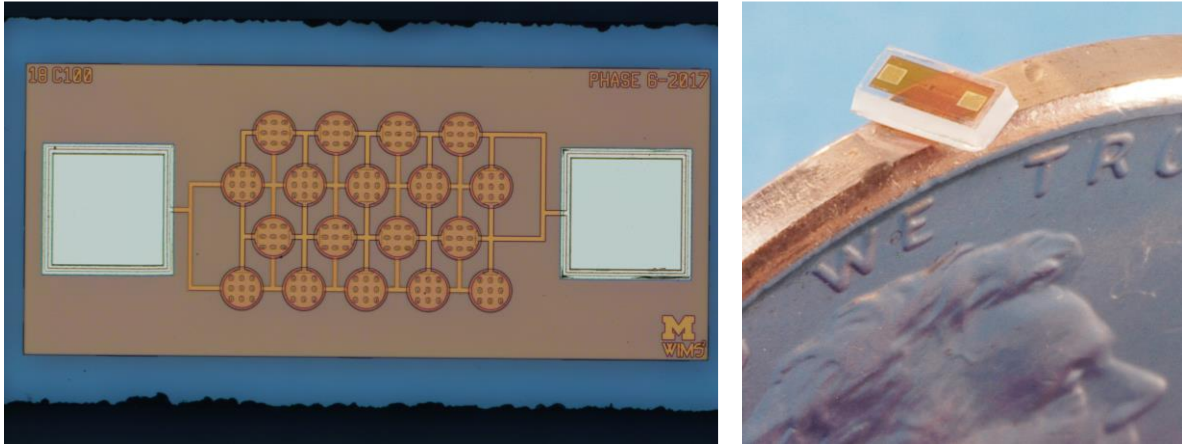

Fig. 4.11: Optical image of commercially diced 18C100 and C100 device on US Penny.

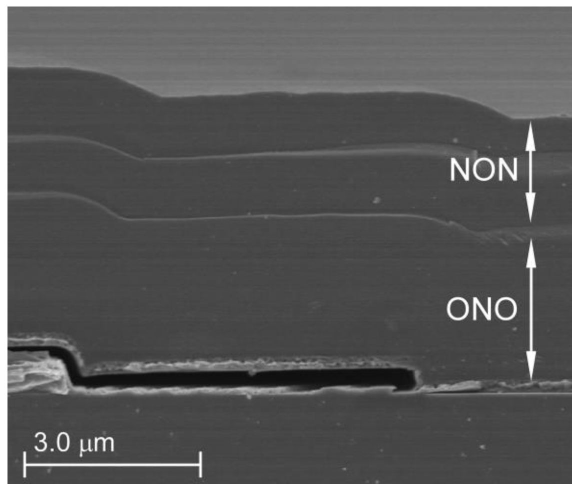

Fig. 4.12: SEM micrograph of cross section of a ø100 µm diaphragm showing inter-electrode gap, upper electrode, and nitride and oxide layers.

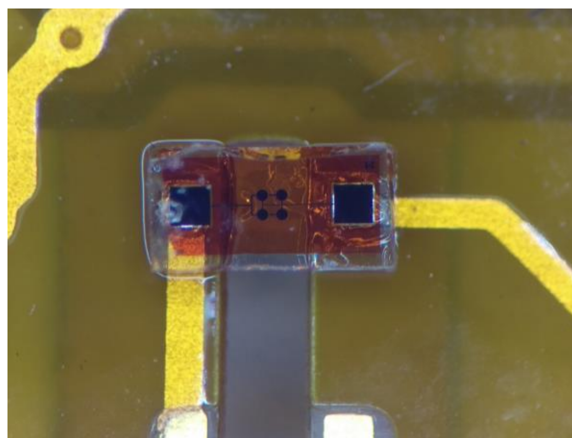
Fig. 4.13: Optical image of 4C100 device commercially mounted onto microsystem PCB.

4.3 Sapphire18 Experimental Results

Large full-scale range pressure sensors (diaphragms measuring ø100 µm) were tested in an oil environment in the same manner previously described (Fig. 2.17). Reduced full-scale range sensors (8C200 and 12C160) were tested in an air environment better suited for the precise application of low pressures. An overview of measured results of the Sapphire18 process and comparison to the previous iterations is provided.

The test results of a single ø100 µm diaphragm device (C100) show a >30% improvement over the Sapphire17 generation, with an average capacitance response of 22.2 fF/MPa (0.18 fF/psi), allowing for an average resolution of 37.5 kPa (5.4 psi) up to 50 MPa (7,250 psi) when integrated into the microsystem.

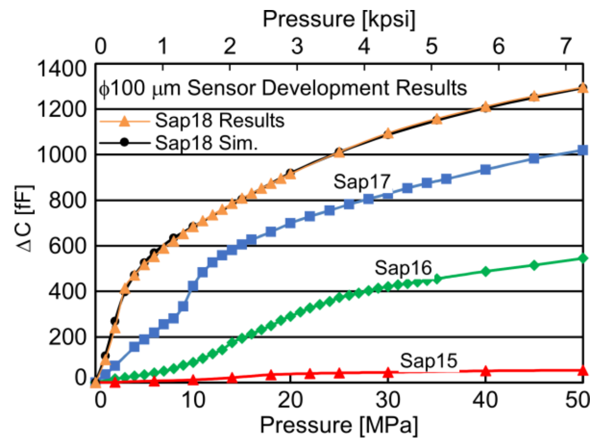

Fig. 4.14: Single ø100 µm diaphragm device (C100) with comparison to previous iterations. Capacitance change in response to applied oil pressure. Sapphire18 matching simulation parameters: Insulation nitride=75 nm, h=4.5 µm; g=0.45 µm; E=80 GPa; Roughness R_q=8 nm; upper electrode openings: 10 µm wide ring @ r=25 µm, no electrode beyond r=40 µm.

The TCO of the C100 device was tested in the same manner as described in section 2.3.1. Due to the slightly different process parameters and reduced chamber gap, the TCO increased slightly to ≈420 ppm/°C (using the experimentally measured 200 fF C_0), Fig. 4.15. It should be noted, though, that the devices showed a temperature response of 0.084 fF/°C, over an order of magnitude lower than the best benchmarked capacitive pressure sensor examined in Chapter 1.

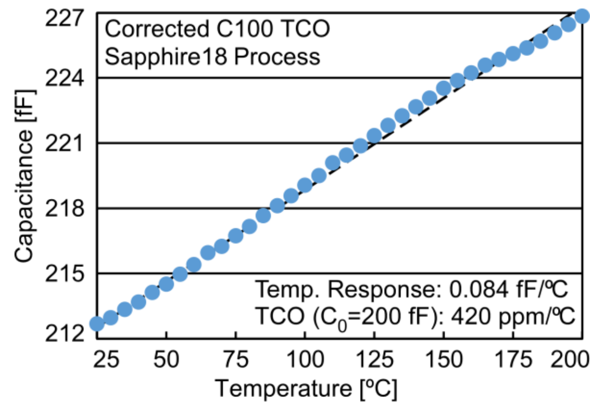

Fig. 4.15: TCO of Sapphire18 C100 device.

In addition to the single diaphragm devices, the four parallel (4C100) and 18 parallel (18C100) diaphragm devices were also successfully tested, displaying near identical responses to the C100 device (albeit multiplied by 4 and 18, respectively). Five devices of each type were tested showing a high degree of response consistency between all devices and designs. The same simulation curve is overlaid on both plots.

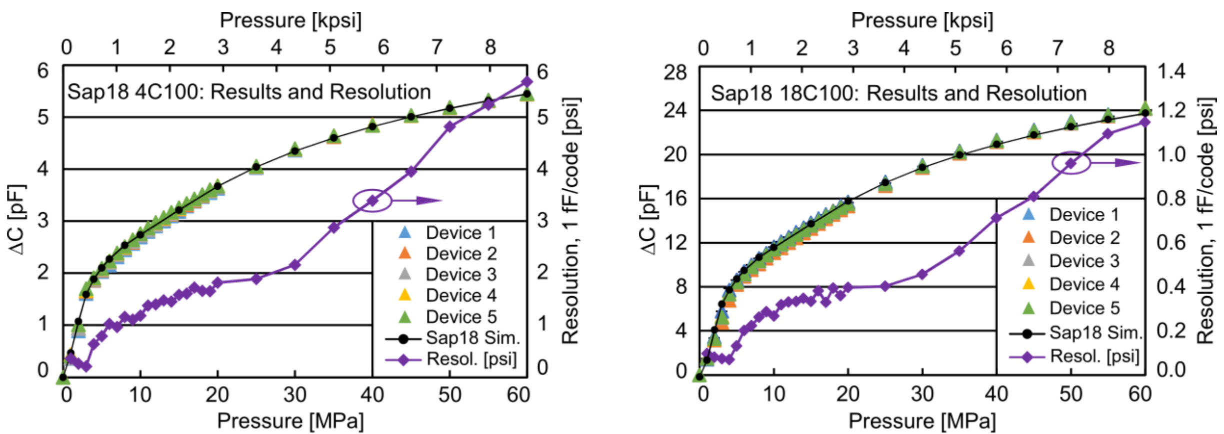

Fig. 4.16: Responses and resoltuion of four parallel-connected (4C100) and 18 parallel-connected (18C100) ø100 µm devices. Capacitance change in response to applied oil pressure. Sapphire18 simulation parameters are identical to the C100 device, Fig. 4.14, but with simulation results multiplied by 4 and 18, respectively. 95% confidence bars not visible at this scale.

The test results of the four parallel ø100 µm diaphragm (4C100) device also shows a >30% improvement over the Sapphire17 generation, with an average capacitance response of ≈103.6 fF/MPa (0.71 fF/psi), allowing for an average resolution of 9.65 kPa (1.4 psi) up to 50 MPa (7,250 psi) when integrated into the microsystem. The 18 parallel ø100 µm diaphragm (18C100)

device does not have a previous generation compliment, as the yield and consistency were insufficient to allow for such a device. It showed an average capacitance response of ≈458 fF/MPa (3.16 fF/psi), permitting an average resolution of 2.2 kPa (0.32 psi) up to 50 MPa (7,250 psi) when integrated into the microsystem.

The reduced full-scale range devices were also successfully tested, demonstrating the capability of the process to fabricate high-sensitivity devices for a full-scale range of 50 kPa (350 Torr) in addition to the high pressure devices shown above. The 12C160 device served as an "insurance" policy, sacrificing capacitance response for a potentially higher yield. It was able to achieve a resolution of <200 Pa (1.5 Torr) up to 100 kPa (700 Torr) with a ≈92% yield, Fig. 4.17.

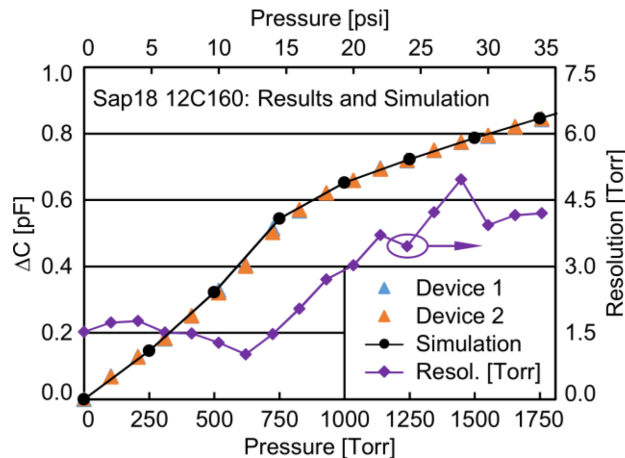

Fig. 4.17: Twelve parallel ø160 µm device (12C160). Capacitance change in response to applied air pressure. Sapphire18 matching simulation: Insulation nitride: 75 nm, h=4.5 µm; g=0.45 µm; E=80 GPa; RMS Roughness R_q=33 nm; upper electrode openings: 10 µm wide rings spaced every 15 µm out to a radius of 60 µm.

The higher capacitance response device, consisting of eight parallel ø200 µm diaphragms (8C200) was able to achieve a resolution of <80 Pa (0.6 Torr) up to a pressure of 50 kPa (350 Torr) (and ≤100 Pa (0.7 Torr) up to a pressure 100 kPa (700 Torr)) with a yield of ≈83%, Fig. 4.18.

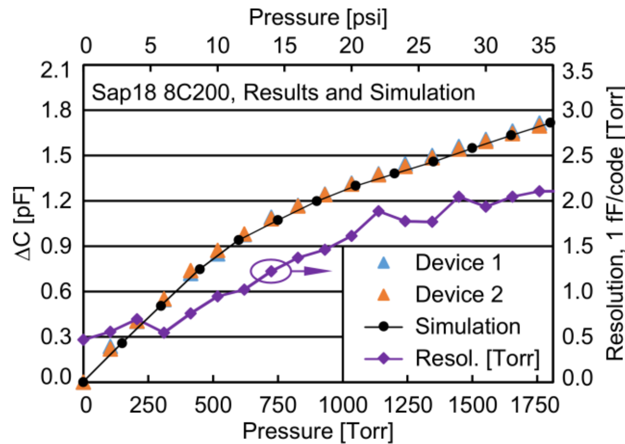

Fig. 4.18: Eight parallel ø200 µm device (8C200). Capacitance change in response to applied air pressure. Sapphire18 matching simulation parameters: Insulation nitride=75 nm, h=4.5 µm; g=0.45 µm; E=80 GPa; RMS Roughness R_q=33 nm; upper electrode openings: 10 µm wide rings spaced every 15 µm out to a radius of 80 µm.

4.4 Discussion and Summary of Sapphire18 Results

By utilizing the lessons learned in both the previous three process iterations and Sapphire18.0 short-loop experiment, it was possible to design a single process permitting the concurrent fabrication of high performance sensors with an extreme degree of full-scale range customizability (greater than three orders of magnitude) while simultaneously adapting it to allow commercial die singulation and automated PCB assembly for a vast increase in potential system integrability and throughput. This permitted the fabrication of sensors that could be used not only in harsh downhole environments with a 50 MPa (7,250 psi) full-scale range while delivering <7 kPa (1.0 psi) resolution, but also in potential biomedical applications with a 50 kPa (350 Torr) full-scale range delivering <80 Pa (0.6 Torr) resolution while maintaining device size (<1 mm^3) and system integrability.

The yield of the smaller diameter (large full-scale range) sensors was greater than 95% while simultaneously increasing the capacitance response by more than 30% compared to the previous generations. The larger diameter devices (≥ø160 µm) had a yield of greater than 80% and the 8C200 device (eight parallelized ø200 µm diameter diaphragms) was able to meet the

system level requirement of a resolution of ≤130 Pa (1 Torr) over a pressure range of 50 kPa (350 Torr). A summary of the devices and goals, their experimentally verified characteristics, and expected resolutions when integrated in the microsystem, is given in Table 4.7.

Table 4.7: Summary of goals and devices fabricated in the Sapphire18 process with estimated pressure resolution in the microsystem with ΔC_{min} = 1 fF/code.

Device	FS Range	Avg. Response	Sensitivity	Resolution	Bits	Yield
Large FSR Goals	*≥50 MPa (≥7250 psi)*	*≥20 fF/MPa (≥0.15 fF/psi)*	---	*<50 kPa (<7.0 psi)*	*>10*	*>90%*
C100 C_0 = 200 fF	50 MPa (7250 psi)	25.9 fF/MPa (0.18 fF/psi)	130k ppm/MPa (893 ppm/psi)	38.6 kPa (5.6 psi)	10.3	>95%
4C100 C_0 = 800 fF	50 MPa (7250 psi)	103.6 fF/MPa (0.71 fF/psi)	130k ppm/MPa (893 ppm/psi)	9.7 kPa (1.4 psi)	12.3	>95%
18C100 C_0 = 3600 fF	50 MPa (7250 psi)	458 fF/MPa (3.16 fF/psi)	127k ppm/MPa (887 ppm/psi)	2.2 kPa (0.32 psi)	14.5	>95%
Reduced FSR Goals	*50 kPa (350 Torr) (7.0 psi)*	*>7.5 fF/kPa >1 fF/Torr (>52 fF/psi)*	---	*<130 Pa (<1 Torr) (0.02 psi)*	*>9.0*	*>80%*
12C160 C_0 = 9.5 pF	100 kPa (700 Torr) (13.5 psi)	5.1 fF/kPa (0.68 fF/Torr) (35.2 fF/psi)	537 ppm/kPa (71.6 ppm/Torr) (3.7k ppm/psi)	196 Pa (1.5 Torr) (0.028 psi)	9.0	>92%
8C200 C_0 = 10.5 pF	50 kPa (350 Torr) (6.8 psi)	13.2 fF/kPa (1.76 fF/Torr) (91.2 fF/psi)	1,257 ppm/kPa (168 ppm/Torr) (8.7k ppm/psi)	75.6 Pa (0.57 Torr) (0.013 psi)	9.3	>83%

CHAPTER 5: Evaluation of the Capacitive Pressure Sensor in a Passive Wireless Sensing System

5.1 Passive Wireless Pressure Sensing

While the capacitive pressure sensors have been developed primarily for the autonomous microsystems previously described, there may be situations where a wired connection to the readout circuitry is not possible. A passive wireless pressure monitoring system utilizing short-range inductive coupling has been developed to evaluate the performance of the sapphire substrate sensors in this use-case. Numerous applications can be environed for this approach, as the readout electronics and power source are typically the limiting factors for harsh environment pressure sensing systems. While the electronics still need to be placed near the passive sensing element, they can be more securely packaged, as a pressure and wired electrical feed-through is no longer required.

A promising application for the reduced full-scale range sensors lies in adding wireless sensing capability to areas within the body, in which pressures typically do not rise above 50 kPa (350 Torr). Often times, pressure sensing can only be measured invasively with catheter-style devices (tethering the patient to cumbersome external equipment and presenting a larger risk of infection [Ogr01]) or require active powered devices (which can require large and potentially hazardous batteries for extended lifetime [Deh05]). General system and sensing requirements for monitoring health conditions in a number of different regions within the body are outlined in Table 5.1, with requirements ranging from a resolution of 40 Pa (0.3 Torr) with a bandwidth of ≥128 Hz to 1300 Pa (10 Torr) with a bandwidth of 1 Hz.

Table 5.1: Bodily pressure monitoring: Estimated requirements of applications and locations

Condition	**Location**	**Pressure [Torr]**	**Resolution [Torr]**	**Bandwidth [Hz]**	**Req. Interr. Range**
Heart failure, disease [Pot08]	Heart (Artery, downstream of stent)	0 – 250	0.3	128	≤30 cm
LAA occlusion [Naj04]	Heart (LAA)	0 – 100	1	64	≤30 cm
Hypertension [Pot08]	Heart (Artery)	20 – 250	2	20	≤30 cm
Motility disorder [Van86]	GI tract	0 – 250	1-10	>1	≤20 cm
Incontinence, others [Maj11]	Bladder	0 – 50	1-10	>1	≤20 cm

While many active or energy harvesting inter-body wireless pressure systems have been developed over the years, few have been commercialized. One successful example, though, is SmartPill, a system for monitoring GI tract pressure and transit time [Has14], which is a swallowable pill (ø11.7 × 26.7 mm^3) with on-board electronics and battery for active transmission of the collected data to a base station. It is capable of measuring pressure (at 1-2 Hz with 10-35 Torr resolution up to 350 Torr), temperature (at 1.5-3 Hz with 2°C resolution between 25-49°C), and pH (at 0.5-12 Hz with 1 pH resolution between 0.5-9.0 pH) for at least five days An example of a batteryless, power harvesting (albeit non-commercialized) system is an implantable blood pressure monitoring device in which the sensing element (ø1.0 × 5.6 mm^3) is inserted directly into the bloodstream while the readout electronics (ø20 × 4.0 mm^3) are placed subcutaneously (connected to the sensor via a 200 mm long data cable) to allow for easier remote powering and data transmission [Cle12]. It is capable of measuring pressure (at 30 Hz with 1 Torr resolution up to 350 Torr) and temperature (between 15-45°C). The subcutaneous portion of the device is inductively linked to an external base station, which is responsible for both remotely powering the device and receiving the collected data.

However, foregoing the use of batteries and active electronics altogether by directly transmitting the pressure sensor data via passive inductive coupling would be desired (to improve system lifetime and biocompatibility). Taking advantage of the capacitive nature of the sensor, the most logical approach for a passive wireless sensing system is an LC resonator, where the resonance frequency is dependent on the pressure applied to the sensor. However, in addition to accurately detecting the sensor capacitance (e.g. the resonant frequency and thus applied pressure), attention must also be paid to the system readout bandwidth so transient pressures can be captured with enough accuracy to be of sufficient use to the physician [Van86].

One of the most successful completely passive wireless pressure sensing systems is that developed by CardioMEMS. It is a designed to monitor blood pressure to detect abdominal aortic aneurysms and heart failure. The system is formed from two fusion-bonded fused silica wafers, measures $30 \times 5 \times 1.5$ mm^3, and has a stated 20 cm interrogation range and 1 Torr resolution. However, the device was designed and targeted at a specific niche application of pressure sensing on the exterior of an artery or endovascular repair stent in order to detect heart failure [Van16]. This has allowed it to see clinical success, but is unsuitable for use in other areas of the body due to its size, fragility, and need for proper alignment for readout (which can be assured due to it known placement and orientation on the stent). Systems shown in Fig. 5.1.

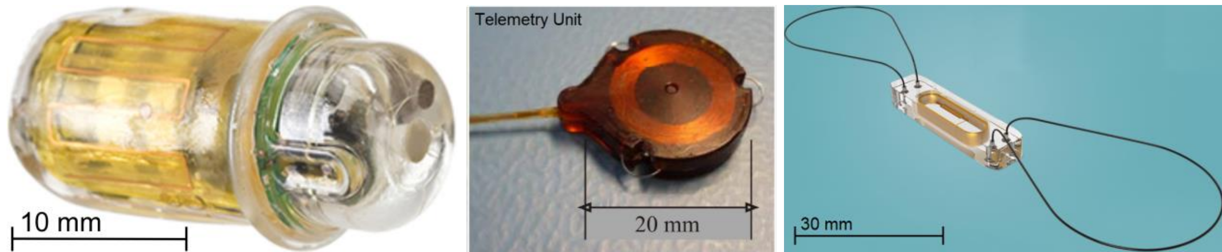

Fig. 5.1: Images of SmartPill [Med18], Blood pressure monitor [Cle12], and CardioMEMS [Sjm18] devices.

Due to the ability of CardioMEMS to find success in a specific sensing regime, targeting a single application is perhaps the best route when designing a biomedical passive wireless system. While SmartPill has had success in GI tract pressure monitoring, it leaves room for improvement in pressure sensing resolution and bandwidth, only capable of 10-35 Torr resolution at ≤2 Hz. If the size, resolution, and bandwidth could be improved (≤2 Torr at ≥64 Hz), it would be possible to more accurately monitor the transit pressures at important junctions in the GI tract, such as the transition between the mouth and stomach, stomach and small intestine, and large intestine and excretion [Cas08]. Additionally, implantation considerations would be greatly simplified, as the system need only be swallowed, removing the requirement for more invasive catheter implantation techniques and antithrombogenic coatings for intravascular insertion of sensing elements [Has14]. It would also allow for a relatively large device diameter (and thus sensor inductor), permitting increased readout distance over use-cases in which size reduction is necessary for implantation.

Focusing on passive (i.e. LC Tank resonance) systems, a benchmarking table of all influential work utilizing passive wireless communication (and the active SmartPill system) is given in Table 5.2, including all reported relevant sensor and system parameters such as size, pressure resolution, readout range, and readout bandwidth, when given.

Table 5.2: LC Tank benchmarking of published and commercial MEMS wireless readout pressure sensors

	Size [mm^3]	Vol. [mm^3]	P. Range [Torr]	Range [mm]	Resolution [Torr]	[Bits]	BW [Hz]	C_0	C Rsp. [fF/Torr]	Ind.	Q	f_0 [MHz]	Freq. Rsp. [kHz/Torr]
Col67	ø5 x 2	39.3	0 – 100	30 (s)	1	6.6	-	700 fF	-	2.5 μH	-	105	300
Fon06 (CM)	30 x 5 x 1.5	225	-20 – 300	200 (s)	1	8.3	200	4.5 pF	3	5 μH	50	35	10
Tak03	ø3.5 x 4	38.5	0 – 800	<1 (s)	50	4.0	-	18.5 pF	5.0	20 nH	-	201	0.5
Tak06	ø3.5 x 20	192	0 – 60	<1 (s)	5	3.6	-	12.5 pF	2.0	55 nH	-	225	57.4
Aka01	2.6x1.6x1	4.2	0 – 50	2 (a)	10	2.3	-	3.65 pF	13.0	1.2 μH	8	73	120
Tak08	4 x 2.4 x 1	9.6	0 – 2625	<1 (s)	50	5.7	-	6.3 pF	0.2	640 nH	1.9	38.6	0.15
Deh02	6 x 6 x 0.5	18.0	400-1000	30 (a)	1	9.2	-	48 pF	20	3.7 μH	30	12	3.2
Ros92	5 x 5 x 1	25.0	0 – 200	22 (a)	25	3.0	-	29.7 pF	8.5	450 nH	5.5	43.1	5.3
Bal03	10x10x0.6	60.0	0 – 750	<1 (a)	50	3.9	-	14.8 pF	-	1.7 μH	5.4	32.5	1.3
Rod08	4 x 2 x 1	8.0	0 – 50	<1 (a)	1	5.6	-	8.5 pF	-	0.8 μH	3	72	400
Saa10	ø4 x 1	12.6	0 – 100	10 (s)	1	6.6	-	5.9 pF	3.5	57 nH	6	250	78
Tee14	3 x 3 x 1	9.0	0 – 100	3 (s)	10	3.3	-	0.60 pF	1.4	20 nH	--	1386	1400
Chi13	7 x 5 x 6	210	0 – 50	<1 (s)	1	5.6	-	5.0 pF	2	1.1 μH	6	63.4	15
Xue12	3x1.5x0.5	2.4	0 – 60	3 (s)	1	5.9	-	0.9 pF	8.8	515 nH	20	210	680
Luo14	ø10 x 2	157	0 – 225	3 (a)	35	2.7	-	4.7 pF	8.9	1.9 μH	-	49	38.7
Che13	ø14 x 1	154	0 – 35	25 (a)	1	5.1	1	9.2 pF	4.7	0.2 μH	-	114	23
Don15	22 x 22 x 1	484	375 – 825	2 (a)	7	6.0	-	8.5 pF [Mur13]	5.6	320 nH	-	93	17.8
Lee16	ø5 x 10	196	7 – 75	20 (s)	7	3.3	0.5	975 fF	0.7	2.0 μH	3	115	304
Has14 (SP)	ø12 x 26	3000	0 – 350	1400	10-35	4.5	1-2	-	-	-	-	434	-
Goals	**<ø12 x 24**	**<3000**	**0 – 350**	**100**	**<1**	**>8**	**>64**	**10.5 pF**	**1.75**	**≈5 μH**	**>100**	**≈20**	**>1.5**

Legend:
(a) Air tested result, (s) Saline tested result
CM: CardioMEMS System
SP: SmartPill (Active Device)
‘ – ’ Parameter not tested or given in work

5.1.1 Wireless Passive Sensing System Design

This section will cover the design of the interrogation system, focusing on its ability to interrogate the sensor with sufficient bandwidth and accuracy. The primary system components of the passive sensing system will include the inductively coupled LC Tank circuit (namely the capacitive pressure sensor and coupled inductor coils), interrogation frequency/voltage source, resonant frequency detection circuitry, output digitization (ADC), and software control.

Therefore, the wireless system can be broken into several required components: (1) capacitive sensor design for 350 Torr full-scale range; (2) sensor and external readout coil design; and (3) external circuitry and software design for frequency interrogation with sufficient speed to deliver the required bandwidth and resolution.

1) Capacitive Pressure Sensor Design:

While a capacitive pressure sensing element is perhaps the most important component of the system, the design, fabrication, and pressure verification were thoroughly explored in Chapter 4. The highest performance sensor consisted of eight parallel connected ø200 μm diameter diaphragms (8C200), allowing for an experimentally verified capacitance response of ≈1.75 fF/Torr (over a 0-350 Torr pressure range) with a C_0 of ≈10.5 pF, shown in Fig. 4.18.

2) Sensor and External Readout Coil Design:

An analysis of a simplified coupled inductor circuit and design of the inductor coils is presented below.

Mutual Inductance and Resonant Frequency Circuit Analysis:

When the two inductor coils are coupled as shown in Fig. 5.2, the resonant frequency of the sensor will manifest itself as a peak in the frequency-dependent complex impedance (e.g. phase between the applied voltage and resultant current) of the readout coil [Tak04]. However, the

magnitude of this phase dip is dependent on the mutual coupling between the coils (proportional to the separation distance and environment between the coils, as well as their physical geometry) and quality factor of the sensor tank (e.g. resistive losses of the sensor and readout coils) [Bal03]. A simplified circuit model of this coupled system is shown in Fig. 5.2, where C_p / R_{LRO} and C_{ps} / R_{LS} are parasitic capacitance and resistances of the readout coil and sensor, respectively, and M is the mutual inductance between the readout and sensor coil antennas.

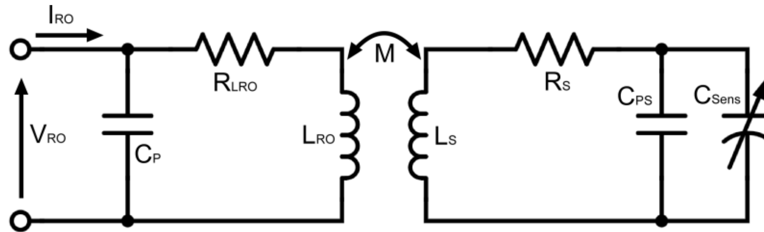

Fig. 5.2: Typical LC Tank circuit model illustrating input voltage and resulting current, parasitic resistances and capacitances, and mutual coupling.

In order to analytically assess the impact of both the readout coil and sensors quality factor and mutual coupling, the equivalent circuit is solved for input impedance. To further reduce equation complexity, the parasitic capacitance on the readout coil can be ignored as long as the resonant frequency of the readout coil is above the resonant frequency of the sensor [Nop11]. (If the resonant frequency of the coil is near the sensor's f_0, it will mask the phase dip of the coil; if it is below the sensor's f_0, the phase dip will be greatly reduced.) With this assumption, the input impedance of the readout coil can be solved, given in equation (5.1).

$$Z_{RO} = \frac{V_{RO}}{I_{RO}} = R_{LRO} + j\omega L_{RO} + \frac{(\omega M)^2}{R_S + j\left((\omega L_S) - \frac{1}{\omega(C_{Sens} + C_{ps})}\right)} \tag{5.1}$$

In order to obtain a better grasp of the physical meaning of the derived equation, substitutions for the coupling coefficient, *k*, quality factor, *Q*, and undamped resonant frequency of the sensor, f_0, can be made so that their effect on the phase dip can be better understood.

$$k = \frac{M}{\sqrt{L_{RO} L_S}} \tag{5.2}$$

$$Q = \frac{1}{R_{LS}} \sqrt{\frac{L_S}{(C_{ps} + C_{Sens})}} \tag{5.3}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_S(C_{ps} + C_{Sens})}} \tag{5.4}$$

While the eventual extracted characteristic of the input impedance of the coil will be the phase (given by the inverse tangent of the imaginary portion divided by the real portion of the impedance), this phase dip "information" is contained in the real portion of the impedance [Nop10], given in equation (5.5) with the above substitutions for k, Q, and f_0.

$$Re\{Z_{in}\} = R_{RO} + (2\pi f L_{RO} k^2 Q)\left(\frac{\frac{f}{f_0}}{1 + Q^2\left(\frac{f}{f_0} - \frac{f_0}{f}\right)^2}\right) \tag{5.5}$$

A further simplification can be made by removing the readout coil resistance, R_{RO}, as it serves only to offset the phase dip, affecting neither the magnitude nor shape, shown in equation (5.6).

$$Ph\{Z_{in}\} \propto Re\{Z_{in}\} \propto \frac{2\pi f L_{RO} k^2 Q \left(\frac{f}{f_0}\right)}{1 + Q^2\left(\frac{f}{f_0} - \frac{f_0}{f}\right)^2} \tag{5.6}$$

Examining equation (5.6), it can be seen that the two primary factors influencing the magnitude (and thus signal to noise ratio) of the phase dip are the quality factor (linearly proportional to Q) and coupling coefficient (proportional to k^2). Therefore, it is of vital importance that the coupling be maximized to maintain a large phase dip peak and that the Q be maximized to both increase and sharpen the phase dip peak for better detection and isolation in a noisy environment. Examples of the phase dip with varying sensor Q and coupling factor are given in Fig. 5.3, illustrating the effects on the resulting extracted phase dip on the readout coil.

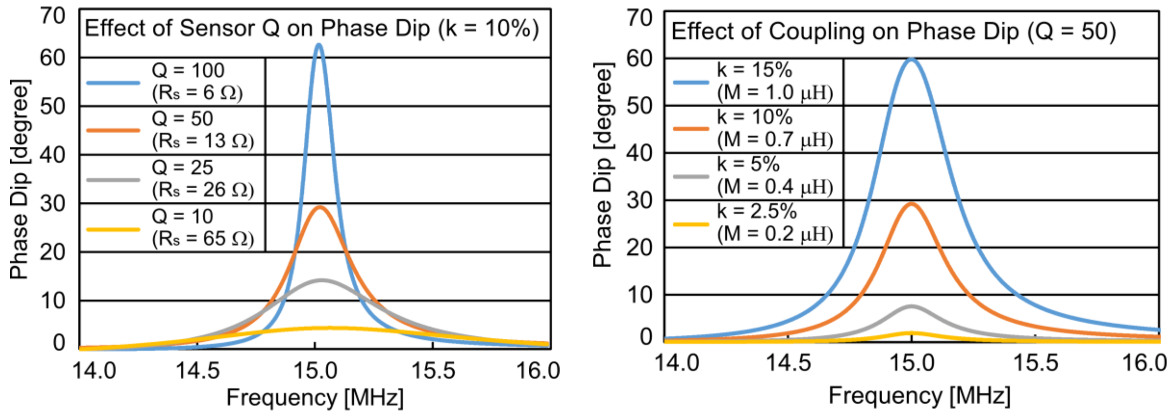

Fig. 5.3: Example of phase response on readout coil for varying sensor quality factor and coupling coefficient using an example circuit with $L_{RO} = L_S = 7\ \mu H$, $C_{PS} = 16.1$ pF.

Sensor and Readout Coil Design:

The first parameter that must be set is the maximum size of the ingestible capsule in which the pressure sensor and coil will be housed. Using the SmartPill as a base of reference, the capsule was set at an outer diameter of no greater than ø12 mm and height of no greater than 24 mm. The primary structure consists of an outer shell to protect the inductor coil and sensor and an inner guide rod on which the inductor coil can be wound and the pressure sensor can be placed. The outer shell is a 0.5 mm thick case with perforations at one end to allow for pressure transfer to the sensor. The insert has a recess in the bottom to allow the pressure sensor to be placed and through hole slits to allow for an inductor to be wrapped horizontally (normal to the x-axis) as well as vertically (normal to the z-axis). This dual axis design will allow for increased coupling to the readout coil due to imperfect sensor orientation with only minimal reduction in coupling on the inner coil due to the outer coil partially obstruction its turns. The insert diameter was set to fit into the shell once the inductor coil was wound, resulting in a final diameter of 10.5 mm and usable length of 17 mm, while the through-holes are 5.2 mm wide and spaced 18.5 mm apart. Threads are used to connect the insert and shell. Structure images are shown in Fig. 5.4.

The coil sizes and effective diameters are limited by the insert; the vertical (z-axis) coil has a maximum diameter and height of ø10.5 × 17 mm, while the horizontal (x-axis) coil is similarly limited to the groove width and spacing at 5.2 × 9.0 × 18.5 mm. While the spacing, number of turns, and wire diameter can be adjusted for maximum efficiency, the largest effective diameters are used in order to maximize coupling, as the coupling between a larger coil and smaller coil will increase as the smaller coil's diameter is increased [Pic04]. The readout coil is not constrained in size by implantability concerns, but rather usability; therefore, it was set in size to approximately 10 × 15 cm^2 (approximating the size of a typical cell phone) so as to not be too cumbersome to use while still being able to sufficiently couple to the sensor coil without perfect alignment [Raj14].

The housing and insert structure were fabricated using a ProJet MultiJet 3D Printer (MJP) with M3 Crystal, a biocompatible, acrylic-based resin. Unlike the typical 3D printed manufacturing technology of Fused Deposition Modeling (FDM) (where an object is built by selectively depositing melted material), MJP utilizes multiple jets to apply a layer of liquid resin which is cured using UV light, creating parts with greater strength and resolution [3DS18].

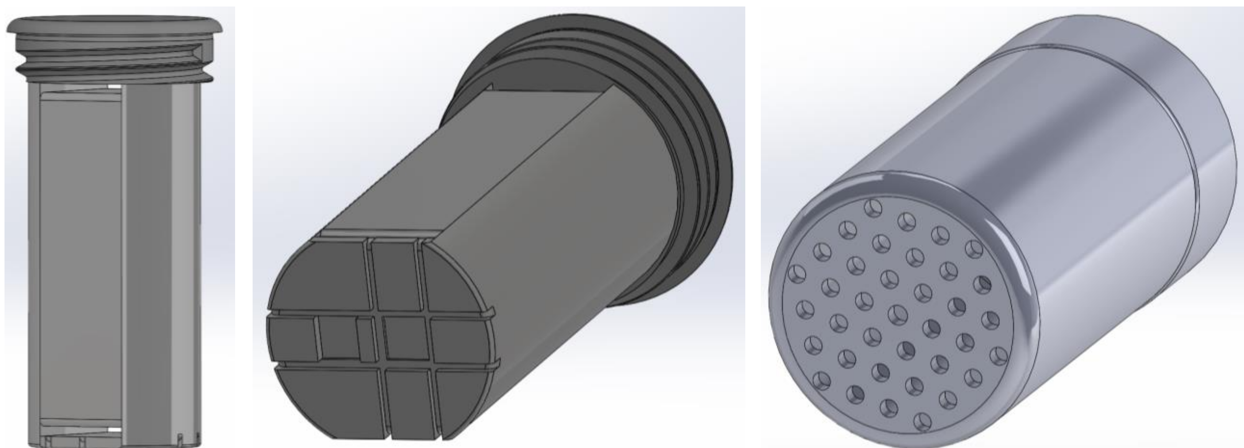

Fig. 5.4: 3D model of LC tank structure showing capability of wire to be wrapped around vertically (z-axis) and through the structure (x-axis), indents and grooves for sensor placement and wire routing on the bottom of the structure, and housing with pressure thru-holes.

With the boundary condition sizes of the inductor coils set, their design could be refined. In order to expedite the initial design, numerical estimation methods using the physical parameters of the coils (coil diameter / height, number of turns, wire diameter, turn spacing, coil separation distance) were used to approximate the sensor and readout inductance [Moh99, Whe28], AC resistance [Whe42], and mutual coupling [Pic04], equations (5.7-5.10), MKS units used for all inputs. These values were then substituted into the equation obtained by solving for the input impedance of the circuit shown in Fig. 5.2 to predict the expected phase dip on the readout coil.

$$L\ [\mu H] = \frac{31.5 * (radius)^2 * (n)^2}{(6 * radius) + (9 * height) + (10 * depth)}, Helical\ coil \tag{5.7}$$

$$L\ [\mu H] = (1.94)(d_{out}^{-1.21})\left(d_{avg}^{2.4}\right)(w)^{-.147}(n)^{1.78}(s)^{-0.03}, Planar\ coil \tag{5.8}$$

$$R_{AC}\ [\Omega] = \frac{Resistivity * Length}{\pi * (skin\ depth) * (2 * Wire\ Radius - skin\ depth)} \tag{5.9}$$

$$M\ [H] = \left(\frac{\mu_0 \pi n_{RO} n_{Sens}}{2}\right)\frac{(Radius_{Sensor})^2 (Radius_{RO})^2}{(R_{RO}^2 + Dist^2)^{1.5}} \tag{5.10}$$

As mentioned previously, it is necessary that the resonant frequency of the readout coil be greater than that of the sensor. If this is not true, the phase dip of the sensor will be greatly diminished, reducing the readout efficacy. Therefore, the diameter and number of turns cannot be arbitrarily increased on the readout coil to maximize the coupling and phase dip. The sensor's resonant frequency is expected to be ≤20 MHz ($L_S \geq 5$ µH, $C_{tot} = (C_{PS} + C_{par}) \geq 15$ pF); therefore, the resonant frequency of the readout coil was limited to ≥25 MHz (assuming a parasitic capacitance of ≈2.5 pF). If the trace width on the readout coil is set at 0.5 mm wide (to reduce the parasitic capacitances and maintain a low coil resistance), this leaves the diameter, spacing, and number of turns for coupling improvement. With these limitations, the resulting maximum coupling can be achieved when the coil traces utilize the maximum area of the coil (e.g. inner diameter ≈0) and most number of turns while maintaining a low enough inductance

(L_{RO} ≤16.2 μH) to keep the resonant frequency ≥25 MHz. With this limitation, the readout coil will, for all diameters near 10-15 cm, have approximately the same inductance (≈16.0 μH), number of turns (15-20), and similar coupling capability.

While there are no such frequency limitations on the sensor coil, it would at first seem that the maximum diameter and number of turns should be used. Utilizing only equation (5.10), this is indeed true; however, one major concern related to tightly wound inductors (that is very difficult to accurately model) is the proximity effect, which greatly increases the series resistance of a coil.

Once this rough refinement (ignoring the proximity effect) of the coils was completed, computationally expensive FEA using the 2D axi-symmetric electromagnetic module of COMSOL was conducted to confirm the numerical estimations and account for the reduction in coupling due to the semi-conductive nature of the blood environment between the coils [Hir50]. The final coil parameters were Readout coil: 10×15 cm^2 in size, 0.5 mm wide trace, 2.0 mm trace spacing, 18 turns, 15.5 μH; Sensor coil (z-axis): 1.05 cm diameter, 28 AWG (ø0.321 mm) wire, 17 mm height, 50 turns, 9.3 μH, 1.4 Ω (ideal straight wire resistance), and Sensor (x-axis): 14 turns, 4.3 μH, 0.6 Ω. This allowed for a phase dip of >0.2° at a readout distance of 10 cm (when coil axes are properly aligned) in the conductive environment. (While the sensor coils have different diameters and number of turns, their coupling is approximately the same.)

Proximity Effect:

A major damping factor in wire wound inductors is the "Proximity Effect" which increases the series resistance in the wire beyond the standard straight wire skin depth effect [Dow66]. It arises when the magnetic field from parallel turns further constrain the skin depth. This is exacerbated as the number of layers in a coil increases; as shown in the Fig. 5.5, the resistance of a coil with a single layer (m=1) is much higher than the AC resistance of a straight wire of the

same length [Fer94]. (f_{NORM} = 1: frequency at which the skin depth and wire diameter are equal). At 10 MHz with a 35 AWG wire, (f_{NORM} = 50) the resistance would only be ≈2 times its DC resistance in a straight wire; however, it is approximately 10 times its DC resistance in a coil with one layer and >500 times its DC resistance in a four layer coil.

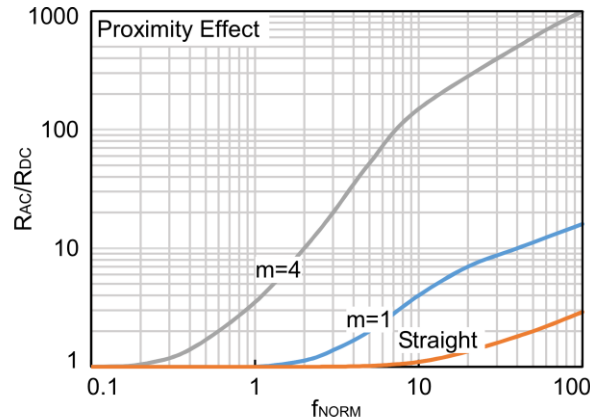

Fig. 5.5: Resistance for a straight wire and one (m=1) and four (m=4) layer inductor

Unfortunately, (apart from assuming tightly wound, multi-layer inductors) the proximity effect is extremely difficult to accurately model due to an extreme dependency on the physical layout of the coil turns. However, in order to minimize this effect, a few approaches can be used. As with all wires at high frequencies, its resistance is approximately proportional to its circumference, not area. As the wire diameter increases, the resistance will always reduce; however, the proximity effect constrains the skin depth even further, exaggerating the effect of wire circumference on resistance, shown in Table 5.3. Therefore, it is necessary to use a larger diameter wire with a single layer in order to reduce the resistance as much as possible.

Table 5.3: Wire resistances (one meter wire length) at 10 MHz

AWG	Diameter [mm]	f_{NORM} [MHz]	R_{DC} [Ω]	R_{AC}, Ideal [10 MHz]	R_{AC}, m=1 [10 MHz]	R_{AC}, m=4 [10 MHz]
28	0.321	0.04	0.207	0.86	4.97	217.4
32	0.202	0.10	0.524	1.42	8.64	366.8
35	0.143	0.20	1.045	2.10	11.50	522.5

The other method that can be used to reduce the proximity effect is to simply reduce the parallel traces proximity to one another. By increasing the distance between each trace, the parallel magnetic field affecting the adjacent turns will be reduced. Four physical inductors (normal to the z-axis) were created using 28 AWG (ø0.321 mm) on the 10.5 mm diameter 3D printed insert shown in Fig. 6.4 (using a 15 pF capacitor to create an LC Tank). The first design consisted of a tight wrap with no gaps between the turns (50 turns), the second design spaced the wires such that there was a gap equal to the diameter of the wire between each turn (25 turns), the third used groups of two (35 turns), and the fourth used groups of three (40 turns). Not considering the increased resistance, more turns should increase the coupling and phase dip. However, as the resistance increases more rapidly due to the proximity effect, the design with the greatest balance between turns (e.g. increased coupling) and resistance (e.g. increased damping and reduced quality factor) was the design with groups of two, shown in Fig. 5.6.

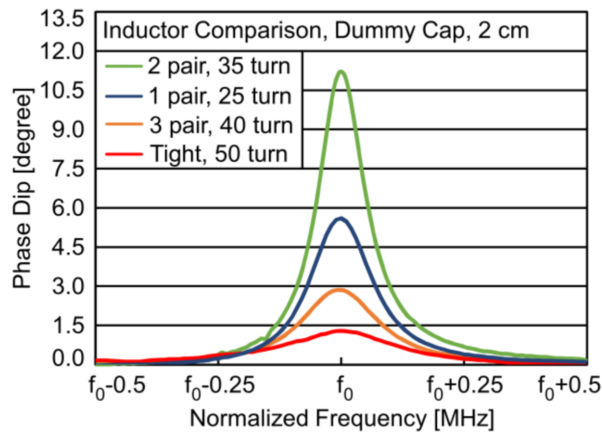

Fig. 5.6: Comparison of inductor designs refining the phase dip magnitude by balancing the coupling and proximity effect. Optimum design utilizes turns in groups of two.

With the coils refined and verified using dummy capacitors, the actual capacitive sensors were attached. Unfortunately, the sensors themselves have large resistive losses associated with the thin metal traces.

Series Resistance of the Sapphire18 Capacitive Pressure Sensor:

Once the sapphire18 capacitive sensor was attached to the refined inductor from Fig. 5.6, the quality factor was observed to substantially reduce, shown in Fig. 5.7. As the inductor was fully characterized with a low ESR dummy capacitor (by fitting values to the circuit in Fig. 5.2), the effective series resistance of the inductor was known (4.1 μH @ 3.5 Ω), then the remaining damping must come from the sensor. When modeled with the same circuit, the additional series resistance from the sensor was found to be approximately 50 Ω. Unfortunately, this large increase in damping caused a great reduction in both the quality factor and magnitude, severely limiting the maximum interrogation range and resolution.

The most effective method used to reduce the series resistance of the sensor was to attach a low equivalent series resistance (ESR) (<0.01 Ω at 50 MHz) capacitor in parallel with the sensor, increasing the phase dip magnitude by four-fold. If the parallel capacitor's value is matched to the sensor (≈10 pF), the equivalent series resistance is reduced by ≈67% to ≈13 Ω (at the cost of increasing the offset capacitance by 10 pF). While this also reduces the frequency response, it greatly improves the sensor Q, and thus the maximum readout distance and resolution. The phase dip with a single pressure sensor (PS), two parallel PS's, parallel PS and dummy, and single dummy capacitor is shown in Fig. 5.7.

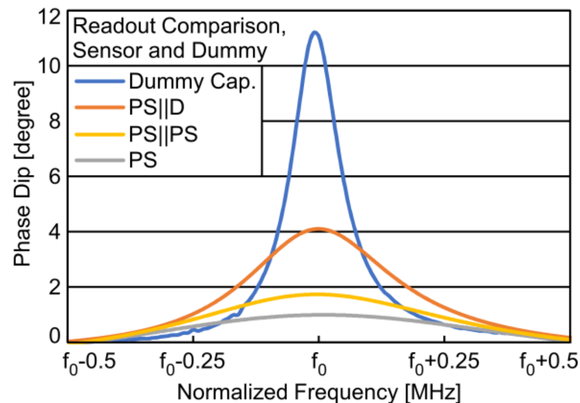

Fig. 5.7: Comparison of capacitive pressure sensor (8C200) and dummy capacitors connected to the same inductor, showing a four-fold increase in magnitude over a single pressure sensor.

The final device with both the vertical and horizontal coils wound, as well as the placement of the sensor and dummy capacitor is shown in Fig. 5.8.

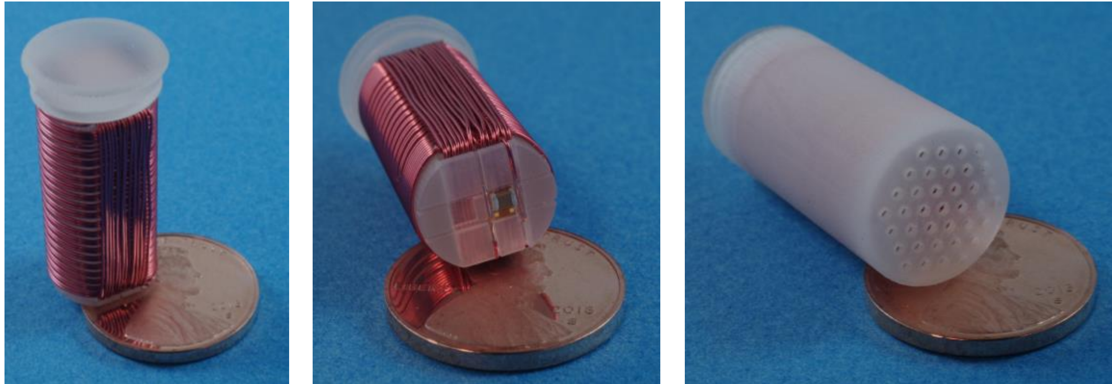

Fig. 5.8: Images of LC Tank 3D printed structure with embedded sensor, showing pressure sensor and dummy capacitor placed into bottom of structure, and final encapsulated tank structure with pressure feed-through holes on bottom.

3) Phase detection circuitry and software control design

The final aspect of this system is the design of the interface circuitry and control software required to excite the readout coil and capture the phase data, block diagram given in Fig. 5.9.

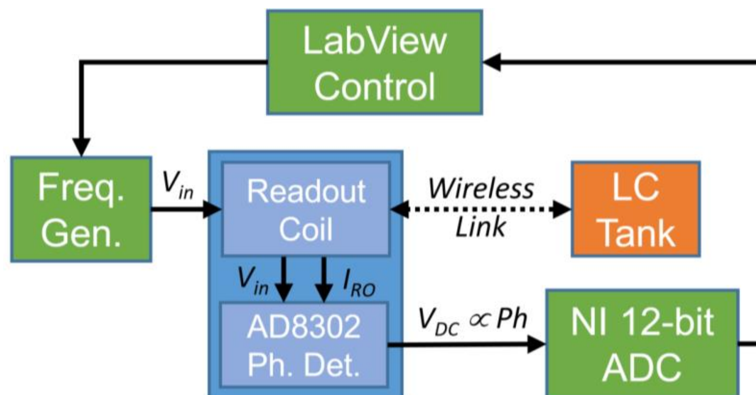

Fig. 5.9: Block diagram of wireless pressure interrogation system showing the readout coil with on-board AD8302 phase detection chip (outlined in blue), wireless link between readout coil and LC tank sensing element (outlined in orange), and hardware implemented with a National Instruments PXI-6115 (outlined in green).

The interface hardware consists of the phase detection circuitry, input voltage (frequency generator), and analog to digital converter. The readout coil was created by with a simple coil trace on the PCB. In order to efficiently and accurately capture the phase difference between the

input voltage and resulting current on the readout coil, an application specific phase detection chip (Analog Devices AD8302) was used. It operates with analog input frequencies as high as 2.7 GHz, requires minimal passive external components, and outputs an analog voltage level directly proportional to the phase difference [Ana02]. Noise was minimized by implementing this chip directly onto the PCB, as long lead transfer to separate detection circuitry was not required. The final readout coil and phase detection chip are shown in Fig. 5.10.

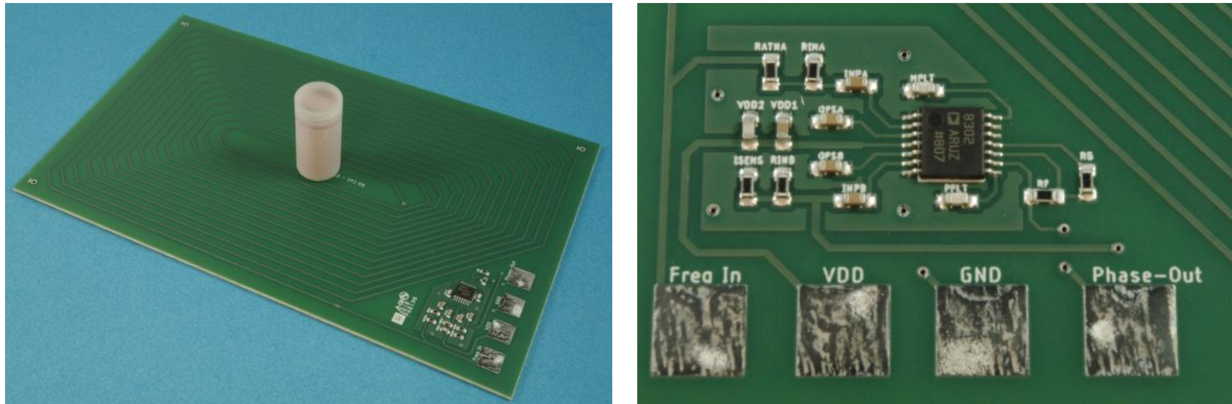

Fig. 5.10: PCB showing the readout coil and AD8302 phase detector circuitry with packaged passive sensor standing in the center (measures 9×15 cm^2). Image of phase detection circuitry (15×30 mm^2) and external connection pads (6×6 mm^2 each) for connection to input interrogation voltage, VDD, GND, and output phase proportional voltage.

The input interrogation voltage, analog to digital converter (used to capture the analog output voltage level of the phase detection chip), and control software were implemented with a National Instruments PXI-6115. It has built-in modules which can generate input signals up to 20 MHz, integrated 12-bit ADC capable of 10 MSPS data capturing, and utilizes LabVIEW software [Nat04], making the software defined hardware synchronization near-trivial.

The program was designed to sweep the input interrogation frequency in discrete steps while simultaneously digitizing the analog output of the phase detection chip with the ADC during this interrogation period. The user inputs consist of the input frequencies range, number of interrogated frequencies (frequency step size), and time per interrogation frequency (and thus the

number of averaged phase data samples). Each of these inputs will have a direct impact on the overall system resolution and bandwidth.

The frequency range will define how wide the interrogation sweep will be; a larger sweep will collect more data, but reduce the maximum bandwidth. However, the interrogation range will not benefit from extending beyond a certain size. Assuming an approximate Gaussian curve (5.11) for the phase dip, the resonant frequency (f_0), quality factor (Q), and phase dip magnitude can be substituted into the Gaussian equation so that they relate to the mean (μ) and standard deviation (σ), given in equations (5.12) and (5.13), and shown in Fig. 5.11.

$$Ph(f) = A\,exp\left(-\left(\frac{(f-\mu)}{\sigma}\right)^2\right) \rightarrow A\,exp\left(-\left(\frac{Q(f-f_0)}{f_0}\right)^2\right) \tag{5.11}$$

$$\mu = f_0 \tag{5.12}$$

$$\sigma = \frac{f_0}{Q} \tag{5.13}$$

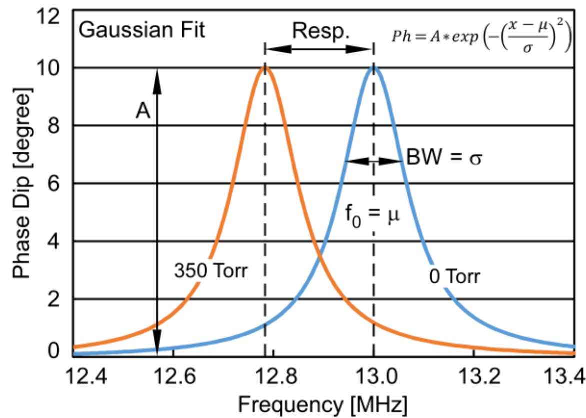

Fig. 5.11. Fitted parameters (bandwidth (σ), mean/resonant frequency (μ), magnitude (A), and frequency response) for the phase dip assuming an approximate Gaussian curve.

If it is desired to capture >99% of the Gaussian phase dip curve, then three standard deviations would be required for 99.7% (e.g. Range = 3σ). However, as the peak moves with pressure, the sweep range must include the lowest frequency (e.g. frequency at highest applied pressure). Therefore, once the frequency response is known ([kHz/Torr]), it can be multiplied by

the expected maximum applied pressure ([Torr]) and added to the six sigma range, giving the required interrogation range in terms of resonant frequency, Q, and frequency response, (5.14).

$$Range = 3(\sigma) + (Resp)(P_{max}) = 3\left(\frac{f_0}{Q}\right) + (Resp)(P_{max}) \quad (5.14)$$

When approximate values for f_0 (≈13 MHz), Q (≈50), frequency response (0.6 kHz/Torr), and pressure (350 Torr) are substituted into (5.14), the required interrogation range is ≈1.0 MHz.

The number of interrogated frequencies will determine the resolution of the phase dip of the swept frequency range. As the number of discrete steps increases, the peak will be more accurately captured, but it will reduce the amount of time available for output averaging (in order to reduce the noise and increase the effective number of bits of the ADC) or reduce the bandwidth given the same interrogation time. As with the interrogation range, though, the step size will not improve resolution beyond a certain point. (The final f_0 is extracted by fitting a Gaussian curve to the data; more data points will not necessarily improve resolution.) Empirical testing showed that gathering more than 10 data points within the bandwidth added no curve fitting benefit. Therefore, the required step size can be approximated as given in equation (5.15).

$$Step\ size = \frac{\sigma}{10} = \frac{f_0}{10 * Q} \quad (5.15)$$

When the expected values for f_0 (≈13 MHz) and Q (≈50) of the LC tank are substituted into equation (5.15), the required step size is approximately 25 kHz. When combined with the required sweep range of 1 MHz, approximately 40 discrete interrogated frequencies are required.

The interrogation time per frequency will allow the ADC to average a number of samples in order to reduce noise and quantization error. As the phase data (DC voltage output from the AD8302 phase detector chip) is digitized by the ADC, it will be quantized to the bit resolution of the specific device, (12 bits, ±2 V for the PXI-6115), resulting in quantitation level of

$\Delta = 4$ V/(2^{12}) = 0.98 mV/code. Assuming the phase detectors output of 30 mV/°, this will result in a quantization level of ≈0.03°/code (with a single digitized data point), limiting the detectable phase dip resolution to ≈0.15° - 0.35° (with at least 5-10 quantized levels needed and assuming no further noise), an unacceptably low resolution. However, a 64 Hz bandwidth requiring 40 discrete frequency steps permits ≈390 µs per interrogated frequency. To account for non-ideal delays (frequency switching time, ADC data transfer, etc…) a total available averaging time of 103 µs is assumed, which will allow for up to 1024 samples to be taken at 10 MSPS (and a theoretical maximum bandwidth of up to 150 Hz). When averaged, these 1024 averaged samples will reduce the noise by √1024 (32) fold, assuming uncorrelated white RMS noise, and increase the effective number of bits by 5, reducing the effective quantization level from 0.98 mV/code to 0.03 mV/code [Can91], a much more acceptable level for low magnitude phase peak detection.

Unfortunately, when the program was created, there was an irreducible "program delay" of approximately 11 ms per interrogated frequency (in addition to the actual 103 µs frequency interrogation time), limiting the effective BW to approximately 2 Hz. This is due to the LabVIEW programming language, which is designed for ease of use and prototyping, not high performance. It utilizes "virtual instrument" programming blocks to initiate the ADC and frequency generators, which have initial startup times and cannot be eliminated. If a custom ADC / frequency generator / microcontroller board was created, the frequency switching time could likely be eliminated, allow for the desired ≥64 Hz bandwidth.

5.1.2 Experimental Test Setup

The final sensor interrogation system is comprised of just three primary elements - a 5 V power supply and ground, the readout coil with on-board phase detector IC, and the NI PXI-6115 encompassing the frequency generator, 12-bit ADC, and LabVIEW software. As shown in

Fig. 5.10, the readout coil PCB has four external connection pads. Two are used to power and ground the phase detector IC and are connected to a power supply. The remaining connections are data IO ports, connected using a shielded co-ax cable, with the frequency input pad connected the PXI's frequency generator and the phase-out pad connected to the PXI's ADC. A two meter cable length was chosen for all cables as a compromise between usability and noise mitigation, allowing the PCB to be correctly positioned for sensor interrogation but minimizing any noise with longer cables.

The system is controlled from a monitor screen connected to the PXI, which allows the user to set a frequency interrogation range, step size, and frequency interrogation time. Once the program is initiated, it will run continuously, displaying the latest phase data for each frequency sweep on screen and storing it for later review.

The power supply and PXI system measure approximately $20 \times 20 \times 10$ cm^3 and $60 \times 60 \times 30$ cm^3, respectively, with a 15" computer monitor for GUI display. These elements are stored on a mobile cart to enable mobile testing capability.

5.2 Experimental Results

With the external readout coil, phase detection circuitry, frequency generation, ADC, control software, and LC Tank sensor designed, the system was experimentally verified. It was first tested in controlled *in situ* conditions using air and conductive saline as a test medium, followed by more realistic *in vivo* conditions with the sensor ingested by a beagle canine model.

5.2.1 *In Situ* Saline Environment Experimental Results

Using the designed components, pressure testing of the sensor in both an air and blood substitute (saline) environment was completed. (Blood has a stated conductivity of between 2,000 and 20,000 µS/cm [Hir50]. To ensure the worst case was tested, a saline mixture of NaCl and DI

water with a conductivity of 40,000 μS/cm was created (using 11.7 mg/L concentration of salt to water). The sensor was placed in a PVC test chamber, filled with saline (or air) and pressurized with a syringe pump. The pressure was monitored with an analog gauge connected in series with the pump and chamber.

The Sapphire18 capacitive pressure sensor (8C200) and 10 pF dummy capacitor were connected to the dual axis inductor design to create the LC tank. The exposed contact pads of the sensor and capacitor were sealed with DowSil© sealant. The structure was placed in the capsule and sealed with SG-ONE Light Consistency Silicone Grease to further ensure the testing environment would not contact the sensor but still allow pressure transmission.

A maximum readout distance of approximately 6 cm was found. Beyond this distance, the signal was too weak (phase dip magnitude of <0.1°) to differentiate between the small applied pressures. It was experimentally verified that the devices showed a frequency response of -0.6 kHz/Torr (-4.45 kHz/kPa) when fully sealed in their capsule with sealing silicone grease. Test results of the sensor in both air and saline environments with 262 Torr (35 kPa) of applied pressure are shown in Fig. 5.12 with the Gaussian fit extracted resonant frequencies at each applied pressure given in Fig. 5.13.

The equivalent circuit parameters (utilizing the circuit from Fig. 5.2) are a sensor inductance of 6.9 μH, dummy capacitor and other parasitic capacitance of 11.5 pF, sensor offset capacitance of 10.5 pF, coil series resistance of 8 Ω, and sensor series resistance of 50 Ω.

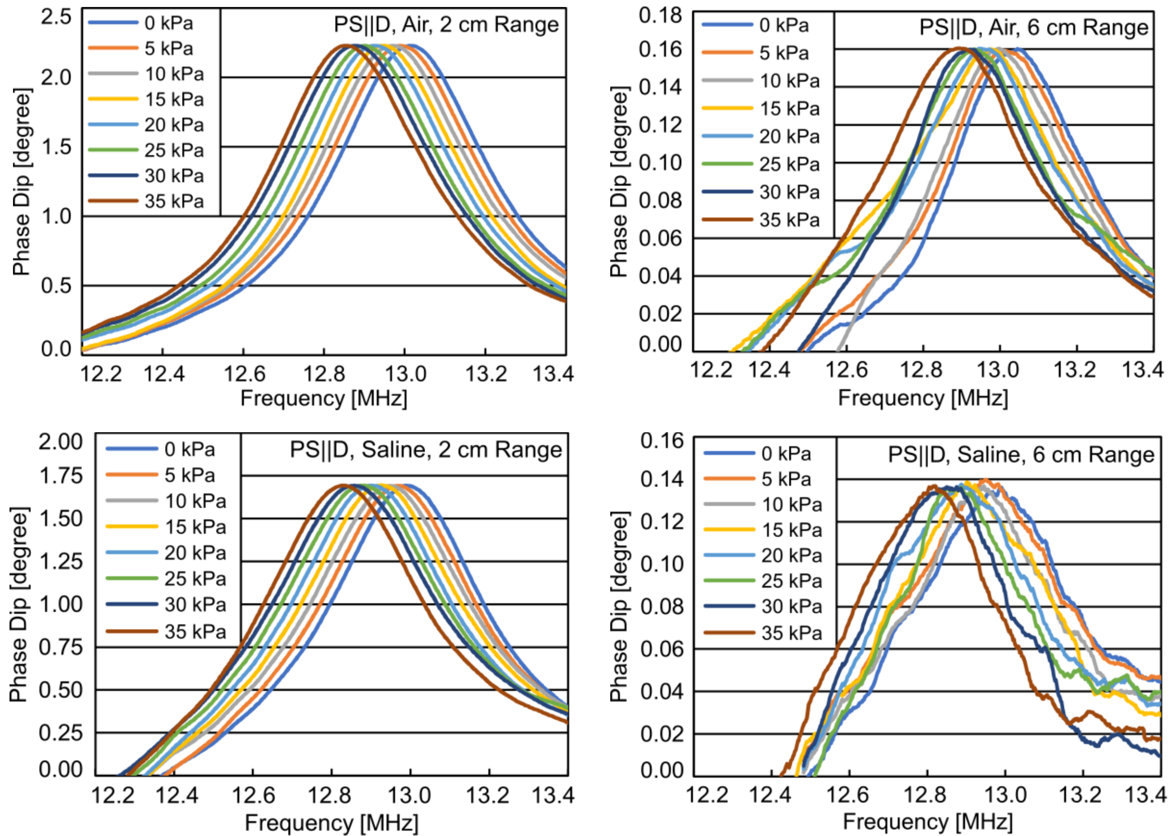

Fig. 5.12: Experimental results of the LC tank in both an air and saline environment. A maximum readout distance of 6 cm was allowed by the device.

Pressure Resolution:

The resolution of the device was determined by taking numerous (n = 50) readings at a single pressure, fitting a Gaussian curve, extracting the peak (e.g. resonant frequency), and determining the standard deviation of these values. This frequency deviation was then divided by the frequency response to give the standard deviation in units of pressure. Assuming a required confidence interval of 95% (e.g. ±2σ), the resolution was then extracted, given in Table 5.4. Due to the relatively low *Q* (from the 50 Ω ESR of the sensor) and reduced frequency response (parallel dummy capacitor increasing the C_0), the resolution is lower than desired. However, a resolution of better than 12 Torr (1.6 kPa) was achieved at the maximum distance of 6 cm, improving upon the average resolution of the SmartPill.

Table 5.4: Resolution / Accuracy of LC Tank in saline environment (n=50)

Interrogation Distance	Phase Dip	Resolution [Torr]		
		2-σ (68%)	**4-σ (95%)**	6-σ (99.7%)
2 cm	1.70°	±0.7	**±1.3**	±2.0
3 cm	1.00°	±0.9	**±1.8**	±2.7
4 cm	0.55°	±1.2	**±2.5**	±3.7
5 cm	0.25°	±3.2	**±6.4**	±9.6
6 cm	0.14°	±6.0	**±11.9**	±17.9

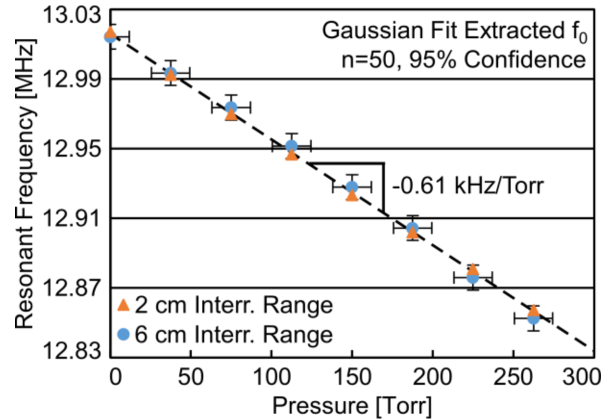

Fig. 5.13: Extracted resonant frequency with a Gaussian curve fitting from the 2 cm and 6 cm interrogation data in saline from Fig. 5.12. Error bars correspond to the pressure/frequency 95% confidence (4-sigma) resolution at n=50. 2 cm error bars are not visible at this scale.

5.2.2 *In Vivo* Canine Model Experimental Results

With the sensor design completed and fully tested in a saline environment, it was then tested *in vivo* in a beagle canine model to verify sensor interrogation capability under more realistic test conditions[3]. Beagles are the preferred FDA testing model due to their size and welfare needs (making animal handling and care easier). The same test setup as described in the previous section was used; the readout coil with on-board phase detector was connected to the National Instruments PXI-6115 and controlled with the LabVIEW software/program. The sealed capsule was administered via mouth and radiographs were taken prior to each measurement to ensure its location within the beagle (Dora), example radiograph shown in Fig. 5.14. Once the system was activated and input parameters set (using an frequency interrogation range 12.2 MHz to 13.6 MHz

[3] Thanks to Professor Duxin Sun, Jeremy Felton, and the Unit for Laboratory Animal Medicine (ULAM), part of the U-M Medical School Office of Research, for assisting with setting up the *in vivo* beagle tests.

and 25 kHz step size, allowing for an ideal bandwidth of ≈175 Hz, but limited to ≈2 Hz due to program delay), readings were taken by centering the readout coil at the approximate location of the capsule (labeled "Reading #") for several seconds to obtain the phase peak. The coil was then moved to Dora's rear (away from the known location of the sensor) to obtain readings in which the coupling between the readout coil and sensor was known to be ≈0 ("Baseline #"). The "Baseline" measurements were averaged and subtracted from the "Reading" measurements in order to better show the resonant frequency peak. (Raw measurements show a non-ideal phase drift (although constant for the same range of interrogated frequencies with no sensor coupling) of ≈±10° due primarily to the electronics influence on the phase.) The "Ref. Signal" is the reading of the LC Tank prior to implantation, taken from the 0 kPa reading in Fig. 5.12 above. Readings were taken immediately after administration and 26 hours later; the capsule remained in the stomach for both readings, results shown in Fig. 5.15.

The capsule was regurgitated on the third day when Dora ate cloth from wrapping on a fellow canine friend, causing her to vomit and expel the capsule, ending the experiment. The recovered LC Tank was re-tested in an air environment and found to still be in working condition with no change in pressure response or resonant frequency, Fig. 5.16.

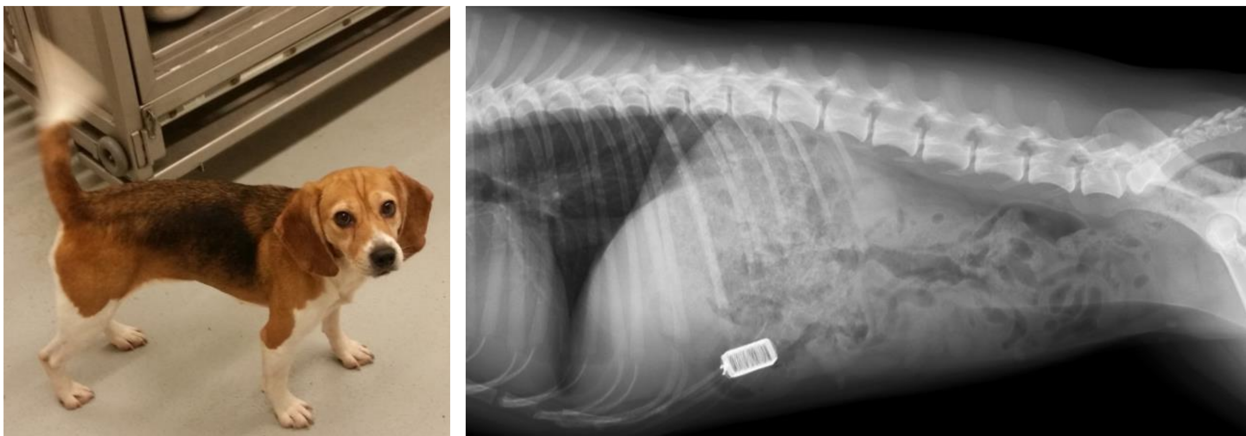

Fig. 5.14: Our test beagle, Dora (left), and a radiograph (right) of capsule in her stomach prior to testing on the first day. It can be seen that the readout coil coupled to the x-axis coil, as the z-axis coil was rotated 90° and normal to the length of Dora.

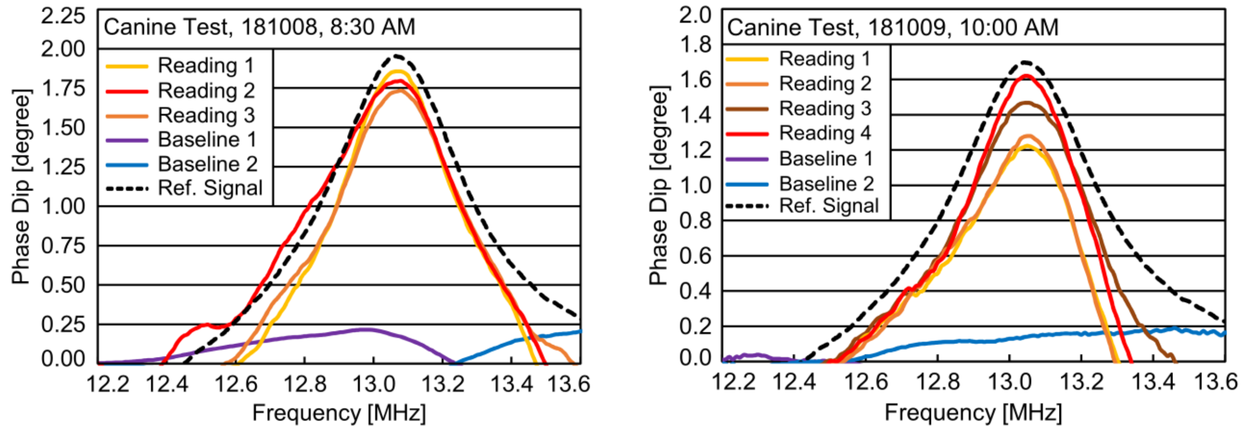

Fig. 5.15: Experimental results of the LC tank in canine on the first and second day. No change in pressure (resonant frequency) was observed. "Reference signal" is reading taken from LC Tank sensor prior to implantation, which shows good agreement with resonant frequency and phase dip peak shape.

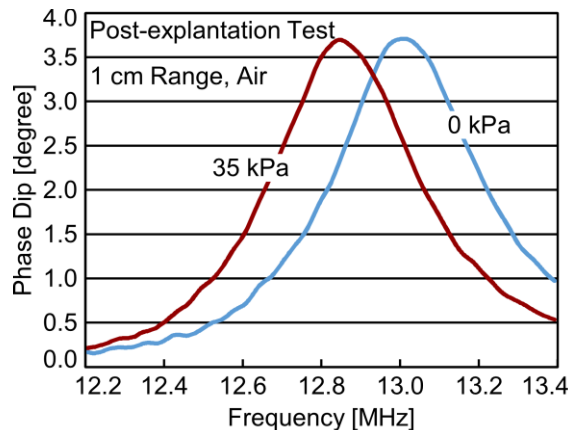

Fig. 5.16: Experimental results of the LC tank device after recovery.

5.3 Conclusions and Summary of the Passive Sensing System

A practical application was successfully demonstrated in which GI tract pressure could be monitored via a passive wireless LC Tank sensor utilizing the Sapphire18 8C200 capacitive pressure sensor. A dual axis inductor design was utilized so as to minimize the reduction in the magnitude of the phase dip due to imperfect orientation and alignment between the sensor and readout coil. Techniques to reduce the series resistance due to the proximity effect of the inductor coil were used to increase the coupling magnitude (i.e. SNR) by an order of magnitude. On-board phase detection circuity was designed and placed on the readout coil PCB to reduce noise. A National Instruments PXI-6115 was used to expedite prototyping by utilizing it's built in frequency

generator, ADC, and LabVIEW software control capability. A program was written to allow an ideal readout bandwidth of at least 64 Hz and up to 150 Hz assuming no program delay. The final packed device demonstrated a frequency response of -0.6 kHz/Torr (-4.45 kHz/kPa). *In situ* testing (using a conductive saline environment) resulted in a maximum interrogation distance of 6 cm with a resolution of 11.9 Torr (1.6 kPa) (1.3 Torr (0.17 kPa) resolution at a 2 cm range) over 262 Torr (35 kPa) of applied pressure. *In vivo* canine beagle testing was also completed, demonstrating a practical application by successfully interrogating an ingested sensor in a canine stomach for over 26 hours.

Unfortunately, the maximum readout distance was limited due to the high equivalent series resistance (ESR) of the capacitive pressure sensor, which significantly reduced the LC Tank's quality factor and phase dip magnitude. By placing a capacitor in parallel with the pressure sensor, the equivalent ESR of the parallel combination was reduced by 70% allowing for a fourfold increase in the phase dip magnitude, but at the cost of reducing the frequency response from ≈1.5 kHz/Torr to the experimentally verified 0.6 kHz/Torr.

Future work to reduce the series resistance of the sensors would allow for an improvement in both the system's range and resolution, as well as permitting the use of a smaller device with fewer turns. Additionally, limitations in the off-the-shelf National Instruments software reduced the effective bandwidth to ≈2 Hz. An application specific microcontroller, digital frequency synthesizer, and ADC implemented onto the readout coil PCB could reduce program delay and improve the bandwidth to its theoretical maximum of ≥150 Hz.

CHAPTER 6: Conclusions and Future Work

6.1 Summary

This chapter summarizes the efforts of developing a process flow for the microfabrication of miniature, high-performance capacitive pressure sensors. Their primary use was intended for sensing in harsh environments of downhole oil exploration where the pressure and temperature can reach ≥50 MPa (≥7,250 psi) and ≥125°C, in which high pressure resolution of ≤50 kPa (7.0 psi) is required, and in which the sensing system must be ≤1 cm^3. Extensive process refinement permitted the fabrication of harsh environment capacitive pressure sensors with unprecedented performance, allowing a full-scale range of 50 MPa, system resolution of 14.5 bits (<7 kPa, <1 psi), C_0 of <4 pF, volume of less than 1 mm^3, TCO of 420 ppm/°C, customizable full-scale range of more than three orders of magnitude, and yield of >95%. The sensor designs were validated through custom autonomous microsystem integration and demonstrated functionality in a both lab and field tests.

While the capacitive pressure sensors were developed primarily for custom microsystems, there are many situations where a wired connection to the readout circuitry is not possible. A passive wireless pressure monitoring system utilizing short-range inductive coupling was developed to evaluate the performance of the sapphire substrate sensors in this use-case. A GI tract application was targeted and sensors designed with a full-scale range of ≤50 kPa (350 Torr) were utilized. A practical application was demonstrated *in vivo*, in which stomach pressure was monitored for two days in a canine model.

A brief timeline illustrating major changes to the Sapphire process, performance records attained, and system integration milestones is given in in Fig. 6.1 below

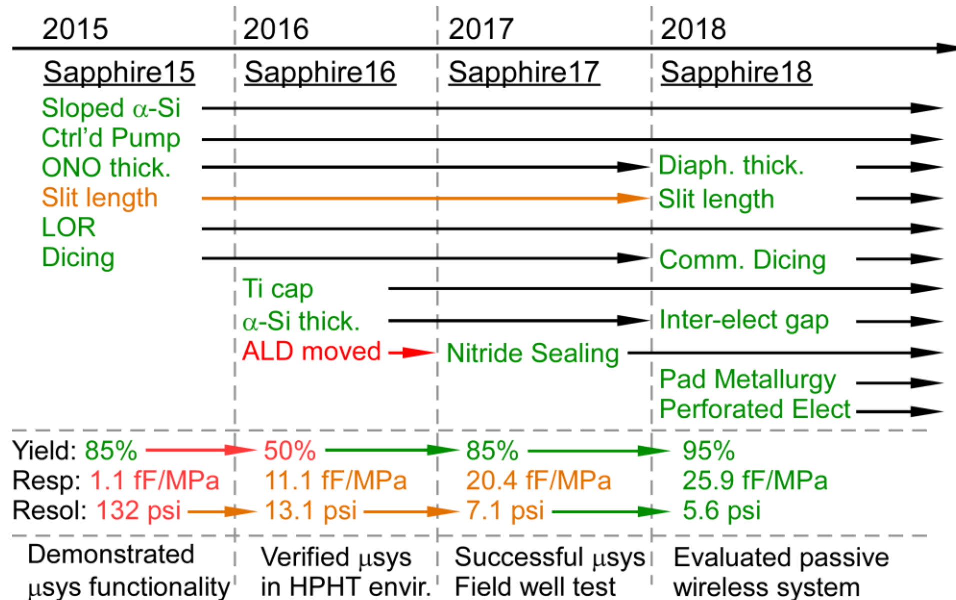

Fig. 6.1: Overview of changes made to the Sapphire Substrate process, as well as performance records and microsystem integration tests.

Major contributions to the microfabrication field are listed. Future work regarding improvements to the biomedical application sensor and system are proposed.

6.1.1 Sapphire15-17 Pressure Sensor

In order to reduce fabrication complexity and temperature coefficients observed with silicon substrates and through-wafer backside contacts, an investigation into utilizing dielectric sapphire substrates and front side contacts was conducted. Many fabrication challenges were investigated and addressed, which permitted a diaphragm yield of ≥85% in the Sapphire15 process, and demonstrating the ability to solve numerous yield limiting challenges by focusing on the interactions between equipment limitations and sensor design. Further improvements were completed and a modified Sapphire16 process was designed, improving the capacitance response by an order of magnitude. The TCO of the Sapphire16 devices was measured to be less than

300 ppm/°C up to 200°C. The sensors were demonstrated to be operational within microsystems at pressures up to 50 MPa (7,250 psi) and temperatures up to 125°C.

Sapphire17 continued the investigation of sapphire substrate pressure sensors, focusing on both yield and sensitivity improvements. By altering the electrode insulation method, monitoring the surface roughness, controlling the dielectric diaphragm stresses, and refining a conventional dicing method, the final device yield was increased to >80% while simultaneously doubling the sensitivity (63,000 ppm/MPa in Sapphire16 to 133,000 ppm/MPa in Sapphire17) of the ≥50 MPa full-scale range (ø100 μm) sensors. These sensors were integrated into the microsystems and tested in both laboratory settings (with simultaneous application of 50 MPa and 125°C) and field borehole (non-laboratory) environments to a depth of 1.3 km in a brine well, which resulted in a simultaneous pressure and temperature of up to 12 MPa (1,750 psi) and 70°C.

The parallelism that allowed for high capacitance response over a wide operating range without loading the capacitance-to-digital readout electronics was due to the great reduction in the parasitic capacitances allowed by the dielectric substrate and diaphragm materials and small offset capacitance of the sensor.

6.1.2 Sapphire18 Pressure Sensor Process

With many of the problems addressed in the Sapphire17 process, an investigation into designs permitting wide full-scale range and improving upon system integrability and singulation throughput was conducted. This process was used to fabricate devices on the same wafer (by altering only sensor diameter) which could be used in downhole applications requiring ≥50 MPa (7,250 psi) full-scale range (demonstrating an average resolution of <2.8 kPa, 0.4 psi) or in biomedical applications requiring ≤50 kPa (350 Torr) (demonstrating an average resolution of

<80 Pa (0.6 Torr)) without any change in active sensor area. The singulated device yield was also improved, maintaining a 95% yield for the high-pressure designs.

With system integration being a major focus, modifications to the device separation distance to allow for commercial die singulation and changes to the contact pad metallurgy to permit automated sensor mounting onto microsystem PCB's were added to the process, vastly increasing throughput and system integration reliability.

It should be noted that the smallest fabricated sapphire substrate capacitive pressure sensor had a diaphragm of ø100 µm, with a total potential minimum volume of <0.04 mm^3 (including adequate kerf width for commercial dicing capability with an active sensor-diaphragm area of <0.01 mm^2 for the single diaphragm ø100 µm devices). The final dimension of the singulated sensors ($1.8 \times 0.8 \times 0.5$ mm^3, 0.75 mm^3) was determined by the microsystem integration requirements (contact pad size and spacing for placement onto the PCB). With such a small active device area, the final sensor could theoretically be reduced in size to accommodate size requirements for sub-millimeter packages with no loss in capacitance response.

6.1.3 Passive Wireless Sensing

While the capacitive pressure sensors have been developed primarily for the wired microsystems, there may be situations where a wired connection to the readout circuitry is not possible. A passive wireless pressure monitoring system utilizing short-range inductive coupling has been developed to evaluate the performance of the sapphire substrate sensors in this use-case. Pressure monitoring within the GI tract has been targeted; an *in situ* range and resolution of 6 cm and 1.6 kPa (12 Torr) has been achieved through conductive saline. A practical application of the sensor has been demonstrated *in vivo*, being implanted and successfully interrogated in a canine model to monitor stomach pressure for over two days.

While a GI tract application was targeted, this use-case demonstrates the potential of the sapphire sensors to be wirelessly interrogated with only passive elements placed in the environment. When the resistive losses in the sensor are reduced in future iterations (which can be accomplished with wider metal traces), the range can be extended and resolution improved.

6.2 Contributions

The main contributions of this work include:

1. Developed a high-yield, surface micromachining fabrication process to create high performance capacitive pressure sensors in which dielectric substrates were utilized to minimize parasitic and offset capacitances and temperature coefficients.
2. Employed modern dry, low temperature (≤400°C) fabrication techniques to minimize chemical waste, fabrication time, and cost.
3. Identified and addressed equipment limitations that constrained yield and performance of the microfabrication process by focusing particularly on interactions between equipment configurations, process integration, and sensor design.
4. Designed and fabricated harsh environment pressure sensors for integration into autonomous microsystems meeting a vast number of system requirements including full-scale range (≥50 MPa), temperature (≥200°C), resolution (≤7 kPa @ 1 fF/code system resolution), and sensor size ($\leq 2 \times 1 \times 0.5$ mm^3).
5. Demonstrated process adaptability to meet commercial requirements in order to increase throughput and system integration reliability, including commercial die singulation and automated PCB mounting and manufacturing requirements.

6. Co-designed devices and process parameters to concurrently fabricate sensors with full-scale range customizability of over three orders of magnitude, extending from harsh downhole environments (≥50 MPa (7250 psi), maintaining <7.0 kPa (1.0 psi) resolution) to biomedical applications (≤50 kPa, (350 Torr), maintaining <80 Pa (0.6 Torr) resolution) without any change in singulated sensor area.
7. Evaluated sapphire substrate devices in a passive wireless pressure sensing use-case where on-board electronics are not possible, utilizing short range inductive coupling. A biomedical application was targeted in which pressure was sensed within the GI tract. *In situ* experiments showed a range, resolution, and bandwidth of 6 cm, 1.6 kPa (12 Torr), and 2 Hz. *In vivo* experiments verified a practical application of the sensor to be ingested and interrogated in a canine beagle model for over 2 days.

6.3 Future Work

6.3.1 Passive Wireless Pressure Sensing Improvements

As discussed in Chapter 5, there are two primary factors limiting the maximum communication distance and resolution for passive LC Tank sensing systems – 1) the effective diameter of the sensors inductive coil, and 2) the total resistance of the system. While the coil diameter is typically set by the environment in which it will be placed, the series resistance can be refined. The largest non-ideality associated with the coil is the skin effect at high frequencies, further exacerbated by the proximity effect. It was shown that this could be minimized by utilizing a larger wire diameter and refining the trace spacing. However, the ESR of the capacitive pressure sensor was found to be nearly an order of a magnitude higher (≈50 Ω) than the refined coil resistance (≈5 Ω), reducing the quality factor, interrogation distance, and resolution substantially. Due to the black box nature of the sensing element, without modifying the process flow and

competing an additional fabrication run, there is nothing that can be done to reduce the sensor ESR. While it was mitigated with the placement of a dummy capacitor, this resulted in an increase in offset capacitance and reduction in frequency response, and thus potential system resolution.

Due to the relatively thin metal (400 nm lower electrode, 200 nm upper electrode) and narrow trace widths (10 μm) connecting the diaphragms, the total resistance of the trace connections alone is approximately 35 Ω (12 Ω for the LE and 23 Ω for the UE) on the 8C200 device. Two options for reducing the resistance are to electroplate and/or widen the diaphragm connection traces. If the trace widths were increased to 30 μm and electroplated to 2.5 μm, the resistance could be reduced to less than 1 Ω, effectively reducing the total ESR by 67% with no impact on the diaphragm design or sensor layout. This still leaves 15 Ω from the upper electrode diaphragms, which were perforated to reduce diaphragm bending and have many etchant access slit openings, greatly reducing the effective cross sectional area. By moving some of the etchant access slits to increase the upper electrode connections, its resistance could likely be reduced by several ohms as well, bringing the total series resistance to approximately 10 Ω. With a reduced sensor resistance, the maximum Q could be substantially improved from the experimentally verified 50 to nearly 100 utilizing the same design as described in Chapter 5. Additionally, a smaller coil (and thus passive sensing element) could be used to obtain the same phase dip magnitude with a reduced overall resistance. Improvements in the Q and frequency response with varying sensor attachment types (where PS_R is the current sensor with 50 Ω series resistance, PS_r is the sensor assuming 10 Ω, and Dummy is a 10 pF capacitor with 0 Ω series resistance) are given in Table 6.1 below. The estimated maximum range is set as the distance at which the coupling drops to ≈0.15° (the minimum coupling experimentally found during *in situ* testing). The resolution is estimated by approximating the standard deviation of the frequency based on the Q,

then dividing by the frequency response. With a reduction in the sensor resistance, the estimated maximum range can be doubled while simultaneously improving the resolution by a factor of three.

Table 6.1: Comparison of LC Tank parameters with varying sensors and series resistances

Sensor Connection	Resonant Freq. [MHz]	Quality Factor	Phase Peak, 2 cm Range	Response [kHz/Torr]	Est. Range	Est. Resol. @ Max. Range
PS_R	17.5	28	0.9°	1.4	3 cm	12 Torr
PS_R || PS_R	13.0	30	1.1°	1.0	4 cm	12 Torr
PS_R || Dummy	13.0	47	1.8°	0.6	6 cm	12 Torr
PS_r	17.5	54	2.0°	1.4	8 cm	4 Torr
PS_r || PS_r	13.0	55	2.3°	1.0	9 cm	4 Torr
PS_r || Dummy	13.0	75	2.8°	0.6	12 cm	4 Torr

The readout system can also be improved by utilizing an on-board frequency synthesizer, ADC, and microcontroller, such as an AD9834 DDS 75 MHz frequency generator [Ana03] and ADSP-CM402F-E microcontroller with built-in 16-bit, 2.5 MHz capture rate ADC [Ana15]. The current implementation of these components (with the National Instruments PXI-6115) results in large program delay, reducing the effective output bandwidth from a maximum of up to 150 Hz to ≈2 Hz. On-chip analog low-pass filtering could also be implemented to reduce any higher frequency noise (as the digitized output is a DC value from the phase converter chip). On-board integration of these components would allow for a reduction in both noise and variations in the phase due to movement in the leads connecting the hardware components, which can obscure the resonant frequency peak of the LC Tank sensor.

6.3.2 Active Wireless Pressure Sensing System

The move to an active sensing system utilizing on board electronics, batteries, and data transmission circuitry, could dramatically improve performance of the sensing system without any alterations to the Sapphire18 sensors. While this approach's disadvantages have been explored, the passive system is limited in range and resolution due to the sensors series resistance. However,

the SmartPill's system parameters can be vastly enhanced, namely the size, bandwidth, and resolution, as shown in Table 6.2.

Table 6.2: Comparison of LC Tank, CardioMEMS, and SmartPill Systems

	Range	**Resolution**	**Size**	**Volume**	**Bandwidth**
LC Tank	6 cm	1 Torr @ 2 cm 12 Torr @ 6 cm	$ø12×24$ mm^3	2850 mm^3	2 Hz
CardioMEMS	20 cm	1 Torr	$30×5×1.5$ mm^3	225 mm^3	200 Hz
SmartPill	140 cm	10 – 35 Torr	$ø12×26$ mm^3	3000 mm^3	1-2 Hz
Desired Goals	≥5 meter	≤0.3 Torr	$≤ø10×15$ mm^3	≤950 mm^3	≥128 Hz

Choosing small, low power, high performing components (MCU/C-to-D, telemetry unit, and battery) and combining them with the miniature ($1.8 \times 0.8 \times 0.5$ mm^3), high performance (1.75 fF/Torr) 8C200 capacitive pressure sensor could allow for a dramatic increase in system performance, as the series resistance of the sensor (the primary limiting parameter of the passive system) typically has no impact on an active C-to-D converters digitization ability. An example of such components, along with their size and relevant data, is given in Table 6.3.

Table 6.3: Components for Active Wireless Pressure Sensing System

Element	**Component**	**Total Size [mm^3]**	**Unit Data**
MCU (C-to-D)	SiLabs C8051F990 [Sil11]	$3.0 \times 3.0 \times 1.0$	1 fF/code
Telemetry Unit	Bluetooth 5.0 communication	$\approx 7.0 \times 7.0 \times 2.0$	≈10 m TXRX
Sensor	3 || 8C200 [Fig. 5.17]	$1.8 \times 2.4 \times 0.5$	5.25 fF/Torr
Battery	Mini batteries	$\approx ø7.0 \times 4.0$	≈10 mAh

In order to combine these components into a single system, they can be integrated onto a flexible PCB designed to be folded and fit into a biocompatible 3D printed capsule similar to the one used in the passive sensing system. Estimated final dimensions and parameters for the proposed active system are given in Table 6.4.

Table 6.4: Proposed active system specifications and benchmarking comparison

	Active System	SmartPill	Passive System	CardioMEMS
Size [mm³]	≈ø10 × 8.0	ø12 × 26	ø12 × 24	30 × 5 × 1.5
Volume	≤650 mm³	3000 mm³	2850 mm³	225 mm³
Range	≥10 meters	140 cm	6 cm	20 cm
System Pres. Resolution	<0.2 Torr (3‖8C200)	10-35 Torr	1 Torr @ 2 cm 12 Torr @ 6 cm	1 Torr
Bits, 350 Torr	10.8	4.5	4.8	8.4
Temperature Sensing	25-45°C @ 1° Resol.	25-49°C @ 1° Resol.	No	No
Bandwidth	Up to 1000 Hz	1-2 Hz	2 Hz	200 Hz
Battery Life	≈5 days	≈5 days	---	---

While only estimates, the proposed active system should be capable of dramatically improving upon the SmartPill system's size (2× reduction), data transmission range (≈100× increase), resolution (≈100× increase), and bandwidth (≈100× increase), all while maintaining a similar battery lifetime. While no accommodations for pH sensing have been made, the extreme increase in all other system aspects is very promising.

Looking forward, inspired by both the potential capabilities of an active system and the extreme size reduction in sensing area (when compared to commercial and academic pressure sensing elements), an active energy harvesting style system can be envisioned where batteries would no longer be required (in order to extend system lifetime, increase biocompatibility, and further reduce system size) and high (<1 Torr) pressure resolution can be preserved. This could potentially allow for sensing in many more areas of the body where system size and lifetime are of critical importance, such as on an artery to monitor for heart failure, on a stent to monitor for restenosis, and in the eye to monitor IOP and glaucoma.

APPENDICES

APPENDIX A: RF Switch Fabrication Modifications

The fabrication of the RF switches presented a specific set of challenges to be addressed. In addition to the issues described and corrected in Chapters 2 and 3, two additional issues were delamination of the α-Si during the PECVD deposition and bending of the released bridges.

The α-Si located over bare sapphire bubbled and delaminated during the PECVD deposition of the ONO stack, which brings the wafer up to 400°C, shown in Fig. A.1. The areas of the α-Si located over the lower electrodes (with a titanium surface to prevent aluminum spiking) had superior adhesion, as the titanium served as an adhesion promoter [Cor04]. (This delamination issue was not seen it the Sapphire15 and Sapphire16 pressure sensor devices, as nearly all of the α-Si was deposited onto a titanium exposed lower electrode.) As the α-Si is deposited at 250°C, it was thought that the thermal expansion mismatch between the sapphire, lower electrode Ti/Al/Ti stack and α-Si caused a buildup of stress that that was released by the delamination. A barrier expansion layer of silicon nitride was used in order to decrease the surface expansion mismatch. When this step was added, the delamination issue was solved.

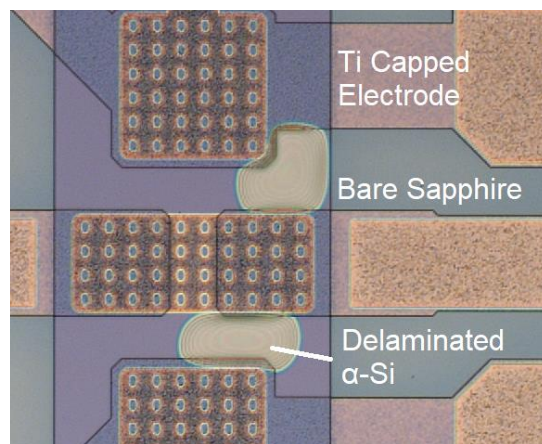

Fig. A.1: Delamination of α-Si after heating to 400°C during PECVD ONO deposition.

The more difficult failure mode to correct, though, was a deformation of the bridge structure. When the fixed-fixed design was combined with the slightly stress imbalanced metal and dielectric stack [Fan96], bending would occur after the XeF_2 release, as shown in Fig. A.2. Ideally, the flat bridge would come into nearly full contact with the lower electrode once actuated, however, the bending significantly reduced the on-state capacitance and overall performance of the switch [Nej16], as once the edges of the bridge contacted the substrate, the deflection ceased and the majority of the bridge electrode remained far above the electrode.

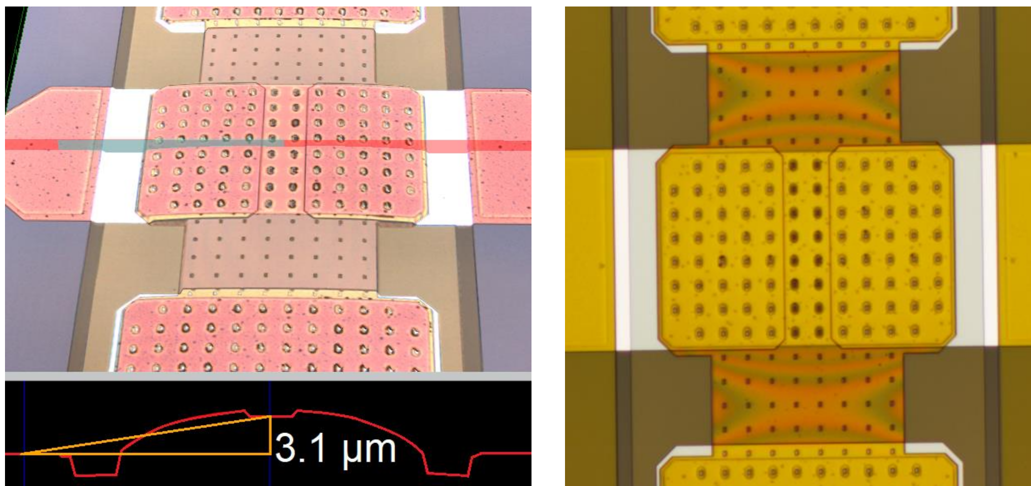

Fig. A.2: Deformation of the fixed-fixed bridge measured with an optical interferometer (left) and optical micrograph showing newton rings, an indication of bending (right).

This bending was likely caused by a z-axis asymmetry in the stress values of the metal/dielectric bridge stack. Because the upper electrode metal is completely free once the bridge is released, the effective substrate of the deposited metal changes from the sapphire substrate to the ONO stack above it. While the sputtered upper electrode metal was characterized to be low stress, it was seen in FEA modeling that after structure release, its stress changes from near neutral to highly compressive (≈300 MPa) due to the difference in thermal expansion coefficients of the sapphire substrate and ONO stack.

This compressive upper electrode (on the bottom of the bridge ONO stack) was simulated in COMSOL with the results closely matching the bending of the bridge seen in the fabricated devices, shown in Fig. A.3.

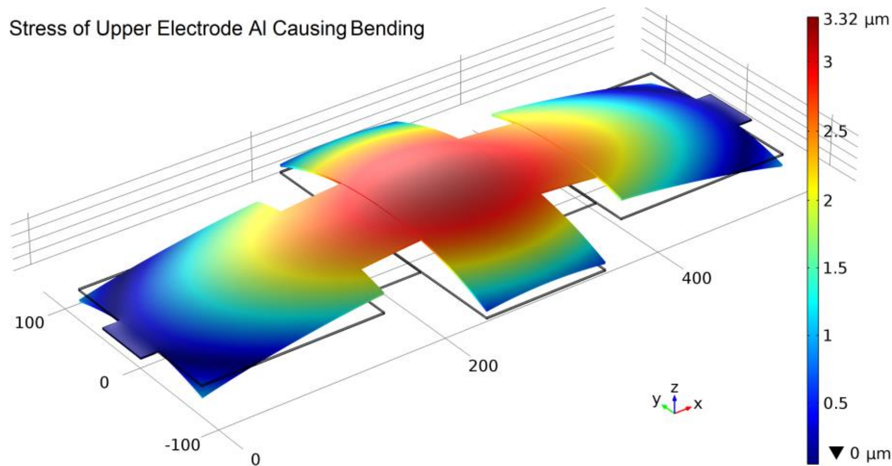

Fig. A.3: Bridge simulation matched to fabricated device (deflection exaggerated for clarity)

In theory, this asymmetry could be accounted for with a thicker compressive layer on the top of the bridge. When a 500 nm layer of oxide was added to the simulation above, the bridge bending reduced from over 3 µm to less than 300 nm, shown in Fig. A.4.

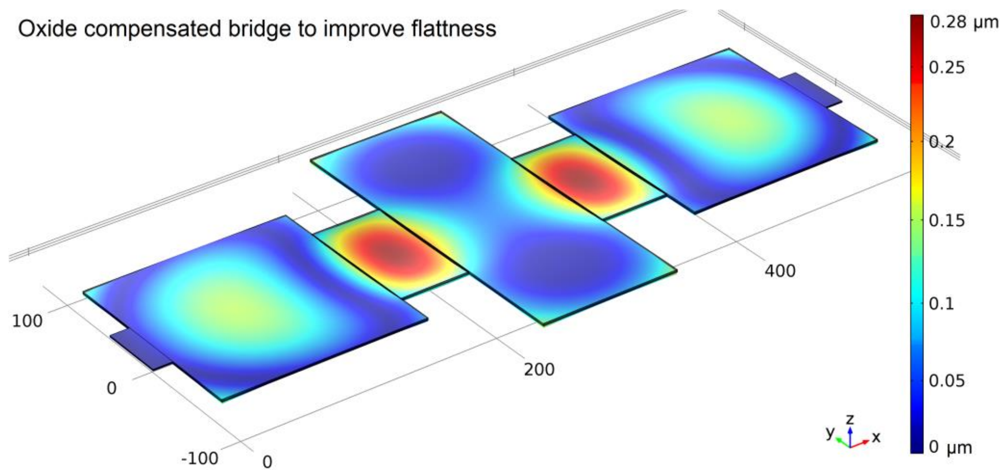

Fig. A.4: COMSOL simulation of RF switch with oxide compensation to improve flatness.

When 300 nm (not the simulated 500 nm) of extra oxide was added to the fabrication process for the RF switches (ONO, 0.15 / 1.4 / 0.45 µm), the bending was significantly reduced (to ≈100 nm across the mid-section), shown in Fig. A.5.

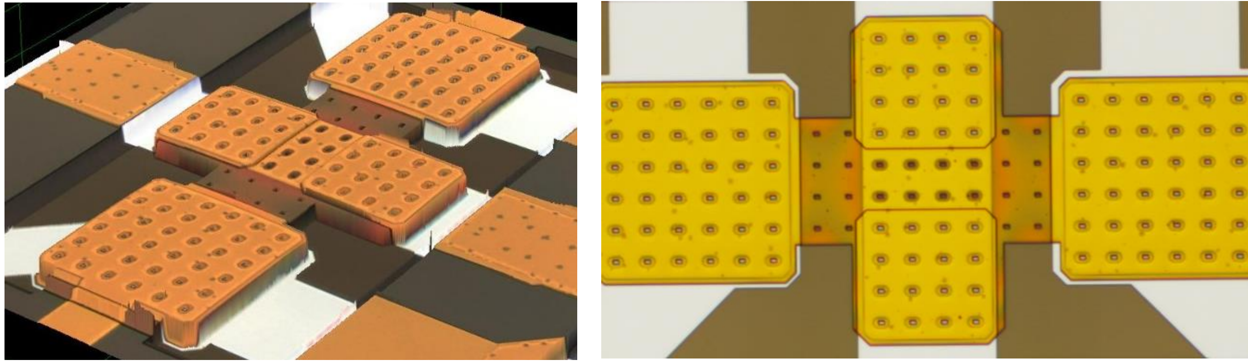
Fig. A.5: RF Switch bridge bending with 300 nm of oxide on top. Measured bending of ≈100 nm. 3D Interferometer (left) and optical (right) images shown.

However, the yield of the RF switches still remained low due to inconsistencies in the stress and thickness levels of the PECVD layers. While it is easy to simulate how stress will affect the bending of the bridge, actually depositing the material with the characterized stress and thickness is much more difficult in practice, especially when small deviations from ideal have such large impacts on the fabricated device. In the first attempt to flatten the RF switches, 500 nm of oxide (the simulated value) was added, but the bridge bent in the opposite direction, as shown in Fig. A.6. It is likely that the simulated stress value of the upper electrode was slightly below the actual values, leading to this over-correction. It was not until a slightly thinner layer (the successful 300 nm) was used, that the bending was corrected.

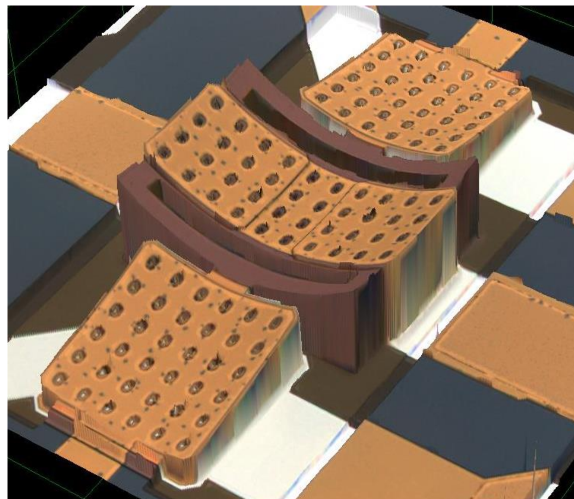
Fig. A.6: Interferometer image of RF switch with 500 nm of oxide added to the top of the dielectric stack, resulting in stress overcompensation and convex bending.

APPENDIX B: Silicon Substrate Process Development

A silicon substrate process was designed to increase the potential for greater dimensional scalability and sensitivity of a bonded silicon/glass process [Eun14] by utilizing surface micromachining of a silicon wafer. This single-p^{++} doped-silicon-wafer fabrication consists of a dry, low temperature (≤400°C) process with 8-mask lithographic microfabrication steps using plasma-based dielectric deposition for structural components and amorphous silicon (α-Si) serving as a sacrificial layer for diaphragm definition [Luo16]. Highly doped, low resistivity (<0.005 Ω-cm) wafers were used to provide electrical connections through its thickness to allow for backside contacts and extreme dimensional scaling. Because etching deep and narrow trenches through silicon to define the insulating boundaries is limited by the DRIE tool aspect ratio, thin wafers (≈300 μm) are selected from the start to reduce the amount of wafer thinning required. A 3-D model and cross section of the capacitive sensor are shown in Fig. B.1 and the process flow is shown in Fig. B.2.

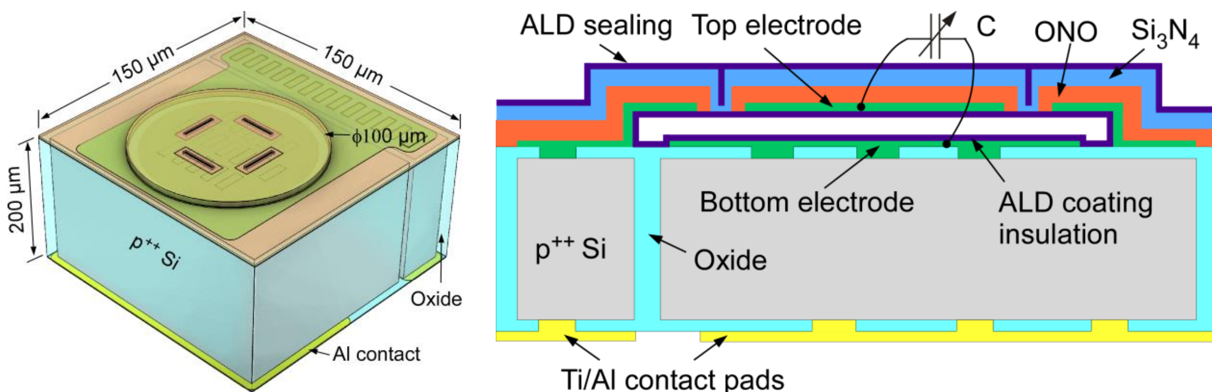

Fig. B.1: 3-D illustration and cross section of silicon capacitive pressure sensor [Luo16].

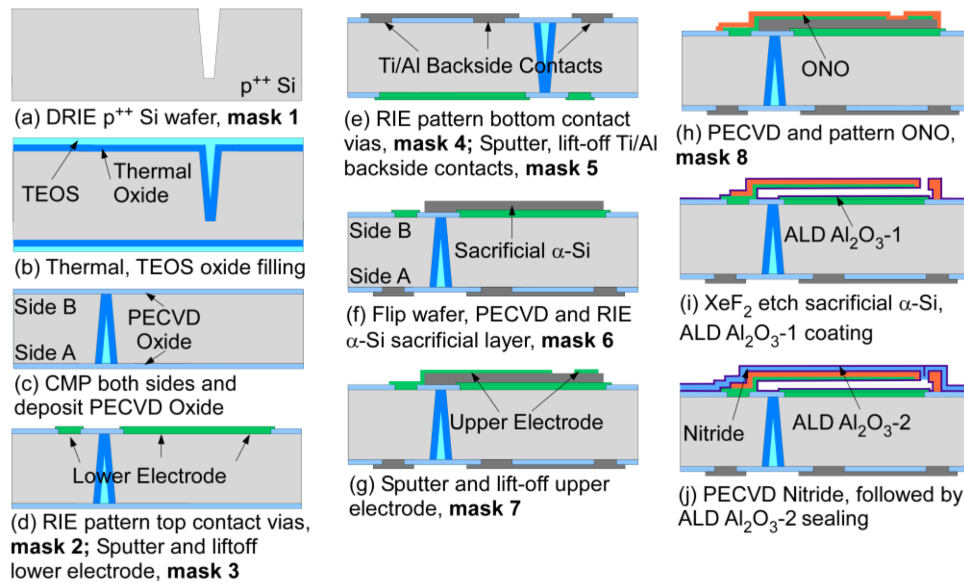

Fig. B.2: p^{++} silicon process flow for capacitive pressure sensor fabrication.

The first step is to deep reactive ion etch (DRIE) insulating channels with 4 μm wide and 250 μm deep features. The resulting trenches are fully filled with silicon oxide combining both thermal oxide and tetraethyl orthosilicate (TEOS) oxide. Thermal oxide provides the highest insulation strength, whereas TEOS provides conformal filling to prevent void formation in refilled trenches. Following oxide refilling, the wafers are polished on both sides using chemical mechanical polishing (CMP), which provides a flat, mirror surface finish. After polishing, PECVD oxide is deposited on both sides to provide insulation. Oxide layers are then selectively dry etched by RIE to provide contact vias for Ni electrodes and backside Al contacts. The Ni and Al electrodes are patterned using lift-off. The sacrificial layer for the discharge chamber is formed by a 3 μm-thick layer of PECVD amorphous silicon (α-Si). The top Ni electrodes are also patterned using lift-off. To provide good step coverage across the α-Si layer, Ni is deposited using sputtering instead of evaporation. A stack of PECVD ONO (oxide-nitride-oxide, ONO, 0.1 μm/0.8 μm/0.1 μm) is deposited to form the initial diaphragm structure, and patterned with etchant access slits. The sacrificial α-Si layer is etched by gas phase XeF_2, which provides isotropic etching and very high selectivity to other materials. ALD Al_2O_3 is deposited to provide

in situ electrode insulation to allow for touch mode operation in which the diaphragm is deflected into the substrate, extending the full-scale range. Etchant access slit and diaphragm sealing is performed by another layer of PECVD nitride, followed by atomic layer deposition (ALD) of Al_2O_3 for hermetic sealing.

Before device fabrication began, characterization of the DRIE trenches and oxide refilling, PECVD α-Si stress, and PECVD nitride stress was completed. A DRIE recipe limiting undercut at the trench opening (which inhibits oxide refilling) was utilized. High α-Si stress can result in wafer bending, film delamination, or complete wafer cracking in extreme cases. Therefore, a low stress recipe was created to allow for the thick (3.0 µm) deposition for cavity definition. High stress nitride can also cause device failure by cracking diaphragms with a large shearing force post-deposition. While these characterization steps were taken to increase the chances of a successful fabrication run, due to the nature of this untested prototype process, several additional issues were encountered during fabrication and addressed in order to yield devices for testing.

B.1. Fabrication Challenges and Improvements

Nitride Characterization: While the stress and deposition rate of the PECVD nitride was carefully characterized before fabrication began (at ideal targets of 58 MPa tensile and 29 Å/s), it was found that by the time the fabrication run was begun, the custom recipe had drifted and there were large variations in the these values from run-to-run, shown in Table B.1, resulting in nitride stress varying between 91 and 175 MPa and deposition rates varying between 22.9 and 35.3 Å/s (resulting in thickness of ±150 nm for the 800 nm nitride layer). In order to correct this, a new recipe was characterized with a lower temperature (380°C → 350°C), reduced Silane flow (50 sccm → 40 sccm), and reduced NH3 flow (40 sccm → 35 sccm). It was thought that by reducing the silane flow, the deposited nitride would be closer to its true stoichiometric ratio of

Si_3N_4, and therefore a more stable deposition in terms of stress and deposition rate. However, the silane was originally increased to reduce the stress of the standard nitride recipe (which was nearly 300 MPa when deposited at 380°C with a silane flow of 33 sccm). Therefore, the temperature was reduced in order to reduce the stress. (The NH_3 flow was also reduced to reduce the potential for large amounts of trapped hydrogen in the film during deposition.) These changes resulted in a reduced stress variance (134 ± 20 MPa) and reduced deposition rate variance (25.6 ± 2.7 Å/s). Due to the potential for a compressive film stress given the tool variances, a slightly higher tensile stress was targeted in order to ensure that even if a lower stress value was created, it would still result in a tensile film, as compressive stress can lead to buckled diaphragms and device failure.

Table B.1: GSI PECVD Nitride Characterization Data

Temp [°C]	SiH_4 [sccm]	NH_3 [sccm]	P [Torr]	RF2 [W]	Dep rate [Å/s]	Stress [MPa]
Modified Recipe #1 Characterization						
380	50	40	3.5	60	35.3	91
380	50	40	3.5	60	26.7	150
380	50	40	3.5	60	22.9	175
380	50	40	3.5	60	33.7	99
380	50	40	3.5	60	23.9	159
380	50	40	3.5	60	35.4	108
Modified Recipe #2 Characterization						
350	40	35	3.5	60	25.7	136
350	40	35	3.5	60	28.4	114
350	40	35	3.5	60	22.9	154

B.2. Fabricated Devices and Test Results

After these fabrication challenges were addressed, smaller diameter capacitive devices (≤ø100 μm) yielded at ≈25%, allowing for a few devices to be successfully tested (shown in Fig. B.3). Each diced device is first mounted to a prototype printed circuit board using conductive silver epoxy. Successful testing of capacitive devices was demonstrated, results shown in Fig. B.4

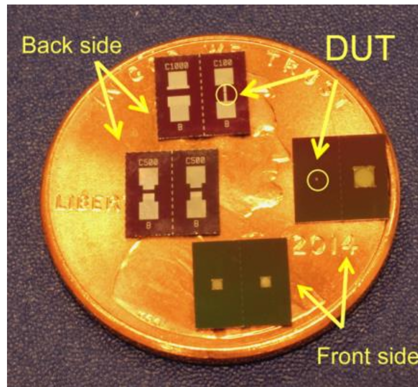

Fig. B.3: Fabricated capacitive device chips diced

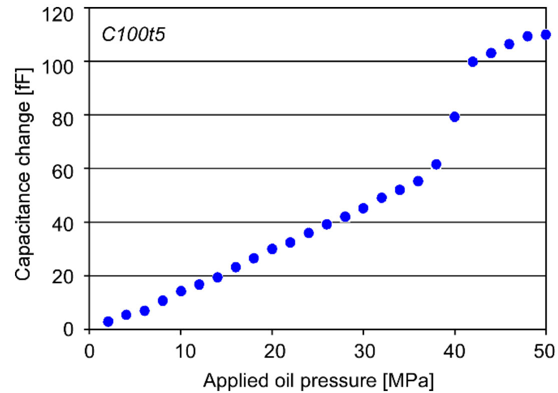

Fig. B.4: Pressure response of a capacitive sensor. Each data point represents an average of ≈30 readings. Error bars not visible.

B.3. Discussion and Summary of Silicon Substrate Process Results

By addressing several process issues before and during fabrication, a single-silicon-wafer fabrication process was developed such that prototype capacitive pressure sensors were successfully fabricated. However, yield still remained low at ≈25% due primarily to diaphragm cracking from high metal stress concentrations, blow-out of larger diaphragms during tool vacuum pump-downs, and wafer cracking and surface roughness resulting from the use of CMP thinned wafers for trench isolation. The capacitive devices also suffered from large parasitic capacitances and TCO (≈25,000 ppm/°C) believed to be caused by the thermal mismatch of the Si/SiO_2 isolation trench parasitic capacitances and PECVD diaphragm and substrate and TCO parasitic capacitances the test PCB and silver epoxy used for electrical connection. However, this fabrication run demonstrated the potential for creating a dry, low temperature, robust process with the potential capability of fabricating many different kinds of devices, assuming the yield could be increased, the parasitic capacitances reduced, and the large TCO decreased.

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