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ADVANCED ENERGY MATERIALS

Supporting Information

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Quantifying Losses and Assessing the Photovoltage Limits in Metal–Insulator–Semiconductor Water Splitting Systems

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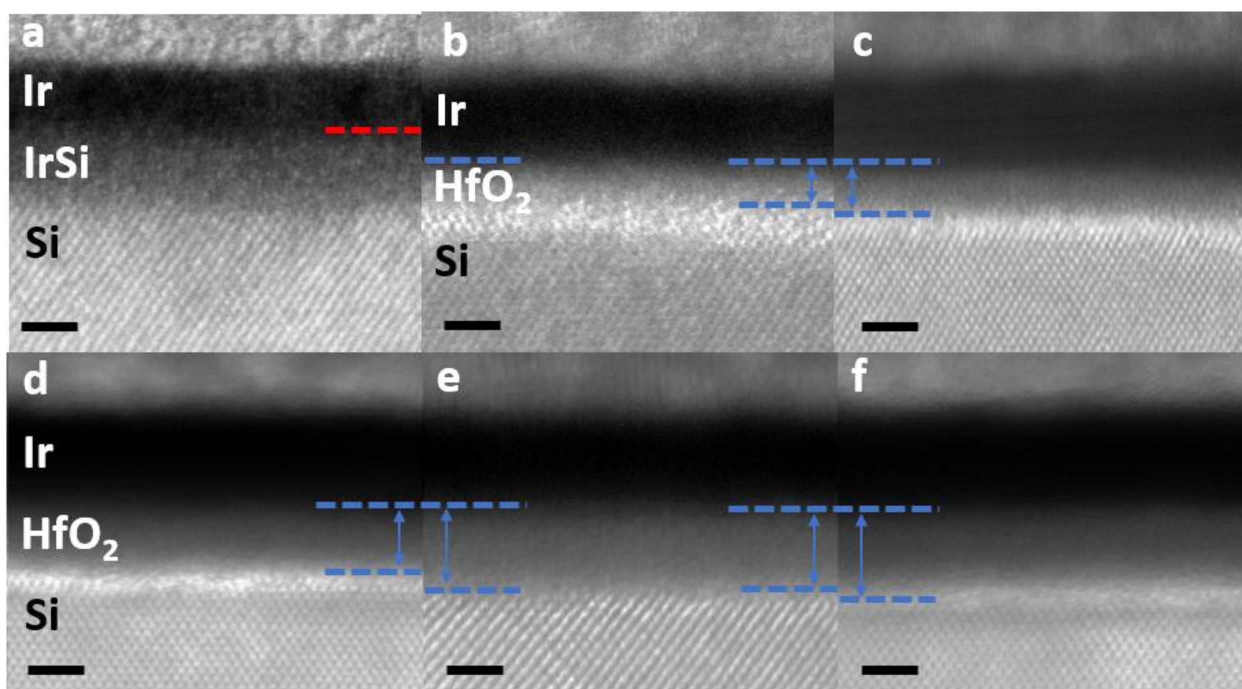

Figure S1: Cross-sectional STEM images of 3.5 nm-Ir/x- HfO_2/n-Si samples. (a) 0 cycles (0 nm) HfO_2, (b) 13 cycles (1.4 nm), (c) 16 cycles (1.6 nm) HfO_2, (d) 19 cycles (2.0 nm) HfO_2, (e) 22 cycles (2.3 nm) HfO_2, and (f) 25 cycles (2.6 nm) HfO_2. The blue arrows represent the thickness of the HfO_2 layer. The black scale bar is 2 nm. We note that the 0 nm HfO_2 has no insulator layer to protect the Si, so when depositing the Ir layer, the Ir penetrates into the Si forming an iridium silicide layer.[1] Therefore, the pure Ir layer is thinner than the other samples, as indicated by the red dashed line in (a).

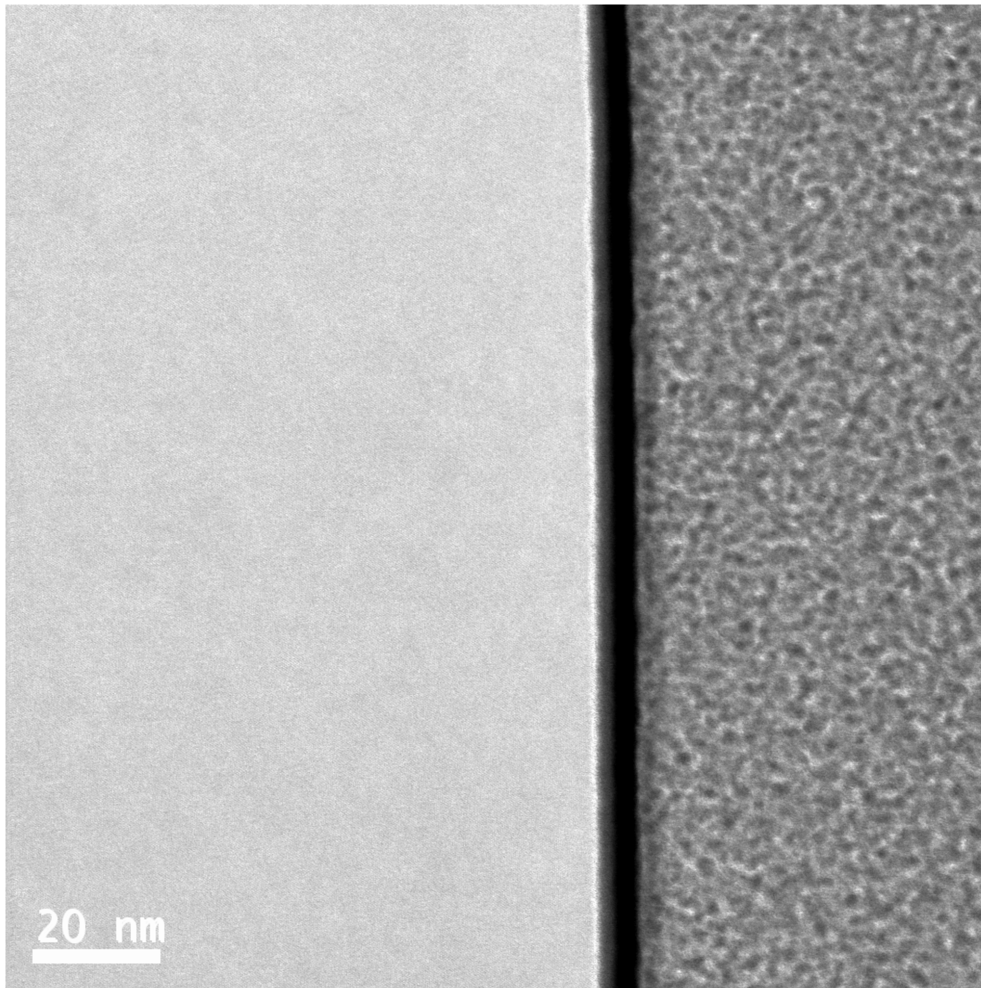

Figure S2: Lower magnification image of the 3.5 nm-Ir/2.3 nm-HfO_2/n-Si sample showing the clear, uniform layers over a wide area. From left to right, the layers are the thick Silicon substrate, thin 0.5nm SiO_2, 2.3 nm HfO_2, 3.5 nm Ir, thick Pt glue/protection.

Insulator lack of pinholes and uniformity

ALD is a widely-recognized method to deposit pinhole-free, conformal layers with sub-nanometer precision.[2,3] Many papers in the water splitting literature have reported ALD of insulator layers in the 1-3 nm range, and no evidence of pinholes has been found for TiO_2,[3,4] Al_2O_3,[5–7] and HfO_2[8,9]. To further support this point, we performed cyclic voltammetry on unmodified n-Si, and on a sample with 19 cycles of HfO_2 deposited on n-Si without a metal layer (Figure S3). The current density of the unmodified n-Si was 1000 times higher than the HfO_2 sample indicating that the HfO_2 sufficiently protects the underlying Si. If pinholes were present, the electrolyte would quickly travel through the pinholes causing an increased and unstable current. Upon cycling the HfO_2 sample, the current remained low and stable, so the presence of pinholes is negligible.

Despite the fact that STEM cross-sections cover a small portion of a given sample, we expect the insulator layer to be uniform throughout the entire wafer.[3,8] For a given HfO_2 thickness deposited on a wafer, the photovoltage was evaluated from multiple pieces throughout the wafer, and only a few mV photovoltage variation is obtained. Even small variations in HfO_2 thickness is expected to significantly change the photovoltage. Therefore, we conclude the HfO_2 thickness obtained from STEM cross-sections is representative throughout the wafer.

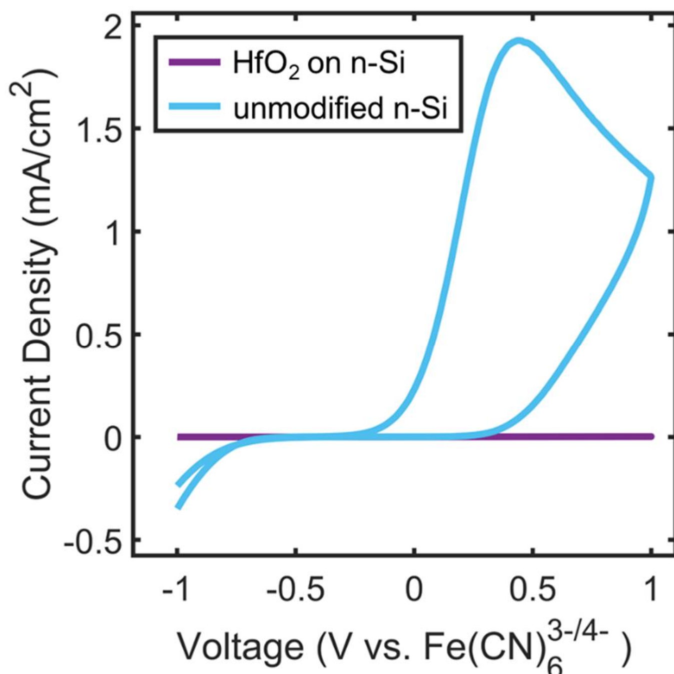

Figure S3: CVs performed in 10/10 mM FFC under 1 sun illumination for an unmodified n-Si sample, and on a sample with 2 nm HfO_2 deposited on n-Si without a metal layer.

Stability of 3.5nm-Ir/2.3nm-HfO_2/n-Si sample

Chronoamperometry was used to assess the stability of a 3.5nm-Ir/2.3nm-HfO_2/n-Si sample. The stability test was performed in 1 M KOH under 1 sun illumination and the sample was held at 1.8 V vs RHE. As shown in Figure S4a, the photocurrent was stable (and slightly increased) over the course of 6 hours with no signs of permanent degradation. Transient drops in the current during the chronoamperometry test are due to the formation and removal of bubbles. LSVs taken every two hours are shown in Figure S4b. The photovoltage and fill factor remained the same throughout the stability test. The photolimited current slightly increased over time as the Ir layer oxidized to IrO_x which allows more light transmission. The increased oxidation of Ir over time is evident from the increase in the oxidation peaks just before the onset of oxygen evolution at about 1 V vs RHE.

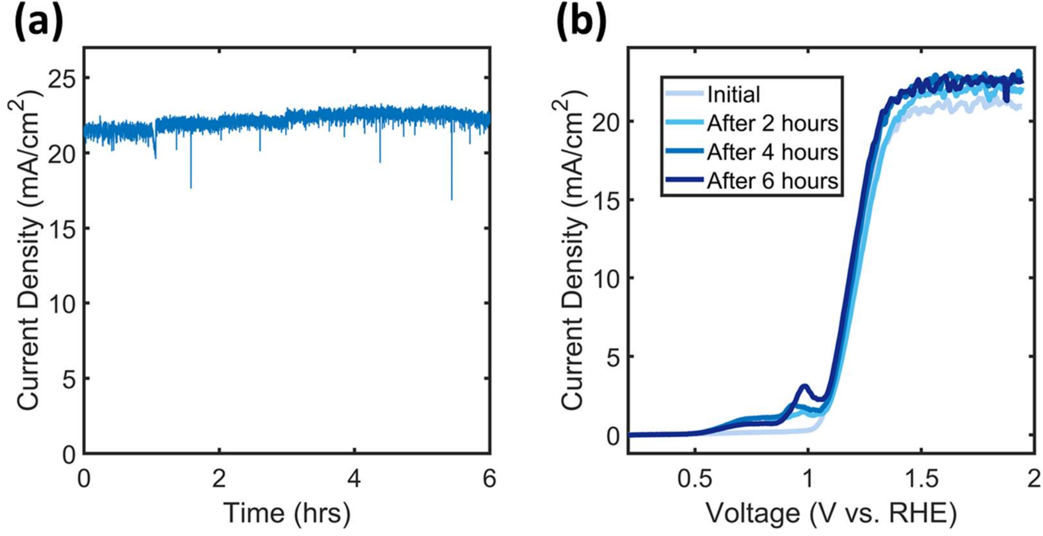

Figure S4: Stability tests on the 3.5nm Ir/2.3nm HfO_2/n-Si sample performed in 1 M KOH under 1 sun illumination (a) Chronoamperometry stability test at an applied potential of 1.8 V vs RHE. (b) LSVs at 2 hour intervals showing stable photovoltage and fill factor.

Showing that $|V_{oc}| < |V_{oc,ideal}|$ for non-ideal systems (n>1)

By plugging Equation 3 into Equation 4a from the main text, an expression for V_{oc} is obtained:

$$-V_{oc} = \frac{nkT}{q} ln\left(\frac{J_{ph}}{A^*T^2}\right) + \phi_{b,ideal} + (n-1)V_n + \frac{nkT}{q} \propto d\sqrt{\phi_n} \quad (S1)$$

Using Equation 4b in the main text $|V_{oc}| - |V_{oc,ideal}|$ can be evaluated:

$$|V_{oc}| - |V_{oc,ideal}| = (n-1)\frac{kT}{q}\, ln\left(\frac{J_{ph}}{A^*T^2}\right) + (n-1)V_n + (n-1)\frac{kT}{q} \propto d\sqrt{\phi_n} \quad (S2)$$

Which simplifies to:

$$|V_{oc,non-ideal}| - |V_{oc,ideal}| = (n-1)\left[\frac{kT}{q}\, ln\left(\frac{J_{ph}}{A^*T^2}\right) + V_n + \frac{kT}{q} \propto d\sqrt{\phi_n}\right] \quad (S3)$$

The term $(n-1)$ is always a positive number so it can be shown that $|V_{oc,non-ideal}| > |V_{oc,ideal}|$ only if:

$$J_{ph} > A^{*}T^{2}exp\left(-\frac{q}{kT}V_{n} - \propto d\sqrt{\phi_{n}}\ \right) \ (S4)$$

Using the experimental values measured in the paper, the value of J_{ph} necessary for this condition to be true is ~ 290 mA/cm^2 for the 2.0 nm HfO_2 system and even larger for lower HfO_2 thicknesses. This is significantly larger than the experimental J_{ph} of ~25 mA/cm^2 (Figure 2a). Therefore, the constraint in Equation S4 doesn't hold and this shows that a high ideality factor will result in a lower open-circuit photovoltage for all practical conditions and confirms $|V_{oc}| < |V_{oc,ideal}|$. The loss in open-circuit voltage as a function of ideality factor is plotted in Figure S5.

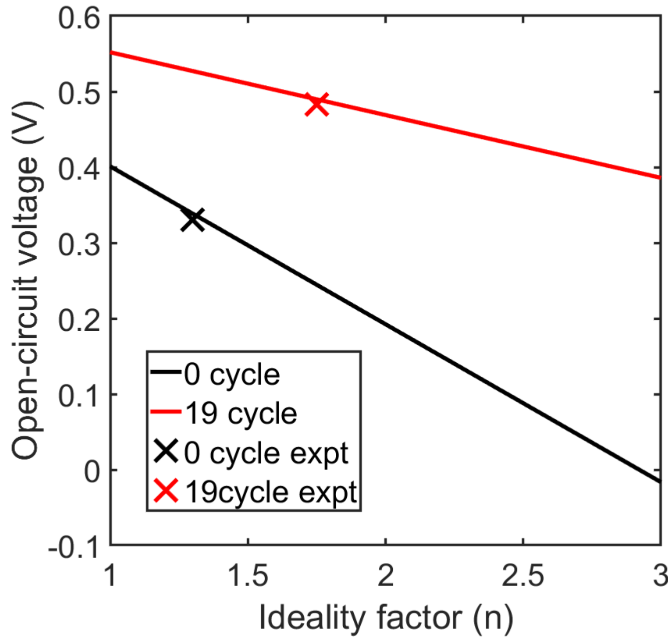

Figure S5*:* Plot of open-circuit voltage decreasing as a function of ideality factor for the 0 cycle and 19 cycle samples. The "x" indicates the experimental values.

Other possible contributions to the ideality factor

Besides the insulator voltage drop, several other non-idealities will also have a small effect on the ideality factor. These include image force lowering, barrier height inhomogeneity, field emission, and recombination in the semiconductor space charge (band bending) region.

Image force lowering results from image charges building up in the metal as charge carriers approach the metal/semiconductor interface. The potential associated with these image charges lowers the barrier height, and the ideality factor resulting from image forces (n_{imf}) is given by:[10]

$$\frac{1}{n_{imf}} = 1 - \frac{1}{4}\left(\frac{q^3 N_d}{8\pi^2 \varepsilon_s^3}\right)^{\frac{1}{4}} \left(\phi_b - V_a - V_n - \frac{kT}{q}\right)^{-\frac{3}{4}} \quad (S5)$$

The resulting ideality factors for all systems is less than 1.005 for V_a = 0V and less than 1.03 for V_a =0.5V. The resulting reduction in the barrier height is less than 13 meV for all samples. Thus the image force lowering has a low impact on the ideality factor and system performance.

Field emission occurs when electrons travel to the metal by tunneling through the space charge region rather than by thermionically emitting over the barrier. This occurs in highly doped semiconductors where the space charge region is very narrow which enables facile electron tunneling. The result is a reduction in the effective barrier height and an increase in ideality factor. The ideality factor from field emission (n_{fe}) is given by:[11]

$$n_{fe} = \frac{qE_{00}}{kT} \coth\left(\frac{qE_{00}}{kT}\right) \quad ; \quad E_{00} = \frac{h}{4\pi}\left(\frac{N_d}{m_e^* \varepsilon_s}\right)^{1/2} \quad (S6)$$

Here, m_e^* is the effective mass of the electron. For the systems studied, the n_{fe} is effectively equal to 1 and the maximum lowering of the barrier height is less than 4 meV. Thus field emission cannot account for the high ideality found in each sample.

The diode equation is derived assuming that the recombination occurs radiatively in the semiconductor bulk. However, real systems may have some degree of recombination in the space charge region. The theoretical ideality factor for such a system is about 2.[12,13] Silicon based diodes have large charge carrier mobilities and thus the space charge recombination is usually not significant at room temperature.[10] Previous studies have found that recombination in the space charge region have a negligible effect on the performance in MIS systems at room temperature.[11,14] Using a typical carrier lifetime of 2e-5 seconds for silicon,[11,14,15] the calculated reverse saturation current from space charge recombination is 3.5e-6 mA/cm^2, which is 2 orders of magnitude lower than the values calculated in Figure 3a of main text. Thus, the contributions from space charge recombination are expected to be small.

Another situation that may result in high ideality factor is inhomogeneous barrier heights throughout the system. It is generally assumed that the thickness of the insulator is not constant through the system, but exhibits a Gaussian distribution.[11,14,16,17] As voltage is applied, the charge carriers can overcome higher barriers which changes the overall effective barrier height of the system. From the variation in the HfO_2 thickness measurements, we don't expect significant differences between samples with different HfO_2 thicknesses. To help confirm this, we have synthesized a 19 cycle sample on a higher doped wafers (0.1-1 ohm-cm resistivity) as opposed to the other samples which were on lower doped wafers (5-8 ohm-cm resistivity). Both the higher doped and lower doped wafers were processed in parallel under identical conditions, so each 19 cycle sample should have similar thickness and inhomogeneity of the HfO_2 layer.

Therefore, if inhomogeneous barrier heights were dominating the ideality factor, then both 19 cycle samples would be expected to have the same ideality factor. The results show that the ideality factor for the higher doped sample is about 2.7 compared to 1.7 for the lower doped sample (Figure S13). Thus inhomogeneous barrier heights are probably not a dominant factor in the ideality factor.

Density of surface states from ideality factor:

None of the factors in the previous section can explain the high ideality factors observed in the MIS systems, which leaves the voltage drop resulting from surface states as the most likely explanation. The origin of the voltage drop in the insulator layer is the buildup of charge in the system as governed by Gauss's Law:[18]

$$\Delta V_i = -d\frac{Q_m}{\varepsilon_i} \qquad (S7)$$

Where d is the insulator thickness, Q_m is the charge in the metal and ε_i is the insulator permittivity. From conservation of charge, the charge in the metal is balanced by the charge on the other side of the insulator which includes contributions from the space charge region (Q_{sc}), the charge in the surface states (Q_{ss}) and the fixed charge (Q_f):

$$-Q_m = Q_{sc} + Q_{ss} + Q_f \qquad (S8)$$

Making the substitution:

$$\Delta V_i = \frac{d}{\varepsilon_i}\left(Q_{sc} + Q_{ss} + Q_f\right) \qquad (S9)$$

It is shown in below discussion fixed charge in the system is negligible. Furthermore, the CV's in Figure S6 show that there is no photoinduced charging of the insulator upon illuminating a 19 cycle p^+-Si sample.

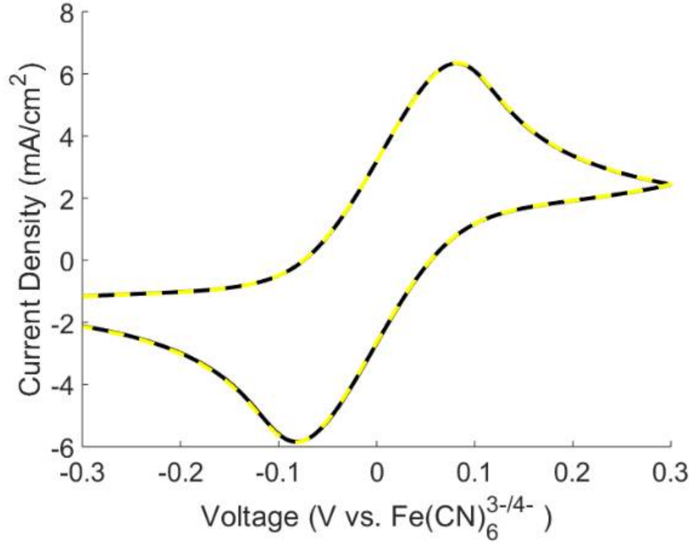

Figure S6: CV of a 3.5 nm-Ir/19 cycle HfO_2/p^+-Si sample in dark (black) and under illumination (yellow) in 10/10 mM FFC solution. The curves are identical which indicates that there is no photoinduced charging of the insulator.

By neglecting fixed charge, the following expression relating the ideality factor to the density of surface states and charge in the space charge region has been previously derived:[18]

$$n = 1 + \frac{\frac{d}{\varepsilon_i}\left(\frac{\varepsilon_s}{W} + qD_s\right)}{1 + \frac{d}{\varepsilon_i} qD_m} \quad (S10)$$

Where, W is the width of the space charge region, ε_s and ε_i are the semiconductor and insulator permittivity. D_s and D_m are the density of surface states in equilibrium with the semiconductor

and the metal, respectively. Assuming that the surface states are only in equilibrium with the semiconductor ($D_m = 0$), then Equation 5 from the main text is obtained. For an ideal system without surface states ($D_m = D_s = 0$), the only charge in the system is from the space charge region and the ideality factor simplifies to:

$$n = 1 + \frac{d\varepsilon_s}{W\varepsilon_i} \qquad (S11)$$

The ideality factor in Equation S11 is the lowest theoretical value that the system can obtain because the charge in the space charge region is unavoidable. Because the ε_i for HfO_2 is relatively large, the ideality factor obtained from Equation S11 is less than 1.001, even for the thickest samples of 2.6 nm. Only a 1 mV drop in the insulator layer is expected. Therefore, the system can achieve essentially ideal performance if there are no contributions from surface states. We note that the above analysis assumes that the insulator parameters are governed by the HfO_2 layer and not the thin interfacial SiO_2 layer because the HfO_2 layer is much thicker.

Based on the experimentally obtained ideality factor of 1.7 for the 19 cycle sample, the expected voltage drop in the insulator layer is 270 mV which results in significant lowering of the barrier height. Assuming that the ideality factor is entirely described by Equation S10 and $D_m = 0$, then the density of surface states in equilibrium with the semiconductor can be calculated. These values are shown in Figure S7. The 0 cycle sample, which is assumed to have an interfacial SiO2 layer of 0.5 nm, has the highest density of surface states. This is the expected result because metal/semiconductor contacts are known to have a significant density of defects from metal-induced gap states (MIGS).[10,19] The number of defects decreases significantly when an HfO_2 layer is introduced. HfO_2 and other high-k dielectrics are known to passivate defects present at metal/semiconductor contacts and reduce the influence of MIGS. However, thicker

HfO_2 results in a higher density of defects in Figure S7 while MIGS theory predicts the opposite behavior. It is not clear exactly why the surface state density would increase with increasing HfO_2 thickness, but these types of trends have also been previously observed with SiO_2.[18] We note that the data in Figure S7 is the upper limit of the density of surface states because here it is assumed that all of the non-idealities are from insulator voltage drop. Other non-idealities may be present to a small degree, as discussed in the previous section.

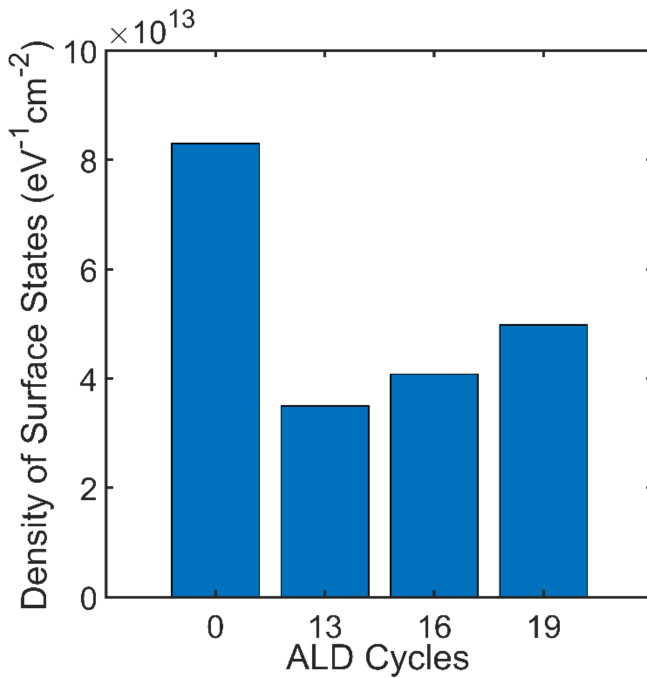

Figure S7: Estimated density of interface states as a function of insulator thickness (HfO_2 ALD cycles).

MIS Thick Insulator Regime

For thin insulator MIS systems (0-2.0 nm HfO_2), the performance can be accurately modeled using Equations 1-4 from the main text. Equation 4 indicates that increasing the

insulator thickness would indefinitely continue increasing the open-circuit photovoltage. However, for thick insulators (>2 nm HfO_2), eventually the minority carrier current is hindered which ultimately limits the photovoltage. The minority carrier tunneling current is given by:[20]

$$J_{h,t} = \frac{4qm_{h,eff}(kT)^2}{h^3 N_V} p_s exp\left(-\propto_t d\sqrt{\phi_p}\right) exp\left(1 - \frac{-\Delta}{kT}\right) \quad (S12)$$

Here, $m_{h,eff}$ is the effective mass for holes, h is Planck's constant, N_V is the effective density of states in the silicon valence band, p_s is the concentration of holes at the Si-insulator interface, ϕ_p is the mean barrier for holes provided by the insulator, and Δ is the energy difference between the metal Fermi level and the hole quasi-Fermi level (see Figure S8c). For thin insulators, effectively all the photogenerated holes will tunnel through the insulator layer to the metal where it can catalyze the reaction. For thick insulators, p_s and Δ must increase to enable the same tunneling current through the insulator. The photovoltage loss is manifested in the Δ term, which is described as a charge extraction loss.

Figure S8 illustrates the thickness dependent tradeoff for ideal systems with no insulator voltage drop (n=1). For the thin insulator in Figure S8a, $J_{h,t}$ is not significantly impeded so there are no losses associated with holes tunneling through the thin insulator. However, J_s is also relatively large resulting in significant electron recombination and a lower photovoltage (i.e. the photovoltage losses are dominated by electron recombination). For the intermediate insulator thickness in Figure S8b, electron recombination is reduced while not significantly impeding $J_{h,t}$. For the thick insulator in Figure S8c, $J_{h,t}$ is significantly impeded, resulting in a charge extraction loss (Δ) which limits the photovoltage (i.e. the photovoltage losses are dominated by hole recombination). In summary, there is a fundamental tradeoff associated with balancing the

losses from the electron recombination current (J_s) and the losses from the hole tunneling current ($J_{h,t}$).

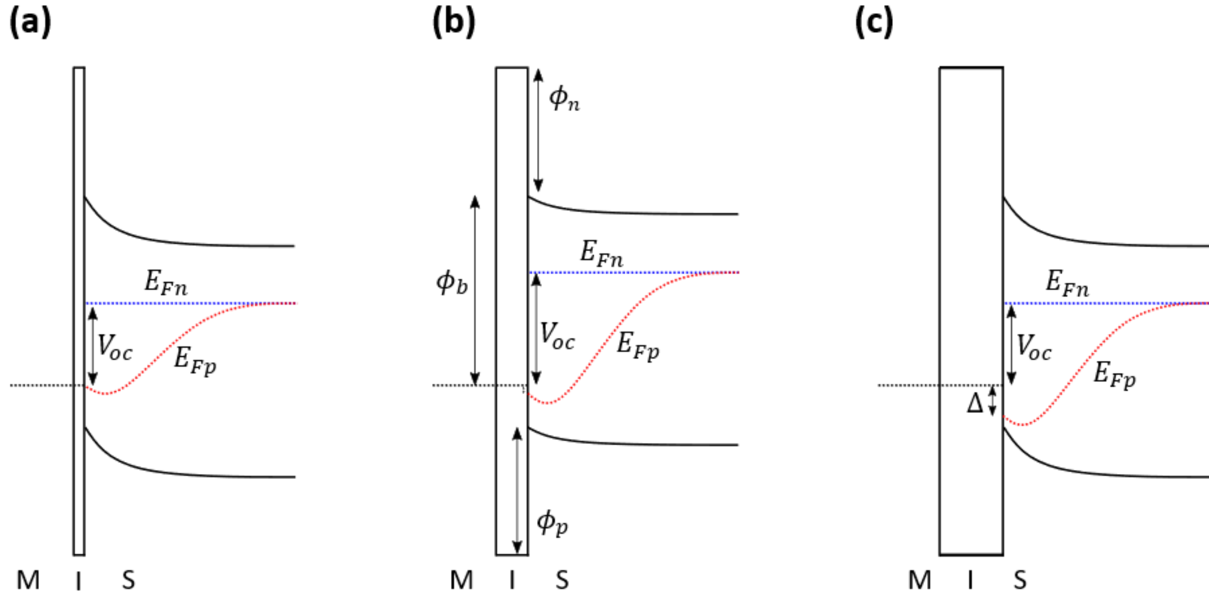

Figure S8: Energy band diagram in quasi-equilibrium (no applied voltage) for illuminated MIS systems with different insulator thicknesses. (a) Thin insulator with a low photovoltage due to significant electron recombination current. (b) Intermediate insulator thickness with optimal photovoltage due to balanced electron recombination current and hole tunneling current. (c) Thick insulator with a lower photovoltage due to impeded hole tunneling current resulting in a charge extraction barrier (Δ). These systems are ideal (n=1) meaning there is negligible voltage drop in the insulator. V_{ph} is the photovoltage which corresponds to 400 mV in (a, c) and 550 mV in (b). Panel (b) illustrates the barrier height (ϕ_b), and insulator barrier for holes (ϕ_p) and electrons (ϕ_n), which are all identical for each of the systems. E_{Fn} and E_{Fp} are the quasi Fermi levels for electrons and holes, respectively.

Because of the additional losses associated with thicker insulators, Equations 1-4 of the main text to not apply for thick insulators. Thus, the ideality factor and reverse saturation current measured by varying the light intensity will not be accurate for thick insulator samples. The extracted values for all thicknesses are shown in Figure S9. Further analysis of the thick insulators (> 2 nm) is beyond the scope of this study.

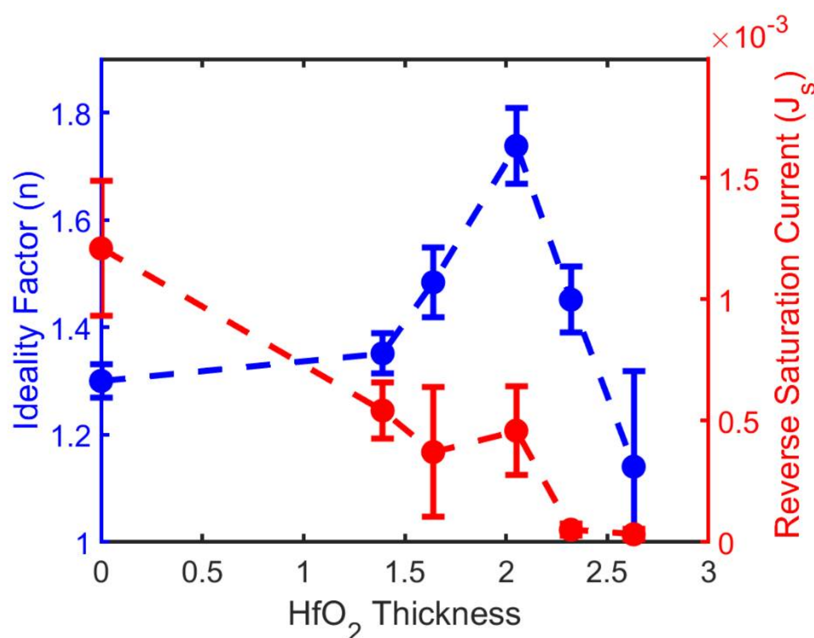

Figure S9: Ideality factor and reverse saturation current for all 3.5 nm-Ir/x-HfO_2/n-Si samples measured by varying light intensity in 350/50 mM FFC and 1 M KCl

Electrochemical Impedance Spectroscopy

To calculate the flat-band potential of the system, the capacitance of the space charge region (C_{sc}) was found experimentally at different applied voltages using electrochemical impedance spectroscopy. The space charge capacitance was extracted by fitting the impedance

data with the equivalent circuit in Figure S10. In the circuit, R_{series} is the series resistance attributed to solution resistance and bulk resistance, $R_{parallel}$ is the parallel resistance attributed to charge transfer through the system. C_{sc} is the capacitance of the space charge region, and C_{ox} is the capacitance of the HfO_2 insulator layer which is calculated by the following equation:

$$C_{ox} = \frac{\varepsilon_{ox} A}{d} \quad (S13)$$

Where ε_{ox} is the permittivity of the HfO_2 which is assumed to be equivalent to the bulk permittivity of $25\varepsilon_0$ (ε_0=8.85e-12 C V^{-1} m^{-1}), A is the surface area of the sample (1.69 cm^2), and d is the HfO_2 thickness. We note that capacitance of the Helmholtz layer has a negligible influence on the system's total series capacitance, so it is not included in the equivalent circuit. Furthermore, the metal/solution charge transfer resistance is neglected due to the facile kinetics of the FFC redox solution.

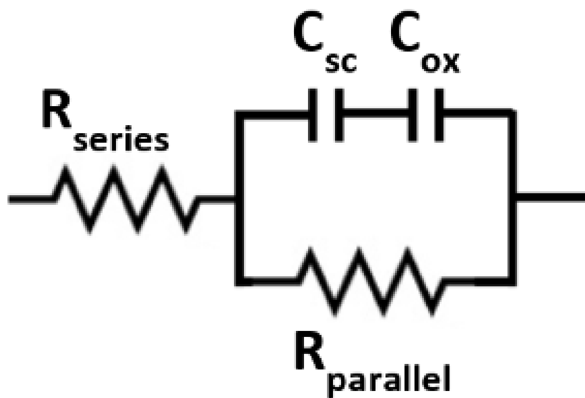

Figure S10: Equivalent circuit used to fit the impedance data.

A representative example of an EIS Bode plot and Nyquist plot for the 19 cycle sample at 0.3 V vs $Fe(CN)_6^{3-/4-}$ is shown in Figure S11. The fitting occurs in a frequency range of 3000-

200,000 Hz which is the region dominated by the capacitive response (phase angle close to -90 degrees).[6,21] Frequencies lower than 3000 Hz resulted in deviations from the characteristic semicircle shape in the Nyquist plot, indicating surface states may be influencing the capacitance for these lower frequencies. After measuring C_{sc} with EIS, the Mott-Schottky equation is used to measure the flat-band potential (V_{fb}):

$$\left(\frac{1}{C_{sc}}\right)^2 = \frac{2}{\varepsilon_s A^2 q N_D}\left(V_a - V_{fb} - \frac{kT}{q}\right) \quad (S14)$$

This equation was defined in the main text Equation 6 and the resulting Mott-Schottky plots are shown for all thicknesses in figure 4a. We note that all of the Mott-Schottky plots are linear, which indicates that surface states are not affecting the measured capacitance for the selected frequency range.[18,22] .

If significant bulk charge or fixed charge were present in the system, we would expect a parabolic or linear shift of V_{fb} with increasing thickness based on the following equation[23]:

$$\mathrm{V_{fb}} = \phi_{\mathrm{m}} - \phi_{\mathrm{s}} - \frac{Q_f}{C_{ox}} - \frac{Q_{bulk} d}{2C_{ox}} \quad (S15)$$

Here, ϕ_{m} is the work function (Fermi level) of the metal, and ϕ_{s} is the Fermi level of Si, Q_f is the fixed charge per unit area located at the semiconductor/insulator interface and Q_{bulk} is the bulk charge per unit volume in the insulator layer. The flat-band potentials in Figure 4b are independent of insulator thickness which indicates the samples have a negligible amount of fixed or bulk charges.

The ideal barrier height (ϕ_{ideal}) is then calculated from the flat-band potential:

$$\phi_{b,ideal} = V_{fb} + V_n = V_{fb} + \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \quad (S16)$$

This equation was defined in the main text Equation 7. The measured values for N_D, V_{fb}, and ϕ_{ideal} are listed in Table S1. The observed range of the doping density determined from the slope of the Mott-Schottky plots is consistent with the manufacturer's specifications. The small variation in N_D results in a Si Fermi level change (V_n) of less than 10 mV, so it affects the calculated values of ϕ_{ideal} and the photovoltages by less than 1.5%. For the 0 cycle sample as well as a duplicate 19 cycle sample, the resistivity of the pristine Si wafer substrates was measured using a four-point probe, and the resistivity was converted to doping density. After measuring resistivity, the wafers were processed normally as described in the methods section. As shown in the table, the resulting doping density from the EIS experiments closely match the doping density obtained from 4-point probe for the pristine wafers.

Using the calculated V_n and given the Si electron affinity (conduction band) of 4.05 eV, the Si Fermi level is about 4.32 eV. Given the average V_{fb} of ~ 0.63 eV, the effective Ir work function is 4.95 eV which is at the lower end of the work function range of 5-5.67 eV for Iridium.[24]

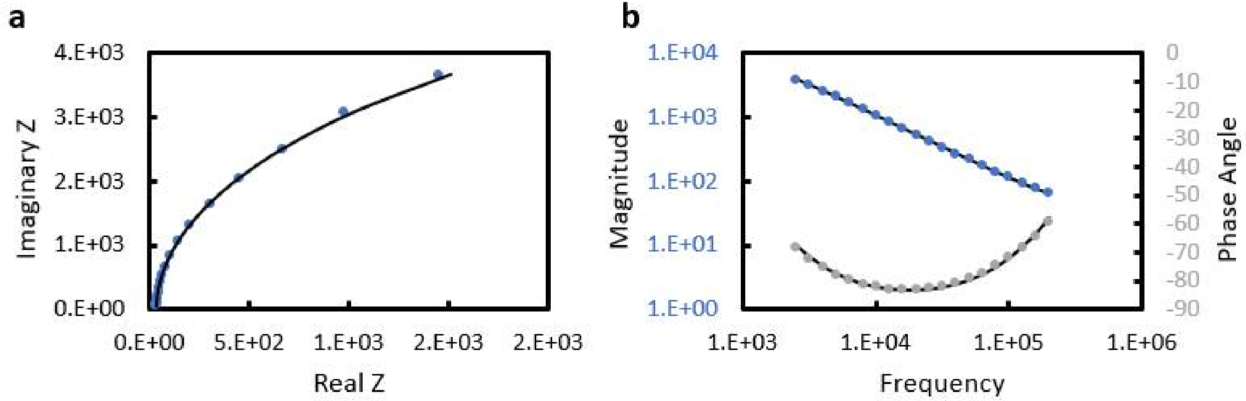

Figure S11: Representative Nyquist plot (a) and Bode plot (b) for the 3.5 nm-Ir/2.0 nm-HfO_2/n-Si sample at 0.3 V vs $Fe(CN)_6^{3-/4-}$ measured in the frequency range of 3000-200,000 Hz in 10/10 mM FFC. The data points are the experimental values, and the black lines are the corresponding fits using the equivalent circuit.

Table S1: Extracted data from the EIS experiments for each sample

Cycles	V_{fb} (eV)	ϕ_{ideal} (eV)	N_D from slope (cm^{-3})	V_n (eV)	N_D from probe (cm^{-3})
0	0.609	0.883	6.40E+14	0.274	6.39E+14
13	0.625	0.901	6.10E+14	0.276	
16	0.634	0.908	6.54E+14	0.274	
19	0.640	0.907	8.33E+14	0.267	
22	0.647	0.921	6.53E+14	0.274	
25	0.635	0.902	8.49E+14	0.274	
19 duplicate	0.628	0.895	8.35E+14	0.268	8.30E+14
19 high dope	0.728	0.920	1.54E+16	0.193	

The tunnel probability term $exp\left(-\propto d\sqrt{\phi_n}\right)$*:*

As discussed in the main paper, the tunnel probability term can be calculated after measuring the barrier height (Equation 3) and the reverse saturation current (Equation 2). The calculated values are shown in Figure S12. As expected, increasing insulator thickness exponentially decreases the tunnel probability term as the electron charge transfer is impeded. We note that the 0 nm HfO_2 sample has a tunnel probability below 1 because of the likely

formation of an adventitious SiO_2 layer. The lowest tunnel probability term for the 2.0 nm HfO_2 results in a ~ 500 fold reduction of electron recombination, which yields a 160 mV photovoltage improvement relative to the 0 nm HfO_2 sample. However, to achieve the 630 mV photovoltage limit governed by the flat-band potential, a tunnel probability term of 1e-4 (10,000 times reduction of electron recombination or 20 times better than the experimental value for 2.0 nm HfO_2) is required for an ideal system. Specifically, about 3 nm of HfO_2 would be required to achieve such a low tunnel current. The fundamental problem is that the hole tunneling current becomes the photovoltage-limiting factor for HfO_2 thickness > 2.0 nm, as previously described. Therefore, engineering a superior insulator material with a larger barrier for electrons (ϕ_n, reducing reverse saturation recombination current), and a smaller barrier for holes (ϕ_p, reducing the tunneling resistance losses) is necessary to achieving the photovoltage limits. This would enable a thicker insulator layer to lower the tunnel probability term while not hindering the hole transfer to the catalyst.

An additional way to improve the tunnel probability term is by focusing on $\propto$ and ϕ_n, which are not readily known for nanoscale HfO_2. The constant $\propto$ is given by the following equation:

$$\propto = \frac{4\pi}{h}\sqrt{2m_e^*} \quad (S17)$$

In literature, the effective mass of the electron (m_e^*) through the insulator is generally assumed to equal the mass of an electron, which results in the constant being equal to 1 and thus $\propto$ is often assumed to be insignificant. However, the effective mass of an electron in nanoscale HfO_2 (with small contributions from the thin interfacial SiO_2 layer) is unknown and may deviate significantly from the bulk value, so we combine $\propto$ with ϕ_n into one term. Using the average

HfO_2 thickness from TEM cross-sections, the combined term $\propto \sqrt{\phi_n}$ was calculated (Figure S12). The term increases with increasing HfO_2 thickness, which is desirable for minimizing the electron recombination tunnel current. This indicates that the tunnel properties of HfO_2 may change as a function of thickness as they approach the properties of bulk HfO_2. Depending on the actual value of $\propto$, the estimated range of ϕ_n is between ~ 0.1-1 eV, which is significantly lower than what might be achievable for HfO_2 on Si (~ 2 eV).[25] To achieve the 1e-4 tunnel probability term for 2 nm HfO_2, $\propto \sqrt{\phi_n}$ would have to equal about 0.46 which corresponds to a reasonable ϕ_n range of 0.22 – 1.9 eV. Therefore, engineering MIS systems with a 2 nm thick HfO_2 layer and a ϕ_n of 2 eV (close to bulk HfO_2 value) is feasible and could conceivably enable the system to achieve photovoltages approaching the 630 mV limit.

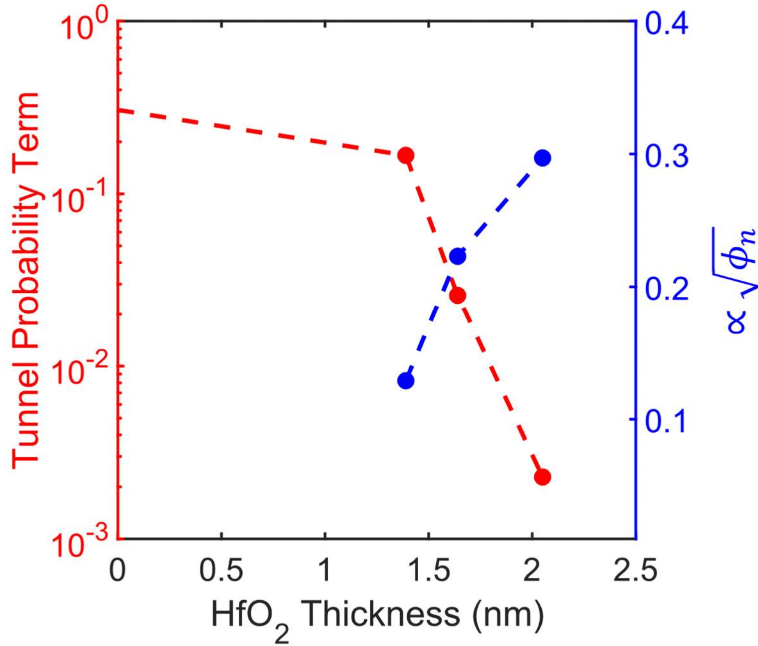

Figure S12: Tunnel probability term $\exp(-\propto d\sqrt{\phi_n})$ and combined term $\propto \sqrt{\phi_n}$ as a function of HfO_2 thickness.

Modeling current-voltage plots

To model the current voltage plots, Equations 1-4 from the main text are used to capture the light absorption and the photovoltage generated by the MIS junction. These equations are coupled to the Butler-Volmer equation which accounts for the electrochemical kinetics of the catalyst:

$$J_{cat} = J_{ocat}\left[\exp\left(\frac{z\beta F(V_{cat}-J_{cat}R_s)}{RT}\right)-\exp\left(\frac{-z\beta F(V_{cat}-J_{cat}R_s)}{RT}\right)\right] \quad (S18)$$

Where J_{cat} is the current through the metal electrocatalyst, J_{ocat} is the electrocatalyst exchange current density, z is the number of electrons in the electron transfer, β is the symmetry factor, F is Faraday's constant, and R_s is the series resistance. The current through the MIS junction and the catalyst are in series, so the overall current-voltage relationship of the system is calculated by:

$$J_{total} = J_{cat} = J_{MIS} \quad ; \quad V_{total} = V_{cat} + V_{MIS} \quad (S19)$$

where the total current, J_{total}, is equal to the current passing through the system as measured by the potentiostat. The total voltage, (V_{total}) is the summation of the voltage required by the electrocatalyst (V_{cat}) and generated by the MIS junction (V_{MIS}).

To model the CVs shown in Figure 3b of the main manuscript, first the p^+-Si control sample are fit to the Butler-Volmer Equation using J_{ocat} , z, and R_s as fitting parameters. Since the p^+-Si and n-Si samples have identical thicknesses of Ir catalyst, all samples are assumed to have the same catalytic activities. For the n-Si samples, the Butler-Volmer equation is then coupled to the MIS diode equations using the experimentally obtained values for J_{ph}, n, J_s,

$\phi_{b,ideal}$, and V_n. By varying the input current and measuring the corresponding voltages in series, the current-voltage characteristics can be modeled and compared to experiment. The model matches the experimental data very well, as shown in Figure 3b from the main text.

Improved photovoltage from annealing a 19 cycle (2 nm thick) HfO_2

Annealing is a promising strategy to improve the quality of the interfaces and remove non-idealities in MIS systems. As shown in figure 6 of the main text, removing these non-idealities can improve the generated photovoltage by up to 70 mV. To explore the benefits of annealing, we performed a 30 minute, 300°C forming gas (5 SCCM H_2 and 95 SCCM N_2) anneal on a 2.0 nm HfO_2 sample before depositing the Ir catalyst (i.e. a pre-metal deposition anneal). Annealing before the metal deposition prevents potentially detrimental reactions between the metal and the insulator, while modifying the semicondcutor/insulator interface. As shown by the CV data in figure 2a, the annealed sample exhibits a 30 mV higher photovoltage (indicated by the shift to the left) than the non-annealed control sample. Specifically, the photovoltage for the annealed sample increased to 510 mV, which is confirmed by the open-circuit voltage measurement in figure 13d. This increased photovoltage could be the result of fewer defects and better ideality factor or the result of an increased flat-band potential. As shown by the Mott Schottky plots in figure 2b, the flat-band potential (x-intercept) for both samples are identical. Therefore, the photovoltage increase is not due to an increased flat-band potential but is rather attributed to an improved ideality factor and more ideal interfaces.

The impact of annealing on the performance under OER conditions in 1 M KOH was also explored. As shown in Figure 13d, the onset potential (evaluated at a current density of 1 mA

cm^{-2}) of the annealed sample favorably shifted 80 mV compared to the non-annealed sample. A photovoltage of 510 mV is demonstrated in figure 13d, which is a 30 mV improvement over the non-annealed sample. The 30 mV photovoltage improvement can only partially explain the 80 mV shift in the onset potential. The remaining shift is due to improved catalytic activity, which may be the result of increased catalyst surface area from depositing on an annealed substrate. We note that this additional shift was not observed in FFC because a shift in FFC is governed entirely by the generated photovoltage, and not by the kinetics of the facile FFC reaction.

While a 30 mV photovoltage increase from annealing is a significant improvement, an additional 40 mV increase is possible according to data in figure 6 of the main paper. Thus, even further increases in photovoltage can be obtained by further optimizing the annealing temperature, duration, and ambient gas.

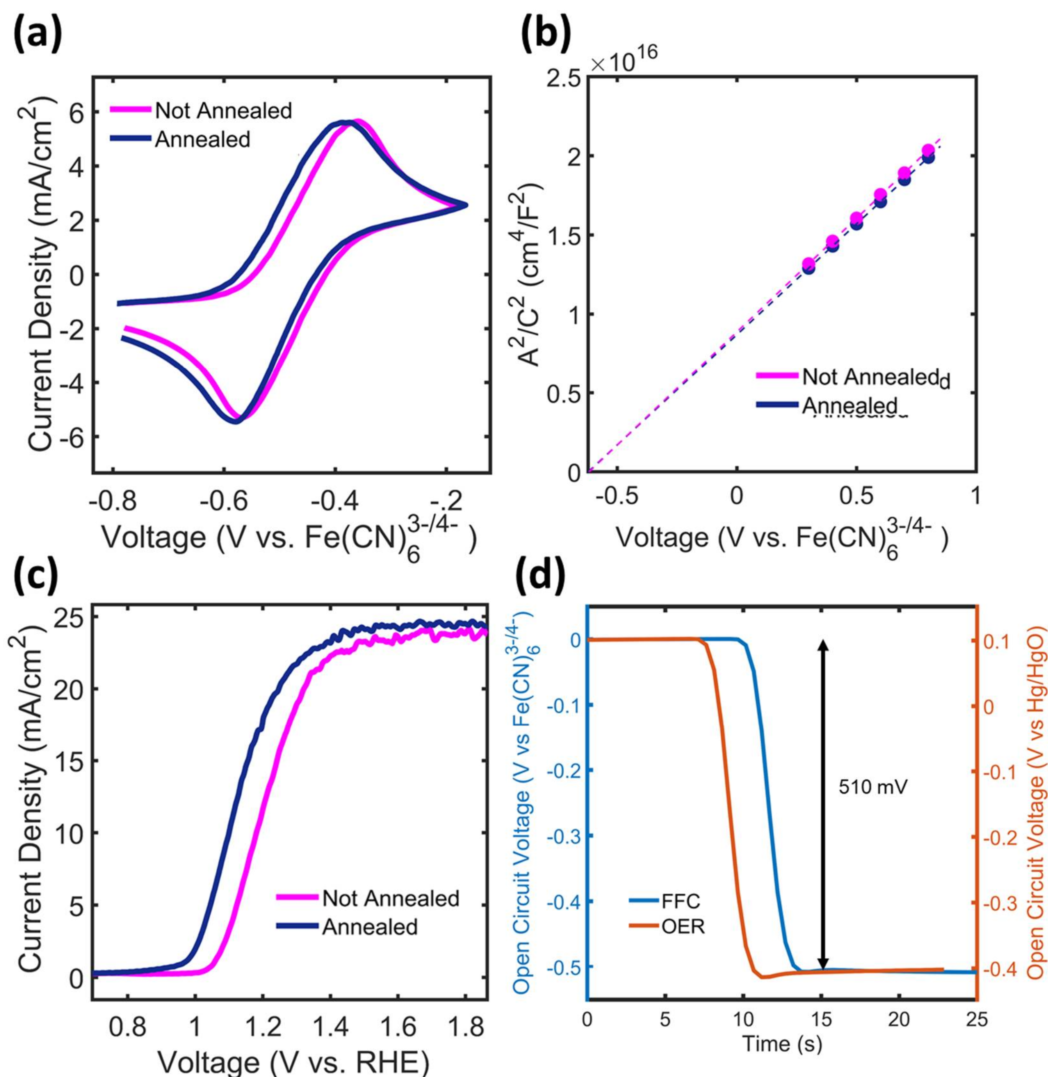

Figure S13: Comparing the effects of annealing a 3.5 nm Ir/2.0 nm HfO_2/n-Si sample. (a) Current voltage plot in ferri/ferrocyanide redox solution showing an 30 mV increase in photovoltage upon annealing, and (b) Mott Schottky plot showing that both systems have identical flat-band potentials. (c) LSV plot under OER conditions in 1 M KOH showing an 80 mV shift in the onset potential upon annealing. (d) open-circuit voltage measurements under dark and light conditions for annealed samples in either FFC or KOH electrolyte. Both samples result in 510 mV photovoltage, demonstrating that a 30 mV photovoltage improvement upon annealing is obtained in both electrolytes.

Comparing 2 nm thick HfO_2 on higher vs lower doped n-Si

Higher doped Si is necessary to increase the flat-band potential and enable higher maximum theoretical photovoltages (see Equation S15 and Figure 6). To explore the impact of using higher doped Si, we have synthesized a 19 cycle HfO_2 sample on a higher doped wafers (0.1-1 ohm-cm resistivity) compared to the lower doped wafers (5-8 ohm-cm resistivity). Both the higher doped and lower doped wafers were processed in parallel under identical conditions. The CVs and the compiled results from EIS and light intensity experiments are shown in Figure S13. The flat-band potential is significantly larger for the higher doped Si due to the shift in the Si Fermi-level. Despite the improved flat-band potential, the photovoltage is actually lower than the lower doped sample. This is because the ideality factor for the higher doped sample is very unfavorable. The high ideality factor is probably a combination of an insulator voltage drop through surface states, and field emission causing deviation from thermionic emission. While the higher doped samples have a higher theoretical photovoltage due to the high flat-band potential, the photovoltage is severely limited by the non-idealities. Given the large flat-band potential and theoretically achievable photovoltage, overcoming these non-idealities is important to achieve systems with greater than 600 mV photovolage. As demonstrated in figure 13, annealing is a promosing strategy to remove non-idealities and optimize the photovoltage.

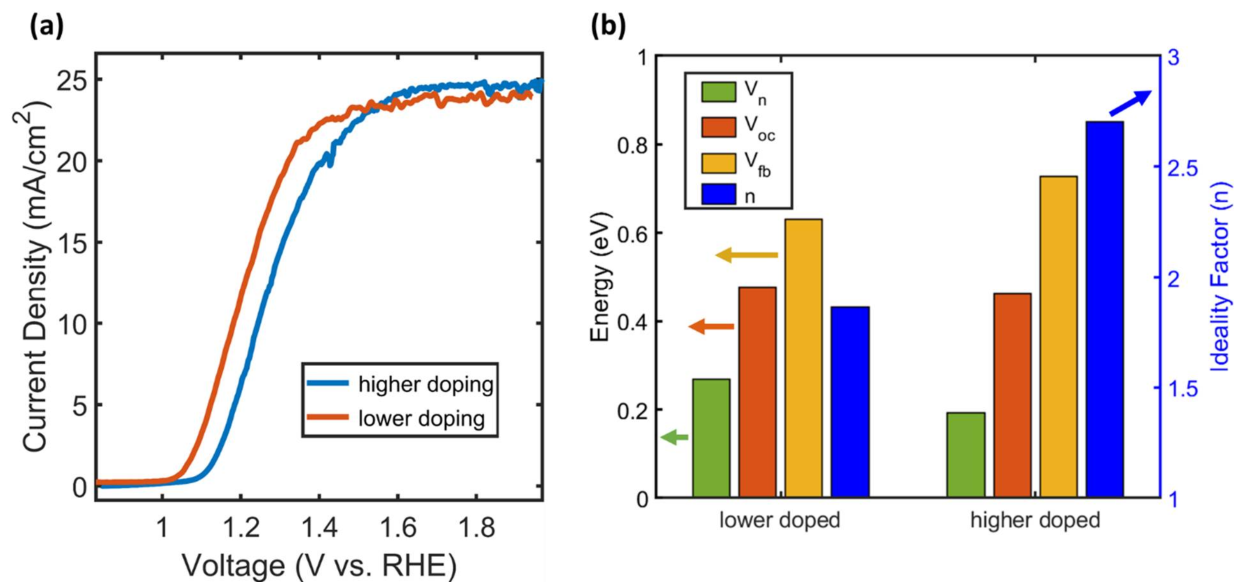

Figure S14: (a) CV in 1 м KOH comparing 3.5nm-Ir/2.0 nm-HfO_2 samples prepared identically, but on Si with different doping levels. (b) Compiled doping density, open-circuit photovoltage, flat-band potential, and ideality factor from EIS and light intensity experiments.

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