# Bidirectional Wireless Telemetry for High Channel Count Optogenetic Microsystems

by

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## DEDICATION

To my dear family for their unconditional support throughout the years.

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## ABSTRACT

In the past few decades, there has been a significant progress in the development of wireless data transmission systems, from high data rate to ultra-low power applications, and from G-b per second to RFID systems. One specific area, in particular, is in wireless data transmission for implantable bio-medical applications. To understand how brain functions, neural scientists are in pursuit of high-channel count, high-density recordings for freely moving animals; yet wire tethering issue has put the mission on pause. Wireless data transmission can address this tethering problem, but there are still many challenges to be conquered.

In this work, an ultra-low power ultra-wide band (UWB) transmitter with feedforward pulse generation scheme is proposed to resolve the long-existing problem in UWB transmitter. It provides a high-data rate capability to enable 1000 channels in broadband neural recording, assuming 10-bit resolution with a sampling rate of 20 kHz to accommodate both action potential (AP) and local field potential (LFP) recording, while remaining in ultra- low power consumption at 4.32 pJ/b. For the bi-directional communication between the wireless and recording/ stimulating module, a bit-wise time-division (B-TDD) duplex transceiver without cancellation scheme is presented. The receiver works at U-NII band (5.2GHz) and shares the same antenna with UWB transmitter. This significantly reduces the area consumption as well as power consumption for implantable systems. The system can support uplink at 200 Mbps for

1000 recording channels and downlink at 10 Mbps for 36 stimulation channels. With a 3.7 Volt 25mAh rechargeable battery, the system should be able to operate more than 1.5 hours straight for both recording and stimulation, assuming 1 LED channel with 100 µA, 10% duty-cycled stimulating current.

The B-TDD transceiver is integrated with a dedicated recording/ stimulation optogenetic IC chip to demonstrate as a complete wireless system for implantable broadband optogenetic neural modulation and recording. The fully integrated system is less than 5 gram, which is suitable for rodent experiments.

# CHAPTER 1
# Introduction

## 1.1 Motivation

"*A typical neuron makes about ten thousand connections to neighboring neurons. Given the billions of neurons, this means there are as many connections in a single cubic centimeter of brain tissue as there are stars in the Milky Way galaxy*." [1]

This quote, by the neuroscientist David Eagleman, describes the immensity within the pursuit of discovering the mystery of brain function which has been a persistent goal for scientists and engineers. Since the first successful recording of *in-vitro* action potential conducted by Adrian in 1920s [2], there have been numerous efforts contributed in this area, especially in the past few decades. In 2015, efforts reached to more than 1,000 channels of parallel broadband recording [3]. The speed of growing has roughly doubled the channel count every 7.4 years, which is approximately aligned with Moore's Law [4]. As the development of neural interface progresses, the increase of channel counts provides more information and data for neuroscientists to analyze, moreover, it also motivates innovation - the desire to record the neural signal while the test subject is moving freely; a task sounding seemly simple, but requiring complex and intricate technical difficulties to overcome. With over a 1,000 channel recordings, the wire connection cannot be handled. The tangling issue also prohibits a completely free moving

experiment session, alongside the bulkiness and discomfort, preventing the experiments to be carried out with human subjects. If it is nearly impossible with wires, wireless is then the necessary and practical path to pursue.

In 1957, the first biomedical wireless telemetry device by Mackay was published. It described a swallowable RF telemetry sending out the temperature and pressure information within gastro-intestinal (GI) tract [5, 6]. Since then, numerous works have been published to address more low- power, higher data rate systems for biomedical application, especially regarding neural implants which will be described further in the next section.

### 1.2 Wireless data telemetry for neural implants application

As mentioned in the previous section, the first RF telemetry for biomedical use was published in 1957 by Mackay. The structure was quite simple, it consists of a BJT, a tapped coil as a Hartley oscillator, two capacitors and a 1.5 volt battery as shown in [5]. The transistor generates two frequencies and acts as a thermometer. The pressure modulation result from motion of the powdered iron near the coil [5].

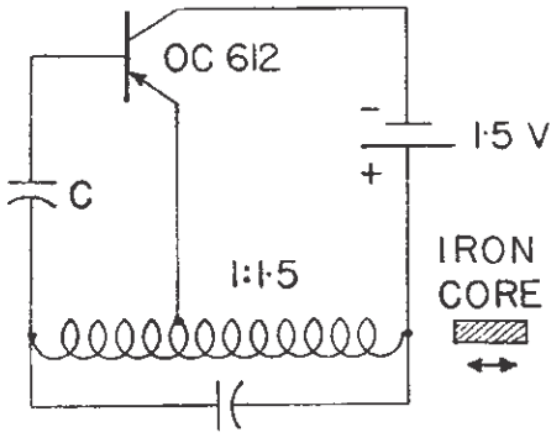


Figure 1-1 First RF transmitter used in biomedical application

Although the structure is simple, the use of coil makes it impossible for neural implants. In 2004, Garris *et al*. proposed to have a backpack structure for wireless transmission of fast-scan cyclin voltammetry (FSCV) with a Commercial Off-The-Shelf (COTS) Bluetooth telemetry for data transmission[7]. In 2006, Harrison *et al*. in University of Utah put wireless data telemetry together with 100- electrode neural recording system to realize a full system integration which pushed the neural interface to the next level[8]. Figure 1-2 shows the complete assembly of the integrated neural interface and the system block diagram is shown in Figure 1-3. This system incorporated Utah Microelectrode Array (UEA) with an ASIC fabricated in CMOS process. It consists of a 10x10 array of amplifiers, a 9-b ADC and a FSK transmitter centered at 433 MHz. The transmitter is based on a LC-tank VCO which transmits at the data rate of 330 kbps and can be retrieved at the distance of 13 cm with a receiver with -86 dBm sensitivity.

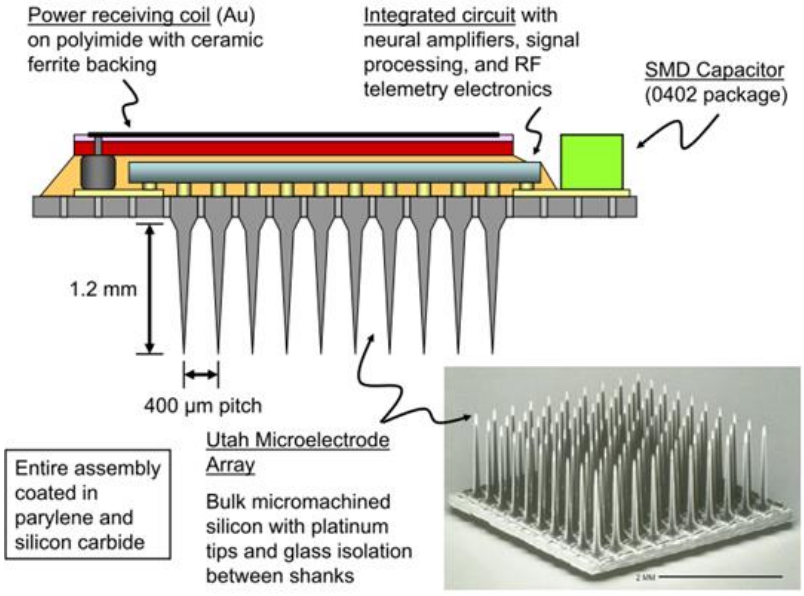



Figure 1-2 Complete integrated neural interface systems [9]

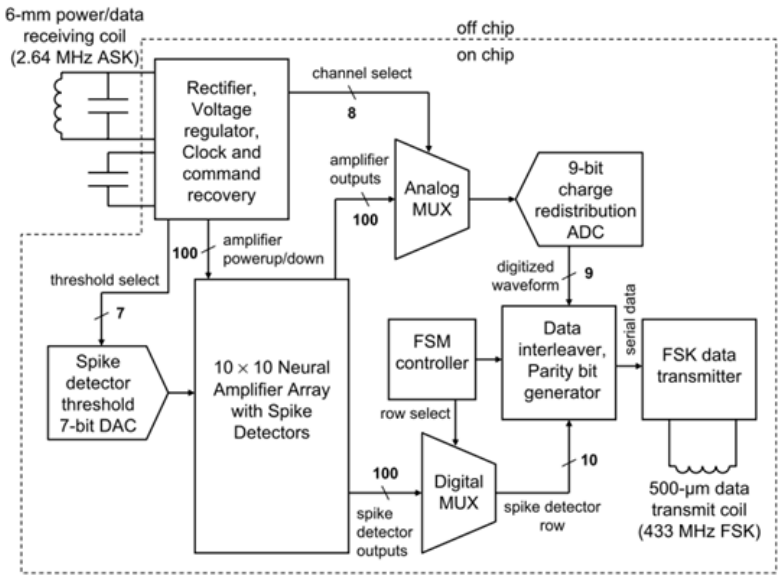
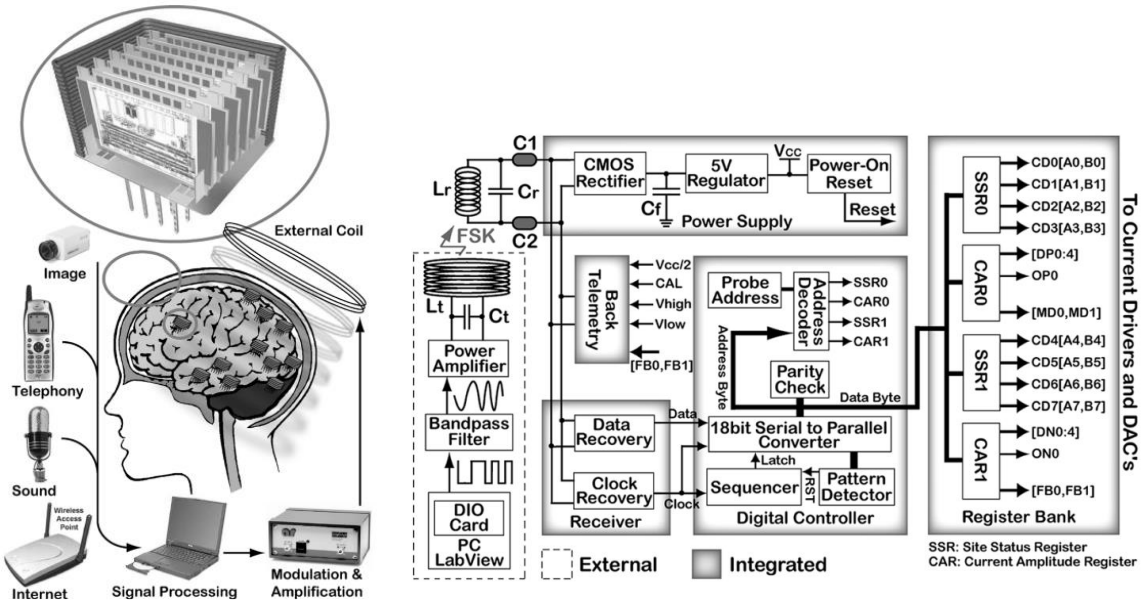



Figure 1-3 System diagram of neural interface [9]

Around the same time, Ghovanloo *et al*. in University of Michigan approached the data transmission differently. As shown in Figure 1-4(a), inductive coupling method was adopted for both data and power delivery.[10]. This system was designed for cortex stimulation which helps to alleviate disorders such as blindness, deafness and severe epilepsy. Figure 1-4(b) shows the integrated Interstim- 2B in a modular fashion. Each module contains eight current drivers, which provide the stimulating current up to ±270 μA with 5b resolution. 64 modules can be used in parallel to drive at most 2048 sites. The inductive –capacitive (LC) tank works as a power receiver at 8.25 mW/module, and also as a data transmitter with a data rate of 2.5 Mbps. Frequency shift keying (FSK) modulation at the frequency of 5/10 MHz is adopted for the data transmission. The transmission distance is 5 mm due to the limitation of inductive coupling.




(a) (b)

Figure 1-4 (a) Multipurpose button-sized wireless microstimulating 3-D array, (b) block diagram of the microsystem in [11]

Since then, data transmissions for implantable applications have been divided into two mainstreams: near and far-field. As mentioned above, inductive coupling is in near-field, while the works in MICS/ ISM band are classified as far- field. Inductive coupling, even though it has the benefit of high conversion efficiency in power and low loss for data transmission according to the Friis law[12], the size of the coil and the transmission distance are the main obstacles prior to fully applicable implantable neural interface. Therefore, we will focus on far-field data transmission throughout this thesis.

Medical Implant Communication Service (MICS) band was formulated in 1999 by U.S. Federal Communications Commission (FCC) under the request of a dedicated band for implanted mobile radio device to transmit data in support of diagnostic and therapeutic function[13]. It set aside the frequency band from 402-405 MHz as well as 2360- 2400 MHz with the maximum Effective Isotropic Radiated Power (EIRP) of 25

microwatt to avoid the risk of interfering with other users in the overlapping bands; including, MetAids, Earth exploration satellites, and meteorological satellites[14]. Serving as a similar purpose, but only much more, Industrial, Scientific and Medical (ISM) band was established in 1985 by FCC due to the rapid growth in low- power, short-range RF radio communication applications. Most commonly-used bands in ISM for medical devices are the 433 MHz, 902-928 MHz, 2.4 GHz and 5 GHz band, with the maximum EIRP of 1 watt.

Works in ISM/ MICS bands have developed rapidly since 2006 due to the predominance in both regulation and the maturity of the transceiver structure. Bradley reported a MICS/ISM band transceiver for implantable medical applications with 2 meter transmission distance. It was equipped with an on-chip wake-up receiver, allowing the system to consume less than 0.9 μW in sleep mode while consuming 5 mW in full operation[15]. While 5 mW is still too power hungry in implantable applications, researchers were then on the mission to further reduce power consumption. In 2009, Bohorquez *et al*. reported a transceiver work in MICS band that adopted super-regenerative receiver (SRR) and further reduced the power consumption by reusing digital controlled oscillator (DCO) from the transmitter [9]. The system consumes less than 1 mW, with receiver sensitivity better than – 93 dBm at the data rate of 120kbps. Same year, Bae *et al*. proposed a MICS compatible FSK transceiver for implantable devices[11]. This work reduced power consumption by lowering the voltage supply from the nominal 1.8 volt for 0.18 μm CMOS process to 0.7 volt, resulting in the power consumption of the whole transceiver to be right under 500 μW at the data rate of 250 kbps. While reducing power supply was an effective way to reduce power, Rai *et al*.

realized that they had to attack where it hurt the most, in other words, the most power hungry block – carrier generator[16]. In this work, instead of voltage- controlled oscillator (VCO) or DCO, they adopted edge combiner structure. The edge combiner overlaps the rising and falling edges of the delay cell and output the combined pulses, as shown in Figure 1-5. This way, instead of generating 403/ 433 MHz output, the delay cell is driven by a reference input at 44.5 MHz which successfully reduces the power consumption by lowering the operating frequency to 1/18.

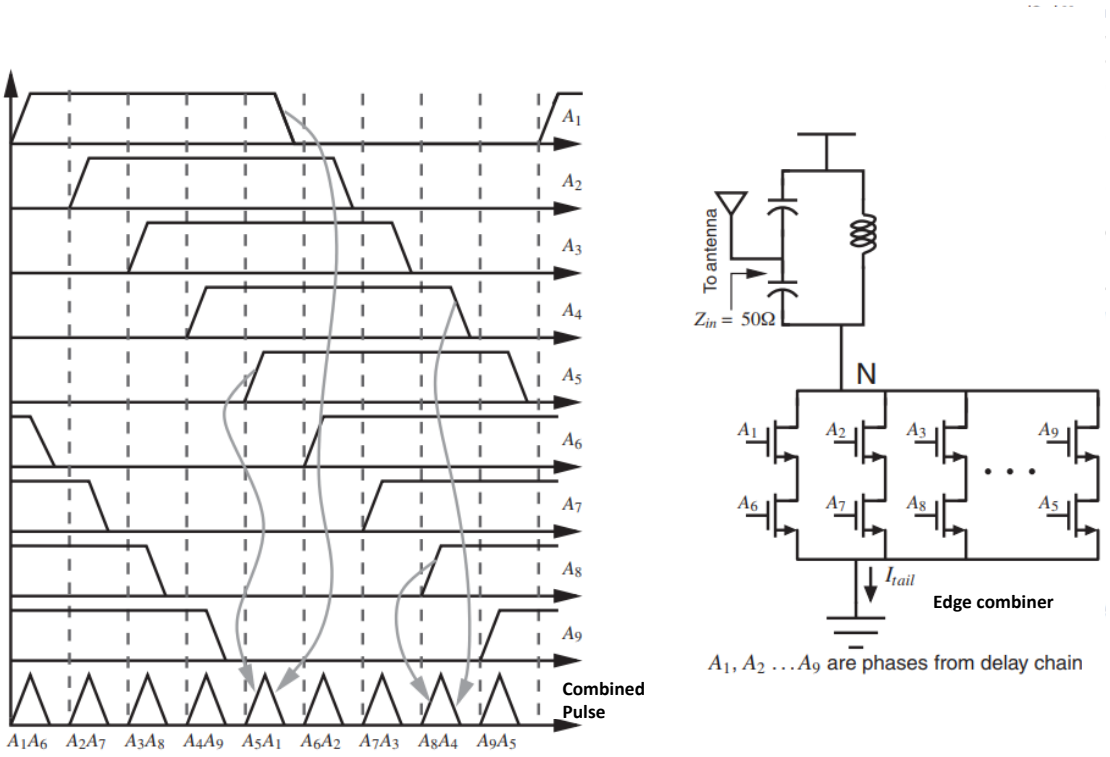



Figure 1-5 Transmitter edge combiner schematic details of [15]

While 403/ 433 MHz transceiver structure was popular, it suffered from a few drawbacks. First, due to the band limitation, it cannot support a higher data rate transmission. As the number of channel increases, the data rate can easily reach more than 10 Mbps. Also, the size of antenna restricted its usage in implantable applications. In

2011, Vidojkoriv *et al*. moved the operating frequency to 2.4 GHz [17]. As shown in Figure 1-6, two 2.4 GHz LC tank VCOs were implemented for carrier generation and core oscillator for transmitter and receiver respectively. This work achieved low power consumption of 1 mW with the data rate at 10 Mbps for transmitter, while receiver consumed 0.5 mW at the data rate of 5 Mbps with sensitivity of -75 dBm.

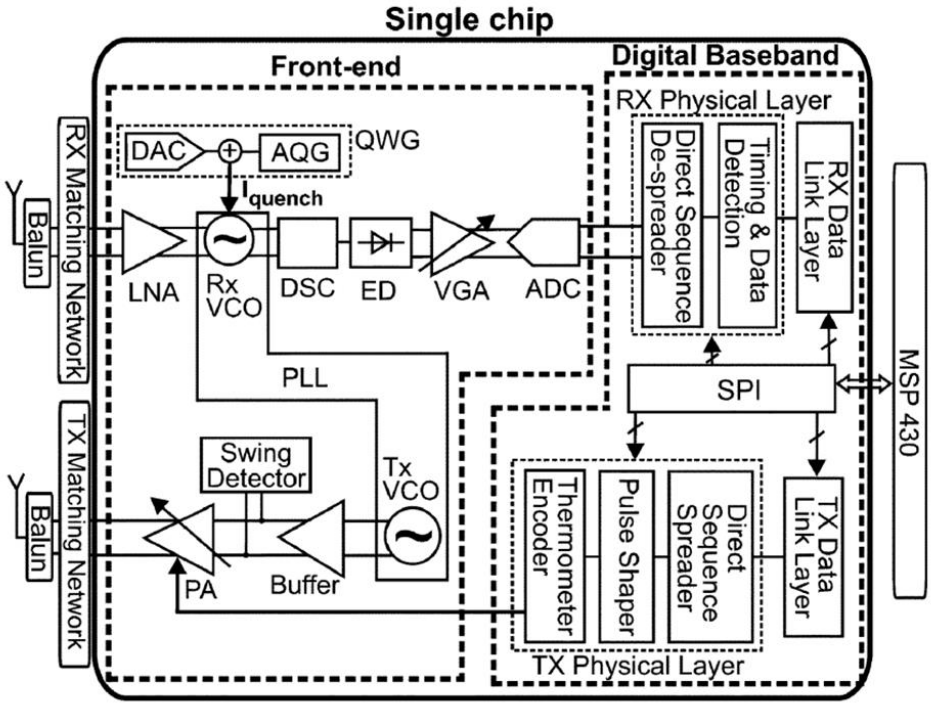



Figure 1-6 Block diagram of 2.4 GHz transceiver

As high data rate was provided in [17], its complexity also became a burden to reduce power consumption. If we look at the neural interface structure more closely, we can immediately observe that the requirement of data rate in the transmitter and receiver are distinctively different. For recording channels, the data rate can easily exceed 30 Mbps assuming it is sampled at 30 kHz, 10 bit resolution with 100 channels, thus the high data rate for transmitter. At the same time, simple command transmissions to change the

setting of the system does not require high data rate, and further reduce the burden of the receiver. Under this logic, Tan *et al*. proposed an asymmetric structure for single- chip wireless neural recording IC in 2014. This work employed binary phase-shift-keying (BPSK) modulation with the transmitting data rate up to 8 Mbps, while the downlink's data rate is at 100 kbps with OOK modulation to save power. The uplink data rate allows 8 recording channels to work simultaneously and achieves the transmitting distance of more than 10 meters[18].

Nevertheless, to achieve even higher date rate to enable more than 100- channel simultaneous recording while maintaining low power consumption, ISM/ MICS band structures start to show feebleness. Continuous- time, or in other words, narrow band transmission has a few fetal drawbacks. Firstly, the high frequency carrier needs to be generated continuously. With the operating frequency at 2.4 GHz, the power consumption of VCO/ DCO and phase-locked loop (PLL) cannot be easily ignored. Also, due to the narrow band criteria, the data rate is also confined. To compensate for the shortcomings mentioned above, a wide-band, pulsed-carrier transmission method is developed, which is known as Ultra- Wide Band (UWB) communications.

### 1.3 UWB Communications

Ultra- wide band concept often considered being developed in 1960 with the development of Linear Time Invariant System description via impulse stimuli, but in fact, the history goes way back to the $19^{th}$ century. Exactly in 1886, Hertz realized that by employing two spark gap generators, each one equipped with antenna and separated by a certain distance, a gap will be created in one generator (receiver) while the other one (transmitter) produces a spark. However, the wireless transceiver concept was not further

developed until 1894 by a young Italian boy, Guglielmo Marconi. Marconi was astonished by Hertz's discovery and soon became obsessed with the possibility of wireless transmission. In 1895, he built his first transmitter as shown in Figure 1-7. As it can be seen in the figure, the antenna was made by a metal plate and the efficiency is very low. With this setup, he was able to transmit signal in the range of hundreds of meter.

Figure 1-7 Marconi's first transmitter

In 1896, after having a meeting with Sir William Preece, one of the most influential people in the field of communication and also, the chief telegraph engineer in Britain, Marconi set up a rooftop link with spark gap transmitters for communication between two stations, separated by one mile in distance in just two weeks' time. Here, the world's first UWB operating radio link was up and running in the June of 1896 [19].

### 1.3.1 Definition and characteristics of UWB signal

The basic principle of UWB communication is by transmitting very short pulse(s) to achieve very low power consumption. In 2002, FCC officially released the criteria and allocation for UWB applications in commercial use [20]. In the regulation, FCC approved the band from 3.1 to 10.6 GHz for UWB communication. The spectrum density is restricted to be -41.3 dBm/MHz within the band, as shown in Figure 1-8 and tabulated in Table 1-1 so the emitting signal does not interfere with existing bands like GPS which operates at 1.2 and 1.6 GHz and personal communication service (PCS) at 1.9 GHz.

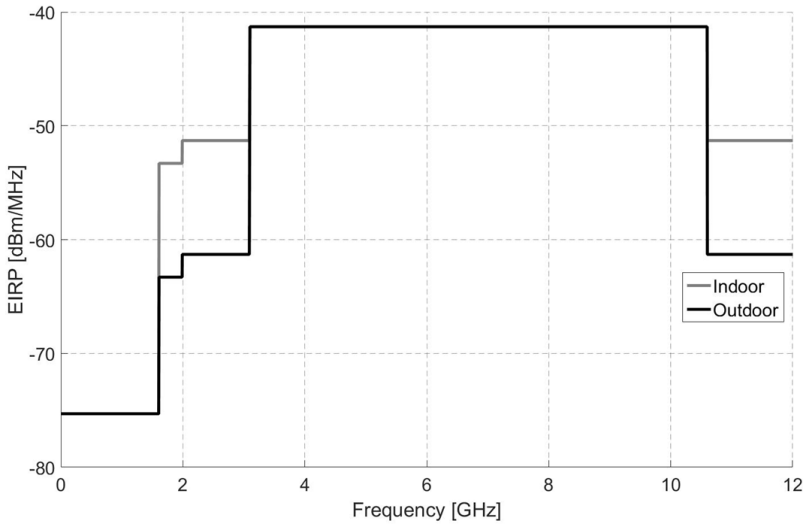



Figure 1-8 FCC EIRP limit for in/outdoor UWB communication

The UWB occupies the bandwidth at least 500MHz or a fractional bandwidth of larger than 0.2, i.e.

$$BW > 500MHz, \text{ or} \tag{1-1}$$

$$B_f = \frac{BW}{f_c} = \frac{(f_H - f_L)}{(f_H + f_L)/2} \geq 0.2 \tag{1-2}$$

, where $BW$ is the bandwidth, $B_f$ is defined as the ratio of the signal bandwidth to the center frequency $f_c$, $f_H$ and $f_L$ are the highest and lowest transmitting frequency within the band, respectively. With UWB's large bandwidth, it can accommodate a much higher data rate than previously mentioned continuous- time transmission, according to Shannon's capacity formula[21]. Compare to other popular wireless communication standards like 802.11a, 802.11b and Bluetooth, UWB has a better performance in spatial capacity and the difference is in the order of magnitudes, as shown in Figure 1-9 [22].

Table 1-1 FCC mask limit

| Frequency Range [23] | Indoor Limit [dBm/MHz] | Outdoor Limit [dBm/ MHz] |
|---|---|---|
| Below 960 | FCC 15.209 | |
| 960-1610 | -75.3 | -75.3 |
| 1610-1990 | -53.3 | -63.3 |
| 1990-3100 | -51.3 | -61.3 |
| 3100-10600 | -41.3 | -41.3 |
| Above 10600 | -51.3 | -61.3 |

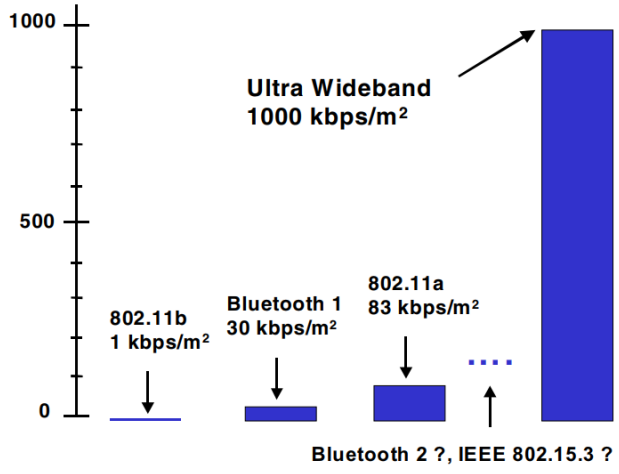



Figure 1-9 Spatial capacity comparison between IEEE 802.11, Bluetooth and UWB [22]

The advantages UWB has over traditional narrow band architectures are not constrained in possessing large bandwidth. Narrow pulse width generation is not only power saving, also providing location information combined with communication [24].

### 1.3.2 Previous works in UWB

In 2009, Tang *et al*. reported a UWB transmitter for low-power high-speed wireless implantable biosensors [25]. The transmitter is equipped with a pulse generator which consists of a voltage-controlled ring oscillator (VCRO) and a buffer. The pulse generator is able to produce pulses with 1 ns width and the pulse repetition rate can be varied from 90 to 270 MHz. The system consumes 21 mW with transmission distance of 4 meters at the data rate of 14Mbps, leading to 1.5 nJ/bit efficiency with the center frequency at 960 MHz. Another work reported by Gao *et al*. was designed for medical sensor applications[26]. The system includes fully integrated transceiver and achieved the power efficiency at 0.35nJ/b for transmitter, 6.2 nJ/b for receiver at a data rate of 10 Mbps. The highly duty-cycled pulse generator contributes the most of the power saving.

The works mentioned above have shared one thing common, which is the method of pulse generation. Similar to continuous- time structures, oscillator structures were implemented for carrier generation. While it is doable in MICS/ ISM bands, generating a 3-5 GHz carrier is undoubtedly very power hungry. In [26], a controllable pulse width generator was implemented to drive the VCO current source for carrier generation. Even though it has the benefit of power saving since it only consumes power while generating pulses, the start-up time for oscillator and driving amplifier cannot be easily ignored. To tackle this problem, carrier- less pulse generator starts to show its potential, and it is known as impulse radio UWB (IR-UWB). There are many advantages of IR-UWB. First,

since it is carrier- less, local oscillators (LO), PLL nor synthesizer is no longer needed, which is a huge power- saving factor. Also, the short pulse generation is highly duty-cycled without having to worry about start-up time, further more power saving is now achievable [27].

Xia *et al*. reported a carrier-less UWB transceiver in 0.13 μm CMOS. In this work, a monolithic 3-5 GHz IR-UWB transceiver is presented that integrates both amplitude and spectrum tenability, thereby providing adaptable spectral characteristics for different data rate transmission[28]. The receiver adopts noncoherent structure which eliminates the need for conventional sample- and- hold structure. The pulse generator in transmitter is composed of digital circuits, including inverter and nand/ nor gates. It combines the edges of rectangular and its inverted self to form a very short duration pulse [28]. This pulse will then be further amplified and sent out for transmission. This work achieves 22 pJ/b and 0.13nJ/b efficiency for transmitter and receiver, respectively, at a data rate of 100 Mbps.

While IR-UWB structure is popular, it has its own issues. In UWB, pulses are sent at a regular repetition rate, and it leads to peaks in the spectrum of the transmitting signal. These peaks are referred to “spectral lines” or “comb lines”, which is undesirable since it limits the maximum transmittable power of UWB. Wentzloff *et al*. reported a delay-based binary phase-shift keying (DB-BPSK) work that by combining BPSK signal, which does not contain the spectral lines, with spectral lines embedded PPM to smooth out the spectrum[29]. This work reduced the spectral lines by 10 dB which allows the maximum emitting power to increase without violating FCC compliance. This work was fabricated

in 90nm CMOS, and achieved pulse repetition frequency (PRF) from 10 k to 16.7 MHz with efficiency from 43 pJ/pulse to 9.6 nJ/pulse.

Another issue with UWB is the transmission distance, to be more specific, the transmission distance at high data rate applications. While UWB needs to follow the stringent FCC rule, the maximum allowable emitting power decreases as the data rate increases. In order to tackle this problem, Geng *et al*. reported a work that allows 500 Mbps data transmission while the spectrum is still under the FCC mask. In this work, frequency hopping (FH) technique is adopted to spread out the energy over high-band UWB (7.25 – 9.5 GHz). The center frequency hops from one to another at the rate of 50 MHz with the distance of 250 MHz, having the duration of the FH bust with the timing margin of 20 ns [30]. This technique improves the link margin by 9 dB with their measurement result. It achieves the communication of 1.2 meters with the efficiency at 26.6 pJ/b.

In short, UWB communication is by far the ultimate method for implantable neural interface applications due to its advantages of low power, high data rate and comparably simpler implementation over traditional continuous- time transceiver structures. Table 1-2 shows the performance comparison for aforementioned state-of-the-art works in different implementation, and UWB structures are showing its leading position.

Table 1-2 Performance comparison of biomedical wireless transceivers

| | | [31] | [32] | [18] | [23]*1 | [33] | [30] | [34] | [35] |
|---|---|---|---|---|---|---|---|---|---|
| Operating band | | ISM | ISM | ISM | MICS | MICS | UWB | UWB/ISM | UWB/ISM |
| Frequency(GHz) | | 2.4 | 2.4 | 2.4 | 400 | 0.4 | 7.25-9.5 | 3.99 | 4/2.4 |
| Modulation | | GFSK | OOK | BPSK/OOK | QPSK | DBPSK | OOK | OOK | OOK/BPSK |
| TX | Output power(dBm) | 0 | N/A | 0.2 | -15 | -15 | -14.3 | -28.9 | -16 |
| | Data rate(Mbps) | 2 | 1 | 1/5/8 | 8 | 0.01-4.5 | 500 | 0.187 | 500 |
| | Power (mW) | 33.9 | 2.37 | 3.66 | 5.6 | 2.27 | 6.9 | 0.00418 | 5.4 |
| | FoM (pJ/b) | 16900 | 2370 | 3700/730/460 | 700 | 504 | 13.8 | 22.29 | 10.8 |
| RX | Sensitivity(dBm) | -82 | -82 | -84.5 | N/A | -100 | -59 | N/A | N/A |
| | Data rate(Mbps) | 2 | 1 | 5 | | 0.01-4.5 | 500 | 0.0078 | 100 |
| | Power(mW) | 40.5 | 0.93 | 10.2 | | 2.19 | 5.9 | 0.0001 | 5 |
| | FoM(nJ/b) | 20.25 | 0.93 | 2.04 | | 0.49 | 0.012 | 0.16 | 0.05 |
| Transmission distance(m) | | N/A | N/A | >10 | | N/A | 1.2 | N/A | N/A |
| Process node(nm) | | N/A | 90 | 130 | 65 | 40 | 65 | 130 | 180 |
| Area($mm^2$) | | N/A | 1.81 | 2.59x2.09 | 1 | 1.7x1.8 | 1.5x1.5 | 13.49*2 | 0.475 |

*1 Transmitter structure only *2 Area includes AFE

## 1.4 Thesis outline

### 1.4.1 Chapter 2: Edge combiner- based ultra-low power UWB transmitter

This chapter present an ultra-low power, ultra-wide band (UWB) transmitter in standard 65nm CMOS processes. The transmitter consists of feedforward edge combiners and interpolators for ultra-low power operation and reliable pulse generation that is essential in UWB transmitters. The implemented circuit avoids pulse-overlapping without complicated calibrations, and has achieved an energy efficiency of 4.32 pJ/b at 200 Mbps data rate. The transmitter is suitable for energy-constraint, high data rate applications such as wireless telemetry in implantable high-density neural recording interfaces.

### 1.4.2 Chapter 3: Bit- wise time division duplex cancellation- free transceiver

This chapter covers the architecture and circuit implementation of the implemented full duplex transceiver without cancellation scheme. This transceiver is able to transmit at

200 Mbps while receiving at 10 Mbps which is suitable for high channel count neural signal recording and stimulation.

### 1.4.3 Chapter 4: System integration of wireless data transmission with optogenetic neural modulator and recording

This chapter presents the integration of the aforementioned bit-wise time division duplex transceiver with existing 32- channel neural recording and 16- channels stimulation chip. It shows the feasibility of full communication and *in-vivo* test results are shown for system validation.

### 1.4.4 Chapter 5: Summary and future works

This last chapter summarizes this thesis by pointing out the important results and suggests a possible future work to improve the works this thesis includes.

# CHAPTER 2
# 4.32-pJ/b, Overlap-Free, Feedforward Edge-Combiner-Based Ultra-Wideband Transmitter for High-Channel-Count Neural Recording

Ultra-wideband (UWB) technology has drawn extensive attention for short distance, high data rate, and ultra-low power applications. One of the most challenging applications is high density neural interface systems where simultaneous recording and real-time stimulation are essential [36]. It requires 20 Mbps data transmission speed for 1,000-channel electrocorticography (ECoG) recording arrays and easily exceeds 200 Mbps for broadband neural recordings with the same channel count1. Thanks to highly duty-cycled operation, UWB systems can accommodate such high data rates while maintaining ultra-low power consumption, making it a unique candidate for wireless data transmission of high-density neural interfaces.

## 2.1 Pulse generation

Several pulse generation schemes are found in literatures such as oscillator-based, delay line-based and edge-combiner based. Oscillator-based scheme is the most straightforward solution when a carrier is needed. As it is widely used in continuous wave transmission, however, it does not have the benefit of low power in comparison to other method mentioned above. To achieve ultra-low power consumption, we adopted the edge combiner-based pulse generation instead of power-hungry oscillator-based

approaches [37, 38]. One of challenges that need to be addressed in conventional edge-combiner architectures is to minimize the variation of individual delay cells. Significant variations between delay stages can result in inconsistent pulse duty cycles and frequency shifting [39].

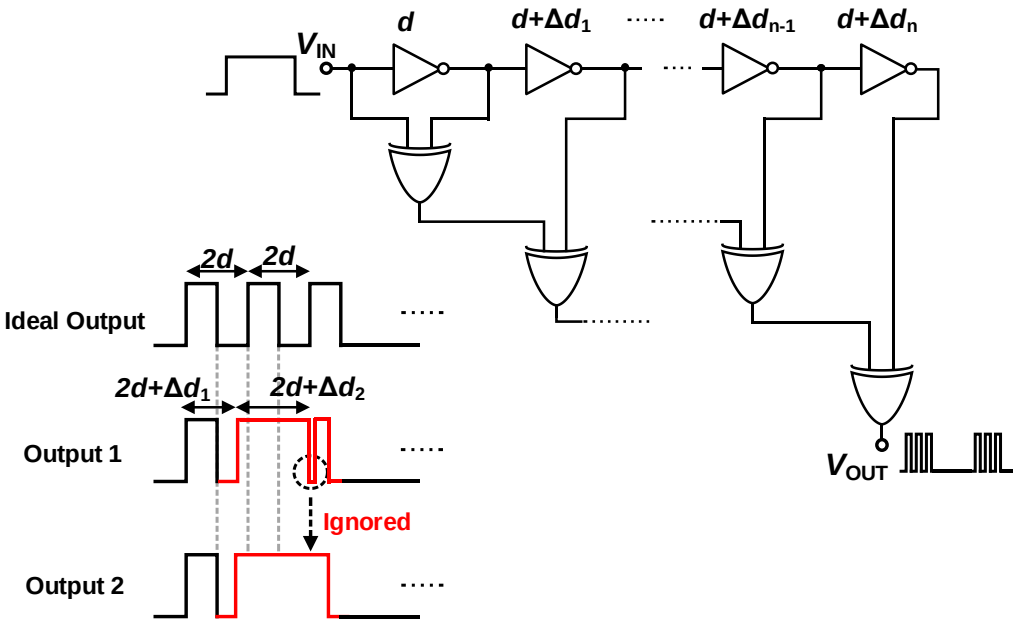
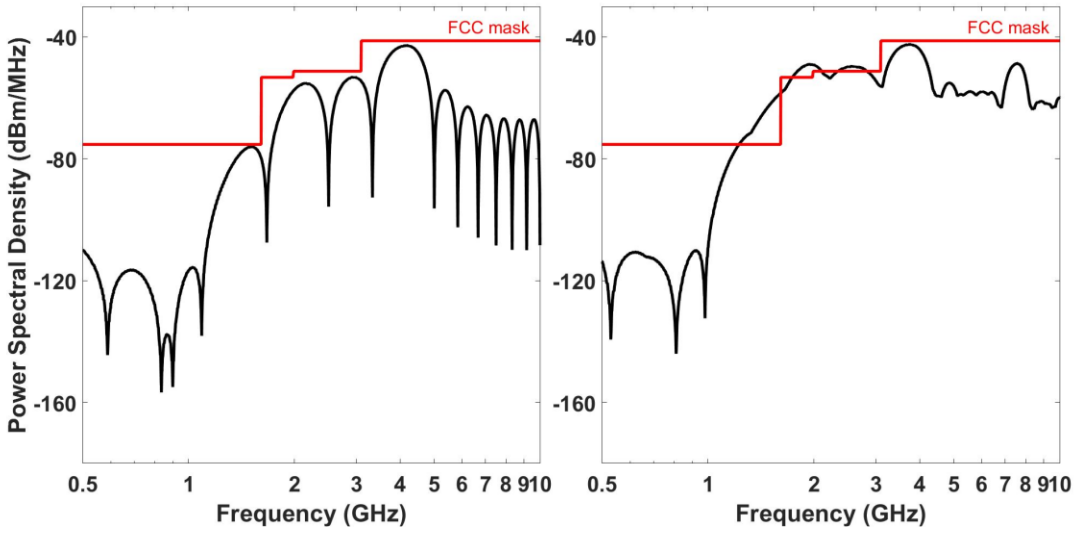



Figure 2-1. Schematic of typical edge combiner circuits and its timing diagram, indicating that delay variations affect the pulse duration of output signals.

As illustrated in Figure 2-1, delay variations ($\Delta d_n$) can affect the generated pulse duration or the timing of arrival (output 1). In the worst-case scenario, the logic gate for combination (XOR) cannot respond to a very short pulse train (output 2). This results in doubling the pulse width or reducing the carrier frequency to half. It consequently increases the unwanted spectral density over the maximum cap of Federal Communications Commission (FCC) regulation. Figure 2-2 shows the power spectral densities (PSD) of the generated pulses (output 2). It is clearly observed that the energy spread from inconsistent pulse widths causes the infringement of FCC. In a recent

literature, a calibration scheme was adopted by adding capacitor arrays in each delay unit to have a better control of pulse widths [39]. Nevertheless, this manual control approach not only needs continuous monitoring of a stream of pulses but also increases the complexity of the system. In this work, we presented an overlapping-free pulse generation scheme by implementing feedforward compensation in the edge combiner.




(a) (b)

Figure 2-2 (a) Power spectral density (PSD) without overlapping issue (ideal output) and (b) PSD with overlapping issue (output 2)

## 2.2 Transmitter architecture

The proposed UWB transmitter consists of an input driver, a feed-forward edge combiner (FFW-EC) with interpolators, and a highly duty-cycled inverter-based power amplifier (PA) driver, as shown in Figure 2-3. The baseband signal is fed into the input driver at 200 Mbps data rate. The output of the driver then activates the feedforward edge combiner to generate desired pulses. The generated pulses are amplified by the PA and then fed into a bandpass filter which is composed of an on-chip capacitor and a bond-

wire inductor. The output is matched to 50 Ohms at 4 GHz with a bandwidth of approximately 1GHz and is connected to an off-chip UWB antenna.

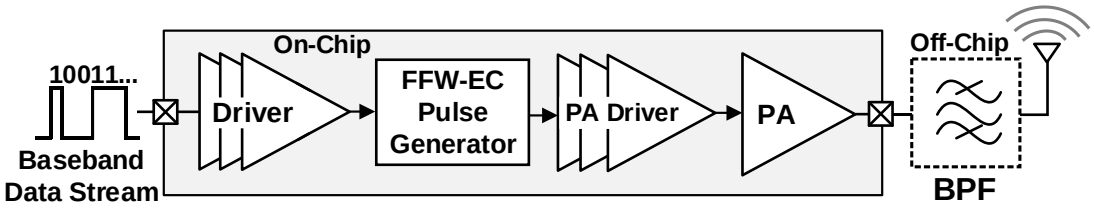



Figure 2-3 System architecture of the proposed UWB TX

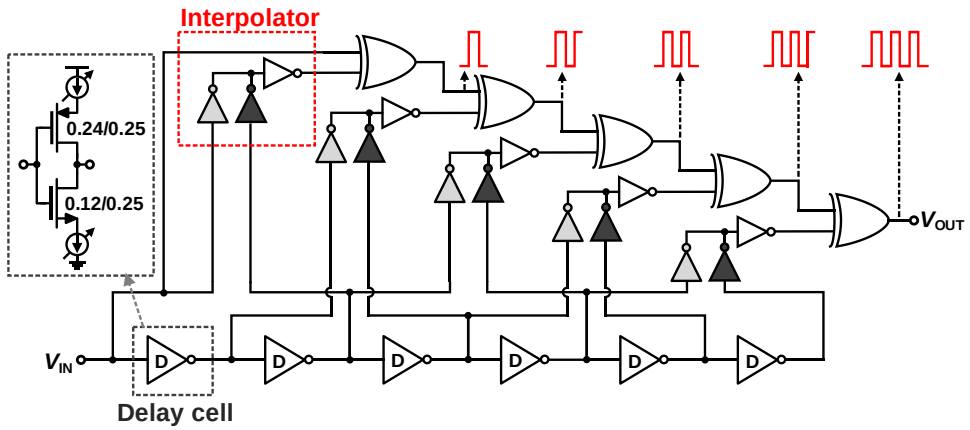



Figure 2-4 Conceptual block diagram of feedforward edge combiner-based pulse generator

### 2.2.1 Feedforward edge-combiner based pulse generator

The proposed feedforward edge combiner is comprised of a chain of variable delay cells and interpolators[40], which are added between every two delay cells as shown in Figure 2-4. The delay cell unit is an inverter with two additional programmable current sources for the control of intrinsic delays in order to provide frequency adjustment for multiple-user applications. The interpolator takes the input and output from the two

neighboring delay cells, and produces a pulse edge with an averaged phase between the two inputs. In mathematical model, the output of the edge combiner is given by:

$$y_n(t) = y_{n-1}(t) + x(t+\theta) - 2 \cdot y_{n-1}(t) \cdot x(t+\theta)$$

$$\theta = \begin{cases} (\tau + \Delta t_n) & \text{(conventional)} \\ (2 \cdot \tau + \Delta t_n + \Delta t_{n+1})/2 & \text{(proposed)} \end{cases} \quad (1)$$

where x(t) is the input of the edge combiner, $y_n(t)$ is the output of the $n^{th}$ stage XOR gate, $\tau$ is the intrinsic delay of a delay unit, $\Delta t_n$ is the variation of delay in each unit, and $\theta$ is the actual delay in each stage with effective variations. The actual delay in each stage can be either slower or faster than $\tau$. In the conventional edge combiner architectures, the variation of delay, $\theta$, is solely affected by that of each stage, i.e., effective variation = $\Delta t_n$. On the contrary, in the proposed implementation the delay is averaged between the two stages, where effective variation = $(\Delta t_n + \Delta t_{n+1})/2$, so that the pulse generator is less sensitive to the delay variations of individual stages. The two inverters of the interpolator, shaded in light and dark grey in Figure 2-4, are sized with a ratio of 1.67 of a unit-size invertor to generate an output edge of averaged phase between the two inputs. The generated edge then, feedforwards to the XOR gate input, thus the falling/rising edges of the XOR gate output will always fall between the two consecutive delay cells to guarantee non-overlapping pulses in any given baseband signals. The addition of interpolators imposes power overhead in the system as compared to the conventional edge combiners. However, the proposed feedforward edge combiner can ensure robust non-overlapping pulses without complicate calibration and continuous supervision required in the conventional systems. Also, precise duty-cycles are generated by taking the average of phases between two consecutive delay cells. To compensate for power overhead, we adopted the OOK modulation scheme to relax the power burden in the

transmitter, leaving the high processing overhead to the receiver side, known as asymmetric data transmission. To achieve additional power saving, we implemented pass gate logics. Pass gate logics consume lower switching energy to charge up a node compared to static logics. Also, the number of pulses allocated for sending 1-bit information has been assigned to three. At 3.6 GHz, the three pulses take up approximately 1 GHz of bandwidth that is sufficiently satisfies the FCC regulations as the minimum bandwidth requirement for UWB is 500 MHz. It also allows multiband transmission for system scalability and multiple-user scenarios.

### 2.2.2 Input driver and inverter-based power amplifier

Because the edge combiner is sensitive to both rising and falling edges, an input driver is required to produce well-defined edges. To save power, a dynamic latch comparator driver is adopted, as shown in Figure 2-5(a). Dual cross-coupled pairs, $M_{3\text{-}4}$ and $M_{9\text{-}10}$ , are implemented to give a fast switching speed. Figure 2-5(b) shows the inverter-based ($M_1$ and $M_2$) PA. It is implemented with two extra power sink and source pairs, $HP_{1\text{-}2}$ and $LP_{1\text{-}2}$, to provide programmability for output power adjustment from -15 to 0 dBm. The output is connected to a band pass filter (BPF) which is composed of a 200 fF on-chip capacitor and a 7 nH bond wire inductor at the band of interest.

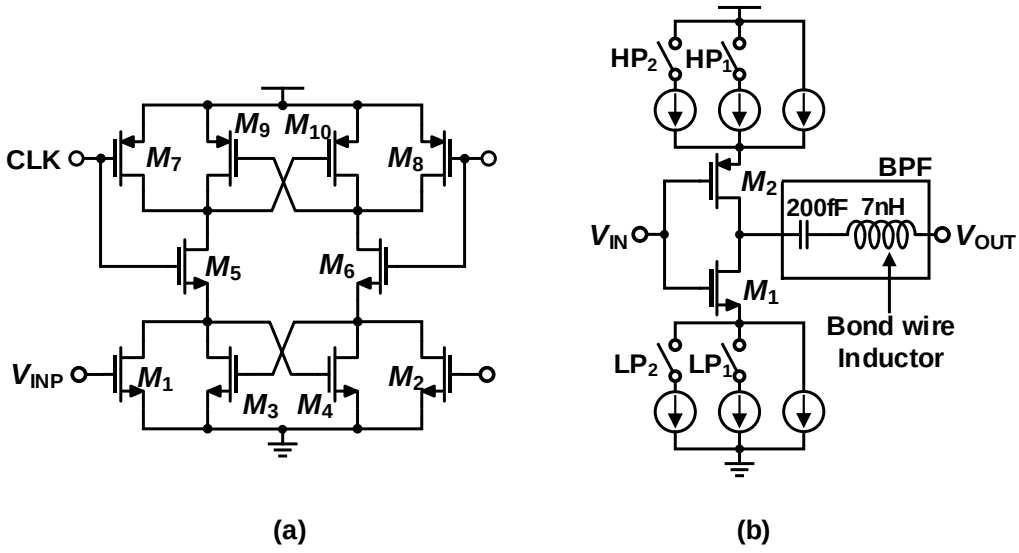



Figure 2-5 (a) Latch-based input driver, and (b) Inverter-based PA.

### 2.3 Experiment results

The transmitter has been fabricated using 65 nm CMOS processes with 1 poly and 9 metal layers. The chip is mounted on a FR4 PCB with voltage regulators to provide stable supplies since the trip point of delay chains is sensitive to supply variations. If this off-chip linear regulator is replaced by an on-chip converter with high PCE, the system power can be further saved[41]. Output matching is done by parasitic capacitance from the PCB along with a bond wire inductor. Figure 2-6 shows the measured baseband signal and the transmitted pulse waveform. The baseband signal is digitized from a subset of pre-recorded broadband neural signals. Output pulses are generated and transmitted when input signals toggle. In Figure 2-7, the measured PSD is under the FCC indoor mask at 200 Mbps with approximately 1 GHz of bandwidth and a center frequency of 3.6 GHz. Figure 2-8(a) shows the chip micrograph. The core area is less than 0.065 $mm^2$. The system consumes 0.867 mW at 200Mbps which is equivalent to 4.34 pJ/b at 1 V power supply.

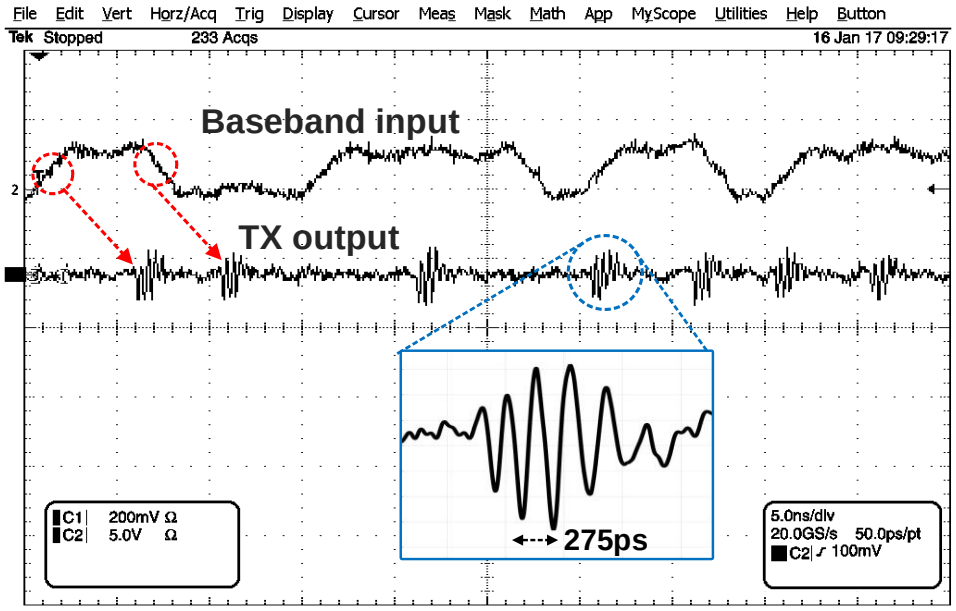



Figure 2-6 Measured baseband signal and transmitter output

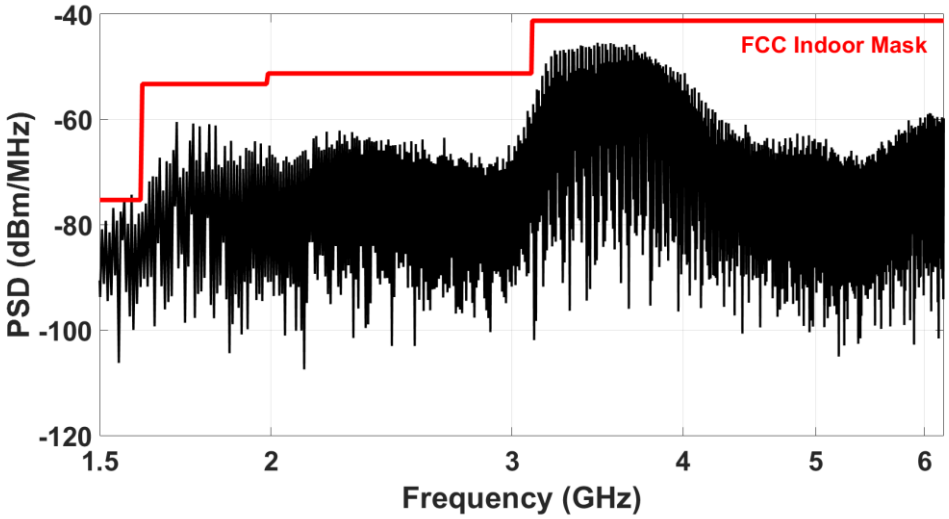



Figure 2-7 Measured power spectral density at a data rate of 200Mbps.

To demonstrate the functionality of the proposed transmitter, an in-vitro testing setup has been made (Figure 2-8(b)). The antenna, TDK ANT1085, at the transmitter side is covered with 5mm-thick ground pork at both top and bottom to emulate the signal

transmission from an implanted system. At the receiver side, off-the-shelf components are assembled on the PCB for signal amplification and detection, including MGA 86563 (Broadcom) for LNA, 4000BP (Johnson Technology) for bandpass filter and HMC713LP3E (Analog devices) for RF power detector. Signal is retrieved from a distance of 20 cm with BER < $10^{-3}$ at a data rate of 50 Mbps, which is constrained by the bandwidth of RF power detector. Table 2-1 summarizes the performance compared with recently published state-of-the-art results. This work has achieved the lowest Figure of Merit (FoM).

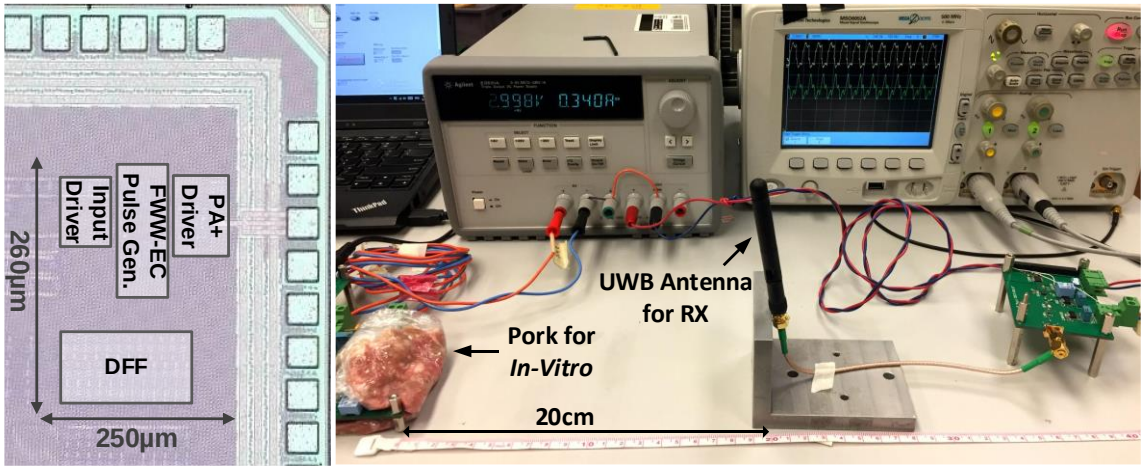



Figure 2-8 (a) Chip microphotograph and (b) In-vitro distance testing setup

Table 2-1 Performance summary with recent UWB transmitters

| | Tech. [42] | Area [$mm^2$] | Pulse generation | Data rate[Mbps] | $P_{OUT}$ [dBm] | Power [43] | FoM [pJ/b] |
|---|---|---|---|---|---|---|---|
| [37] | 65 | 4.6* | Oscillator | 1000 | -8.7 | 21.4 | 21.4 |
| [38] | 65 | 1.7 | Oscillator | 1000 | -26 | 7.46 | 7.46 |
| [39] | 65 | 0.182 | E.C. | 200 | -4 | 36 | 180 |
| [44] | 90 | 0.37 | E.C. | 12 | -7 | 0.54 | 45 |
| [45] | 65 | 0.032 | Oscillator | 0-50 | -11 | 0.8 | 8-16 |
| **This work** | **65** | **0.065** | **E.C.** | **200** | **-9** | **0.86** | **4.32** |

*Including TRX  E.C. = Edge Combiner

## 2.4 Chapter conclusion

In this work, a robust overlap-free ultra-low power ultra-wideband transmitter is presented by using 65 nm CMOS technology. It successfully regulates the timing of rising/falling edges and ensures non- overlapped pulse train by implementing feedforward edge-combiners. It has achieved the lowest FoM of 4.32 pJ/b at 200 Mbps with frequency programmability for multi-user scenarios. This work is applicable to accommodate 1,000-channel broadband neural signal recording and 10k-channel ECoG recording.

# CHAPTER 3
# Ultra- low power, Cancellation-Free, Bit-Wise Time-Division Duplex Transceiver for High Channel Count Closed-Loop Neural Interface

## 3.1 Introduction

As the channel count of recording/ stimulating increases, the need of high data rate wireless data transmission has been attracting more and more attention. Single direction of data transmission, however, is no longer sufficient for integrated systems. The inability to send stimulating signal or change channel settings without disturbing recorded data transmission is troublesome in understanding neural signal behavior.

As desirable as it sounds to have dual- direction communication ability in systems, nevertheless, there are challenges needed to be addressed appropriately. Firstly and most importantly, the system should not be hearing its own self, i.e. self-interference. One simple solution is that the transceiver uses different frequency bands for communication [46]. If these two bands are separated far enough in spectrum, the input matching of the receiver can filter out, if not all, the self-generated signal, assuming it is narrow-band signal.

Full duplex, on the other hand, supports transmission at the same frequency band simultaneously, potentially resulting in significant improvement in wireless network performance [47-49]. Works are proposed to transmit/ receive at the same frequency band, but attenuating the signal by separating receiving and transmitting antennas in the distance of multiple of half the wavelength [50-52]. These solutions are definitely trivial; however, they both need more than one antenna. For implantable systems, two-antenna

scenario increases the module area, causing discomfort for the animal-under-test, thus shorten the experiment duration. Some works pursued the goal differently. With known transmitted signal, it can be cancelled within the system. The cancellation scheme can be approached digitally, in analog or even both combined. In analog scenario, the receiver treats the self- transmitted signal as noise, and subtracts it from the received signal[51, 52]. This approach will need to be closely calibrated in signal delay and system amplification so that the unwanted signal can be cancelled out while the in-coming signal remains undisrupted. Digital cancellation, on the contrast, applies sophisticated DSP techniques to cancel the unwanted signal after the analog demodulation is completed [43, 53, 54]. However, the dynamic range of ADC limits the possible self-interference reduction. A sufficient amount of cancellation needs to be done before the digitization; thus, digital approach is generally applied in additional to analog approach[48].

As described above, either approaches are area consuming or complicate in implementation. We here propose an energy-efficient bit-wise time-division duplex (B-TDD) wireless transceiver for real-time, high channel count, bidirectional neural interface applicable to freely-behaving animal studies *in-vivo*.

### 3.2 Transceiver architecture

In order to build a cancellation- free, one- antenna solution for the bit-wise time division- duplex transceiver, we propose to utilize the advantage of ultra-wide band transmitter described in chapter 2. In time domain, ultra- wide band transmitter emits very short duration of pulses enables free allocation of incoming signal, as shaded dark red in Figure 3-1(a). With data rate of 200 Mbps, it has almost 80% of “blank space” within a single transmission time frame given the carrier frequency is 4GHz. In frequency

domain, due to the wide band characteristic of UWB, we can use the same antenna for receiving, as long as the band resides within 3.1-10.6GHz.

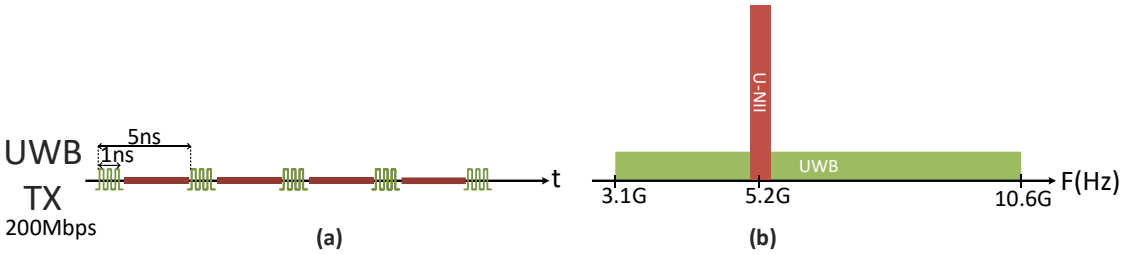



Figure 3-1 (a) Chip microphotograph and (b) In-vitro distance testing setup

Figure 3-2 shows the top level architecture of proposed B-TDD transceiver. It contains a continuous- time, U-NII band receiver, a feedforward edge combiner- based ultra-wide band transmitter, a digital controller and a 400MHz phase- locked loop (PLL).

As mentioned above, the operating band of receiver and transmitter is overlapped, one antenna is thus shared upon transmission and receiving. When the data is being emitted from the transmitter, a control signal is sent to the receiver to turn off the amplification of the receiver. Once one bit information is being transmitted, the control signal will turn on the LNA so the receiver can amplify and demodulate the incoming RF signal at U-NII band. Digital controller is implemented on chip to handle the demodulated signal from receiver, decode the signal and redistribute to the SPI for communication with recording/ stimulation modules. A 400MHz type-2 analog PLL is also implemented to provide the main clock throughout the whole chip.

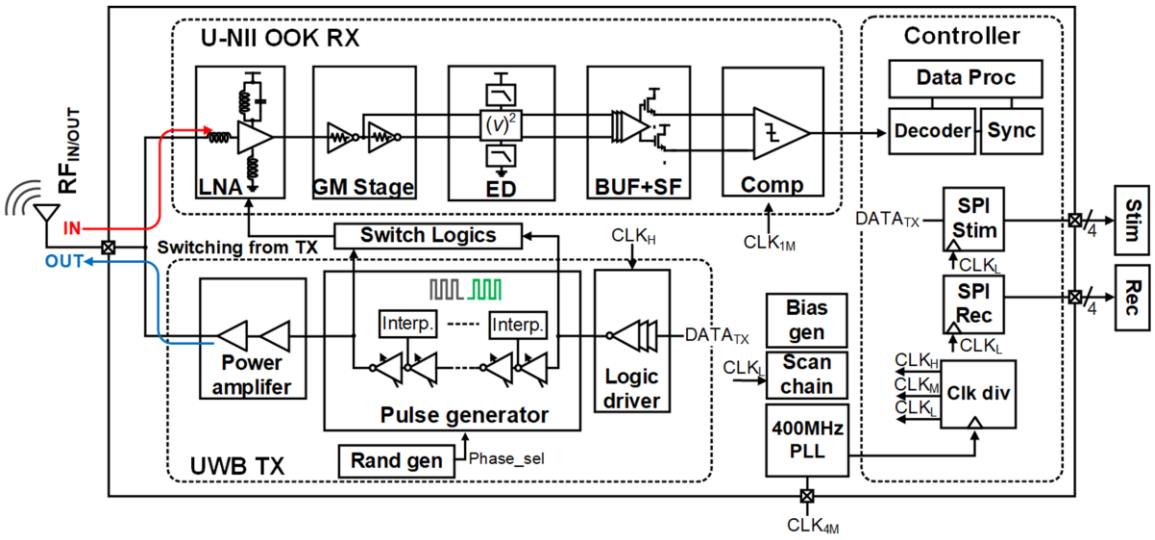



Figure 3-2 Top level architecture of proposed transceiver

The transceiver is implanted in asymmetric fashion, which leaves high complexity processing at the base station. The advantages of asymmetric structures have been reported numerous times in literatures, especially for biomedical application. Hence, the proposed transceiver adopts ultra-wide band structure for transmitter while continuous-time, OOK modulation is the best candidate for receiver, considering the restriction of low power dissipation of implantable systems.

### 3.2.1 Transmitter structure

As shown in chapter two, a feed-forward, edge combiner- based structure is used for transmitter. It provides an overlapping– free scheme for ultra- wide band pulse generation and transmission.

In UWB, pulses are sent in a regular repetition rate, and it leads to peaks in the spectrum of the transmitting signal. These peaks are referred to “spectral lines” or “comb lines”, which is undesirable since it limits the maximum transmittable power of UWB, as shown in Figure 3-3 and Figure 3-4. In order to resolve this issue, randomly delayed

pulses used in DB-BPSK is previously presented in [24]. While it allows UWB transmitter to emit higher power without violating FCC mask, the communicating distance can be further improved by utilizing frequency hopping (FH) technique[30].

In

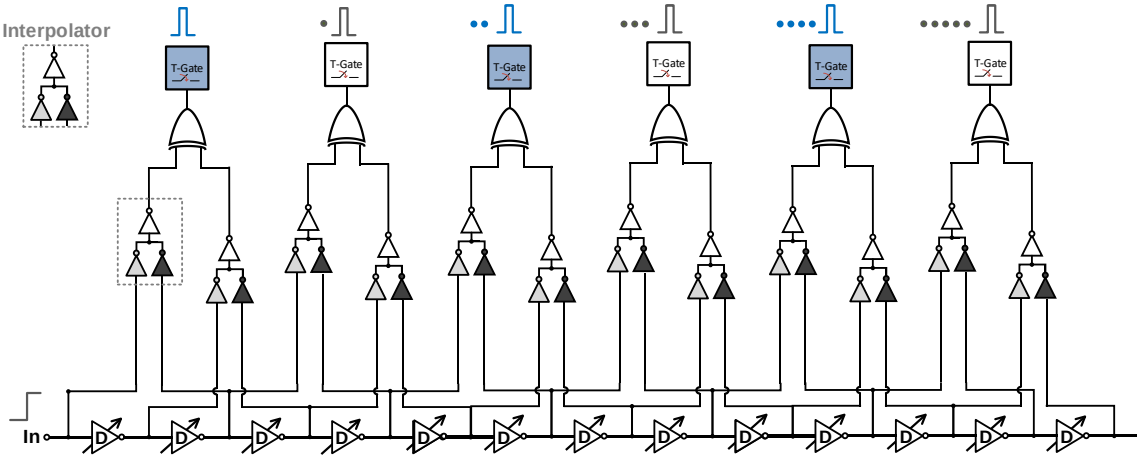



Figure 3-5 shows the simplified structure diagram of overlapping free, frequency hopping pulse generator. It adopts the edge combiner-based structure mentioned in chapter 2 to ensure no overlapping in generated pulses. The generated pulses are separated into two groups, shaded blue and grey. With randomly selected on/ off of the transmission gates (T-Gate), the pulse generator produces pulse train which has phase delay of $\pi$ between transmitted data. A frequency hopping scheme is also implemented with variable delay cells chain.

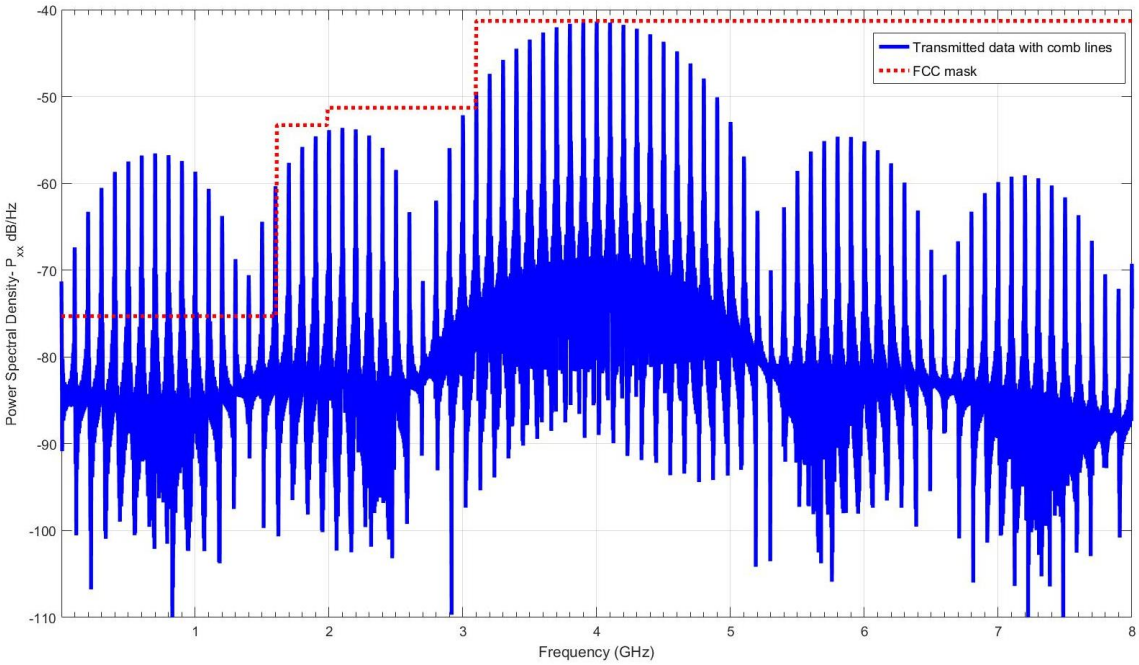



Figure 3-3 Transmitted signal in frequency domain

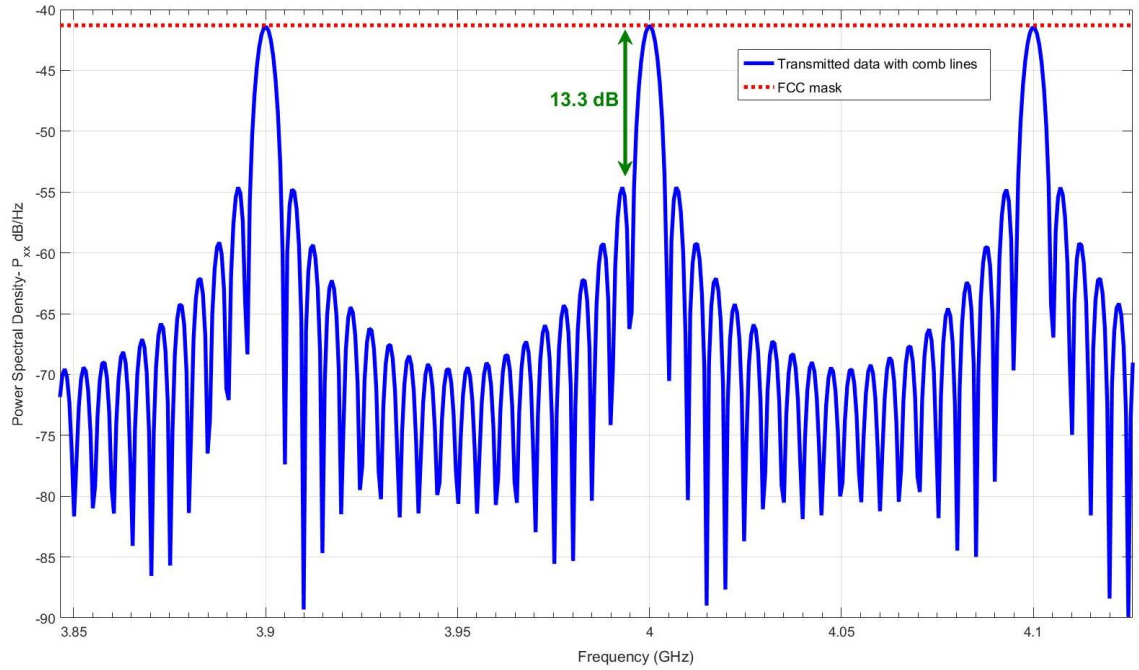



Figure 3-4 Zoom-in of the comb lines

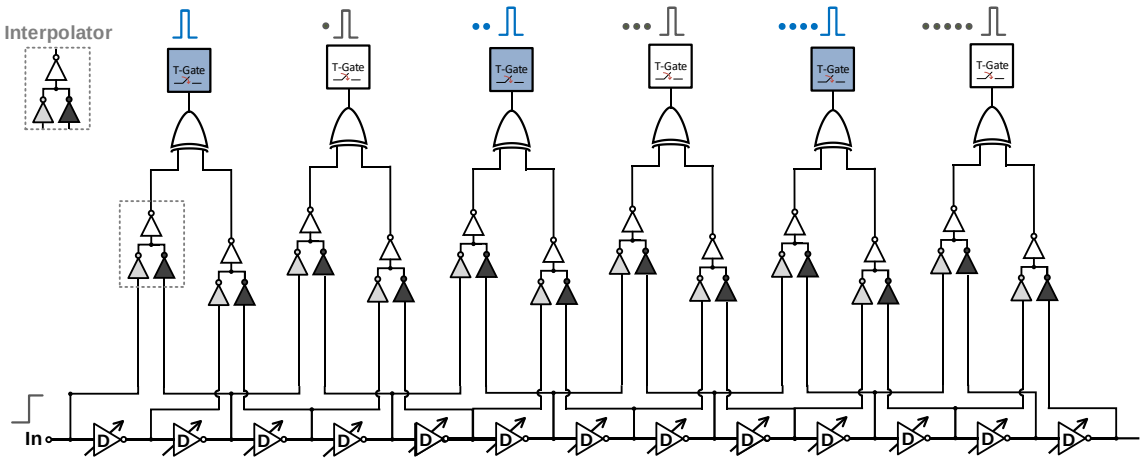



Figure 3-5 Simplified diagram of overlapping- free, frequency hopping pulse generator

### 3.2.2 Receiver structure

Figure 3-6 shows the block diagram of U-NII band receiver. It is composed of a low noise amplifier (LNA) as the first stage amplification, a GM stage for additional gain, an envelope detector to down convert the signal to baseband, further amplified by IFAMP stage before demodulated by the comparator.

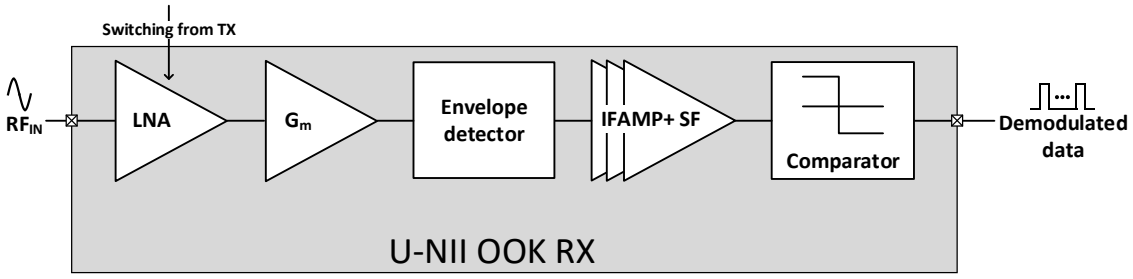



Figure 3-6 Block diagram of U-NII band receiver

The receiver is designed to interface with the transmitter for B-TDD purpose with a date rate of 10Mbps. As mentioned above, first stage LNA is turned off during the emission of transmitter signal which leads to approximately 20% of power loss in receiving data, assuming the transmitter is operating at its full speed. In order to

compensate for the loss, the comparator is oversampling at 50MHz and the 5× oversampled data is sent to the digital controller for the winner-take-all voting and further discriminate either the demodulated signal is for recording channel commands or stimulation parameters by the result of the header description. The voting system will output the demodulated 1 bit result based on the majority poll among 5 incoming data. In simulation, the voting scheme improves the BER performance by 6 dB at 0.1% error rate compared to the case without the voting as shown in Figure 3-7.

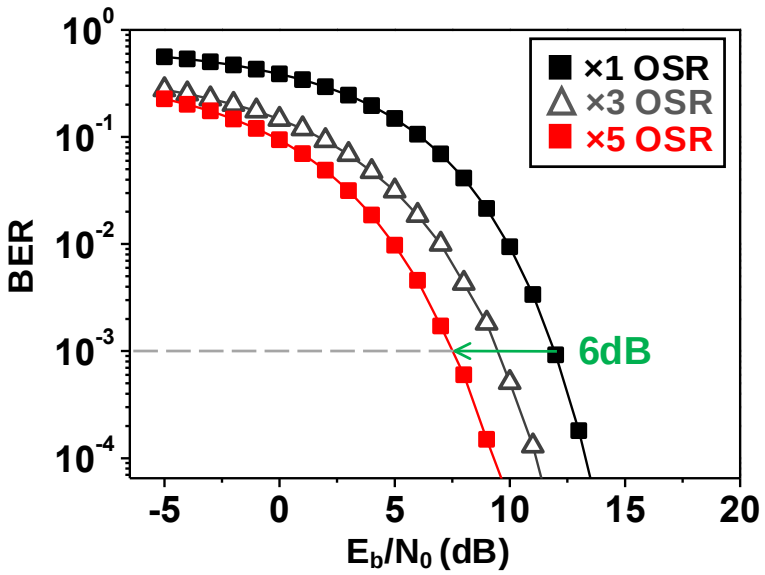



Figure 3-7 BER vs. OSR demodulation

### 3.3 Circuit implementation

Since the transmitter structure is similar to the one mentioned in chapter 2, we will briefly discuss the new features added onto the system. The main focus will be on the receiver implementation.

#### 3.3.1 FFW-ED pulse generator equipped with delayed hopping ability

In order to reduce the spectral lines, the pulse generator is now equipped with frequency hopping mechanism and delayed pulse generation. As shown in Figure 3-8(a),

the pulse generator is composed of a chain of variable delay cells, interpolators, exclusive-or gates and transmission gates (T- Gates) grouped in two.

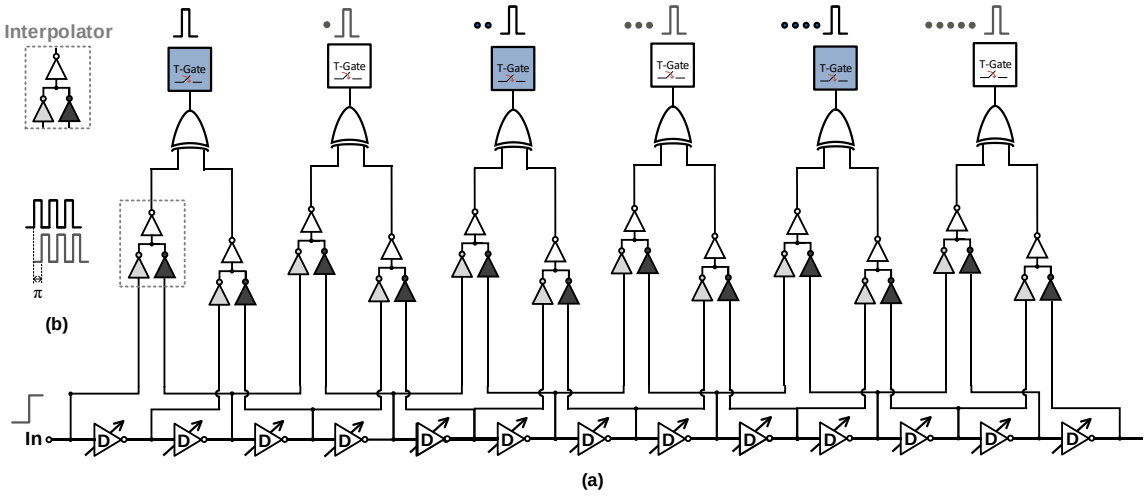



Figure 3-8 FWW-ED pulse generator with delayed hopping ability

The working principle of interpolation has been illustrated in detail in chapter 2 which will prevent overlapping of the generated pulses. Here, the new addition is the T-gates that separate the generated pulses into two groups with a phase delay of $\pi$, as shown in Figure 3-8(b). The control on the T- gates is generated by a pseudo random binary sequence (PRBS) block in the digital controller.

The delay cell chain is composed of inverters with variable current sources with binary weights, as shown in Figure 3-9(a). $P_{1\text{-}2}$ and $N_{1\text{-}2}$ are implemented with high $V_T$ (HVT) transistors to reduce the leakage. Figure 3-9(b) shows the circuit structure of inverter-based power amplifier. The generated pulses from pulse generator will be fed into $IN_{1\text{-}6}$, if not bypassed by T-gates. The combined pulses train will then be emitted by $M_{8\text{-}9}$, with the matching accomplished by the on-chip output capacitor $C_1$ and the bond-wire inductor.

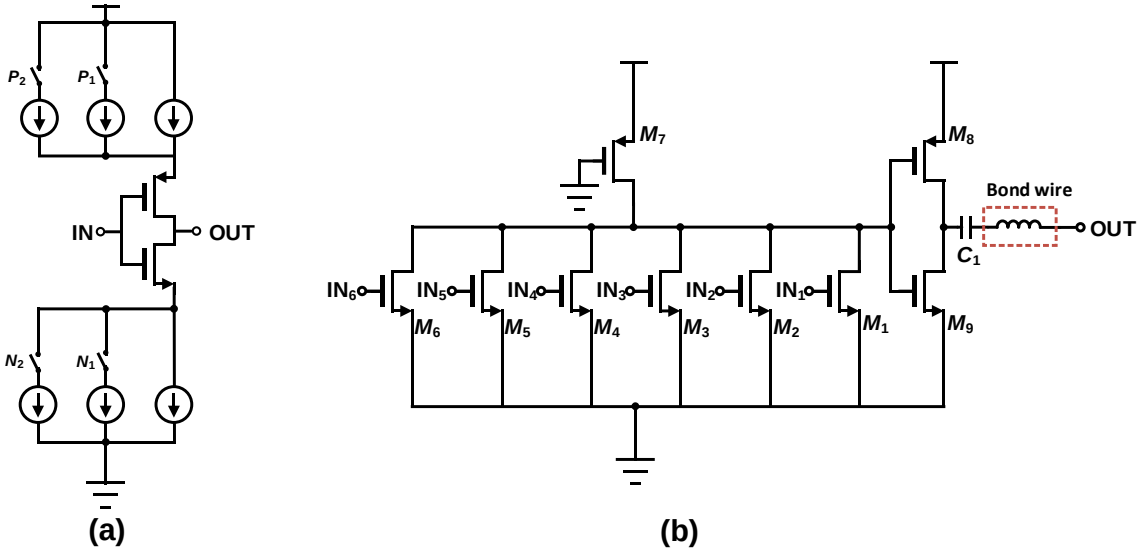



Figure 3-9 (a) Delay cell with variable delay (b) Inverter-based power amplifier

$M_{1\text{-}6,8\text{-}9}$ are low $V_T$ (LVT) transistors for high speed operation since each pulse has duration as small as 200p seconds. The output capacitor $C_1$ and bond- wire inductor are carefully calculated for matching purpose, giving 600f F for $C_1$ and 2.8n H for the bond-wire inductor.

### 3.3.2 Switch-able low noise amplifier design

As shown in Figure 3-10, source degeneration scheme is adopted for the LNA design since a narrow band is required for our application. The input impedance can be derived as[55]:

$$Z_{in} \approx s\ \ L_g + L_s\ \ + \frac{g_{m1}L_s}{C_{gs}} + \frac{1}{sC_{gs}} \tag{3-1}$$

In order to achieve good input matching, the input return loss $S_{11}$ can be derived as:

$$\begin{aligned} S_{11} &= \frac{Z_{in} - R_s}{Z_{in} + R_s} \\ &= \frac{s(L_g + L_s) + \dfrac{1}{sC_{gs}}}{s(L_g + L_s) + 2 \cdot \dfrac{g_m L_s}{C_{gs}} + \dfrac{1}{sC_{gs}}} \\ &= \frac{s^2 + \dfrac{1}{C_{gs}(L_g + L_s)}}{s^2 + 2 \cdot \dfrac{g_m L_s}{C_{gs}(L_g + L_s)} \cdot s + \dfrac{1}{C_{gs}(L_g + L_s)}} \\ &= \frac{s^2 + {\omega_o}^2}{s^2 + Bs + {\omega_o}^2} \\ &= \frac{s^2 + {\omega_o}^2}{s^2 + \dfrac{\omega_o}{Q} s + {\omega_o}^2} \end{aligned} \tag{3-2}$$

, in which

$$R_s = \frac{g_{m1}L_s}{C_{gs}} \tag{3-3}$$

$$\omega_o^2 = \frac{1}{C_{gs}\ \ L_s + L_g} \tag{3-4}$$

$$B = 2 \cdot \frac{g_{m1}L_s}{C_{gs}\ \ L_s + L_g} \tag{3-5}$$

$$Q = \frac{\omega_o}{2R_s} L_s + L_g \tag{3-6}$$

,where $R_s$ = 50Ω, $\omega_o$ is the resonant frequency, $B$ is the -3-dB matching bandwidth and $Q$ is the quality factor. Per the design, the inductance of input matching is achieved by both bond-wire and on-chip inductor to provide a better flexibility while the $C_{gs}$ is the parasitic capacitance of input transistor $M_1$.

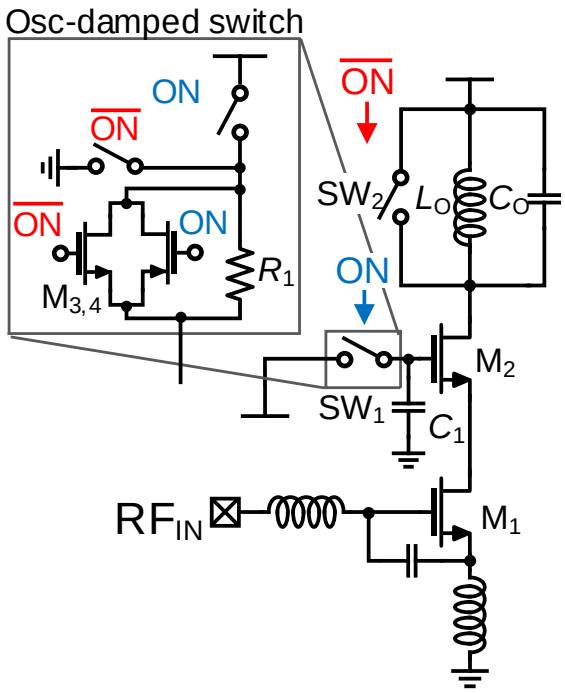



Figure 3-10 Circuit diagram of switch-able low noise amplifier

To calculate the mid-band gain and frequency response, $S_{21}$ can be easily calculated as[56] :

$$
\begin{aligned}
S_{21} &= 2 \cdot \frac{RF_{out}}{RF_{in}} \\
&= \frac{-2g_{m1}\omega_o{}^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o{}^2} \cdot \frac{r\omega_{o1}{}^2 + sL\omega_{o1}{}^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o{}^2} \\
&\equiv \frac{-2g_{m1}\omega_o{}^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o{}^2} \cdot Z_L\ s \\
&\equiv G_{m21}\ s\ \cdot Z_L\ s
\end{aligned}
\tag{3-7}
$$

, where $\omega_{o1}{}^2 \equiv 1/L_oC_o$, $r$ and $L$ represents the equivalent series resistance and inductance of the inductor $L_o$. In equation 3-7, $G_{m21}(s)$ is the transconductance of the input stage assuming a perfect matching, i.e. $v_{g1} = v_{RF,IN}/2$ . $Z_L(s)$ is the equivalent load impedance seen at the output node $RF_{out}$.

As mentioned, the fast and complete switching in the LNA is a one of the most essential requirements for our B-TDD duplex because it guarantees less crosstalk between the up- and down-links. For this purpose, we use two switches, $SW_{1,2}$ to control the gate bias of $M_2$, as well as the output tank in the LNA, as shown in Figure 3-10. The switch control is directly correlated with the transmission signal. When the baseband sends the data to the transmitter, the data edge is forwarded to logic gates to disable the RX amplification. As soon as TX pulses are transmitted, the last edge will then active the RX to start receiving signal. With the given technology of 65 nm process, the fast switching for receiving signals within 4 ns of the time slot is easily implementable. However, too fast switching, in particular, on-switching can inject instantaneous current into the tank, resulting in prolonged ringing in a high-Q tank as shown in Figure 3-11. To alleviate the wrong decision caused by the ringing, we intentionally insert a 2.5 kΩ

damping resistor ($R_1$) in the gate of $M_2$. While turning on the LNA, the charging path $R_1$–$C_1$ gives a larger time constant (800 ps) to smooth out the transition of current injection into the tank thus completely suppress the ringing as shown in Figure 3-11. On the other hand, when the edge triggers the RX switch signal to transition from short to open, the oscillation is inherently suppressed by the $SW_2$ in parallel with the tank. Therefore, to restore the fast operation, a transmission gate composed of $M_{3,4}$ is inserted to reduce the equivalent resistance into 131 Ω (in simulation), recovering the fast operation.

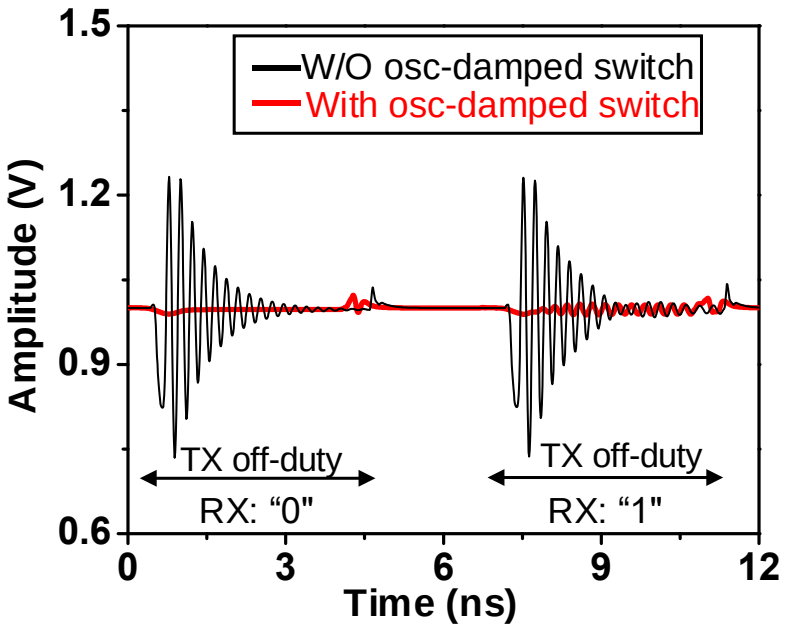



Figure 3-11 Switch noise damping comparison

### 3.3.3 GM gain stage design

To provide additional gain, an inverter-based, self-biased single- to- differential gain stage is adopted and the structure is shown in Figure 3-12. In ultra- low power applications, inverter-based with resistive feedback topology is popular because of its

simplicity and smaller area consumption compared to LC tank structure [57-59]. Resistive feedback, inverter-based amplifier exhibits large bandwidth product and also yields to larger gain since the input transconductance is now twice by utilizing both $M_1$ and $M_2$ as input.

As shown in Figure 3-12, $C_1$ and $C_2$ work as decoupling capacitors to separate the bias from previous stage, *i.e.* LNA, while $M_1$ is biased via additional current source set by $V_B$ and $M_2$ uses resistive feedback to set the gate biasing point. The output of first stage will then be forward to the gate of $M_3$ through a decoupling capacitor $C_3$ and further amplified to produce differential output for envelope detector.

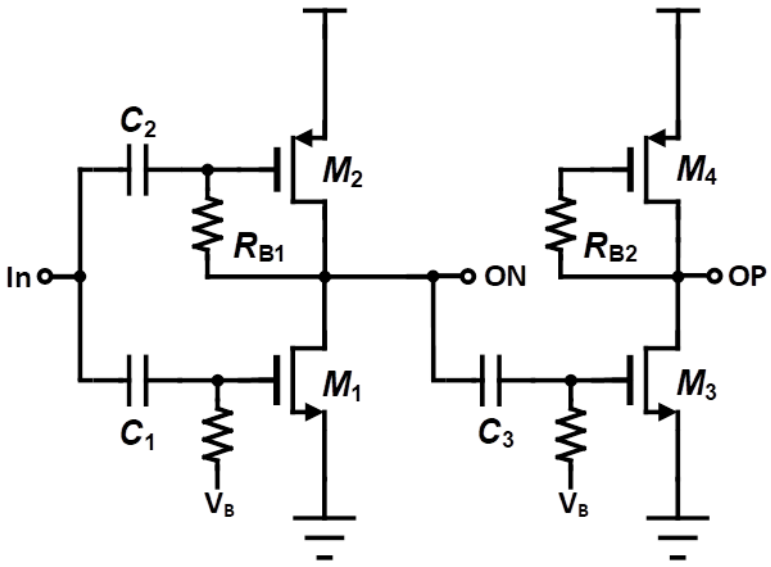



Figure 3-12 Inverter-based self-biased gain stage

The intrinsic voltage gain is expressed as:

$$\frac{V_{ON}}{V_{IN}} = -(g_{mN} + g_{mP} - \frac{1}{R_{B1}}) \cdot (R_{B1} // r_{on} // r_{op}) \tag{3-8}$$

, where $g_{mN}$ , $g_{mP}$ is the transconductance, $r_{on}$ , $r_{op}$ is the parallel output resistance of $M_1$ and $M_2$ respectively.

To provide a differential input for the envelope detector, an extra stage to produce 180 degree phase shift is also implemented through $M_3$, $M_4$ and $R_{B2}$. The voltage gain can be expressed as:

$$\frac{V_{OP}}{V_{g,M_3}} = -g_{mN}(r_{on_3} // R_L), \tag{3-9}$$

$$R_L = \frac{R_{B2} + r_{op4}}{1 + g_{m4} r_{op4}} \tag{3-10}$$

### 3.3.4 RF envelope detector design

After the GM stage, the signal will be fed into the envelope detector as shown in Figure 3-13. The main idea of this structure is that it takes the advantage of the nonlinearity of transistors while biased at weak inversion, as first introduced in [60]. When biased in weak inversion, the current of transistor can be written as[61, 62]:

$$I_d = I_0 e^{\frac{V_G - V_{th}}{nV_T}} \cdot \left( e^{\frac{-V_S}{V_T}} e^{\frac{-v_i^+}{V_T}} - e^{\frac{-V_D}{V_T}} \right) \tag{3-11}$$

, and we define the signal directly related to input signal as:

$$I_d = I_Q e^{\frac{-v_i^+}{V_T}} \tag{3-12}$$

,where $I_Q = I_0 e^{\frac{V_G - V_{th}}{nV_T}} e^{\frac{-V_S}{V_T}}$ , $V_T$ is the thermal voltage ( $k_B T / q$ ), $V_{th}$ is the threshold voltage n corrects the slope of the transfer function for losses due to capacitive division [62]. The power series expansion of equation (3-12) can be written as:

$$I_d = I_Q \left[ 1 + (\frac{-v_i^+}{V_T}) + \frac{1}{2!}(\frac{-v_i^+}{V_T})^2 + \frac{1}{3!}(\frac{-v_i^+}{V_T})^3 + ... \right] \tag{3-13}$$

With input signal written as a single tone sine wave: $v_i^+ = A\sin(2\pi f_{in} t)$, the 2nd order term of equation (3-13) then becomes:

$$i_{2nd} = \frac{I_Q A^2}{4V_T^2} 1 - \cos(2\pi(2 f_{in})t) \tag{3-14}$$

From equation (3-14), one DC term is obtained while the $2f_{in}$ term can be easily filtered out. With the differential structure shown in Figure 3-13, $v_{on}$ can then be expressed as:

$$v_{on} = \frac{-I_Q A^2 R_{out}}{2V_T^2} \tag{3-15}$$

, while $R_{out}$ is the output resistance seen at the node.

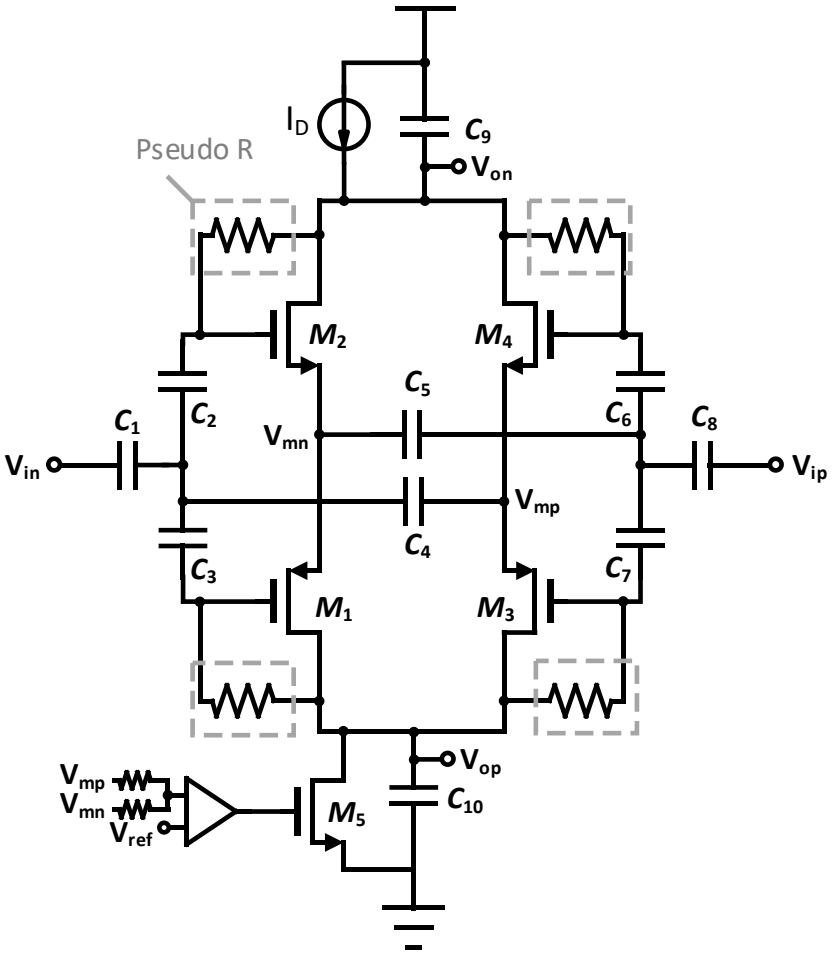



Figure 3-13 Circuit structure of envelope detector

To provide differential output, the bottom part of the envelope detector is then the mirrored structure by adopting PMOSs and a common-mode feedback current source $M_5$ to define the operating point. With the same analysis method, $v_{op} = I_Q A^2 R_{out} / 2V_T^2$ can be easily obtained.

### 3.3.5 Baseband amplifier design

Figure 3-14 shows the baseband 2-stage buffer with a common-mode feedback stage. The first stage adopts feedback resistors $R_{1,2}$ to define the gate bias of $M_{3,4}$. Second stage

output $V_{op}$, $V_{on}$ are fed into the common-mode feedback stage via resistors $R_{3,4}$ and compare to the reference voltage $V_{ref}$ to adjust the gate bias of $M_{7,8}$.

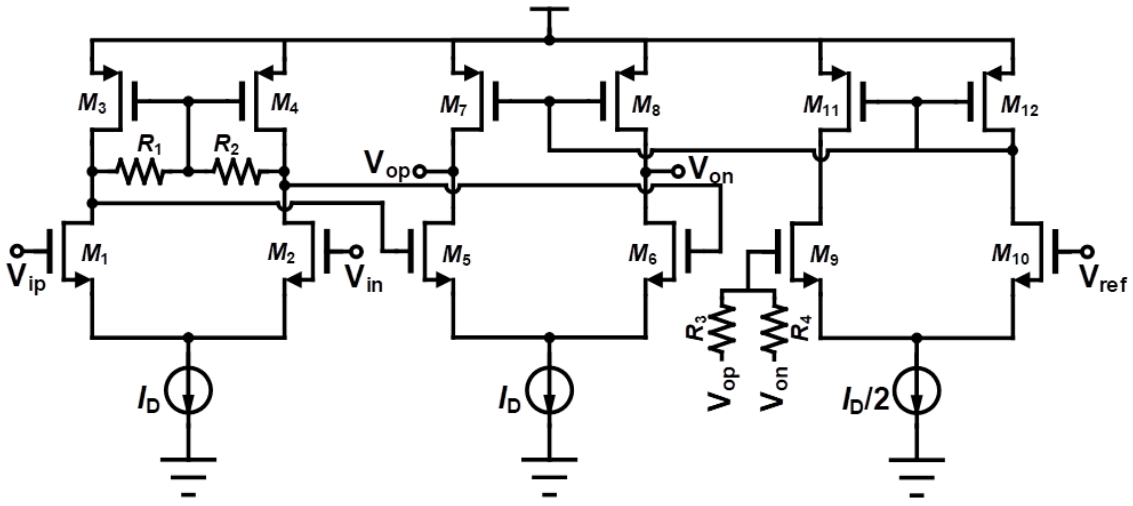



Figure 3-14 Circuit diagram of baseband buffer

### 3.3.6 Comparator design

A two crossed-coupled pair structure dynamic comparator is shown in Figure 3-15. When the CLK = low, $M_{11,12}$ drag the output nodes to VDD while $M_{7,8}$ are shut off, leaving no constant current flowing the either branches. In the meantime, $M_{3,4}$ drag the drain of input pair to ground for a clean reset. When CLK switches from low to high, the difference at the drains of input transistors gets positively reinforced and further discharges the output node $V_{OP}$ and $V_{ON}$ at different rate due to the voltage difference between input pair. The output latches then strongly enhance the output difference further until one of $M_{9,10}$ is turned off, and the comparing process is completed. The transitioning current also gets shut off once the comparing is done so no static power is consumed.

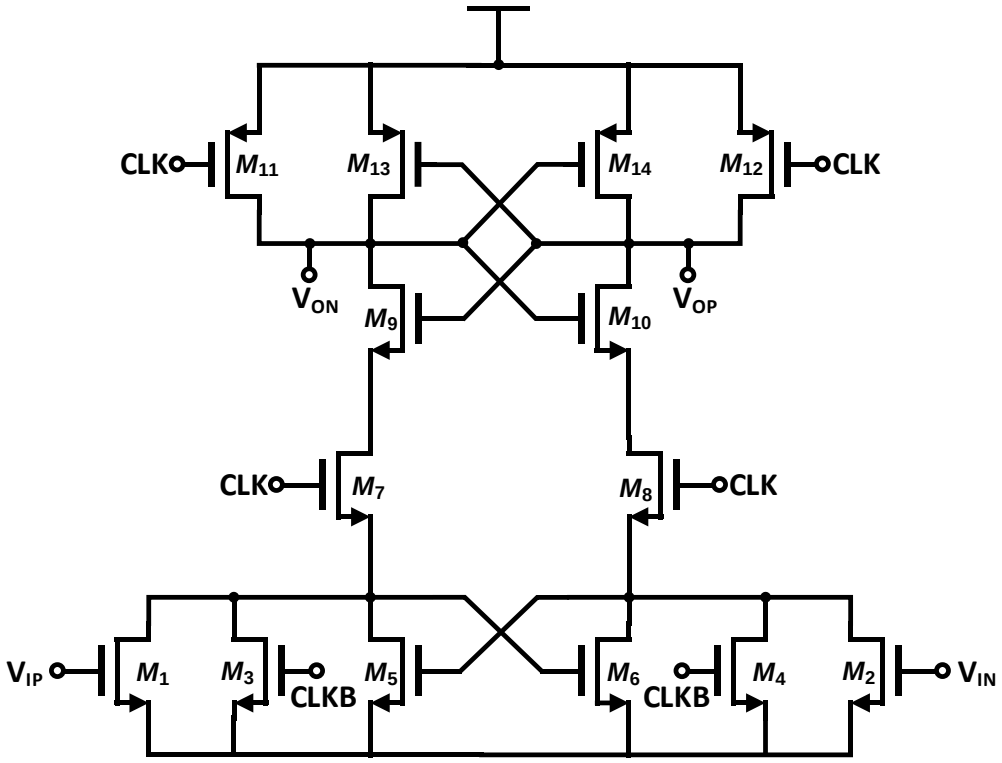



Figure 3-15 Comparator circuit diagram

To reduce the offset, input transistors and the cross- coupled inverters need to be checked carefully[63]. According to [42], the offset is roughly proportional to $1/\sqrt{WL}$, where W and L is the width and length of the input transistors, so large size inputs are adopted. As for the cross- coupled inverters, the mismatch of $V_t$ dominates the offset performance and can be expressed as [64]:

$$\sigma\ \Delta V_t\ = \frac{A_{vto}}{\sqrt{W - DW\quad L - DL}} \tag{3-16}$$

, where $\sigma\ \Delta V_t$ is the standard deviation of the $V_t$ mismatch, $A_{vto}$ is the Pelgrom [42] coefficient, and *DW* and *DL* are the channel length and width reduction parameters respectively. From equation (3-16), the sizes of the inverter and latches are maximized without affecting the speed of the comparator.

### 3.4 Experiment results

This chip was fabricated in a 65 nm RF CMOS process. The chip microphotograph is shown in Figure 3-16. The area is 1.4 × 0.56 $mm^2$, while the core is less than 0.35 $mm^2$. Figure 3-17 shows the power spectral density (PSD) of the UWB transmitter. The PSD is under the FCC indoor mask with a rate at 200 Mbps PRBS data train with the frequency hopping, as well as the random delayed scheme applied. The pulse overlapping is prevented so there is no peak at half the transmitting frequency, 2.4GHz, as shown in Figure 3-18 shows the enlarged transmitted waveform with Pout approximately at -8 dBm, carrier frequency at 4.8GHz.

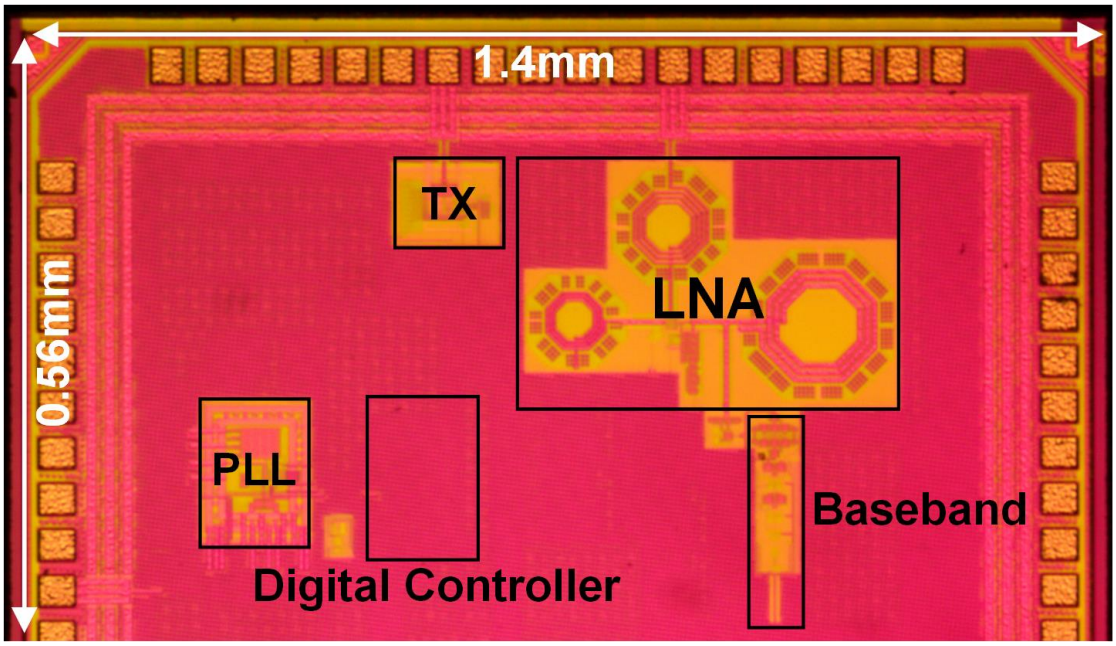



Figure 3-16 Chip microphotograph

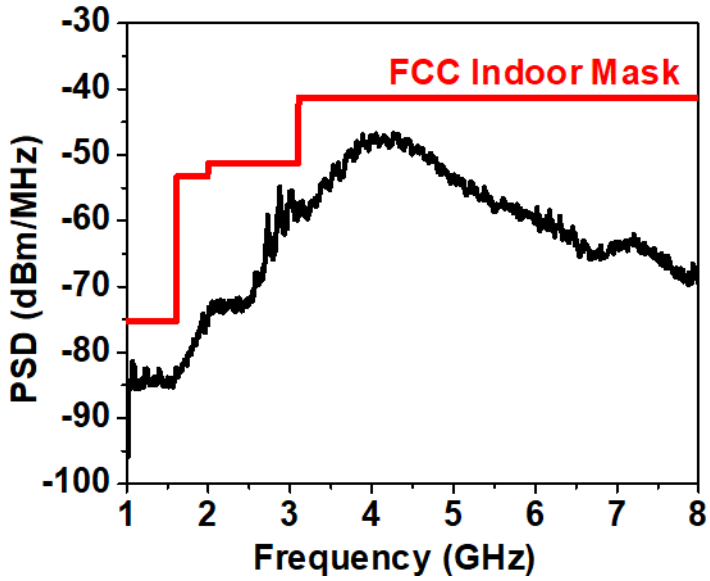



Figure 3-17 UWB PSD at a data rate of 200Mbps

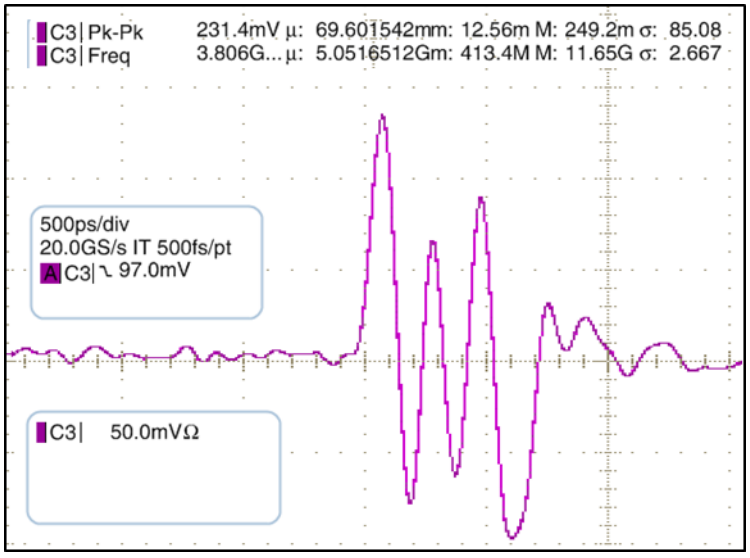



Figure 3-18 Snapshot of the enlarged transmitted waveform

Figure 3-19 shows the input matching of the receiver LNA. The value is under −10 dB at the band of interest (5.15−5.25GHz). The BER versus input power plot is also shown in Figure 3-20. The sensitivity with <10-3 BER is -73.4 dBm at 10Mbps. Figure 3-21 is the transient waveform of fragmented digitized signal of pre-recorded neural

signal sending to transmitter. The transmitter output pulses are generated when the input signals toggle are also provided in the inset of Figure 3-18. The recovered and demodulated waveform of receiver is shown in Figure 3-22 at 10Mbps. The performance summary is shown in Table 1.

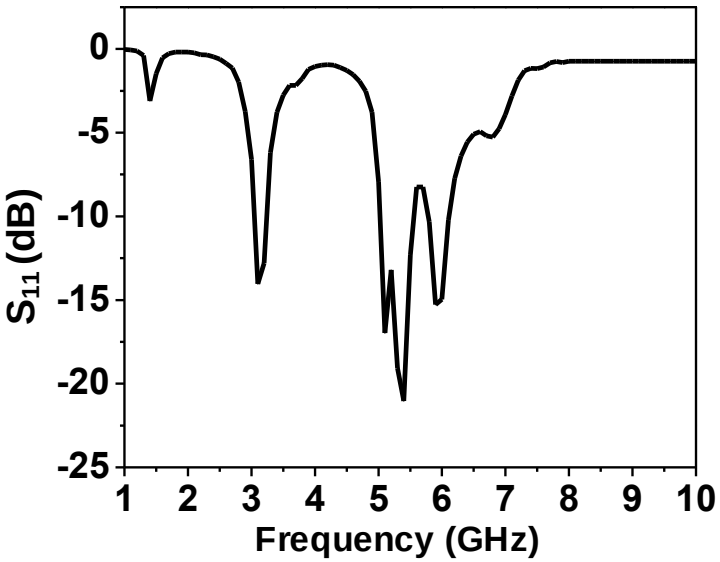



Figure 3-19 Receiver input $S_{11}$

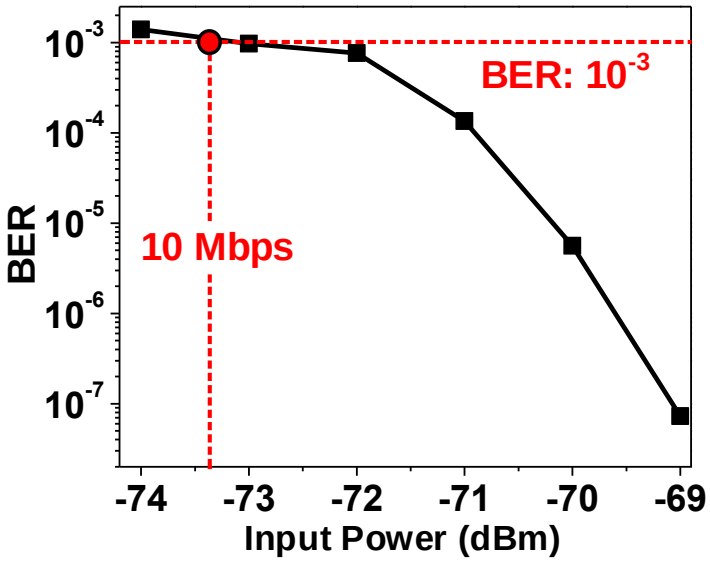



Figure 3-20 BER vs input power (dBm)

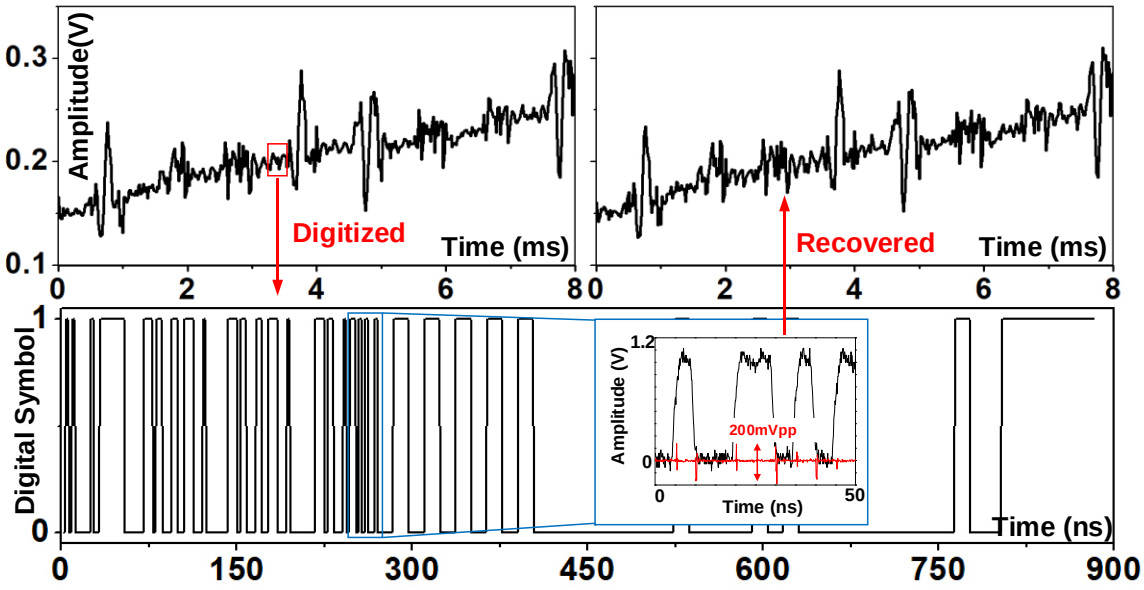



Figure 3-21 Transmitter transient waveform

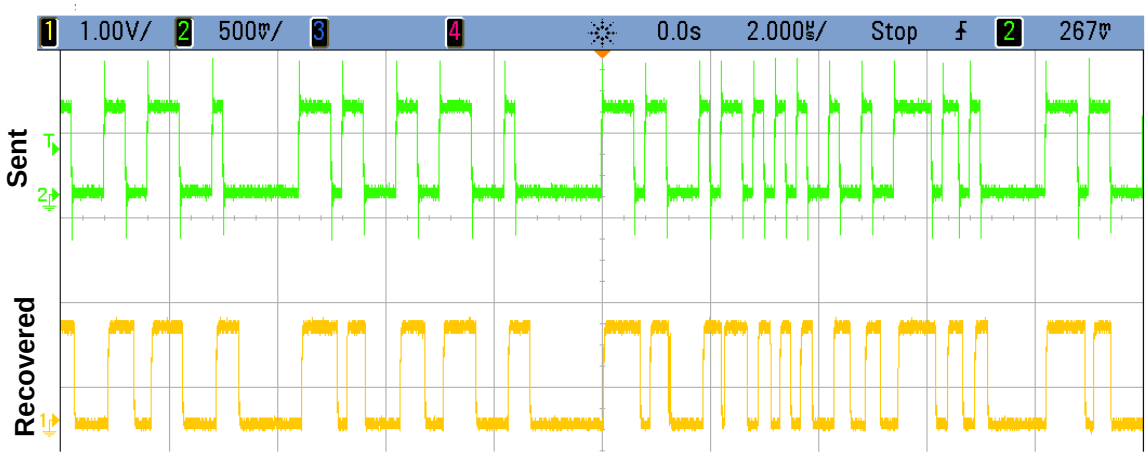



Figure 3-22 Receiver transient waveform

Table 3-1 Performance Comparison of Duplex Transceiver Systems

| | | **This work** | [31] | [33] | [35] | [18] | [65] |
|---|---|---|---|---|---|---|---|
| Technology(nm) | | 65 | N/A | 40 | 180 | 130 | 65 |
| Frequency (GHz) | | 5.2/UWB | 2.4 | 0.4 | 2.4/UWB | 2.4 | 0.1-1.5 |
| Bi-directional communication | | Yes | Yes | No | Yes | Yes | Yes |
| Method for bi-direction | | Bit-wise time division mux | Packet-wise time division mux[1] | N/A | Dual band full duplex | Switch | Self-cancelling |
| TX | Data rate (Mbps) | 200 | 2 | 0.01-4.5 | 500 | 1/5/8 | 0.1-1.5 |
| | Max $P_{out}$ (dBm) | -3 | -18 -0 | -10 | N/A | 0.2 | -10 |
| | FoM(pJ/b) | 9.7 | 16900 | 504 | 7 | 460[2] | 37333[5] |
| RX | Modulation | OOK | N/A | DBPSK | OOK | OOK/BPSK | N/A |
| | Data rate (Mbps) | 10 | 0.25-2 | 0.01-4.5 | 100 | 0.1/1/5/8 | N/A |
| | Power (mW) | 3.2 | 40.5 | 2.19 | 5 | 0.78[3], 10.2[4] | 43-56[6] |
| | FoM(nJ/b) | 0.32 | 20.25 | 0.49 | 0.05 | 7.8[3], 1.275[4] | 37333[5] |
| | Sensitivity(dBm) | -73.4 | -82 | -83 | N/A | -77[4] | $< 1e^{-12}$ |
| Integration level | | Fully integrated | Fully integrated | Fully integrated | External clock + controller | External biasing | RF front-end + LO generation |
| Area ($mm^2$) | | 0.35 | N/A | 3.06 | 0.8 | 3.3 | 1.5 |

[1]Switching time = 130μs, [2]at its highest data rate, [3]sensor OOK, [4]gateway BPSK, [5]full chip FoM, [6]full chip

## 3.5 Summary and chapter conclusion

We have presented a cancellation free, ultra- low power transceiver designed for high channel count neural recording and optogenetic simulation system. The transceiver module adopts asymmetric structure and B-TDD scheme to realize real-time, closed-loop control, while maintaining ultra-low power consumption at 9.7 pJ/b in transmitter and 0.32 nJ/b in receiver. By sharing one antenna, it highly reduces the module area, enables compact implementation which is indispensable for high channel- count implantable neural interface applications.

# CHAPTER 4
# System Integration of Wireless Data Telemetry and Optogenetic Neural Modulation and Recording

## 4.1 Introduction

Since it made its first entrance in 2005[66], optogenetic research has been gaining its popularity in neural science research. This technique genetically modifies specific types of neurons to express light-sensitive ion channels, called opsins, on their membranes [67]. The channels then react to specific wavelength of light to further excite or inhibit neural activities. Compare to traditional electrical currents, the optical stimulation is more precise to the cells it reaches, while a suggested possibility of reduction in electrically stimulated subjects' reaction time when it appeared outside the receptive field [68]. It also makes simultaneous recording much easier, while the electrical method tends to saturate the recording amplifier or induces huge artifacts that cannot be easily compensated afterwards.

With a previously fabricated and published work in our lab [67, 69], a closed-loop, bidirectional neural interface with optoelectrode are ready to be integrated with wireless transceiver for compact, free-moving experiments. From an engineering perspective, the interconnection between blocks, the heat dissipation, and the power and timing distribution are the first challenges to come to mind. On top of that, when the application is focused on implantable devices, it becomes increasingly more complicated. Bio-compatible material for the implanted devices is the first necessity so the animal doesn't have rejecting reactions to the devices. Temperature change also needs to be closely

monitored to keep an unharmful environment for the brain cells of animal- under- test. The system weight is also important. The total system weight, including power sources, assembly cables and any interconnections, should be no more than 10% of the animal weight. When the test object is a larger animal, like a rat or a genuine pig, around a 30-gram constraint is applied. However, for smaller rodents like mice, a strict 3-gram system is required.

### 4.2 Previous works

There have been some efforts devoted in the integration of optogenetic systems and wireless modules. Commercially, Teleopto from Amuza and Helios from Plexon all provide wireless communication capabilities for optogenetic from 1-3 gram sizes, however, no recording channels are implemented and the stimulation channel count is very limited.

[70-72] provide higher chancel counts for stimulation and recording, nevertheless, the use of COTS (commercial off-the-shelf) components for wireless modules severely constrains the expansion possibility for higher channel counts due to the limited data rate and signal bandwidth.

### 4.3 Proposed integration

To accommodate high channel count optogenetic neural modulation and recording, a data rate of 200 Mbps is required, assuming 1000 channels, 10-bit resolution, 20 kHz sampling rate for recording, while 36 channels stimulation can be supported by 10 Mbps. An integration of previously presented wireless transceiver and existing recording/ stimulation module for optogenetics is proposed in this chapter.

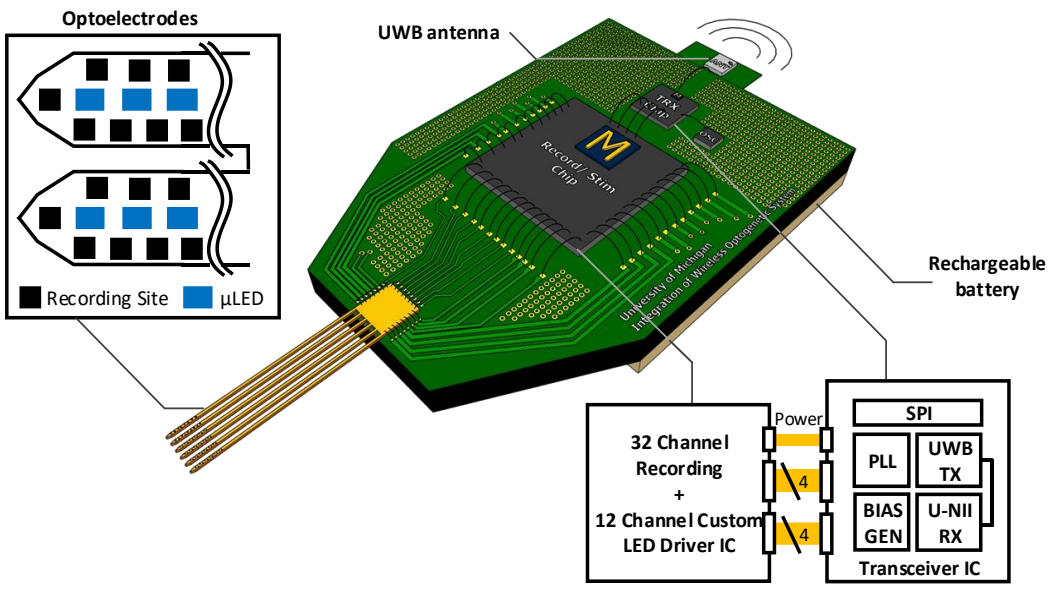



Figure 4-1 Proposed integrated wireless optogenetic system

To be able to conduct experiments with small rodents, the total weight of the system should be less than 3 gram or 30 gram for rats. With 0.64g, 3.7 volt, 25mAh rechargeable battery[73], the full integration should be able to record, stimulate and transmit data continuously for more than 1.5 hours, under the assumption that 1 LED channel is biased at 100µA, 10% duty-cycled stimulation. The proposed integration is shown in Figure 4-1. It includes the optoelectrode, one integration print circuit board (PCB), the recording/ stimulation chip [69], the B-TDD transceiver chip, an off-the-shelf antenna, one 4MHz crystal oscillator, and a rechargeable battery (shaded beige at the bottom of the PCB). The chips will be wire-bonded onto the PCB with gold and the interconnections will be realized with copper on PCB.

Figure 4-2 shows the block diagram of proposed system integration. As an expansion of previously published work [74], systematic interconnection and power distribution are put into consideration. As shown in the figure, the communication between two ICs is

based on serial peripheral interface (SPI), which is implemented in both chips while the one on transceiver chip serves as the master. Once the transmitted wireless signal from base station is demodulated by transceiver chip, it will initiate a communication link with the optogenetic chip and send $SCLK_{stim/rec}$, $CHIP\_EN_{stim/rec}$, $MOSI_{stim/rec}$ and $MISO_{stim/rec}$ signals to recording and stimulation blocks separately. For recording part, the digitized neural signal will be sent as $MISO_{rec}$ signal to the transmitter while any change of control will be sent as $MOSI_{rec}$ from the transceiver side. As for the stimulation part, $MOSI_{stim}$ signal will be sent from the receiver for stimulation commend and current parameters as well as $SCLK_{stim}$ and $CHIP\_EN_{stim}$ for communication purpose. One 200MHz clock signal is also sent to the stimulation block from the PLL, which is driven by an off-the-shelf 4MHz crystal oscillator.

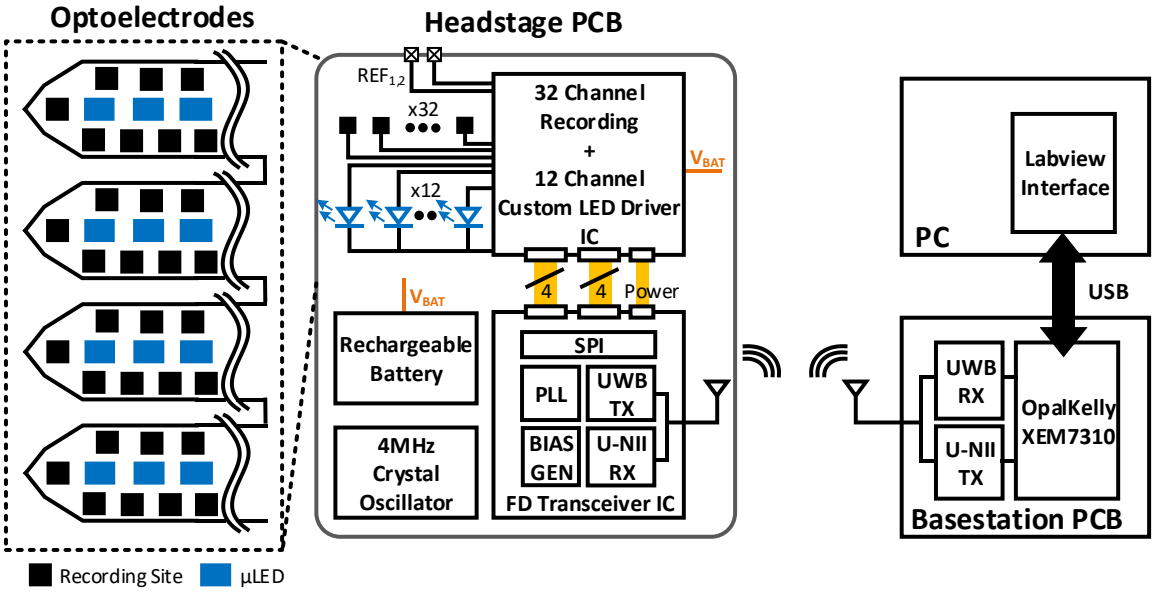



Figure 4-2 Proposed system integration block diagram, derived from [67]

The power source is realized by utilizing an off-the-shelf rechargeable battery[73]. The optogenetic chip is equipped with integrated low-dropout (LDO) linear regulators which serve as the power sources for the crystal oscillator, the optogenetic chip and the wireless transceiver chip. With the battery capacity of 25mAh, the full system should be able to run continuously for more than 3 hours, under the constraint of 1 LED channel is biased at 100μA, 10% duty-cycled stimulation. A 4- layer FR4 structure is adopted as the headstage PCB and the surface is specially treated with electroless nickel electroless palladium immersion gold (ENEPIG) for chip- on- board (COB) requirement. All the traces on PCB are specifically designed to match to 50 Ohms for transceiver chip if necessary. The total system weighs 3.7 gram, which will be suitable for small rodent experiment.

To pick up neuronal activities and deliver optical stimulation, a μLED-12-32-F flexible optoelectrode is adopted in the integration. The optoelectrodes are fabricated using gallium- nitride- on- silicon (GaN- on- Si), gallium nitride/ indium gallium nitride multi-quantum- well (GaN/ InGaN MQW) LED wafers with heavily boron- doped silicon(($p^+$- Si, $N^A \approx 1 \times 10^{20}$ $cm^{-3}$) substrates. It integrates 12 μLED with dimensions 10 x 16 μm each, 3 per shank and is able to emit light with peak wavelength of 460 nm and 40 nm for FWHM, as well as 32 recording channels distributed in 4 shanks, providing the electrode impedance of 100-1500 kΩ [75].

The base station is composed of a base station PCB, a wideband antenna and a PC. A UWB receiver composed of off-the-shelf components is implemented, as well as a U-NII band transmitter. An OpallKelly XEM 7310 board is mounted on the base station PCB to communicate with the LabView interface in PC via USB connection. The LabView

program controls the baseband digital signal, including the controlling commends to recording block and the current/ stimulation parameter to the simulation block, and also displays the demodulated neural signal from the headstage sent by the wireless transceiver chip.

### 4.4 Animal experiment methods

The animal procedures were approved by the Institutional Animal Care and Use Committee of the University of Michigan IACUC (protocol number: PRO-7275). One male C57BL/6J mouse (32 g) and one transgenic male mouse (JAX stock #007612) were used in this study. The mice were kept on a regular 12 h–12 h light–dark cycle and housed in pairs before surgery. No prior experimentation had been performed on these animals. AAV5, CaMKII promoter driven channel rhodopsin-2 (ChR2, AAV5-CaMKIIa-hChR2(H134R)-EYFP) virus was injected in CA1 region of the hippocampus of the wild type mouse, resulting in expression of ChR2 in pyramidal neurons. Atropine (0.05 mg/kg, s.c.) was administered after isoflurane anesthesia induction to reduce saliva production. The body temperature was monitored and kept constant at 36–37 °C with a DC temperature controller (TCAT-LV; Physitemp, Clifton, NJ, USA). Stages of anesthesia were maintained by confirming the lack of nociceptive reflex. Skin of the head was shaved and the surface of the skull was cleaned by hydrogen peroxide (2%). A 1 mm diameter craniotomy was drilled at 1.5 mm posterior from bregma and 2 mm lateral of the midline. The dura was removed over the dorsal CA1 region and virus was injected. Viruses were purchased from the University of North Carolina Vector Core [76]. After the surgery, the craniotomy was sealed with Kwik-Sil (World Precision Instruments) until the day of recording. On the day of recording, mice were anesthetized with isoflurane, the

craniotomy was cleaned (virus injected animal) or prepared (transgenic animal) and a 32-channel µLED silicon probe (32 recording channels and 12 LED) [77] was lowered to the CA1 region of the hippocampus. 15 min length of simultaneous recording and stimulation were performed using one µLED from one shank (all µLEDs were tested at least once). Our custom chip (OSC2P1) was used to record signals (n = 32 channels) and to deliver current pulses (n = 12 µLED).

### 4.4.1 Animal data processing

The recorded data were analyzed by custom scripts written in MATLAB (MathWorks, USA). Offline, spikes were detected and automatically sorted using the Kilosort algorithm (Pachitariu et al.) followed by manual curation using Phy (https://phy-contrib.readthedocs.io/) to get well-isolated single units (multi-unit and noise clusters were discarded). To measure the effect of LED stimulation on neuronal activity, peristimulus time histograms (PSTHs) were built around stimulus onset (spike trains were binned into 10-ms bins). Baseline and light-induced firing rate were calculated for each single unit. Baseline was defined as light-free epochs (500 ms) between trials and stimulation period as the light was on (5000 ms). Wilcoxon-signed rank test was used to compare the mean firing rate per trial (n = 43 trials) during baseline and LED stimulation.

## 4.5 Experiment results

Before realizing the full headstage scenario, an intermediate integration board is designed and tested to verify the functionality. An *in-vivo* session is also conducted to show the capability.

### 4.5.1 Intermediate integration stage

Figure 4-3 shows the intermediate integration PCB. A transceiver test PCB is designed to easily mount on the board, which communicates to FPGA and the recording and stimulation chip. The board has Omnetic connector to the left to connect to the testing probe via a cable for recording and optical stimulation. The size of the board is 220 mm by 220 mm.

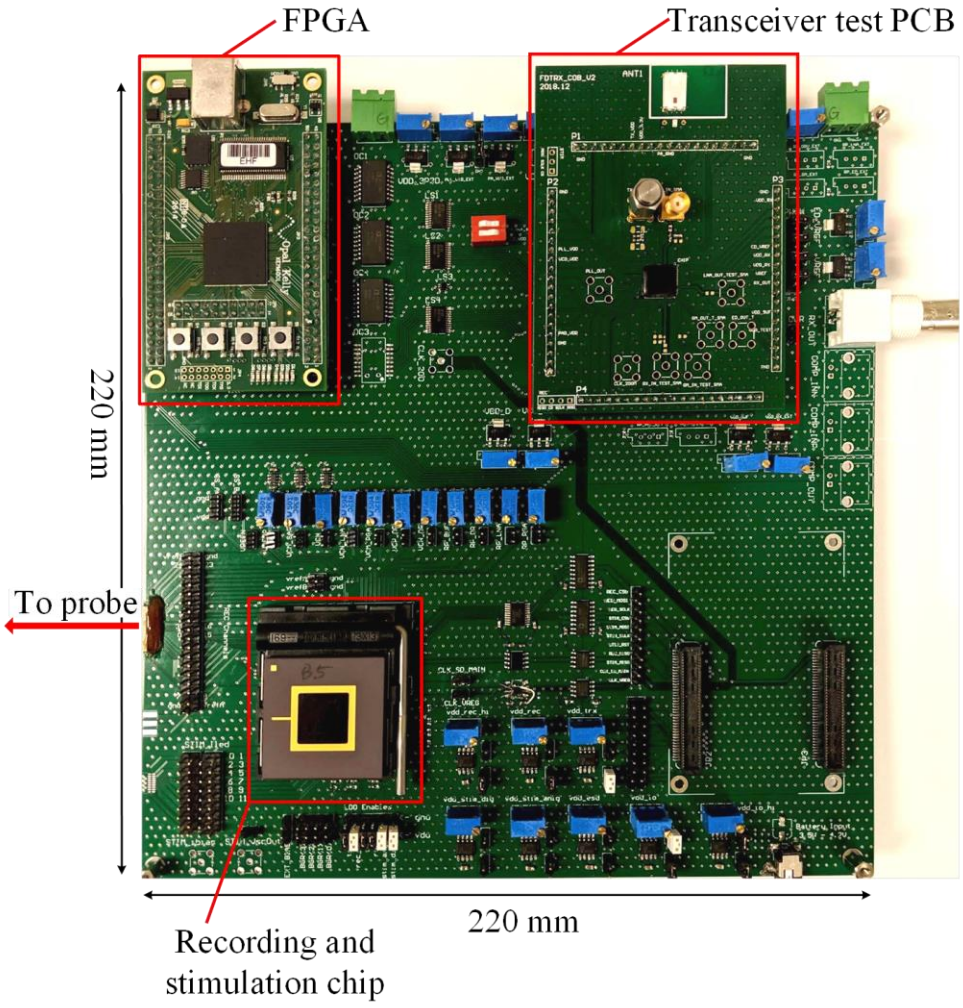



Figure 4-3 Intermediate integration PCB

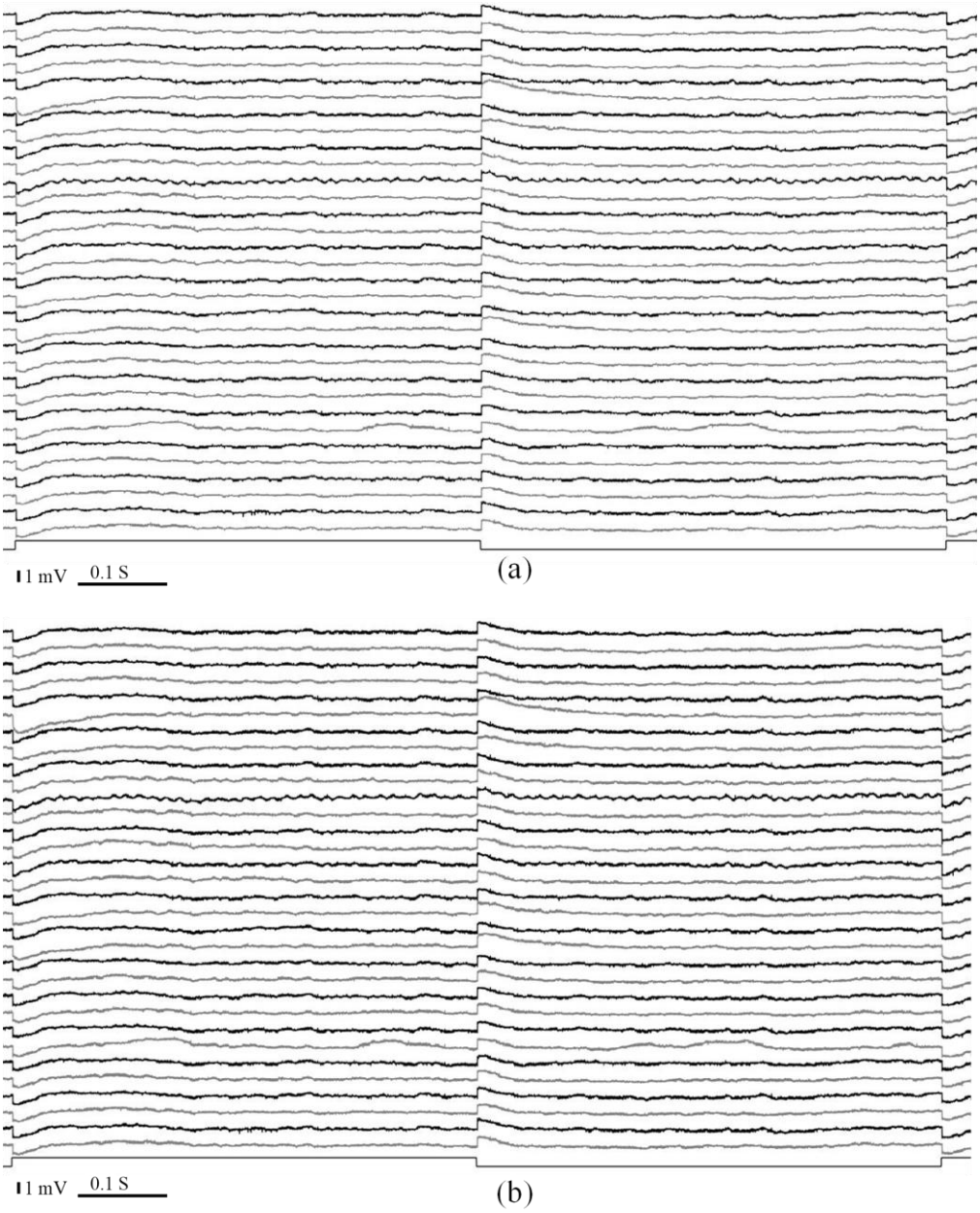



Figure 4-4 In-vivo testing result in transient on intermediate board of (a) recording chip output and (b) recovered signal from base station

Figure 4-4(a) shows the *in- vivo* transient response of the neuronal signal under the stimulation of 100 μA, 1Hz with 50% duty cycle from the ASIC output, while Figure 4-4(b) is the recovered signal from the base station. Figure 4-5 shows the experiment result after spike sorting and analysis. Figure 4-5(a) is the band passed filtered signal of

channel 2. Note the spiking activity and the simulation artifacts (asterisks). In (b) shows the mean waveform of a putative interneuron recorded on shank 2 while the error bar represents 1 standard deviation. The autocorrelation histogram of the single unit recorded in (b) is shown in (c).

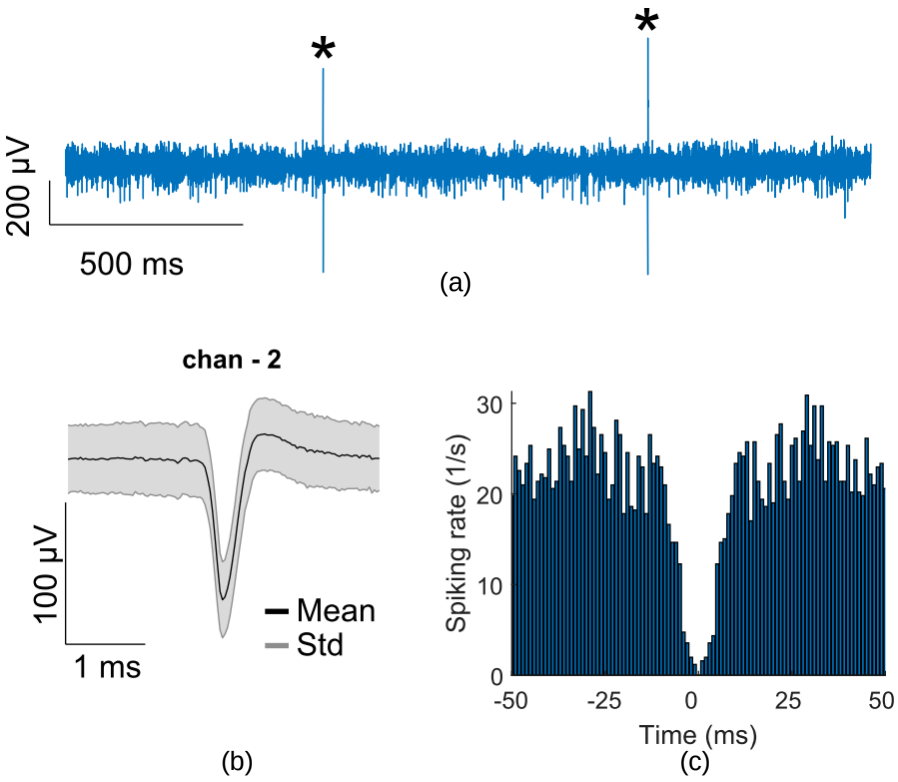



Figure 4-5(a) Bandpass filtered signal (500-8000Hz), (b) mean waveform of a putative interneuron and (c) autocorrelation histogram of the single unit in (b)

### 4.5.2 Small headstage integration

The headstage is shown in Figure 4-6 and Figure 4-7(a). It has both transceiver chip and 32/12- ASIC directly wire-bonded to the PCB. As proposed, commercially available antenna is on board, as well as the local oscillator and 25mAh battery which are installed in the back of the PCB. In the figure, the headstage is connected with the probe which has

32 channels of recording sites and 12 channels of μLED for optical stimulation. The same configuration is used in *in-vivo* experiment, as shown in Figure 4-7(c). The headstage PCB is 38mm by 17mm in size, the area reduction is more than 70x comparing to the intermediate board. The headstage weighs 3.7 g without battery and 5.0 g with battery, makes it suitable for rodent experiment.

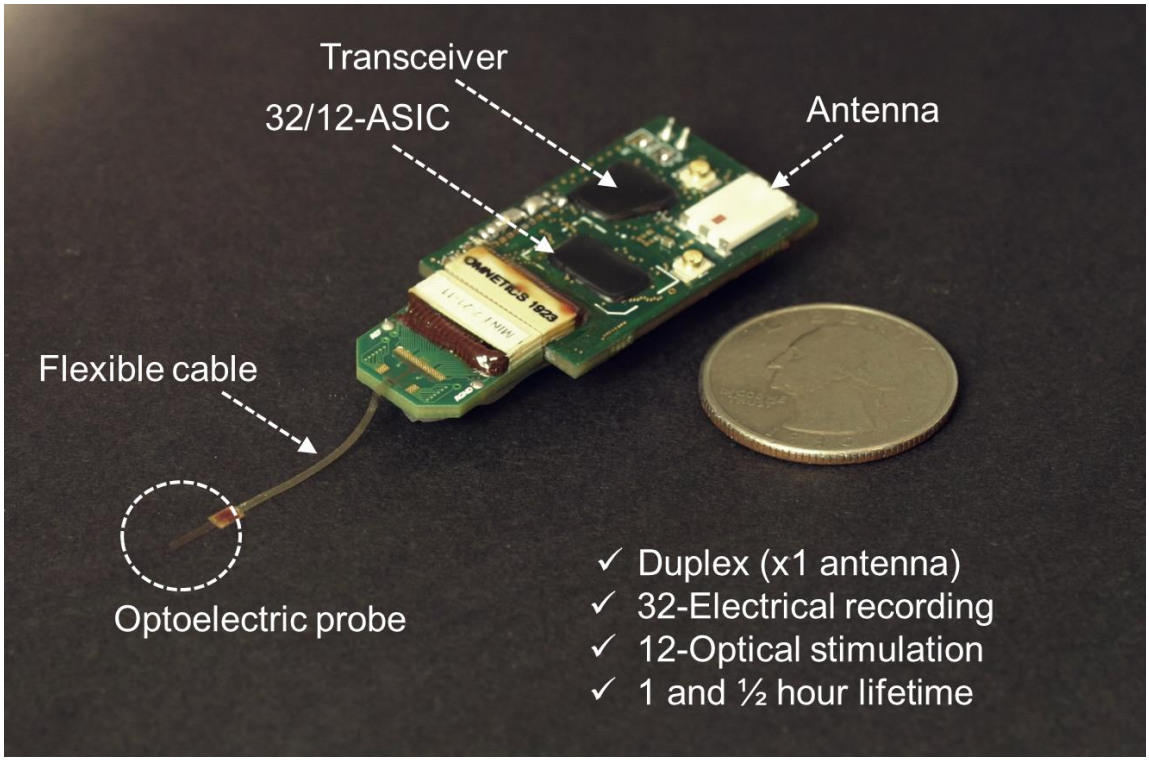



Figure 4-6 Small integration headstage

Figure 4-7(b) shows the *in-vivo* setup. The headstage is mounted on top of the transgenic mouse while the base station is 1 meter away. The headstage is operating solely on battery power as shown in Figure 4-7(c).

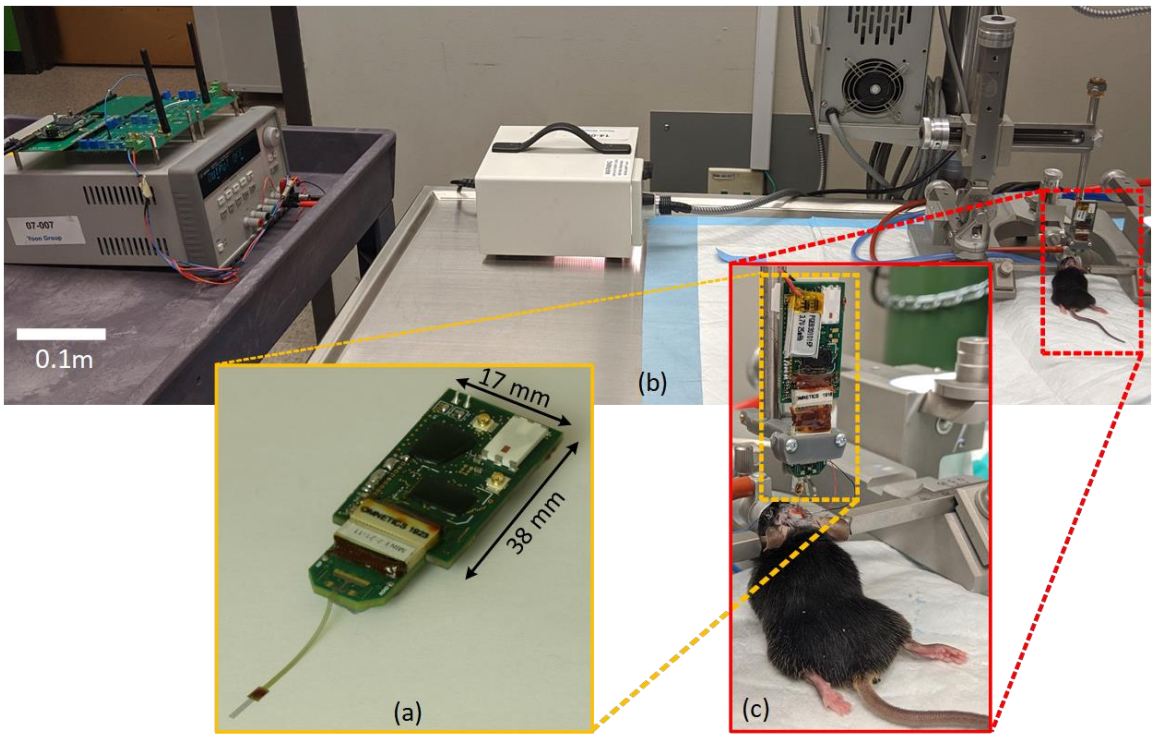



Figure 4-7 (a) Small integration board with probe, (b) In-Vivo setup and (c) enlarged headstage with transgenic mouse

The *in-vivo* result in transient is shown in Figure 4-8. While Figure 4-8(a) shows the ASIC output, the retrieved signal from base station is shown in Figure 4-8(b). 100 µA, 1 Hz with 50% duty cycle current is applied for µLED optical stimulation. With one meter of distance, the retrieved BER is below 0.1%.

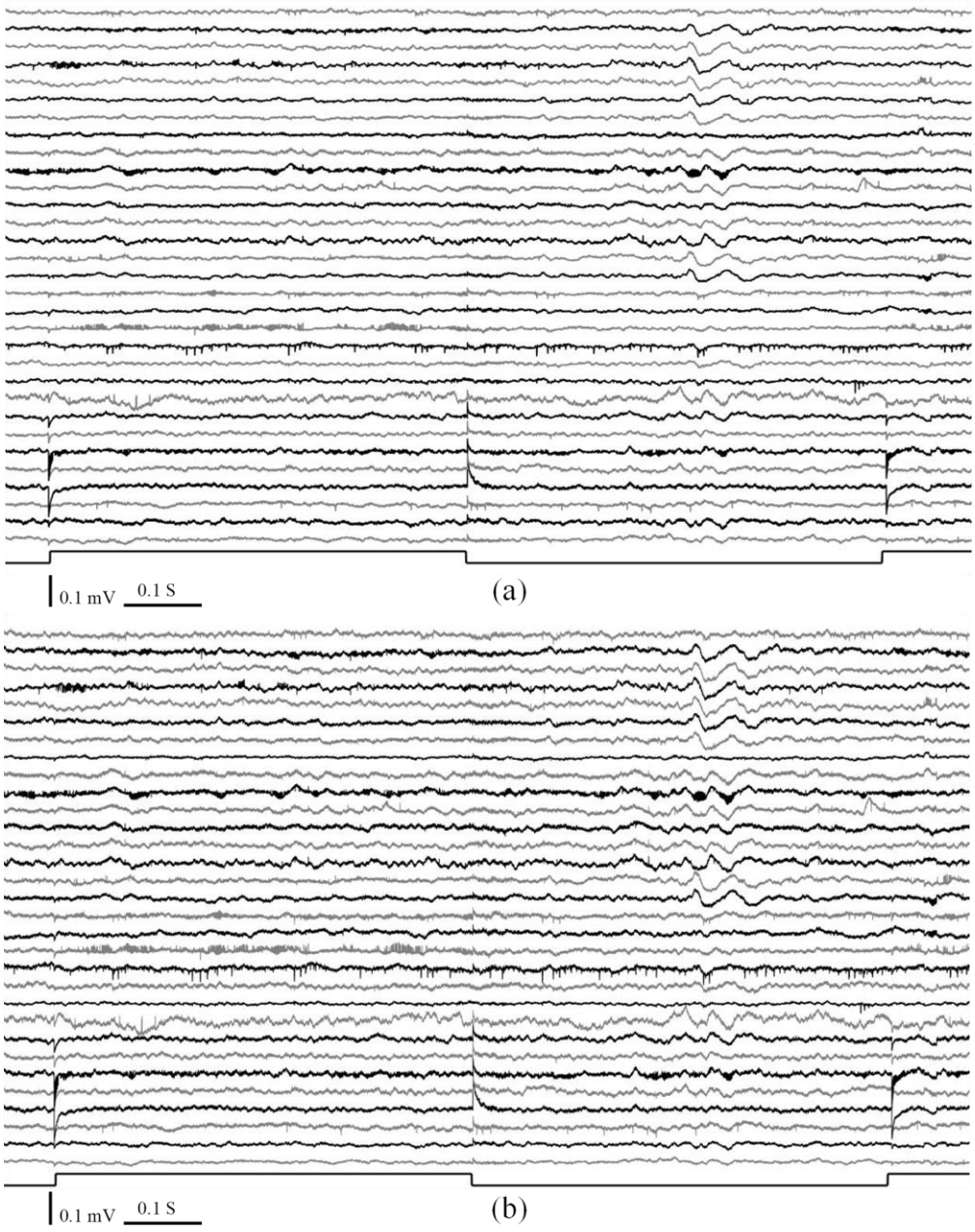



Figure 4-8 *In-vivo* testing result on small integration board of (a) recording chip output and (b) recovered signal from base station

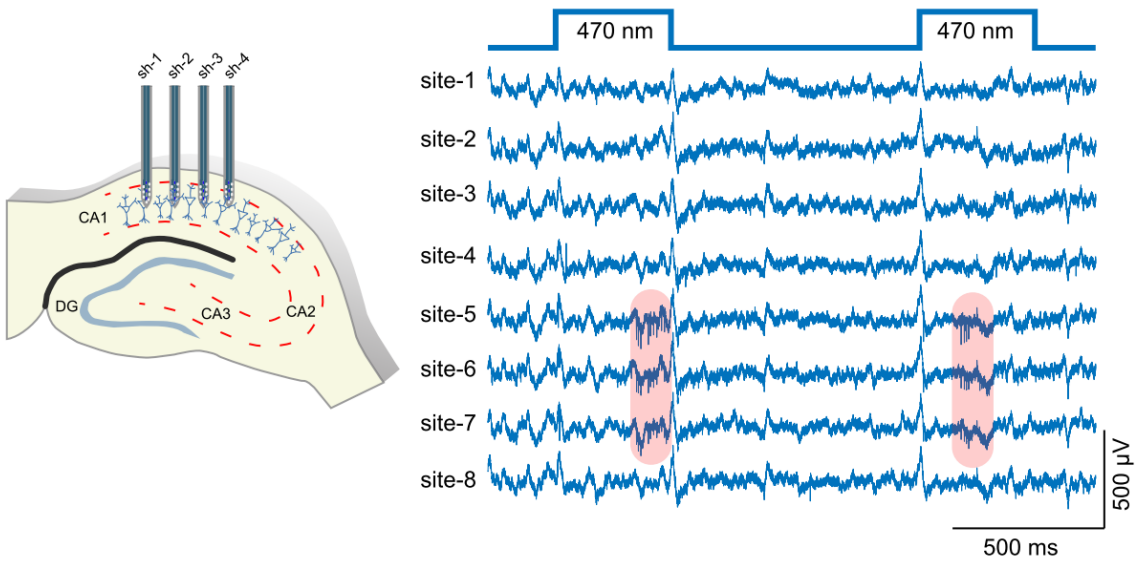



Figure 4-9 (a) Location of the µLED probe and (b) raw signal recorded on shank 3

Figure 4-9 (a) shows the location of µLED probe. The electrode was lowered to the CA1 region of the hippocampus where LED-2 on shank 3 was turned on at 100 µA, 1 second period and 30% duty cycle. Figure 4-9(b) shows the raw signal recorded on shank 3. 2 trials of the light induced neuronal effects are shown, the effect is highlighted in red. Light induced artifacts are also present in the raw data at stimulation onset and offset.

Figure 4-10(a) shows the details of shank 3 of the µLED probe. Note that LED-2 was illuminated during the example trances. Figure 4-10 (b) shows the high-pass filtered signal of Figure 4-9 (b) where $4^{th}$ order butterworth filter with 600 Hz cutoff corner is applied. Light-induced activity is highlighted in red.

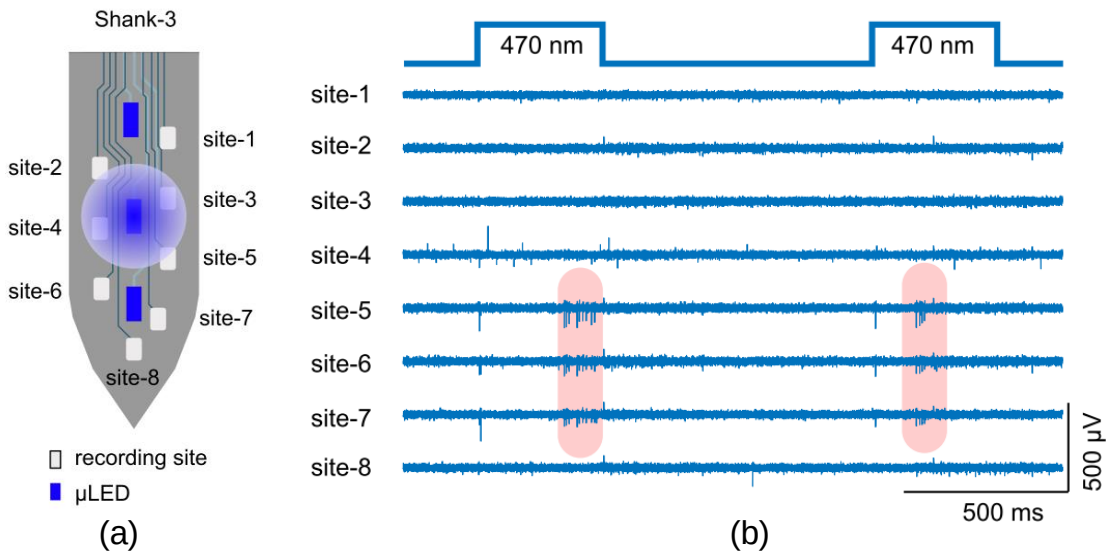



Figure 4-10 (a) Details of shank 3 and (b) high-pass filtered signal

## 4.6 Chapter conclusion

In this chapter, we have presented a full integration of a 32- channel recording, 12-channel optical stimulation ASIC with B-TDD wireless data telemetry onto a 38 mm x 17 mm headstage, together with the optogenic probe to show as a complete wireless system of implantable broadband optogenetic neural modulation and recording platform. The full system is operating on battery power and the total weight is under 5 g, which makes it suitable for rat experiment. The system is validated through *in-vivo* experiment at 1 meter distance with < 0.1% BER for wireless data transmission.

# CHAPTER 5
# Summary and Future Work

## 5.1 Summary

The goal of this research is to enable the high channel count neural signal recording and optogenetic stimulation with the aid of wireless data transmission to reduce the cable connection, realizing small form factor headstage module, as shown in Figure 4-1. To achieve the ultimate goal, power consumption, area constraint and weight limitation were all put into consideration in designing the final headstage.

First to overcome is the high speed data transmission for recording channels. A power efficient overlap-free feed-forward edge combiner based ultra- wide band transmitter is proposed and implemented. The work achieved state-of-the-art figure of merit in terms of the power efficiency with 4.32 pJ/b at 200 Mbps, while realizing overlap- free pulse generation which ensures the generated pulse is compatible with FCC compliance. The work is fabricated in 65 nm CMOS technology and applicable to accommodate 1,000-channel broadband neural signal recording and 10k-channel ECoG recording.

After one way communication is accomplished, bidirectional transmission is mandatory for sending commands for both recording and stimulation channels. With the constraints in power and area, a bit-wise time duplex transceiver is then developed. It utilizes the overlap in spectrum for UWB and U-NII band so that only one antenna is required. To avoid the power- hungry cancellation scheme, a bit-wise time division duplex structure is adopted. The transceiver module adopts asymmetric structure and B-

TDD scheme to realize real-time, closed-loop control, while maintaining ultra-low power consumption at 9.7 pJ/b in transmitter and 0.32 nJ/b in receiver. By sharing one antenna, it highly reduces the module area, enables compact implementation which is indispensable for high channel- count implantable neural interface applications.

The final product, integration of optogenetic stimulation and neural recording module with wireless data telemetry is so far vividly portrayed. A small headstage PCB is designed to accommodate the recording/ stimulation module and wireless transceiver is finally presented. The module weighs 3.7 g without battery and sizes 38.1 mm x 17mm, which is suitable for rodent experiment. The rechargeable battery can support the headstage continuously running for more than 3 hours at 100 μA, 10% duty cycled stimulating pulses. The headstage are tested with in-vivo experiment to verify the capability and the result is shown in chapter 4.

## 5.2 Future works

As the work presents full functionality for wireless optogenetic system, there are still improvements can be further pursue to make the system more robust and suitable for neural scientific studies. Here are a few suggestions:

- Wireless power transferring. As the data telemetry resolves the cable connection issue, the power source is still a concern. Although light-weight batteries are available in the market, the capacity and the weight are not ideal for implantable application. Many efforts have been put in the field of wireless power transferring. Due to the nature of our application, attempts in far- field transferring to improve the efficiency are very much desired as the size of the antenna plays an important role in implantable applications.

- Clock data recovery (CDR) circuit. Synchronization of the wireless data transmission can be realized in different ways, one of the most reliable is by adopting CDR. A CDR module integrated with the headstage transceiver will reduce the chance where the headstage needs to resynchronize with the base station, further cut down the data loss due to the resynchronization. With a CDR, the local oscillator on the headstage can also be eliminated for further area reduction and power cut.
- Full integration of transceiver and recording/ stimulation module. To prove the concept of wireless optogenetic system, two separate modules are wire-bonded onto the headstage PCB. As close as they can be with each other, the area between these two chips is still considered wasteful. Full integration of the two modules on the same die will be enticing, also make the headstage smaller and more applicable for small rodent experiments.

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