Photovoltaic Energy Harvesting for Millimeter-Scale Systems

by

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To my family

For their love and support

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Table of Contents

Dedication ii

Acknowledgements iii

List of Figures vi

List of Tables xvii

Abstract xviii

Chapter 1 Introduction 1

Chapter 2 Small-area Silicon Photovoltaic Cells 10

Chapter 3 Small-area GaAs Photovoltaic Cells 28

Chapter 4 Subcutaneous Phovoltaic Energy Harvesting 49

Chapter 5 Monolithic GaAs Photovoltaic Modules 66

Chapter 6 Vertical dual junction GaAs Photovoltaics 83

Chapter 7 Monolithically Integrated Microscale LED and Photovoltaic Module 99

Chapter 8 Conclusion and Futuer Works 115

Appendix 128

Bibliography 143

List of Figures

Figure

1.1. IoT^2 applications for biomedical, security, micro-robots and industrial monitoring (adopted from [1])……………………………………………………………………………...1

1.2. The standard terrestrial AM 1.5 solar spectrum……………………….……………...3

1.3. An equivalent circuit of the photovoltaic cell with parasitic resistances.……………..…...4

1.4. An example current and power versus voltage curves of the photovoltaic cell, illustrating the short circuit current, the open circuit voltage and the maximum power point…….……5

1.5. White and near infrared LED spectra compared with the solar spectrum…………………7

1.6. Comparison chart of illuminance from indoor to outdoor conditions (adopted [21])……..7

1.7. Conceptual illustration of subcutaneous photovoltaic energy harvesting through tissue…..8

2.1. Schematic illustration of conventional high-efficiency solar cell (adopted from [29])…...11

2.2. (a) Schematic illustration of device structure and (b) optical microscope image of a fabricated 1 mm^2 device……………………………………………………………12

2.3. Simulated power conversion efficiency under 100 nW/mm^2 illumination at 800 nm (dashed) and 850 nm (solid) for variable (a) base thickness and (b) base doping concentration...13

2.4. Simulated current–voltage characteristics of silicon photovoltaic cells with / without lightly doped emitter under 660 nW/mm^2 illumination at 850 nm…………………………...…14

2.5. Optical microscope images of the resulting DRIE isolation trenches……………….…...15

2.6. Measured current versus voltage characteristic of photovoltaic cell with 1 mm^2 under dark condition………...………………………………..…………………………….…….…18

2.7. (a) Extracted J0 and (b) diode ideality factors versus P/A (mm^{-1}) ratio from 1.4 mm^{-1} to 35.84 mm^{-1} corresponding device size from 10 mm^2 to 0.02 mm^2……………..………...18

2.8. Measured (solid) and simulated (dashed) current-voltage characteristics of photovoltaic cell under 660 nW/mm^2 illumination at 850 nm………………………………………19

2.9. Measured and simulated external quantum efficiency (EQE) characteristics for the 100 nm LPCVD Si_3N_4 passivated cell along with a surface reflectance curve (dashed) of cell between 375 nm and 1100 nm wavelength.…………………………………….………...20

2.10. Measured current versus voltage characteristics of different passivation layers for 10 mm^2 cell under 850nm LED illumination with 660nW/mm^2.…………………………..…21

2.11. Measured *J-V* under dark conditions for samples with different passivation layers………21

2.12. Measured *J-V* characteristics and corresponding conversion efficiency and comparison to device simulation with no surface and sidewall losses and an ideal Shockley–Queisser model…………………………………………………………………………..23

2.13. Measured power conversion efficiency versus NIR illumination for varying device passivation and comparison to commercial c-Si (IXYS Corporation: KXOB22-12X1, [42])……………………………………………………………………………………25

2.14. Measured fill factor versus NIR illumination for varying device passivation and comparison to commercial c-Si (IXYS Corporation: KXOB22-12X1, [42])…………….25

2.15. An equivalent circuit model of PV diode with parasitic series and shunt resistances……..26

2.16. Measured power conversion efficiency versus NIR illumination for varying device passivation and comparison to commercial c-Si. Simulated values using a diode model in (a) are shown assuming J0 and n values shown in the inset and varying shunt resistance in (Ω-cm^2)……………………………………………………………………27
3.1. Schematic diagram of conventional GaAs photovoltaic device structure…………………29
3.2. (a) Schematic diagram of optimized device structure, (b) Optical microscope image of fabricated GaAs PV cell at mm-scale………………………………………………30
3.3. Simulated (a) energy band diagram and (b) profile of photogeneration rate under illumination……………………………………………………………………31
3.4. Simulated maximum power density under 100 nW/mm^2 illumination at 800 nm and 850 nm versus variable base (a) doping concentration and (b) thickness……………………32
3.5. Measured current density versus voltage curves of different passivation studies of 6.4 mm^2 cell under (a) 850 nm NIR-LED illumination with 660 nW/mm^2 and (b) white LED illumination with 580 lux (1.38 μW/mm^2)………………………………………………34
3.6. Measured and Simulated (dashed) EQE characteristics of $(NH4)_2S$ + Si_3N_4 passivated sample along with the wavelength range between 400 nm and 900 nm…………………35
3.7. Measured power conversion efficiency values of various passivation studies versus P/A (mm^{-1}) ratio from 1.69 mm^{-1} to 55.56 mm^{-1} corresponding device size from 6.4 mm^2 to 0.0052 mm^2……………………………………………………………………36
3.8. Measured current versus voltage of 0.25 mm^2 cell under dark conditions………………37
3.9. Extracted reverse saturation current values of different passivation studies versus P/A (mm^{-1}) ratio from 1.69 mm^{-1} to 125 mm^{-1} corresponding device size from 6.4 mm^2 to 0.001 mm^2……………………………………………………………………………38

3.10. Extracted J_{02} parameters along with P/A Extracted J_{02} parameters along with P/A (mm^{-1}) ratio from 1.69 mm^{-1} to 125 mm^{-1}……………………………………………..…….39

3.11. Measured (solid) power conversion efficiency values under NIR illumination at a wavelength of 850 nm for the $(NH_4)_2S$ + Si_3N_4 passivated PV cell and for commercial c-Si solar cell [42] for comparison. Simulated (dashed) values varying shunt resistance in Ω-cm^2) are shown using extracted J_0 and n diode parameters shown in the inset.………..…41

3.12. Measured current density versus applied voltage characteristics with corresponding maximum power conversion efficiency and comparison to Shockley–Queisser model, device simulation with no surface and sidewall recombination losses and commercial silicon PV (IXYS Corporation: KXOB22-12X1, [42]) under (a) NIR illumination and (b) white LED illumination. …………………………………...….………………….…43

3.13. Measured fill factor versus variable (a) NIR and (b) white LED illumination conditions, compared to commercial c-Si cell (IXYS Corporation: KXOB22-12X1, [42]) and our custom silicon PV cell (discussed in Chapter 2) with well-optimized LPCVD Si3N4 passivation……………………………………………………………………………..44

3.14. Comparison with calculated (dashed) and measured V_{OC} values for square GaAs cells with varying the sidewall length. …………...…………………………………………..…..45

3.15. Comparison with calculated (dashed) and measured J_{SC} values for square GaAs cells with varying the sidewall length, assuming the fixed EQE around 80 % for theoretical calculation……………………………………………………………………………..46

3.16. Comparison with calculated (dashed) and measured power conversion efficiency values for square GaAs cells with varying the sidewall length……………………..…………47

3.17. Measured efficiency versus variable NIR LED illumination conditions, compared to commercial c-Si cell (IXYS Corporation: KXOB22-12X1, [32]) and our custom silicon PV cell (discussed in Chapter 2) with well-optimized LPCVD Si_3N_4 passivation.........48

4.1. The light propagation and the optical properties of biological tissues (adopted from [79,81])..........51

4.2. Optical properties of biological tissues, illustrating the optical transparency windows in NIR wavelength ranges (adopted from [20])..........52

4.3. Measured temperature of post-craniotomy subdural feline brain tissue under 850 nm NIR irradiation over 10 min exposure..........53

4.4. Current density versus voltage curves of silicon and GaAs photovoltaic cells under 1.06 μW/mm^2 at 850 nm wavelength and 25 ℃..........55

4.5. External quantum efficiency spectra of silicon and GaAs photovoltaic cells..........56

4.6. Current density versus voltage curves of silicon and GaAs photovoltaic cells and comparison to Shockley–Queisser model under 1.06 μW/mm^2 at 850 nm wavelength.....57

4.7. Temperature dependence of power density versus voltage ranging from room temperature (25 ℃) to conventional body temperature (37 ℃) for (a) Silicon and (b) GaAs............58

4.8. Measured transmittance versus thickness of porcine skin and chicken breast under 1.08 μW/mm^2 at 850 nm wavelength..........59

4.9. Power conversion efficiency versus thickness of porcine skin and chicken breast for (a) Silicon and (b) GaAs photovoltaic cells under 1.08 μW/mm^2 at 850 nm wavelength.......60

4.10. Output power versus input power plots for (a) Silicon and (b) GaAs photovoltaic cells through 5 mm porcine skin and 10 mm chicken breast along with minimum 50 nW/mm^2

operating power of low-power microelectronics and minimum 10 μW/mm^2 low-level light therapy (LLLT)……………………………………………...…………………..62

4.11. Photo of dissected mouse and mounted PV cells used to measure NIR energy harvesting…………………………………………………………………...…63

5.1. Schematic diagrams of (a) a switched capacitor network and (b) a bulk off-chip inductor for the DC-DC voltage up-conversion (adopted from [92])…….……..……………...…..67

5.2. Schematic diagrams of (a) device structure illustrating PV cell junction, junction barrier isolation, and shunt leakage path, and (b) equivalent circuit model of the PV module…...68

5.3. Optical microscope images of two different fabricated PV modules……………….……....69

5.4. Measured *J*-*V* characteristics of PV modules with GaAs and AlGaAs barrier layers (a) under 850 nm NIR LED illumination at 1.02 μW/mm^2 and (b) under white LED illumination at 586 lux. Comparisons are shown to simulated results (dashed) with shunt leakage removed…………………………………………………...…………..71

5.5. Measured *J*-*V* curves for varying number of PV cell series connection and (inset) corresponding power conversion efficiency at the maximum power point……..…..…..72

5.6. Schematic diagram of shunt leakage measurement between bottom n-contacts of adjacent PV cells..……………………………………..………………………...…...73

5.7. Measured shunt leakage current under (a) dark and (b) NIR illumination conditions for three different barrier structures: no barrier, p-GaAs junction, and p-$Al_{0.3}Ga_{0.7}As$ junction…………………………………………………………………………..74

5.8. Simulated energy band diagrams between the PV cell base and semi-insulating substrate under dark conditions for three different barrier layer structures: no barrier, p-GaAs junction, and p-$Al_{0.3}Ga_{0.7}As$ junction…………………………………………….…75

5.9. Comparison of measured *P-V* characteristics between PV arrays and single PV cell (a) under 850 nm NIR illumination at 1.02 μW/mm^2 and (b) under white LED illumination at 586 lux……………………………………………………………..…………………..77

5.10. Light intensity dependence of (a) power conversion efficiency and (b) fill factor for single PV and PV modules with p-GaAs and p-AlGaAs barrier junction isolation under NIR illumination...78

5.11. Light intensity dependence of (a) power conversion efficiency and (b) fill factor for single PV and PV modules with p-GaAs and p-AlGaAs barrier junction isolation under white LED illumination…...……79

5.12. Optical microscope images of a wireless mm-scale sensor system with integrated PV module (a) before and (b) after encapsulation…………………….……………...………80

5.13. Monitored battery voltage output of this mm-scale system during the charging process under 110 lux indoor illumination……………………………………………………..81

6.1. Schematic illustration of (a) monolithically grown and (b) mechanically stacked multi-junction device structures (adopted from [104,106])………...……………….………..85

6.2. Schematic diagrams of (a) single dual-junction PV cell and (b) dual-junction PV module illustrating PV cell junction, junction barrier isolation, and shunt leakage path……..…85

6.3. Simulated current voltage characteristics of dual junction cells with variable thickness of a top cell under 850 nm NIR illumination at 1 μW/mm^2……………………………………86

6.4. Simulated external quantum efficiency (EQE) spectra for different thickness of top PV cells in the dual-junction structure with the fixed thickness of bottom PV cell at 3.5 μm…87

6.5. Comparison of simulated *J-V* characteristics between single-junction and dual-junction PV cells under 850 nm NIR illumination at 1 μW/mm^2…………………………...………88

6.6. Optical microscope image of fabricated dual junction PV cell at μm-scale……..………89

6.7. Measured *J-V* and *P-V* characteristics of fabricated dual junction PV cells with 6.4 mm^2 size under 2.02 $\mu W/mm^2$ NIR illumination at wavelength of 850 nm…………….……..90

6.8. Measured *J-V* and *P-V* characteristics of fabricated dual junction PV cells with 150 μm x 150 μm size under 2.02 $\mu W/mm^2$ NIR illumination at wavelength of 850 nm………..…91

6.9. Optical microscope images of two different fabricated DJ PV modules that have 4 and 8 cells connected in series……………………………………..…………………...91

6.10. Measured *J-V* and *P-V* characteristics of PV modules with 4 cells in series……..……..92

6.11. Measured *J-V* and *P-V* characteristics of PV modules with 8 cells in series…...................93

6.12. Comparison of measured J-V characteristics between DJ and SJ PV cells under 850 nm NIR illumination at 6.62 $\mu W/mm^2$……………….………………………..….…………..…94

6.13. Measured EQE spectra of DJ and SJ PV cells and comparison with simulated EQE spectrum of DJ PV cell……………………………………………………….……..…95

6.14. Comparison of measured *J-V* characteristics between SJ (8 cells in series) and DJ (4 cells in series) PV arrays under 850 nm NIR illumination at 2.02 $\mu W/mm^2$……………………96

6.15. Comparison of measured *J-V* characteristics between SJ (8 cells in series) and DJ (8 cells in series) PV arrays under 850 nm NIR illumination at 2.02 $\mu W/mm^2$……………………96

7.1. Conceptual illustration of a full system for recording and transmitting the neural signals and a PV / LED module in the system for NIR wireless power transfer and data communications (Drawn by Jongyup Lim)……………………………………………..100

7.2. Experiment set up for measuring the NIR optical transmittance through the dura samples using laser and LED illumination sources……………………...…………………….102

7.3. Measured NIR transmittance through post-craniotomy feline dura samples under 850 nm laser illumination……………………………………..………………………….……..102

7.4. Measured NIR transmittance through post-craniotomy NHP dura samples under 850 nm, 970 nm and 1050 nm NIR LED illumination………………………………..………..103

7.5. Schematic diagram of monolithically integrated µ-LED / PV module illustrating tandem junction of PVs and junction barrier isolation between LED and PV…………..……….104

7.6. Optical microscope image of fabricated LED / PV module at µm-scale…………….…..104

7.7. Measured *I-V* and *P-V* characteristics of dual junction PV cell under 850 nm NIR LED illumination at 100 µW/mm^2…………………………………………………………....105

7.8. Monte-Carlo simulation of NIR emission from a µ-LED through dura to the SPAD repeater, with estimated efficiency of 0.1% (photons received at SPAD with 100 µm diameter relative to photons emitted from LED) (Simulated by Michael Barrow) ……...106

7.9. Measured *I-V* characteristic of fabricated LED with 50 µm x 50 µm size……………….107

7.10. Measured photoluminescence (PL) versus wavelength curve of fabricated LED with 50 µm x 50 µm size……………………………………………………………………...…108

7.11. Measured light output versus applied current curve of fabricated LED with 50 µm x 50 µm size……………………………………..……………………………..…………108

7.12. Detected SPAD output (10 µs deadtime) versus LED input pulses (40 µs pulse width, 100 µs period, 1.54 applied voltage) (Collaborating with Jongyup Lim)………..………….109

7.13. Measured *I-V* characteristics of PV cell before / after the shared connection to LED cathode under 850 nm NIR LED illumination at 150 µW/mm^2…………………….……..…….110

7.14. Measured leakage current between LED cathode and PV anode with / without the isolation trench………………………………………...………………………...……..111

7.15. Measured *I-V* characteristics of PV cell with / without the isolation trench under 850 nm NIR LED illumination at 150 μW/mm^2……………………………...……………….111
7.16. Extracted EQE versus applied current curves of variable size LEDs……………………112
7.17. (a) Measured temperature dependent photoluminescence spectra of InGaAs LED and (b) extracted peak intensity values versus variable temperature from 300 K to 13 K (collaborating with Anthony Aiello)…………………………………………...….113
8.1. Cross-sectional concept diagram of the integration of GaAs PV / LED modules, silicon chips and neural probe……………………………………………………………..…116
8.2. Schematic diagrams for (a) the front side and (b) back side of GaAs PV / LED module for the vertical integration, illustrating the through wafer via, interconnects and back contacts……………………………………….……………..………………117
8.3. (a) Microscope and (b) scanning electron microscopy (SEM) images of through wafer vias of GaAs, deeper than 50 μm……………………………………………………..117
8.4. (a) An image of the thinned GaAs wafer mounted to the flexible tape and (b) a microscope image of the backside of thinned wafer, exposing the TWVs and predefined alignment mark……………………………………………………………………………….118
8.5. (a) An optical microscope image of backside of thinned GaAs with TWVs, and (b) electrical characteristics measured through two GaAs TWVs in series (collaborating with Michael Barrow)…………………………………..……………..…………....118
8.6. Photon detection probability along with wavelengths at different excess bias at room temperature (adopted from [122])…………………………….……………………..120
8.7. Optimized device parameters of DH AlGaAs LED with the emission wavelength at 780 nm………………………………………..……………..……...…….……..120

8.8. (a) Simulated current versus voltage characteristics and (b) IQE versus voltage curves of DH AlGaAs LED, compared to InGaAs QW LED…………………………………..…121

8.9. Simulated EQE spectra for variable aluminum mole fraction of top PV cells in the DJ structure with the fixed thickness of top PV cell at 400 nm and comparison with the normalized spectrum of commercialized white LED with 3000 K color temperature…..123

8.10. Figure. 8.10. Simulated J-V characteristics of dual junction cells with variable aluminum mole fraction of a top cell under white LED illumination (3000 K color temperature) at 1 μW/mm^2…………………………………………………………………….……..…..123

List of Tables

Table

1.1. Energy harvesting sources for wireless power transfer (adopted from [7])……..……..…..2

2.1. Optimized device parameters under 850 nm NIR illumination at 100 nW/mm^2…………14

2.2. Extracted diode parameters of 10 mm^2 cells using 1 diode equation (1)...........................22

2.3. Device size dependence on device parameters of LPCVD passivated cells………..…..…24

3.1. Extracted diode parameters of 6.4 mm^2 cells from 1-Diode equation………………..…..38

3.2. Extracted diode parameters from a 2-Diode equation……………………..……..………..40

4.1. Optimized device parameters of silicon and GaAs PV cells for NIR wavelength……..…54

4.2. Parameters measured at various locations on the mouse sample…………….………..…..64

6.1. Optimized device parameters of dual junction PV cell and module, designed for NIR wavelength at 850 nm…………………………………………………………...……..88

6.2. Comparison of measured device performances between DJ and SJ PV cells under 850 nm NIR illumination at 6.62 µW/mm^2………………………………………..……..…..94

6.3. Comparison of measured device performances between SJ and DJ PV modules with 4 and 8 cells in series under 850 nm NIR illumination at 6.62 µW/mm^2………………….97

Abstract

The Internet of Things (IoT) based on mm-scale sensors is a transformational technology that can be applied to a wide range of applications for biomedical devices, surveillance, micro-robots and industrial monitoring. Energy harvesting approaches to power IoT have traditionally utilized thermal energy, mechanical vibrations and radio frequency electromagnetic radiation. However, the achievement of efficient energy scavenging for IoT at the mm-scale has been elusive. Here I show that photovoltaic cells at the mm-scale can be an alternative means of wireless power transfer to mm-scale sensors for IoT, utilizing ambient indoor lighting or intentional irradiation of near-infrared (NIR) LED sources through biological tissues, where the power conversion efficiency is limited by sidewall / perimeter recombination losses and shunt resistance.

First, I show that silicon photovoltaic cells at the mm-scale can achieve a power conversion efficiency of more than 17 % under 850 nm NIR irradiation at 1 μW/mm^2 using the optimized sidewall passivation studies using LPCVD Si_3N_4 without the concern of shunt leakage degradation. However, fundamental material characteristics of silicon such as higher dark current limit the open circuit voltage and corresponding power conversion efficiency.

On the other hand, GaAs based PV cells have a possibility to boost the energy harvesting efficiency under low-flux conditions due to superior optical properties, range of tunable bandgap energies, low dark current, a large shunt resistance in comparison to crystalline silicon photovoltaic cells. GaAs photovoltaic cells at the mm-scale can achieve a power conversion efficiency of more than 30 % under 850 nm NIR irradiation at 1 μW/mm^2 and around 20 % under white LED

illumination at 580 lux, which guarantees perpetual operation of mm-scale sensors.

The practical requirements of subcutaneous photovoltaic energy harvesting in terms of the optical properties of biological tissues, near-infrared transmittance of various tissue samples, the maximum exposure limit, and the body temperature effect are explored. Our results demonstrate that external infrared energy harvesting from ambient sources or intentional irradiation are sufficient to power mm-scale sensor systems utilizing silicon or GaAs PV cells that are specifically designed and optimized for energy harvesting in the NIR transparency window for biological tissue. Sufficient power generation is achieved for perpetual operation of mm-scale systems for implant depth of at least 15mm including hair / skin / muscle / bone under NIR illumination at 850 nm.

Furthermore, monolithic GaAs photovoltaic modules offer an efficient means for energy harvesting and direct battery charging in mm-scale systems. I demonstrated GaAs PV modules at the mm-scale with high efficiency under low-flux conditions, where AlGaAs junction barrier isolation provided a critical step in limiting shunt leakage current between series connected cells. We observed power conversion efficiency of 26.3 % under 850 nm infrared LED illumination at 1.02 μW/mm2 and 16.3 % under white LED illumination at 586 lux (1.4 μW/mm2), with a 90 % voltage up-conversion efficiency to reach an operating voltage of 5 V for direct battery charging.

Dual-junction GaAs photovoltaic cells and modules at sub millimeter scale are demonstrated for efficient wireless power transfer for Internet of Things (IoT) and bio-implantable applications under monochromatic illumination. The dual-junction approach meets demanding requirements for these applications by increasing the output voltage per cell with reduced area losses from isolation and interconnects. A single PV cell (150 μm x 150 μm) based on the dual-junction design demonstrates power conversion efficiency above 22 % with greater than 1.2 V

output voltage under low-flux 850 nm near-infrared LED illumination at 6.62 μW/mm^2, which is sufficient for batteryless operation of miniaturized CMOS IC chips. The output voltage of dual junction PV modules with 8 series-connected cells demonstrates greater than 10 V for direct battery charging while maintaining a module power conversion efficiency of more than 18 %.

Finally, I demonstrate monolithic PV / LED modules at the μm-scale for brain-machine interfaces, enabling two-way power and data transfer in a through-tissue configuration. The dual junction GaAs PV cell provides sufficient power (~ 1 μW) and voltage (> 1.4 V) for battery-less operation of CMOS circuitry under 850 nm NIR illumination at 100 μW/mm^2 within the tissue exposure limit. The monolithically integrated InGaAs μ-LED emits NIR light pulses at detectable power levels (> 1 nW) under realistic energy harvesting levels from PV cells, where we have demonstrated example digital pulse detection with a single photon avalanche photodiode (SPAD). The wafer-level assembly plan for the 3D vertical integration of GaAs LED / PV modules, CMOS silicon chips, and neural probes is proposed, using the through-wafer via, wafer thinning, flip chip bonding, laser dicing, and final packaging.

CHAPTER 1

Introduction

1.1. Internet of Things (IoT)

The Internet of Things (IoT) is a transformative technology that can be applied for a variety of applications [1-2], which interconnects individual objects and devices to a network without human interfaces. Furthermore, continued scaling of electronic systems, and the proliferation of wireless mm-scale sensor networks have enabled a paradigm shift referred to Internet of Tiny Things (IoT^2) [1-2]. These unique features of IoT^2 with small form factors at mm-scale open new capabilities of various applications for biomedical, security, micro-robots and industrial monitoring as shown in Fig. 1.1.

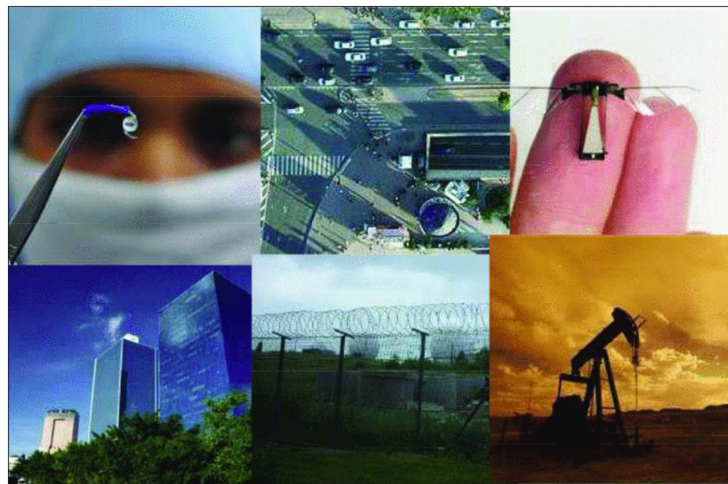


Figure 1.1. IoT^2 applications for biomedical, security, micro-robots and industrial monitoring (adopted from [1]).

1.2. Wireless power transfer for the IoT^2

The IoT^2 necessitates a means of energy harvesting from ambient and stable sources to achieve self-powered devices with small form factors at mm-scale. Several different energy sources utilizing thermal energy [3], mechanical vibrations [4] and radio-frequency (RF) electromagnetic radiation [5-6] have been evaluated and tested as shown in Table 1.1, though miniaturization and reliability / stability of the ambient sources are still primary limiting factors. Photovoltaic energy harvesting provides an alternative means of wireless power transfer to these miniaturized low-power systems using ambient or intentional illumination sources, where the power requirement of mm-scale sensors for the energy-autonomous operation is roughly 10 μW (active) and 0.5 nW (standby), respectively [8-11].

Power Source	Power Density
Photovoltaics (outdoors)	15,000 μW/cm^2
Photovoltaics (indoors)	10 μW/cm^2
Thermoelectric (5 ^{o}C gradient)	40 μW/cm^2
Piezoelectric (shoe inserts)	330 μW/cm^3
Vibration (building)	300 μW/cm^3
Ambient radio frequency	< 1 μW/cm^2

Table 1.1. Energy harvesting sources for wireless power transfer (adopted from [7]).

1.3. Basic characteristics of photovoltaic cells

1.3.1 Photovoltaic effect

The photovoltaic effect refers to the conversion process of light energy into electrical energy. Light from sun or other sources is electromagnetic radiation or photons whose energy is

determined by the wavelength of light from the equation (1)

$$E = \frac{hc}{\lambda} \tag{1}$$

where h is Planck's constant, c is the speed of light and λ is the wavelength. For example, the sun emits light with a wide range of wavelengths from ultraviolet (UV) to infrared (IR) ranges. The spectrum reaching to the Earth is absorbed and scattered through the atmosphere and its intensity is dependent on the angle of incident. The standard spectrum is called Air Mass (AM) 1.5 [12] as shown in Fig. 1.2 when the sun is at the elevation angle of 42°, which has the integrated intensity at 1 mW/mm^2.

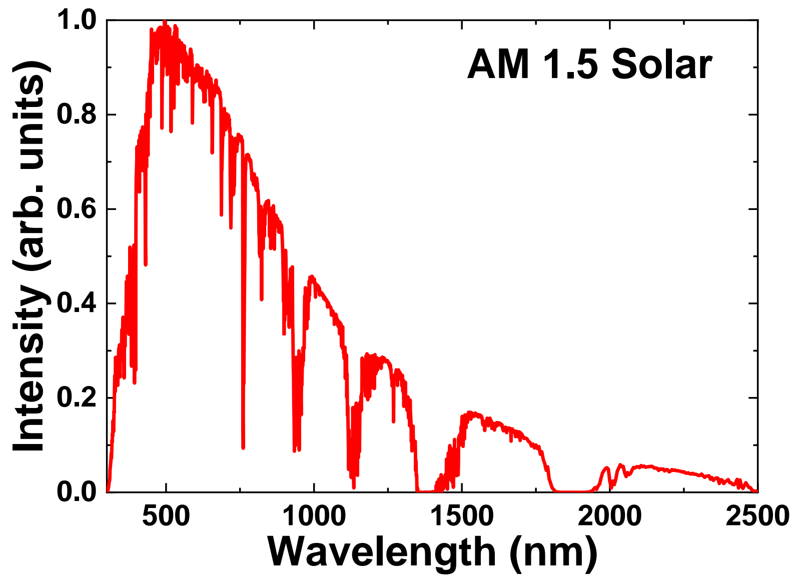


Figure 1.2. The standard terrestrial AM 1.5 solar spectrum.

1.3.2. Basic operation of photovoltaic cells

Photovoltaic cells usually based on p-n junction diodes absorb the incident photons above the bandgap and generate the electron-hole pairs that diffuse toward the junction. The generated carriers are separated and collected to the external circuit, generating the electrical power. The generated photocurrent is described by following equation (2)

$$J_{SC} = q \int b_s(E) QE(E) dE \quad (2)$$

where b_s is the incident spectral photon flux density, *QE* is the quantum efficiency. QE is a key parameter for the operation of photovoltaic cells, relevant to the efficiency of absorption, separation, and collection of carriers. Under the dark condition, photovoltaic cells behave like a normal rectifying diode in opposite direction to the photocurrent following the equation (3)

$$J_{dark}(V) = J_0(e^{qV/kT} - 1) \quad (3)$$

where V is the applied voltage, J_0 is the reverse saturation current, k is Boltzmann's constant and T is temperature. The equivalent circuit of the photovoltaic diode is illustrated in Fig 1.3.

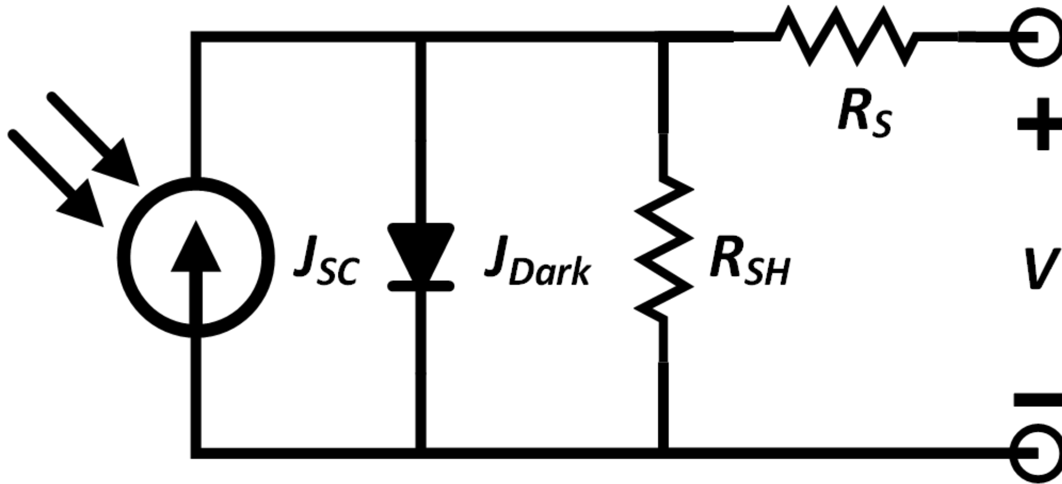


Figure 1.3. An equivalent circuit of the photovoltaic cell with parasitic resistances.

The total current of photovoltaic cells from the superposition approximation as is described by following equation (4).

$$J(V) = J_{SC} - J_{dark}(V) = J_{SC} - J_0(e^{qV/kT} - 1) \quad (4)$$

For the open-circuited diode ($J = 0$), the maximum potential difference called the open circuit voltage (V_{OC}) is obtained, which is given by the equation (5).

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{J_{SC}}{J_0} + 1\right) \quad (5)$$

The output power is given by the equation (6)

$$P = JV \tag{6}$$

where P has the its maximum (P_m) at the maximum power point. Another important parameter is the fill factor, describes the squareness of the J-V curve using the equation (7).

$$FF = \frac{P_m}{J_{SC} V_{OC}} \tag{7}$$

The power conversion efficiency (η_C) of the photovoltaic cell is defined by the equation (8)

$$\eta_C = \frac{P_m}{P_{in}} \tag{8}$$

where P_{in} is the incident power density.

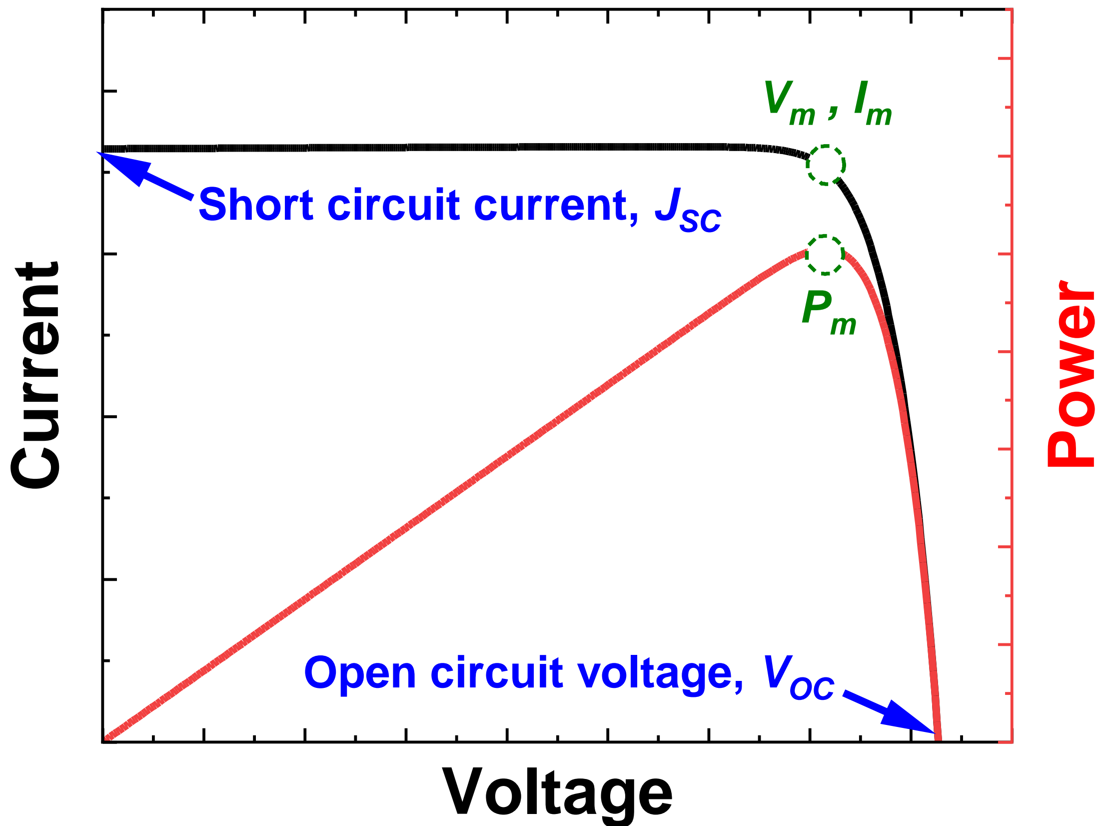


Figure 1.4. An example current and power versus voltage curves of the photovoltaic cell, illustrating the short circuit current, the open circuit voltage and the maximum power point.

1.3.3. Parasitic resistances

In the actual photovoltaic cell, parasitic series and shunt resistances as show in Fig. 1.3 can degrade cell performance. The parasitic resistance components for a photovoltaic cell are described by the equation (9)

$$J = J_{SC} - J_0 \left[\exp\left(\frac{q(V+JAR_s)}{nkT}\right) - 1\right] - \frac{V+JAR_S}{AR_{sh}} \quad (9)$$

where J_{SC} is the short-circuit current density, and R_S and R_{SH} are series and shunt resistance, respectively. The series resistance is related to the resistance of the cell material and contacts, governing the device operation at high current densities under high-flux outdoor or concentrated conditions. The shunt resistance relevant to the leakage of current through the cell or sides becomes increasingly important under low-flux conditions where short-circuit current values are small.

1.4. Photovoltaic energy harvesting for the IoT[2]

Photovoltaics are well known for efficient large scale power generation and for their use in self-powered electronic devices at the macroscale. While the physical dimensions of PV devices and systems may be reduced, miniaturization to the mm-scale present new challenges in achieving high conversion efficiency. Furthermore, sources such as ambient indoor lighting or infrared radiation for wireless power transfer differ dramatically from solar irradiance in terms of both spectral content and flux [13-16] as shown in Fig. 1.3, 1.4 and 1.5. Dark current and shunt conductive paths in photovoltaic cells become much more important at small dimensions and low flux ambient indoor or subcutaneous conditions [13-18] in comparison to typical outdoor solar irradiation (approximately a factor of 1,000 lower flux than AM 1.5). High-efficiency PV cells can meet the power requirements (> 50 nW/mm^2) [8,13] of these systems through optimization of the spectral response in appropriate spectral windows: 425-650 nm [19] for ambient indoor lighting

and 700-1100 nm for the infrared transparency window for biological tissue [19-20].

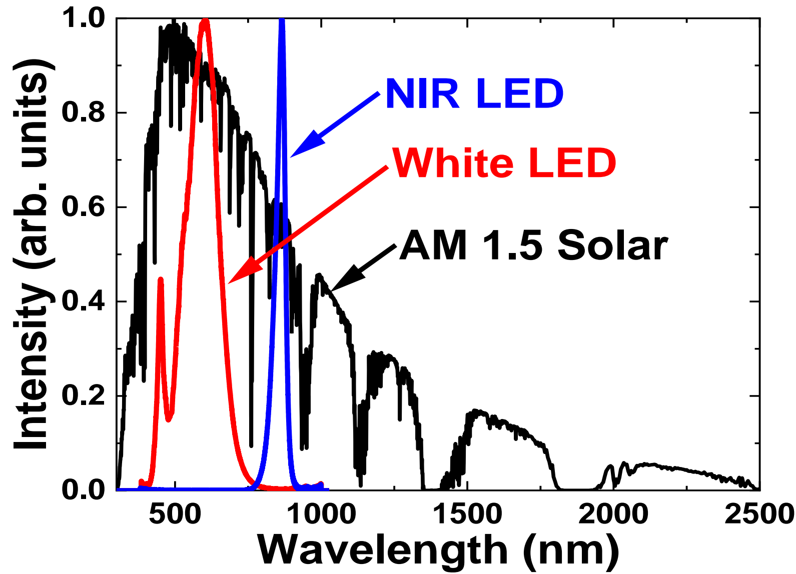


Figure 1.5. White and near infrared LED spectra compared with the solar spectrum.

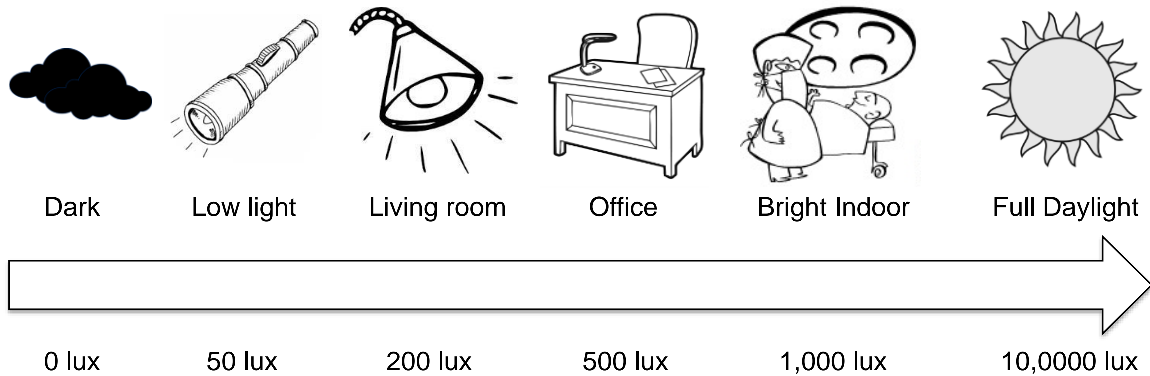


Figure 1.6. Comparison chart of illuminance from indoor to outdoor conditions (adopted [21]).

Previous works on photovoltaic wireless power transfer (WPT) for IoT^2 were cm-scale or larger and tested under extremely high intensity of laser illumination in mW range [22], comparable to the intensity used for laser therapy treatments [23]. Here we demonstrate that photovoltaic cells at mm-scale or below can provide power densities needed for the perpetual operation of miniaturized systems via low-level irradiation under indoor lighting or NIR

illumination at a wavelength of 850 nm in a through-tissue configuration.

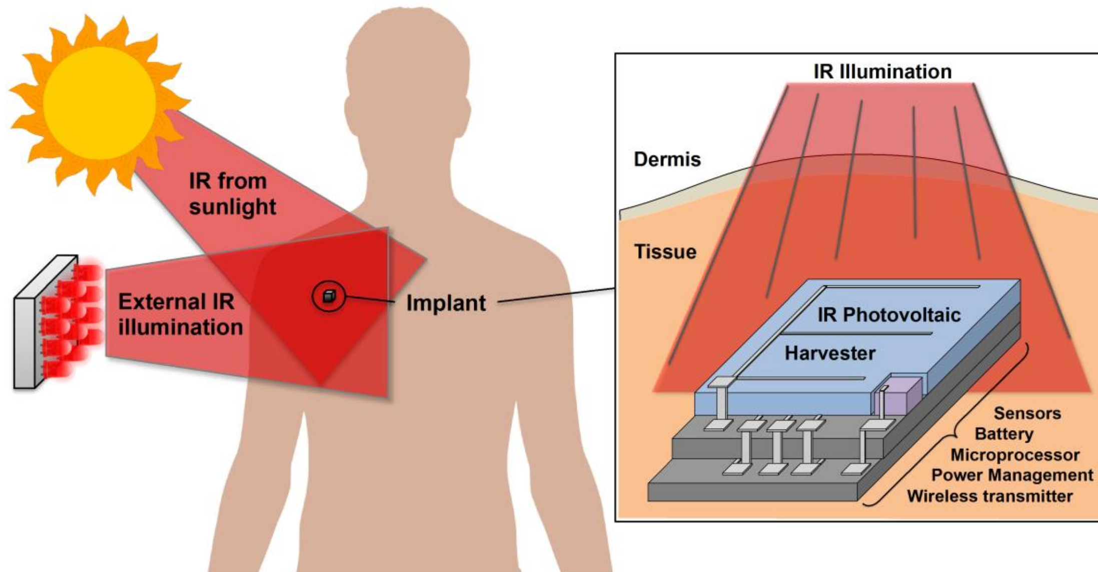


Figure 1.7. Conceptual illustration of subcutaneous photovoltaic energy harvesting through tissue.

1.5. Thesis organization

This thesis includes an in-depth study of silicon and GaAs based photovoltaic energy harvesting for mm-scale systems under low-flux indoor or subcutaneous conditions from the theoretical device simulation / modeling to the actual device fabrication / packaging.

Chapter 2 introduces silicon photovoltaic cells at the mm-scale and their performance limiting factors in terms of the sidewall recombination loss and shunt resistance for the operation of miniaturized photovoltaic cells under low-flux conditions. The effective solutions to overcome these limiting factors are evaluated, using the optimized device structures and sidewall passivation studies.

Chapter 3 provides an in-depth study of GaAs based photovoltaic cells at the mm-scale to boost the energy harvesting efficiency under low-flux conditions. The optimized chemical and

dielectric passivation studies on the sidewall and surface of GaAs and their effects on device performances are explored.

Chapter 4 demonstrates the feasibility of subcutaneous energy harvesting using mm-scale silicon and GaAs photovoltaic cells through the near-infrared optical transparency window of various tissues samples.

Chapter 5 shows an approach of monolithic GaAs photovoltaic modules, offering an efficient means for energy harvesting and direct battery charging in mm-scale systems without the voltage up-conversion loss. The AlGaAs junction barrier isolation scheme is introduced as a critical step in limiting shunt leakage current between series connected cells.

Chapter 6 explores vertically stacked dual-junction PV cell and module in the same GaAs material for direct powering to IoT and bio-implantable applications with narrowband spectral response and miniaturized device size at sub mm-scale. The effectiveness of dual junction approach to increase the output voltage per cell with reduced area losses from isolation and interconnects is discussed for the ultimate battery-less operation of miniaturized CMOS IC chips.

Chapter 7 introduces an approach of a monolithic GaAs based PV / LED module and a full system assembly at the µm-scale for brain-machine interfaces such as “neural dust”, enabling two-way optical power and data transfer in a through-tissue configuration.

Chapter 8 proposes future works for the wafer-level integration of neural probe assemblies including GaAs PV / LED wafer, CMOS silicon chips and neural probes through the through-wafer via, wafer thinning, and flip chip bonding. The modified and improved µ-LED design optimized for CMOS SPAD arrays are also proposed.

CHAPTER 2

Small-area Silicon Photovoltaic Cells

2.1. Introduction

Silicon photovoltaics is an attractive option for wireless energy harvesting in mm-scale systems that can be widely used for novel applications including IoT and bio-implants due to their excellent visible and NIR response, compatibility with silicon CMOS [24], and reduced cost, utilizing ambient sources from solar irradiation and indoor lighting or an intentional LED illumination. Conventional high efficiency silicon photovoltaic cells at cm-scale or larger as shown in Fig 2.1 are well established for solar energy and optimized for visible and NIR wavelength range with above 90 % external quantum efficiency (EQE), where low flux solar response has demonstrated a power conversion efficiency of 13.5 % under 1 μW/mm^2 [25] and 13.1 % under 3 μW/mm^2 AM 1.5 illumination [26]. However, specific requirements for device operation under extremely low-flux conditions, miniaturization of device size down to mm-scale, and a stackable device configuration to integrate silicon PV cells with existing miniaturized CMOS systems have not been addressed, where perimeter/sidewall recombination [13, 21] and shunt resistance [21] are expected to be critical. In this chapter, mm-scale silicon photovoltaic cells are explored for low-flux energy harvesting.

2.2. Device structure & Fabrication

The device structure of conventional high-efficiency silicon PV cells [27-29] with above 25 % efficiency under AM 1.5 solar irradiation [12] is fabricated by using a high-quality crystalline silicon wafer with a few hundred microns thick (300 – 500 μm) for efficient light absorption as shown in Fig. 2.1. The front surface of wafer is textured into inverted pyramids using wet or dry etching processes to reduce the reflection losses, which is passivated with high-quality silicon oxide for lowering the surface recombination. The differential heavy doping of n layer near the front metal fingers and rear point contacts on the back side of wafer for heavily doped p-type region are used to reduce the additional front and rear surface recombination losses.

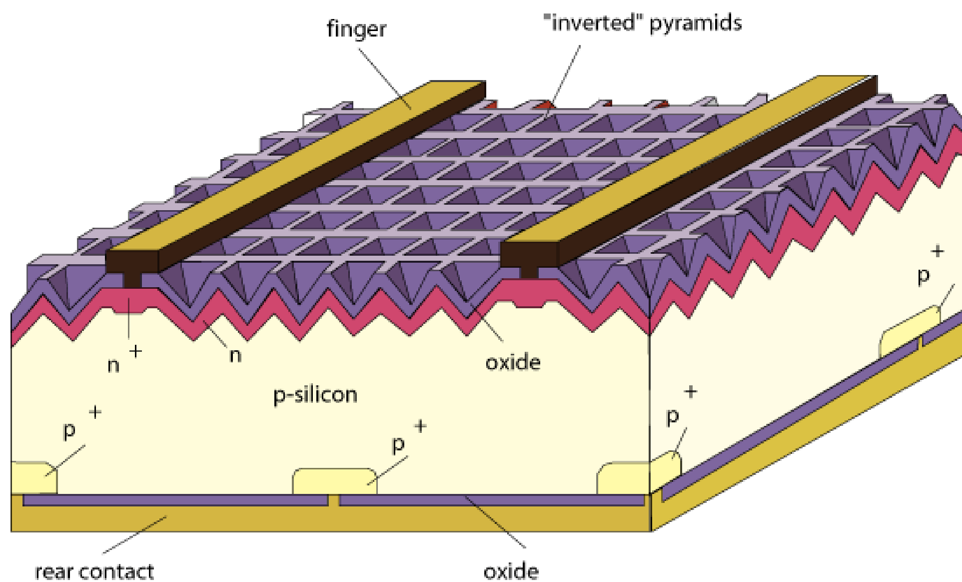
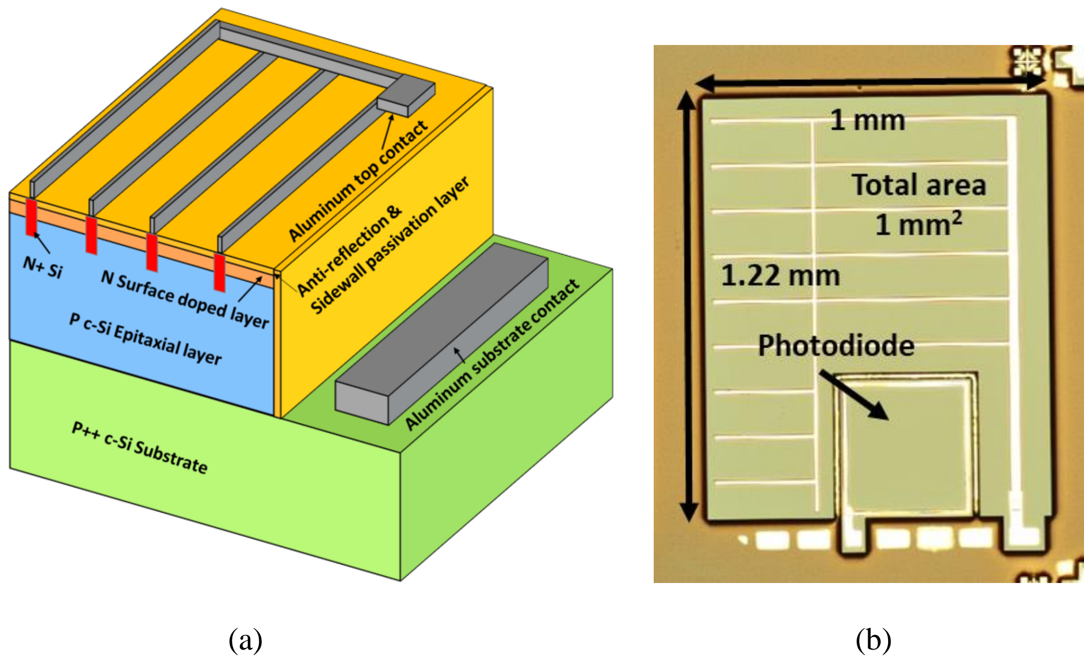


Figure 2.1. Schematic illustration of conventional high-efficiency solar cell (adopted from [29]).

Our silicon photovoltaic cells were designed based on the structure of commercial silicon PV cells [27-29]. The baseline device structure consists of a thick p-type silicon base layer on heavily doped p-type silicon substrate, diffused lightly doped n-type emitter near the surface between heavily doped emitter contacts on the top surface with the goal of improving carrier

collection and passivated front surface using high-quality oxide layer, as shown in Fig. 2.2 (a). In contrast to conventional solar silicon PV cells, the baseline geometry utilizing a heavily doped substrate and lightly doped base is selected in this work to provide top contacts to facilitate a stacked configuration for mm-scale systems [8] and guarantee controllable thickness and doping concentration for optimization of the device structure to specific spectral ranges and characterization of shunt resistance of the device. Furthermore, anti-reflection coating layers were used rather than the surface texturing because the recombination losses from surface and sidewall are critical for mm-scale systems under low-flux applications.

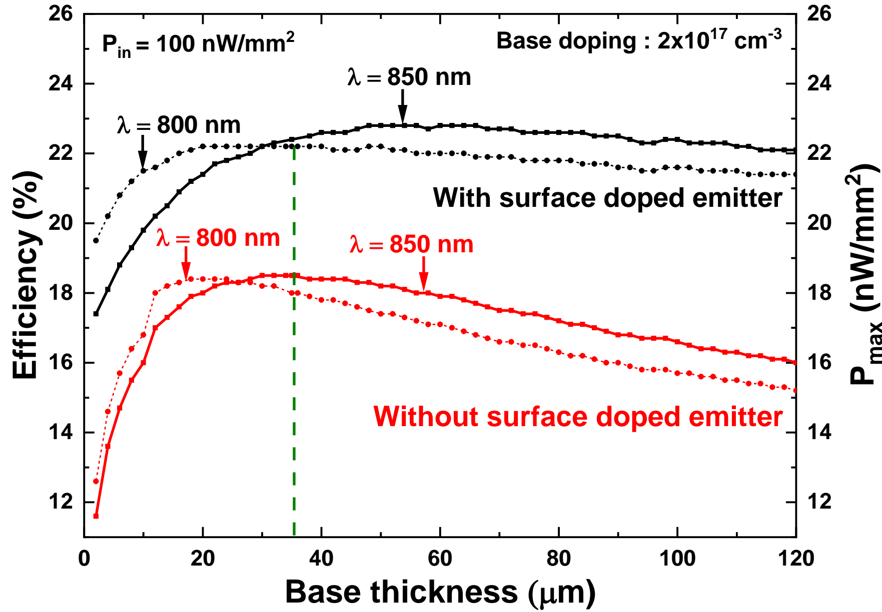


(a) (b)

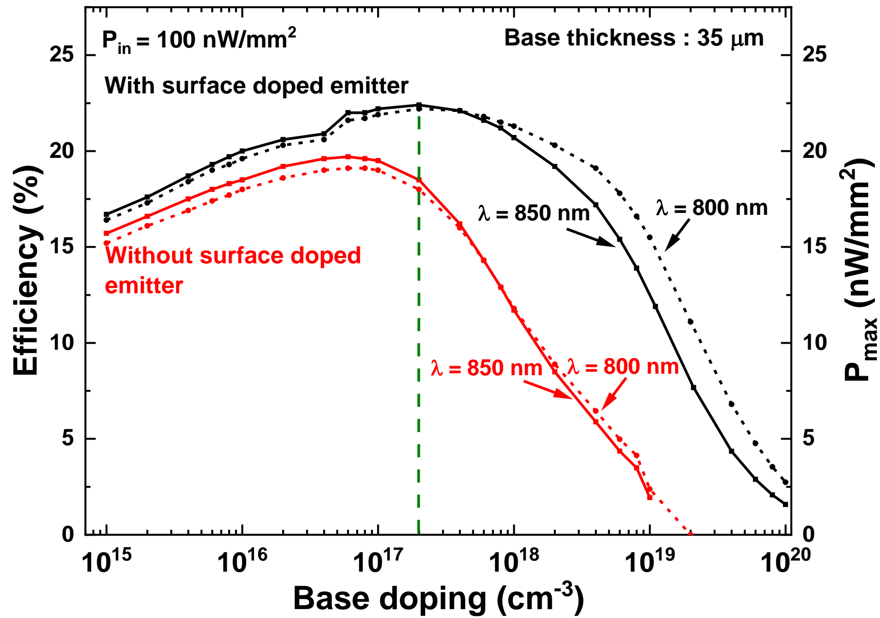
Figure 2.2. (a) Schematic illustration of device structure and (b) optical microscope image of a fabricated 1 mm^2 device.

The detailed device parameters are simulated using Sentaurus Device [30], using built-in values for silicon material parameters at 300 K and neglecting the edge effects including surface recombination and sidewall recombination. The base thickness and doping concentration were optimized for irradiation between 800 nm and 850 nm at a power density of 100 nW/mm^2. The dependence of power conversion efficiency on base layer thickness and doping concentration are

shown in Fig. 2.3. Base thickness near 35 μm, corresponding to the optical absorption depth of silicon [31] at 300 K, and base doping concentration near 2x10^{17} cm^{-3} were found to provide near optimal performance under the NIR illumination conditions simulated.



(a)



(b)

Figure 2.3. Simulated power conversion efficiency under 100 nW/mm^2 illumination at 800 nm (dashed) and 850 nm (solid) for variable (a) base thickness and (b) base doping concentration.

The inclusion of a surface n-type emitter with thickness of 340 nm and concentration of 2.5×10^{16} cm^{-3} was found to significantly increase the short-circuit current and corresponding power conversion efficiency due to the improved carrier collection throughout the device, as shown in Fig. 2.4. Optimized device parameters are summarized in Table 2.1.

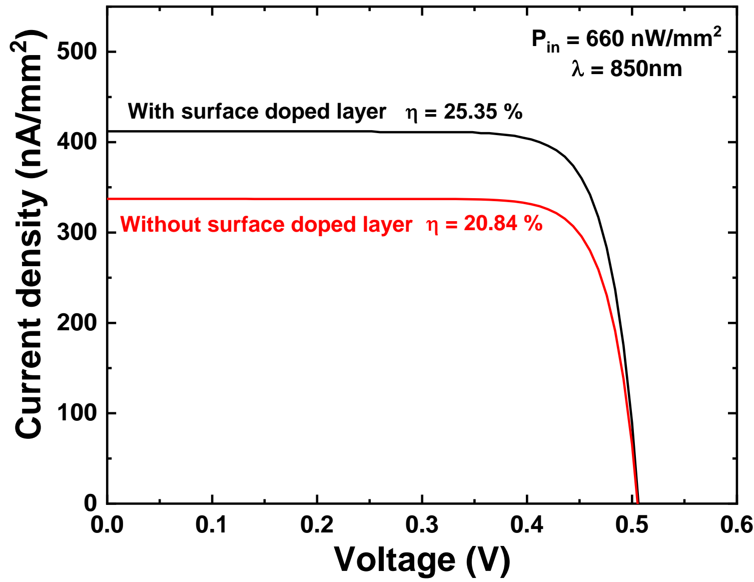


Figure 2.4. Simulated current–voltage characteristics of silicon photovoltaic cells with / without lightly doped emitter under 660 nW/mm^2 illumination at 850 nm.

Parameter	Value	Unit
Base thickness	35	µm
Base doping concentration	2×10^{17}	cm^{-3}
N-type surface layer thickness	0.34	µm
N-type surface layer doping	2.5×10^{16}	cm^{-3}
Anti-reflection Si_3N_4 layer	100	nm
Emitter width	3	µm
Emitter depth	0.46	µm

Table 2.1. Optimized device parameters under 850 nm NIR illumination at 100 nW/mm^2.

A lightly-doped emitter with 1.2 μm thickness and $5x10^{18}$ cm^{-3} peak concentration was formed through a subsequent 300 nm reactive ion etch of the top surface. The main huddle during device fabrication is closely connected to deep trenches (> 40 μm) for bottom p-contacts and device isolation. The well-established deep reactive-ion etching (DRIE) was used to etch the epitaxial silicon layer down to the heavily doped substrate as shown in Fig. 2.5. The patterning process over the deep trench was not easy due to poor sidewall coverage of spin coated photoresist (PR) and unwanted PR residues in the deep trenches, which was solved by using a sticky PR named SPR 7.0, lowering PR spinning speed below 1000 rpm, and using a low temperature annealing process around 85 ^oC. Aluminum contacts were fabricated for n-type and p-type layers using conventional photolithography, electron beam evaporation, and wet chemical etching processes. The detailed device fabrication recipe is included in Appendix. Due to the strong sidewall / perimeter dependence of small area PV cells [13,21], variable device area was studied in the range of 0.02 mm^2 to 10 mm^2, corresponding to a perimeter/area (P/A) ratio of from 35.84 mm^{-1} to 1.4 mm^{-1}.

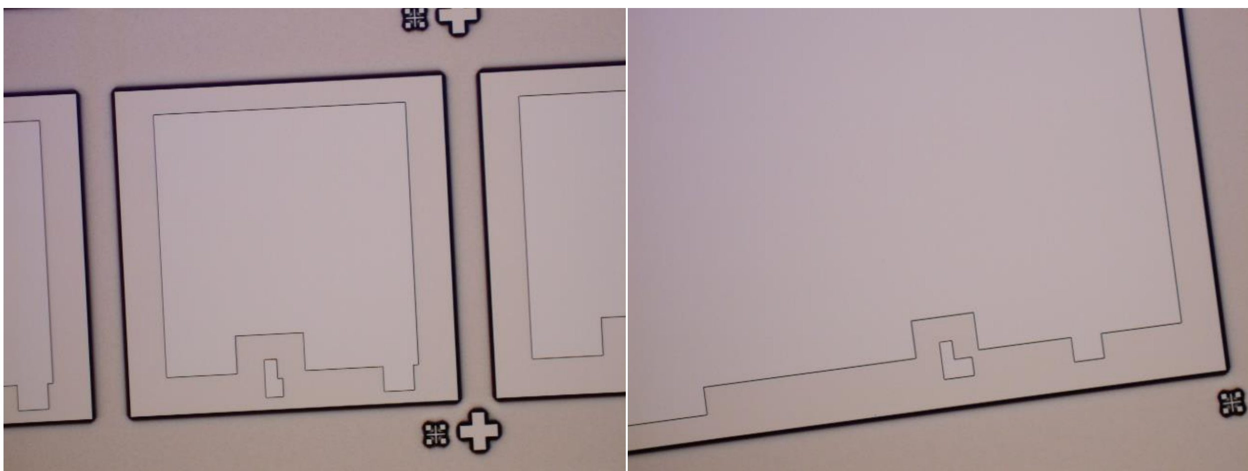


Figure 2.5. Optical microscope images of the resulting DRIE isolation trenches.

2.3. Surface / Sidewall passivation studies

Several sidewall and surface passivation layer processes were investigated, since surface recombination is expected to have a major impact on device performance for small mm-scale devices operating under low-flux conditions. Passivation layers studied in this work include low-pressure chemical vapor deposition (LPCVD) of Si_3N_4, LPCVD a-Si due to good coverage on the deep exposed sidewall of LPCVD process [32] and resulting improved passivation for dangling bonds of the surface and sidewall [33-34], SiO_2 via dry thermal oxidation due to reduction in interface states by the high quality material growth directly using the existing silicon material on the sidewall and surface, plasma enhanced chemical vapor deposition (PECVD) of Si_3N_4, PECVD SiO_2 due to lower growth temperature of PECVD process below 400 ^oC and compatibility to other possible chemical passivation studies [35-40], and no passivation for comparison. Further details on the six different passivation layers under study are as follows:

1) 50 nm LPCVD Si_3N_4 at 800 ^oC + 50 nm PECVD Si_3N_4 at 380 ^oC.

2) 25 nm LPCVD a-Si at 560 ^oC + 100 nm PECVD Si_3N_4 at 380 ^oC.

3) 40 nm thermally grown dry SiO_2 at 900 ^oC + 50 nm LPCVD Si_3N_4 at 800 ^oC + 100 nm PECVD SiO_2 at 380 ^oC.

4) 100 nm PECVD Si_3N_4 at 380 ^oC.

5) 100 nm PECVD SiO_2 at 380 ^oC.

6) control sample without passivation.

2.4. Characterization methods

Electrical current density versus voltage (*J-V*) characteristics under dark and illumination were measured using Keithley 2400 / 4200 semiconductor characterization systems. Low-flux

illumination conditions were controlled by a microscope-compatible 850 nm infrared light emitting diode and calibrated power-meter. Power conversion efficiency was measured for irradiation at a power density of 660 nW/mm^2, which is extremely dim in comparison to the power density of AM 1.5 sunlight of 1000 μW/mm^2 [12]. The EQE spectrum was measured on select samples using a system equipped with a halogen white light source, lock-in amplifier, monochromator and calibrated photodetector.

2.5. Results

2.5.1. Sidewall recombination loss

Dark current measurements for variable size of PV cells that are passivated by thermal silicon dioxide as shown in Fig. 2.6 were done to demonstrate the size dependence on device characteristics and corresponding numerical parameters for dark current were obtained by fitting the forward biased region from 0 V to 0.4 V to the diode equation

$$J = J_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \qquad (1)$$

where J is the total current density, V is the applied voltage, n is the diode ideality factor, k is the Boltzmann constant, T is the temperature and J_0 is the reverse saturation current. Extracted diode parameters as shown in Fig. 2.7 show a strong perimeter dependence, ranging from 0.443 to 15.9 nA/mm^2 for J_0 and from 1.285 to 1.723 for the ideality factor. This unwanted increase in diode parameters including reverse saturation current and ideality factor is attributed to an increase in Shockley–Read–Hall (SRH) recombination in the space charge region near the sidewall. In comparison to simulation results as shown in Fig. 2.8, measured values of V_{OC} and corresponding efficiency are still substantially lower than simulated values assuming no losses from surface and sidewall recombination and surface reflection.

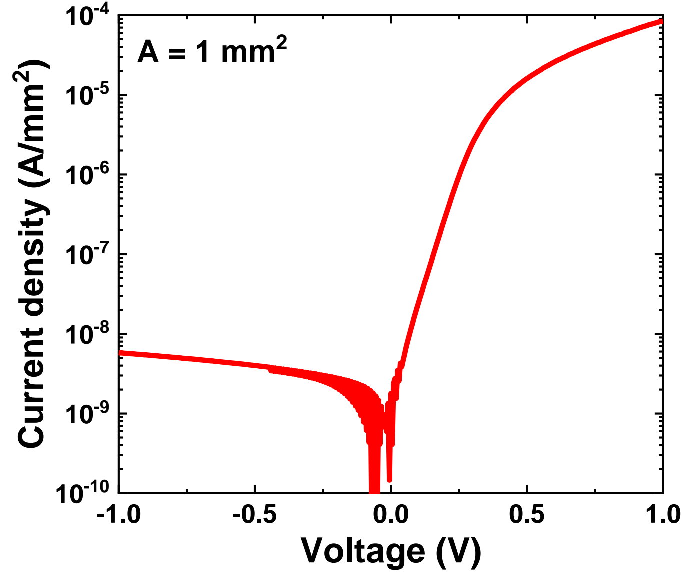


Figure 2.6. Measured current versus voltage characteristic of photovoltaic cell with 1 mm^2 under dark condition.

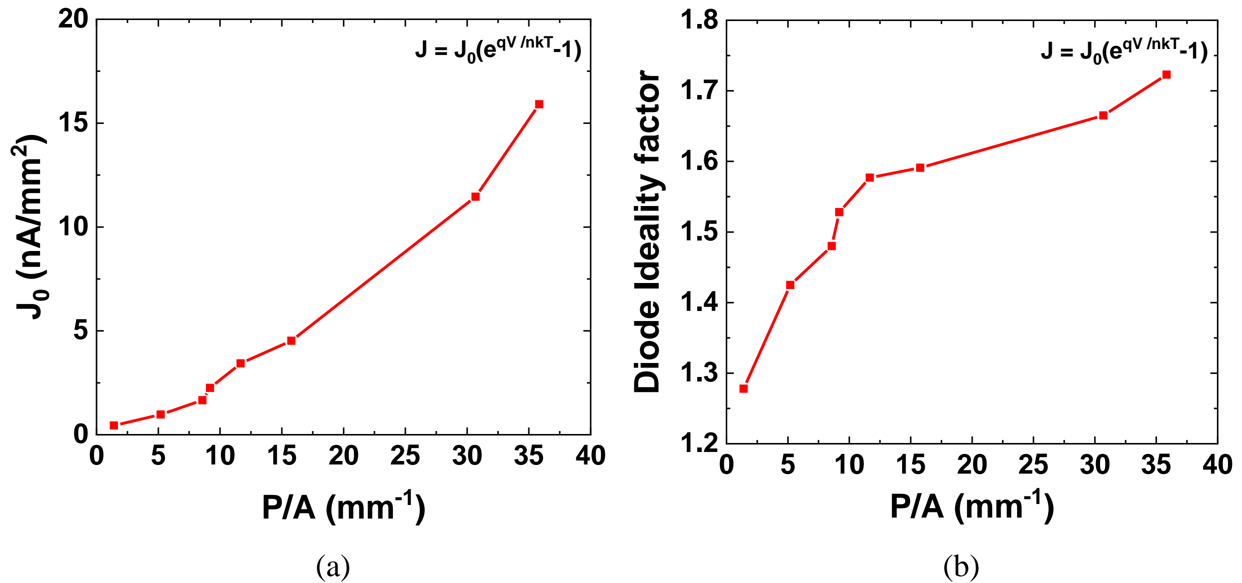


Figure 2.7. (a) Extracted J_0 and (b) diode ideality factors versus P/A (mm^{-1}) ratio from 1.4 mm^{-1} to 35.84 mm^{-1} corresponding device size from 10 mm^2 to 0.02 mm^2.

The primary source of efficiency reduction is likely due to non-ideal thermal silicon dioxide passivation of the p-type sidewall resulting in reduced minority carrier diffusion length, requiring improved passivation of the sidewall to approach the simulated efficiency values.

Improved passivation of the sidewall may be achieved by using a-Si or Si_3N_4 [33] to approach the simulated efficiency values. Losses associated with the high doping concentration at the emitter surface interface, such as free carrier absorption or Auger recombination are other efficiency limiting factors. An optimized doping profile of the surface n-type emitter through selective etching between the light harvesting and metal finger regions are required, as well as improved design of the surface passivation layer to serve as an anti-reflection coating and layer to effectively reduce bulk and sidewall recombination losses.

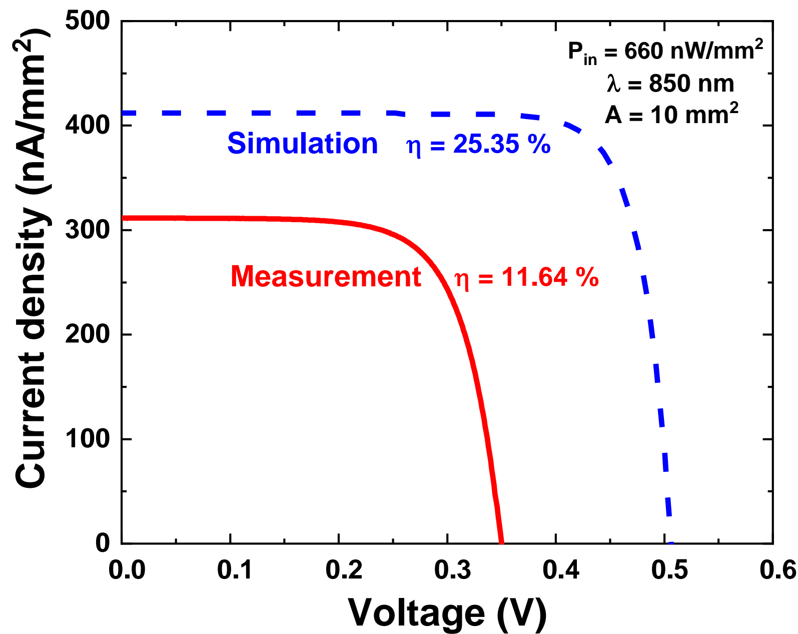


Figure 2.8. Measured (solid) and simulated (dashed) current-voltage characteristics of photovoltaic cell under 660 nW/mm^2 illumination at 850 nm.

2.5.2. Passivation studies

Silicon cells with variable passivation layers and optimized surface n-type emitter were fabricated. The passivation layers served the dual purpose of sidewall passivation and an anti-reflection coating, where the surface reflectance was optimized at a wavelength of 800 nm. The 100 nm Si_3N_4 is expected to provide 1-2 % surface reflectance at 850 nm as shown in Fig. 2.9.

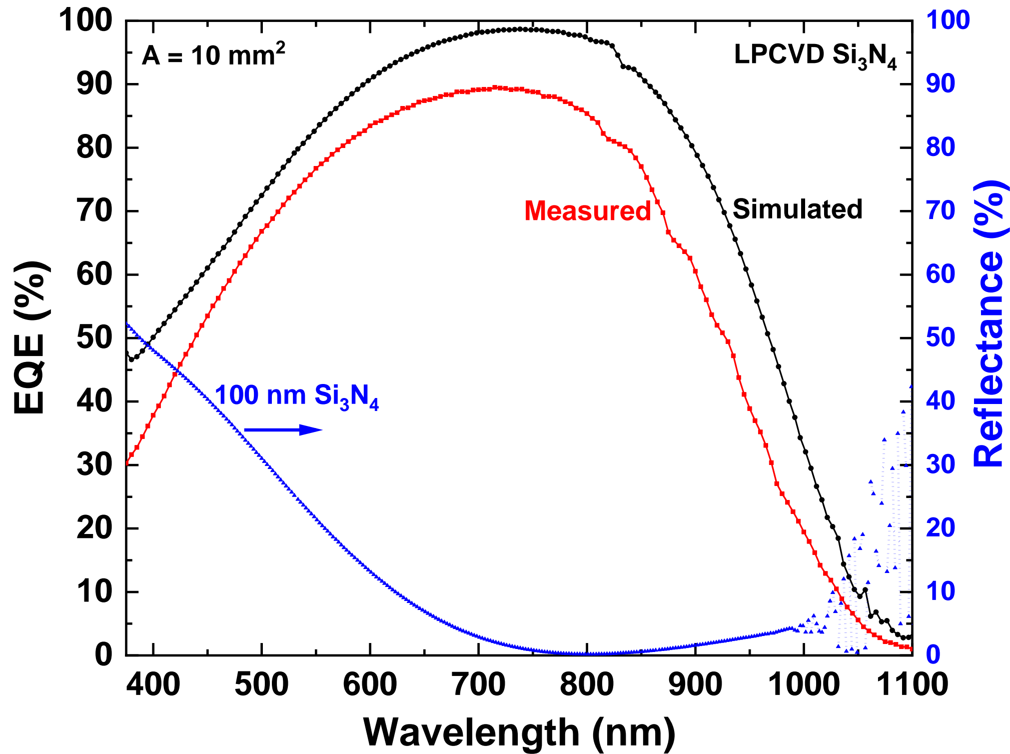


Figure 2.9. Measured and simulated external quantum efficiency (EQE) characteristics for the 100 nm LPCVD Si_3N_4 passivated cell along with a surface reflectance curve (dashed) of cell between 375 nm and 1100 nm wavelength.

Fabricated device sizes were 1 mm^2 and 10 mm^2. A comparison of *J*-*V* results is shown in Fig. 2.10, where LPCVD Si_3N_4 and LPCVD a-Si passivation demonstrate the highest power conversion efficiency of 17.12 % and 16.16 %, respectively. The improved efficiency originates primarily from an increase in V_{OC}, with relatively similar J_{SC} values. From the EQE measurement as shown in Fig 2.10, the device structures including the base thickness and anti-reflection layer are well optimized both for visible and NIR wavelength with above 80% EQE over this wavelength range. Dark *J*-*V* characteristics are shown in Fig. 2.11, with results from parameter extraction summarized in Table 2.2. The LPCVD Si_3N_4 and a-Si passivation processes demonstrate a clear reduction in reverse saturation current and reduction in ideality factor from 1.968 to 1.393, demonstrating that the LPCVD processes is effectively passivating the deep sidewall with Si_3N_4

and a-Si. The improved dark *J-V* characteristics demonstrate a clear agreement with the measured improvements in V_{OC} for the Si_3N_4 and a-Si processes.

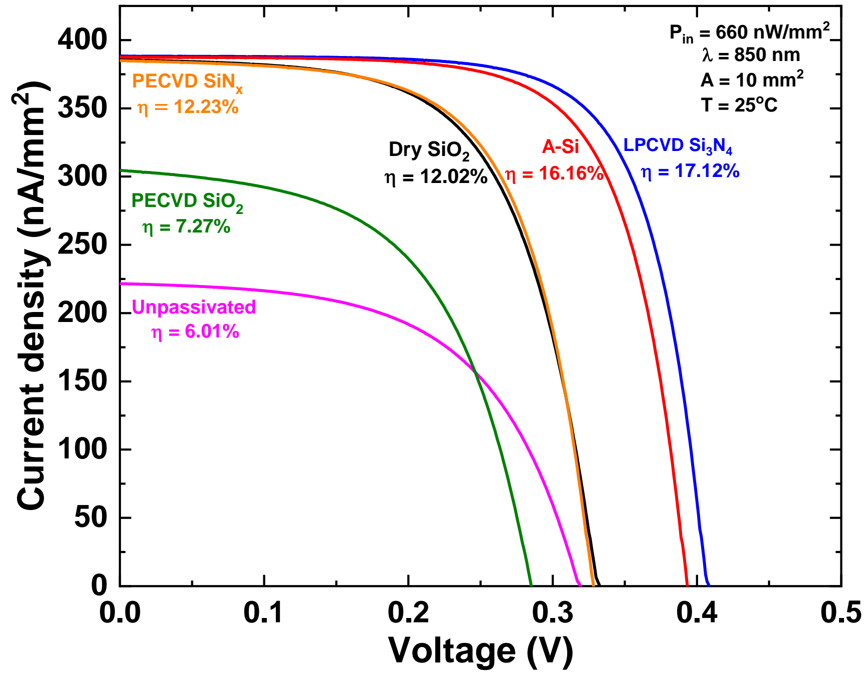


Figure 2.10. Measured current versus voltage characteristics of different passivation layers for 10 mm^2 cell under 850nm LED illumination with 660nW/mm^2.

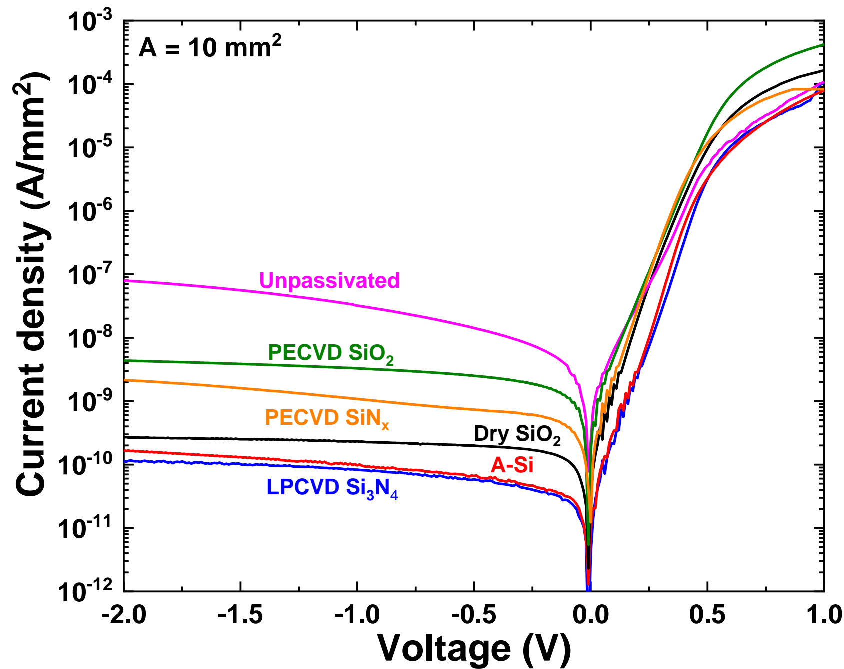


Figure 2.11. Measured *J-V* under dark conditions for samples with different passivation layers.

Passivation	J_0 (A/mm^2)	n
LPCVD Si_3N_4	5.31 x 10^{-12}	1.393
LPCVD a-Si	8.87 x 10^{-12}	1.419
Dry SiO_2	3.54 x 10^{-10}	1.851
PECVD Si_3N_4	7.03 x 10^{-11}	1.498
PECVD SiO_2	1.04 x 10^{-9}	1.943
Unpassivated	4.07 x 10^{-10}	1.968

Table 2.2. Extracted diode parameters of 10 mm^2 cells using equation (1).

2.6. Discussion

The maximum efficiency achieved in the cells for this study is 17.12% for the LPCVD Si_3N_4 under low-flux 850 nm LED illumination. This provides a power density of 113 nW/mm^2, above the desired value of 100 nW/mm^2 for mm-scale systems [8,21]. The results are also improved over previously reported commercial cm-scale c-Si photovoltaic cells that were tested under the low-flux solar spectrum condition of 3000 nW/mm^2, with reported efficiency of 13.1% [26].

The limitation on power conversion efficiency of these cells are mainly attributed to a reduction in V_{OC}, as illustrated in Fig. 2.12 comparing measured and calculated / simulated results. The calculated results from Shockley–Queisser (SQ) limit [41] assumed complete absorption of all photons above band gap of silicon, no non-radiative recombination losses and lossless transport of excited carriers. The simulated results from the drift-diffusion device simulation in Sentaurus Device used the practical material parameters of silicon and a 2D cross section of device, with no sidewall or surface recombination. The evident reduction in measured V_{OC} in comparison to values obtained from the SQ limit and device simulation arises from the increase in reverse saturation

current due to non-radiative recombination losses including sidewall and surface recombination as indicated in equation (2)

$$V_{OC} = \frac{nkT}{q} ln \left(\frac{J_{SC}}{J_0} + 1\right) \quad (2)$$

where J_{SC} is the short-circuit current, J_0 is the reverse saturation current, n is the diode ideality factor, k is the Boltzmann constant and T is the temperature.

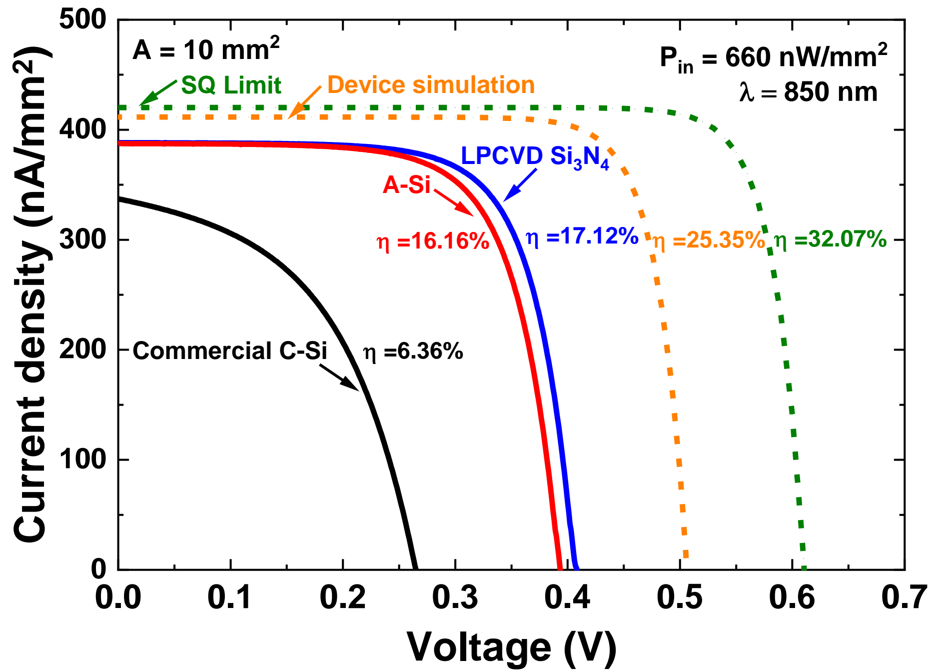


Figure 2.12. Measured *J-V* characteristics and corresponding conversion efficiency and comparison to device simulation with no surface and sidewall losses and an ideal Shockley–Queisser model.

As shown in Table 2.3, V_{OC} values and corresponding conversion efficiency decreases for the smaller 1 mm2 devices, suggesting that sidewall recombination is more important for mm-scale applications in comparison to conventional cm-scale photovoltaic cells. Degradation in conversion efficiency under low incident light intensity by shunt resistance compared to the negligible impacts of series resistance can also impact the utility of PV cells for energy harvesting applications.

Passivation	LPCVD Si_3N_4		LPCVD a-Si	
Size (mm^2)	10	1	10	1
P/A (mm^{-1})	1.18	3.13	1.18	3.13
J_{SC} (nA/mm^2)	388.29	403.18	387.47	404.66
V_{OC} (V)	0.409	0.384	0.394	0.359
Efficiency (%)	17.12	15.91	16.16	15.53
J_0 (A/mm^2)	5.31×10^{-12}	2.36×10^{-11}	8.87×10^{-12}	1.45×10^{-11}
Ideality factor	1.393	1.502	1.419	1.356
Fill factor	0.711	0.678	0.699	0.705

Table 2.3. Device size dependence on device parameters of LPCVD passivated cells under illumination of 660 nW/mm^2 at a wavelength of 850 nm.

Power conversion efficiency and fill factor under variable intensity illumination were examined for the cells with LPCVD Si_3N_4 and a-Si passivation, as shown in Fig. 2.13 and Fig. 2.14. The measured devices exhibit a decrease in efficiency with reduced illumination, with similar behavior for both passivation techniques. Measured results for a commercial c-Si solar cell (IXYS Corporation: KXOB22-12X1) [42] with 22 % power conversion efficiency under AM 1.5 illumination are shown for comparison, which exhibits a more dramatic decrease in fill factor and corresponding efficiency with reduced illumination. To examine the possible influence of efficiency degradation due to shunt leakage, conversion efficiency as shown in Fig. 2.16 was simulated using a diode model (Fig. 2.15) with assuming extracted J_0 and n values from dark current measurement of tested cell and variable shunt resistance using an equation

$$J = J_{sc} - J_0 \left[exp\left(\frac{q(V+JAR_s)}{nkT} \right) - 1 \right] - \frac{V+JAR_s}{R_{sh}} \qquad (2)$$

where J_{SC} is the short circuit current, J_0 is the reverse saturation current, n is the diode ideality factor, T is the temperature, A is the device area, k is the Boltzmann constant, R_S is the parasitic series resistance and R_{Sh} is the parasitic shunt resistance.

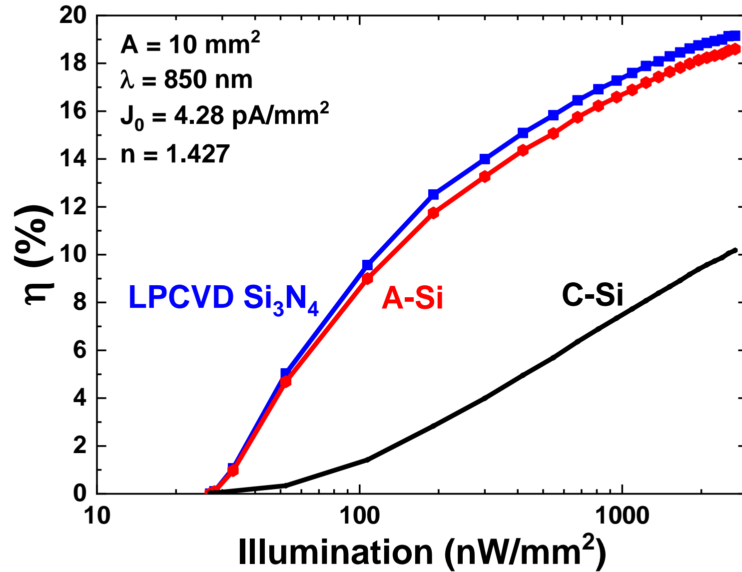


Figure 2.13. Measured power conversion efficiency versus NIR illumination for varying device passivation and comparison to commercial c-Si (IXYS Corporation: KXOB22-12X1, [42]).

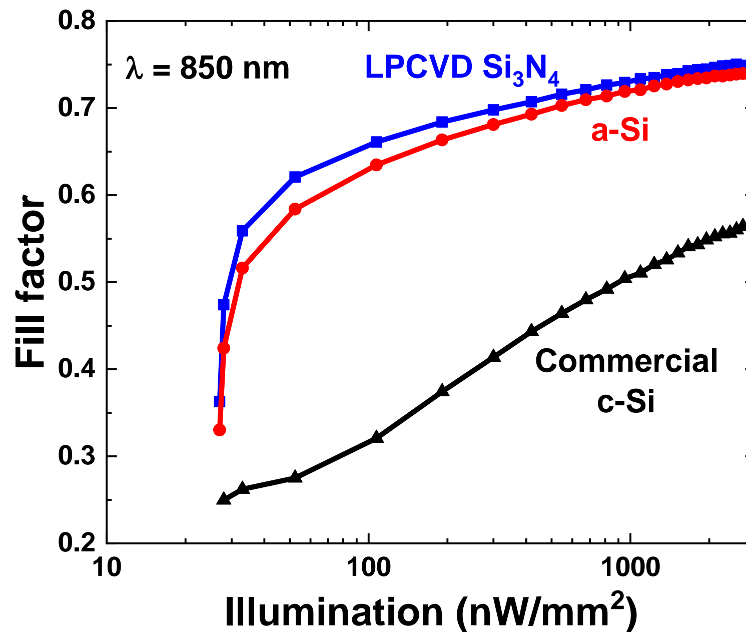


Figure 2.14. Measured fill factor versus NIR illumination for varying device passivation and comparison to commercial c-Si (IXYS Corporation: KXOB22-12X1, [42]).

The LPCVD Si_3N_4 and a-Si passivated cells studied in this work demonstrate a shunt resistance above 10 MΩ-cm^2, sufficient to prevent degradation in efficiency for the range of illumination studied. Efficiency degradation with illumination follows expected behavior where cells are limited by the dark current (reverse saturation current density, J_0). Further improvements in cell efficiency will therefore require reduction in J_0, where techniques such as atomic layer deposition of Al_2O_3 [33-34] and chemical surface treatments including NH_4F [35-36], $(NH_4)_2S$ [37-38] and H_2S [39-40] may be beneficial.

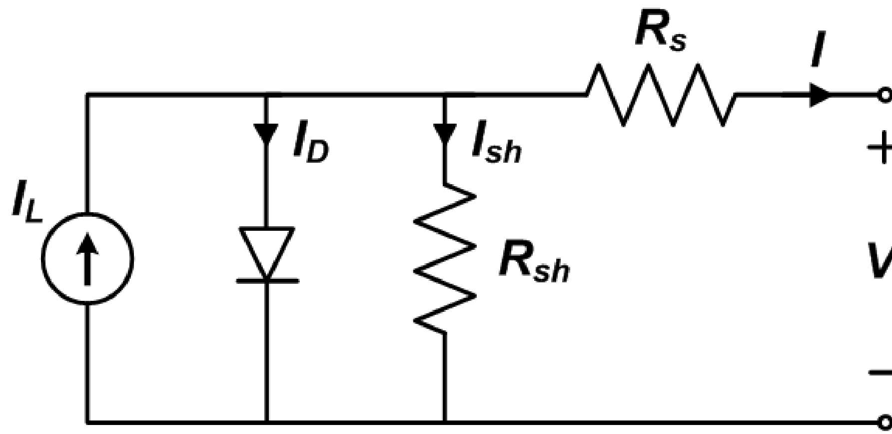


Figure 2.15. An equivalent circuit model of PV diode with parasitic series and shunt resistances.

2.7. Conclusion

Small area Si photovoltaic cells were optimized based on simulation results for energy harvesting applications in mm-scale systems. High EQE above 80% and power conversion efficiency exceeding 17 % are demonstrated under low-flux NIR illumination. The device performance was dramatically improved by LPCVD passivation. In contrast to conventional c-Si PV, the cells in this work demonstrate stable performance under low illumination intensity that is limited by dark current rather than shunt leakage. The good performance of the small-area silicon

cells under low illumination conditions are promising for through-tissue infrared energy harvesting and IoT applications, where further improvements may be achieved by additional measures to reduce recombination losses at interfaces.

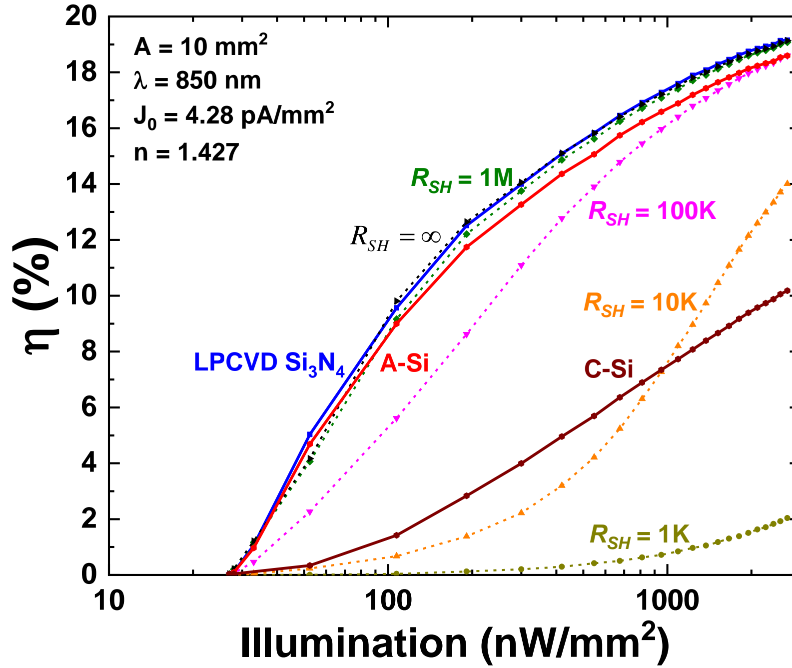


Figure 2.16. Measured power conversion efficiency versus NIR illumination for varying device passivation and comparison to commercial c-Si. Simulated values using a diode model in (a) are shown assuming J_0 and n values shown in the inset and varying shunt resistance in (Ω-cm^2).

CHAPTER 3

Small-area GaAs Photovoltaic Cells

3.1. Introduction

Photovoltaic energy harvesting provides an alternative means of wireless power transfer (WPT) for mm-scale systems [37,43-45], where the ambient solar irradiation and indoor lighting or an intentional LED illumination could provide sufficient energy to PV cells and conventional high efficiency PV cells [46] convert this wavelength region efficiently with above 90 % external quantum efficiency (EQE). The key challenges to obtaining highly efficient PV energy harvesting are that device performances of PV cells at mm-scale or smaller under low-flux illumination are degraded by shunt resistance [13,21,26] and sidewall / perimeter recombination losses [13,47]. Previous works on photovoltaic WPT [37,43-45] for low-flux applications are cm-scale or larger and tested under extremely high intensity of laser illumination in mW range [45,48], which is not suitable for fully remote device operation. One of reported silicon PV cells at mm-scale in the previous chapter addressed and relatively overcame these challenges, which had above 17 % power conversion efficiency under low-flux NIR illumination below 1 $\mu W/mm^2$ at a wavelength of 850 nm. However, fundamental material characteristics of silicon such as higher dark current and shunt leakage compared to other III-V compound semiconductors limit the open circuit voltage and corresponding power conversion efficiency. On the other hand, GaAs based PV cells have a possibility to boost the energy harvesting efficiency due to superior optical properties matched to

the desired wavelength region, low dark current and low shunt leakage, which worked successfully under low-flux indoor conditions [13,21] and could provide sufficient power for mm-scale systems. In this work, the details of mm and sub-mm scale GaAs photovoltaics cells optimized for low-flux energy harvesting applications and their performance limiting factors are explored.

3.2. Device structure & Fabrication

The structure of conventional high-efficiency GaAs PV cells [46] as shown in Fig. 3.1 consists of a thicker base (several µm thick) and thinner emitter (several hundred nm thick) layers with addition of higher bandgap window and back surface field layers. The cells are based on n-p or p-n designs because minority diffusion lengths can be greater than the absorption depth for either doping types. The higher bandgap window and back surface field layers using lattice matched InGaP or AlGaAs materials are incorporated to reduce the surface recombination losses by reflecting minority carriers away from the surface.

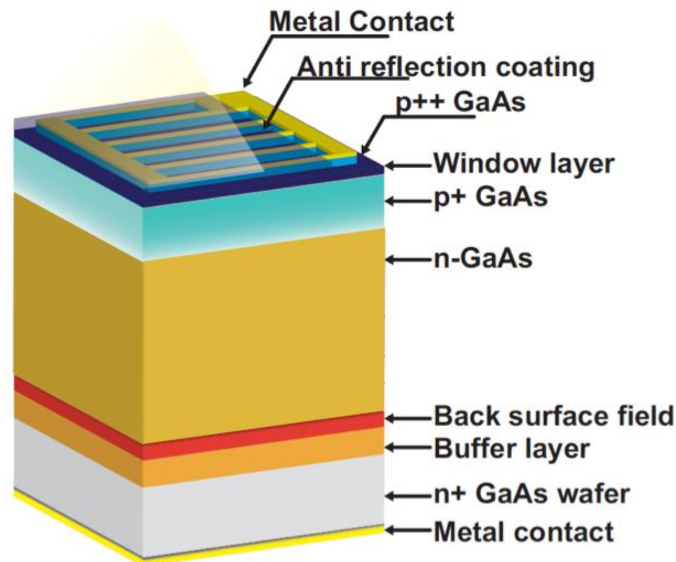
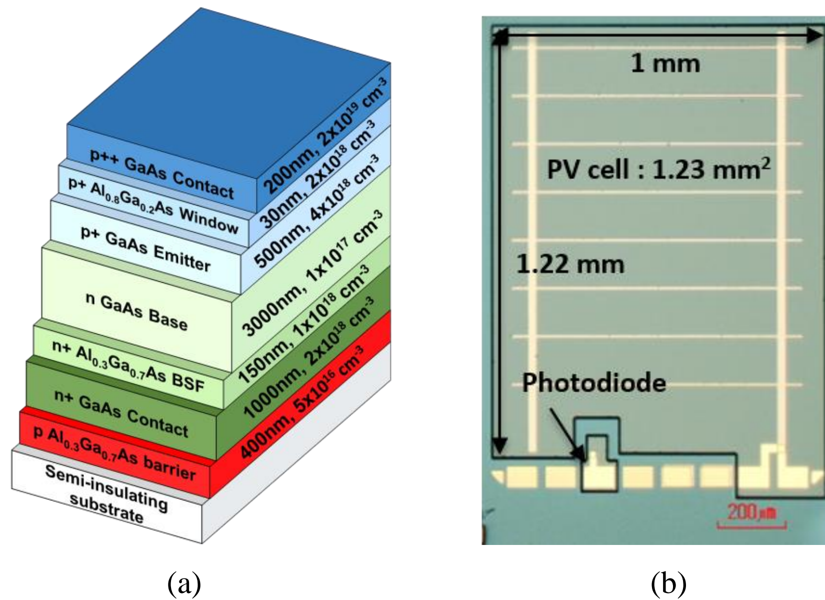


Figure 3.1. Schematic diagram of conventional high-efficiency GaAs photovoltaic device structure.

Our device structure grown by molecular beam epitaxy (MBE) utilizing the structure of conventional high efficiency GaAs solar cells consists of n-base and p-emitter layers with addition of p-$Al_{0.8}Ga_{0.2}As$ window and n-$Al_{0.3}Ga_{0.7}As$ back surface field layers on a semi-insulating GaAs substrate for the possible PV array design as shown in Fig. 3.2 (a). Devices were fabricated using the chlorine based reactive-ion etching (RIE) to etch the epitaxial layers down to the n+ contact layer, the conventional photolithography using photoresists and physical vapor deposition (PVD) of thin metal films (Detailed fabrication recipe is included in Appendix)

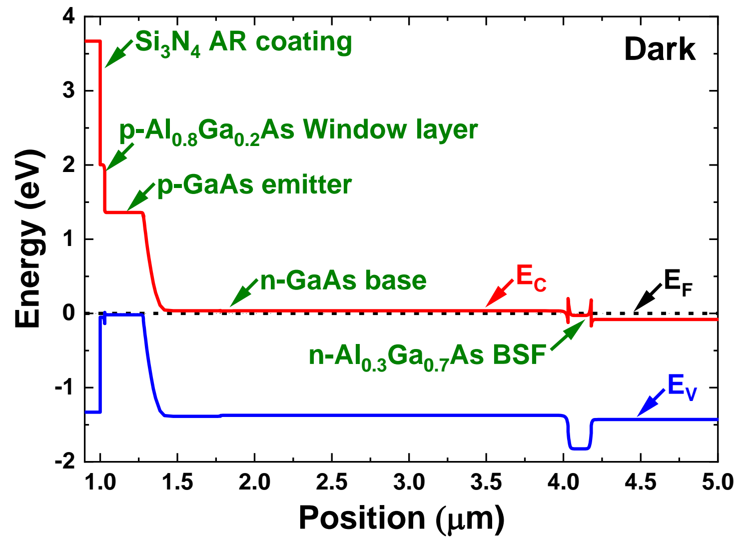


(a) (b)

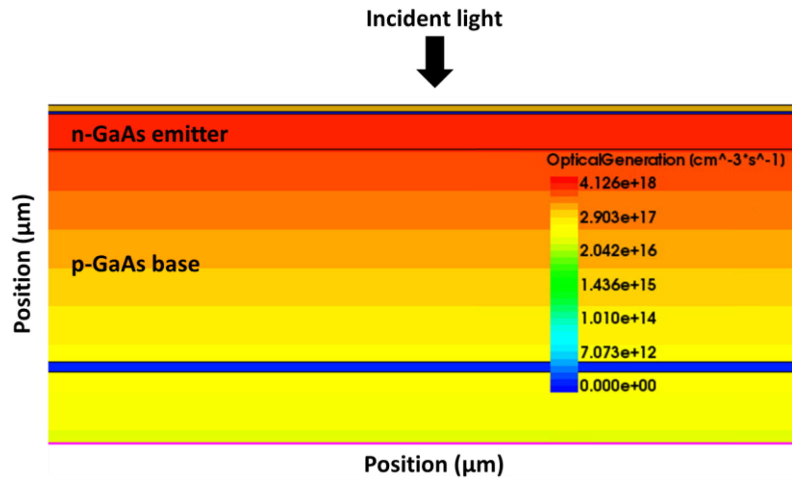
Figure 3.2. (a) Schematic diagram of optimized device structure, (b) Optical microscope image of fabricated GaAs PV cell at mm-scale.

The layer structure of GaAs photovoltaic (PV) cell for low-flux energy harvesting was optimized based on simulation results using Synopsys Sentaurus [30] using widely accepted material parameters at 300 K and neglecting recombination effects from the surface/sidewall. The simulated energy band diagram and the profile of photo-generation rate under NIR illumination were indicated in Fig. 3.3. The device parameters are designed both for visible and NIR wavelength ranges under low intensity illumination at 100 nW/mm^2, where the device performance is

dominated by shunt resistance. The base doping concentration of 10^{17} cm^{-3} and base thickness of 2.75 μm result in the maximum output power density under 100 nW/mm^2 at a wavelength range between 800 nm and 850 nm as shown in Fig. 3.4. The optimized device parameters are summarized in Fig. 3.2 (a). Devices with varying area were fabricated to study the influence of sidewall / perimeter recombination losses [13,21,26], ranging from 0.001 mm^2 to 6.4 mm^2, corresponding to perimeter / area (P/A) ratio from 125 mm^{-1} to 1.7 mm^{-1}.

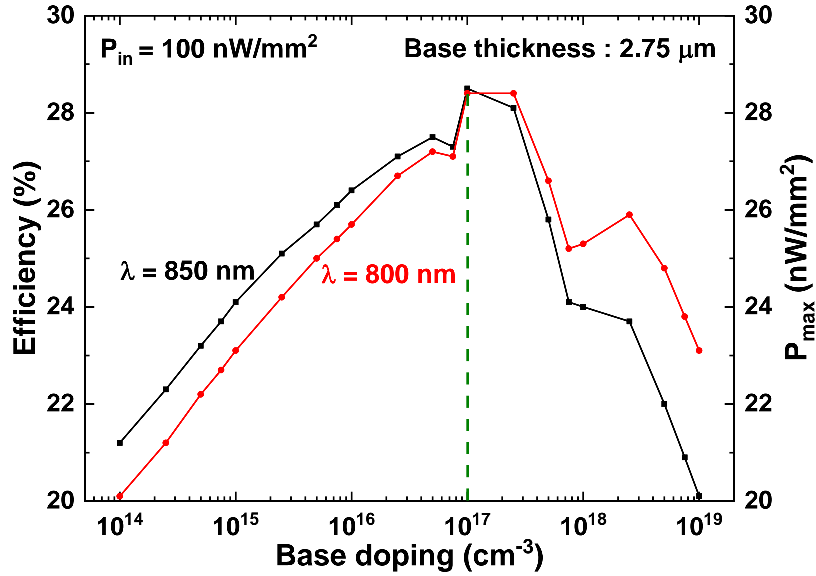


(a)

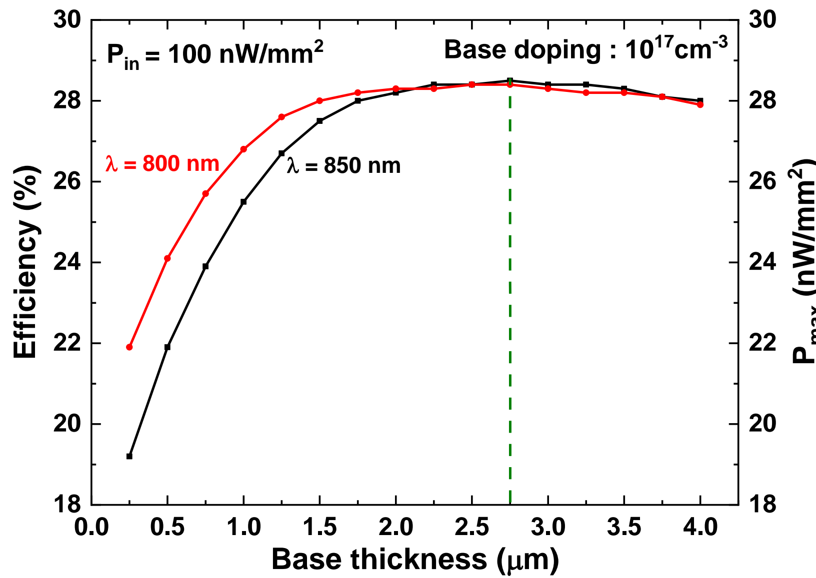


(b)

Figure 3.3. Simulated (a) energy band diagram and (b) profile of photogeneration rate under illumination.



(a)



(b)

Figure 3.4. Simulated maximum power density under 100 nW/mm^2 illumination at 800 nm and 850 nm versus variable base (a) doping concentration and (b) thickness.

3.3. Passivation studies

Various passivation processes were studied including dielectric passivation and chemical passivation methods to reduce the sidewall/perimeter recombination losses, including plasma

enhanced chemical vapor deposition (PECVD) Si_3N_4, $(NH4)_2S$ [49-51] and NH_4OH [52] with subsequent PECVD Si_3N_4, NH_4OH with subsequent atomic layer deposition (ALD) Al_2O_3 [52]. The dielectric passivation layers using PECVD Si_3N_4 and ALD Al_2O_3 were used to reduce the interface traps and passivate the dangling bonds on the surface and sidewall. The chemical passivation studies using $(NH4)_2S$ and NH_4OH were used to etch the native oxide and passivate the surface and sidewall using the additional sulfur bonds in $(NH4)_2S$ or make the hydroxylated surface using NH_4OH ready for dielectric passivation deposition [52]. Further details of the different passivation processes are as follows:

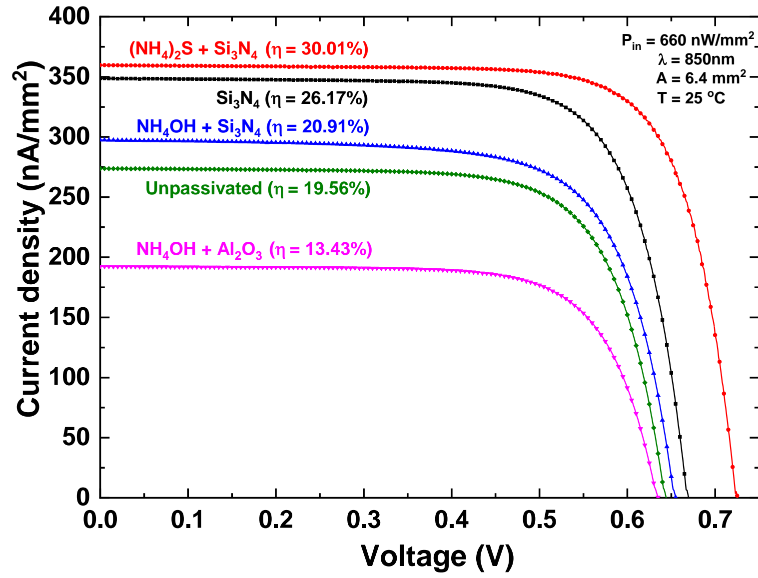
1) 100 nm PECVD Si_3N_4 at 380 °C.
2) $(NH_4)_2S$ (23% in H_2O) for 10 min at room temperature + 100 nm PECVD Si_3N_4 at 380 °C
3) NH_4OH (29 % in H_2O) for 3 min at room temperature + 100 nm PECVD Si_3N_4 at 380 °C,
4) NH_4OH (29 % in H_2O) for 3 min at room temperature + 25 nm ALD Al_2O_3 at 150 °C,
5) a sample without passivation.

3.4. Results

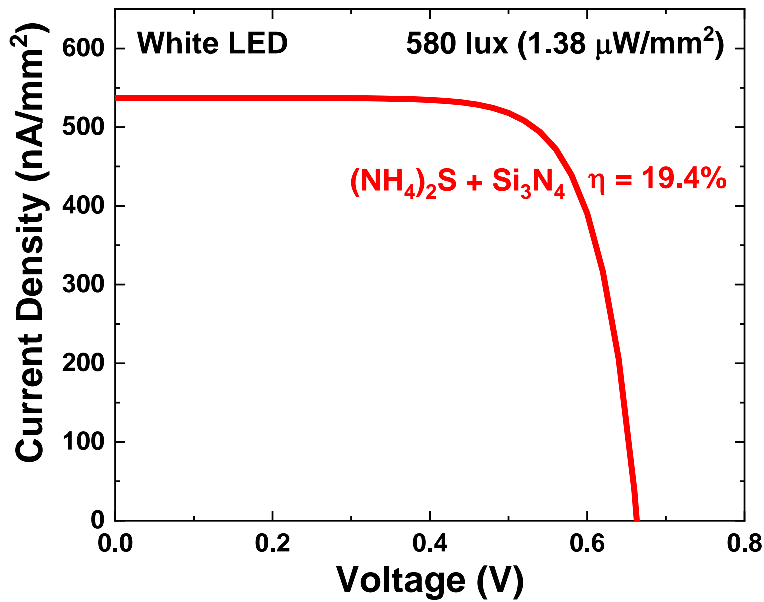
3.4.1. Passivation layer

The *J-V* characteristics of 6.4 mm^2 GaAs PV cells passivated with the five different passivation layers under 660 nW/mm^2 illumination at a wavelength of 850 nm and 580 lux (1.38 $\mu W/mm^2$) white LED illumination are shown in Fig. 3.5. A 100 nm PECVD Si_3N_4 passivation layer matched to both visible and NIR wavelength ranges as shown in Fig. 3.5 increased the short circuit current (J_{SC}) compared to control sample without passivation by reducing the surface reflectance and the surface recombination loss. The ammonium sulfide ($(NH_4)_2S$) treatment encapsulated with PECVD Si_3N_4 layer for long-term stability of layers [53] improved both the short

circuit current density (J_{SC}) and the open circuit voltage (V_{OC}), which results in the maximum power conversion efficiency above 30 % under 850 nm NIR illumination with 660 nW/mm^2 and around 20 % under white LED illumination with 580 lux can supply sufficient power to a mm-scale system with the minimum power requirement of 50 nW/mm^2 [8,13].



(a)



(b)

Figure 3.5. Measured current density versus voltage curves of different passivation studies of 6.4 mm^2 cell under (a) 850 nm NIR-LED illumination with 660 nW/mm^2 and (b) white LED illumination with 580 lux (1.38 μW/mm^2).

The EQE measurement as shown in Fig. 3.6 on this (NH4)$_2$S passivated sample shows that the device structure is well optimized for visible and NIR wavelength ranges with above 70 % EQE and 5-7 % discrepancy between simulated and measured EQE values is observed over the desired wavelength region due to the surface reflection from metal fingers. Further studies of different passivation layer effects on device performance for variable size of cells from 0.0052 mm^2 to 6.4 mm^2 corresponding perimeter/area (P/A) ratio 55.56 mm^{-1} to 1.69 mm^{-1} are shown in Fig. 3.7. The device performance of cells with varying size cells is strongly dependent on the P/A ratio, illustrating the critical impact of sidewall recombination loss as one of the most critical limiting factors for these small-area PV cells [13,47], as discussed further in discussion section.

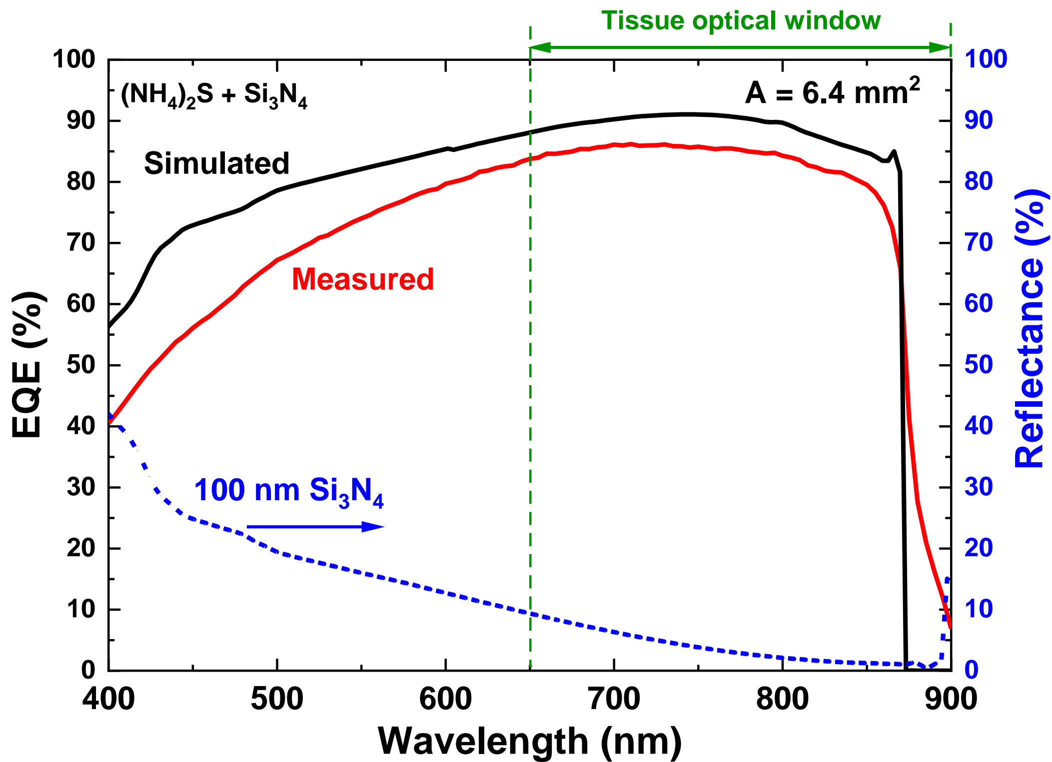


Figure 3.6. Measured and Simulated (dashed) EQE characteristics of $(NH_4)_2S$ + Si_3N_4 passivated sample along with the wavelength range between 400 nm and 900 nm.

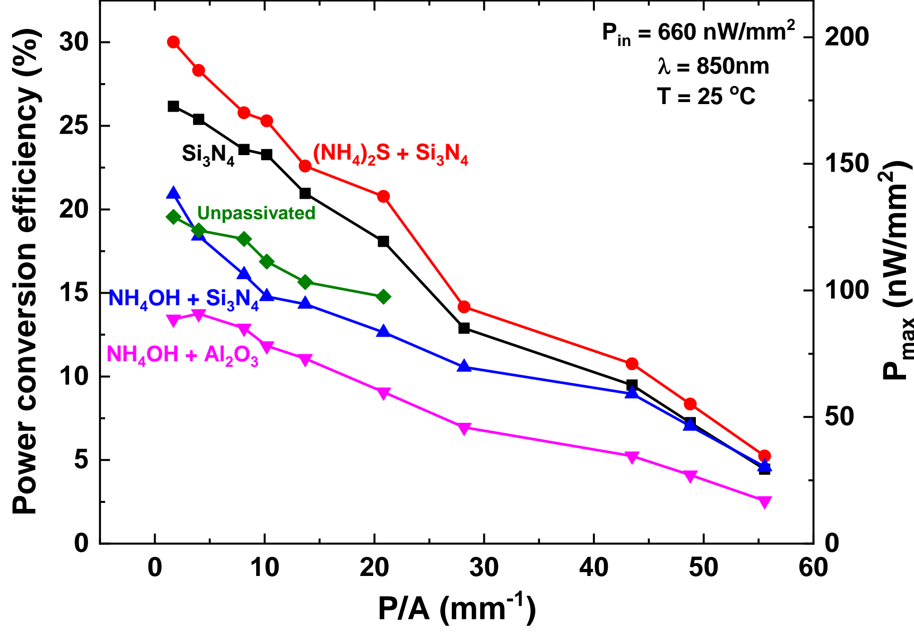


Figure 3.7. Measured power conversion efficiency values of various passivation studies versus P/A (mm^{-1}) ratio from 1.69 mm^{-1} to 55.56 mm^{-1} corresponding device size from 6.4 mm^2 to 0.0052 mm^2.

The $(NH_4)_2S$ treatment improved V_{OC} values of various size PV cells and this V_{OC} improvement is closely relevant to the reduction in the reverse saturation current (J_0) as indicated in equation (1)

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{J_{SC}}{J_0} + 1\right) \qquad (1)$$

where n is the ideality factor, k is the Boltzmann constant, T is the temperature, J_0 is the reverse saturation current density, and J_{SC} is the short circuit current density. The $(NH_4)_2S$ treatment etched the native oxide [49-51] on the surface/sidewall and effectively passivated the dangling bonds with additional sulfur bonds, resulting in the reduction of J_0. The NH_4OH treatment reduced J_{SC} due to increased optical scattering from the rough surface though the NH_4OH treatment etched the native oxide [52] to achieve more electronically favorable surface properties before the dielectric passivation. The 25 nm ALD Al_2O_3 did not provide an optimal anti-reflection match to the desired

wavelength range, which increased the surface reflectance over the desired wavelength region more than the optimized 100 nm PECVD Si_3N_4 layer, resulting in a reduction in J_{SC}. The detailed device parameters regarding p-n junction diode equations and recombination losses were extracted from results of dark current measurement.

3.4.2. Dark current measurements

Dark current measurements were conducted on all PV cells with varying P/A ratio to examine the impact of surface passivation properties. The dark *J-V* plots of 0.25 mm^2 samples were shown in Fig. 3.8 and the extracted J_0 parameters shown in Fig. 3.9 obtained by curve fitting to the forward bias region between 0 V and 0.7 V using the 1-diode equation (2)

$$J = J_0 \left[exp\left(\frac{qV}{nkT}\right) - 1\right] \qquad (2)$$

where J is the total current density, J_0 is the reverse saturation current, V is the applied voltage, k is the Boltzmann constant, T is the temperature.

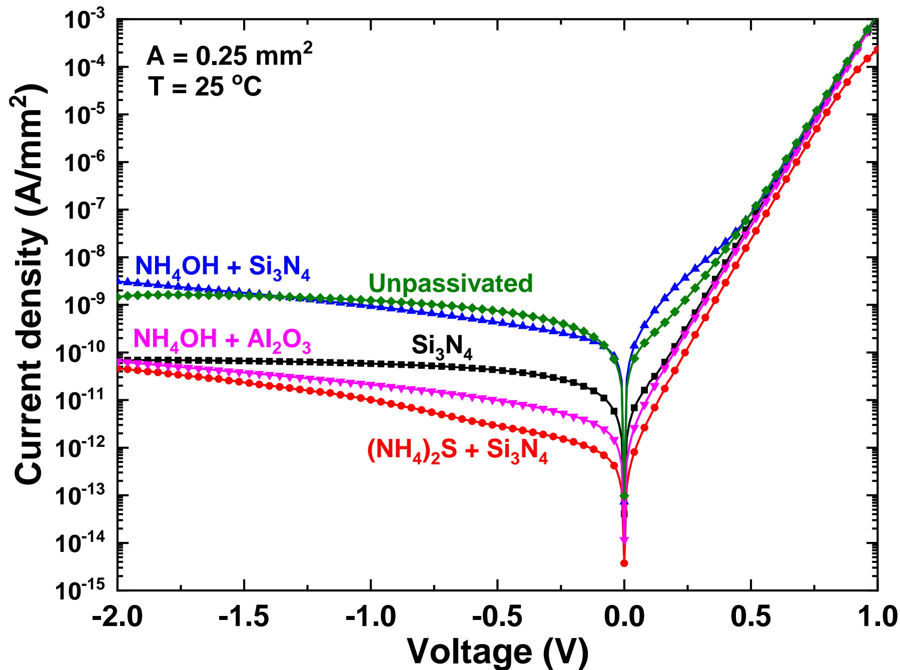


Figure 3.8. Measured current versus voltage of 0.25 mm^2 cell under dark conditions.

The extracted J_0 parameters for all passivation studies shown in Fig. 3.9 show the clear P/A ratio dependence due to increased sidewall/perimeter recombination losses as expected. The dramatic reduction in J_0 over all measured PV cells from $(NH_4)_2S$ treatment was also observed in Fig. 3.9. For example, extracted J_0 of 6.4 mm^2 PV cells summarized in Table 3.1 was reduced from 0.9038 pA/mm^2 for the sample without passivation to 0.0673 pA/mm^2 for the sample passivated with $(NH_4)_2S$ + PECVD Si_3N_4, agreeing with the improvement in V_{OC} as indicated in Fig. 3.5.

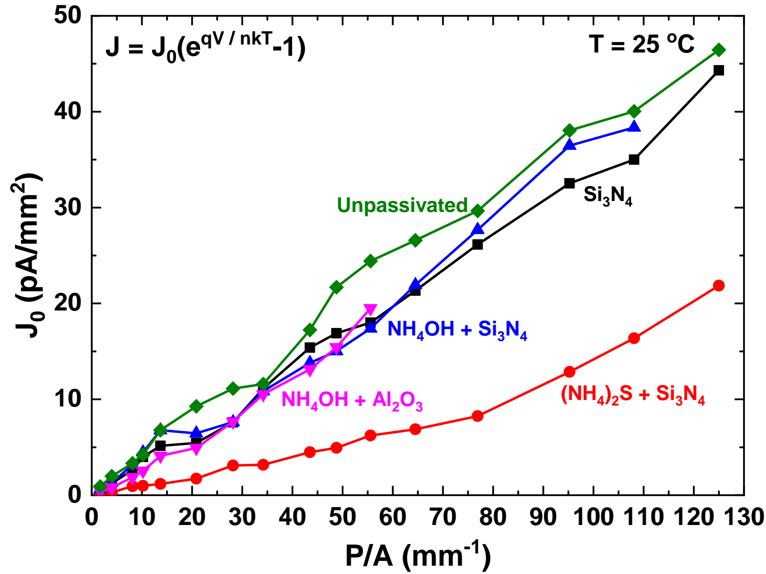


Figure 3.9. Extracted reverse saturation current values of different passivation studies versus P/A (mm^{-1}) ratio from 1.69 mm^{-1} to 125 mm^{-1} corresponding device size from 6.4 mm^2 to 0.001 mm^2.

Passivation	J_0 (pA/mm^2)	n
Si_3N_4	0.6157	1.939
$(NH_4)_2S + Si_3N_4$	0.0673	1.801
$NH_4OH + Si_3N_4$	0.5853	1.933
$NH_4OH + Al_2O_3$	0.4532	1.906
Unpassivated	0.9038	1.969

Table 3.1. Extracted diode parameters of 6.4 mm^2 cells from 1-Diode equation.

The diode ideality factor (n) of 6.4 mm^2 cells summarized in Table 3.1 supported previous results that the ideality factor values near n = 2 for samples are dominated by the space charge region (SCR) recombination losses mainly connected to the sidewall recombination losses and the $(NH_4)_2S$ treatment with subsequent Si_3N_4 deposition reduced the diode ideality factor from 1.969 to 1.801, suggesting that the sulfur treatment unpinned the Fermi-level [53] and reduced the SCR recombination losses from surface and sidewall regions [54-55]. Numerical parameters relevant to the perimeter recombination losses can be extracted by curve fitting to the forward bias region using the 2-diode equation (3)

$$J = J_{01}\left[exp\left(\frac{qV}{kT}\right) - 1\right] + J_{02}\left[exp\left(\frac{qV}{2kT}\right) - 1\right] \qquad (3)$$

where J_{01}, J_{02} are the saturation current densities for carrier recombination in the quasi-neutral region and in the space charge region, respectively. The extracted J_{02} along with P/A ratio are plotted in Fig. 3.10.

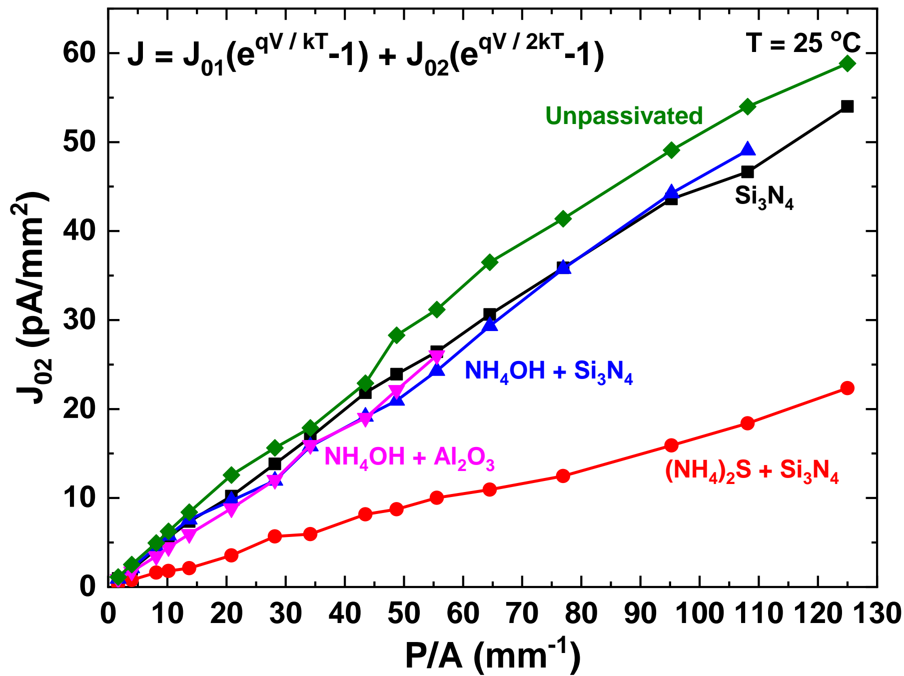


Figure 3.10. Extracted J_{02} parameters along with P/A Extracted J_{02} parameters along with P/A (mm^{-1}) ratio from 1.69 mm^{-1} to 125 mm^{-1}.

The extracted J_{02} exhibiting the strong linear P/A dependence [47,56] can be expanded as (4)

$$J_{02} = J_{02B} + J'_{02P}\left(\frac{P}{A}\right) \qquad (4)$$

using the linear curve fitting to J_{02} using (4) are summarized in Table 3.2, which indicate that the effect of Si_3N_4 passivation mainly reduced the bulk recombination current density from 1.934 pA/mm^2 to 0.7831 pA/mm^2 rather than the perimeter recombination loss from 0.4882 pA/mm to 0.4596 pA/mm compared to the control sample without passivation. The additional NH_4OH treatment with Si_3N_4 passivation also had a slight improvement in the perimeter recombination loss and made the optimized passivation to the bulk recombination only. ALD Al_2O_3 passivation reduced the bulk recombination losses significantly from 1.934 pA/mm^2 to 0.0438 pA/mm^2, but had little impact on reducing perimeter recombination loss. However, the $(NH_4)_2S$ treatment reduced both for bulk and perimeter recombination losses dramatically from 1.934 pA/mm^2 to 0.1409 pA/mm^2 for the bulk recombination and from 0.4882 pA/mm to 0.1714 pA/mm for the perimeter recombination, suggesting that the exposed mesa edges were effectively passivated with additional sulfur bonds.

Passivation	J_{02B} (pA/mm^2)	J'_{02P} (pA/mm)	S_0L_S (cm^2/s)
Si_3N_4	0.7831	0.4596	13.66
$(NH_4)_2S + Si_3N_4$	0.1409	0.1714	5.09
$NH_4OH + Si_3N_4$	0.313	0.4507	13.4
$NH_4OH + Al_2O_3$	0.0438	0.4518	13.43
Unpassivated	1.934	0.4882	14.51

Table 3.2. Extracted diode parameters from a 2-Diode equation.

The important parameters relevant to J'_{02P} can be extracted using (5) [47,56]

$$J'_{02P} = qn_i S_0 L_S \qquad (5)$$

where n_i is the intrinsic carrier concentration, S_0 is the surface recombination velocity and L_S is the effective surface diffusion length. The extracted S_0L_S product of the $(NH_4)_2S$ treated sample was 5.09 cm^2/s where the high efficiency GaAs based solar cells had $S_0L_S < 1$ cm^2/s [47,56-57]. Further improvements in the device structure and passivation studies are still needed to overcome the perimeter recombination losses.

3.4.3. Shunt resistance

The degradation from the parasitic shunt resistance dominating the device operation under low-flux illumination was investigated for the sample with $(NH_4)_2S$ + Si_3N_4 passivation varying the illumination intensities as shown in Fig. 3.11.

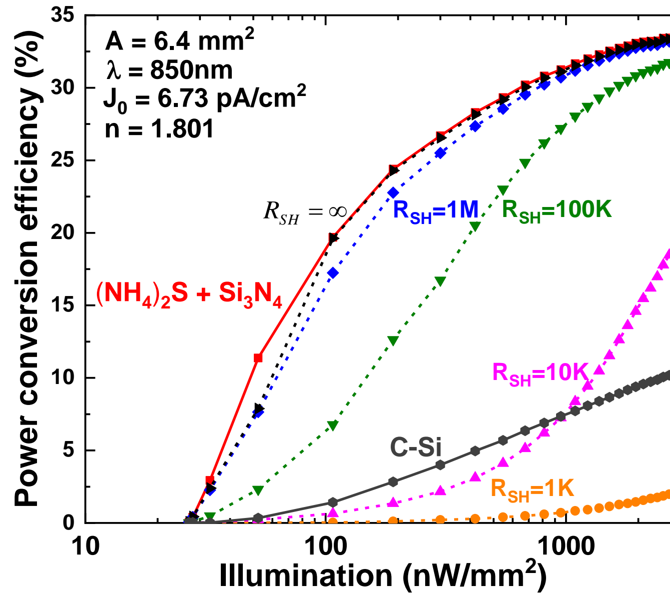
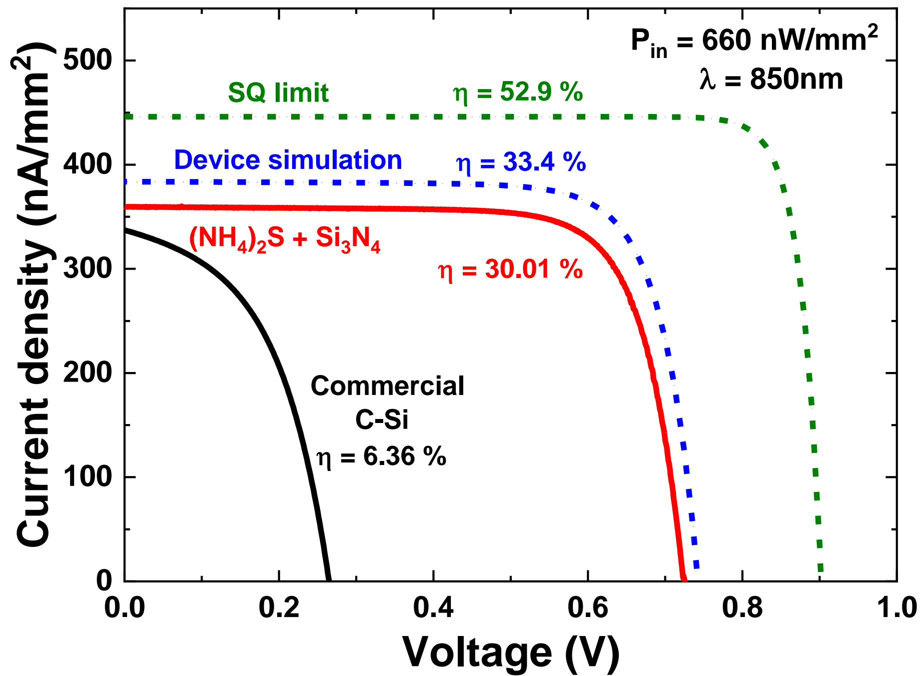


Figure 3.11. Measured (solid) power conversion efficiency values under NIR illumination at a wavelength of 850 nm for the $(NH_4)_2S$ + Si_3N_4 passivated PV cell and for commercial c-Si solar cell [42] for comparison. Simulated (dashed) values varying shunt resistance in (Ω-cm^2) are shown using extracted J_0 and n diode parameters shown in the inset.

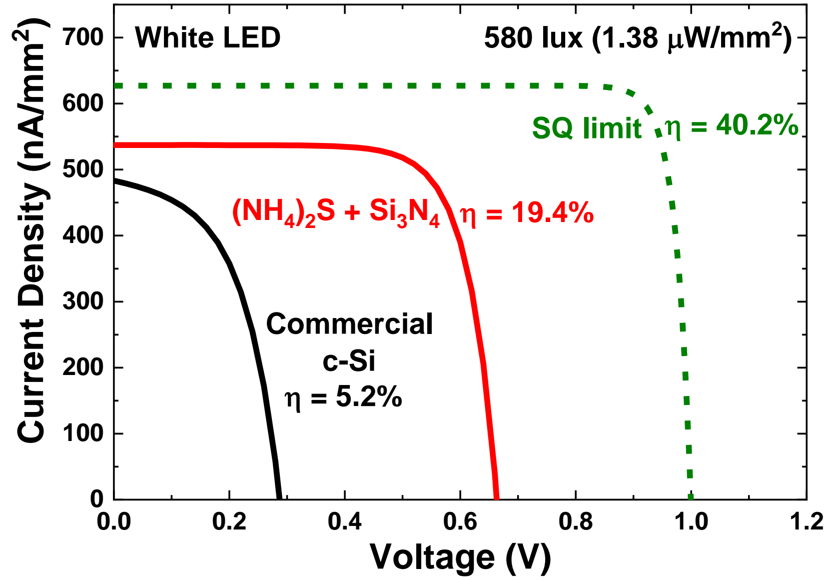
The simulated values for the comparison were calculated using the diode equation (6)

$$J = J_{sc} - J_0\left[exp\left(\frac{q(V+JAR_S)}{nkT}\right) - 1\right] - \frac{V+JAR_S}{R_{sh}} \qquad (6)$$

where J_{SC} is the short circuit current, R_S is the parasitic series resistance and R_{Sh} is the parasitic shunt resistance, using numerical extracted diode parameters from Table 3.1 and varying the shunt resistance values in Ω-cm^2. As shown in Fig. 3.11, the performances of measured GaAs PV cell under various NIR illumination conditions from 30 nW/mm^2 to 2.69 μW/mm^2 were free of the shunt resistance degradation with above 10 MΩ-cm^2 shunt resistance value that is consistent with the previous GaAs PV cell results though the commercial crystalline silicon solar cell (IXYS Corporation: KXOB22-12X1) [42] with above 22 % power conversion efficiency under AM 1.5 solar irradiation shows the clear performance degradation especially in fill factor from the shunt resistance under dim visible and NIR illumination around 1 μW/mm^2 as shown in Fig. 3.12.



(a)



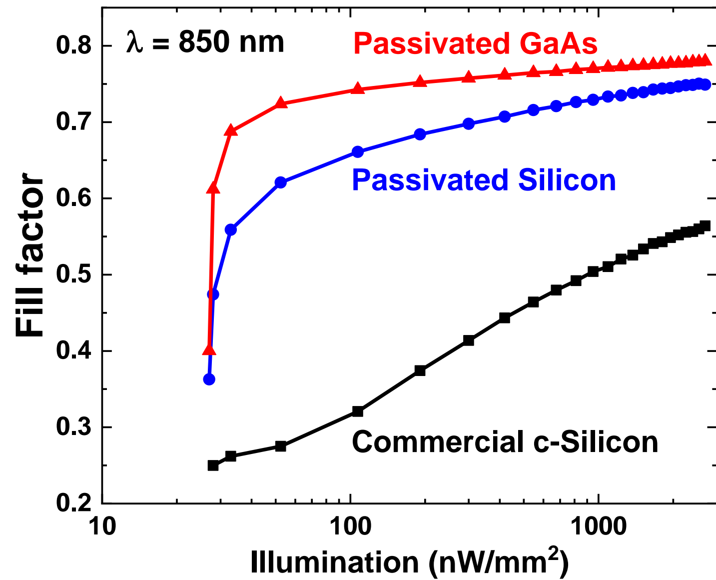
(b)

Figure 3.12. Measured current density versus applied voltage characteristics with corresponding maximum power conversion efficiency and comparison to Shockley–Queisser model, device simulation with no surface and sidewall recombination losses and commercial silicon PV (IXYS Corporation: KXOB22-12X1, [42]) under (a) NIR illumination and (b) white LED illumination.

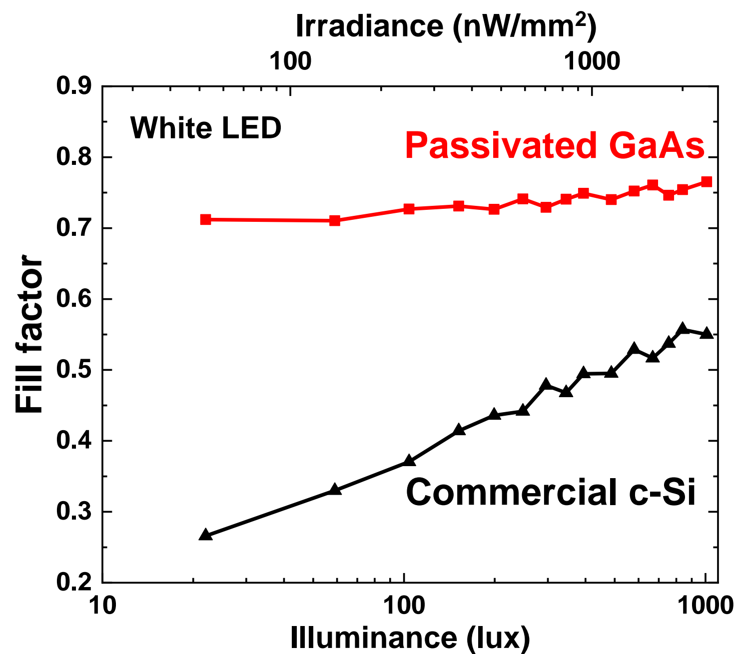
3.5. Discussion

The power conversion efficiency for a 6.4 mm^2 cell is greater than 30 % under 850 nm NIR illumination at 660 nW/mm^2 and around 20 % under white LED illumination at 580 lux (1.38 μW/mm^2) through the optimization of device structure and improvement in V_{OC} from optimized sidewall passivation studies using $(NH_4)_2S$ and PECVD Si_3N_4. This efficiency approaches the expected value from simulation results using a 2D device schematic and well-established material parameters of GaAs with no surface and sidewall recombination losses, as shown in Fig. 3.12. The parasitic shunt resistance of optimized GaAs PV cell is on the order of 10 MΩ-cm^2 range as shown in Fig. 3.11, which can sufficiently overcome the shunt resistance degradation in fill factor under variable visible and NIR illumination conditions in compassion to commercial silicon PV cell that show a drastic fill factor degradation as shown in Fig. 3.13. Furthermore, our silicon PV cell that

was discussed in previous Chapter 2 maintained the similar fill factor values for GaAs under extremely dim light condition due to well-optimized passivation studies on the surface and sidewall using LPCVD Si_3N_4 [32] as shown in Fig. 3.13 (a), suggesting that silicon PV cells can also overcome the shunt resistance degradation using a proper passivation layer for low-flux device operating conditions.



(a)



(b)

Figure 3.13. Measured fill factor versus variable (a) NIR and (b) white LED illumination conditions, compared to commercial c-Si cell (IXYS Corporation: KXOB22-12X1, [42]) and our custom silicon PV cell (discussed in Chapter 2) with well-optimized LPCVD Si3N4 passivation.

The J_0 and J_{02} values extracted from dark *J-V* measurements are gradually increased with increasing P/A ratio, which shows a dramatic reduction in dark current from 1.934 to 0.1409 pA/mm^2 for the bulk recombination current and from 0.4882 to 0.1714 pA/mm for the perimeter recombination coefficient from the $(NH_4)_2S$ treatment encapsulated with PECVD Si_3N_4, attributed to the sulfur passivation of surface states [49-51]. The measured V_{OC} values in Fig. 3.14 agree with theoretically calculated values using the extracted diode parameters in Table 3.2 with the fixed EQE of photogenerated current for variable size PV cells, showing a reduction from the increased reverse saturation current originated from sidewall/perimeter recombination losses. The deviation of measured V_{OC} for small PV cells below 200 µm sidewall length is relevant to J_{SC} degradation.

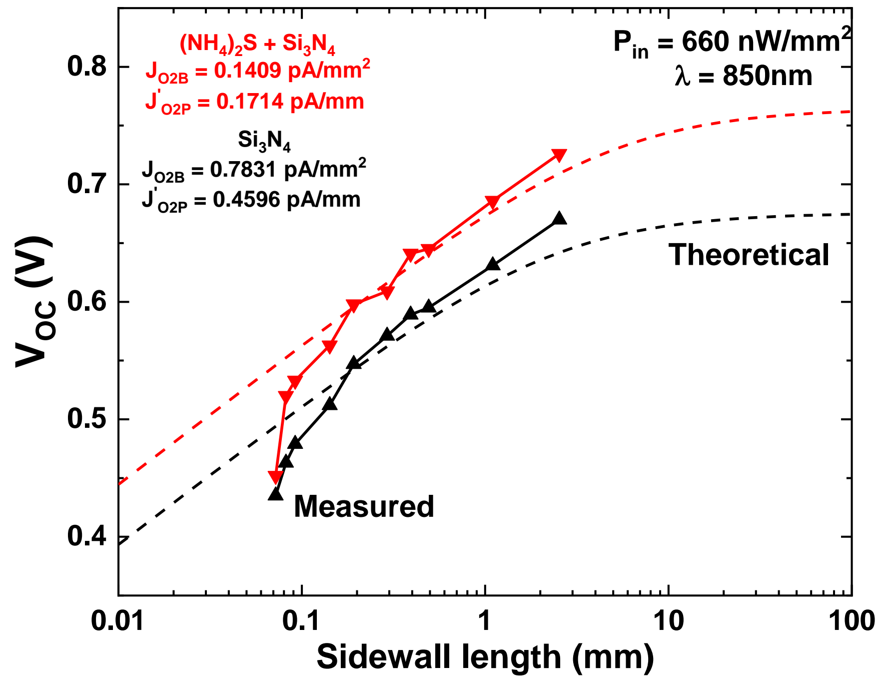


Figure 3.14. Comparison with calculated (dashed) and measured V_{OC} values for square GaAs cells with varying the sidewall length.

The measured J_{SC} values as shown in Fig. 3.15 exhibit a sharp drop as cell size decreases though theoretical J_{SC} should be independent of device size. One of the major J_{SC} limiting factors for small PV cells is optical shadowing from metal fingers, pads and interconnects in the dark harvesting area, suggesting a novel device design using vertical dual junction (discussed in Chapter 6) for extremely small PV cells at sub-mm scale.

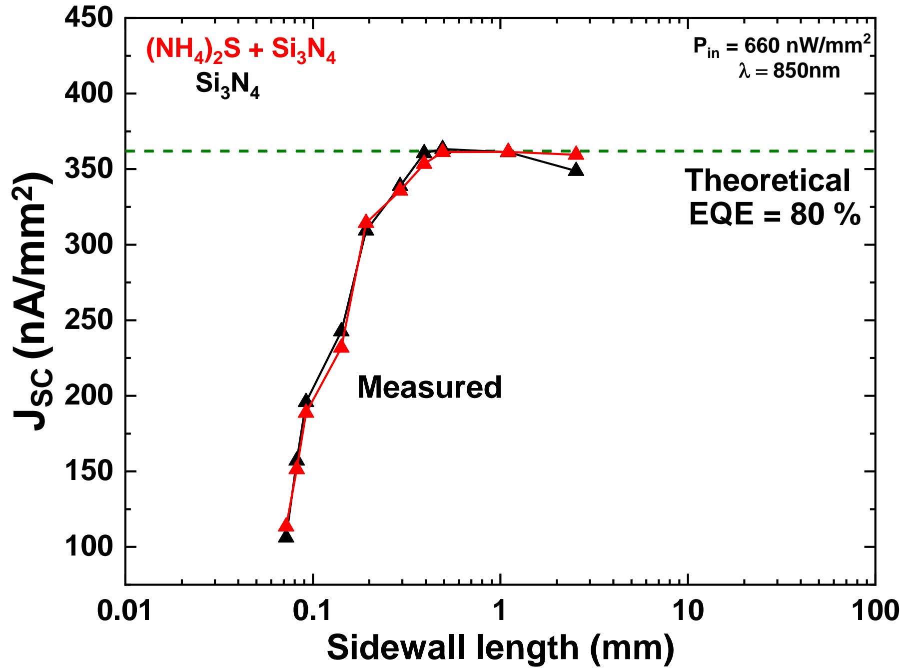


Figure 3.15. Comparison with calculated (dashed) and measured J_{SC} values for square GaAs cells with varying the sidewall length, assuming the fixed EQE around 80 % for theoretical calculation.

The overall power conversion efficiency values are shown in Fig. 3.16, and are limited by factors including an unavoidable sidewall recombination loss, optical shadowing from metal pads and deal area near sidewall. Therefore, further improvements in power conversion efficiency approaching Shockley–Queisser (SQ) limit [41] assuming complete absorption of all photons above band gap, no non-radiative recombination losses and lossless collection of excited carriers indicated in Fig. 3.12 will require continued reduction in edge effects, where the surface and sidewall passivation using wide bandgap materials matched to the lattice constant of GaAs such

as InGaP [58] or AlGaAs [59] may be required. The surface reflectance from metal pads might be reduced from transparent metal anode contacts such as Indium Tin Oxide (ITO) [60], Aluminum-doped Zinc Oxide (AZO) [60] or Ti/ITO [58]. Overall, single GaAs PV cells showed superior device performances than silicon PV cells compared to custom (discussed in Chapter 2) and commercial silicon PV cells (IXYS Corporation: KXOB22-12X1) [32] under broad illumination conditions as shown in Fig. 3.17 due to higher output voltage originated from the material characteristics, which is promising for more sophisticated device structures such as PV array and multi-junction PV cells.

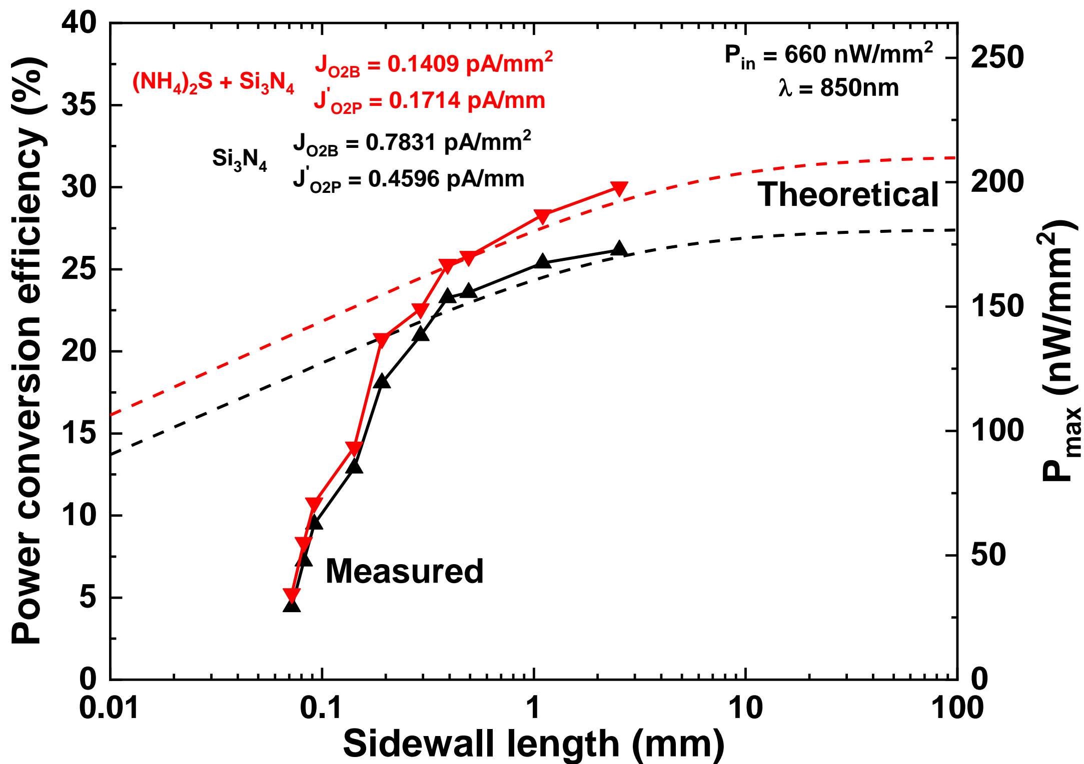


Figure 3.16. Comparison with calculated (dashed) and measured power conversion efficiency values for square GaAs cells with varying the sidewall length.

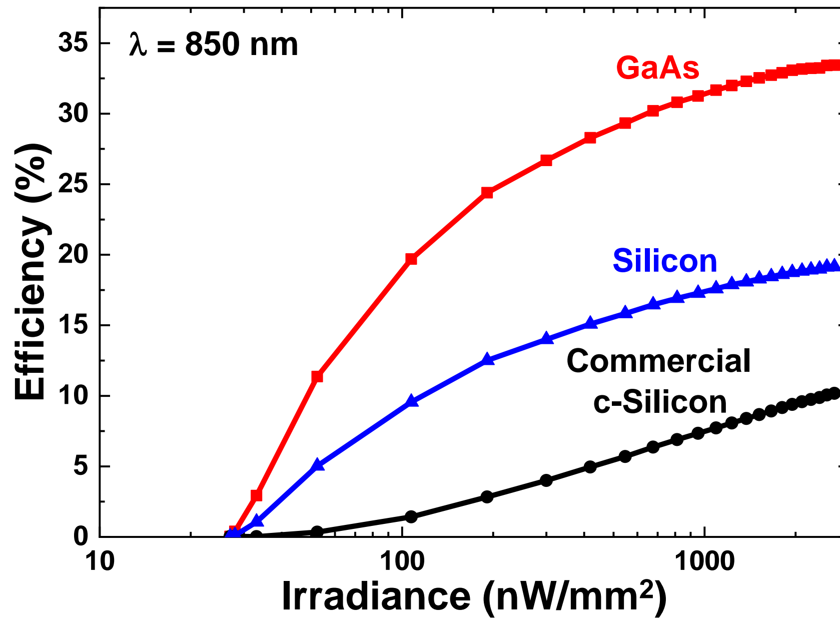


Figure 3.17. Measured efficiency versus variable NIR LED illumination conditions, compared to commercial c-Si cell (IXYS Corporation: KXOB22-12X1, [32]) and our custom silicon PV cell (discussed in Chapter 2) with well-optimized LPCVD Si3N4 passivation.

3.6. Conclusion

GaAs photovoltaic cells at mm-scale and μm-scale were optimized for wireless energy harvesting applications for mm-scale systems. Power conversion efficiency values beyond 30 % under low-flux NIR illumination below 1 $\mu W/mm^2$ and around 20 % under indoor lighting around 600 lux were achieved. The $(NH_4)_2S$ and PECVD Si_3N_4 passivation methods improved the device performance dramatically by reducing the surface/sidewall recombination losses. The optimized device structure was free of performance degradation from shunt leakage under low-flux illumination. High efficiency GaAs photovoltaic cell under low-flux illumination makes wireless photovoltaic energy harvesting for mm-scale systems into a feasible approach, where further improvements may be accomplished by further reduction in edge effects and optical shadowing from electrical contacts.

CHAPTER 4

Subcutaneous Photovoltaic Energy Harvesting

4.1. Introduction

Wireless biomedical implantable devices are prospective technologies that can be applied to a variety of applications for monitoring physiological variables [61-64]. For these implantable applications, low-power systems on the mm-scale [8,65-68] with efficient energy harvesters from ambient and stable sources are essential to make these technologies practical. Several different energy sources utilizing thermal energy [3,69,70] and mechanical vibrations [4,71,72], and radio-frequency (RF) electromagnetic radiation [5,6,73-75] have been evaluated and tested, though miniaturization and reliability / stability of the ambient sources are still primary limiting factors. Wireless power transfer via RF inductive coupling [5,6,73-75] is currently used in implantable systems due to highly efficient power transfer around 58 % at 13.56 MHz through the tissue with 250 mm^2 implanted coil area [74]. However, the power transfer efficiency is highly dependent on the distance between primary and secondary coils [74-75], decreasing power transfer efficiency exponentially. Efficiency also decreases dramatically as implantable device size decreases to sub mm-scale and below due to lateral and angular misalignments [76] and weak coupling [75] with mm-scale antenna receivers. An ultrasound source can also safely send power similar to the RF source, having an issue with the miniaturization due to bulky ultrasound transducers. On the other hand, Biological tissue also provides a means of wireless power transfer in the near-infrared (NIR)

spectral region, where there are two optical transparency windows in the 650 nm to 1350 nm range (First: 650 nm ~ 950 nm, Second: 1000 nm ~ 1350 nm) [20,77,78]. Photovoltaic cells can efficiently convert in this NIR spectral region [29,46] with external quantum efficiency (EQE) approaching 100 %, and are commonly utilized for high-efficiency solar cells. Photovoltaic cells for NIR subcutaneous energy harvesting face challenges in achieving high efficiency under low irradiance conditions in cells of small area, where shunt conductance [13,33] and perimeter recombination losses can dramatically degrade performance [13]. Such cells are far more sensitive to shunt and recombination losses in comparison to solar cells that are typically cm-scale or larger and operating under irradiance that is orders of magnitude higher. Previous work on NIR photovoltaic infrared energy harvesting for biomedical implants [44] utilized PV cells on the cm-scale utilizing relatively high laser light irradiation (mW range), comparable to the intensity used for laser therapy treatments [23]. Here we demonstrate that our silicon and GaAs photovoltaic cells at mm-scale from previous chapters can meet practical requirements for subcutaneous energy harvesting and provide power densities needed for the perpetual operation of implantable devices via low-level irradiation at a wavelength of 850 nm in a through-tissue configuration.

4.2. Optical properties of biological tissues

The optical properties of biological tissues are important to estimate the light propagation, absorption and scattering through various tissue types as shown in Fig. 4.1. for the feasibility of subcutaneous energy harvesting and designing highly efficient PV cells. The optical properties of tissues [20,79,80] are determined in terms of the absorption coefficient, μ_a (cm^{-1}), the scattering coefficient μ_s (cm^{-1}), the scattering function $p\,(\theta,\ \psi)$ (sr^{-1}) where θ is the deflection angle of scatter and ψ is the azimuthal angle of scatter and the refractive index of the tissue n'. For thicker tissues

where the orientations of scattering are random due to multiple scattering events, the dependent of ψ is averaged and ignored. The averaged θ through the multiple scattering is described by the anisotropy of scatter $g=<cos\theta>$. These optical coefficients are subject to variations in blood, water, collagen and fiber contents.

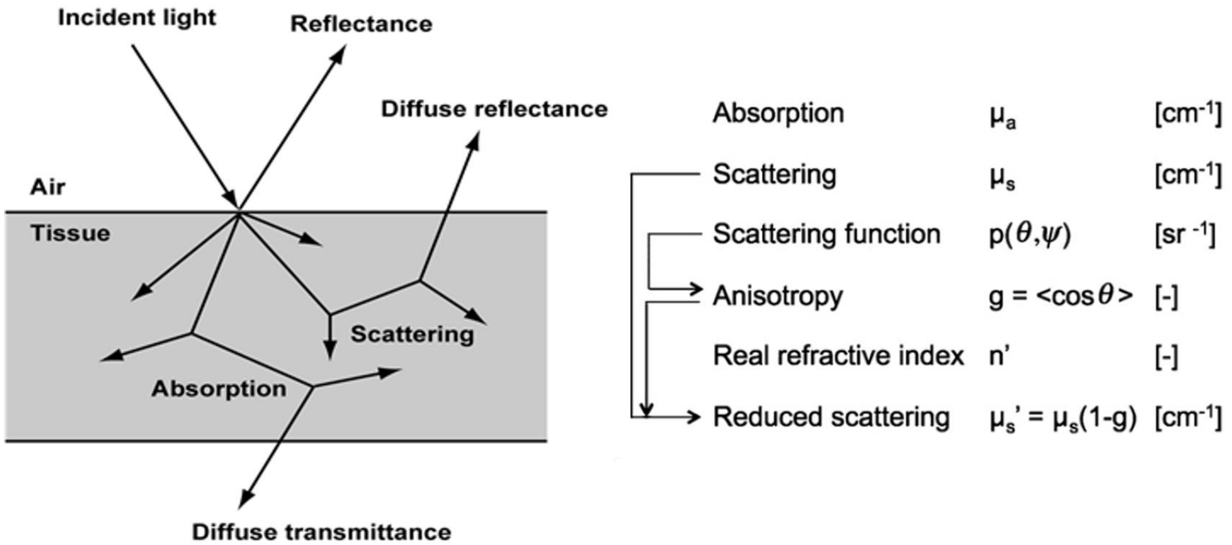


Figure 4.1. The light propagation and the optical properties of biological tissues (adopted from [79,81]).

The measured optical properties of tissues including oxygenated blood, deoxygenated blood, skin and fatty tissues in Fig. 4.2 showed that absorption and scattering from several tissues were lowest in the NIR regions between 650 nm and 1350 nm [20,79], which are called optical transparency windows of biological tissue (First: 650 nm ~ 950 nm, Second: 1000 nm ~ 1350 nm). The peak at the absorption between 950 nm and 1000 nm is from the water in the blood. At wavelengths longer than 1350 nm, the absorption by water and lipids is also increased. Silicon and GaAs photovoltaic cells can efficiently covert the NIR wavelength range that is well matched to the first transparency window of biological tissues.

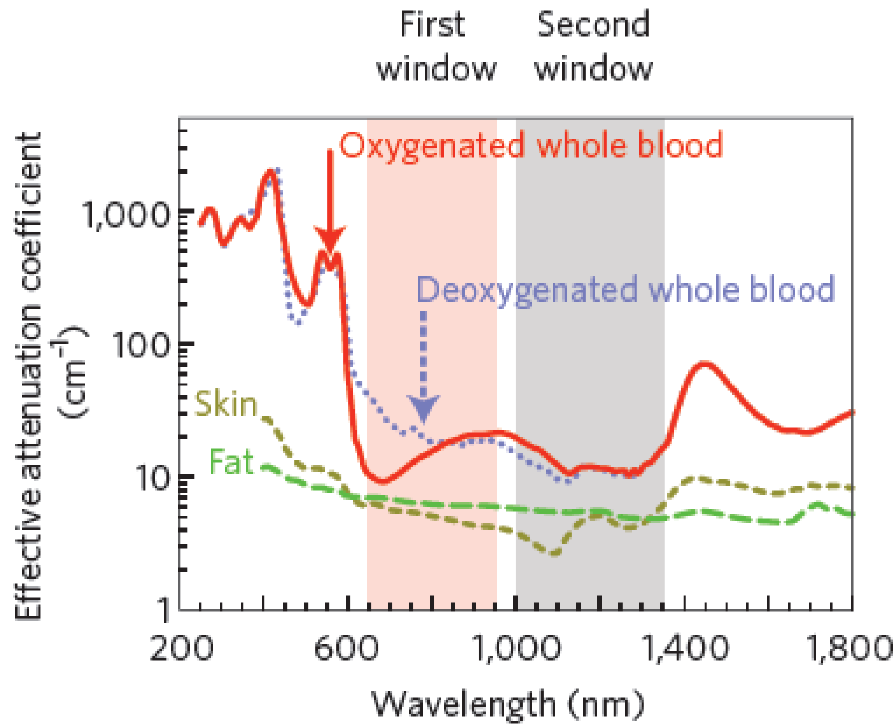


Figure 4.2. Optical properties of biological tissues, illustrating the optical transparency windows in NIR wavelength ranges (adopted from [20]).

4.3. Maximum NIR exposure limit

The maximum NIR exposure limit connected to the corresponding tissue temperature increase due to NIR illumination is a key issue for PV energy harvesting under subcutaneous conditions, following the American National Standards Institute (ANSI) standards [82]. We performed experiments to compare our results to ANSI standards. We implanted a micro temperature probe [83] beneath the dura and measured the temperature rise of the surrounding tissue in response to NIR LED irradiation in a post-craniotomy ex vivo feline. The measured temperature was increased around 2.5 ºC for input irradiation at 0.8 mW/mm^2 over a 20 minute NIR LED irradiation at 850 nm wavelength as shown in Fig. 4.3. This temperature increase is expected to be a worst-case scenario, since active blood flow in cerebral tissue and cerebrospinal

fluid will aid in maintaining temperature. Given this measurement, the maximum NIR exposure limit at 850 nm wavelength was around 0.64 mW/mm^2 (below the NIR limit of 1.36 mW/mm^2 using ocular extended sources from ANSI [82]) to achieve a temperature increase of ~2 ºC which is the recommended temperature limit for biological tissues [84].

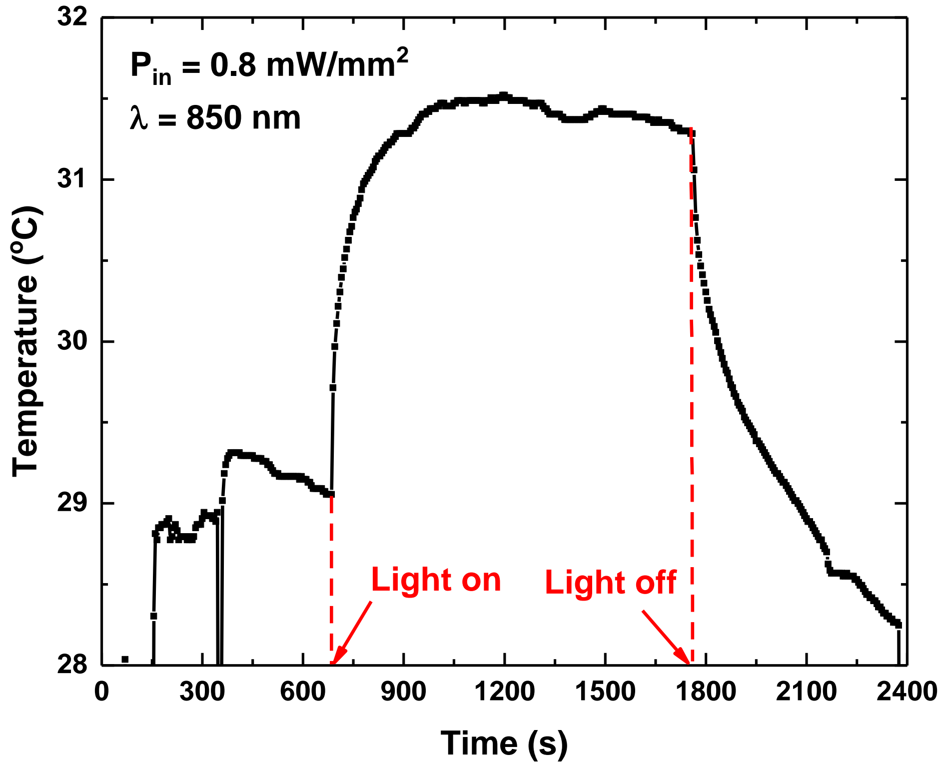


Figure 4.3. Measured temperature of post-craniotomy subdural feline brain tissue under 850 nm NIR irradiation over 10 min exposure.

4.4. Cell performance under NIR illumination

We have studied both silicon and GaAs PV cells in previous chapters, where silicon offers advantages of compatibility with microelectronics technology, while GaAs offers superior light absorption properties, low dark current, and high shunt resistance. The silicon and GaAs PV cell designs were optimized for NIR illumination conditions using device simulations. The optimized

device parameters for silicon and GaAs PVs under low-flux NIR illumination between 800 nm and 850 nm are summarized in Table I.

Material	Silicon		GaAs		
Parameter	Type	Value	Type	Value	Unit
Base thickness	p	35	n	2.75	μm
Base doping	p	2×10^{17}	n	10^{17}	cm^{-3}
Emitter thickness	n	0.34	p	0.5	μm
Emitter doping	n	2.5×10^{16}	p	4×10^{18}	cm^{-3}
Anti-reflection Si_3N_4 layer	-	100	-	100	nm

Table 4.1. Optimized device parameters of silicon and GaAs PV cells for NIR wavelength.

Fabricated cells utilized highly optimized surface passivation and anti-reflection layers to minimize perimeter recombination effects and the surface reflection at a wavelength of 800 nm; 50 nm low-pressure chemical vapor deposition (LPCVD) Si_3N_4 + 50 nm plasma enhanced chemical vapor deposition (PECVD) Si_3N_4 for Silicon and 100 nm PECVD Si_3N_4 with $(NH_4)_2S$ surface treatment for GaAs. The baseline performance of the PV cells is shown in Fig. 4.4 under 1.06 μW/mm^2 LED irradiance at a wavelength of 850 nm, which is tested under extremely dim irradiance conditions in comparison to AM 1.5 sunlight conditions of 1000 μW/mm^2 and the ANSI maximum exposure limit around 1.36 mW/mm^2 and represents an approximate irradiance scenario for charging under subcutaneous conditions. The current-voltage characteristics are shown in Fig. 4.4, demonstrating power conversion efficiency values of 17.82 % for silicon PV and 31.63 % for GaAs PV. The short circuit current density (J_{SC}) is similar for both silicon and GaAs, indicating similar conversion of the infrared flux to photocurrent.

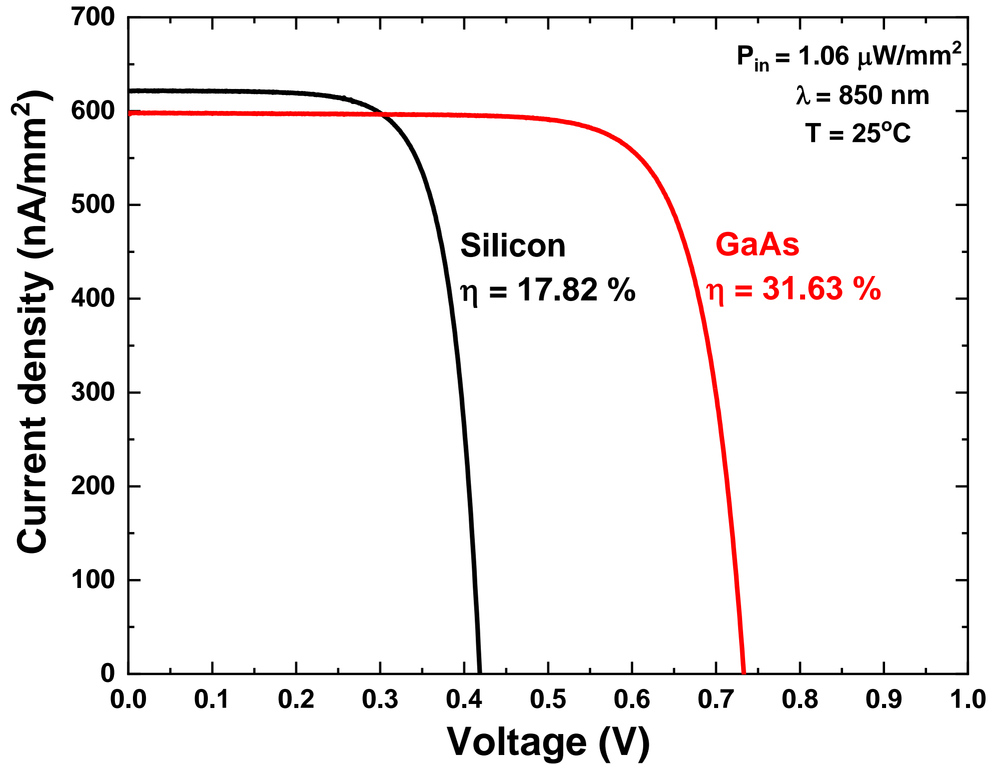


Figure 4.4. Current density versus voltage curves of silicon and GaAs photovoltaic cells under 1.06 μW/mm^2 at 850 nm wavelength and 25 °C.

The external quantum efficiency (EQE) spectra shown in Fig. 4.5 confirms J_{SC} results, with above 80% EQE for both silicon and GaAs over the desired NIR range between 700 nm and 850 nm. The metal fingers used in the cell design are a primary factor limiting J_{SC} and EQE where approximately 7% of the light is reflected by metal coverage on the top surface. The primary difference in power conversion efficiency between silicon and GaAs cells is the variation in open circuit voltage (V_{OC}), which tracks the material bandgap energy. The performance of the silicon and GaAs photovoltaic cells are limited by non-radiative perimeter, surface, and Shockley-Read-Hall (SRH) recombination losses [13] in practical PV devices, reducing the V_{OC} below the theoretical Shockley–Queisser (SQ) limit [41] assuming complete absorption of all photons above band gap, no non-radiative recombination losses and lossless transport of excited carriers. As

shown in Fig. 4.6, while these PV cells demonstrate high power conversion efficiency, the SQ limit is calculated to be 32% for silicon and 53% for GaAs under 660 nW/mm^2 at a wavelength of 850 nm.

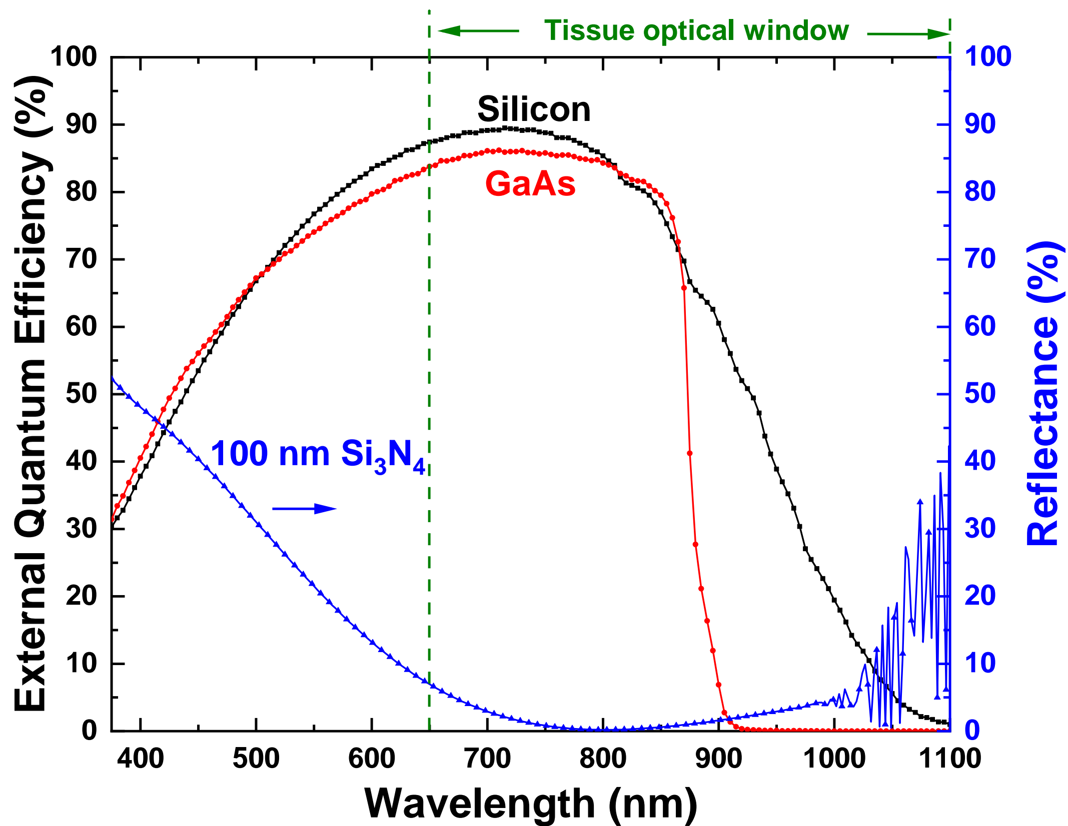


Figure 4.5. External quantum efficiency spectra of silicon and GaAs photovoltaic cells.

4.5. Temperature dependence

The operating temperature of biomedical implantable devices should also be considered, where body temperature ranges between 36 °C and 37 °C, in contrast to the typical room temperature of 25 °C. The increase in operating temperature can degrade the device performance by increasing the thermal carrier generation and corresponding increase in reverse saturation current and decrease in open circuit voltage.

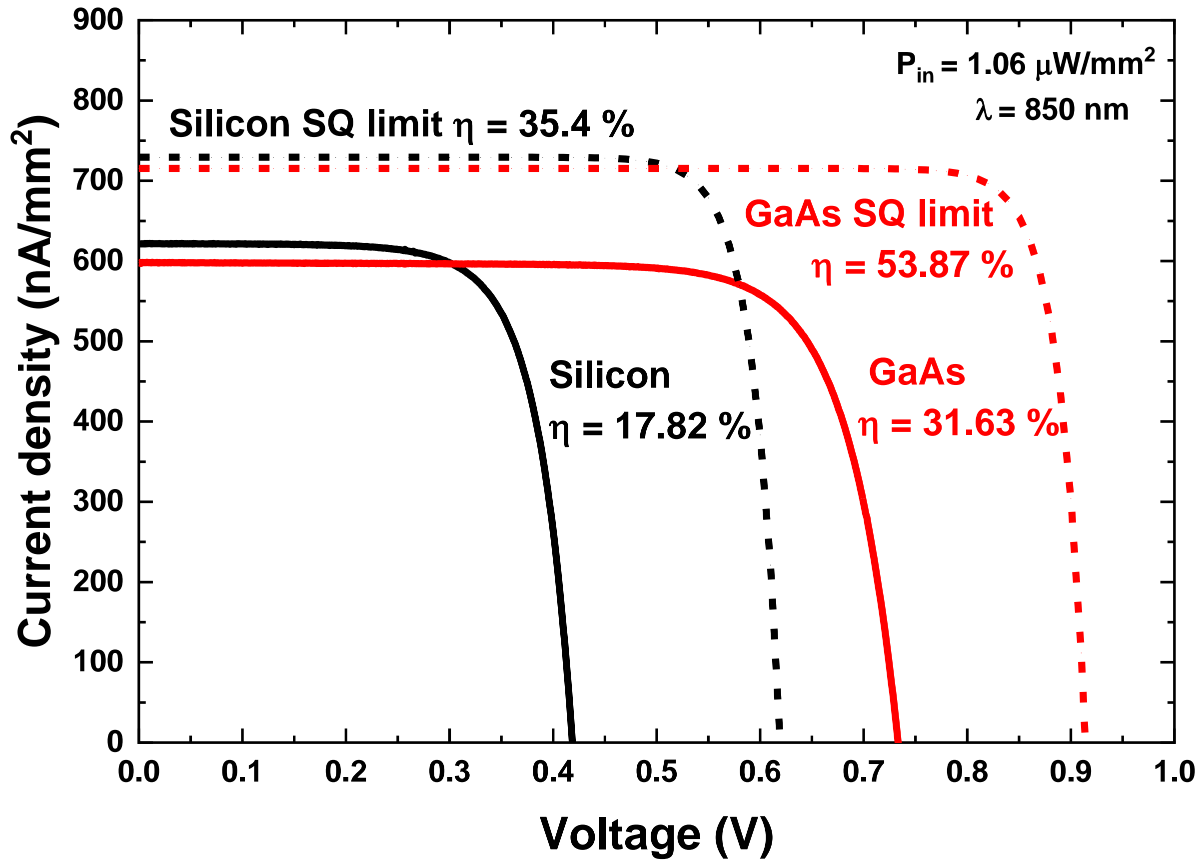
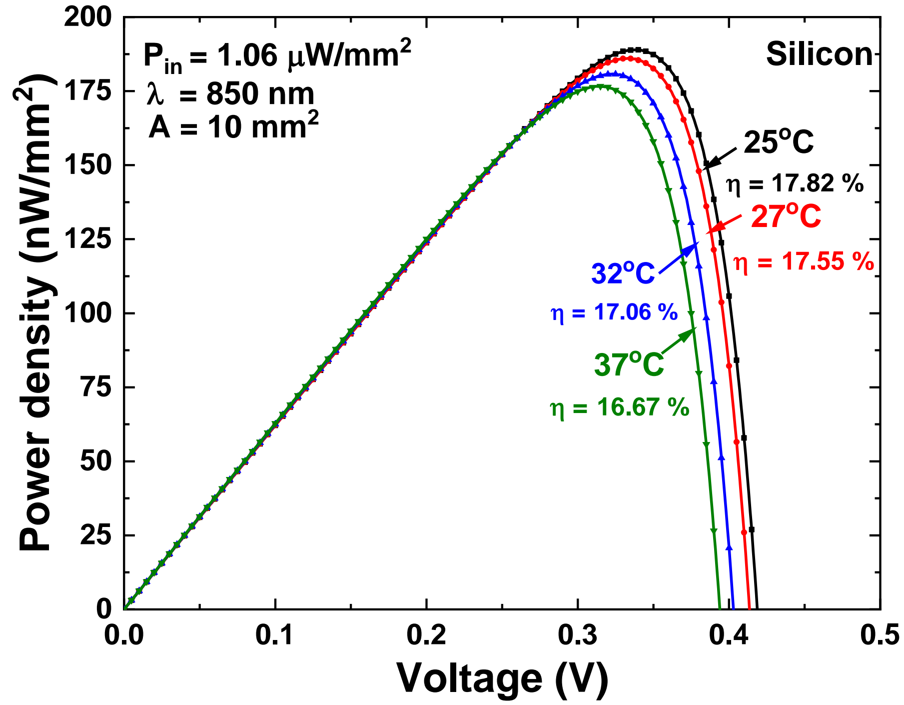
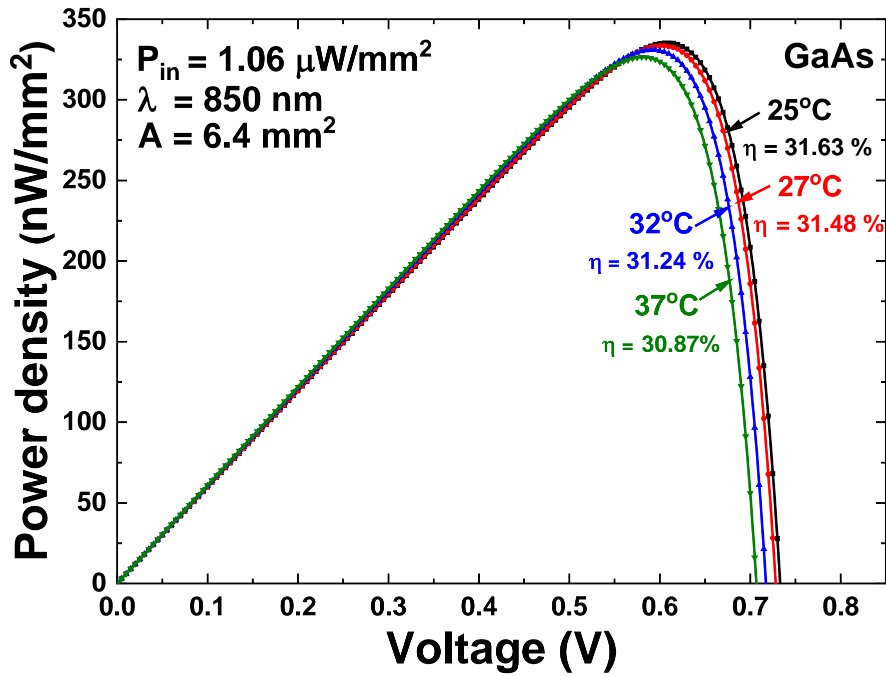


Figure 4.6. Current density versus voltage curves of silicon and GaAs photovoltaic cells and comparison to Shockley–Queisser model under 1.06 μW/mm^2 at 850 nm wavelength.

The temperature dependence of the power density versus voltage is shown in Fig. 4.7 (a) and (b) for silicon and GaAs cells, respectively, exhibiting a reduction in V_{OC} of 2.09 mV/°C for silicon and 2.23 mV/°C for GaAs. The corresponding reduction in the power conversion efficiency in this temperature range is 0.097 %/°C for silicon and 0.069 %/°C for GaAs. These values are consistent with theoretical temperature dependence of PV cells [86] where such minor variations in conversion efficiency can generally be neglected; i.e. room-temperature characteristics provide an adequate representation of energy harvesting performance.



(a)



(b)

Figure 4.7. Temperature dependence of power density versus voltage ranging from room temperature (25 ºC) to conventional body temperature (37 ºC) for (a) Silicon and (b) GaAs.

4.6. Subcutaneous energy harvesting

We tested the feasibility of subcutaneous photovoltaic energy harvesting with variable thickness of tissue models via porcine skin and chicken breast to approximate properties of human skin [86-90] and muscle [78]. Initially, an infrared LED at 850 nm was aligned to photovoltaic cells at a fixed distance and the incident illumination density adjusted by the applied voltage to the infrared LED was scanned using a calibrated photodetector. The tissue samples with variable thickness were placed between the LED and PV cell to measure current-voltage characteristics in a through-tissue configuration. The measured transmittance of tissue samples with variable thickness and the dependence of PV cell output power density on tissue thickness were shown in Fig. 4.8 and 4.9 for irradiation under 1.08 $\mu W/mm^2$ at a wavelength of 850 nm. The chicken breast model exhibits a near linear dependence of transmittance and power density versus thickness rather than an exponential dependence of absorption, which might be caused by the possible variation in thickness of samples.

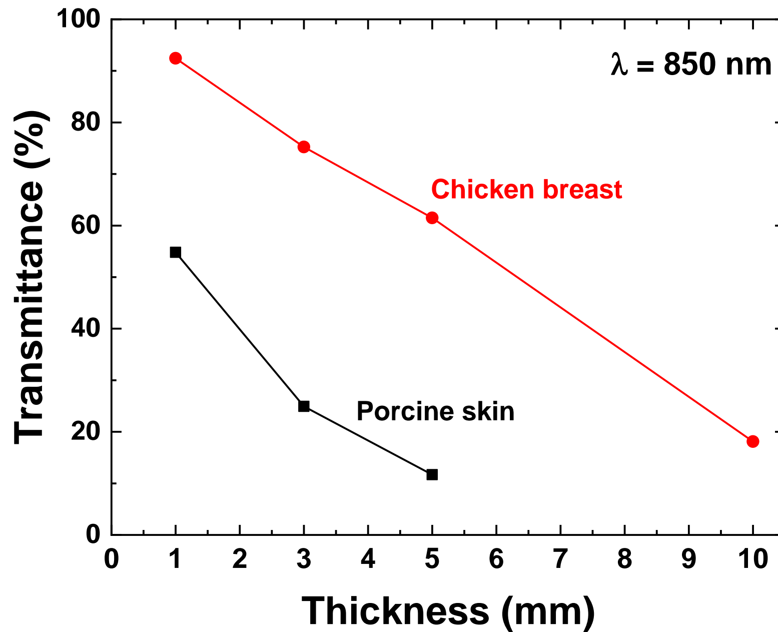
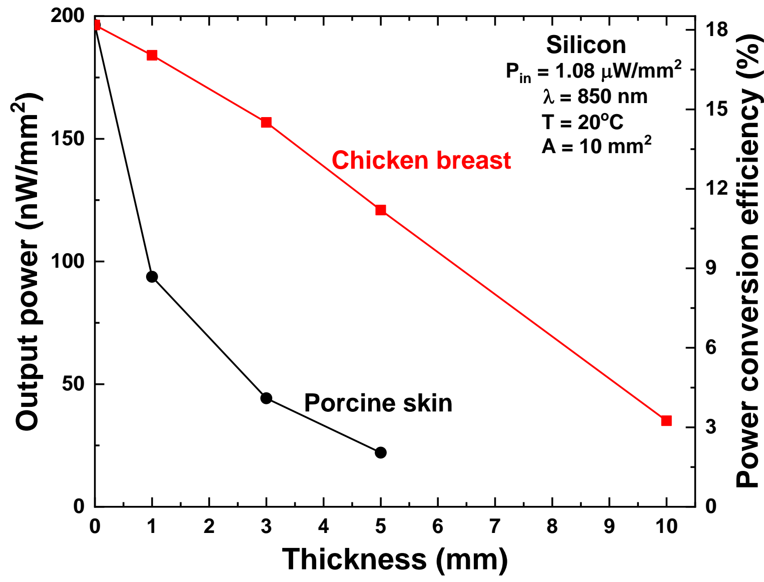
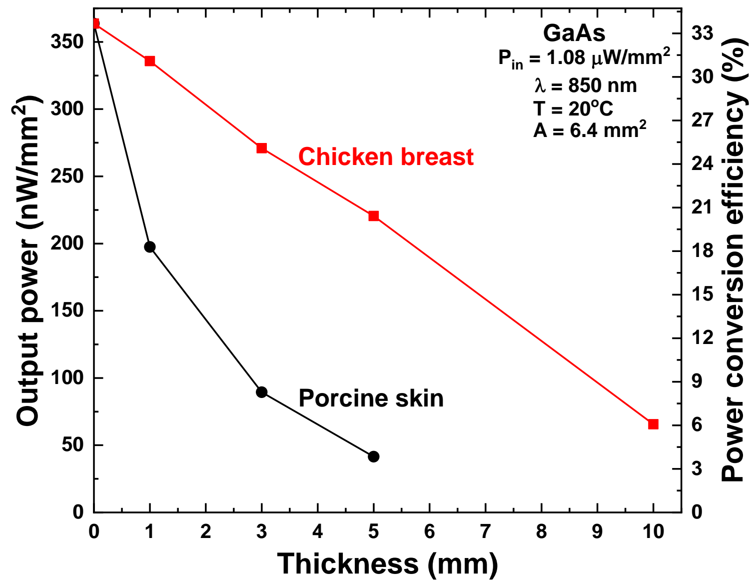


Figure 4.8. Measured transmittance versus thickness of porcine skin and chicken breast under 1.08 $\mu W/mm^2$ at 850 nm wavelength.



(a)



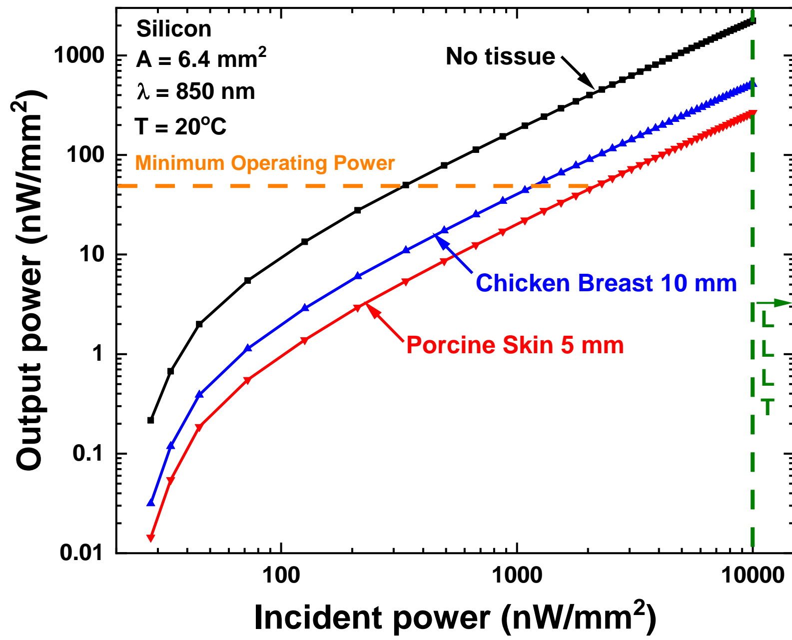
(b)

Figure 4.9. Power conversion efficiency versus thickness of porcine skin and chicken breast for (a) Silicon and (b) GaAs photovoltaic cells under 1.08 μW/mm^2 at 850 nm wavelength.

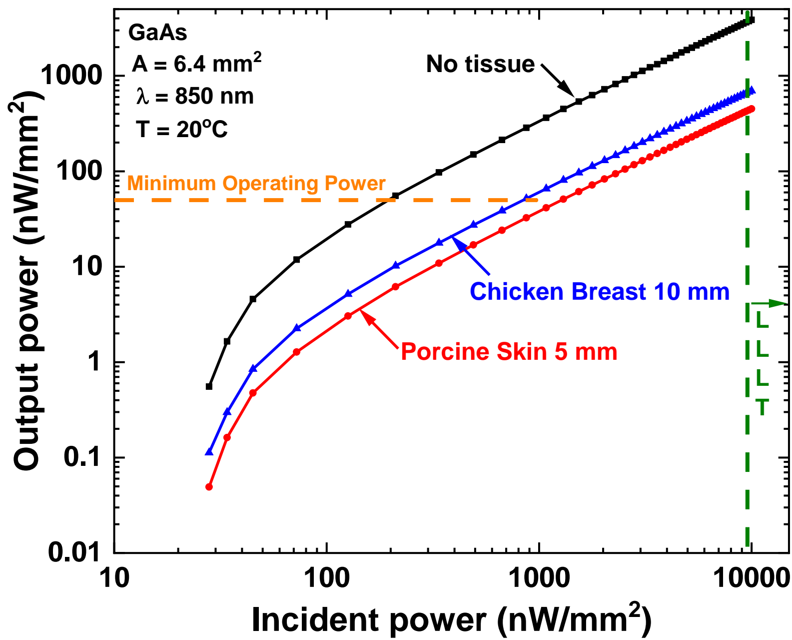
Optical characteristics of chicken breast was roughly extracted by the Beer-Lambert relation [78]:

$$P_{out} = P_0\, e^{-\alpha d} \qquad (1)$$

where *Pout* is the electrical power density produced by the cell, P_0 is the incident infrared power density, α is the attenuation coefficient, and d is the tissue thickness. An extracted attenuation coefficient of the chicken breast sample is around 1.706 cm^{-1} at wavelength of 850 nm. Optical attenuation will occur via absorption and scattering, depending on the cell structure [79], and portions of blood, chromophores and pigments in the tissue. The constant attenuation coefficient for the chicken breast samples suggests a homogeneous medium, providing a good model for optical penetration into uniform soft tissue samples. The attenuation coefficient is similar to prior reports for human skin of 0.37 ± 0.12 cm^{-1} [77] and subcutaneous adipose tissue of 1.1 ± 0.03 cm^{-1} over the wavelength range between 620 nm and 1000 nm, and tumor samples [88] with attenuation coefficients of 3.29 ± 1.02 cm^{-1} and 4.77 ± 0.77 cm^{-1} at 789 nm wavelength. The power density dependence for harvesting through porcine skin exhibits a sharp attenuation near surface, suggesting an inhomogeneous medium. Optical transmission through human skin occurs via three primary layers [77,78,89]: the epidermis (100 μm thick), dermis (1 - 4 mm thick) and subcutaneous fat (1 - 6 mm thick). Attenuation in the epidermis and dermis is dominated by Mie scattering [91] via collagen fibers, where attenuation is reduced for latter propagation in fatty tissue. The porcine skin model therefore represents a good approximation to transmission through skin with high density of collagen fibers [86] in the dermis compared to human skin, and represents a worst case scenario for IR attenuation. The dependence of output power density versus input irradiance is shown in Fig. 4.10 for silicon and GaAs samples of 5 mm porcine skin and 10 mm chicken breast. Above irradiance of approximately 100 nW/mm^2, the harvesting efficiency is approximately constant, corresponding to the linear relationship on the log-log scale of Fig. 4.10. The energy harvesting efficiency decreases below irradiance of 100 nW/mm^2, attributed to the regime where dark current density in the PV cells approaches the photo-generated current.



(a)



(b)

Figure 4.10. Output power versus input power plots for (a) Silicon and (b) GaAs photovoltaic cells through 5 mm porcine skin and 10 mm chicken breast along with minimum 50 nW/mm^2 operating power of low-power microelectronics and minimum 10 μW/mm^2 low-level light therapy (LLLT).

The approximate requirement to power mm-scale systems is 50 nW/mm^2, which is demonstrated for all tissue samples in Fig. 4.10 for irradiance above 2.3 μW/mm^2 for silicon and 1.3 μW/mm^2 for GaAs. This irradiance condition is within an acceptable range of operation, and is below the typical minimum power density of 10 μW/mm^2 that is safely used in low-level laser therapy (LLLT) [23] for medical treatments and below the maximum NIR exposure limit with 1.36 mW/mm^2 from ANSI, and produces a slight rise (below 0.5 °C) in the temperature of tissue / PV with negligible temperature degradations for PVs [45].

We studied a more complex energy harvesting scenario using NIR transmission through a previously dissected mouse to include complex combinations of hair, skin, bone, muscle, and organs. The dissected mouse sample was placed between the LED and PV cell for seven specific sections of the mouse sample, as shown in Fig. 4.11. Energy harvesting was measured using LED irradiance from above, with PV cells placed beneath the mouse. PV performance for the seven locations are summarized in Table II.

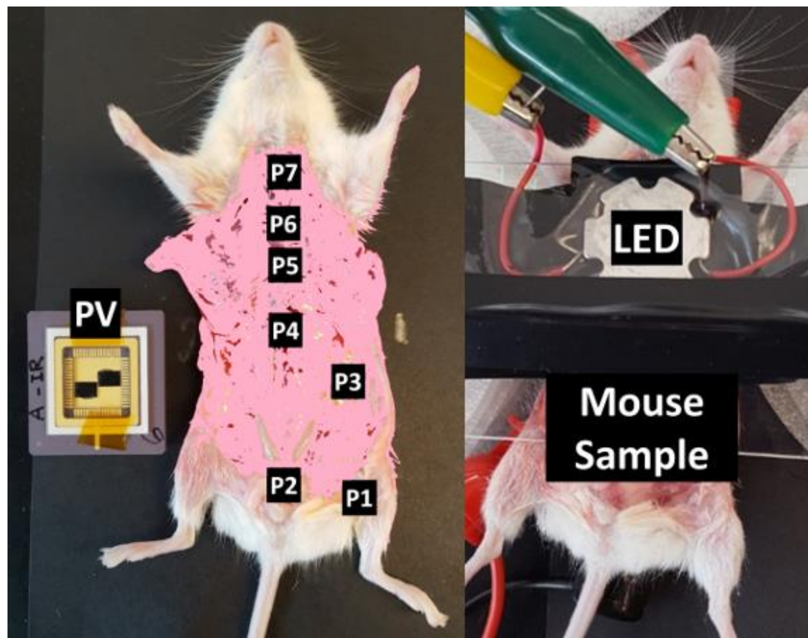


Figure 4.11. Photo of dissected mouse and mounted PV cells used to measure NIR energy harvesting.

#	Thickness [mm]	Input power [μW/mm^2]	GaAs		Silicon	
			Output power [μW/mm^2]	Efficiency [%]	Output power [μW/mm^2]	Efficiency [%]
Point 1	7	134	5.12	3.82	2.82	2.1
Point 2	10	134	2.74	2.05	1.48	1.1
Point 3	4	134	12.24	9.13	7.75	5.79
Point 4	6	134	8.04	6.00	4.85	3.62
Point 5	10	134	3.4	2.53	2.07	1.54
Point 6	12	134	1.19	0.89	0.82	0.61
Point 7	15	134	0.29	0.21	0.17	0.12

Table 4.2. Parameters measured at various locations on the mouse sample.

LED irradiation at 134 μW/mm^2 (within the maximum exposure limit ~ 640 μW/mm^2) demonstrated stable harvesting capabilities at all seven locations. The ability to demonstrate energy harvesting at these locations, particularly point 7, which is a 15mm thick thorax region with high tissue density, shows great promise for infrared power transfer. Our silicon and GaAs cells demonstrate the ability to power biologically implanted mm-scale systems under low NIR irradiance conditions (approximately 1 μW/mm^2). Beyond the power generated by the PV cells, the implantable system will require an interface to directly power the system or to charge a battery. We have previously demonstrated that energy harvesting circuitry can exceed 78 % [92] at similar scale and low-flux conditions using a series/parallel PV network to match the charging voltage required for a battery without the need for voltage up-conversion. Further improvements in the cell structure will require the encapsulation of photovoltaic cells with bio-compatible and transparent polymer packaging materials such as poly(methyl methacrylate) (PMMA) [93] and polydimethylsiloxane (PDMS) [44,94] or glass [95] for long-term stability to reduce the toxicity

concern of arsenic compounds.

4.7. Conclusion

We show that photovoltaic cells at the mm-scale can achieve a power conversion efficiency of more than 17 % for silicon and 31 % for GaAs under 1.06 μW/mm^2 infrared irradiation at 850 nm, which is the extremely dim light condition compared to the maximum exposure limit around 1.36 mW/mm^2 from ANSI and the. These photovoltaic cells demonstrate highly efficient energy harvesting through various biological tissue samples from ambient sunlight, or irradiation from infrared sources such as used in present-day surveillance systems by utilizing the near infrared (NIR) transparency window between the 650 nm and 1350 nm wavelength range. Sufficient power generation above 50 nW/mm^2 is achieved for perpetual operation of mm-scale systems for implant depth of at least 15 mm including hair / skin / muscle / bone under 850 nm NIR illumination at 134 μW/mm^2.

CHAPTER 5

Monolithic GaAs Photovoltaic Modules

5.1. Introduction

The most critical issue in ensuring perpetual operation of systems is the overall power generation. In contrast to large-area applications, cost per unit area is a secondary factor in mm-scale systems due to the small PV area (and hence, low cost). This enables the use of high-performance materials such as III-V compound semiconductors. Furthermore, to maximize energy capacity, the battery of the mm-scale systems often has a high open-circuit voltage, which is several times higher than the typical open circuit voltage of a single photovoltaic cell. A switched capacitor network as shown in Fig. 5.1 (a) is one of the typically used methods to achieve voltage up-conversion, where switching and resistive losses limit efficiency to approximately 50 % [92]. The other prevalent method for voltage up-conversion is to use a large off-chip inductor as shown in Fig. 5.1 (b), interfering with the miniaturization and the integration to mm-scale systems. Direct series/parallel connections of PV cells provide an appealing alternative for voltage up-conversion, where a PV network with over 80 % power conversion efficiency has been demonstrated [92]. However, monolithic PV arrays present several challenges in minimizing losses associated to device isolation and shunt leakage paths between series connections [18,96]. Monolithic silicon PV arrays present several challenges including low voltage generation (large number of series-connected cells required to achieve desired voltage) and low optical absorption strength (thick

absorber regions are required, making device isolation problematic) [18,97]. The larger voltage generation and high optical absorption strength of GaAs and related compound semiconductors provide a much more attractive platform for monolithic PV modules.

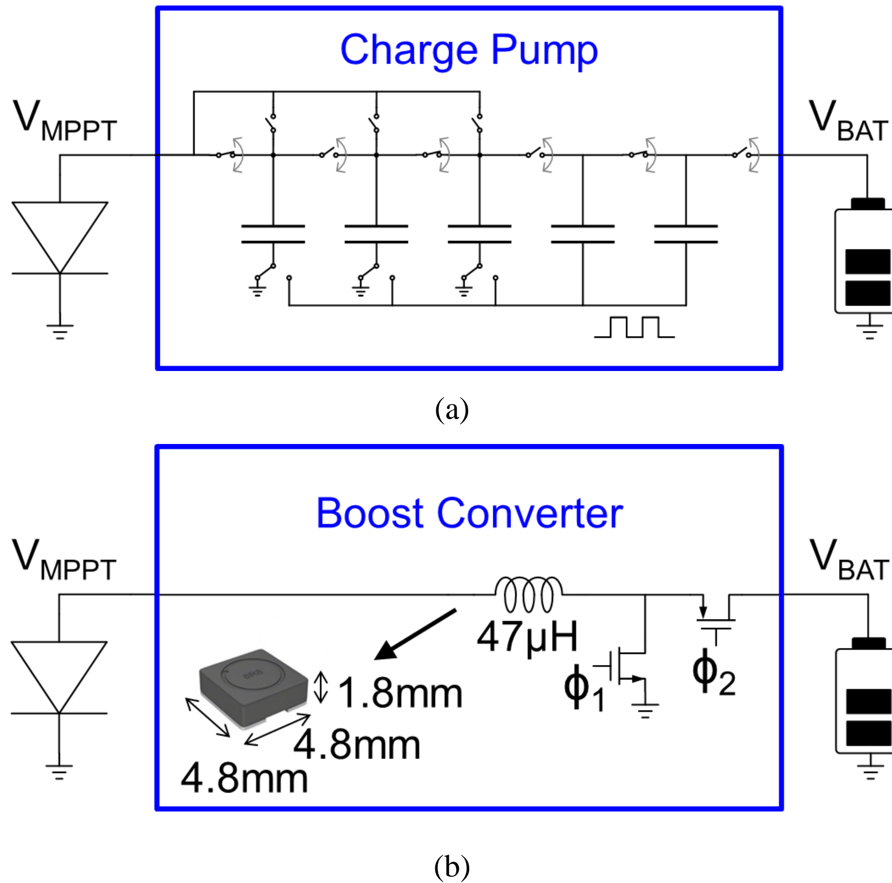


Figure 5.1. Schematic diagrams of (a) a switched capacitor network and (b) a bulk off-chip inductor for the DC-DC voltage up-conversion (adopted from [92]).

Previously, a laser power converter based on a six-cell GaAs PV module array was demonstrated at the mm-scale with conversion efficiency greater than 52 % under monochromatic illumination at 13.2 W/cm^2 (132 mW/mm^2), with efficiency limited by perimeter recombination and shunt leakage through the semi-insulating GaAs substrate [18]. In this work, we present monolithic GaAs-based PV modules at the mm-scale operating under low flux conditions (< 10

μW/mm²) as a means to power IoT systems or bio-implantable sensors without the requirement for DC-DC voltage up-conversion.

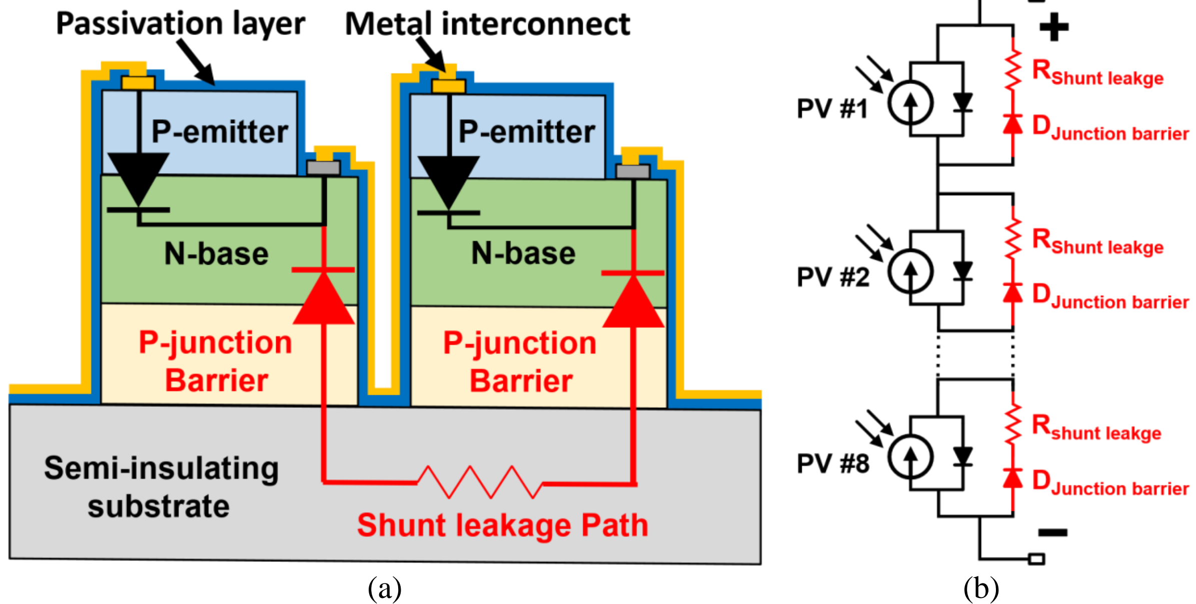


Figure 5.2. Schematic diagrams of (a) device structure illustrating PV cell junction, junction barrier isolation, and shunt leakage path, and (b) equivalent circuit model of the PV module.

5.2. Experiment

We used a baseline PV cell structure (Fig. 3.1 (a)) grown by molecular beam epitaxy (MBE) based on our previously reported high-efficiency single-junction GaAs PV cells, where the critical limiting factor from exposed sidewall/perimeter recombination losses of single PV cells was dramatically reduced utilizing the ammonium sulfide chemical treatment and subsequent silicon nitride deposition. Monolithic PV arrays were constructed on semi-insulating GaAs substrates. While the semi-insulating GaAs substrate provides a high-resistivity material to facilitate series connection of PV cells, there is still a path for shunt leakage current that can degrade the fill factor, as illustrated in Fig. 5.2 (a). We examined three approaches to investigate

shunt current leakage:

1) semi-insulating substrate alone,

2) p-GaAs junction barrier (500 nm thick, 10^{16} cm^{-3} doping)

3) p-$Al_{0.3}Ga_{0.7}As$ junction barrier (400 nm thick, $5x10^{16}$ cm^{-3} doping).

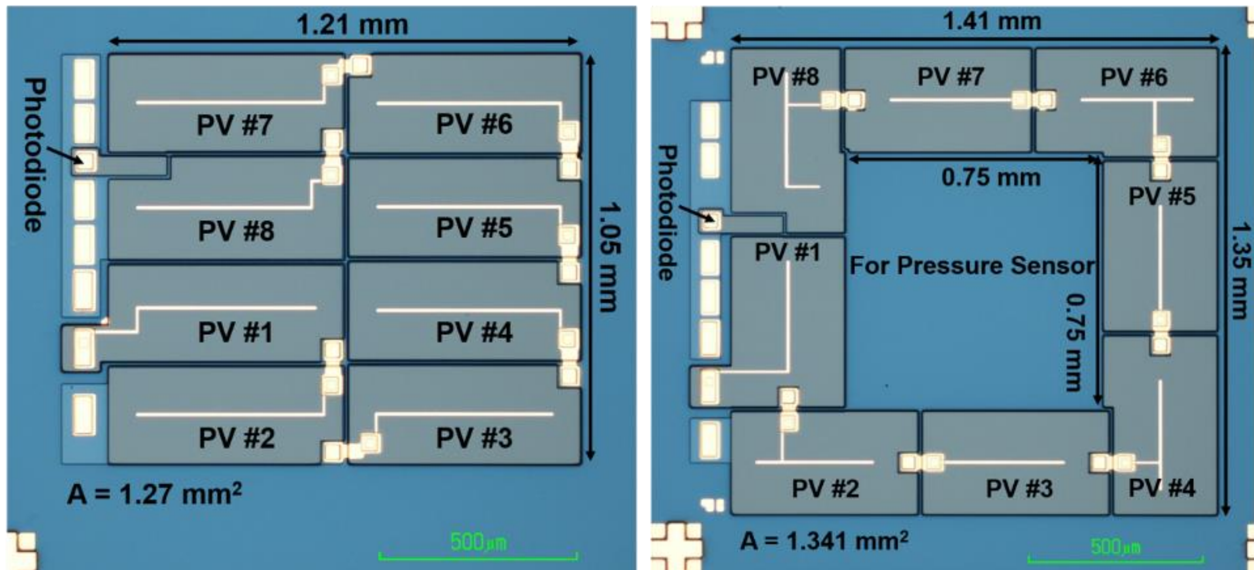


Figure 5.3. Optical microscope images of two different fabricated PV modules.

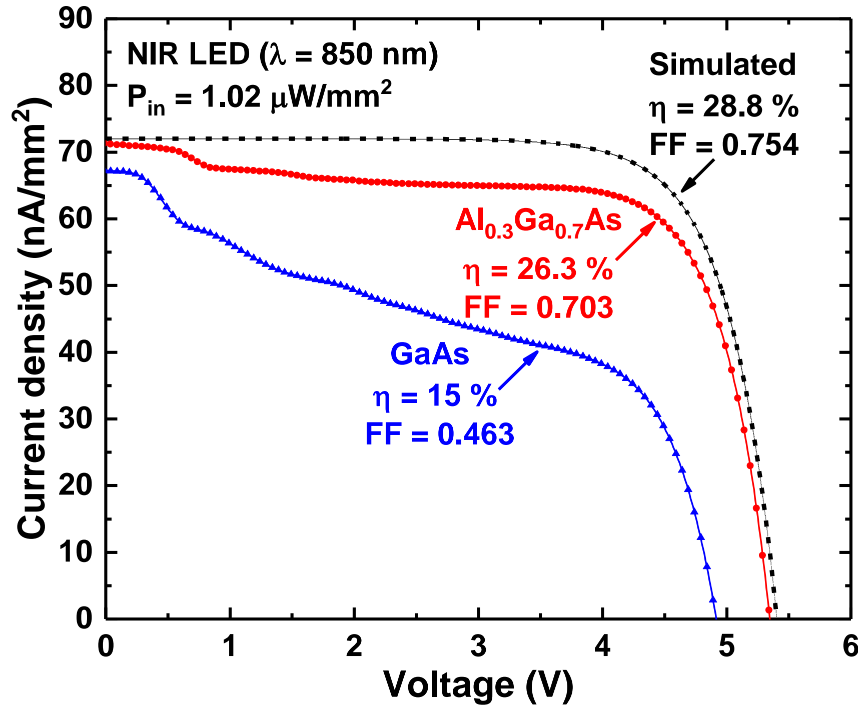
We simulated electrical characteristics for each approach using Synopsys Sentaurus TCAD [30] to obtain optimized parameters for layer thickness, p-type doping concentration, and Al mole fraction. We fabricated PV modules with 8 single PV cells (255 μm x 595 μm) connected in series with 10 μm trenches for device isolation, as shown in Fig. 5.3. The 8-cell series connection was designed to achieve a voltage output of approximately 5 V for direct battery charging. The PV module design also incorporated a small integrated photodiode for optical communications, and the possibility to incorporate an open location to mount an external sensor (e.g., pressure) for the system. We measured the electrical characteristics of the PV modules under dark and illuminated conditions using Keithley 2400 and 4200 semiconductor characterization tools. Illumination

utilized a calibrated white light LED or 850 near-infrared (NIR) LED. The incident LED light intensity was approximately 1 μW/mm^2 (420 lux) to simulate a reasonable indoor or subcutaneous low-flux condition that is approximately 1,000 times smaller than AM 1.5 [12] full sun conditions. We studied incident light dependence by varying the irradiance in increments of 10 lux for white light LED illumination and 100 nW/mm^2 for NIR LED illumination.

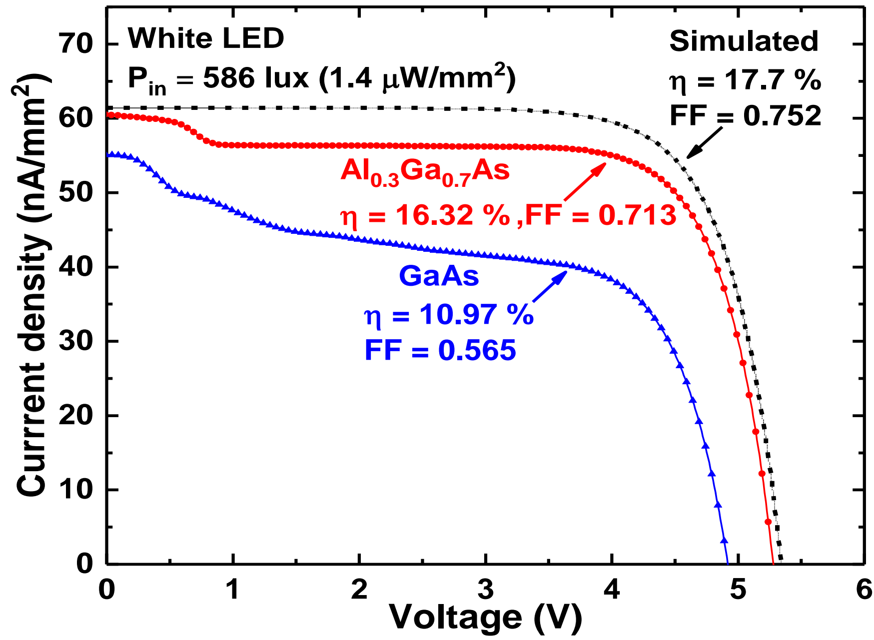
5.3. Results

5.3.1. Junction barrier isolation

The *J*-*V* characteristics of fabricated PV modules with p-GaAs and p-$Al_{0.3}Ga_{0.7}As$ junction barrier isolation are shown in Fig. 5.4 for 850 nm NIR LED illumination at 1.02 μW/mm^2 and white LED illumination at 586 lux (1.4 μW/mm^2).



(a)



(b)

Figure 5.4. Measured J-V characteristics of PV modules with GaAs and AlGaAs barrier layers (a) under 850 nm NIR LED illumination at 1.02 μW/mm^2 and (b) under white LED illumination at 586 lux. Comparisons are shown to simulated results (dashed) with shunt leakage removed.

We extracted diode parameters from single PV cells to simulate the *J-V* characteristics for series-connected cells without shunt leakage, as shown in Fig. 5.4. PV modules with both p-GaAs and p-$Al_{0.3}Ga_{0.7}As$ junction barrier isolation produced an open circuit voltage of approximately 5 V. This voltage is near the intended design, and is sufficient for direct battery charging without voltage up-conversion. The PV module with p-GaAs junction barrier isolation demonstrated a dramatic degradation in fill factor from 0.754 to 0.463 in comparison to simulated *J-V* characteristics neglecting the shunt leakage current. As a result, the overall power conversion efficiency under NIR illumination decreases from the expected value of 28.8 % to 15.0 % due to the inability of the GaAs junction barrier to sufficiently block shunt leakage current. We observed a dramatic improvement in performance by incorporating p-$Al_{0.3}Ga_{0.7}As$ junction barrier isolation,

where the measured power conversion efficiency of 26.3 % under NIR illumination compares favorably to the simulated result of 28.8 % for no shunt leakage.

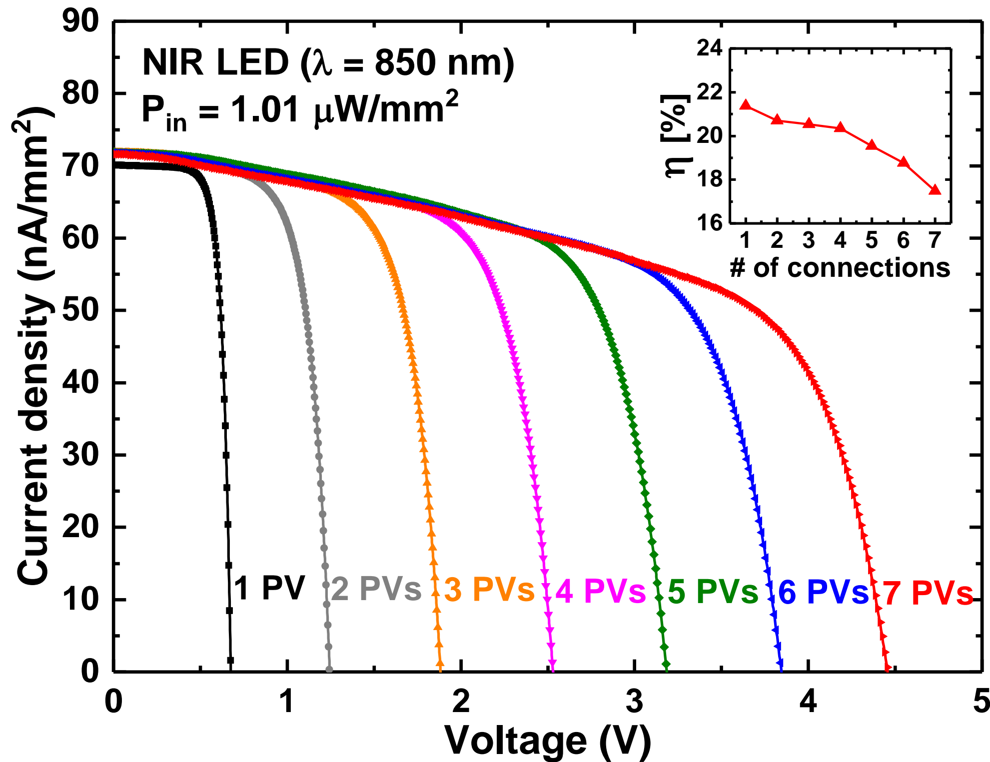


Figure 5.5. Measured *J-V* curves for varying number of PV cell series connection and (inset) corresponding power conversion efficiency at the maximum power point.

The influence of shunt leakage on the performance of monolithic PV modules is further illustrated by the dependence of *J-V* on the number of series-connected cells (p-GaAs junction barrier isolation), as shown in Fig. 5.5. The overall power conversion efficiency for NIR illumination demonstrates a clear decrease from 21.4 % to 17.5 %, with a fill factor decreasing from 0.71 to 0.582, as the number of series connections increases from 1 to 7. The degradation in the *J-V* characteristics shows an obvious shunt leakage characteristic, as represented by the equivalent circuit model shown in Fig. 5.2 (b).

5.3.2. Characteristic of shunt leakage

We measured shunt leakage current between n-contacts of adjacent PV cells without metal interconnects under dark condition for the three device isolation schemes, as shown in Fig. 5.6.

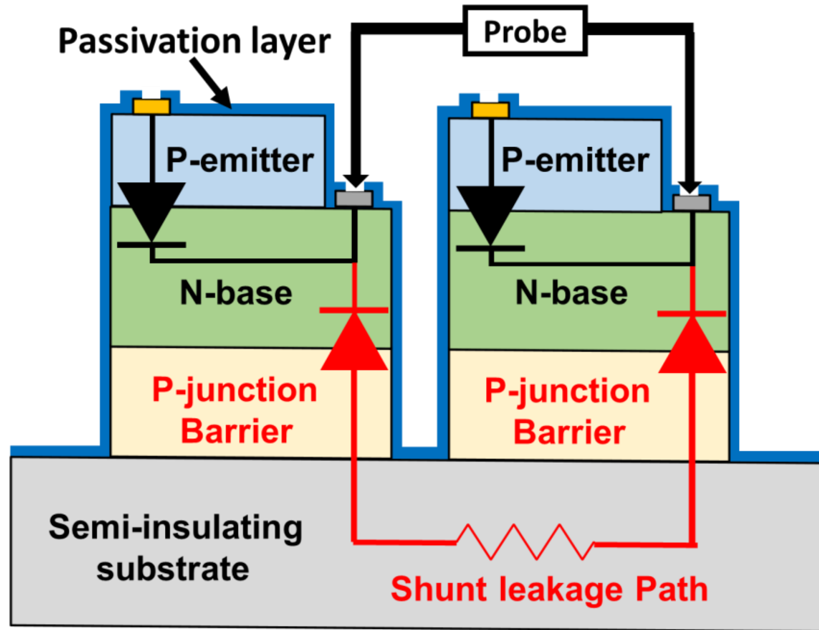
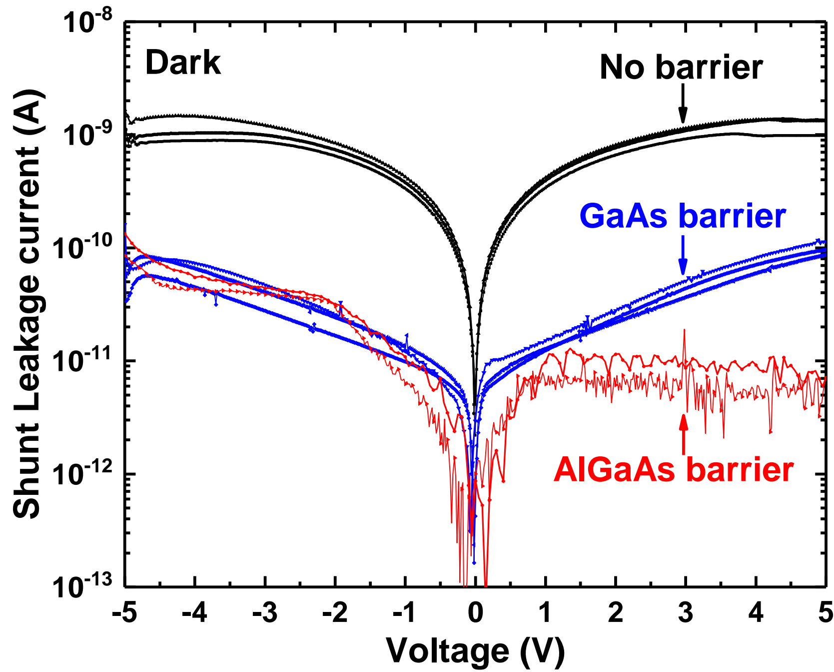
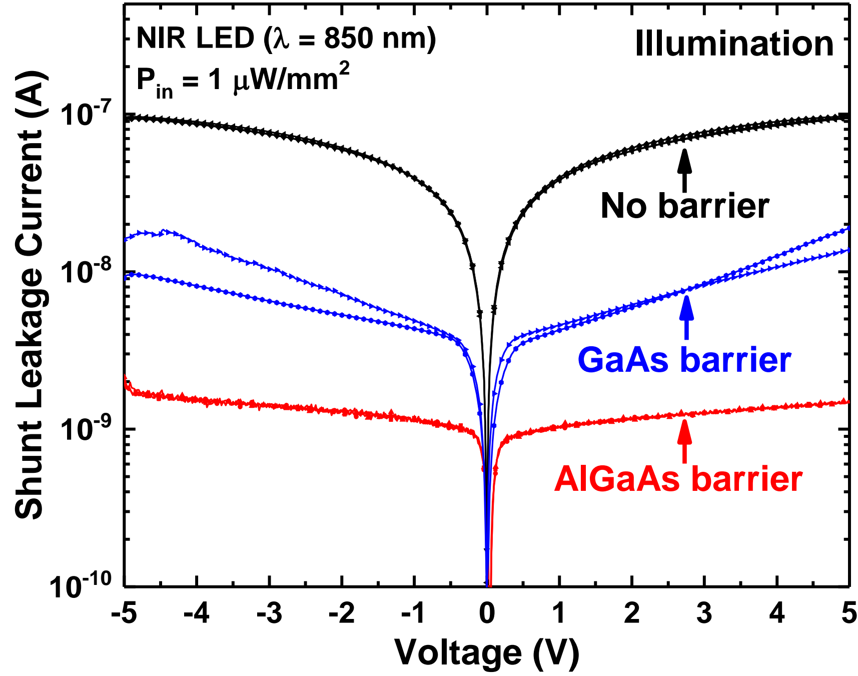


Figure 5.6. Schematic diagram of shunt leakage measurement between bottom n-contacts of adjacent PV cells.



(a)



(b)

Figure 5.7. Measured shunt leakage current under (a) dark and (b) NIR illumination conditions for three different barrier structures: no barrier, p-GaAs junction, and p-$Al_{0.3}Ga_{0.7}As$ junction.

As shown in Fig. 5.7 (a), we observe an approximately linear *I*-*V* characteristic for the shunt current leakage without junction barrier isolation, suggesting that it is limited by the resistance of the semi-insulating GaAs substrate. We observe a clear reduction in shunt leakage current by incorporating p-GaAs and p-AlGaAs junction barrier isolation. The shunt leakage *I*-*V* characteristic for the p-GaAs junction barrier has a near exponential dependence, suggesting that leakage is mediated by the energy barrier height of the p-GaAs junction. We observe a further reduction in shunt leakage for the incorporation of a p-AlGaAs junction barrier isolation, which is near the instrument limitation of 1 pA and may be attributed to the increased energy barrier height. The energy barrier height for the three device isolation designs is illustrated in the simulated energy band diagrams shown in Fig. 5.8. Despite the large reduction in shunt current for the addition of p-GaAs barrier isolation, there is still an obvious degradation in PV module efficiency due to shunt

leakage current (Fig. 5.4). Furthermore, for all three cases of junction barrier isolation, we observe a very low shunt leakage current that is near or below the nA range and would not be expected to dramatically impact PV module efficiency. Therefore, the shunt leakage current characteristics under dark conditions cannot fully explain our observed behavior of the PV modules under illumination.

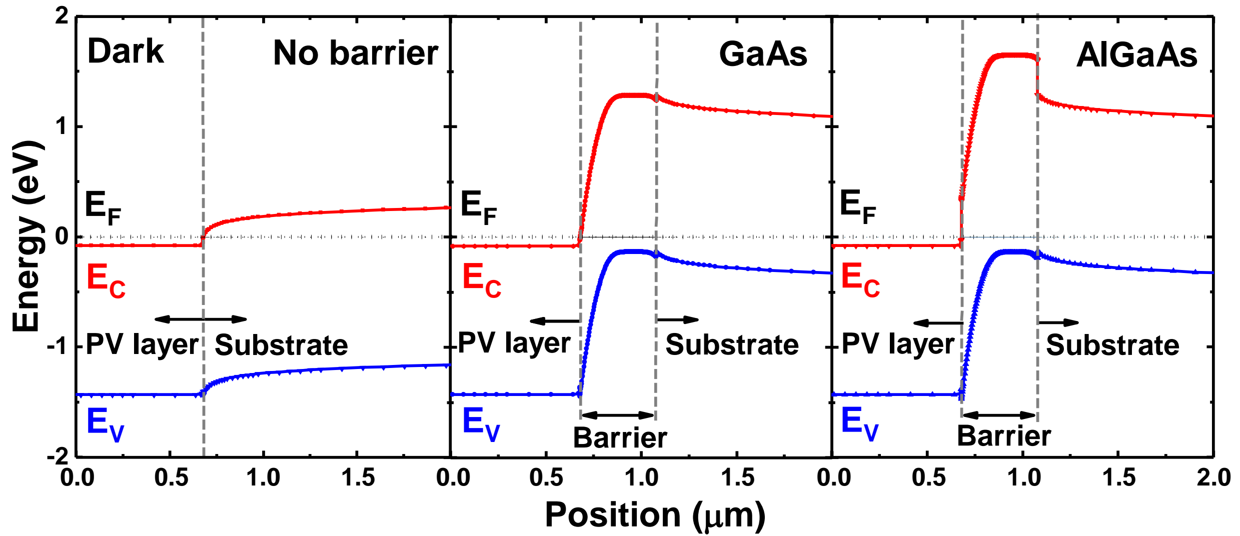


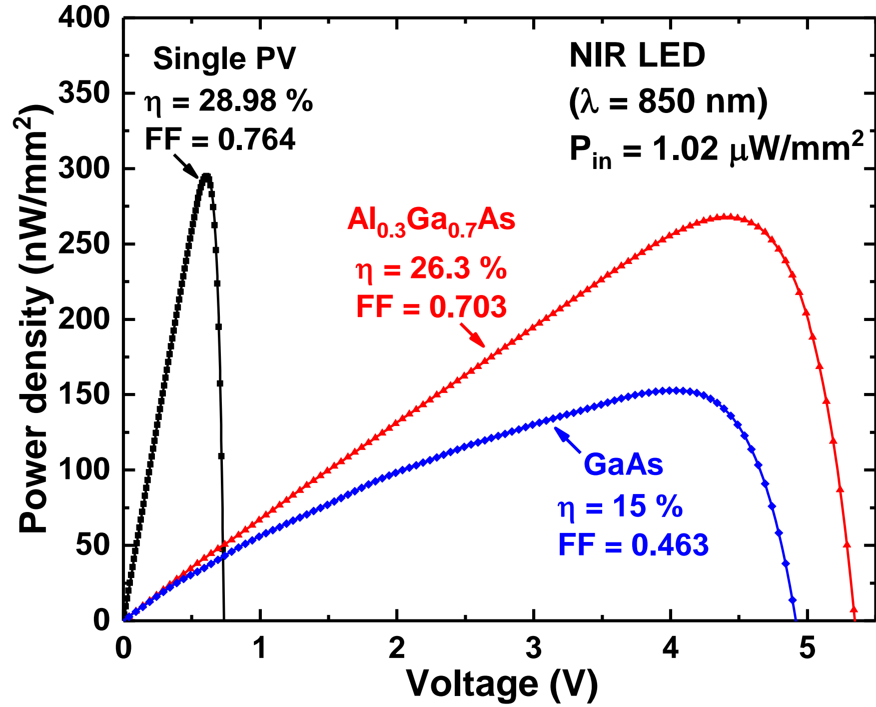
Figure 5.8. Simulated energy band diagrams between the PV cell base and semi-insulating substrate under dark conditions for three different barrier layer structures: no barrier, p- GaAs junction, and p-$Al_{0.3}Ga_{0.7}As$ junction.

We subsequently measured the shunt leakage current between n-contacts of adjacent single PV cells under illumination and observed a substantial increase in leakage current (Fig. 5.7 (b)). The photo-activated behavior may be interpreted as an undesired increase in photoconductivity at the junction barrier and/or exposed regions of the semi-insulating GaAs substrate. We believe that the nonlinear bias dependence of the photo-activated leakage current may explain the nonlinear shunt leakage current observed in the modules shown in Fig. 5.4. For all three junction isolation leakage techniques, the shunt current increased by a factor of approximately 100. The shunt

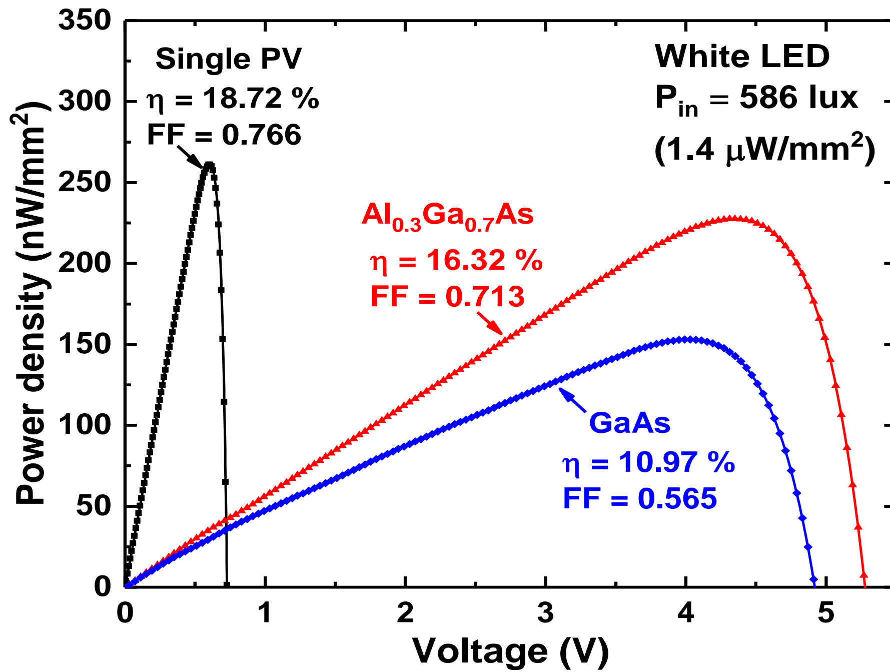
leakage for the p-GaAs junction barrier isolation rises to the level of 10 nA, comparable to the photogenerated current, resulting in the observed reduction in PV module performance due to shunt leakage. In contrast, the larger barrier height associated with our p-AlGaAs junction isolation approach significantly improves the ability to block shunt leakage current under illumination. The p-AlGaAs junction barrier isolation limits the shunt leakage current under illumination to approximately 1 nA, preserving the fill factor and overall power conversion efficiency of PV modules.

5.3.3. Comparison of PV module performance to single PV cell

To gauge the overall power generation of the PV modules, we examined the resulting *P-V* characteristics and compared to a 6.4-mm^2 single PV cell, as shown in Fig. 5.9. The power conversion efficiency of a 1.27-mm^2 PV module with p-AlGaAs junction barrier isolation was 26.3 % under 850 nm infrared LED illumination at 1.02 μW/mm^2 and 16.3 % under white LED indoor conditions at 586 lux (1.4 μW/mm^2). We observed a dramatic decrease in power generation for the p-GaAs junction barrier isolation module, as expected based on the shunt leakage degradation observed in *J-V* characteristics. The power conversion efficiency of the PV module with p-AlGaAs junction barrier isolation, however, approaches the simulated result neglecting shunt leakage current. In comparison to the single PV cell, the PV module with AlGaAs junction barrier isolation provides a voltage that is approximately eight times higher, with approximately 1/8 current reduction.

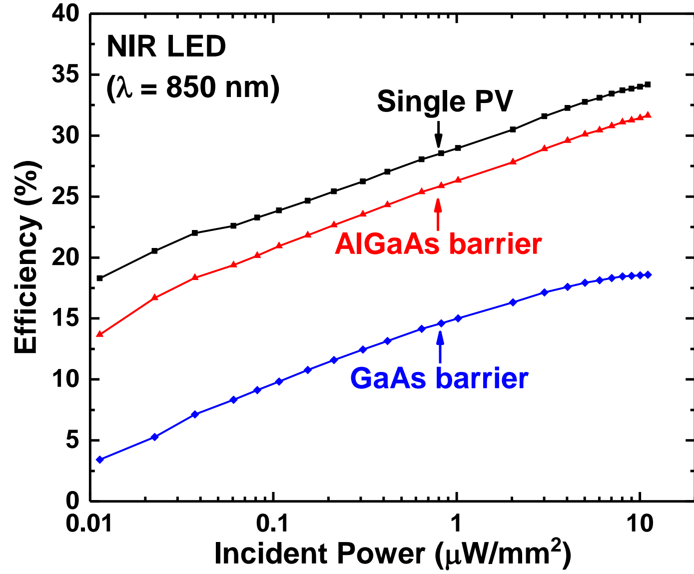


(a)

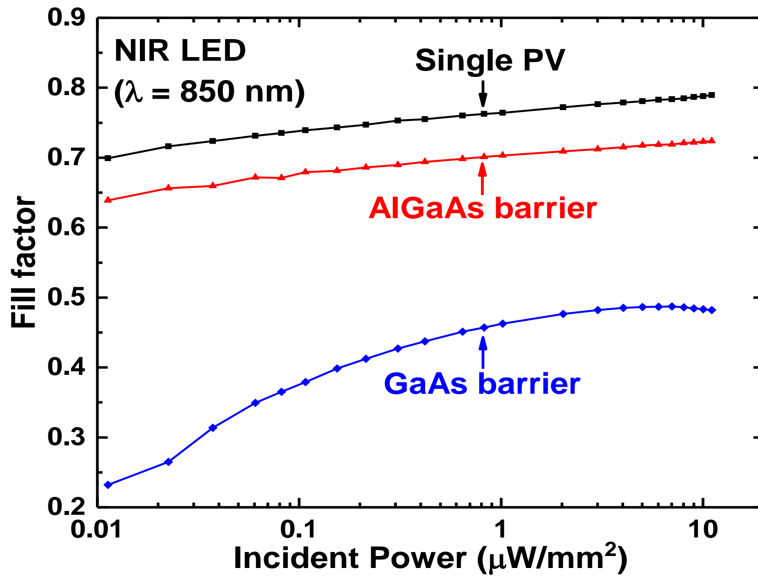


(b)

Figure 5.9. Comparison of measured *P-V* characteristics between PV arrays and single PV cell (a) under 850 nm NIR illumination at 1.02 μW/mm^2 and (b) under white LED illumination at 586 lux.



(a)

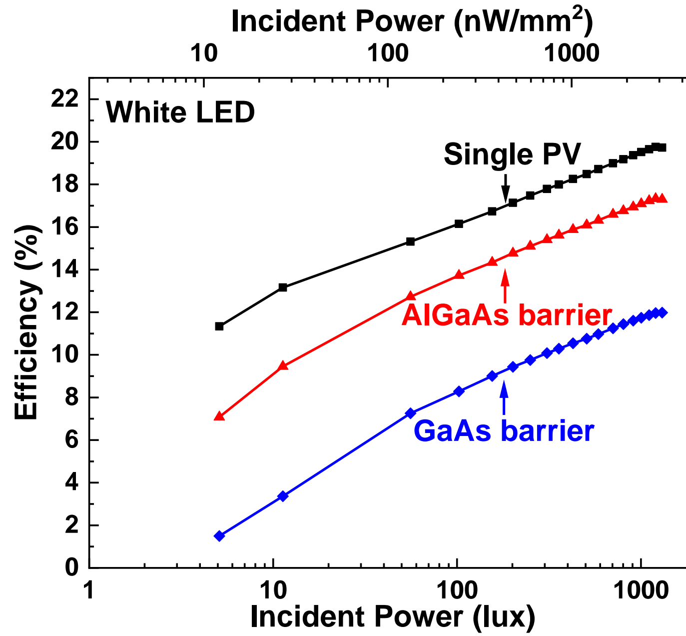


(b)

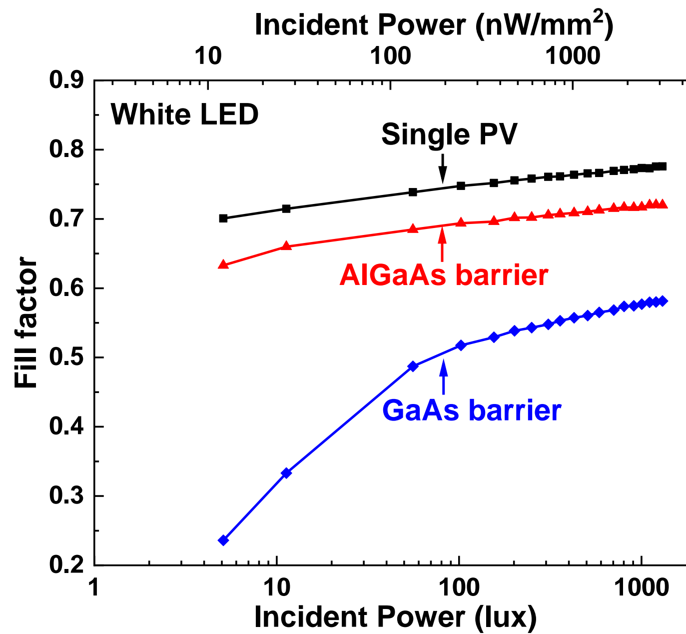
Figure 5.10. Light intensity dependence of (a) power conversion efficiency and (b) fill factor for single PV and PV modules with p-GaAs and p-AlGaAs barrier junction isolation under NIR illumination.

The voltage generated by the PV module is sufficient for direct battery charging, and provides an effective voltage up-conversion efficiency of approximately 90 % for both NIR and white LED illumination. We observe a strong dependence of power conversion efficiency on

incident light intensity, as shown in Fig. 5.10 for NIR illumination and Fig. 5.11 for White LED illumination.



(a)



(b)

Figure 5.11. Light intensity dependence of (a) power conversion efficiency and (b) fill factor for single PV and PV modules with p-GaAs and p-AlGaAs barrier junction isolation under white LED illumination.

This dependence has been previously studied for small-area GaAs cells, and attributed to perimeter sidewall recombination. Consistent with our *J-V* and *P-V* curves, the shunt leakage current for PV modules with p-GaAs barrier junction isolation results in power conversion efficiency degradation over the full range of light intensity studied. The p-AlGaAs barrier junction isolation module demonstrates power conversion efficiency that approaches the performance of the single PV cell for the full range of illumination intensity. These results confirm that the PV module with p-AlGaAs junction barrier isolation can maintain efficiency comparable to a single PV cell under extremely dim light conditions below 100 nW/mm^2.

5.3.4. Practical application of mm-scale PV energy harvesting

To illustrate the utility of mm-scale PV modules, we constructed a fully-encapsulated 17 mm^3 wireless sensor system incorporating a GaAs PV module (Fig. 5.12) [98]. The system includes a 16 µAh thin-film lithium-ion battery pair that is directly charged by the PV module through a reverse-current blocking diode.

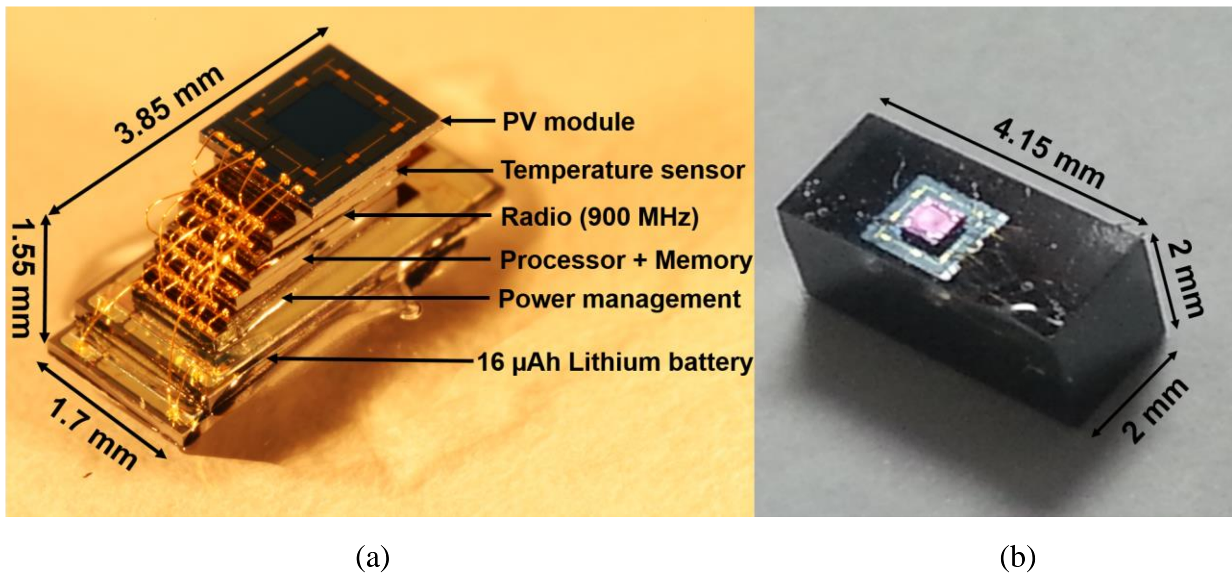


Figure 5.12. Optical microscope images of a wireless mm-scale sensor system with integrated PV module (a) before and (b) after encapsulation.

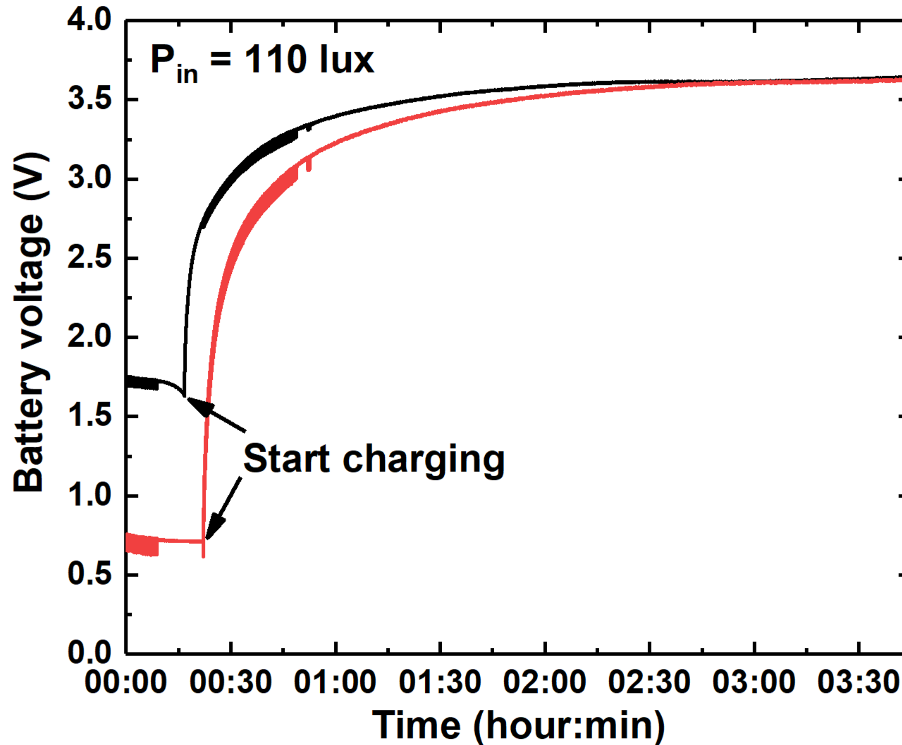


Figure 5.13. Monitored battery voltage output of this mm-scale system during the charging process under 110 lux indoor illumination.

Battery charging characteristics under dim indoor illumination at 110 lux are shown in Fig. 5.13. The PV module demonstrates a clear recovery of battery voltage within 2 hours, providing adequate energy storage to operate the system. illumination at 110 lux are shown in Fig. 5.12. The PV module demonstrates a clear recovery of battery voltage within 2 hours, providing adequate energy storage to operate the system. The average power requirement to report temperature every 30 minutes is 28.4 nW, comparing favorably to the average power generation of the PV module of 70.8 nW under 200 lux. While the PV system demonstrates the ability to power a mm-scale wireless sensor nodes, there are still opportunities to further improve conversion efficiency through reducing losses that appear at low light intensity (e.g., perimeter recombination) and losses associated with shunt leakage current for modules [18] providing voltage up-conversion.

5.4. Conclusion

Photovoltaic modules offer an efficient means for energy harvesting and direct battery charging in mm-scale systems. This application places unique demands on both PV cells and the module, where PV cells require high performance under much dimmer conditions than conventional solar cells and PV modules have a critical emphasis on maximizing area and electrical isolation of adjacent cells. We demonstrated GaAs PV modules at the mm-scale with high efficiency under low-flux conditions, where AlGaAs junction barrier isolation provided a critical step in limiting shunt leakage current between series connected cells. We observed power conversion efficiency of 26.3 % under 850 nm infrared LED illumination at 1.02 $\mu W/mm^2$ and 16.3 % under white LED illumination at 586 lux (1.4 $\mu W/mm^2$), with a 90 % voltage up-conversion efficiency to reach an operating voltage of 5 V for direct battery charging. We applied a monolithic PV module to demonstrate the perpetual operation of a mm-scale wirelessly interconnected temperature logger system. Further improvements in mm-scale PV module efficiency may be gained by continued improvement in reducing perimeter leakage current in small-area cells and reduction in shunt leakage through techniques such as epitaxial layer transfer to fully insulating substrates [99] or vertical multi-junction designs [100].

CHAPTER 6

Vertical dual junction GaAs Photovoltaics

6.1. Introduction

In previous chapters, we demonstrated single PV cells and monolithic PV modules to directly power fully wireless mm-scale or sub mm-scale systems for IoT and bio-implantable applications or to charge batteries of those systems without DC-DC voltage up-conversion [98]. Series connected single junction (SJ) PV modules at the mm-scale have been demonstrated, providing output voltage of greater than 5 V and voltage up-conversion efficiency of more than 90 %. However, there are fill factor losses associated with shunt leakage paths through the shared substrate [18] and efficiency losses when scaling to small systems due to perimeter losses [13,21]. There is a continuing challenge to miniaturize such PV systems down to the sub mm-scale with minimal optical losses from device isolation and metal interconnects and efficient voltage up-conversion. Vertically series connected junctions offer an alternative option for efficient voltage up-conversion, which is commonly used for broadband solar illumination and devices with multiple junctions for differing bandgap energies [101-104]. In this work, we demonstrate dual-junction (DJ) photovoltaic cells at sub mm-scale under low-flux monochromatic illumination (which can also be applied to narrowband visible indoor lighting). The devices use junctions with the same GaAs-based materials and bandgap energies, where cells are designed to evenly divide optical absorption in each junction, while doubling the voltage output for the DJ series connection and considering demanding requirements for miniaturized devices under low-flux operating

conditions. The DJ approach provides a means of voltage up-conversion while reducing the number of lateral series connections and corresponding shunt leakage paths for monolithic PV modules.

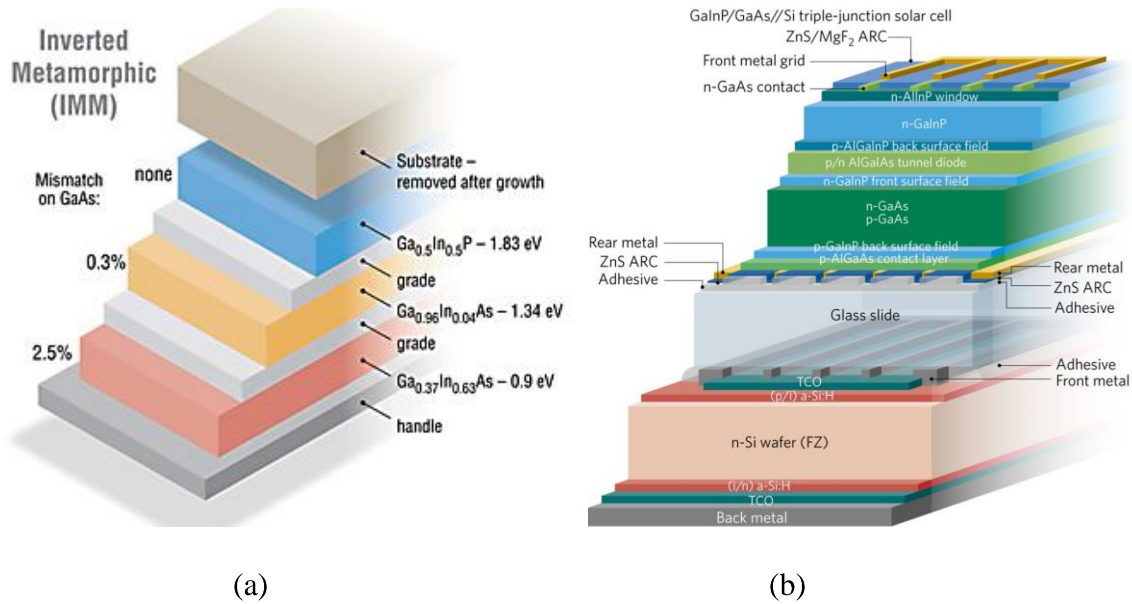
6.2. Dual-junction device design

6.2.1. Device structure

The conventional multi-junction (MJ) solar cells to boost the power conversion efficiency above 40 % as shown in Fig. 6.1 are utilizing monolithically grown [101-103] or mechanically stacked / bonded [104] materials with optimized band gaps for different spectral contents, where the wider band gap material is placed at the top for the absorption of shorter visible and UV wavelengths and longer wavelength light at the NIR region is absorbed by the lower band gap material below. Monolithic tandem cells based on III-V materials (InGaP/GaAs/InGaAs) [101-103] are preferred due to a higher absorption coefficient and tunability of band gaps using almost lattice matched alloys, where individual cells are connected by heavily doped p-n junctions called tunnel junctions for the series connection of individual cells. Flowing currents of each cell need to be matched through the optimization of device structures due to the series connected device configuration. Advantages of MJ design are to harness more portion of the incident solar spectrum and extract photogenerated electrons with a chemical potential close to incident photons and almost no kinetic / thermalization energy losses, which generates higher power output under the same solar irradiation. The previous laser power converters [105] using vertically-stacked multiple p-n GaAs junctions were designed for the NIR wavelength range between 800 nm and 850 nm.

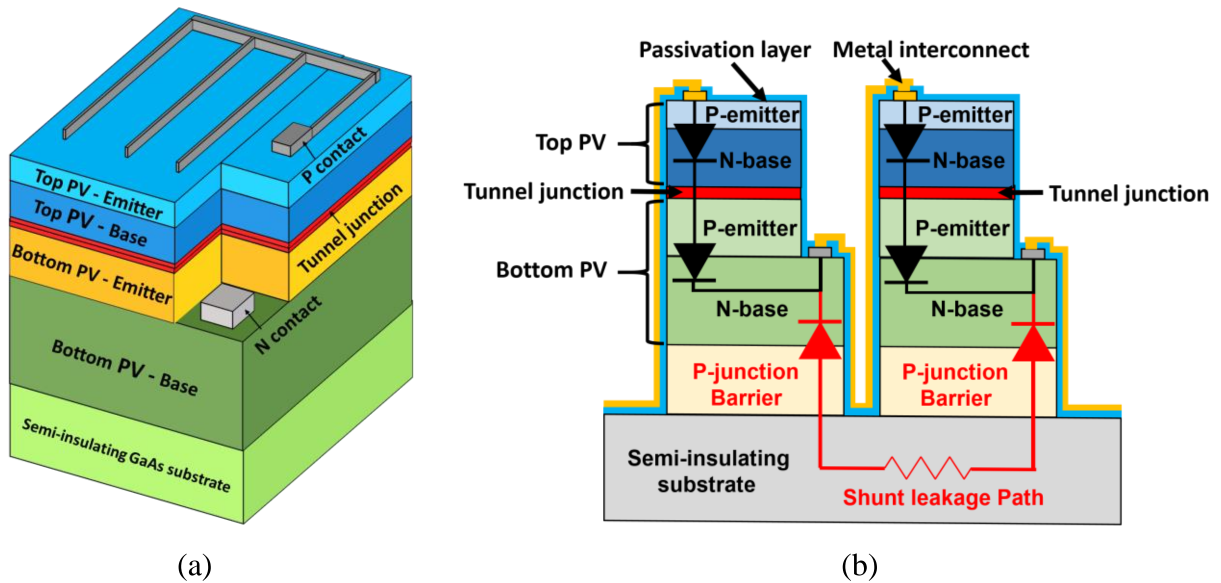
In this work, we designed two monolithic dual-junction (DJ) PV cells in the same GaAs with optimized thicknesses of each cell based on the structure of conventional III-V tandem cells,

connected by tunnel junction and designed for a 50 % current match for narrow spectral ranges from visible and NIR wavelengths. The AlGaAs window and back surface layers were incorporated to both top and bottom cells as shown in Fig. 6.2.



(a) (b)

Figure 6.1. Schematic illustration of (a) monolithically grown and (b) mechanically stacked multi-junction device structures (adopted from [104,106])



(a) (b)

Figure 6.2. Schematic diagrams of (a) single dual-junction PV cell and (b) dual-junction PV module illustrating PV cell junction, junction barrier isolation, and shunt leakage path.

6.2.2. Device simulation

Detailed device parameters were optimized utilizing a Sentaurus device simulation tool [30] using well-established physical models for band-to-band tunneling, drift-diffusion currents and photocurrent generation from a transfer-matrix method (TMM). As shown in Fig. 6.3 and Fig 6.4, we initially simulated variable thickness of a top PV cell with the fixed thickness of bottom PV cell at 3.5 μm under low-flux 1 μW/mm^2 NIR illumination at a wavelength of 850 nm, where one-sun solar irradiation is around at 1 mW/mm^2 [12] and typical indoor lighting is around 400 lux (~ 1 μW/mm^2) [13,21].

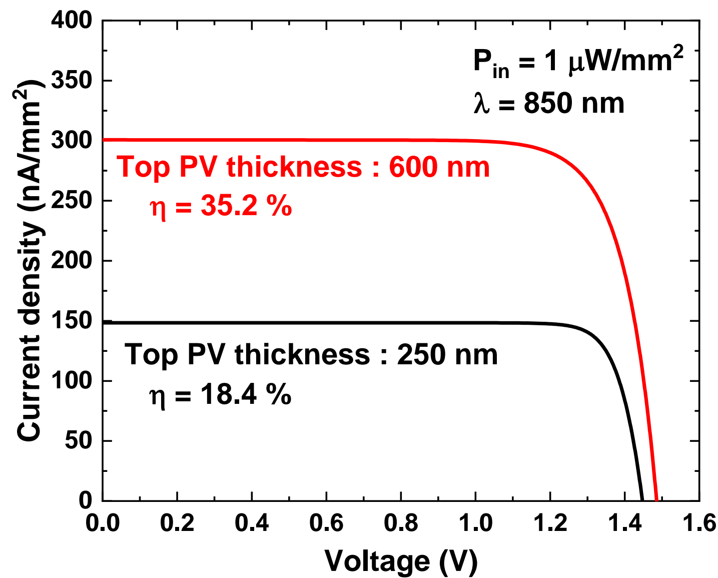


Figure 6.3. Simulated current voltage characteristics of dual junction cells with variable thickness of a top cell under 850 nm NIR illumination at 1 μW/mm^2.

According to current-voltage (*J-V*) simulation results in Fig. 6.3, there is an evident drop in short circuit current (J_{SC}) of the thinner top cell (100 nm p-type emitter and 150 nm n-type) compared to J_{SC} of the thicker top cell (100 nm p-type emitter and 500 nm n-type base) due to the mismatched current between top and bottom PV cells, degrading the power conversion efficiency from 35.2 % to 18.4 %. Furthermore, we can control the peak wavelength of external quantum

efficiency (EQE) above 40 % by controlling thickness of the top cell from orange wavelength at 600 nm targeted for indoor lighting conditions (50 nm p-type emitter and 50 nm n-type base) to NIR wavelength at 850 nm targeted for bio-implantable devices (100 nm p-type emitter and 500 nm n-type base), while having low efficiency off the peak response (short wavelength) due to mismatched absorption between top and bottom junctions.

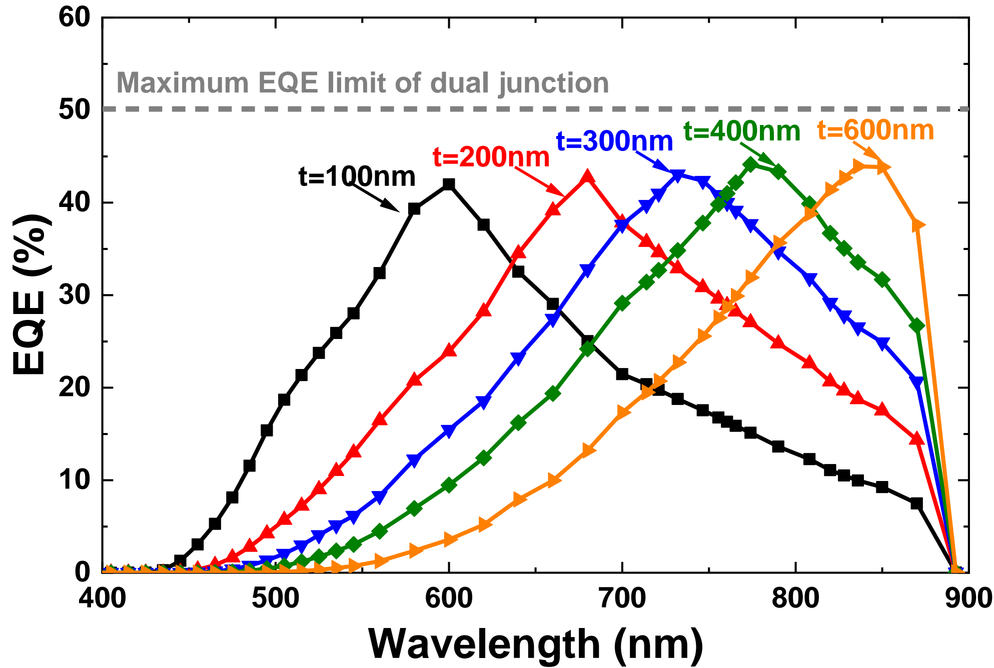


Figure 6.4. Simulated external quantum efficiency (EQE) spectra for different thickness of top PV cells in the dual-junction structure with the fixed thickness of bottom PV cell at 3.5 μm.

Simulated *J*-*V* comparison results between dual-junction (DJ) and single-junction (SJ) PV cells under NIR illumination as shown in Fig. 6.5 show that the DJ PV cell has comparable power conversion efficiency (> 30 %) to SJ PV cell with double output voltage (> 1.4 V), which is promising to guarantee the batteryless operation of CMOS chips. Monolithic PV modules utilizing the optimized individual single DJ PV design for higher voltage generation between 5 – 10 V were also considered by incorporating the additional $Al_{0.3}Ga_{0.7}As$ junction barrier (400 nm thick and p-

type doping at 5 x 10^{16} cm^{-3}) on the semi-insulating substrate. Optimized device parameters especially for NIR 850 nm wavelength as an example are summarized in Table 6.1.

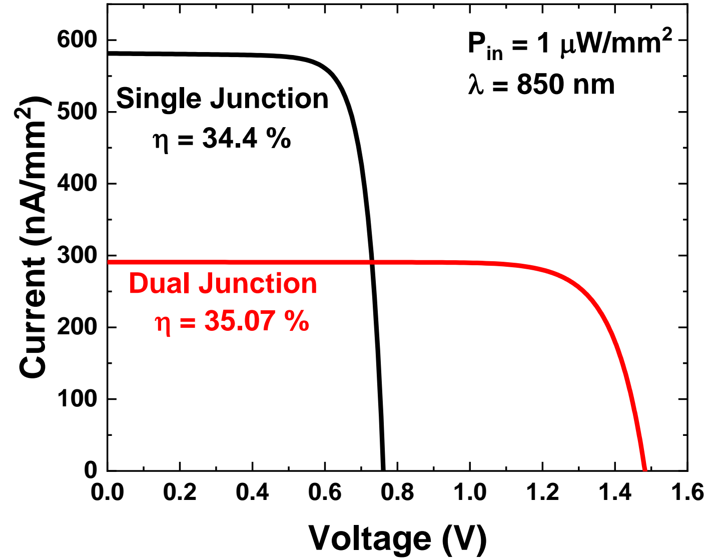


Figure 6.5. Comparison of simulated *J-V* characteristics between single-junction and dual-junction PV cells under 850 nm NIR illumination at 1 μW/mm².

Type	Material	Thickness (nm)	Doping (cm^{-3})	Layer information
P++	GaAs	200 nm	$2x10^{19}$	Top PV - anode contact
P+	$Al_{0.8}Ga_{0.2}As$	30 nm	$2x10^{18}$	Top PV - window layer
P+	GaAs	100 nm	$4x10^{18}$	Top PV - emitter
N	GaAs	500 nm	$1x10^{17}$	Top PV – base
N+	$Al_{0.3}Ga_{0.7}As$	30 nm	$1x10^{18}$	Top PV - back surface field
N++	GaAs	15 nm	$1x10^{19}$	Tunnel junction
P++	GaAs	15 nm	$4x10^{19}$	Tunnel junction
P+	$Al_{0.8}Ga_{0.2}As$	30 nm	$2x10^{18}$	Bottom PV - window layer
P+	GaAs	500 nm	$4x10^{18}$	Bottom PV – emitter
N	GaAs	3000 nm	$1x10^{17}$	Bottom PV – base
N+	$Al_{0.3}Ga_{0.7}As$	150 nm	$1x10^{18}$	Bottom PV - back surface field
N++	GaAs	1000 nm	$2x10^{18}$	Bottom PV – cathode contact
P-	$Al_{0.3}Ga_{0.7}As$	400 nm	$5x10^{16}$	Barrier layer
--	GaAs	625 μm	Semi-insulating	Substrate

Table 6.1. Optimized device parameters of dual junction PV cell and module**,** designed for NIR wavelength at 850 nm.

6.2.3. Device fabrication and testing methods

Wafers based on optimized layer structures (Table 6.1) from the simulation were grown by molecular beam epitaxy on semi-insulating GaAs substates. We fabricated square DJ PV cells ranging from 100 μm to 2.5 mm on a side. Devices were fabricated using conventional photolithography, etching, contact metallization, and liftoff processes, as shown in Fig 6.6. Special attention was devoted to surface/perimeter passivation [13,21] due to their importance for miniaturized PV cell performance, where we used a diluted ammonium sulfide solution treatment [49-51] and a subsequent plasma-enhanced chemical vapor deposition (PECVD) silicon nitride layer [53] that also serves as a top surface anti-reflection coating. Monolithic PV cell modules were fabricated with four and eight connected cells in series using lithographically defined metal interconnects, as shown in Fig. 6.9. These monolithic DJ modules provide voltage up-conversion that combines both vertical and lateral series connections. The detailed device fabrication recipe is included in Appendix.

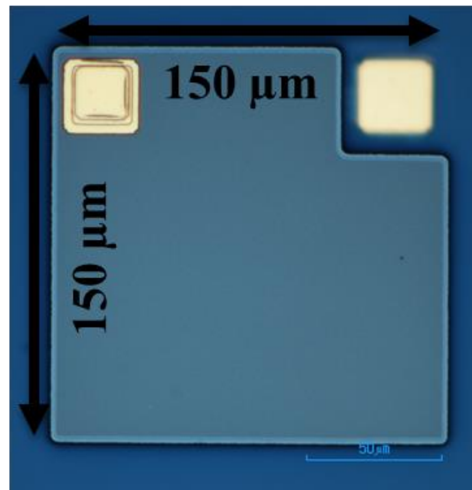


Figure 6.6. Optical microscope image of fabricated dual junction PV cell at µm-scale.

Electrical characteristics (J-V and P-V) under NIR illumination conditions were measured using a Keithley 4200/2400 parameter analyzer. NIR illumination up to 10 μW/mm^2 used a

commercial 850 nm NIR light emitting diode and calibrated power meter. The EQE spectrum was measured using a grating monochromator, xenon white light source, lock-in amplifier, and calibrated photodetector. The measured *J-V* and power density versus voltage (*P-V*) characteristics were used to extract JSC, open circuit voltage (V_{OC}), maximum power density (P_{max}), and fill factor $FF = P_{max} / (V_{OC}*J_{SC})$.

6.3. Results

6.3.1. Single dual-junction PV cells

Fabricated single DJ PV cells at mm-scale and sub mm-scale were measured under low-flux NIR illumination below 10 μW/mm^2 and their device performance parameters especially for fill factor (FF) were extracted Measured single DJ PV cell with 6.4 mm^2 size achieved power conversion efficiency above 26 % with more than 1.4 V output voltage under 850 nm NIR LED illumination at 2.02 μW/mm^2 as shown in Fig. 6.7 while maintaining the extracted fill factor around 0.806 under the dim lighting condition without the degradation from shunt resistance of each junction.

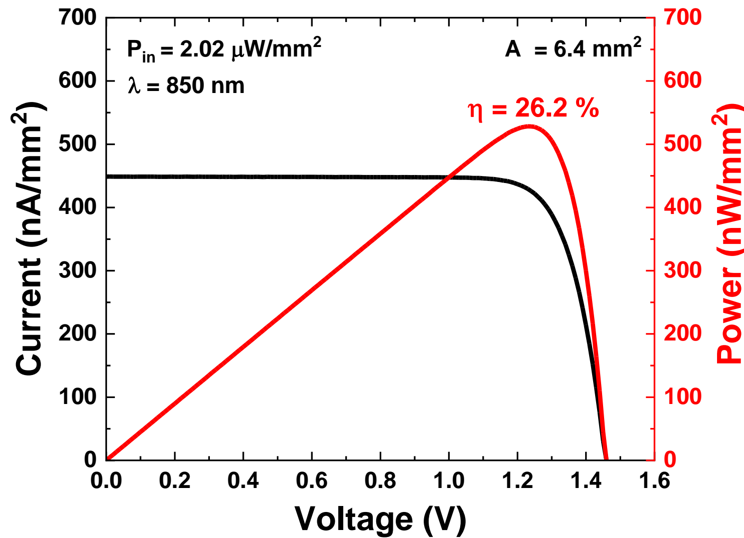


Figure 6.7. Measured *J-V* and *P-V* characteristics of fabricated dual junction PV cells with 6.4 mm^2 size under 2.02 μW/mm^2 NIR illumination at wavelength of 850 nm.

Furthermore, the extremely small size PV cell at µm-scale (150 µm x 150 µm) demonstrated power conversion efficiency greater than 22 % with more than 1.2 V output voltage under higher NIR LED illumination at 6.62 µW/mm^2 and produced the output power around 33 nW (1.49 µW/mm^2) as shown in Fig. 6.8, which is sufficient to directly power miniaturized CMOS IC chips [2,8,68] and enables fully remote sensor nodes at µm-scale [98].

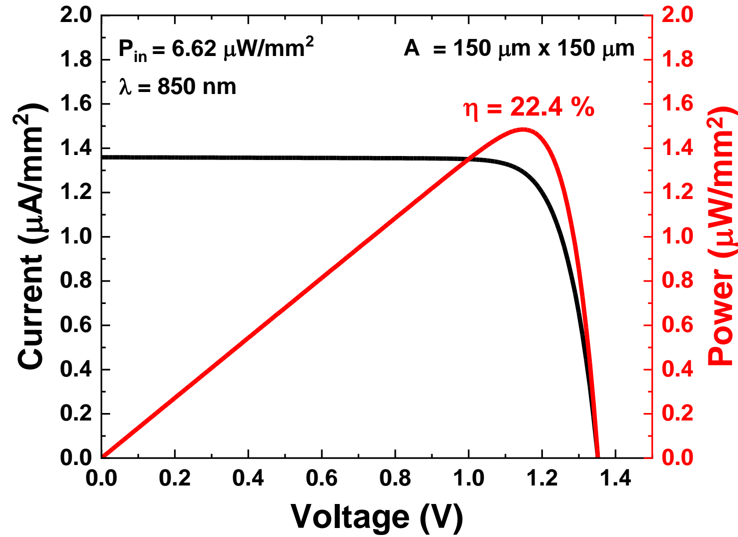


Figure 6.8. Measured *J-V* and *P-V* characteristics of fabricated dual junction PV cells with 150 µm x 150 µm size under 2.02 µW/mm^2 NIR illumination at wavelength of 850 nm.

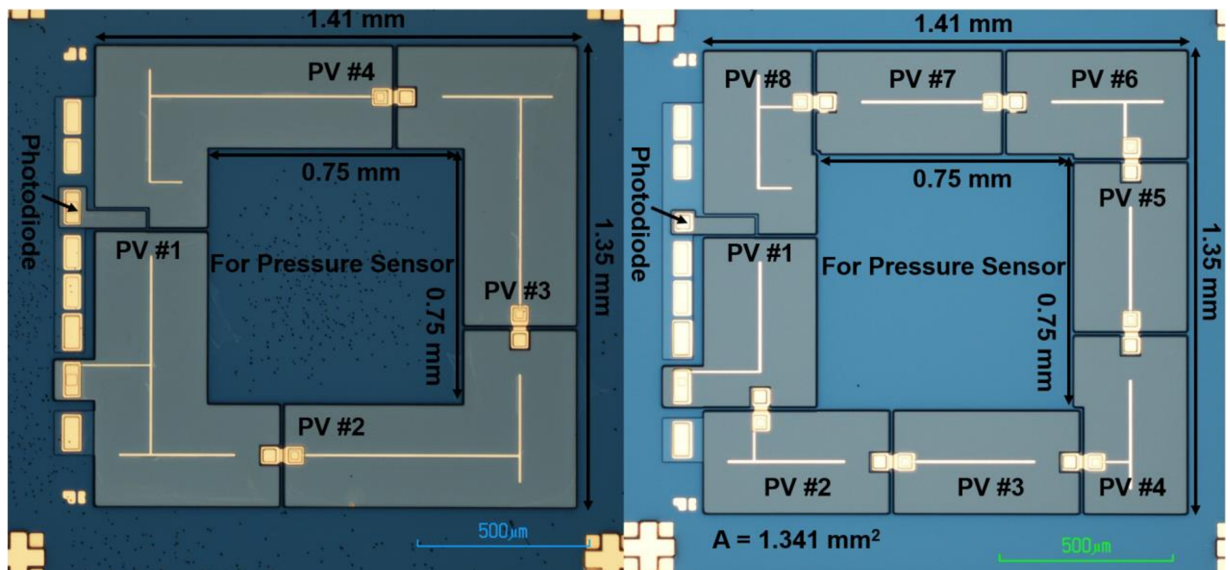


Figure 6.9. Optical microscope images of two different fabricated DJ PV modules that have 4 and 8 cells connected in series.

6.3.2. Dual-junction PV modules

Power conversion in monolithic PV modules with four and eight series connected DJ cells are shown in Fig. 6.9, demonstrating higher output voltage that is suitable for direct battery charging capabilities without an inevitable loss during DC-DC voltage up-conversion [92,98]. PV modules with four series connected DJ cells (total of eight diode junctions) in Fig. 6.10 produce an output voltage > 5 V, power conversion efficiency of 23.7 %, and overall voltage up-conversion efficiency of approximately 84 % compared to baseline single-junction PV cells with the output voltage below 1 V, originated from the incorporated AlGaAs junction barrier layer between series connected PV cells. The eight series-connected DJ cell module (total of 16 series connected diode junctions) produces an output voltage > 10 V with an efficiency of more than 18 %, where there is a clear drop in fill factor due to the shunt leakage degradation [98].

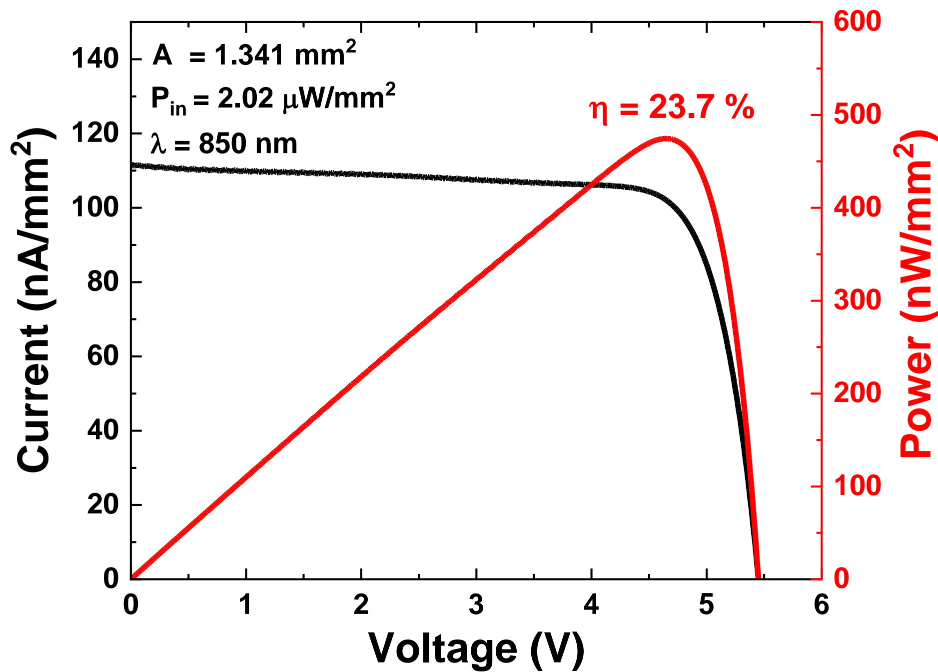


Figure 6.10. Measured *J-V* and *P-V* characteristics of PV modules with 4 cells in series.

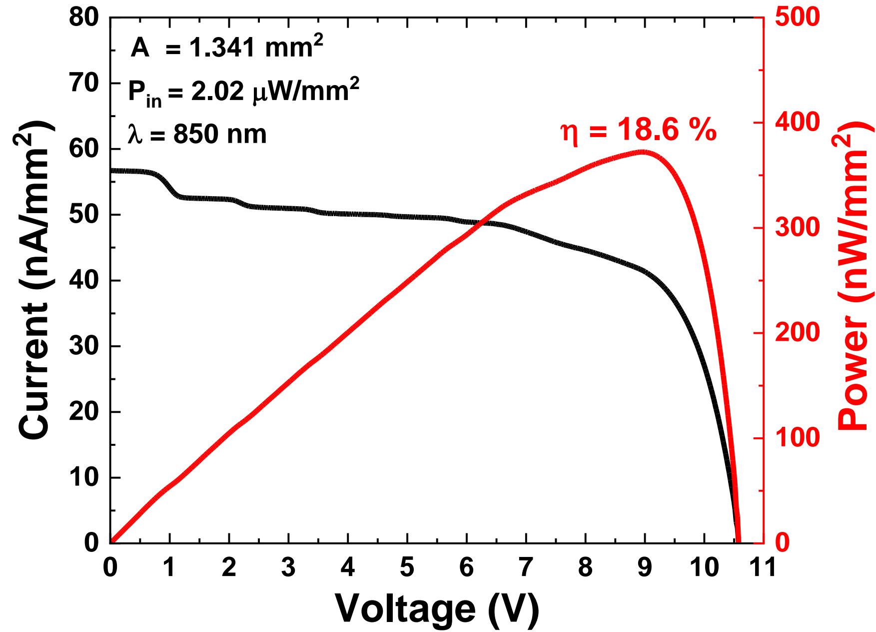


Figure 6.11. Measured *J-V* and *P-V* characteristics of PV modules with 8 cells in series.

6.4. Discussion

Device performances of single DJ and SJ PV cells under the same 850nm NIR illumination at 6.62 μW/mm^2 were compared as shown in Fig. 6.12 and summarized in Table 6.2. Though there were doubled output voltage (> 1.2 V) and improvement in fill factor above 0.8 as designed in the DJ structure, an undesirable loss of approximately 10 % was observed in photo-generated current (40 % of SJ design, ideally 50 %), results in 6 % efficiency loss. The additional EQE measurement was required to characterize the current loss in the DJ structure more. The EQE measurement of DJ PV cell in Fig. 6.13 indicated that DJ structure was well optimized for the peak wavelength at 850 nm. However, in comparison to measured EQE values of SJ and simulation results of DJ, EQE values at a wavelength of 850 nm were around 38 % for DJ, 85 % for SJ and 45 % for DJ simulation. There was an observed 5 - 7 % EQE loss at 850 nm wavelength, matched to measured lower short-circuit current level of DJ PV cells and requiring more optimization of tunnel junction and the structure of top PV cell.

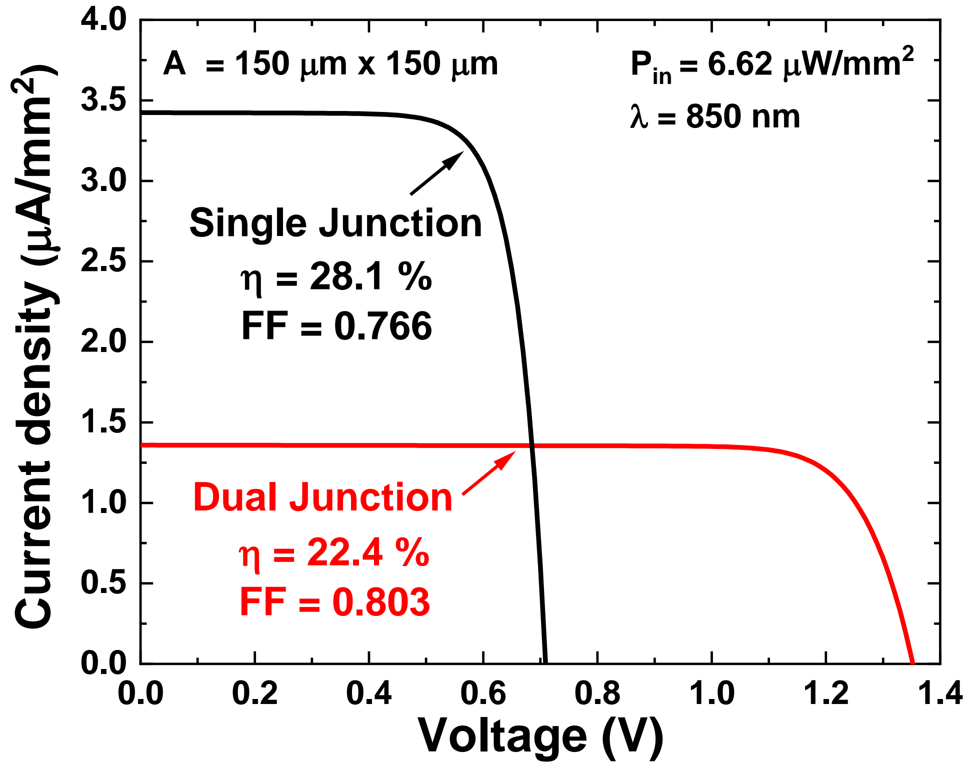


Figure 6.12. Comparison of measured J-V characteristics between DJ and SJ PV cells under 850 nm NIR illumination at 6.62 μW/mm^2.

Parameters	SJ	DJ
I_{SC} (μA/mm^2)	3.42	1.36
V_{OC} (V)	0.71	1.36
P_{MAX} (μW/mm^2)	1.86	1.49
P_{MAX} (nW)	41.9	33.5
Fill factor	0.766	0.803
η (%)	28.1	22.4

Table 6.2. Comparison of measured device performances between DJ and SJ PV cells under 850 nm NIR illumination at 6.62 μW/mm^2.

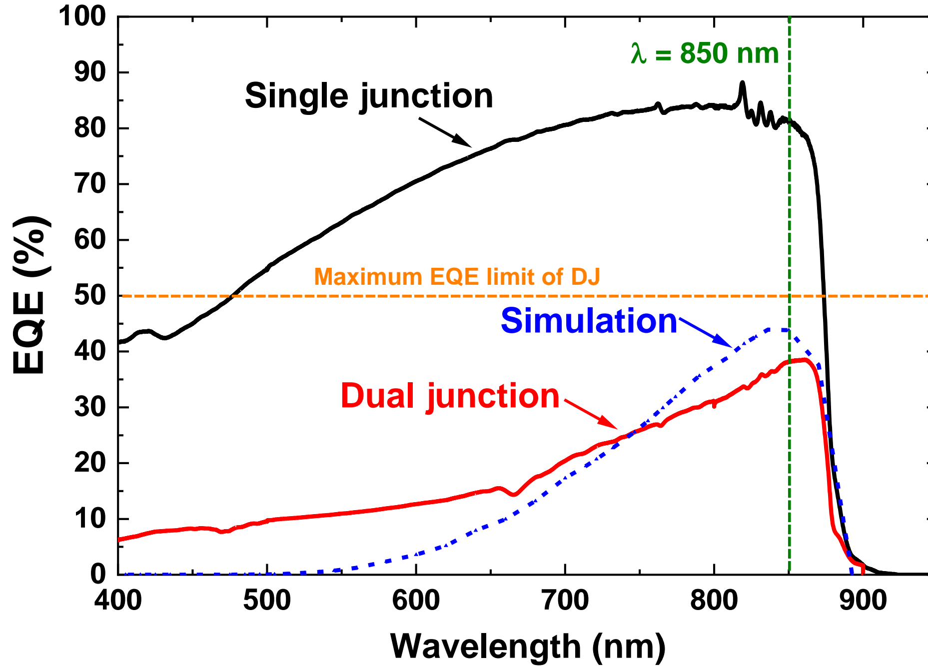


Figure 6.13. Measured EQE spectra of DJ and SJ PV cells and comparison with simulated EQE spectrum of DJ PV cell.

Furthermore, device performances of SJ and DJ PV modules were compared under 850 nm NIR illumination as shown in Fig. 6.14 and Fig. 6.15. PV modules targeted for above 5 V voltage generation in Fig. 6.14 used total 4 series-connected cells for DJ and 8 series-connected cells for SJ, where the DJ PV module had the improved fill factor around 0.775 than that of the SJ PV module around 0.712 by reducing the number of series connections. However, the power conversion efficiency of the DJ PV module was degraded from 26.8 % to 23.7 %, originated from the photogenerated current loss of individual single DJ PV cells in the module. When both SJ and DJ PV modules used the same 8 cells connected in series as shown in Fig. 6.15, the DJ PV module produced doubled output voltage above 10 V as designed. On the other hand, the measured fill factor of this module was degraded more from 0.712 to 0.618 and corresponding dropped efficiency from 26.8 % to 18.6 % due to higher applied voltage, where the current $Al_{0.3}Ga_{0.7}As$

barrier layer might be insufficient to block the shunt leakage current through the semi-insulating substrate properly.

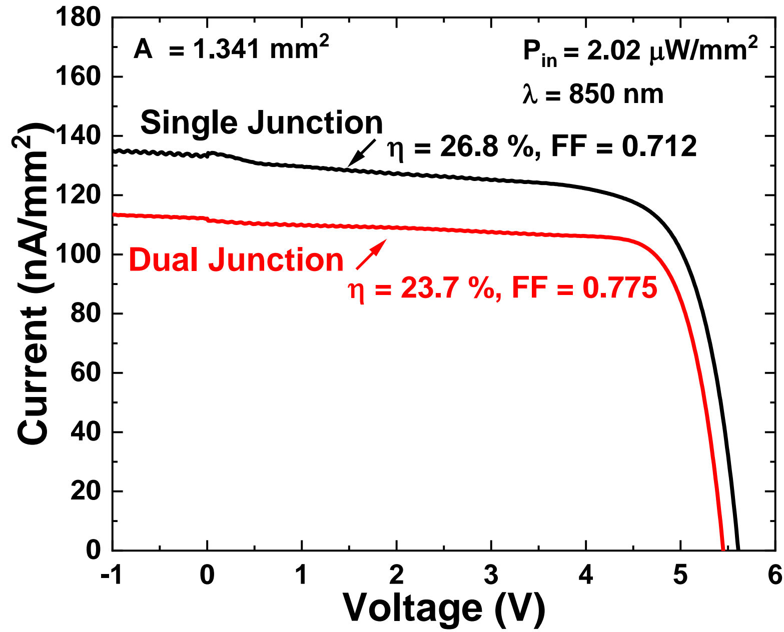


Figure 6.14. Comparison of measured *J-V* characteristics between SJ (8 cells in series) and DJ (4 cells in series) PV arrays under 850 nm NIR illumination at 2.02 μW/mm^2.

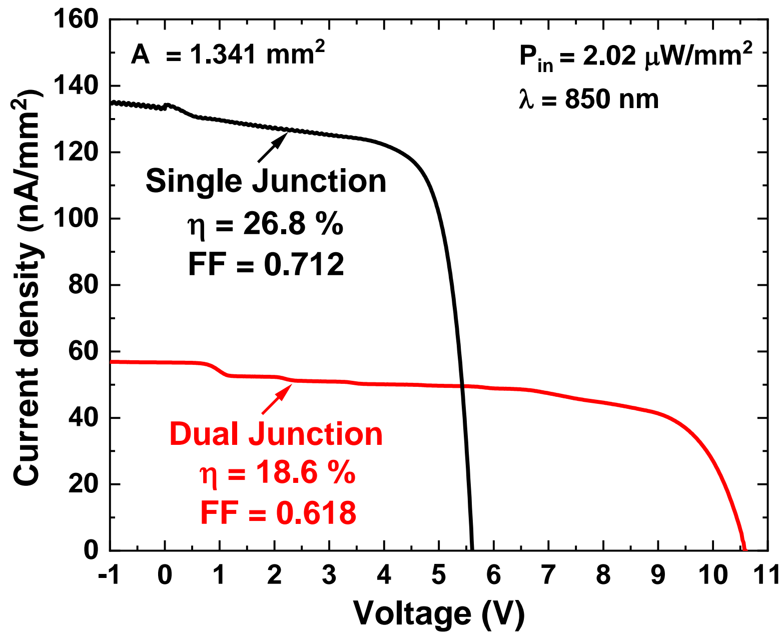


Figure 6.15. Comparison of measured *J-V* characteristics between SJ (8 cells in series) and DJ (8 cells in series) PV arrays under 850 nm NIR illumination at 2.02 μW/mm^2.

Parameters	SJ	DJ	
# of cells	8	4	8
I_{SC} (nA/mm^2)	133	112	56.68
V_{OC} (V)	5.61	5.46	10.62
P_{MAX} (nW/mm^2)	541	479	376
Fill factor	0.712	0.775	0.618
η (%)	26.8	23.7	18.6

Table 6.3. Comparison of measured device performances between SJ and DJ PV modules with 4 and 8 cells in series under 850 nm NIR illumination at 6.62 μW/mm^2.

Further improvements in the performance of DJ PV cells and modules are possible from further optimization of the tunnel junction and layer structure of the top junction to reduce photo-generated current losses. The shunt leakage current of PV modules through the substrate can be reduced using thicker junction barrier layers with wider bandgap AlGaAs (> 30 % aluminum) or techniques such as epitaxial lift-off (ELO) [103,107] to transfer the active layers to insulating substates or vertically-stacked multi-junction designs [105] rather than laterally interconnected cells.

6.4. Conclusion

Vertically stacked DJ PV cells and modules are demonstrated to increase operating voltage for direct powering of miniature devices for IoT and bio-implantable applications with low-irradiance narrowband spectral illumination. The DJ approach increases the output voltage per cell and minimizes area losses from device isolation and interconnects in comparison to SJ cells. DJ PV cells at small dimensions (150 μm x 150 μm) demonstrate power conversion efficiency greater than 22 % with more than 1.2 V output voltage under low-flux 850 nm NIR LED illumination at

6.62 μW/mm^2, which is sufficient for batteryless operation of miniaturized CMOS IC chips. The output voltage of DJ PV modules with four series-connected single cells was greater than 5 V while maintaining an efficiency of more than 23 %. Further power conversion efficiency improvements are expected by optimizing designs to minimize photocurrent collection losses and shunt resistance losses through the substrate in modules. In addition to monochromatic NIR illumination, the GaAs DJ approach also shows promise for efficient energy harvesting under narrowband artificial indoor lighting conditions.

CHAPTER 7

Monolithically Integrated Microscale LED and Photovoltaic Module

7.1. Introduction

Neural recording, and ultimately the achievement of brain machine interfaces [84,108-112], ultimately relies on truly floating, wireless neural recording implants that do minimal damage and enable high channel count (> 1,000). Wireless power delivery and data communications are critical, though the small dimensions required (10's to low 100's of micrometers) and constraints placed by surrounding biological tissue make conventional wireless approaches highly inefficient. Radio-frequency (RF) links suffer from dramatic antenna efficiency loss when scaled to sub-mm size [74,75] due to lateral and angular misalignments [76] and weak coupling [75] with mm-scale antenna receivers or require high frequency (> 50 GHz), which results in tissue absorption and high power consumption [113-115]. Ultra-sound offers a path to high efficiency wireless power transfer comparable to RF but faces difficulty scaling to sub-mm size due to bulky transducers [116]. Near-Infrared light (NIR, 650 – 1350 nm) offers a transparency window for biological tissue [80,117] and device technologies with high efficiency at the micrometer scale. A system on a chip based for recording neural activities has been demonstrated using NIR for wireless power and data communications [118,119]. This device used an AlGaAs diode that operated simultaneously as a photovoltaic (PV) cell for power generation and light emitting diode (LED) for data communications. However, the input irradiance around 100 mW/mm^2 to operate the chips was far

much higher than the maximum exposure limit at 1.36 mW/mm^2 from ANSI [82], which might cause the damage to the brain due to the temperature increase under the intensive illumination at visible wavelength region. Also, the energy harvesting of PV cell was interrupted during the light pulse generation for the communication. Scaled microscale LEDs (μ-LEDs) on the order of 50 μm square have demonstrated the ability for scaled implantable devices for optogenetics [120], though operating at visible wavelengths and at lower power density that would not meet demands for neural dust.

We propose an approach for wireless neural recording based on arrays of implanted microscale probes (motes) with a NIR link to a repeater unit that would be inductively linked to an external device as shown in Fig. 7.1. Each mote would consist of a non-invasive cerebral implant and an integrated and packaged CMOS / optoelectronic device floating on the pia. Each mote would communicate through the arachnoid and dura mater to a cranial implant repeater unit that would be inductively coupled to an external device.

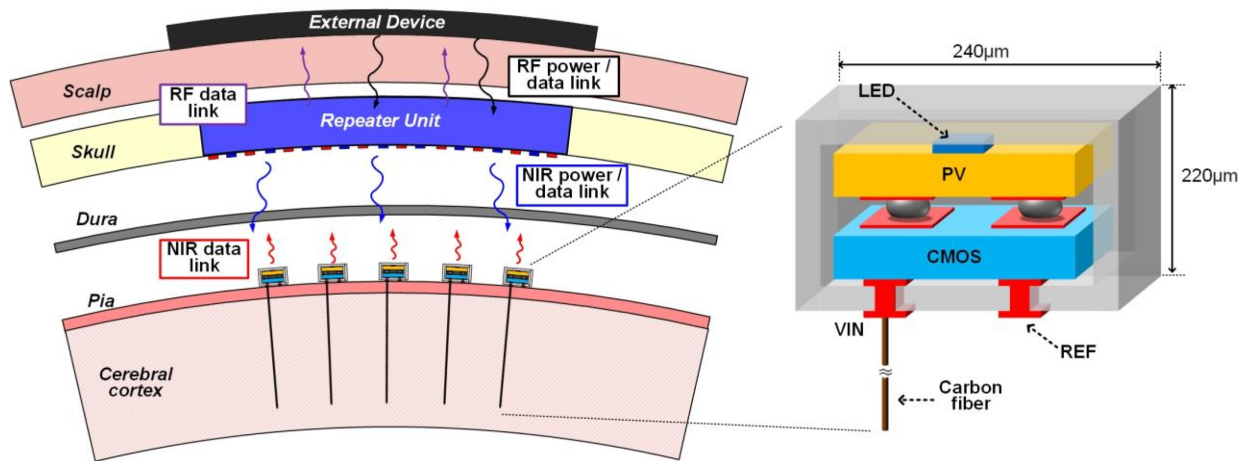


Figure 7.1. Conceptual illustration of a full system for recording and transmitting the neural signals and a PV / LED module in the system for NIR wireless power transfer and data communications (Drawn by Jongyup Lim).

In this work, we specifically focus on the "last millimeter" problem for meeting the wireless power and data communications requirements between the motes and the repeater unit, utilizing monolithically integrated GaAs / InGaAs based PV and μ-LED module at μm-scale. We used 850 nm NIR light for wireless power transfer and downlink data communication to the motes, and 1000 nm NIR light for uplink communication from the motes to the repeater. We selected the shorter wavelength (λ = 850 nm) for power generation to maximize PV power and voltage generation to the CMOS circuitry. In turn, the longer wavelength for the data communication uplink (λ = 1000 nm) reduces the minimum required voltage to drive the μ-LEDs. As a result, the μ-LED driver circuits can operate directly on the PV cell voltage without the need for voltage up conversion, thereby reducing the circuit complexity, power loss and CMOS layer size. Separate wavelengths also provide a means to distinguish the two optical signals.

7.2. Optical transmittance of dura maters

The optical transmittance of NIR light through the dura mater [80,117] is a key point for the feasibility of the proposed device concept for the NIR optical link, determined by optical absorption and scattering in the tissue due to the structural elements (collagen fibrils) and base substance (interstitial fluid). We measured NIR transmission through the dura of the post-craniotomy feline and a non-human primate (NHP) using the NIR LED and laser sources aligned to a calibrated photodetector as shown in Fig. 7.2. The dura showed high optical transmittance of > 85 % for the thinner feline dura under 850 nm NIR laser illumination and > 35 % for the thicker NHP dura under 850 nm, 970 nm and 1050 nm NIR LED illumination as show in Fig. 7.3 and Fig. 7.4, which is well matched to previously reported results [80,117]. As a result, we estimated the transmittance for humans slightly more conservative at 30 %, which is sufficient to guarantee

the operation of NIR based PV and LED modules.

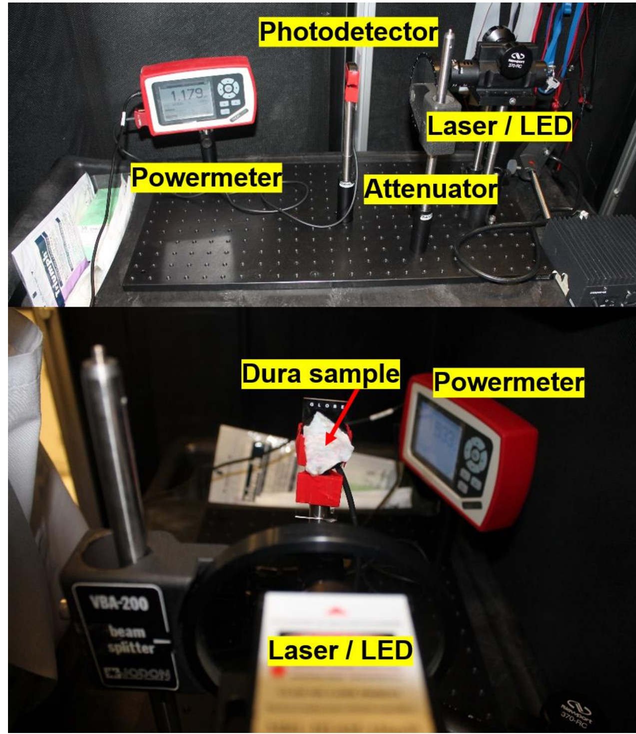


Figure 7.2. Experiment set up for measuring the NIR optical transmittance through the dura samples using laser and LED illumination sources.

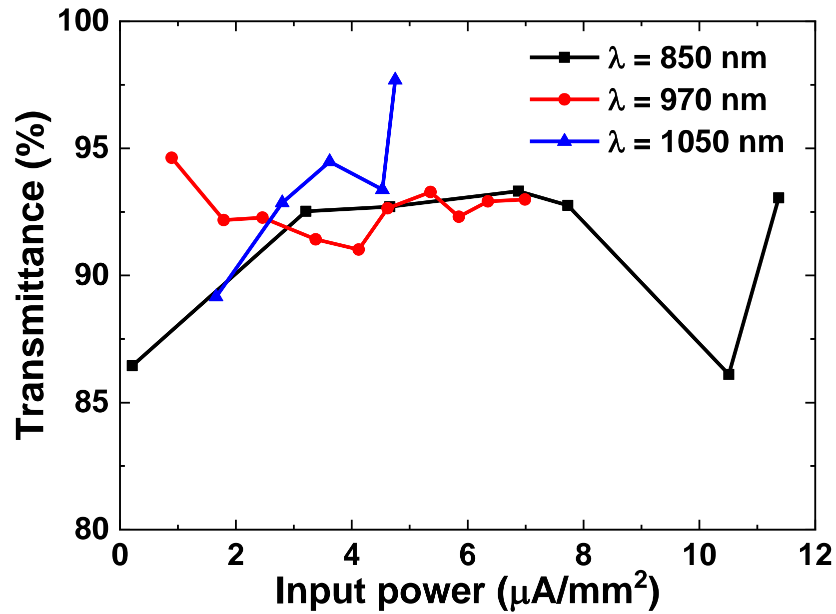


Figure 7.3. Measured NIR transmittance through post-craniotomy feline dura samples under 850 nm laser illumination.

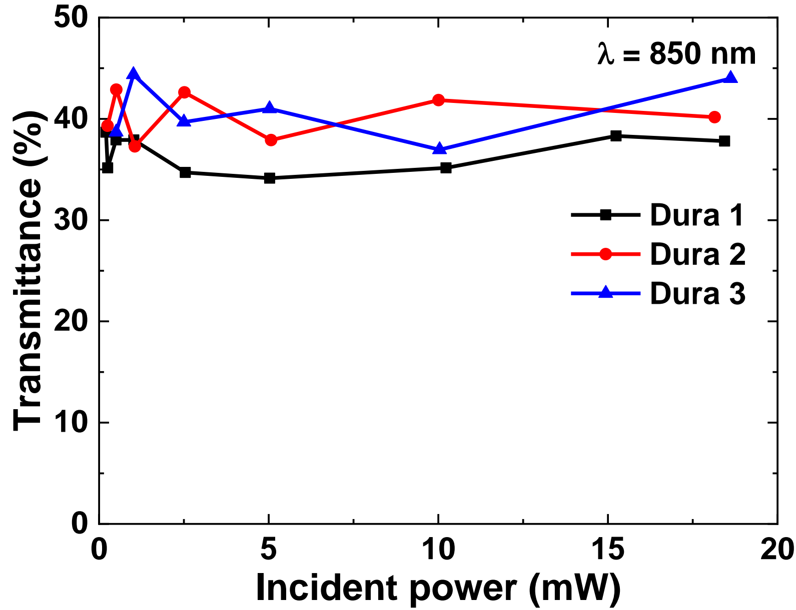


Figure 7.4. Measured NIR transmittance through post-craniotomy NHP dura samples under 850 nm, 970 nm and 1050 nm NIR LED illumination.

7.4. PV / LED module structure and fabrication

We designed monolithically integrated GaAs / InGaAs based on PV and LED nodule at µm-scale as shown in Fig. 7.5, utilizing 850 nm NIR light for wireless power transfer to PV under low-flux condition and 1000 nm NIR light emission form µLED for uplink communication. We fabricated the module with µm-scale size (190 µm x 170 µm for PV and 50 µm x 50 µm for LED) as shown in Fig. 7.6 using the conventional fabrication processes, where the chlorine based reactive-ion etching (RIE) to etch the epitaxial AlGaAs / GaAs / InGaAs layers down to desired contact layers both for PV and LED by controlling the etch depth using the surface profiler, the conventional photolithography using photoresists, plasma enhanced chemical vapor deposition (PECVD) of insulating films for passivation of the exposed sidewall, and physical vapor deposition (PVD) of thin metal films were used. The PV cell incorporated a vertically-stacked, dual-junction configuration optimized for a wavelength of 850 nm (The detailed device structure

was discussed in Chapter 6). The series connection of the two junctions doubles the voltage output, which can achieve sufficient voltage for direct powering of a CMOS chip with the minimum voltage requirement near 1.4 V [115] while also avoiding critical area and power losses due to metal interconnects and DC-DC voltage up-conversion. Two monolithic PV cells connected by tunnel junction were designed for a 50 % current match at a NIR wavelength of 850 nm by controlling the thickness of each cell. The $In_{0.2}Ga_{0.8}As$ multi quantum-well (QW) μ-LED for NIR data links monolithically integrated with the PV cell, designed for emission at 1000 nm.

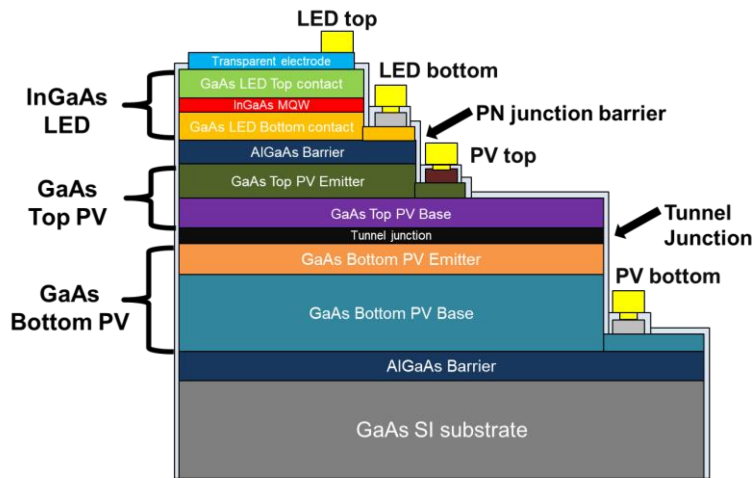


Figure 7.5. Schematic diagram of monolithically integrated μ-LED / PV module illustrating tandem junction of PVs and junction barrier isolation between LED and PV.

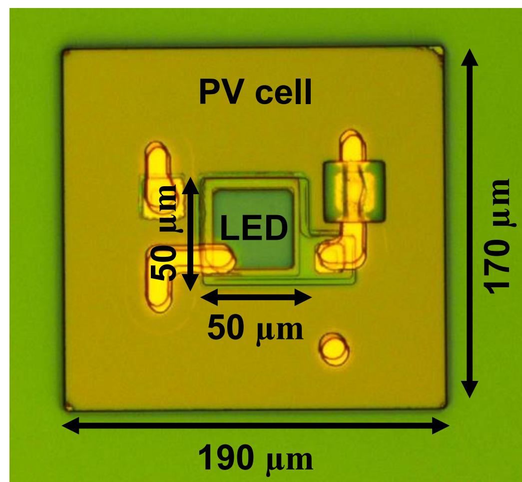


Figure 7.6. Optical microscope image of fabricated LED / PV module at μm-scale.

7.5. PV / LED module performance

7.5.1. Photovoltaic energy harvesting

A fabricated PV cell (190 μm x 170 μm) as shown in Fig. 7.7 demonstrated power conversion efficiency greater than 25 % and provides ~ 1 μW with more than 1.4 V output voltage under 850 nm NIR LED illumination at 100 μW/mm^2 (6 x lower than tissue exposure limit of 640 μW/mm^2), which is sufficient to directly power miniaturized CMOS IC chips subcutaneously without the concern of tissue heating above 2 ℃ [84].

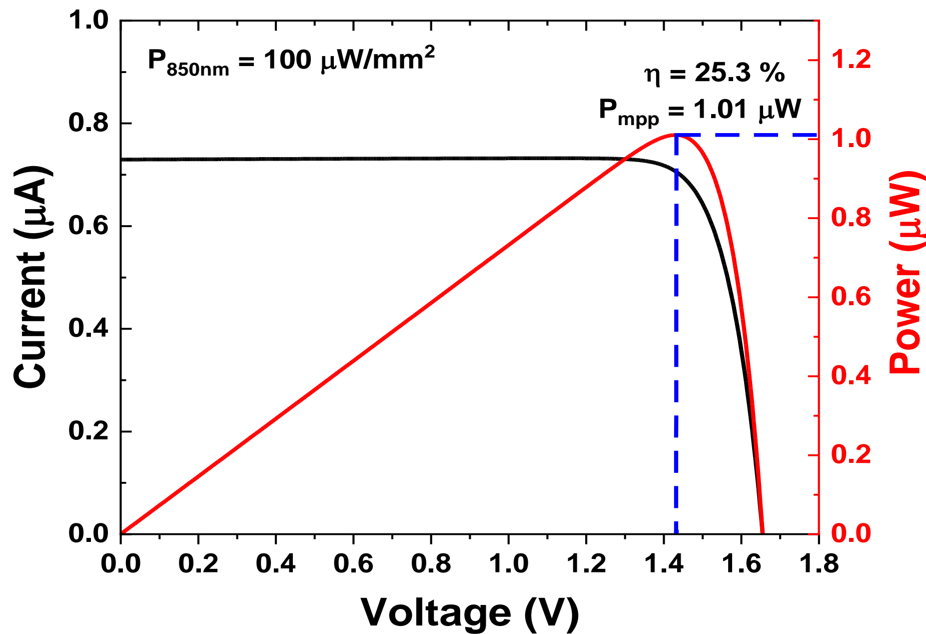


Figure 7.7. Measured *I-V* and *P-V* characteristics of dual junction PV cell under 850 nm NIR LED illumination at 100 μW/mm^2.

7.5.2. Micro-LED data-communications link

The NIR data link between the motes and the Repeater is designed to use a μ-LED on the motes and a single-photon avalanche detector (SPAD) array [121] at the Repeater, operating at a wavelength of 1000 nm. This wavelength provides high transmittance through the dura, high

quantum efficiency for InGaAs based photodetectors, and minimizes voltage and power requirements to fire the μ-LED. The use of a SPAD [122] – a photodetector with internal gain operating in Geiger mode – provides a highly sensitive means of detecting signals from the motes, where only a few photons at the receiver are needed to trigger a response. The photons emitted from the LED should exceed the dark count rate of a SPAD on the Repeater, given by the following equation (1)

$$N_{LED} > \frac{(DCR)(F)(\Delta t)}{\eta_{dura}\eta_{SPAD}} \quad (1)$$

where η_{dura} is the number of photons received at the SPAD relative to number of photons emitted by the LED, η_{SPAD} is the detection efficiency of the SPAD, *DCR* is the SPAD dark count rate, *F* is the noise margin (multiplier) for number of photons above *DCR* desired to achieve the desired signal-to-noise ratio, and Δt is the time window. Monte Carlo simulation [123] of NIR emission from the microscale LED through dura is shown in Fig. 7.8, accounting for tissue absorption and scattering [80,117], and Lambertian distribution of light output from a planar LED device.

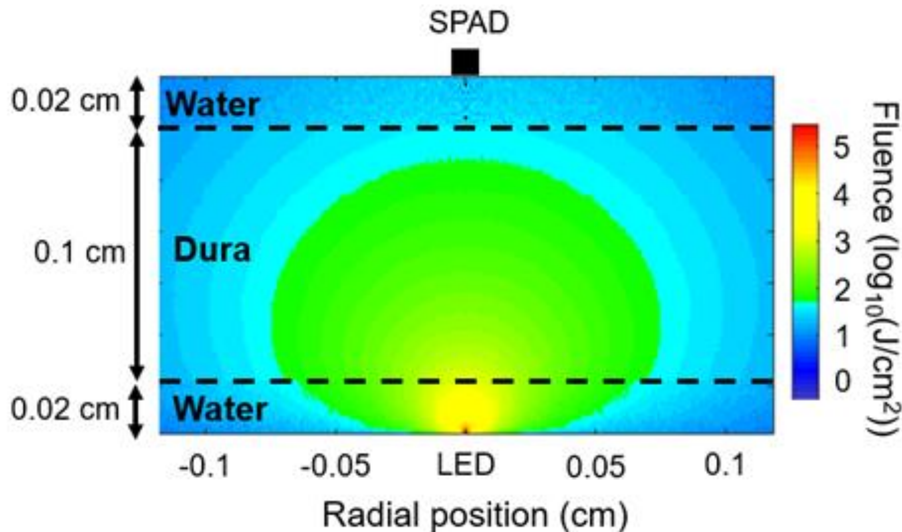


Figure 7.8. Monte-Carlo simulation of NIR emission from a μ-LED through dura to the SPAD repeater, with estimated efficiency of 0.1% (photons received at SPAD with 100 μm diameter relative to photons emitted from LED) (Simulated by Michael Barrow)

The efficiency of this optical link is estimated to be $\eta_{dura} = 0.1$ %. Assuming conservative values typical of commercial SPADs, $\eta_{SPAD} = 10$ %, $DCR = 5{,}000$ counts / second; a noise margin of $F = 100$; the LED is required to provide $N_{LED} > 1\text{x}10^6$ photons for a time window corresponding to $\Delta t = 1/DCR = 200$ μs. This corresponds to an LED optical power of 1 nW in a 200 μs pulse, where alternatively shorter pulse widths and higher LED power can be scaled to ensure detection at the Repeater. The fabricated μ-LED (50 μm x 50 μm) showed exponential *I-V* characteristics with the turn-on voltage around 1 V (below the output voltage of PV cell) as shown in Fig. 7.9 and a clear emission peak at a wavelength of 1000 nm from the photoluminescence (PL) result in Fig. 7.10. The emitted light output from LED along with the applied DC current was measured by the calibrated photodetector with 1 cm diameter, showing that μ-LED meets required optical power (> 1 nW) for wireless two-way communications when the applied current is above 10 μA as shown in Fig. 7.11.

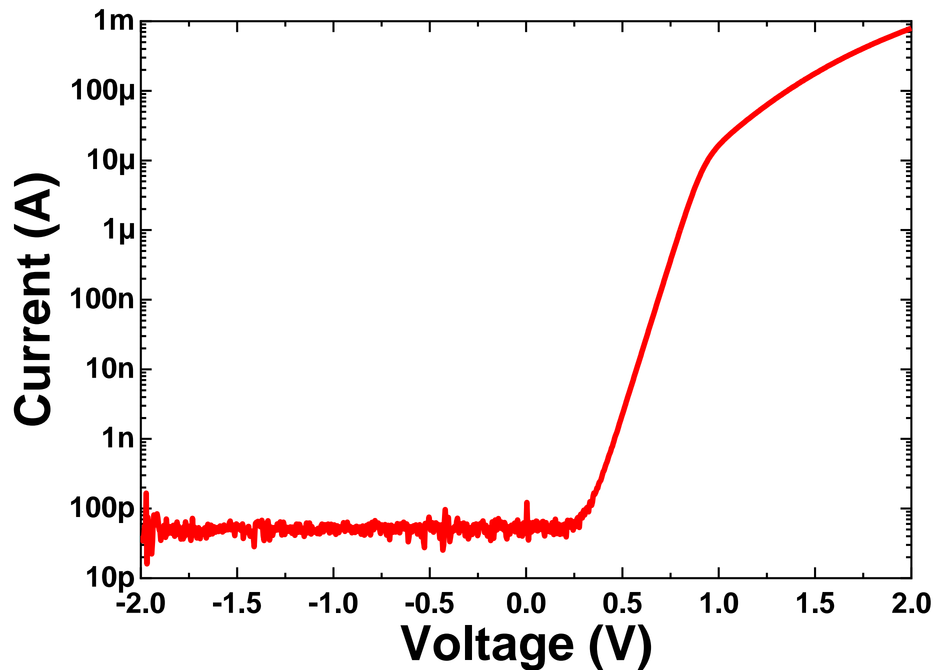


Figure 7.9. Measured *I-V* characteristic of fabricated LED with 50 μm x 50 μm size.

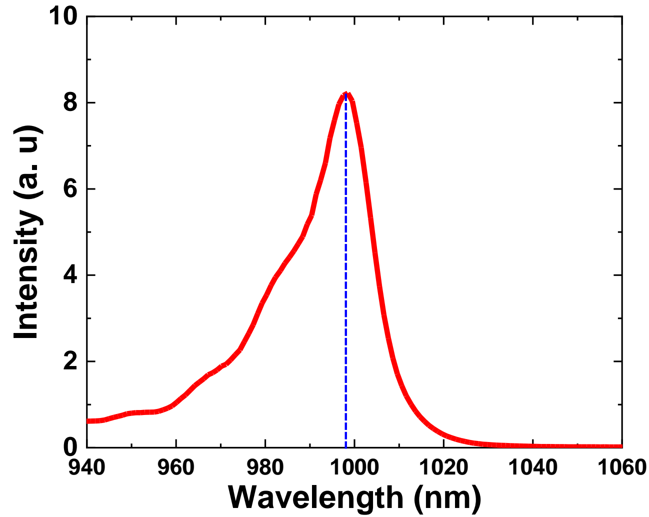


Figure 7.10. Measured photoluminescence (PL) versus wavelength curve of fabricated LED with 50 μm x 50 μm size.

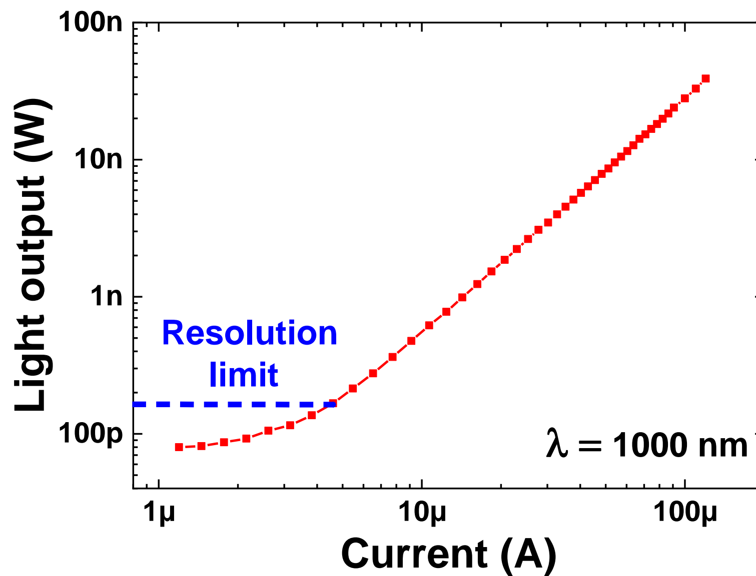


Figure 7.11. Measured light output versus applied current curve of fabricated LED with 50 μm x 50 μm size.

We also demonstrated the practical pulse detection with the SPAD. The applied input pulses to LED with 40 μs pulse width and 1.54 V amplitude (corresponding LED current ~ 839 μA) was clearly detected by the SPAD with 10 μs dead time as shown in Fig. 7.12, which is promising for the NIR based data up-link.

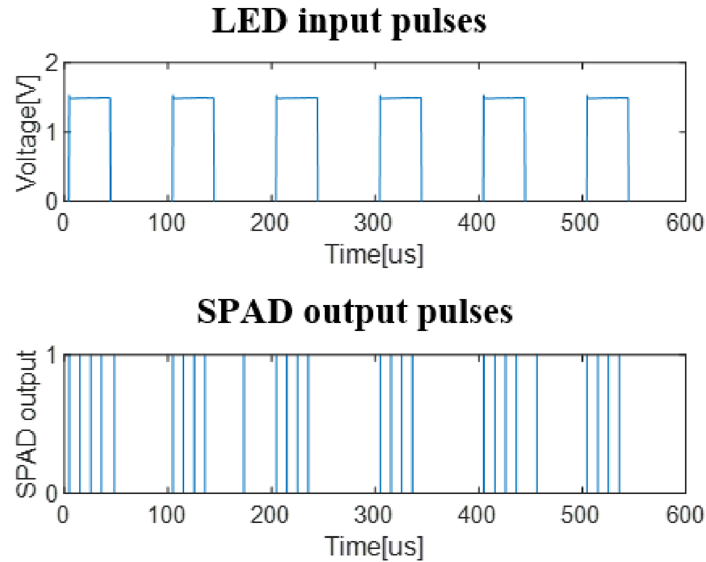


Figure 7.12. Detected SPAD output (10 μs deadtime) versus LED input pulses (40 μs pulse width, 100 μs period, 1.54 applied voltage) (Collaborating with Jongyup Lim).

7.6. Discussion

7.6.1. PV and LED isolation

We successfully demonstrated that the fabricated GaAs PV cell (190 μm x 170 μm) using the dual-junction design generated ~ 1 μW with more than 25 % power conversion efficiency and above 1.4 V output voltage under 850 nm NIR LED illumination at 100 μW/mm^2 (6 x lower than tissue exposure limit), which is sufficient to guarantee the batteryless operation of miniaturized CMOS IC chips under subcutaneous conditions. For the operation of a stacked full system, the PV / μ-LED module needs to be connected to the CMOS control circuity using the through-wafer vias and interconnects [124,125] or metal wires from the wire-bonding process. The connection of the PV / μ-LED module to CMOS circuitry requires shared cathodes between devices, requiring electrical isolation to avoid degradation due to shunt leakage current through the device stack at the required operating voltages. After sharing cathodes, the output voltage of PV cell was degraded

around 1.0 V as shown in Fig. 7.13 due to poor isolation, which is problematic to operate the full system without the additional charge storage layer. The current p-type $Al_{0.3}Ga_{0.7}As$ barrier with 100 nm thickness and $5x10^{16}$ cm^{-3} doping was not sufficient to block the leakage current, where the leakage current between LED cathode and PV anode showed the clear diode behavior as shown in Fig.7.14. In this manner, we defined an isolation trench with 10 μm wide and 7 μm deep between LED and PV by etching down to the semi-insulating GaAs substrate with high resistivity around 10 MΩ-cm. The isolation trench between PV and μLED blocked the leakage current successfully below 10's nA range (Fig. 7.14) even under NIR LED illumination, which makes the output voltage of PV cell recovered to its originally designed value (> 1.4 V) as shown in Fig. 7.15. Though this isolation method was working properly without the additional modification of current epi-structure, this method made unwanted area losses and increased the fabrication complexity for patterning the PR and depositing the interconnects due to deep trench with the poor aspect ratio. A new epi-structure using the AlGaAs based p-n junction isolation layers between PV and μ-LED might be helpful to block the leakage current by increasing the barrier height.

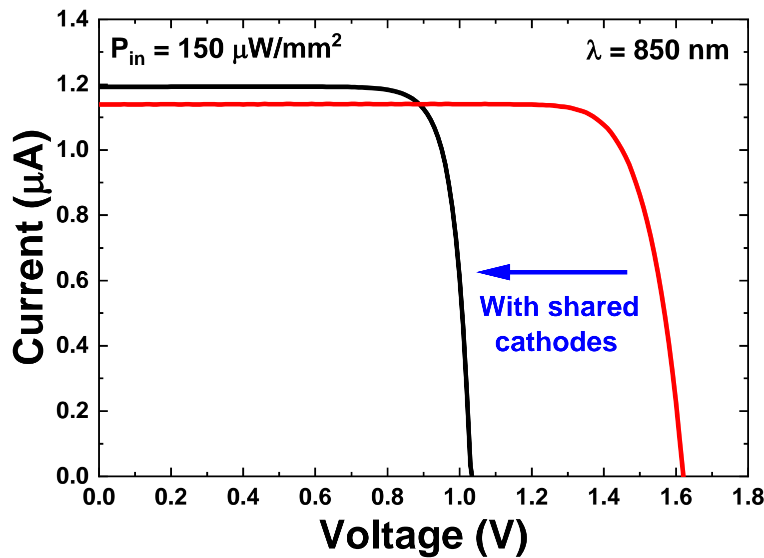


Figure 7.13. Measured *I-V* characteristics of PV cell before / after the shared connection to LED cathode under 850 nm NIR LED illumination at 150 μW/mm^2.

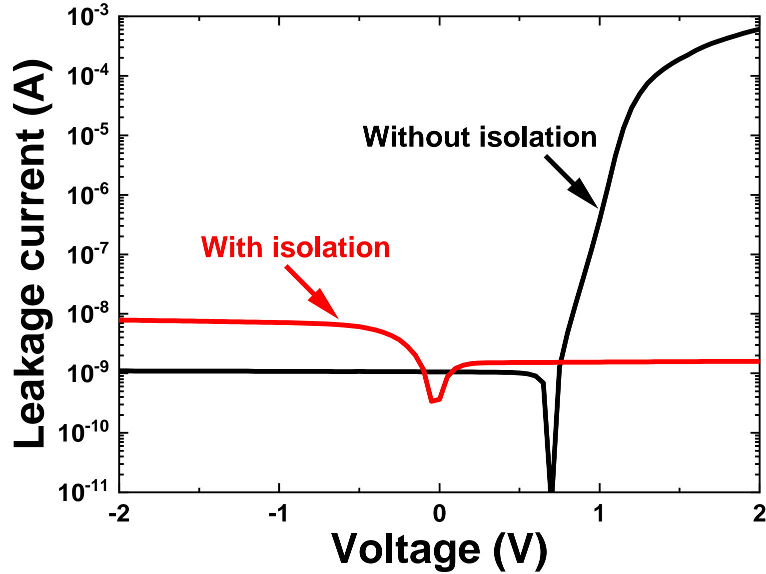


Figure 7.14. Measured leakage current between LED cathode and PV anode with / without the isolation trench.

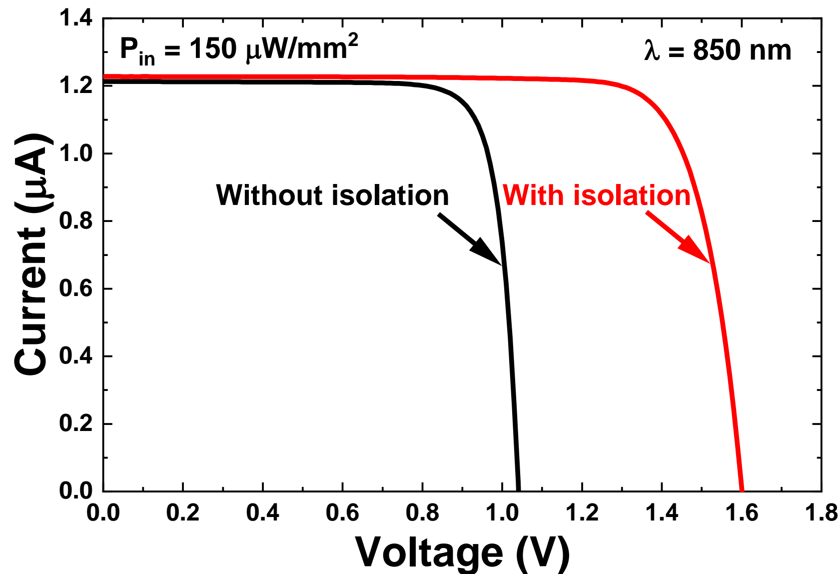


Figure 7.15. Measured *I-V* characteristics of PV cell with / without the isolation trench under 850 nm NIR LED illumination at 150 μW/mm^2.

7.6.2. μ-LED performance

The monolithically integrated $In_{0.2}Ga_{0.8}As$ QW μ-LED (50 μm x 50 μm) showed good exponential *I-V* characteristics and emitted the enough light (> 1 nW) with the center wavelength

at 1000 nm for NIR data link. The fabricated LED demonstrated the example detection of digital pulses (pulse width ~ 40 μs, period ~ 100 μs, applied LED current amplitude ~ 800 μA) using the highly sensitive SPAD for wireless two-way communications. However, the system operation using shorter pulses below 100 ns is preferred for the energy efficient detection at the SPAD, where the current LED might be problematic because the LED requires more than 1 mA applied current to emit the optical power > 1 μW as shown in Fig. 7.11. This low-intensity light output can be explained by the extracted external quantum efficiency (EQE) from the *L-I* curves. The extracted EQE was below 0.1 %, which is far much lower than simulated EQE results ~ 1 % assuming the 50 % internal quantum efficiency (IQE) and 2 % extraction efficiency through the planar surface. The EQE measurements for variable area μ-LEDs were done to characterize the sources of poor EQE of μ-LED as shown in Fig. 7.16. Variable area μ-LEDs showed clear degradation in EQE below 100 μm x 100 μm due to the possible increase in sidewall / perimeter recombination losses, mitigated by additional sidewall passivation [49-51] and changing pad geometry for current spreading.

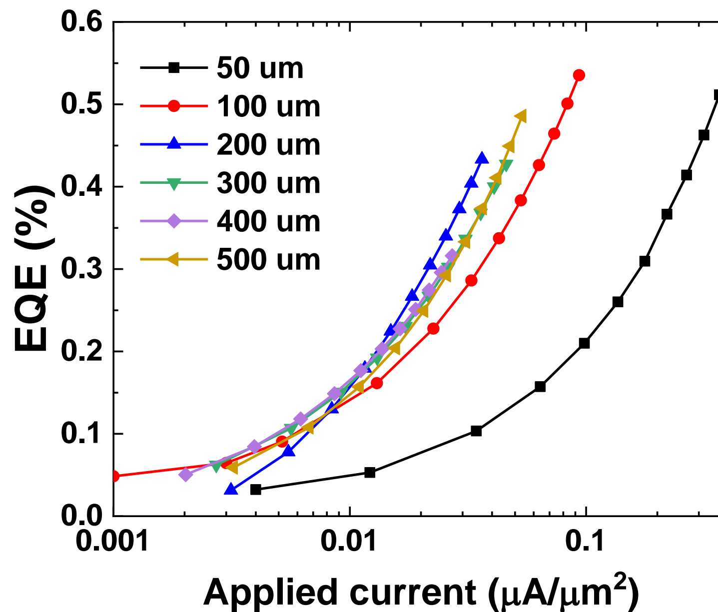


Figure 7.16. Extracted EQE versus applied current curves of variable size LEDs.

The temperature dependent PL measurement was done for the InGaAs epi-wafer to estimate the IQE, showing that the clear blue shift of peak wavelengths and the gradual improvement in the PL intensity were observed as the temperature was decreased from 300 K to 13 K as shown in Fig. 7.17. However, the rough extraction of IQE by comparing the peak intensity at 13 K to the peak intensity at 300 K was around 10 %, which means that InGaAs QW material is relatively fine and these is not a major issue in epitaxial structure and quality of growth.

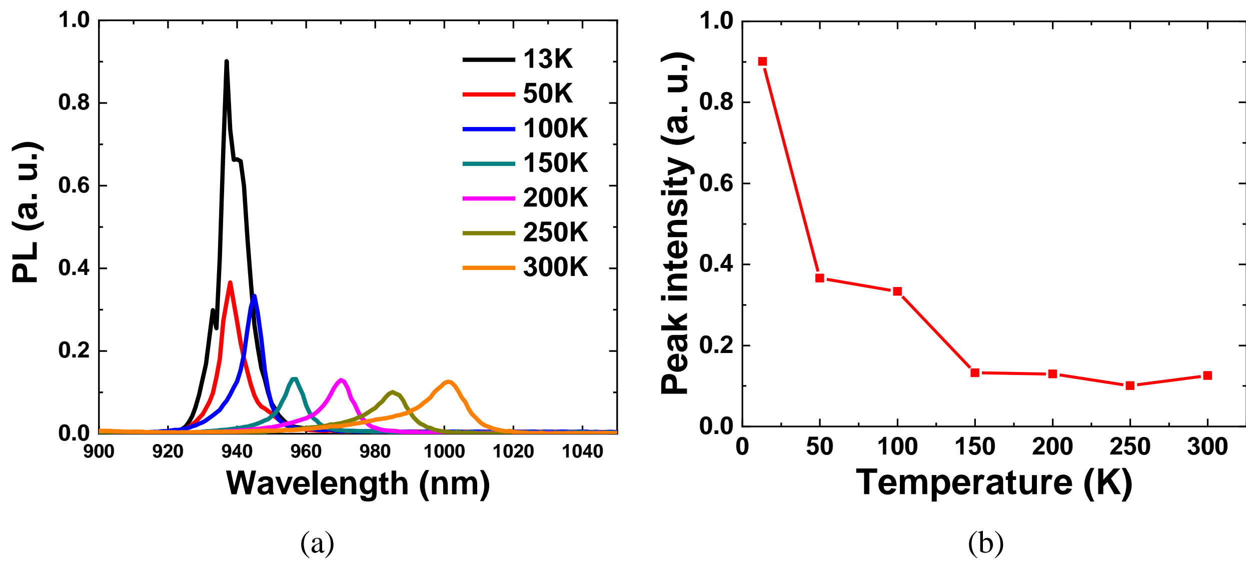


Figure 7.17. (a) Measured temperature dependent photoluminescence spectra of InGaAs LED and (b) extracted peak intensity values versus variable temperature from 300 K to 13 K (collaborating with Anthony Aiello).

In summary, main reasons for the low EQE of InGaAs LED are connected to poor light extraction efficiency through the planar surface, current spreading and dead area near sidewall. Further improvements in LED performances are possible using the surface texturing or roughing [126] to improve the extraction efficiency, modifying the cladding layer design for better light extraction and current spreading, and mitigating the sidewall / perimeter recombination losses from the chemical and dielectric passivation studies.

7.7. Conclusion

Our monolithic PV / μLED module demonstrates the viability of near-infrared light to meet power and data communications requirements for devices at dimensions desired for bio-implantable systems such as "neural dust". The dual junction GaAs PV cell provides sufficient power (~ 1 μW) and voltage (> 1.4 V) for battery-less operation of CMOS circuitry under 850 nm NIR illumination at 100 μW/mm^2 within the tissue exposure limit. The monolithically integrated InGaAs μ-LED emits NIR light pulses at detectable power levels (> 1 nW) under realistic energy harvesting levels from PV cells, where we have demonstrated example digital pulse detection with a single photon avalanche photodiode (SPAD).

CHAPTER 8

Future work and conclusion

8.1. Future work

8.1.1. 3D vertical integration

The proposed system (in Chapter 7) for recording and transmitting the neural signals through the NIR optical link requires the wafer-level vertical integration of the GaAs PV / LED module and CMOS silicon chips as shown in Fig. 8.1, while maintaining a total thickness below 150 μm. The integration processes [124,125] are including the through-wafer via (TWV) processing, wafer thinning, flip chip bonding, laser dicing, neural probe insertion, packaging and die singulation. TWVs are defined both for GaAs (Fig. 8.2) and silicon wafers using the well-established deep reactive ion etching (DRIE) recipes (chlorine based etch for GaAs [127] and fluorine based etch for silicon [128]), deeper than the target thickness of wafer thinning in order to expose the via after the wafer thinning process. Next, a 30 nm Al_2O_3 for the insulating layer and subsequent a 10 nm Pt for the conducting layer are deposited via atomic layer deposition (ALD), which provides a conductive path through the TWVs while preventing shorting to the substrate. The patterned Pt layer is used as a seed layer for electrochemical deposition (ECD) of copper to fill the TWV, which improves the conduction of TWVs. A parylene layer with 20 μm thickness is deposited prior to thinning for the mechanical support of thinned GaAs and silicon wafers around 50 μm thickness. After the thinning process, back contacts on the thinned GaAs wafer are defined

using the sputtered films with 10 nm / 500 nm Ti / Au. For silicon chips, the additional holes for the insertion and the electrical connection of neural probes are etched on the backside of the chips using DRIE and deposit the insulating Al_2O_3 and the conducting Pt again using ALD. Both flexible GaAs and silicon wafers are then mounted to the rigid silicon carrier wafers and attached together using the flip chip bonding process with 30 µm solder balls on the back contacts of GaAs and the front contacts of silicon followed by the alignment of chips and a solder reflow. Once two chips are bonded together, the assemblies are fully delineated by laser dicing, where the diced assemblies are mounted temporally on the tape for the future packaging process. The neural probes are inserted to the assemblies using the silver paint for the electrical connection. The fully assemblies are passivated by bio-compatible packaging methods for multi-year implantation. \

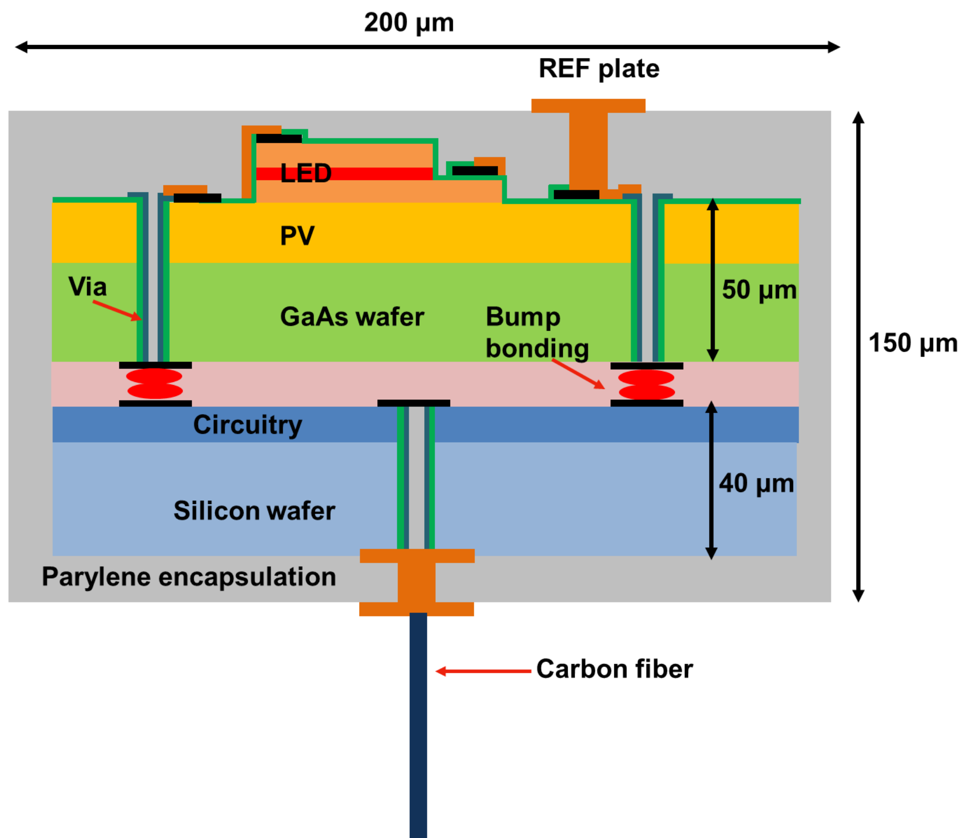
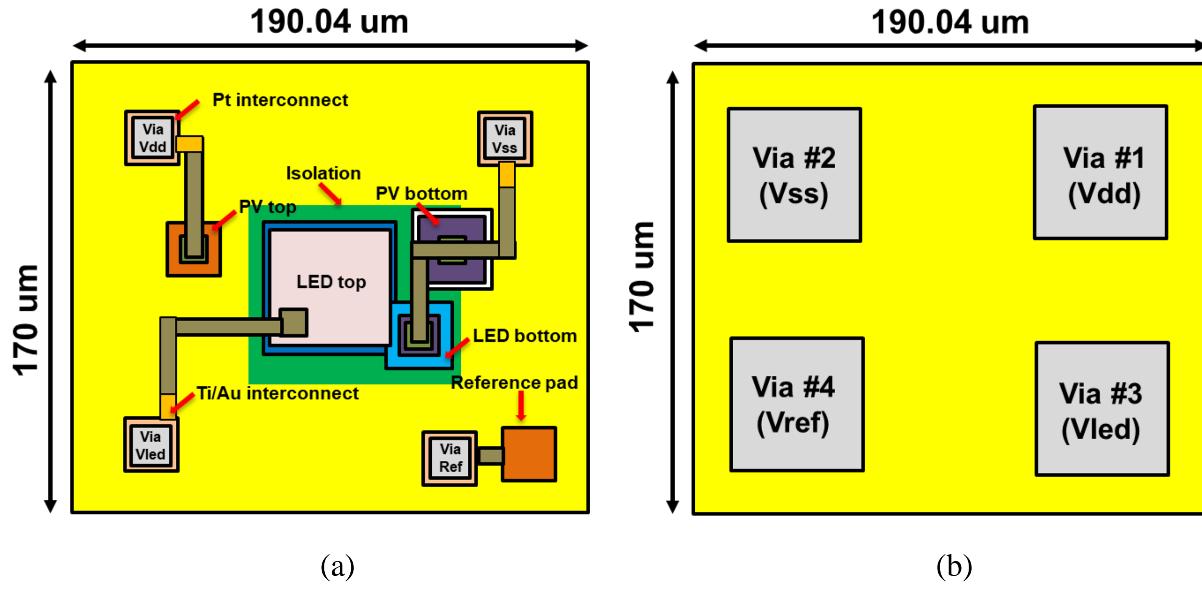


Figure 8.1. Cross-sectional concept diagram of the integration of GaAs PV / LED modules, silicon chips and neural probe.



(a) (b)

Figure 8.2. Schematic diagrams for (a) the front side and (b) back side of GaAs PV / LED module for the vertical integration, illustrating the through wafer via, interconnects and back contacts.

Initial results for TWVs for GaAs (Fig. 8.3 as an example) and silicon showed the well-defined TWVs with 50 µm deep and 20 µm wide, where the exposed sidewall was covered by the insulating 30 nm Al_2O_3 and subsequent conducting 10 nm Pt layers.

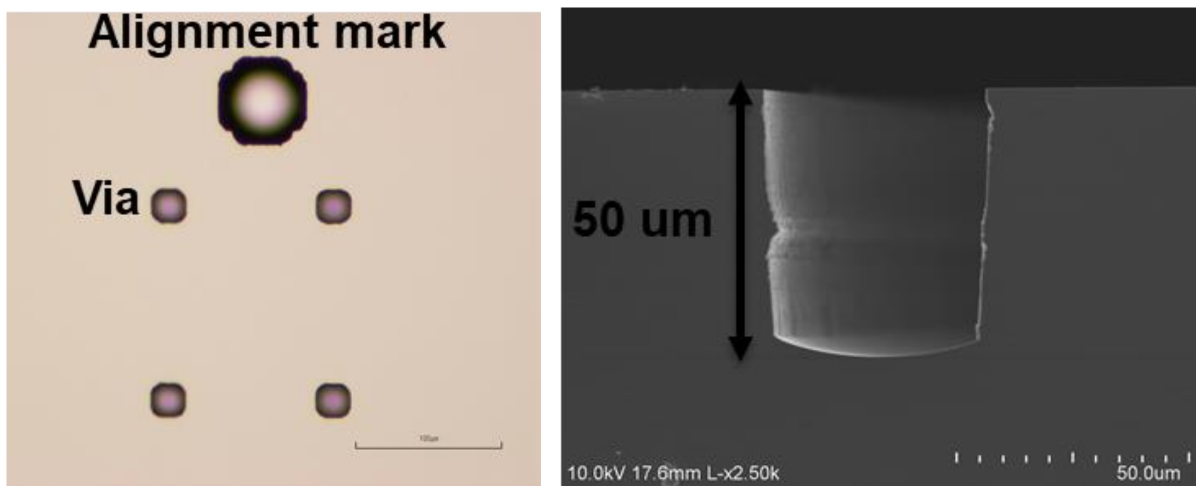
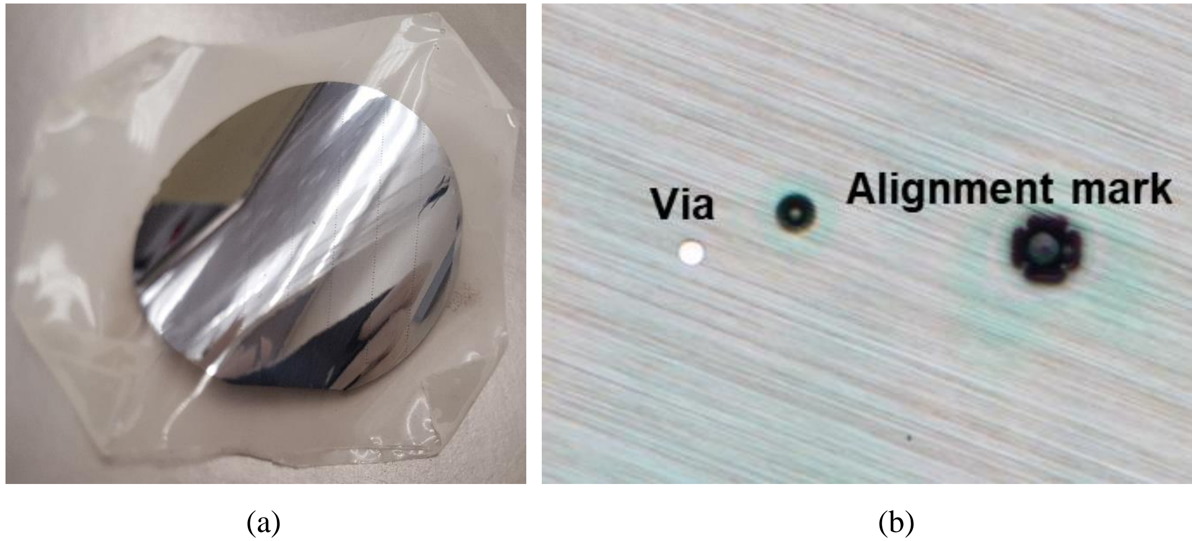


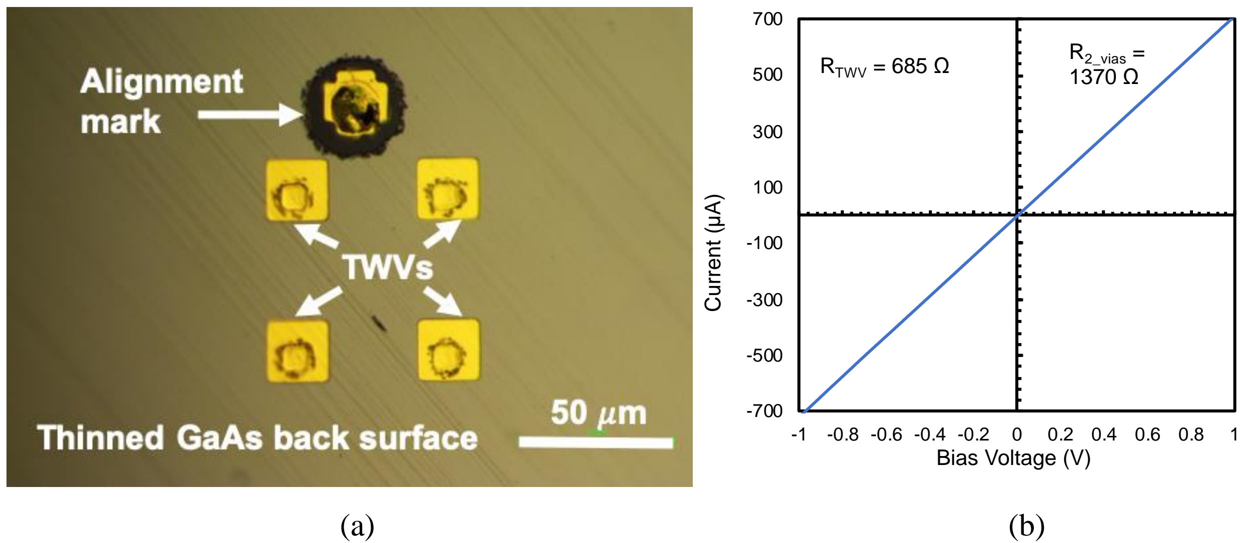
Figure 8.3. (a) Microscope and (b) scanning electron microscopy (SEM) images of through wafer vias of GaAs, deeper than 50 µm.

The wafer thinning process followed by Ti / Au back contact deposition on the thinned wafers were successfully done as shown in Fig. 8.4, where the TWVs were well exposed and the electrical connection between top and bottom contacts through the thin ALD conducting layer with a resistance of 685 Ω was observed as shown in Fig. 8.5.



(a) (b)

Figure 8.4. (a) An image of the thinned GaAs wafer mounted to the flexible tape and (b) a microscope image of the backside of thinned wafer, exposing the TWVs and predefined alignment marks.



(a) (b)

Figure 8.5. (a) An optical microscope image of backside of thinned GaAs with TWVs, and (b) electrical characteristics measured through two GaAs TWVs in series (collaborating with Michael Barrow).

Further process development and improvement will be required to make the full assemblies in terms of via backfill using the ECD copper, electrical properties of conducting layers through TWVs, flip chip bonding, carrier wafer handling, laser dicing and packaging.

8.1.2. AlGaAs double heterojunction LED

A repeater unit (RU) in the epidural space (discussed in Chapter 7) for the wireless communication with the integrated assemblies of GaAs PV / LED modules, silicon chips and the external unit (EU). The RU emits modulated 850nm NIR light for power transfer to PV and data downlink to the CMOS chips. The RU receives the neural recording signals through the dura mater using an array of 1000 nm NIR SPADs, where the current single InGaAs / InP based SPADs [121,129] show reasonable detection performances above 10 % quantum efficiency (λ = 900 nm ~ 1700 nm) that is sufficient to operate the current system. However, InGaAs / InP based SPADs have some issues to make an array structure at mm-scale size for our target of 1000 + channel count, requiring the integrated cooling system and yield issues [121,129]. On the other hand, the CMOS SPAD arrays [122,130], at mm-scale are already developed with the operating wavelength range from 340 nm to 900 nm as shown in Fig. 8.6, which means that our emission wavelength at 1000 nm from InGaAs LED is not adequate for the wireless communication to the CMOS SPAD array. In this manner, we switch the target wavelength to 780 nm because this wavelength has good transmittance of human dura mater (> 30 %) [80,117], selective to the powering wavelength at 850 nm to GaAs PV and the well-established LED structures using AlGaAs based double heterojunction (DH) [131,132] without the concern for the lattice mismatch. The proposed AlGaAs DH device structure is shown in Fig. 8.7. The active $Al_{0.12}Ga_{0.88}As$ layer cladded by larger bandgap $Al_{0.3}Ga_{0.7}As$ layers improves the carrier injection efficiency and reduces non-radiative

recombination losses from the surface. The top p+ AlGaAs layer is thick around 1 μm for the better current spreading.

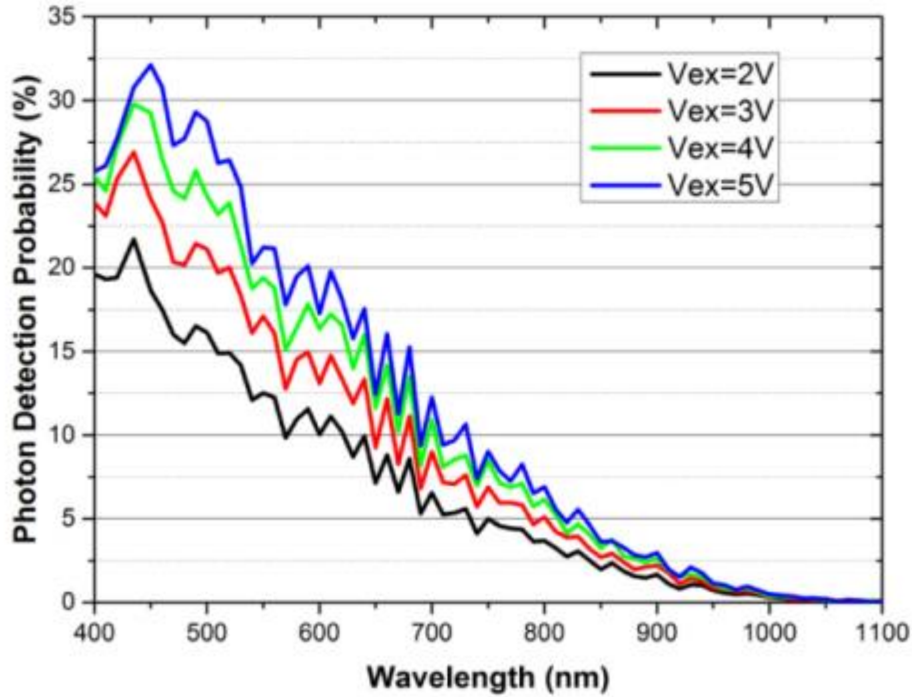
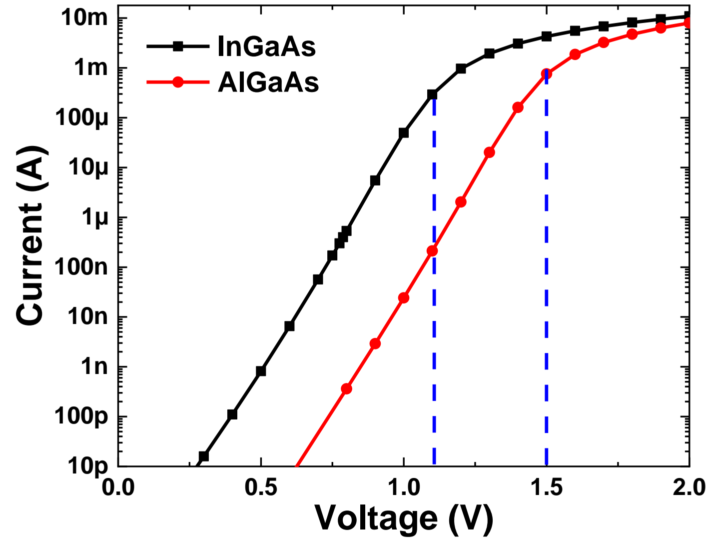


Figure 8.6. Photon detection probability along with wavelengths at different excess bias at room temperature (adopted from [122]).

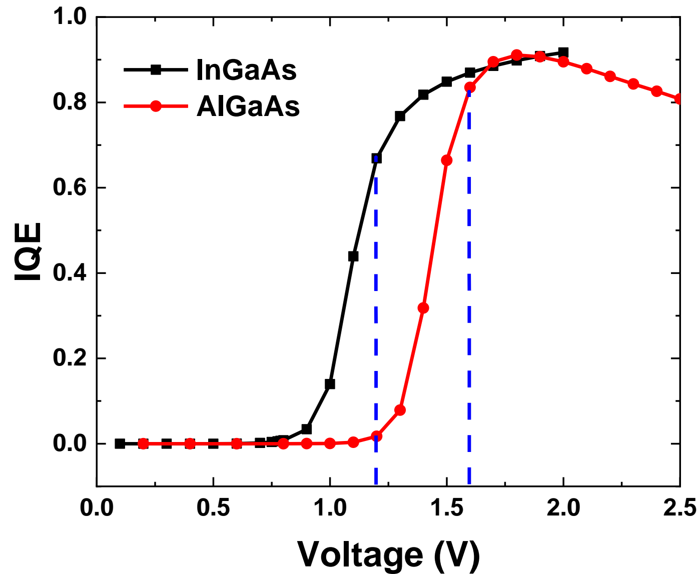
200 nm GaAs:Si (2.0E+19 p-type), 580 ℃, 1 μm/hr
1000 nm $Al_{0.30}Ga_{0.70}As$ (2.0E+18 p-type), 650 ℃, 1.43 μm/hr
100 nm $Al_{0.12}Ga_{0.88}As$ (UD), 650 ℃, 1.14 μm/hr
500 nm $Al_{0.30}Ga_{0.70}As$:Si (1.0E+18 n-type), 650 ℃, 1.43 μm/hr
100 nm GaAs:Si (1.0E+18 n-type), 580 ℃, 1 μm/hr
GaAs:Si substrate (500 μm, DSP)

Figure 8.7. Optimized device parameters of DH AlGaAs LED with the emission wavelength at 780 nm.

The simulation results of optimized DH AlGaAs LED compared to the original InGaAs LED as shown in Fig. 8.8 show good current-voltage characteristics with the turn-on voltage above 1.5 V while maintaining high IQE above 80 % at our operating regime, which is promising for our future repeater designs using CMOS SPAD arrays for the operation of 1000 + count neural probe assemblies.



(a)



(b)

Figure 8.8. (a) Simulated current versus voltage characteristics and (b) IQE versus voltage curves of DH AlGaAs LED, compared to InGaAs QW LED.

8.1.3. Multi-junction PV designs for visible light

The data of dual-junction (DJ) PV cells and modules thus far has focused on a monochromatic wavelength of 850 nm, providing an important spectral region for bio-implantable devices or laser power converters. Extending the DJ approach to indoor lighting applications requires designs that shift the peak EQE towards visible wavelengths. This may be accomplished by either reducing the top junction thickness (Fig. 6.4), or increasing the bandgap energy for the optical absorption regions of the device. Reducing thickness of a top GaAs junction is not an optimal solution since the bandgap energy of GaAs material at 1.424 eV is not perfectly adequate for the indoor lighting spectrum, requiring wider bandgap around 1.9 eV [15,21]. Increasing aluminum content in the top GaAs absorbing region can be an effective approach to shift peak EQE to the visible spectral region while increasing the bandgap energy close to the ideal bandgap energy for the indoor lighting spectrum. Simulated EQE spectra for DJ designs with varying aluminum mole fraction in top junctions are shown in Fig. 8.9, demonstrating a shift to visible wavelengths. High EQE values are reached in the 600-650 nm region, corresponding to high flux regions for the soft white artificial lighting with 3000 K color temperature. Simulated J-V characteristics for DJ designs with GaAs and $Al_{0.4}Ga_{0.6}As$ absorber top junctions are shown in Fig. 8.10 for illumination with a soft white LED. The use of higher aluminum mole fraction in the top cell results in a substantial increase in power conversion efficiency with values exceeding 30 %. The incorporation of a wider bandgap top junction also provides a higher output voltage due to the more optimal match to the ideal bandgap energy for the indoor lighting spectrum [15,21].

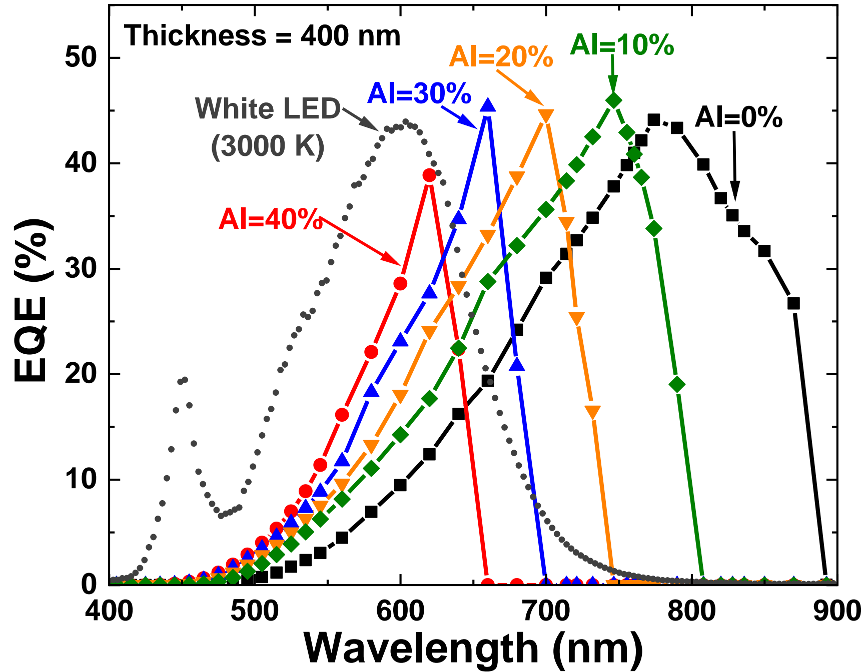


Figure 8.9. Simulated EQE spectra for variable aluminum mole fraction of top PV cells in the DJ structure with the fixed thickness of top PV cell at 400 nm and comparison with the normalized spectrum of commercialized white LED with 3000 K color temperature.

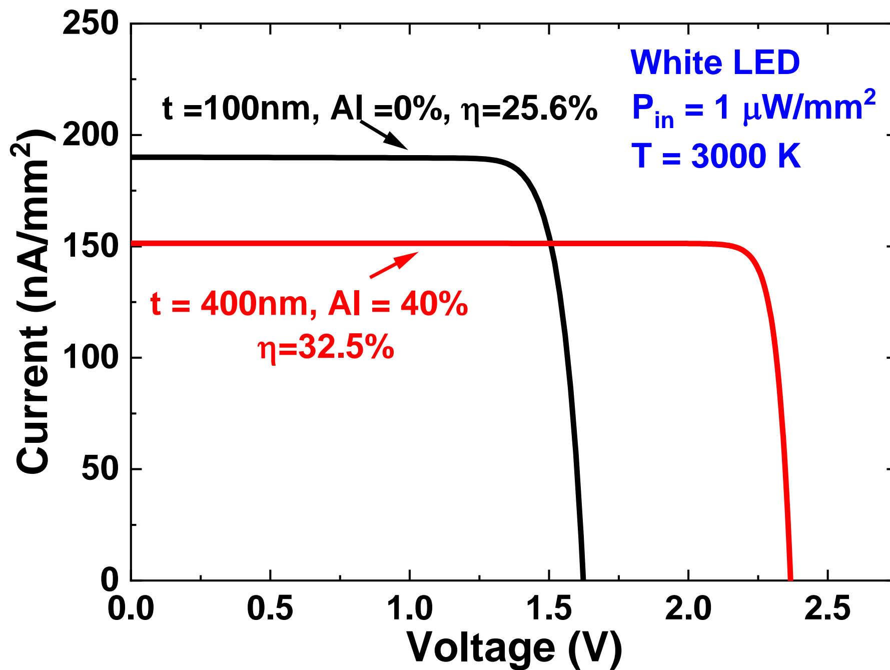


Figure. 8.10. Simulated *J-V* characteristics of dual junction cells with variable aluminum mole fraction of a top cell under white LED illumination (3000 K color temperature) at 1 μW/mm^2.

8.2. Conclusion

This thesis covers an in-depth study of photovoltaic energy harvesting for the Internet of Things (IoT) and bio-implantable devices based on mm-scale sensors, which can be applied to a variety of applications including biomedical devices, surveillance, micro-robots and industrial monitoring. Energy harvesting approaches to power miniaturized mm-scale sensors have traditionally utilized thermal energy, mechanical vibrations and radio frequency electromagnetic radiation. However, the achievement of efficient energy harvesting at the mm-scale or sub mm-scale has been elusive.

In this work, I show that photovoltaic cells and modules at the mm-scale or sub mm-scale can be an alternative means of wireless power transfer to mm-scale sensors for IoT and bio-implantable devices, utilizing ambient indoor lighting (425-650 nm) or intentional irradiation of near-infrared LED sources (700-1100 nm) through biological tissue. Dark current and shunt conductive paths in photovoltaic cells become much more important at these small dimensions and low flux illumination conditions in comparison to typical outdoor solar irradiation (approximately a factor of 1,000 lower flux than AM 1.5).

Single silicon and GaAs photovoltaic cells at the mm-scale can achieve a power conversion efficiency of greater than 17 % for silicon and 30 % for GaAs under 850 nm NIR irradiation at 1 μW/mm^2 through the optimized device structure and sidewall/surface passivation studies, which guarantees perpetual operation of mm-scale sensors. These photovoltaic cells demonstrate highly efficient energy harvesting through various biological tissue samples from ambient sunlight, or irradiation from infrared sources. Sufficient power generation above 50 nW/mm^2 is achieved for perpetual operation of mm-scale systems for implant depth of at least 15 mm including hair / skin / muscle / bone under 850 nm NIR illumination at 134 μW/mm^2 within the maximum tissue exposure limit. Furthermore, monolithic single-junction GaAs photovoltaic modules offer an

efficient means for voltage up-conversion to charge battery directly in mm-scale systems. I demonstrate SJ GaAs PV modules at the mm-scale with high efficiency under low-flux conditions, where AlGaAs junction barrier isolation provided a critical step in limiting shunt leakage current between series connected cells. I observed power conversion efficiency of great than 26 % under 850 nm infrared LED illumination at 1 $\mu W/mm^2$ and 16 % under white LED illumination at 586 lux (1.4 $\mu W/mm^2$), with a 90 % voltage up-conversion efficiency to reach an operating voltage of 5 V for direct battery charging. However, there are fill factor losses associated with shunt leakage paths through the shared substrate and efficiency losses when scaling to small systems due to perimeter losses. There is a continuing challenge to miniaturize such PV systems down to the sub mm-scale with minimal optical losses from device isolation and metal interconnects and efficient voltage up-conversion.

Vertically stacked DJ PV cells and modules are demonstrated to increase operating voltage for direct powering of miniature devices for IoT and bio-implantable applications with low-irradiance narrowband spectral illumination. The DJ approach increases the output voltage per cell and minimizes area losses from device isolation and interconnects in comparison to SJ cells. DJ PV cells at small dimensions (150 μm x 150 μm) demonstrate power conversion efficiency greater than 22 % with more than 1.2 V output voltage under low-flux 850 nm NIR LED illumination at 6.62 $\mu W/mm^2$, which is sufficient for batteryless operation of miniaturized CMOS IC chips. The output voltage of DJ PV modules with eight series-connected single cells was greater than 10 V while maintaining an efficiency of more than 18 %. Further power conversion efficiency improvements are expected by optimizing designs to minimize photocurrent collection losses and shunt resistance losses through the substrate in modules. In addition to monochromatic NIR

illumination, the GaAs DJ approach also shows promise for efficient energy harvesting under narrowband artificial indoor lighting conditions.

Finally, monolithic PV/LED modules at the sub mm-scale for brain-machine interfaces are demonstrated, enabling two-way optical power and data transfer in a through-tissue configuration. The DJ GaAs PV cell provides sufficient power (~ 1 μW) and voltage (> 1.4 V) for batteryless operation of CMOS circuitry under 850 nm NIR illumination at 100 $\mu W/mm^2$ within the tissue exposure limit. The monolithically integrated InGaAs μ-LEDs emit NIR light pulses (1000 nm) at detectable power levels (> 1 nW) under realistic energy harvesting levels from PV cells, where we have demonstrated example digital pulse detection with a single photon avalanche photodiode (SPAD). The wafer-level assembly plan for the 3D vertical integration of three different systems including GaAs LED/PV modules, CMOS silicon chips, and neural probes is proposed, using the through-wafer vias, wafer thinning, flip chip bonding, laser dicing, and final packaging.

Appendix

Fabrication Recipes for Silicon and GaAs Photovoltaic Cells

1. Silicon Photovoltaic cells

1.1. Surface n-type doing

1.1.1. RCA clean

1.1.2. Phosphorous doping (S5T1) : $POCl_3$ at 975 ℃

(Deposition : 12 min, Anealing : 10 min), PSG thickness 80nm

1.1.3. Measured sheet resistance: 9.65 Ω / sq (epi-wafer), 8.8 Ω / sq

(Monitor wafer: Sheet resistance without surface doping, 755 Ω / sq)

1.1.4. BHF for PSG etch (After the etching, the surface should be 'Hydrophobic')

1.2. Shallow device isolation #1

1.2.1. Surface clean: Nanostrip for 15 min

1.2.2. Dehydration bake: 150 ℃, 10 min

1.2.3. PR coating (ACS200): SPR 3.0, 2000 rpm, 3 um thick,

1.2.4. PR exposure (MA6): 8 s exposure time, hard contact, 30um gap

1.2.5. Post exposure bake (ACS200): 115 ℃, 90 s

1.2.6. PR development (ACS200): 60 s, Develop 300DEV (Recipe)

1.2.7. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

1.2.8. Back surface cleaning: Acetone, IPA clean

1.2.9. DRIE (STS4): 40 s etch time, 3.4 µm target etch depth

1.2.10. PR strip (Yes plasma stripper): 800 W, 400 s, 150 ℃, 80 sccm O_2

1.2.11. Wafer cleaning : 5 min Acetone, 5 min IPA

1.2.12. DI water Spin / Rinse / Dry

1.3. Deep device isolation #2

1.3.1. Wafer cleaning: 5 min Acetone, 5 min IPA

1.3.2. DI water Spin / Rinse / Dry

1.3.3. Dehydration bake: 150 ℃, 10 min

1.3.4. PR coating (ACS200): SPR 3.0, 2000 rpm, 3 um target,

1.3.5. PR exposure (MA6): 8 s exposure time, hard contact, 30 µm gap

1.3.6. Post exposure bake (ACS200): 115 ℃, 90 s

1.3.7. PR development (ACS200): 60 s, Develop 300DEV (Recipe)

1.3.8. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

1.3.9. Back surface cleaning: Acetone, IPA clean

1.3.10. DRIE (STS4): 7 min 30 s etch time, 44 µm target etch depth

1.3.11. PR strip (Yes plasma stripper): 800 W, 400 s, 150 ℃, 80 sccm O_2

1.3.12. Wafer cleaning: 5 min Acetone, 5 min IPA

1.3.13. DI water Spin / Rinse / Dry

1.4. Etch heavily doped surface layer ~ 300 nm

1.4.1. Wafer cleaning: 5 min Acetone, 5 min IPA

1.4.2. DI water Spin / Rinse / Dry

1.4.3. Dehydration bake: 150 ℃, 10 min

1.4.4. HMDS deposition (Yes image reversal oven)

1.4.5. PR coating (CEE spinner): SPR 7.0, 2000 rpm, 10 µm thick

1.4.6. Soft bake (Hot plate): 85 ℃, 330 s

1.4.7. PR exposure (MA6): 30 s exposure time, hard contact, 30 µm gap

1.4.8. Post exposure delay: 3 hours to finish the photochemical reaction

1.4.9. Post exposure bake (Hot plate): 85 ℃, 90 s

1.4.10. PR development (CEE developer): AZ726, DP 80-80

1.4.11. Plasma ashing (Yes plasma stripper): 100 W, 200 s, 35 sccm O_2

1.4.12. DRIE (P5000): 1 min etch time, 300 nm target etch depth,

Poly PAT BKM (Recipe, 40 sccm HBr, 40 sccm Cl_2)

1.4.13. PR strip (Yes plasma stripper): 800 W, 400 s, 150 ℃, 80 sccm O_2

1.4.14. Wafer cleaning: 5 min Acetone, 5 min IPA

1.4.15. DI water Spin / Rinse / Dry

1.4.16. Residue removal: 5 min BHF

1.5. Passivation layer deposition

1.5.1. RCA clean

1.5.2. Dry oxide deposition (S3T1): 15 min growth at 900 ℃, 40 nm target

1.5.3. Amorphous silicon deposition (S3T3): 40 min growth at 560 ℃,

25 nm target thickness, 4.35 refractive index

1.5.4. LPCVD Si_3N_4 (S2T3): 10 min growth at 800 ℃, 50 nm target thickness

1.6. Metal openings – Top

1.6.1. Wafer cleaning: 5 min Acetone, 5 min IPA

1.6.2. DI water Spin / Rinse / Dry

1.6.3. Dehydration bake: 150 ℃, 10 min

1.6.4. HMDS deposition (Yes image reversal oven): 300 s

1.6.5. PR coating (CEE spinner): SPR 7.0, 1000 rpm, 15 µm thick

1.6.6. Soft bake (Hot plate): 85 ℃, 600 s

1.6.7. PR exposure (MA6): 45 s exposure time, hard contact, 30 µm gap

1.6.8. Post exposure delay: 4 hours to finish the photochemical reaction

1.6.9. Post exposure bake (Hot plate): 85 ℃, 600 s

1.6.10. PR development (CEE developer): AZ726, DP 80-80, DP 60-60

1.6.11. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

1.6.12. RIE for dry oxide (LAM9400): 90 s etch time, 150 nm target etch depth, mnf_oxide1 (Recipe)

1.6.13. RIE for Si_3N_4 (LAM9400): 60 s etch time, 100 nm target etch depth, mnf_oxide1 (Recipe)

1.6.14. RIE for a-Si (LAM9400): 60 s etch time, 150 nm target etch depth, mnf_oxide1 (Recipe)

1.6.15. Wafer cleaning: 5 min Acetone, 5 min IPA

1.6.16. DI water Spin / Rinse / Dry

1.6.17. Sample cleaning (Yes plasma stripper): 800 W, 120 s, 150 ℃, 80 sccm O_2

1.7. Metal openings - Bottom

1.7.1. Wafer cleaning: 5 min Acetone, 5 min IPA

1.7.2. DI water Spin / Rinse / Dry

1.7.3. Dehydration bake: 150 ℃, 10 min

1.7.4. HMDS deposition (Yes image reversal oven): 300 s

1.7.5. PR coating (CEE spinner): SPR 7.0, 1000 rpm, 15 µm thick

1.7.6. Soft bake (Hot plate): 85 ℃, 600 s

1.7.7. PR exposure (MA6): 80 s exposure time, hard contact, 30 µm gap

1.7.8. Post exposure delay: 4 hours to finish the photochemical reaction

1.7.9. Post exposure bake (Hot plate): 85 ℃, 600 s

1.7.10. PR development (CEE developer): AZ726, DP 80-80, DP 80-80

1.7.11. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

1.7.12. RIE for dry oxide (LAM9400): 180 s etch time, 400 nm target etch depth, mnf_oxide1 (Recipe)

1.7.13. RIE for Si_3N_4 (LAM9400): 180 s etch time, 300 nm target etch depth, mnf_oxide1 (Recipe)

1.7.14. RIE for a-Si (LAM9400): 180 s etch time, 200 nm target etch depth, mnf_oxide1 (Recipe)

1.7.15. Wafer cleaning: 5 min Acetone, 5 min IPA

1.7.16. DI water Spin / Rinse / Dry

1.7.17. Sample cleaning (Yes plasma stripper): 800 W, 120 s, 150 ℃, 80 sccm O_2

1.8. Metal patterning for top and bottom contacts

1.8.1. Wafer cleaning: 5 min Acetone, 5 min IPA

1.8.2. DI water Spin / Rinse / Dry

1.8.3. Pre-metal cleaning: 100:1 HF, 120 s etch time

1.8.4. Metal deposition (Enerjet): Aluminum, 300 nm target thickness

1.8.5. HMDS deposition (Yes image reversal oven): 300 s

1.8.6. PR coating (CEE spinner): SPR 3.0, 1000 rpm, 5 µm thick

1.8.7. Soft bake (Hot plate): 115 ℃, 90 s

1.8.8. PR exposure (MA6): 24 s exposure time, hard contact, 30 µm gap

1.8.9. Post exposure delay: 1-3 hours to finish the photochemical reaction

1.8.10. Post exposure bake (Hot plate): 115 ℃, 90 s

1.8.11. Image reversal (Yes image reversal oven): 45 min

1.8.12. Flood exposure (MA6): 50 s exposure time, hard contact, 30 µm gap

1.8.13. Post exposure delay: 1-3 hours to finish the photochemical reaction

1.8.14. Post exposure bake (Hot plate): 115 ℃, 90 s

1.8.15. PR development (CEE developer): AZ726, DP 80-80

1.8.16. Flood exposure (MA6): 30 s exposure time, hard contact, 30 µm gap

1.8.17. PR development (CEE developer): AZ726, DP 80-80

1.8.18. Hard baking (Hot plate): 110 ℃, 300 s

1.8.19. Aluminum etching (Acid 73): 100 Å/s etch rate, 50 ℃,

60 s etch time (10 s over etch)

1.8.20. Wafer cleaning: 5 min Acetone, 5 min IPA

1.8.21. DI water Spin / Rinse / Dry

1.9. Anti-reflection coating layer deposition

1.9.1. PECVD Si_3N_4 deposition for a-Si (GSI PECVD): 100 nm target thickness,

380 ℃ deposition temperature, low reflectance at λ = 850 nm

1.9.2. PECVD Si_3N_4 deposition for Si_3N_4 (GSI PECVD): 50 nm target thickness,

380 ℃ deposition temperature, low reflectance at λ = 850 nm

1.9.3. PECVD SiO_2 deposition for dry oxide (GSI PECVD): 100 nm target,

380 ℃ deposition temperature, low reflectance at λ = 850 nm

1.10. Via – Top

1.10.1. Wafer cleaning: 5 min Acetone, 5 min IPA

1.10.2. DI water Spin / Rinse / Dry

1.10.3. Dehydration bake: 150 ℃, 10 min

1.10.4. HMDS deposition (Yes image reversal oven): 300 s

1.10.5. PR coating (CEE spinner): SPR 7.0, 1000 rpm, 15 μm thick

1.10.6. Soft bake (Hot plate): 85 ℃, 600 s

1.10.7. PR exposure (MA6): 45 s exposure time, hard contact, 30 μm gap

1.10.8. Post exposure delay: 4 hours to finish the photochemical reaction

1.10.9. Post exposure bake (Hot plate): 85 ℃, 600 s

1.10.10. PR development (CEE developer): AZ726, DP 80-80, DP 60-60

1.10.11. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

1.10.12. RIE for dry oxide (LAM9400): 90 s etch time, 120 nm target etch depth, mnf_oxide1 (Recipe)

1.10.13. Wafer cleaning: 5 min Acetone, 5 min IPA

1.10.14. DI water Spin / Rinse / Dry

1.10.15. Sample cleaning (Yes plasma stripper): 100 W, 60 s, 60 ℃, 35 sccm O_2

1.11. Via – Bottom

1.11.1. Wafer cleaning: 5 min Acetone, 5 min IPA

1.11.2. DI water Spin / Rinse / Dry

1.11.3. Dehydration bake: 150 ℃, 10 min

1.11.4. HMDS deposition (Yes image reversal oven): 300 s

1.11.5. PR coating (CEE spinner): SPR 7.0, 1000 rpm, 15 μm thick

1.11.6. Soft bake (Hot plate): 85 ℃, 600 s

1.11.7. PR exposure (MA6): 80 s exposure time, hard contact, 30 μm gap

1.11.8. Post exposure delay: 4 hours to finish the photochemical reaction

1.11.9. Post exposure bake (Hot plate): 85 ℃, 600 s

1.11.10. PR development (CEE developer): AZ726, DP 80-80 x2, DP 60-60

1.11.11. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

1.11.12. RIE (LAM9400): 180 s etch time, 270 nm target etch depth, mnf_oxide1 (Recipe)

1.11.13. Wafer cleaning: 5 min Acetone, 5 min IPA

1.11.14. DI water Spin / Rinse / Dry

1.11.15. Sample cleaning (Yes plasma stripper): 100 W, 60 s, 60 ℃, 35 sccm O_2

1.12. Bonding pad metallization

1.12.1. Wafer cleaning: 5 min Acetone, 5 min IPA

1.12.2. DI water Spin / Rinse / Dry

1.12.3. Aluminum oxide removal: 5 s etch time (Aluminum etchant type A), 30 Å/s etch rate

1.12.4. Aluminum deposition (Enerjet): 1 µm target thickness

1.12.5. HMDS deposition (Yes image reversal oven): 300 s

1.12.6. PR coating (CEE spinner): SPR 7.0, 2000 rpm, 10 µm thick

1.12.7. Soft bake (Hot plate): 85 ℃, 330 s

1.12.8. PR exposure (MA6): 30 s exposure time, hard contact, 30 µm gap

1.12.9. Post exposure delay: 3 hours to finish the photochemical reaction

1.12.10. Post exposure bake (Hot plate): 85 ℃, 90 s

1.12.11. PR development (CEE developer): AZ726, DP 80-80 x2

1.12.12. PR exposure (MA6): 20 s exposure time, hard contact, 30 µm gap

1.12.13. Post exposure bake (Hot plate): 85 ℃, 60 s

1.12.14. PR development (CEE developer): AZ726, DP 80-80, DP 60-60

1.12.15. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

1.12.16. Hard baking (Hot plate): 110 ℃, 300 s

1.12.17. Aluminum etching (Acid 73): 100 Å/s etch rate, 50 ℃,

120 s etch time (20 s over etch)

1.12.18. Wafer cleaning: 5 min Acetone, 5 min IPA

1.12.19. DI water Spin / Rinse / Dry

2. GaAs Photovoltaic cells

2.1. Top contact for p-GaAs

2.1.1. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.1.2. HMDS (Yes plasma stripper): 300 s

2.1.3. PR coating (CEE spinner): SPR 3.0, 4000 rpm, 2.2 um thick,

2.1.4. Soft bake (Hot plate): 115 ℃, 90 s

2.1.5. PR exposure (MJB3): 9 s exposure time, hard contact

2.1.6. Post exposure bake (Hot plate): 115 ℃, 90 s

2.1.7. Image reversal (Yes plasma stripper): 45 min

2.1.8. Flood exposure (MJB3): 12 s exposure time, hard contact

2.1.9. Post exposure bake (Hot plate): 115 ℃, 90 s

2.1.10. PR development (CEE developer): AZ726, DP 40-40

2.1.11. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

2.1.12. Native oxide etch: NH_4OH: DI water = 10 ml : 200 ml, 30 s etch time

2.1.13. Metal deposition (Enerjet): Ti / Pt / Au = 50/100/200 nm

2.1.14. Metal lift-off: 10 min Acetone, 5 min IPA, 5 min DI water

2.2. Selective etch for heavily doped top p-GaAs

2.2.1. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.2.2. HMDS (Yes plasma stripper): 300 s

2.2.3. PR coating (CEE spinner): SPR 3.0, 4000 rpm, 2.2 um thick,

2.2.4. Soft bake (Hot plate): 115 ℃, 90 s

2.2.5. PR exposure (MJB3): 9 s exposure time, hard contact

2.2.6. Post exposure bake (Hot plate): 115 ℃, 90 s

2.2.7. PR development (CEE developer): AZ726, DP 40-40

2.2.8. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

2.2.9. GaAs etch: Citric acid : H_2O_2 : DI water = 30 ml : 10 ml : 1500 ml,

8 – 10 min etch time, Surface color check (Dark blue)

2.2.10. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.3. Device isolation down to n+ layer

2.3.1. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.3.2. HMDS (Yes plasma stripper): 300 s

2.3.3. PR coating (CEE spinner): SPR 3.0, 4000 rpm, 2.2 um thick,

2.3.4. Soft bake (Hot plate): 115 ℃, 90 s

2.3.5. PR exposure (MJB3): 9 s exposure time, hard contact

2.3.6. Post exposure bake (Hot plate): 115 ℃, 90 s

2.3.7. PR development (CEE developer): AZ726, DP 40-40

2.3.8. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

2.3.9. RIE (LAM9400): Cl_2 : BCl_3 : Ar = 20 : 20 : 20 sccm, 4 µm target depth

220 – 270 Å / s etch rate according to exposed area, 180 s etch time

2.3.10. Surface treatment : H_3PO_4 : H_2O_2 : DI water = 60 : 20 : 1000 ml,

10 s etch time

2.3.11. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.3.12. Plasma cleaning (Yes plasma stripper): 800 W, 120 s, 150 ℃, 80 sccm O_2

2.4. Bottom contact metallization – n-GaAs

2.4.1. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.4.2. HMDS (Yes plasma stripper): 300 s

2.4.3. PR coating (CEE spinner): SPR 3.0, 4000 rpm, 2.2 um thick,

2.4.4. Soft bake (Hot plate): 115 ℃, 90 s

2.4.5. PR exposure (MJB3): 9 s exposure time, hard contact

2.4.6. Post exposure bake (Hot plate): 115 ℃, 90 s

2.4.7. Image reversal (Yes plasma stripper): 45 min

2.4.8. Flood exposure (MJB3): 16 s exposure time, hard contact

2.4.9. Post exposure bake (Hot plate): 115 ℃, 90 s

2.4.10. PR development (CEE developer): AZ726, DP 40-40

2.4.11. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

2.4.12. Native oxide etch: NH_4OH: DI water = 10 ml : 200 ml, 30 s etch time

2.4.13. Metal deposition (Enerjet): Ni/Ge/Au/Ti/Pt/Au = 5/30/100/50/100/200 nm

2.4.14. Metal lift-off: 10 min Acetone, 5 min IPA, 5 min DI water

2.5. Device isolation down to n+ layer

2.5.1. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.5.2. HMDS (Yes plasma stripper): 300 s

2.5.3. PR coating (CEE spinner): SPR 3.0, 4000 rpm, 2.2 um thick,

2.5.4. Soft bake (Hot plate): 115 ℃, 90 s

2.5.5. PR exposure (MJB3): 14 s exposure time, hard contact

2.5.6. Post exposure bake (Hot plate): 115 ℃, 90 s

2.5.7. PR development (CEE developer): AZ726, DP 40-40

2.5.8. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

2.5.9. RIE (LAM9400): Cl_2 : BCl_3 : Ar = 20 : 20 : 20 sccm, 5.7 μm target depth

220 – 270 Å / s etch rate according to exposed area, 180 s etch time

2.5.10. Surface treatment : H_3PO_4 : H_2O_2 : DI water = 60 : 20 : 1000 ml,

10 s etch time

2.5.11. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.5.12. Plasma cleaning (Yes plasma stripper): 800 W, 120 s, 150 ℃, 80 sccm O_2

2.6. Ammonium sulfide ($(NH4)_2S$) treatment for sidewall/surface passivation

2.6.1. Ammonium sulfide ($(NH4)_2S$): 23 %, 10 min treatment

2.6.2. DI water clean

2.7. PECVD Silicon nitride deposition for AR coating and passivation

2.7.1. PECVD Si_3N_4 deposition (GSI PECVD): 100 nm target thickness,

380 ℃ deposition temperature, low reflectance at λ = 850 nm

2.8. Via – Top and bottom pads

2.8.1. Wafer cleaning: 5 min Acetone, 5 min IPA. 5 min DI water

2.8.2. HMDS deposition (Yes image reversal oven): 300 s

2.8.3. PR coating (CEE spinner): SPR 3.0, 4000 rpm, 2.2 um thick,

2.8.4. Soft bake (Hot plate): 115 ℃, 90 s

2.8.5. PR exposure (MJB3): 14 s exposure time, hard contact

2.8.6. Post exposure bake (Hot plate): 115 ℃, 90 s

2.8.7. PR development (CEE developer): AZ726, DP 40-40

2.8.8. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

2.8.9. RIE (LAM9400): mnf_oxide1 (Recipe), 120 s etch time, 180 nm target

2.8.10. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.8.11. Plasma cleaning (Yes plasma stripper): 800 W, 120 s, 150 ℃, 80 sccm O_2

2.9. Bonding pad metallization

2.9.1. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.9.2. HMDS (Yes plasma stripper): 300 s

2.9.3. PR coating (CEE spinner): SPR 3.0, 4000 rpm, 2.2 um thick,

2.9.4. Soft bake (Hot plate): 115 ℃, 90 s

2.9.5. PR exposure (MJB3): 14 s exposure time, hard contact

2.9.6. Post exposure bake (Hot plate): 115 ℃, 90 s

2.9.7. Image reversal (Yes plasma stripper): 45 min

2.9.8. Flood exposure (MJB3): 16 s exposure time, hard contact

2.9.9. Post exposure bake (Hot plate): 115 ℃, 90 s

2.9.10. PR development (CEE developer): AZ726, DP 40-40

2.9.11. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

2.9.12. Metal deposition (Enerjet): Ti/Al/Ti/Au = 10/7000/10/300 nm

2.9.13. Metal lift-off: 10 min Acetone, 5 min IPA, 5 min DI water

2.10. Bottom contact metallization – n-GaAs

2.10.1. Wafer cleaning: 5 min Acetone, 5 min IPA, 5 min DI water

2.10.2. Dehydration bake (Hot plate): 115 ℃, 60 s

2.10.3. PR coating (CEE spinner): LOR 10B, 4000 rpm, 0.9 um thick,

2.10.4. Soft bake (Hot plate): 165 ℃, 180 s

2.10.5. PR exposure (MJB3): 14 s exposure time, hard contact

2.10.6. Post exposure bake (Hot plate): 115 ℃, 90 s

2.10.7. PR development (CEE developer): AZ726, DP 40-40

2.10.8. Plasma ashing (Yes plasma stripper): 100 W, 60 s, 35 sccm O_2

2.10.9. Metal deposition (Enerjet): Ti/Au = 10/500 nm

2.10.10. Metal lift-off: 20 min Remover PG at 65 ℃, 10 min IPA, 5 min DI water

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