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Quad-bus motor drive system for electrified vehicles based on a dual-output–single-inductor structure

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Abstract: 48 V electric system architecture has been recently introduced to accommodate an increasing number of electric components in mild hybrid electric vehicles. In this study, two additional DC buses are added for electric machines including 36 and 24 V AC- and DC-motor/actuator loads, in a 48/12 V power supply system. This structure can yield significant benefits, especially for electrified vehicles that have more electric machines and actuators. A single-inductor multi-output structure is employed, with a control strategy that produces linear transfer functions and is less sensitive to load variation, to accommodate multiple-bus motor/actuator drives. The proposed structure and control strategy can offer options for selecting proper bus voltages, optimising the electric machine's power density. Both simulations and experiments have been performed to verify the system structure and control schemes using 36 and 24 V electric machines connected to the additional dual-output buses on top of the existing 12/48 V bus structure.

1 Introduction

The recent technological innovations in electric and autonomous vehicles require more electric components including more onboard electric motors/actuators. The 48 V power system has recently been introduced by European automobile companies due to the increasing number of electric components in electric vehicles [1, 2]. In this structure, the traditional 12 V net still exists for low-voltage electronic loads along with the 48 V bus [3–6].

The majority of high-power components in 48 V electrified vehicles are electric machines and actuators. Therefore, higher-power density in electric machine drives can contribute to the improvement of a vehicle's fuel economy. For electric machines, a higher voltage can lower motor currents for the same power. The lower currents will decrease the wire thickness and copper losses that can influence the power density of electric machine drives. In this manner, for the motors/actuators, proper voltage/current matching will improve the drive system's power density [7].

For commercial, industrial, and military vehicles (especially for high-compression diesel engine vehicles), the 24 V system has been used [8], and hence an additional 24 V supply can provide a better option for component original equipment manufacturers to employ electric motors in electrified vehicles. The 36 V electric machines have been used for integrated starter–alternator systems [9] in electrified vehicles. The additional 36 V supply can give an option for mid-power actuation systems in electrified vehicles.

In this paper, a dual-output–single-inductor (DOSI) circuit structure is employed to deliver power to the DC output buses (36 and 24 V) from the input (48 V net) to provide additional bus voltages to electric machine loads, enabling four voltage buses (12, 24, 36, and 48 V) to offer four voltage-selection options for electric machines in electrified vehicles.

The DOSI structure has advantages in having fewer circuit elements and conversion stages, which will result in both a lower cost and a more compact size compared with other structures with several independent single-inductor–single-output converters [10–26]. Despite its merits on cost and a simpler structure, the single-inductor–dual-output circuit suffers in handling load variations, especially for highly dynamic loads such as electric motor loads, since the DOSI structure has been typically used for low-power integrated circuits [10–17, 22–24].

In [11], a time-multiplexing control scheme is used to control multi-output DC–DC converters, suppressing cross-regulation problems. However, this approach has a higher inductor current and output voltage ripple along with switching noise under heavy load conditions. Ma *et al.* [12] used freewheel switching scheme to handle heavy and dynamic loads and to decouple the outputs. The additional switch and the current flow during the freewheeling mode will increase the cost and power losses in the converter. In [13], a digital control scheme using separate regulation of common- and differential-mode voltages is proposed. This approach requires an adaptive gain compensation for dynamic loads due to the cross-regulation. In [14], duty ratios are calculated based on the reference current for each current controller. However, this approach has different control bandwidths for the control loops, and hence, one output voltage is influenced by load variations.

A small-signal modelling-based state feedback control approach is developed in [15]. This method is sensitive to variations of the input and converter parameters since the design is performed around a specific operating point.

In [19], a DOSI buck converter's stability is improved based on an analysis of the differences in reference currents, initial inductor current, and input voltage for the peak current-mode control. A hysteresis current loop is applied in [24] to accelerate the response of the loops. Owing to the hysteresis control, the approach has somewhat higher-voltage ripple. To reduce intrinsic output voltage ripples, a fly capacitor is used in [25], and a technique that can automatically switch between pulse-width modulation (PWM) and pulse-skip modulation is utilised in [26].

Many conventional control methods typically derive the transfer function based on steady-state values (of the input and output variables) at a given specific operating point. Therefore, for highly dynamic loads, several operating points along with the circuit parameters and input voltages need to be taken into account.

These control issues limit the application areas of the DOSI structure and make it difficult to apply to highly dynamic electric motor loads. To utilise the DOSI structure with the 12/24/36/48 V configuration for electrified vehicles that have an increasing number of DC and AC motors, a voltage/current regulation strategy that is less sensitive to load variations and has less dependency between the 36 and 24 V bus loads is necessary. In the

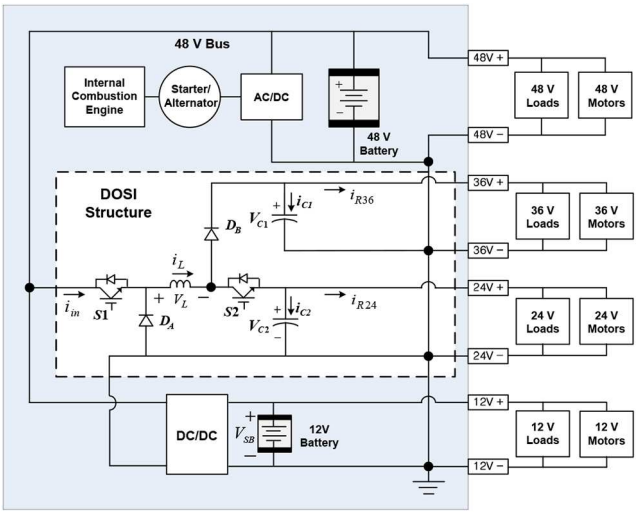

Fig. 1 *Proposed multiple-bus motor drive system structure for 48 V electrified vehicles*

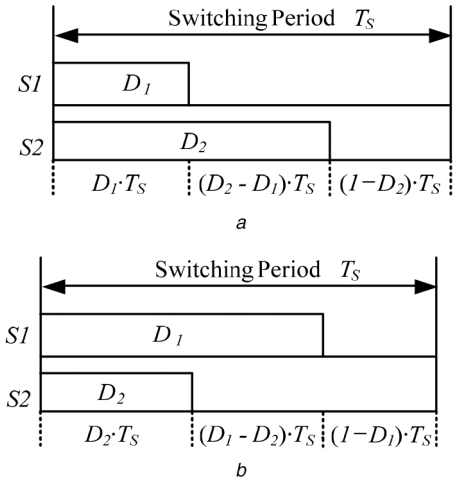

Fig. 2 *Switching statuses for S_1 and S_2*
(a) $D_1 < D_2$ case, ***(b)*** $D_1 > D_2$ case

Table 1 Statuses of V_L, i_{C1}, and i_{C2}

Status		V_L	i_{C1}	i_{C2}
$D_1 < D_2$	$D_1 \cdot T_S$	$V_{in}-V_{C2}$	$-i_{R36}$	i_L-i_{R24}
	$(D_2-D_1)\ T_S$	$-V_{C2}$	$-i_{R36}$	i_L-i_{R24}
	$(1-D_2)\ T_S$	$-V_{C1}$	i_L-i_{R36}	$-i_{R24}$
$D_1 > D_2$	$D_2 \cdot T_S$	$V_{in}-V_{C2}$	$-i_{R36}$	i_L-i_{R24}
	$(D_1-D_2) \cdot T_S$	$V_{in}-V_{C1}$	i_L-i_{R36}	$-i_{R24}$
	$(1-D_1) \cdot T_S$	$-V_{C1}$	i_L-i_{R36}	$-i_{R24}$

proposed approach, the output variables of the 36 and 24 V bus voltage controllers are average capacitor currents, unlike the conventional approaches. On the basis of the average capacitor current commands and the measured 36 and 24 V bus load currents, an inductor current command is formulated. In this way, the transfer functions of the 36 and 24 V are linearised to avoid controller gain compensation at different operating points. Owing to the linear transfer functions of the 36 and 24 V voltage control loops, the system is less sensitive to operating-point variation when utilising it for highly dynamic electric machine drives.

To validate the DOSI circuit configuration and control in the quad-bus power supply system, several brushed DC and brushless permanent-magnet (PM) AC-motor drives are loaded through the two additional output buses (24 and 36 V) in the system. A simulation study using the PSIM package is done first, and then experiments based on a prototype including the Texas Instruments F28335 microprocessor are performed to validate the proposed circuit configuration and control schemes.

2 Proposed approach

2.1 Multiple-bus motor drive system in the quad-bus power supply structure

Fig. 1 presents the multiple-bus motor drive system configuration based on the DOSI circuit for 48 V-powered automobiles. Owing to the cost and weight, an isolated structure with a transformer has not been considered in this vehicle application. Additional output buses (36 and 24 V) along with the existing 48 and 12 V buses can offer better voltage/current matching and flexibility to improve the power density of electric motors [7]. In this paper, the primary focus is put on the DOSI structure for 36 and 24 V buses and its control scheme to drive 36 and 24 V electric machines, since 48 and 12 V electric motors and loads are directly connected to a 48 V battery and a 12 V battery. Fig. 2 depicts the duty ratios (D_1, D_2) of switch elements in the DOSI structure to control 36 and 24 V buses. Also, Table 1 summarises the voltages of the main inductor and the two capacitor currents (i_{C1}, i_{C2}). The voltage drops of switches and diodes and line resistors are ignored for simplification. On the basis of Table 1, an average inductor voltage $\bar{V}_L$ is derived as

$$(D_1 < D_2 \text{ case})\ \bar{V}_L = D_1 (V_{in} - V_{C2}) + (D_2 - D_1) \cdot (-V_{C2}) + (1 - D_2)(-V_{C1}) \quad (1)$$

$$(D_1 > D_2 \text{ case})\ \overline{V_L} = D_2 (V_{in} - V_{C2}) + (D_1 - D_2) \cdot (V_{in} - V_{C1}) + (1 - D_1)(-V_{C1}) \quad (2)$$

For both cases, the duty ratio D_1 is derived as

$$D_1 = \frac{\overline{V_L} + (1 - D_2) V_{C1} + D_2 V_{C2}}{V_{in}} \quad (3)$$

During a steady state, the average inductor voltage ($\overline{V_L}$) in (3) will be zero.

The average current of capacitor 1 (I_{C1}) is obtained in Table 1 as in cases (1) and (2). Then, the following equation is derived:

$$1 - D_2 = \frac{I_{C1} + I_{R36}}{I_L} \Rightarrow I_L = \frac{I_{C1} + I_{R36}}{1 - D_2}. \quad (4)$$

where I_L and I_{R36} are the average currents of the main inductor and 36 V load during a switching cycle period.

Similarly, the average current of capacitor 2 (I_{C2}) is derived for both the $D_1 < D_2$ and $D_1 > D_2$ cases as

$$D_2 = \frac{I_{C2} + I_{R24}}{I_L}. \quad (5)$$

Substituting (5) into (4), the following inductor current command can be formulated:

$$I_L^* = I_{C1}^* + I_{R36} + I_{C2}^* + I_{R24}. \quad (6)$$

As shown in (6), the average inductor current command (I_L^*) can be obtained based on I_{C1}^* and I_{C2}^* (capacitor current commands), which are determined from the V_{C1} and V_{C2} voltage controllers and the load currents (I_{R36}, I_{R24}), as shown in Fig. 3. In the proposed approach, the voltage controller outputs are capacitor current commands (I_{C1}^*, I_{C2}^*) instead of an inductor current command to obtain a linear transfer function for the voltage control loop; hence, linearisation at a specific operating point is not necessary. This is an important step in using the DOSI structure for dynamic motor drives. Then, substituting both (4) and (5) into (3), the required duty ratio D_1^* is derived as

$$D_1^* = \frac{V_L^* + ((I_{C1}^* + I_{R36})/I_L^*)\,V_{C1} + ((I_{C2}^* + I_{R24})/I_L^*)\,V_{C2}}{V_{in}} \quad (7)$$

For the required duty ratio D_2^*, an equation is formulated based on (5) using the inductor and capacitor current commands, as shown in Fig. 3. According to (1)–(7), the control structures of 36 and 24 V buses are created and presented in Fig. 3.

For the voltage control loop, both proportional integral (PI) and integral proportional (IP) voltage controllers can be applied. In this paper, an IP voltage controller is used based on the claims in [27, 28] to reduce overshoot and improve step responses. A step-response comparison is provided in Section 3.

Fig. 4 presents the 36 V bus capacitor voltage control loop to derive a transfer function. As aforementioned, the bus voltages are regulated based on the currents of the output capacitors instead of on the main inductor current to yield a linear transfer function. Therefore, the 36 and 24 V bus voltage controllers make them not directly related to each other and less sensitive to load variations.

The 36 V bus voltage control loop's transfer function is exemplified based on Fig. 4 as below:

$$\frac{V_{C1}}{V_{C1}^*} = \frac{K_{p1}K_{i1}/C_1}{S^2 + (K_{p1}/C_1)S + ((K_{p1}K_{i1})/C_1)}. \quad (8)$$

Then, the gain K_{p1} and K_{i1} are calculated based on the damping ratio ζ and natural frequency ω_n as

$$K_{p1} = 2\,C_1\,\zeta\,\omega_n \quad (9)$$

$$K_{i1} = C_1\,\omega_n^2/K_{P1}. \quad (10)$$

2.2 Discontinuous conduction mode (DCM) analysis

The control strategies in Section 2.1 are based on an assumption that the circuit is operating under continuous conduction mode (CCM). The conditions for CCM operation can be obtained based on Fig. 5 and Table 1.

At a critical condition shown in Fig. 5, the peak inductor current is calculated by the inductor voltage shown in Table 1

$$i_{LA} = \frac{1}{L}V_L D_1 T_S = \frac{1}{L f_S}(V_{in} - V_{C2})\,D_1 \quad (11)$$

During the interval $(D_2–D_1)T_S$, the current variation Δi_{L_AB} can be derived. Then, i_{LB} will be obtained as

$$i_{LB} = i_{LA} - \Delta i_{L\_AB} = \frac{V_{in}D_1 - V_{C2}D_2}{L f_S}. \quad (12)$$

The average load current of the 36 V bus I_{R36} is derived as well at the border of continuous–discontinuous conduction based on Fig. 5

$$I_{R36\_Crit} = \frac{1}{2}i_{LB}(1 - D_2) = \frac{V_{in}D_1 - V_{C2}D_2}{\delta}(1 - D_2) \quad (13)$$

where $\delta = 2\,L\,f_S$. Recognising that the load resistance of the 36 V bus is $R_{36} = V_{C1}/I_{R36}$, the critical value of the 36 V bus load resistance is derived using the steady-state V_{C1} voltage (V_{C1_SS}) based on (4)

$$V_{C1\_SS} = \frac{V_{in}D_1 - V_{C2}D_2}{(1 - D_2)}. \quad (14)$$

$$R_{R36\_Crit} = \frac{V_{C1\_SS}}{I_{R36\_Crit}} = \frac{\delta}{(1 - D_2)^2}. \quad (15)$$

Fig. 6 presents the current waveforms under DCM.

In the DOSI converter, i_{in} equals i_L during on the interval of the $S1$ switch; otherwise, it is zero, as depicted in Fig. 6. Therefore, the average input current $I_{in}$is formulated based on (11) and Fig. 6

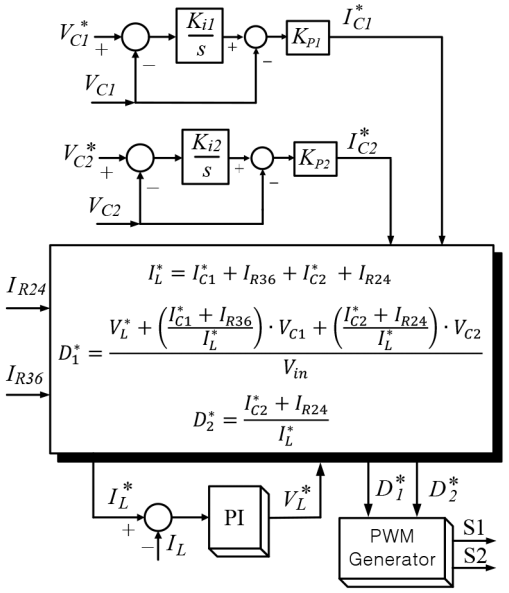

Fig. 3 *Control strategy of the multi-bus motor drive system*

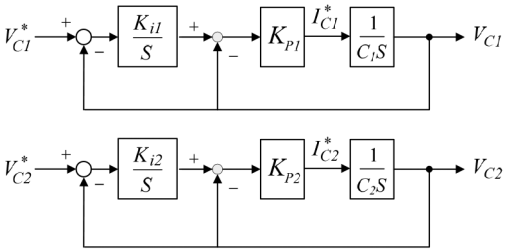

Fig. 4 *Voltage control loops for the 36 and 24 V buses*

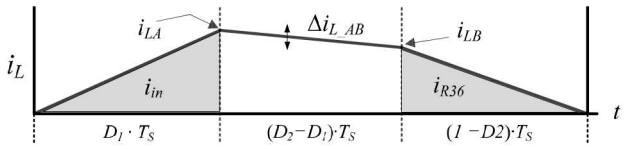

Fig. 5 *Inductor current waveform at a critical condition*

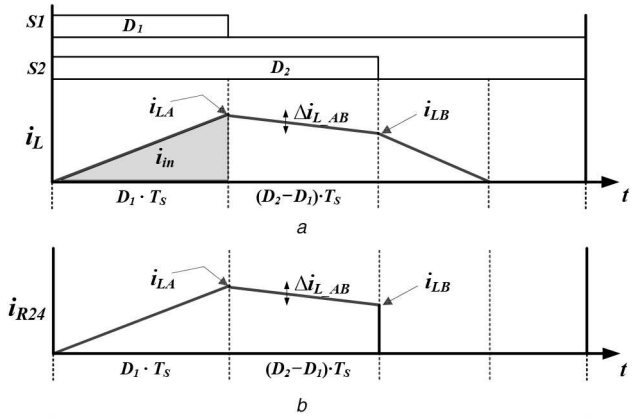

Fig. 6 *Inductor and load currents in DCM*
(a) Inductor current (i_L) waveform in DCM, ***(b)*** 24 V bus load current (i_{R24}) waveform in DCM

$$I_{in} = \frac{(V_{in} - V_{C2})\,D_1^2}{2\,L\,f_s} = \frac{(V_{in} - V_{C2})\,D_1^2}{\delta}. \quad (16)$$

Equating the average input power (P_{in}) to the output power (P_O), ignoring power losses, the output voltage (36 V bus side) can be derived under DCM

$$V_{\text{in}} \cdot \frac{(V_{\text{in}} - V_{C2})\, D_1^2}{\delta} = \frac{V_{C1}^2}{R_{36}} + \frac{V_{C2}^2}{R_{24}} \tag{17}$$

Then, based on Fig. 6*b*, the average load current of the 24 V bus I_{R24} is obtained as

$$I_{R24} = \frac{\left(V_{\text{in}} D_1^2 + 2\, V_{\text{in}} D_1 D_2 - 2\, V_{\text{in}} D_1^2 - V_{C2} D_2^2\right)}{\delta}. \tag{18}$$

Recognising $I_{R24} = V_{C2}/R_{24}$, and substituting (18) into (17) to solve for V_{C1}

$$V_{C1} = \sqrt{\frac{R_{36}}{\delta}}\,(V_{\text{in}} D_1 - V_{C2} D_2). \tag{19}$$

Fig. 7*a* presents the V_{C1} voltage variation as a function of D_1, D_2, and R_{36} under DCM. Fig. 7*b* shows a combined graph of the V_{C1} voltages at the critical condition, i.e. the boundary condition based on (15) using R_{36_Crit}, and at the DCM.

This DCM analysis has been performed to analyse the boundary conditions of the 24 V/36 V voltage control. A control strategy in DCM will be the future work and lies beyond the scope of this paper.

3 Simulation study and experimental verification

On the basis of the DOSI circuit and control schemes depicted in Fig. 3, simulations and experiments are performed. For the simulation study and experiments, the parameters shown in Tables 2 and 3 below are used for the DOSI circuit and load motors. For the simulations and experiments, it is assumed that the circuit is operating under CCM. To observe basic controller performance, the system is tested with resistive loads first.

Initially, a simulation is performed connecting resistive loads to the 36 and 24 V outputs, and the result is presented in Fig. 8. The voltage command of the 36 V bus is sequentially changed (24 V→36 V→24 V→36 V). Similarly, the 24 V bus voltage command is changed as well (12 V→24 V→12 V→24 V).

As presented in Fig. 8, decent step voltage responses have been observed. Fig. 9 indicates the output voltage response with lower capacitance values (the switching frequency is 10 kHz). The capacitance values (C_1 and C_2) are decreased from 470 to 100 µF to observe the controller response under a sudden load change (36 V bus load: 24–12 Ω; 24 V bus load: 18–9 Ω) at 0.3 s. As shown in Fig. 9, a lower capacitance value will increase the output voltage perturbation during the transient under the load change. However, the change does not significantly influence the stability of the controller (down to 100 µF).

Fig. 10 presents the influence of the equivalent series resistance (ESR) in the capacitors on the controller response (from 0 to 0.4 Ω). The higher ESR value increases the output voltage ripple but does not significantly influence the stability of the controller (tested up to 0.9 Ω).

Fig. 11 presents a step-response comparison between the IP and PI voltage controllers. Slightly less overshoot is observed with the IP controller (same damping ratio and natural frequency are used for both controllers).

As a next step, 24 and 36 V DC motors are connected to the DC buses accordingly. Fig. 12 presents the system response when 24 and 36 V DC motors are directly connected to the buses sequentially, without a speed controller, using only a single switch to create a sudden load change. A PWM controller is not used for this test to create a dynamic load change with a large motor-starting current. The inductor current i_L exposes the system response of the DC-motor on/off test, as shown in Fig. 12.

A 36 V DC motor is turned on first (connected to the 36 V bus), followed by a 24 V DC motor being turned on. The 36 and 24 V bus voltage responses indicate that the proposed control structure can handle the load change reasonably well.

To test the system with AC-motor loads, three-phase PMSM machines are loaded through the 24 and 36 V buses with three-phase inverters. As presented in Fig. 13, two PM synchronous motors (PMSMs) are operating at different speeds. The 36 V PMSM is running at a steady-state speed of 1000 rpm, whereas the 24 V PMSM's steady-state speed is 500 rpm. The two output bus voltages are well-regulated at the given commanded values, supplying power to the two PMSMs. For the two PMSMs, a

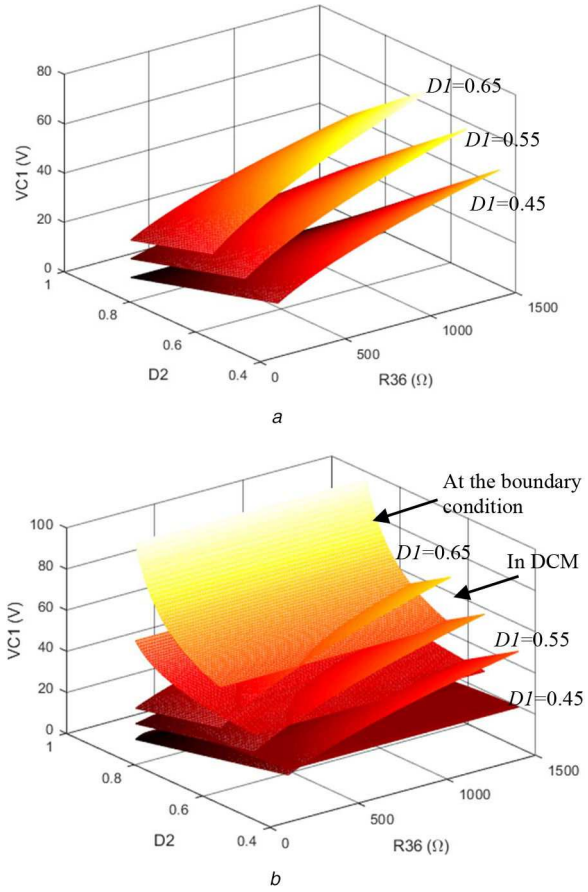

Fig. 7 *V_{C1} in DCM and critical conditions at the border of continuous–discontinuous conductions*
(a) V_{C1} voltage in DCM, ***(b)*** Combined mesh plot of V_{C1} voltages in DCM and at the border of continuous–discontinuous conditions

Table 2 DOSI converter circuit parameters

Parameters	Value
inductance (L)	2 mH
capacitance (C_1, C_2)	470 µF
input voltage (V_{in})	48 V
switch voltage (max V_{DS})	100 V
switch continuous current (max)	28 A
switching frequency	20 kHz

Table 3 Motor parameters

Parameters	Value
24 V PMSM motor rated speed	4000 r/min
24 V PMSM rated current	5.21 A
24 V PMSM peak torque	0.96 Nm
36 V PMSM motor rated speed	4000 r/min
36 V PMSM rated current	5 A
24 V DC-motor rated speed	2000 rpm
24 V DC-motor rated current	2 A
36 V DC-motor rated speed	2000 r/min
36 V DC-motor rated current	5 A

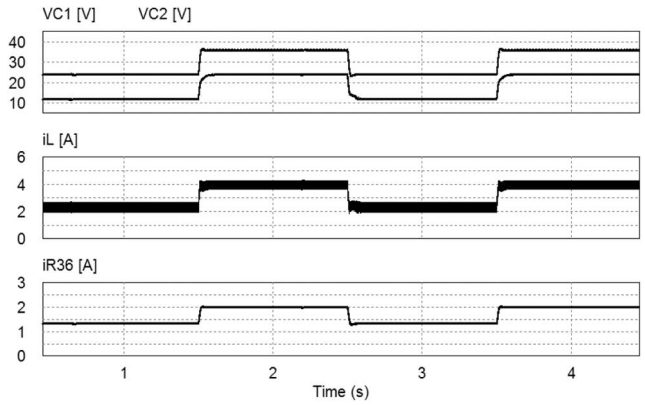

Fig. 8 *Simulation results: step voltage response with resistive loads. Top to bottom: V_{C1} and V_{C2} voltages, inductor current (i_L), and 36 V bus (i_{R36}) load current*

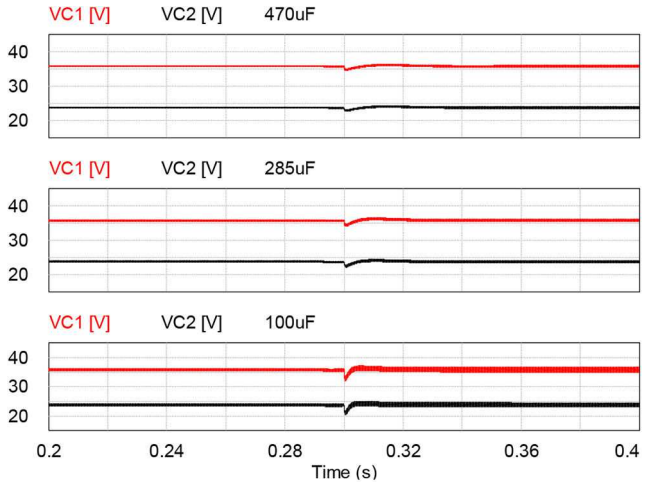

Fig. 9 *Output voltage response with lower capacitance values (top: 470 μF; middle: 285 μF; and bottom: 100 μF)*

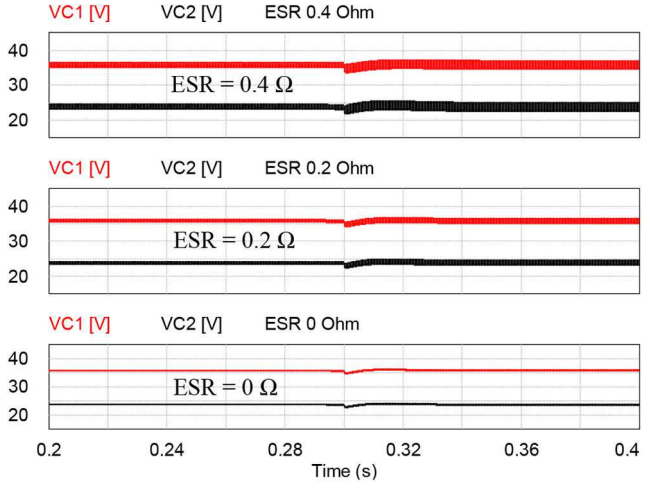

Fig. 10 *Output voltage response with different ESR values in the capacitors C_1 and C_2*

standard field-oriented control, reported in [29], has been adapted to regulate the PMSMs' torque and speed.

Fig. 14 presents additional simulation results, changing the PMSMs' loads to further observe the control performance. Both the 24 and 36 V motor loads have been sharply changed from a 25 to 60% load at 1.5 s. As presented in Fig. 14, the output voltage controller can maintain the bus voltage reasonably well without significant voltage ripples.

To validate the circuit structure and control strategy experimentally, a test bed using the Texas Instruments F28335

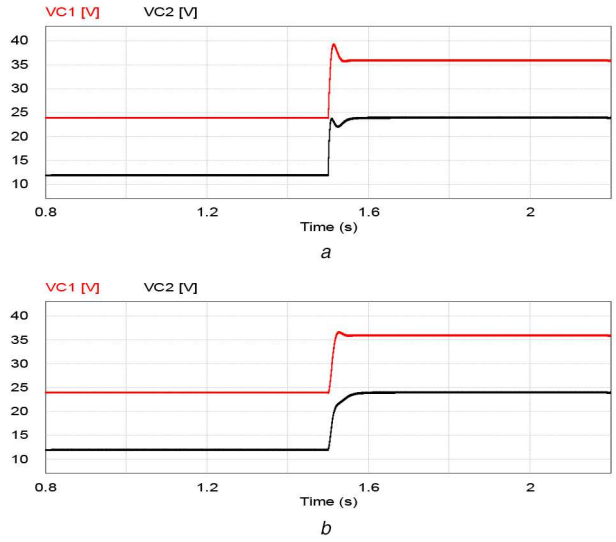

Fig. 11 *Step-response comparison with IP and PI voltage controllers (same damping ratio and natural frequency are used)*
(a) With a PI voltage controller, ***(b)*** With an IP voltage controller

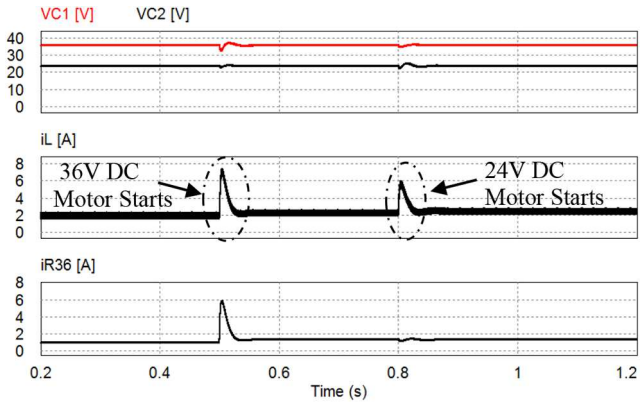

Fig. 12 *Simulation result: DC-motor-load test. Top to bottom: V_{C1} and V_{C2} voltages, inductor current (i_L), and 36 V bus (i_{R36}) load current*

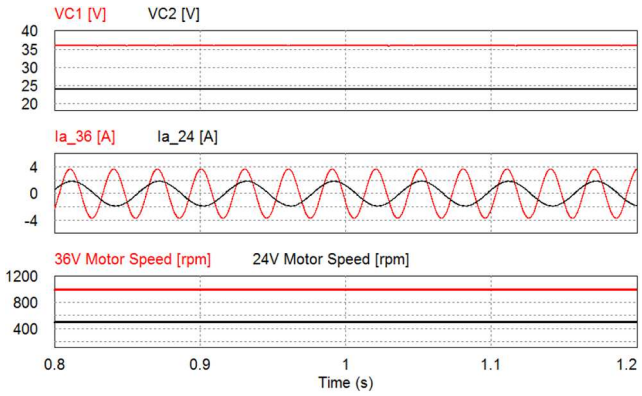

Fig. 13 *Simulation results with two PMSM drives at a steady state. Top to bottom: V_{C1} and V_{C2} voltages, phase A currents of the 36 and 24 V PMSMs, and motor speeds of the 36 and 24 V PMSMs*

microprocessor is built. Fig. 15 presents experimental results of the 36 and 24 V step voltage responses (the control frequency is 10 kHz). The voltage command is step changed both for the 36 V bus (0 V→36 V→24 V→36 V) and the 24 V bus (0 V→24 V→12 V→24 V).

Then, a step load change test is performed on the 36 V bus. Fig. 16 shows experimental results under the 36 V load change (20 Ω→10 Ω→20 Ω). As observed in Fig. 16, the influence on the control of the two bus voltages is not significant.

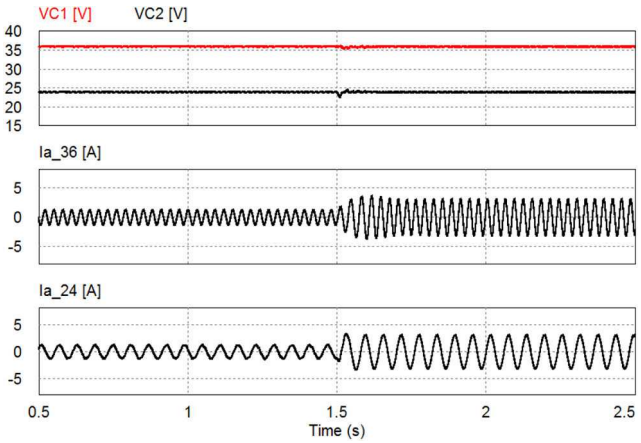

Fig. 14 *Simulation result: response under a sudden motor-load change. Top to bottom: V_{C1} and V_{C2} voltages, phase A current of the 36 V PMSM, and phase A current of the 24 V PMSM*

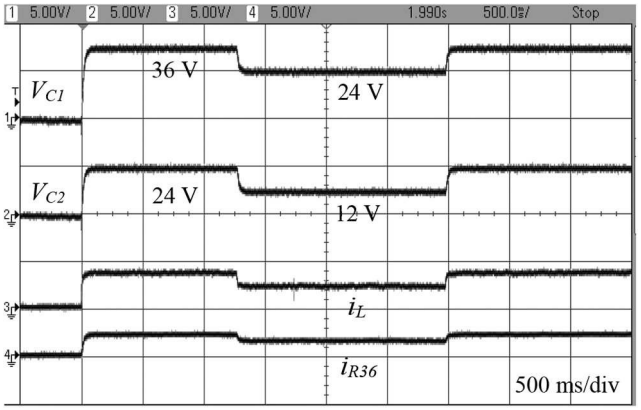

Fig. 15 *Experimental results: step voltage response. Top to bottom: V_{C1} and V_{C2} [24 V/div], i_L [5 A/div], and i_{R36} [4 A/div]*

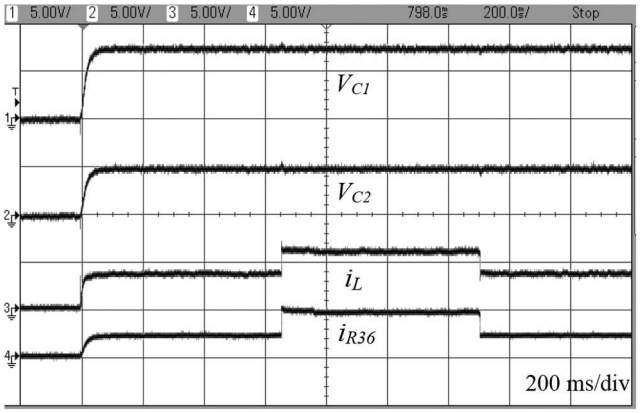

Fig. 16 *Experimental results: system response under a sudden load change. Top to bottom: V_{C1} and V_{C2} [24 V/div], i_L [5 A/div], and i_{R36} [4 A/div]*

As a next step, DC motors are connected to the 36 and 24 V buses. The current spike due to the starting of the 36 and 24 V DC motors causes voltage perturbations, as shown in Fig. 17. However, the proposed control structure can compensate for the perturbation within a reasonable transient period.

To further verify the validity of the system, AC-motor (PMSM) loads are connected to the 36 and 24 V buses. The standard sensorless vector control approach in [29] is used to regulate the speeds and torques of the two PMSMs. For the PMSMs, six switches (silicon metal–oxide–semiconductor field-effect transistor) inverters are used with 20 kHz switching frequency.

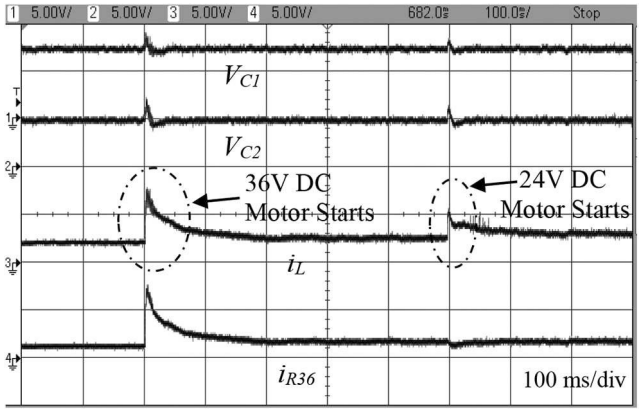

Fig. 17 *Experimental results: system response with two DC-motor loads. Top to bottom: V_{C1} and V_{C2} [24 V/div], i_L [5 A/div], and i_{R36} [4 A/div]*

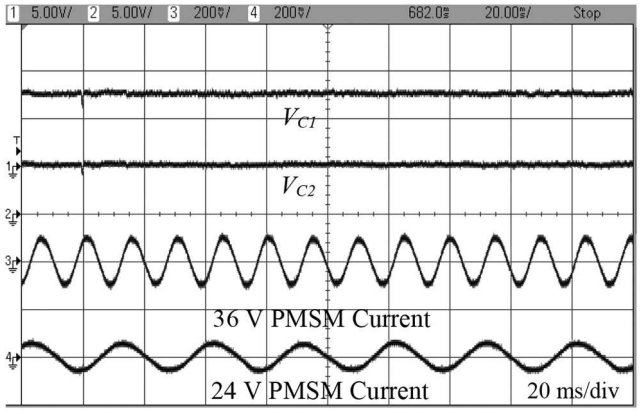

Fig. 18 *Experimental results: system response with two permanent magnet alternating current motor loads. Top to bottom: V_{C1} and V_{C2} [24 V/div], 36 V PMSM current (phase A) [4 A/div], and 24 V PMSM current (phase A) [4 A/div]*

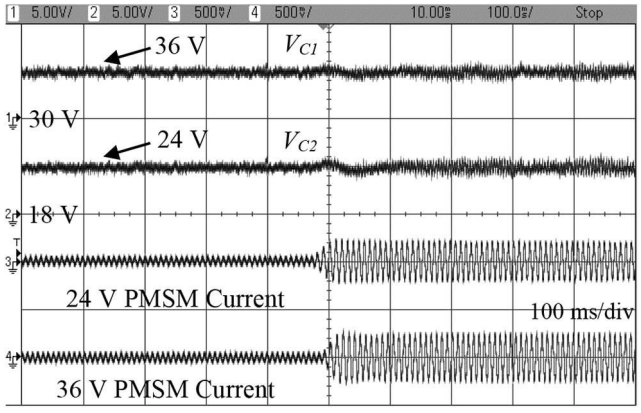

Fig. 19 *Experimental results: system response under sudden motor-load changes at 1800 rpm. Top to bottom: V_{C1} and V_{C2} [6 V/div], 24 V PMSM current (phase A) [10 A/div], and 36 V PMSM current (phase A) [10 A/div]*

Fig. 18 shows the system response at a steady-state speed when the 36 V bus-side motor is operating at 1000 rpm and the 24 V bus-side PMSM is at 500 rpm.

The system response under sudden motor-load changes (25–70%) is also presented in Fig. 19. The PMSM motors are coupled to DC machine loads. The resistors connected to the load DC motors are changed to create a sudden load change. As shown in Fig. 19, voltage perturbations of <15% of the regulated output voltages are observed.

Fig. 20 shows the system response when the PMSM motor speed changes from 0 to 1500 rpm (both 24 and 36 V PMSMs accelerate). Under this setting, the motor starting and acceleration (position sensorless drive) are smooth, without significant voltage

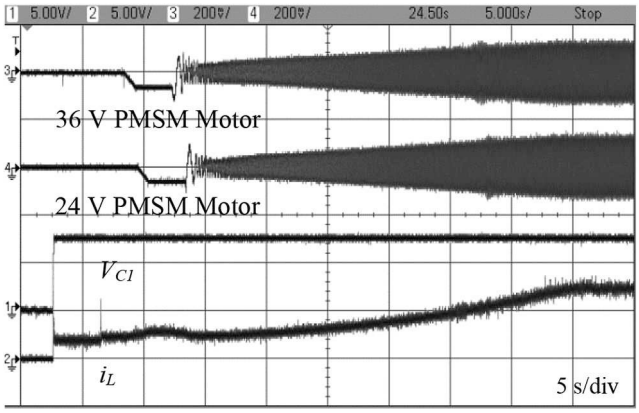

Fig. 20 *Experimental results: PMSM motor speed change (acceleration from 0 to 1500 rpm). Top to bottom: 36 V PMSM current (phase A) [4 A/div], 24 V PMSM current (phase A) [4 A/div], V_{C1} [24 V/div], and i_L [5 A/div]*

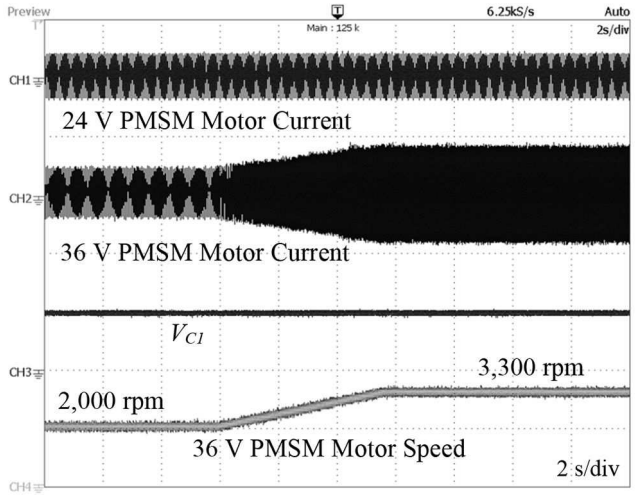

Fig. 21 *Experimental results: PMSM motor speed change (acceleration from 2000 to 3300 rpm). Top to bottom: 24 V PMSM current (phase A) [5 A/div], 36 V PMSM current (phase A) [5 A/div], V_{C1} [36 V/div], and 36 V PMSM motor speed [2000 rpm/div]*

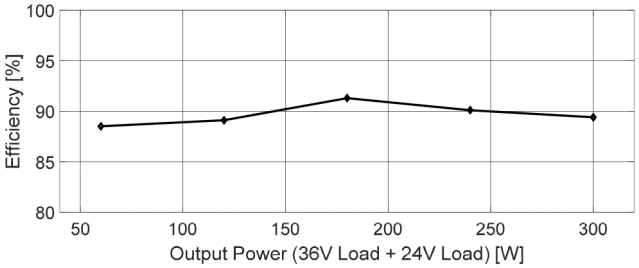

Fig. 22 *Measured efficiency curve of the prototype DOSI system*

perturbations in the two output buses. Also, Fig. 21 presents the system response when the 36 V PMSM speed changes from 2000 to 3300 rpm.

As presented in the experimental results (Figs. 17–21), two bus voltages are maintained adequately well under DC- and AC-motor loads.

Fig. 22 indicates the measured efficiency of the DOSI system based on the proposed approach. The peak efficiency is 91.7%, which is similar to [20, 21] (91.3, 92%), a little higher than [22–25] (91, 89, 88, and 87%), and a little lower than [26] (93.5%). The feasibility of the multi-bus motor drive system and control method has been validated experimentally, as presented in Figs. 15–21. The control method proposed in this paper can maintain the DC-bus voltages under load variations with acceptable perturbations and overshoots.

4 Conclusion

A multiple-bus motor drive system based on a quad-bus power supply with a DOSI structure has been proposed for 48 V electrified vehicles. A control structure has been introduced to regulate both 24 and 36 V buses connected to dynamic motor loads in the DOSI structure. The 12/24/36/48 V buses proposed in this paper can provide a better voltage/current match for electric motors to improve their power density and will offer additional voltage-selection options. This quad-bus structure can benefit electrified vehicles that require more electric machines with a variety of power ratings. The proposed DOSI converter structure and control scheme have been validated both by simulations and experiments.

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