

Efficient coding schemes for low-rate wireless personal area networks

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Abstract: The emerging market of Internet of things has created great demand for low-cost, low-power wireless technologies. Existing IEEE 802.15.4 standard is designed for low-rate wireless personal area networks (LR-WPANs). However, current standard does not fully utilise the benefit of the code redundancy. In this study, the authors propose new coding schemes for LR-WPANs with improved coding gain. They first propose a block code based on extended Bose–Chaudhuri–Hocquenghem (BCH) code that increases the minimum Hamming distance compared with the existing code used in LR-WPANs. The computational complexity of the encoder and decoder remains about the same. In addition, by applying the extended BCH code directly to LR-WPANs, the data rate of the system can be increased without sacrificing coding performance. They further propose a tail-biting convolutional (TBC) code with optimum generator polynomials for LR-WPANs. The proposed TBC code enjoys significant performance improvement while preserving the effective code rate as well as a low decoding complexity. Simulation results validate the effectiveness of the proposed coding schemes.

1 Introduction

As the Internet of things (IoT) attracts more and more attention recently, low-cost and low-power wireless communications become essential to provide ubiquitous connectivity [1]. Constant-envelope modulation technique and low-rate (LR) coding schemes are adopted to improve power efficiency and system performance of LR wireless personal area networks (LR-WPANs) at different frequency bands. Among all wireless standards, IEEE 802.15.4 standard plays an important role in IoT for LR-WPANs. The 2.4 GHz physical layer (PHY) in IEEE 802.15.4 standard supports an over-the-air data rate of 250 kb/s. Direct sequence spread spectrum (DSSS) is applied to improve system performance and the chip rate is 2 Mb/s. The signals are then modulated by offset quadrature phase shift keying (OQPSK) with half-sine pulse shaping filter [2]. Since this modulation is identical to minimum shift keying (MSK) modulation, the transmitted signals have constant envelope. Such a transmitter has advantage in adopting non-linear power amplifiers and achieving high-power efficiency.

Conventional approaches apply differential detection to detect MSK signals. The performance of such detection schemes is not satisfactory [3–7]. The coherent detection achieves good performance. However, it is sensitive to initial phase error or frequency offset. Dai *et al.* [8] proposed a robust detector, which provides satisfactory performance with only 1 dB loss compared with the coherent detector in additive white Gaussian noise (AWGN) channel.

In addition to improve the performance of demodulation schemes, the overall system performance can be further improved by fully utilising the benefit of the code redundancy. For example, DSSS in IEEE 802.15.4 standard is not simple spreading. It provides coding gain in addition to spreading gain. The symbol-to-chip

mapping can be viewed as a (32, 4) block code. The minimum Hamming distance of this code is 12. The coding gain is ~2 dB at packet error rate (PER) of 1% [9].

From channel coding perspective, the coding scheme provided in current standard is not optimal. For general block codes, Griesmer [10] suggested an upper bound of minimum Hamming distance of the codes. The minimum Hamming distance must be ≤ 16 for a (32,4) code, suggesting that extra coding gain is possible. For convolutional codes, the bound of free distance listed in [11] limits the system performance. The convolutional codes with maximum free distance can be utilised to improve performance. In a word, there is plenty of room to improve the code efficiency for LR-WPANs.

In this paper, we propose new coding schemes with improved coding gain for LR-WPANs. We propose a block code based on extended Bose–Chaudhuri–Hocquenghem (BCH) code that improves the coding gain. Such benefit is obtained without extra computational complexity. By applying the extended BCH code directly to LR-WPANs, the data rate can be increased without sacrificing the coding performance. To obtain additional coding gain, we further propose a tail-biting convolutional (TBC) code with optimum generator polynomials for LR-WPANs. System performance can be significantly improved.

The rest of this paper is organised as follows. Section 2 provides system setup for LR-WPANs. We take the coding scheme of the 2.4 GHz PHY in IEEE 802.15.4 standard as an example for further discussion. Section 3 proposes new coding schemes based on block codes. The proposed coding scheme based on convolutional codes is presented in Section 4. Simulation results are provided in Section 5 that demonstrates the effectiveness of the proposed coding schemes. Section 6 extends the proposed coding schemes to other LR-WPANs standards. Finally, Section 7 concludes this paper.

2 System setup

In this section, we provide a system setup for LR-WPANs. Fig. 1 shows the transceiver structure of general LR-WPANs. An LR encoder is applied to improve the receive sensitivity. The coded bits are then modulated to transmitted signals. To meet the spectral mask, pulse shaping filter is applied. The digital baseband signals are then transformed to analogue domain by digital-to-analogue converter. For a single-carrier, narrow-band system in the applications of LR-WPANs, AWGN channel is reasonable assumption. At the receiver side, the baseband analogue signals are sampled to digital signals by analogue-to-digital converter. Matched filter is utilised to maximise the signal-to-noise ratio (SNR) of the received signals. After synchronisation, the receiver demodulates and decodes the signals.

Channel coding is essential to improve the system performance in LR-WPANs. In this paper, we take the coding scheme of the 2.4 GHz PHY in IEEE 802.15.4 standard as an example for further discussion. The encoder for IEEE 802.15.4 standard is shown in Fig. 2. The information bits are segmented into symbols every 4 bits. The symbol $\mathbf{u}=(u_0, u_1, u_2, u_3)$ is spread to a 32 bit chip sequence, which is denoted by $\mathbf{c}=(c_0, c_1, \dots, c_{31})$. Table 1 is the symbol-to-chip mapping table in IEEE 802.15.4 standard. OQPSK with half-sine pulse shaping filter is applied. Such modulation is identical to MSK modulation. Since the analogue transmitted signals have constant envelope, power-efficient non-linear power amplifiers can be applied in the transmitter.

The encoder used in the standard is not simple spreading. It provides coding gain. The coding gain for a coded binary OQPSK system can be approximated by [12]

$$\gamma \simeq 10 \log_{10} \left(R_c d_{\min} - \frac{k \ln 2}{E_b/N_0} \right), \quad (1)$$

where k is the length of information bit sequence, n is the length of codewords, d_{\min} is the minimum Hamming distance of the set of codewords, $R_c = k/n$ is the code rate and E_b/N_0 is the SNR per bit. In IEEE 802.15.4 standard, the encoder maps every four information bits to a 32 bit chip sequence. The minimum Hamming distance of the set of codewords is 12. The coding gain is about 2 dB [9]. On the other hand, this set of codewords is not optimised for coding gain.

3 Coding schemes based on linear block codes

Since linear block codes are easy to implement and analyse, and their performances are similar to that of general block codes, we focus on

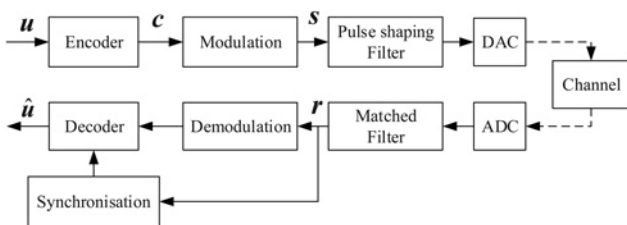


Fig. 1 Transceiver structure of general LR-WPANs

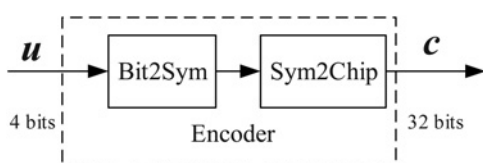


Fig. 2 Encoder of the 2.4 GHz PHY in IEEE 802.15.4 standard

Table 1 Symbol-to-chip mapping table in IEEE 802.15.4 standard

Data symbol (u_0, u_1, u_2, u_3)	Chip values (c_0, c_1, \dots, c_{31})
0000	11011001110000110101001000101110
1000	11101101100111000011010100100010
0100	00101110110110011100001101010010
1100	00100010111011011001110000110101
0010	01010010001011101101100111000011
1010	00110101001000101110110110011100
0110	11000011010100100010111011011001
1110	10011100001101010010001011101101
0001	10001100100101110000011101111011
1001	1011100011001001011000001110111
0101	0111101110001100100101100000111
1101	01110111101110001100100101100000
0011	00000111011110111000110010010110
1011	01100000011101111011100011001001
0111	10010110000001110111101110001100
1111	110010010111000000111011110111000

finding new coding schemes with improved coding gain for LR-WPANs in this section. This paper is equivalent to finding a set of codewords with large minimum Hamming distance. It is known that the Griesmer bound [10], which is effective for codes with low code rate, provides an upper bound of linear block codes. With the Griesmer bound, the minimum Hamming distance d_{\min} of linear block codes is bounded by

$$\sum_{i=0}^{k-1} \left\lceil \frac{d_{\min}}{2^i} \right\rceil \leq n, \quad (2)$$

where ‘ $\lceil \cdot \rceil$ ’ denotes the smallest integer that is larger than or equal to the input. For (32,4) linear block codes, Griesmer bound suggests that $d_{\min} \leq 16$. On the other hand, the bound table in [13] shows that linear block codes with $d_{\min} = 16$ are possible. Our task is to find the codes that achieve the Griesmer bound.

We start the search with some well-studied linear block codes. One of the best-known codes, which are attractive for low-to-moderate block length, is BCH code. From the extensive list of BCH codes, we observe that BCH codes do not support the codeword length $n = 32$. Instead, the (31,6) primitive BCH code provides the largest minimum Hamming distance $d_{\min} = 15$ with codeword length $n = 31$ [12]. From [14], we know that by adding a parity-check bit, the (n, k) binary linear block code with odd minimum Hamming distance d_{\min} can be extended to a new $(n+1, k)$ code. Meanwhile, the minimum Hamming distance of the extended code is also increased by 1. By padding a parity-check bit to the (31,6) BCH code, the codeword length becomes 32 and the minimum Hamming distance of this code increases to 16.

To design a bound-achieving (32,4) block code that is compatible with the 2.4 GHz PHY in IEEE 802.15.4 standard, we choose a subset of the (32,6) extended BCH code corresponding to four independent information bits. A possible way to generate a (32,4) code based on the (32,6) extended BCH code is shown in Fig. 3. The input information bits, which are segmented into blocks of 4 bits, can be expressed as $\mathbf{u}=(u_0, u_1, u_2, u_3)$. In the ‘Bit Pad’ block, \mathbf{u} is extended to \mathbf{u}' by padding two bits. These two bits can be padded in any position of \mathbf{u} . Valid combinations can be $\mathbf{u}'=(u_0, u_1, u_2, u_3, 0, 1)$ or $\mathbf{u}'=(u_0, u_1, u_2, 0, u_3, 1)$. To be complied with the IEEE 802.15.4 standard, we emphasise that the padded bits are not allowed to be all zeros. Since in this case,

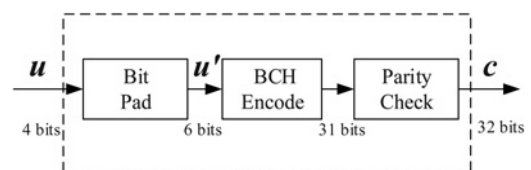


Fig. 3 (32,4) Code based on the (32,6) extended BCH code

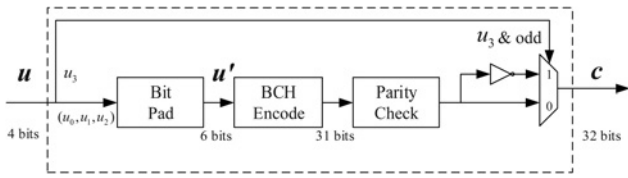


Fig. 4 Proposed (32,4) code based on extended BCH code for LR-WPANs

all-zero or all-one codewords are possible. The mean transmit power may be different from other codewords. In addition, the pattern in all-zero or all-one codewords may interfere with other systems transmitting in the same frequency band. The ‘BCH Encode’ block encodes the 6 bit sequence u' with the corresponding (31,6) BCH code. At last, by adding a parity-check bit to the output of the BCH encoder, we obtain a 32 bit codeword $c = (c_0, c_1, \dots, c_{31})$. The proposed coding scheme can be summarised in Fig. 3.

By studying the codewords of the (32,6) extended BCH code, we observe that half of the 64 codewords are mutual complements of the other half. All chips between two complementary codewords are opposite. Each pair of such codewords has the largest Hamming distance 32 for the (32,6) extended BCH code. The design of encoder and decoder can be further simplified by this property. Fig. 4 shows the updated (32,4) block code. The four information bits $u = (u_0, u_1, u_2, u_3)$ are separated into two parts: (u_0, u_1, u_2) and u_3 . In the ‘Bit Pad’ block, three bits are padded to (u_0, u_1, u_2) . One valid combination is $u' = (u_0, u_1, u_2, u_3 = 0, 0, 1)$. The corresponding BCH code and extended BCH code can be obtained. In this case, only eight codewords are chosen. The bit u_3 is utilised to generate the complementary codewords. When $u_3 = 1$, we first generate the corresponding codeword with $u_3 = 0$. Then, we flip all bits in the codeword to get the complementary codeword with a logic inverter. It is worth noting that these eight codewords are not generated from the BCH encoder and the parity-check bit extension. However, it is easy to show that these eight codewords are valid codewords satisfying the extended BCH code. Table 2 gives one possible symbol-to-chip mapping table of the proposed (32,4) code. The proposed code has a minimum Hamming distance of 16 and performs better than the codewords used in the IEEE 802.15.4 standard.

The performance of the coding schemes for LR-WPANs can be further improved. With a given codeword length n , (1) indicates that the coding gain of block codes increases linearly with respect to the information bit length k when the minimum Hamming distance d_{\min} is the same. Since the (32,6) extended BCH code achieves the same minimum Hamming distance $d_{\min} = 16$ as the proposed (32,4) code, the (32,6) extended BCH code as shown in Fig. 5 can be directly applied in LR-WPANs to provide better coding gain. The information bits are segmented into blocks of 6 bits, which can be defined by $u = (u_0, u_1, u_2, u_3, u_4, u_5)$.

Table 2 Symbol-to-chip mapping table of the proposed (32,4) code based on extended BCH code

Data symbol (u_0, u_1, u_2, u_3)	Chip values (c_0, c_1, \dots, c_{31})
0000	00000110010110111101010001001111
1000	1000010101101100011111001101001000
0100	01000100111000001100101010111011
1100	11000111110011010010000101011100
0010	00100110000011001010111011010101
1010	101001000010101101100011110010
0110	01100101101111010100010011100001
1110	11100110100100001010111011000110
0001	11110011010010000101011011010000
1001	01111010100010011100000110010111
0101	10111011000111110011010010000100
1101	0011100000110010110111010100011
0011	11011000111110011010010000101010
1011	01011011110101000100111000001101
0111	10011010010000101011101100011110
1111	00011001011011110101000100111001

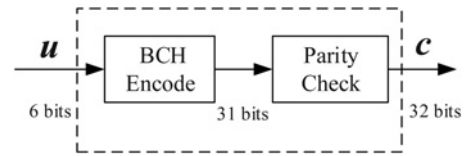


Fig. 5 (32,6) Extended BCH code for LR-WPANs

Similarly, we obtain a 32 bit codeword $c = (c_0, c_1, \dots, c_{31})$ by adding a parity-check bit after the (31,6) BCH encoder. To avoid all-zero or all-one codewords, a whitening block can be applied.

Next, we will discuss the decoder of the proposed coding schemes. In short-range communications such as IEEE 802.15.4, AWGN channel is considered to be the general case [15]. At the receiver side, with perfect synchronisation, the received baseband signal can be represented as

$$r_i = s_i + v_i, \quad (3)$$

where r_i is the received baseband signal at the ideal sampling time, s_i is the i th chip modulated with OQPSK in a 32-chip sequence and v_i is the equivalent AWGN with variance σ^2 . Since the proposed (32,4) code is based on the (32,6) extended BCH code, existing decoding algorithms of BCH codes are available. However, the performance of these hard-decision decoding algorithms is not satisfactory. With a coherent demodulator for the OQPSK system [8], the information is only contained in one branch and the noise in the other branch can be completely ignored. The i th chip in a symbol for coherent demodulator can be described as

$$r'_i = \begin{cases} \text{Re}\{r_i\} = s'_i + \text{Re}\{v_i\}, & (i \bmod 2) = 0, \\ \text{Im}\{r_i\} = s'_i + \text{Im}\{v_i\}, & \text{otherwise,} \end{cases} \quad (4)$$

where $\text{Re}\{x\}$ is the real part of x , $\text{Im}\{x\}$ is the imaginary part of x and $s'_i \in \{-1, +1\}$ is the i th chip modulated with binary phase shift keying. For a certain codeword c , the corresponding mapped chip sequence would be $s' = (s'_0, s'_1, s'_2, \dots, s'_{31})$. Since $\text{Re}\{v_i\}$ and $\text{Im}\{v_i\}$ are Gaussian noises with variance $\sigma^2/2$, the conditional probability density function of received bit r'_i given a prior information of transmitted bit s'_i can be estimated by

$$f(r'_i | s'_i) = \frac{1}{\sqrt{\pi\sigma^2}} e^{-(r'_i - s'_i)^2 / \sigma^2}. \quad (5)$$

The conditional probability density function of the received 32-chip sequence given a prior information of the transmitted chip sequence s' can be estimated by

$$\begin{aligned} f(\mathbf{r}' | \mathbf{s}') &= \prod_{i=0}^{31} e^{-|r'_i - s'_i|^2} \\ &= \left(\prod_{i=0}^{31} e^{-(r'_i)^2 + 1} \right) \times e^{\sum_{i=0}^{31} 2r'_i s'_i}, \end{aligned} \quad (6)$$

where $\mathbf{r}' = (r'_0, r'_1, r'_2, \dots, r'_{31})$ is the received soft chip sequence. In (6), the term $\prod_{i=0}^{31} e^{-(r'_i)^2 + 1}$ is a constant for all possible codewords c . The term $\sum_{i=0}^{31} 2r'_i s'_i$ is a real number. Since e^x is a monotonically increasing function when x is real, the maximum-likelihood (ML) sequence decoder of the above block code can be written as

$$\begin{aligned} \hat{c} &= \arg \max_c f(\mathbf{r}' | \mathbf{s}') \\ &= \arg \max_c \sum_{i=0}^{31} r'_i \cdot s'_i. \end{aligned} \quad (7)$$

Equation (7) suggests that the optimal cross-correlation between the received soft chips and the modulated codeword gives the ML sequence decoder of the codeword.

By adopting the proposed (32,4) code defined in Fig. 4, we can further simplify the ML sequence decoder by computing only half of the correlation values since half of the codewords are just the opposite values of the other codewords.

At the end of this section, we would like to discuss the computational complexity of the proposed block coding schemes. Comparing the proposed (32,4) code with the code used in the standard (as shown in Table 1), a simple look-up-table (LUT) can be applied as the encoder. The codewords used in the standard have cyclic shift structure that can be applied to further simplify the encoder design. Nevertheless, the encoder complexities of both codes are low. For the proposed (32, 6) code, the LUT-based encoder is slightly more complex than the code used in the standard. On the other hand, if we generate the codewords from the BCH generator polynomial, the encoder of the (32, 6) code can also be simple.

In the decoder, the above proposed ML sequence decoder achieves optimal symbol error rate for the proposed block codes as well as the code used in the standard. As we discussed earlier, for the proposed (32,4) code, we only need to compute eight cross-correlation values between received soft chips and the candidate codewords. Given the properties of the code used in the standard, we conclude that the optimal decoder also needs to compute eight cross-correlation values. Thus, the decoding complexities of these two codes are about the same. For the proposed (32,6) extended BCH code, 32 cross-correlation values need to be computed. The decoding complexity is slightly higher than the (32,4) code. In summary, the proposed block code provides additional coding gain to the LR-WPANs systems with no or little additional computational complexity.

4 Coding schemes based on convolutional codes

In Section 3, we propose the improved coding schemes based on linear block codes. The proposed coding schemes are similar to that used in current standard and require minimum changes to the standard. The proposed coding schemes achieve the upper bound of d_{\min} as linear block codes. In practice, the coding gain can be further improved if we do not restrict the type of codes. One of the alternative codes is convolutional code. In this section, we discuss the possibility of applying convolutional codes to LR-WPANs. Optimum generator polynomials of convolutional codes are utilised for LR-WPANs.

In general, we assume that the encoder has a code rate $R_c = 1/n$ with constraint length K in LR-WPANs. The asymptotic coding gain for convolutional codes with soft decision in AWGN channel can be defined as

$$\gamma \simeq 10 \log_{10}(R_c d_f), \quad (8)$$

where d_f is the free distance of convolutional codes. For a given code rate R_c , the asymptotic coding gain is restricted by the free distance of convolutional codes. The free distance of convolutional codes is directly related to the generator polynomials. The Heller bound or the upper bound of the free distance of convolutional codes with code rate $R_c = 1/n$ is given by [11]

$$d_f \leq d_H \triangleq \min_{l \geq 1} \left[\frac{2^{l-1}}{2^l - 1} (K + l - 1)n \right], \quad (9)$$

where ' $\lfloor \cdot \rfloor$ ' denotes the largest integer that is less than or equal to the input. Assume that d_H is minimised at $l=h$, that is, $d_H = \min_{h \geq 1} \lfloor (2^{h-1}/2^h - 1)(K + h - 1)n \rfloor$. Then, a tighter bound can be obtained when d_H is odd and $d_H > (2^{h-1}/2^h - 1)\{(K + h - 1)$

$n - 1 + 2^{1-h}\}$. We have

$$d_f \leq \min_{l \geq 1} \left[\frac{2^{l-1}}{2^l - 1} (K + l - 1)n \right] - 1. \quad (10)$$

Exhaust search of generator polynomials, which can be terminated when the free distance of encoder achieves the improved Heller bound, has been executed to find maximum free distance convolutional codes [12]. The maximum free distance convolutional codes are often deemed as optimum convolutional codes in AWGN channel. Frenger *et al.* [16] presented a family of rate-compatible LR convolutional codes with maximum free distance. Maximum free distance codes with rates ranging from 1/4 to 1/512 and constraint lengths between 3 and 11 are tabulated in [16]. With these codes, a convolutional code of any code rate $R_c = 1/n$ can be obtained for different constraint lengths, resulting in flexible and powerful coding schemes. In this paper, we utilise the existing LR convolutional codes for further discussion.

In LR-WPANs, the packet length is usually small. The application of convolutional codes may result in rate loss when transmitting additional known terminating bits to flush out the memory. TBC codes can help to eliminate the rate loss by initialising the memory state with actual tail bits in the transmitted sequence. It is widely used in numerous communication systems such as the worldwide interoperability for microwave access and the long-term evolution. In IEEE 802.15.4 standard, the maximum length of payload is as small as 20 bytes. The TBC codes with optimum generator polynomials are suitable coding schemes for short-packet applications.

Let C be an $(n, 1)$ TBC code, where n is the number of output bits per input information bit. The encoder of TBC code is initialised with the tail $K - 1$ information bits in the transmitted sequence, where K is the constraint length of the code. The output bits per information bit are generated corresponding to memory state and generator polynomials, which can be defined by $c = (c_0, c_1, \dots, c_{n-1})$.

At the receiver side, many studies have been made to reduce the decoding complexity of the ML decoders for tail-biting trellises [17–19]. Sub-optimal decoders such as wrap-around Viterbi algorithm [20] and other alternatives [21] are also developed. Since decoding algorithms of the TBC code are not the focus of this paper, we select a low-complexity sub-optimal method in [21] to decode the TBC code for LR-WPANs. Denote $\mathbf{r}' = (r'_0, r'_1, \dots, r'_{nL-1})$ as the received soft chip sequence, where L is the length of the information sequence. Copying the ending nT values of \mathbf{r}' to the front of the received sequence, and copying the leading nH values of \mathbf{r}' to the end of the received sequence, the extended received sequence for TBC code decoder is given by

$$\mathbf{r}_e = (r'_{nL-1-(nT-1)}, \dots, r'_{nL-1}, r'_0, r'_1, \dots, r'_{nL-1}, r'_0, \dots, r'_{nH-1}), \quad (11)$$

where T is the length of copied information bits in the tail and H is the length of copied information bits in the head. A super trellis can be constructed on \mathbf{r}_e . It is safe to assume that the starting and terminating states are known as all-zero states for this trellis. Viterbi algorithm can be applied to the super trellis \mathbf{r}_e . The corresponding decoder output of the middle L bits is the decoder output. The performance loss of this sub-optimal decoder is negligible when $T \geq 5K$ and $H \geq 5K$ [21].

In IEEE 802.15.4 standard, the chip rate is eight times to that of information bits, which can be viewed as an encoder with code rate $R_c = 1/8$. For a given code rate $R_c = 1/8$, the maximum free distance of improved Heller bound is shown in Fig. 6. The maximum free distance increases almost linearly with constraint length K . However, the number of states in trellis, which indicates the complexity of decoding algorithm, increases exponentially with the constraint length of the code. The constraint length $K = 7$ is chosen as a compromise between performance and complexity

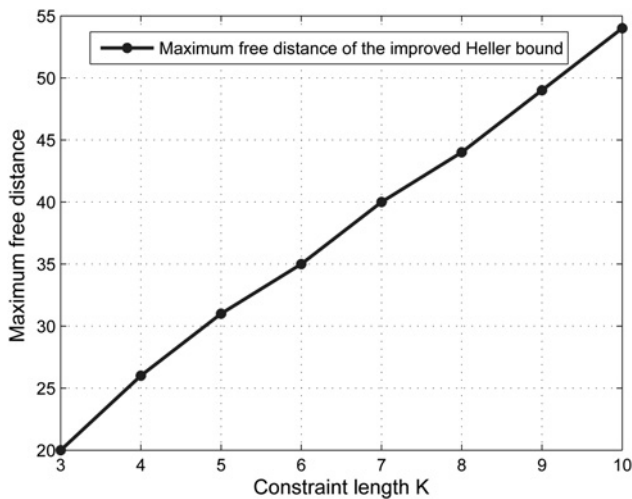


Fig. 6 Maximum free distance of the improved Heller bound with code rate $R_c = 1/8$

[22, 23]. The corresponding generator polynomials of TBC code in octal format are 117, 127, 135, 135, 145, 155, 171, 173 [16].

Next, we evaluate the encoding and decoding complexities of the proposed TBC code. The encoder of the TBC involves the operation of shift registers with length 6. The encoder complexity is low. In the decoder part, the sub-optimal reduced complexity circular Viterbi decoding algorithm [21] gives satisfactory performance with comparable complexity as the regular Viterbi algorithm. Such decoder has higher computational complexity than the ML sequence decoder for the block code. However, the computational complexity of the Viterbi-like algorithm is still acceptable for LR-WPAN systems with reasonable increase of the logic size and memory size. We emphasise that the coding gain of the proposed TBC code is significant comparing with the block code in the standard.

5 Simulation results

In this section, we explore the PER performance of the proposed coding schemes. The transceiver structure is shown in Fig. 1. The encoder block takes random binary input and generates coded bits. The coded bits are mapped to constellations with OQPSK modulation. A half-sine pulse shaping filter is applied in the transmitter. AWGN channel and Rayleigh flat-fading channel are utilised in the following simulations. At the receiver side, matched filter is utilised to maximise the SNR of the received signals. Perfect synchronisation is assumed. For the block code, the ML decoder in (7) is applied. For the TBC code, a low-complexity sub-optimal Viterbi algorithm [21] is utilised for decoding. The detailed description of the decoding algorithm is listed in Section 4. The system performance is evaluated at PER of 1% with effective payload length of 20 bytes. The number of simulated packets is 10^7 in every SNR condition. The simulation setup is summarised in Table 3.

In the first simulation, we compare the PER performance of the (32,4) code used in current standard, the (32,4) code based on

Table 3 Simulation parameters

Parameters	Values
modulation	OQPSK
pulse shaping filter	half-sine
chip rate	2 Mb/s
payload length	20 bytes
number of packets	10^7

extended BCH code, the (32,6) extended BCH code and the TBC code with optimum generator polynomials in AWGN channel.

Fig. 7 shows the PER performance of different coding schemes in AWGN channel. The PER performance with respect to SNR per bit is shown in Fig. 7a. For LR-WPANs, the receive sensitivity is usually measured by SNR per chip. We redraw Fig. 7a in Fig. 7b to show the PER performance with respect to SNR per chip. The dashed lines show PER performance of the (32,4) code used in current standard; the solid lines show PER performance of the (32,4) code based on extended BCH code; the dash-dotted lines show PER performance of the (32,6) extended BCH code; and the dotted lines show PER performance of the TBC code with optimum generator polynomials. From Fig. 7a, we observe that at the PER of 1%, the (32,4) code based on extended BCH code achieves about 0.5 dB coding gain compared with the (32,4) code used in current standard. The (32,6) extended BCH code achieves about 1.8 dB coding gain compared with the (32,4) code used in current standard. While the TBC code with optimum generator polynomials achieves about 4.3 dB coding gain compared with the (32,4) code used in current standard.

In Fig. 7b, the x-axis changes to SNR per chip, which denotes the receive sensitivity in practice. Since the (32,4) code based on extended BCH code and the (32,4) code used in current standard have the same rate, the performance gain is 0.5 dB in terms of the sensitivity as well. We would like to emphasise that the encoding

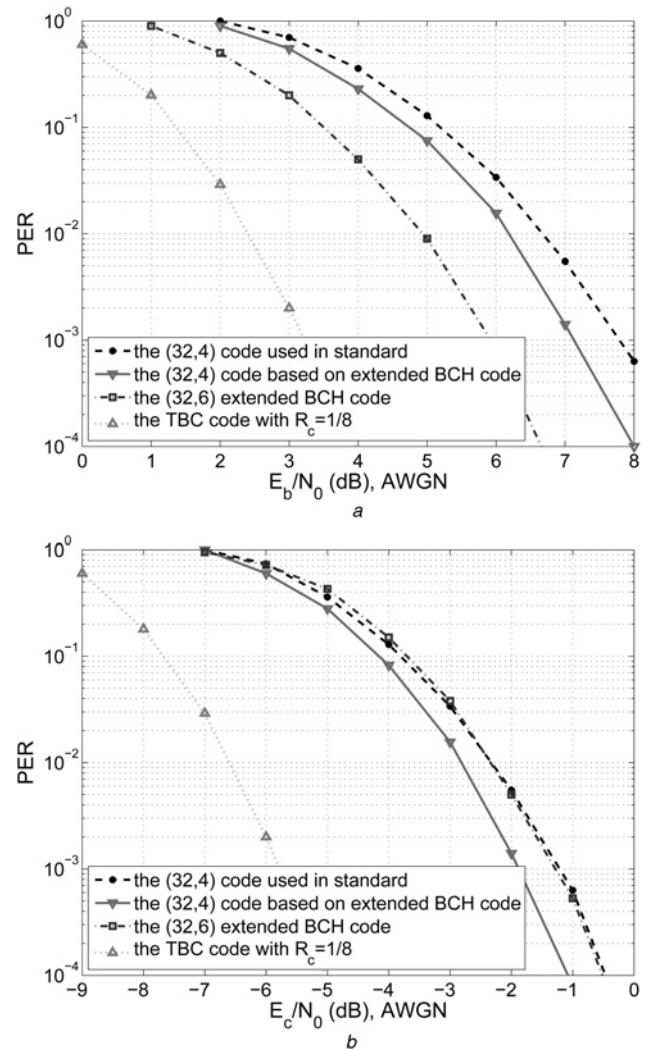


Fig. 7 PER performance of the proposed codes in AWGN channel

a PER performance of the proposed codes with respect to SNR per bit in AWGN channel
 b PER performance of the proposed codes with respect to SNR per chip in AWGN channel

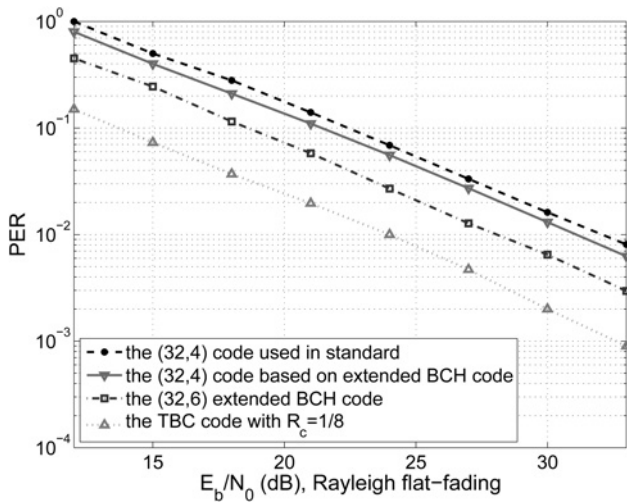


Fig. 8 PER performance of the proposed codes in Rayleigh flat-fading channel

and decoding complexities of the two codes are about the same. The performance of the (32,6) extended BCH code is about the same as that of the (32,4) code used in current standard. However, with the (32,6) extended BCH code, the data rate improves by 50%. The performance improvement of TBC code is significant. The above three coding schemes have their specific advantages. The (32,4) code based on extended BCH code improves performance without extra complexity. The (32,6) extended BCH code improves the data rate without receive sensitivity loss. The TBC code with optimum generator polynomials significantly improves the performance at the expense of extra decoding complexity.

In the second simulation, we repeat the simulation in Rayleigh flat-fading channel. The PER performance with respect to SNR per bit is shown in Fig. 8. The definition of each line in Fig. 8 follows the definition in the first simulation. We observe that the (32,4) code based on extended BCH code, the (32,6) extended BCH code and the TBC code with optimum generator polynomials achieves about 1.0, 4.0 and 8.0 dB coding gain compared with the (32,4) code used in current standard, respectively. The performance improvement in Rayleigh flat-fading channel is even more significant than that in AWGN channel.

6 Discussion

The purpose of this paper is to provide solutions in improving the coding gain of LR-WPANs. Our proposed coding schemes can be applied to other LR-WPANs standards as well. For example, IEEE 802.15.4c standard has similar coding scheme to IEEE 802.15.4 standard. Every four information bits (u_0, u_1, u_2, u_3) are mapped to a 16-chip sequence [24]. The minimum Hamming distance of this (16,4) code is $d_{\min}=6$. This coding scheme does not fully utilise the benefit of the code redundancy either. By adopting similar coding scheme as shown in Fig. 4, we design a (16,4) code based on extended BCH code, which achieves the upper bound of linear block (16,4) code with $d_{\min}=8$. The (16,5) extended BCH code is found to improve the data rate without performance loss. In addition, the optimum generator polynomials of the TBC code in octal format with code rate $R_c=1/4$ and constraint length $K=7$ are 117, 127, 155, 171 [16].

Fig. 9 shows the performance with respect to SNR per bit of the (16,4) code used in IEEE 802.15.4c standard, the (16,4) code based on extended BCH code, the (16,5) extended BCH code and the TBC code with optimum generator polynomials in AWGN channel. The simulation setup is similar to that in Section 5. The definition of each line follows the definition in Fig. 7. Compared with the (16,4) code used in IEEE 802.15.4c standard, the performance gains of the (16,4) code based on extended BCH

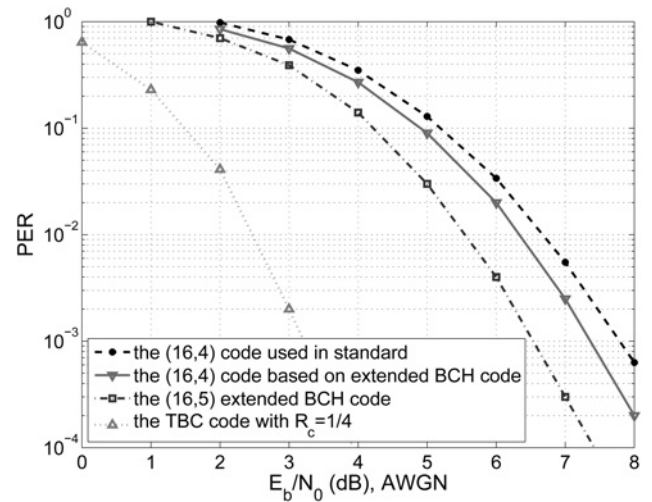


Fig. 9 PER performance of the proposed codes for IEEE 802.15.4c standard in AWGN channel

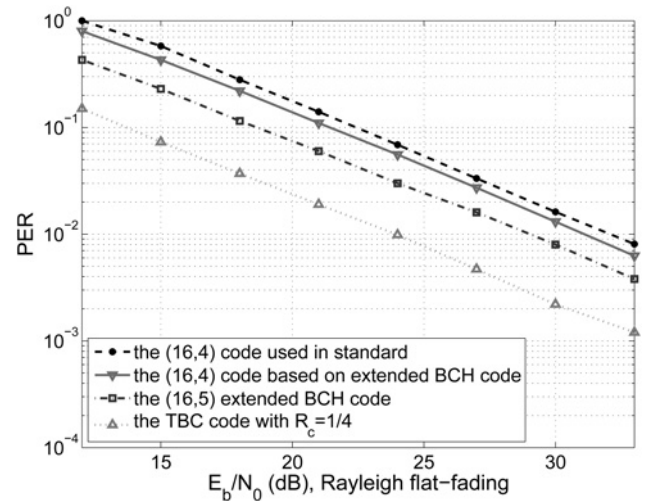


Fig. 10 PER performance of the proposed codes for IEEE 802.15.4c standard in Rayleigh flat-fading channel

code, the (16,5) extended BCH code and the TBC code with optimal generator polynomials are 0.4, 0.9 and 4.1 dB, respectively.

Similarly, Fig. 10 shows the performance with respect to SNR per bit of the (16,4) code used in IEEE 802.15.4c standard, the (16,4) code based on extended BCH code, the (16,5) extended BCH code and the TBC code with optimum generator polynomials in Rayleigh flat-fading channel. The definition of each line follows the definition in Fig. 7. Compared with the (16,4) code used in IEEE 802.15.4c standard, the performance gains of the (16,4) code based on extended BCH code, the (16,5) extended BCH code and the TBC code with optimal generator polynomials are 1.0, 3.0 and 8.0 dB, respectively.

7 Conclusion

In LR-WPANs, existing coding techniques do not fully utilise the benefit of the code redundancy. In this paper, we propose new coding schemes that achieve the largest minimum Hamming distance d_{\min} or free distance d_f at the required code rate. In IEEE 802.15.4 system, the proposed (32,4) code achieves about 0.5 dB improvement in terms of PER performance in AWGN channel and 1.0 dB in Rayleigh flat-fading channel. In addition, the design

complexities of encoder and decoder remain about the same. The coding gain of the (32,6) extended BCH code is 1.8 dB in AWGN channel and 4.0 dB in Rayleigh flat-fading channel. With the (32,6) extended BCH code, the data rate can be increased by 50% with no performance loss. The TBC code with optimum generator polynomials significantly improves the system performance by 4.3 dB in AWGN channel and 8.0 dB in Rayleigh flat-fading channel. The proposed coding schemes can be extended to other LR-WPANs standards.

8 Acknowledgments

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