A Bulk Silicon SOI Process for Active Integrated Sensors

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Abstract

This paper reports a process for the formation of very high quality single-crystal silicon films on glass substrates The process utilizes the electrostatic bonding of silicon and glass wafers, with subsequent etching of the silicon to form silicon-on-insulator (SOI) films having thicknesses controlled from less than 2 μm to over 20 μm with better than 10% uniformity The use of Corning type 1729 glass substrates yields an excellent thermal expansion match to the silicon film and allows the use of post-bond processing temperatures as high as 850 °C, permitting the formation of both transducer and transistor structures in the film after bonding and etch-back Thus, the process offers one means of integrating MOS or bipolar circuitry into dissolved-wafer sensing structures MOS devices formed in such films show characteristics similar to those in standard bulk silicon, including n-channel mobilities of 640 cm^2/V s, the highest ever reported for SOI on glass A variety of related processes are also possible, where some or all of the high-temperature silicon device processing is performed before bonding to the glass substrate

Introduction

Over the past several years, the design/fabrication options for silicon sensors have expanded considerably with the introduction of surface micromachining techniques [1–4] which permit the realization of a variety of sensors and actuators, particularly resonant structures, using laterally-undercut sacrificial layers These processes permit single-sided wafer processing to be carried out and are compatible with the integration of on-chip circuitry [5], however, the control of stress in the deposited sensing films is challenging, and the structures are difficult to scale vertically Bulk silicon transducer processes have also broadened considerably with the use of silicon fusion for microstructure formation [6] In addition, silicon-on-glass processes based on bonding and etch-back (dissolved-wafer processes) [7–9] offer the ability to create a variety of microstructures from bulk silicon using a simple single-sided process These structures can be scaled vertically over a broad range using diffused or epitaxial etch-stops and avoid many of the stress-controlled problems associated with deposited films, however, the monolithic integration of active circuitry in such structures has not yet been demonstrated While hybrid circuitry may be acceptable or even preferred for many applications, other applications require monolithic signal processing for lead minimization, signal amplification, or cost reduction The use of a substrate which is electrically insulating, thermally insulating, or optically transparent is also often desirable, and the dissolved-wafer silicon-on-glass process offers obvious advantages for these devices

There are many possible approaches to the monolithic integration of circuitry with dissolved-wafer processes, and the bulk-silicon SOI approach reported here represents one of them In it, etch-stops are first created in the silicon wafer using diffusion or epitaxy, followed by the use of anodic bonding and etch-back to form a single-crystal silicon film on the glass support wafer Additional processing is then used to create transducers and high-performance circuitry on the monolithic chip The process produces better quality silicon films than do recrystallized SOI processes [10] and has the added advantage of allowing the use of arbitrarily thick silicon films It also permits the formation of three-dimensional structures and devices in the SOI layer Wafer topography permitting, device contacts and interconnects can be routed on top of the SOI film, avoiding lead transfers and simplifying packaging This approach appears particularly attractive for applications such as active-matrix liquid-crystal displays, large-area tactile imagers, and ultraminiature pressure/flow sensors which require high-performance on-chip readout electronics and/or distributed signal processing

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Process Description

The basic approach to creating the thin silicon film on the glass substrate is shown in Fig 1 The process begins with a ⟨100⟩ oriented silicon wafer having an epitaxial layer in which the eventual devices will be created A silicon etch-stop is realized at the epi–substrate junction using any of several techniques Two approaches have been used in this research In the first, a heavily-doped (p-type, $>10^{19}$ cm^{-3}) diffused boron buried layer is used between the epitaxial film and a lightly doped substrate A boron-concentration-sensitive etchant can then be used to remove the bulk silicon substrate and stop on the heavily-doped boron layer The second approach utilized a heavily-doped (n-type or p-type, $>10^{18}$ cm^{-3}) substrate with an epitaxial layer of the desired thickness and resistivity grown directly on it Such p/p$^+$ or n/n$^+$ CMOS wafers are widely available for use in CMOS VLSI These wafers are then subjected to a concentration-sensitive etchant that removes the bulk substrate and stops on the lightly-doped epitaxial layer We refer to this method as the CMOS etch-stop (CES) process One can also conceive etch-stop processes that employ an electrochemical etch-stop where an externally applied potential is used to control the silicon etch rate at the junction As with any epitaxial process, the growth conditions should be optimized to minimize out-diffusion into the film and defects induced by the etch-stop layer

The silicon wafer with the appropriate etch-stops is next electrostatically bonded to a glass substrate by a standard process [11] Both Corning type 1729 and Corning type 7740 substrates have been used successfully Corning type 1729 glass has several distinct advantages, including thermal expansion coefficient, anneal point, and composition [12] Type 1729 glass offers an almost exact match in thermal expansion coefficient to silicon from room temperature to over 800 °C The high anneal point (853 °C) of this glass permits device fabrication after the silicon film has been formed on the glass substrate, because oxidation and implanted-dopant activation processes become feasible in the 800 °C to 850 °C range Type 1729 glass is also 'alkali free', in that sodium and potassium are not necessary constituents of the material

The type of glass used in the process also affects the bonding conditions Figure 2 shows the time required to achieve a bonded area of approximately one square inch for various bonding voltages and glass thicknesses A distributed contact was used to apply a potential to the silicon wafer and a point contact was used to ground the glass wafer The point contact was used with the glass on top so that one could view the bond as it propagated across the interface While the required voltage is generally higher for the type 1729 glass than for the type 7740, scaling the type 1729 glass thickness down to 0 5 mm should reduce the bonding voltage by nearly a factor of two, placing it in a range similar to that for the 7740 glass

In glasses containing alkali, such as type 7740, the mobile cations (Na^+) drift toward the anode (silicon), causing an increased fraction of the applied potential to be dropped near the silicon–glass bonding interface This provides a greater force to pull the two surfaces together [12] and results in lower bond voltages In an alkali-free glass such as type 1729, the voltage distribution in the glass is more uniform [10], resulting in the

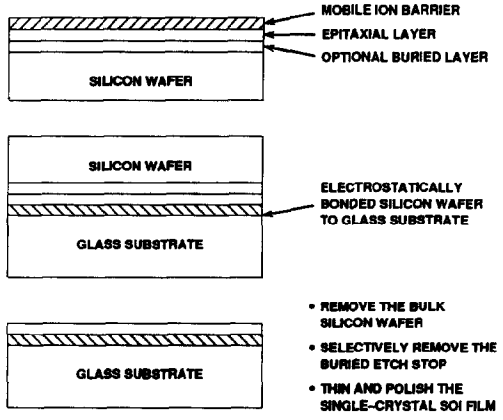

Fig 1 Process flow for producing single-crystal silicon films on glass

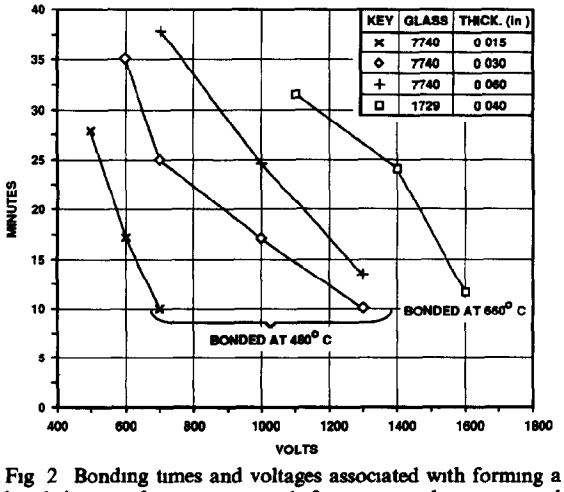

Fig 2 Bonding times and voltages associated with forming a bonded area of one square inch for various glass types and thicknesses

need to use higher bonding voltages to achieve the same force at the silicon–glass interface While sodium thus plays an important role in determining the potential distribution in the bonding materials, it is not thought to contribute to the chemical process of glass–silicon bond formation Oxygen ions generated from defects in the glass, particularly E-centers, are thought to drift towards the anode, where they form a covalent bond with the silicon [10] Due to the high local forces generated by the electrostatic field, a bonded area coverage of over 99 8% on three inch wafers has been typically observed As with electrostatic bonds between type 7740 glass and silicon, the type 1729 glass-to-silicon bond is stronger than the silicon itself, with fracture occurring in the bulk of the silicon wafer rather than at the interface This supports the idea that oxygen from the glass acts as the bridging atom between the two bonding surfaces, since the Si–O bond is about 2 5 times stronger than the Si–Si bond

In device applications, a stress-compensated multilayer film of silicon dioxide, silicon nitride and silicon dioxide [13] is deposited on the silicon surface via pyrolytic CVD prior to bonding to the glass This film functions as a mobile ion barrier, preventing sodium ion migration into the silicon during subsequent device processing Electrostatic bonding between dielectrically-coated silicon wafers and type 1729 glass has typically been performed at 670 °C, and subsequent heating to as much as 850 °C has not noticeably altered the bond or its strength Fracture studies have demonstrated that the bonded interface as well as the interface between the ion barrier and silicon are both stronger than the Si–Si bonds in the bulk wafer The back surface of the glass wafer is typically coated with a layer of silicon nitride to encapsulate the glass completely, thus minimizing the possibility of ionic contamination of the silicon

After bonding, the silicon wafer is subjected to an unmasked etch to remove the bulk silicon wafer down to the buried etch-stop With boron etch-stop technology, an ethylenediamine–pyrocatechol–water (EDP) solution [14] has been used The EDP etch rate in silicon effectively drops to zero as the boron concentration reaches the $10^{19}\,cm^{-3}$ range With the CES process, an 8 3 1 acetic, nitric, hydrofluoric acid etch has been employed [15] The 8 3 1 etchant slows by a factor of at least 100 when encountering the lightly-doped epitaxial layer, effectively yielding an etch-stop as well

Following the removal of the bulk silicon, the remaining SOI film is further etched to remove the buried layer, if the boron etch-stop is used This etch is also used to reduce the film thickness to within a few microns of the desired value The SOI film is then completed by polishing the surface using conventional techniques This results in a very high quality SOI film that is comparable to a bulk silicon surface In this work, these etching processes have allowed high quality 75 mm SOI wafers to be formed The boron etch-stop process has yielded slightly better silicon film thickness uniformity, while the CES substrates have yielded better epitaxial film quality

The SOI film that results from either of these processes can then be patterned to form dielectrically isolated islands of silicon on the glass surface This was typically done by depositing a layer of low-temperature silicon dioxide on the polished surface of the silicon film The oxide was then patterned using conventional lithography techniques and used as a mask for subsequent preferential silicon etching, typically with EDP The thickness contour plot for an SOI film formed using a 28 μm epitaxial layer and the boron etch-stop process is shown in Fig 3 The plot was derived by surface profilometry after preferentially removing the buried layer with a chemical etch Over most of the wafer area, the film thickness is uniform to within 5%, and some of the variation noted is probably due to nonuniformity in the epitaxial and buried-layer thicknesses themselves

The overall process is capable of producing SOI films which are uniform in thickness to within 10% or better (e g , $\pm 0\,5\,\mu$m on a 5 μm final film) This uniformity is adequate for most sensing applications, and it could be improved with tighter process control X-ray diffraction measurements for the SOI films on glass have shown these films to be ⟨100⟩ oriented and essentially identical to the starting substrate Studies with defect-sensi-

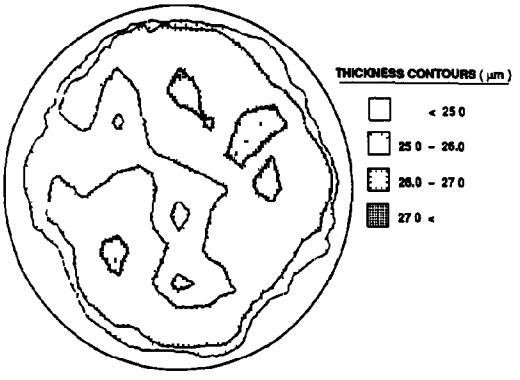

Fig 3 Measured thickness contours for an SOI film on a 75 mm glass wafer The SOI film had a mean thickness of 26 8 μm after removal of the boron etch-stop layer

tive etchants have shown the SOI films to be of similar quality to the original epitaxial layer prior to bonding Hall measurements on 1 2–5 μm thick n-type silicon films produced using the boron etch-stop technology on type 1729 glass with an ion barrier have produced electron mobilities of 890 cm^2/V s and hole mobilities of 350 cm^2/V s as compared with values of 1105 and 342 cm^2/V s obtained in the bulk, respectively

Device Structures

One of the principal advantages of this process over other SOI approaches is that high-temperature processing of the silicon is possible prior to glass substrate attachment, so that a variety of structures can be created using the ability to process both sides of the silicon film Figure 4 shows an MOS structure realized using single-sided processing of the film Both n-channel and p-channel MOSFETs have been realized using this process The n-channel devices resulted in electron surface mobilities of 640 cm^2/V s, the highest ever reported for an SOI transistor on glass [16] The off-state drain leakage current was less than 0 1 pA/μm This is an exceptionally low value for SOI transistors and compares favorably with the best devices yet reported on glass substrates The upper limit of 850 °C on post-bond processing temperatures allows relatively standard gate oxidation processes to be used for MOS device fabrication This temperature range is also sufficient for ion-implanted dopants to be fully activated through thermal annealing

Figure 5 shows a bipolar transistor structure realized using double-sided film processing A high-temperature diffusion was used prior to electrostatic bonding to form a highly doped n^+ buried collector layer on the back surface of the SOI film A mobile ion barrier is then deposited and standard processing used to form the silicon film on glass As with the MOS devices above, device islands were formed using a selective anisotropic etch, and deposited oxides were used to

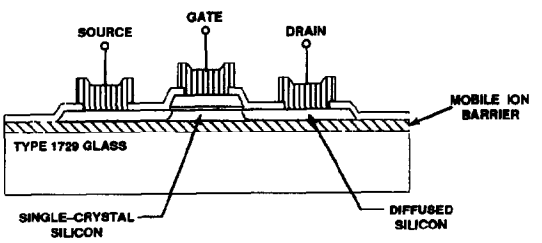

Fig 4 An MOS transistor structure formed in single-crystal silicon on glass

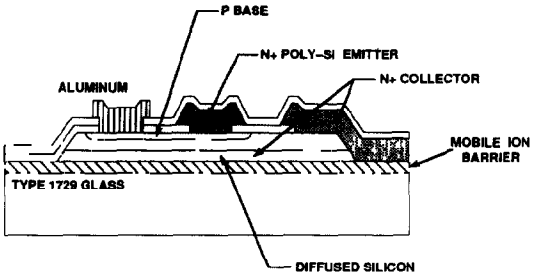

Fig 5 A vertical NPN bipolar transistor structure on glass The n^+ buried collector is formed using a pre-bond diffusion from the front of the silicon wafer

passivate the device The p-type base was implanted with boron using an oxide mask and a polysilicon emitter was formed using CVD The devices were then annealed and an oxide passivation layer was deposited Contact holes were then opened, and aluminum was deposited and patterned to form the interconnect These BJTs are still being optimized with regard to the polysilicon emitter technology, however, the entire process has been run without other difficulty

Where islands are etched to provide lateral dielectric isolation, thicker or more conformal resists are required for post-island processing as the film thickness increases This limits feature size to approximately 5 μm for our current films and lithography technology This minimum feature size is adequate for most sensing applications, but could probably be reduced by adopting a multilayer resist technology Nonetheless, planarity difficulties can limit the range of useful film thicknesses when lithography is required after island formation

Figure 6 shows the proposed process [17] for an ultraminiature pressure sensor with on-chip electronics A CMOS epitaxial wafer is deep diffused with boron to form a rim for the transducer, while a shallow, high-temperature boron diffusion is used for the recessed diaphragm A barrier dielectric is deposited and the wafer is sealed to the glass, after which the bulk of the wafer is dissolved to the etch-stop Relatively standard device processing (< 850 °C) is then used to form readout circuitry in the remaining circuit islands All of the individual steps in this fabrication sequence have been successfully run individually, and the overall combined process is now being implemented

A variety of other alternative processes could also be implemented with this approach to sensor fabrication Particularly attractive for some applications are those in which most or all of the circuit processing is done prior to glass bonding, so that the devices are on the lower surface of the

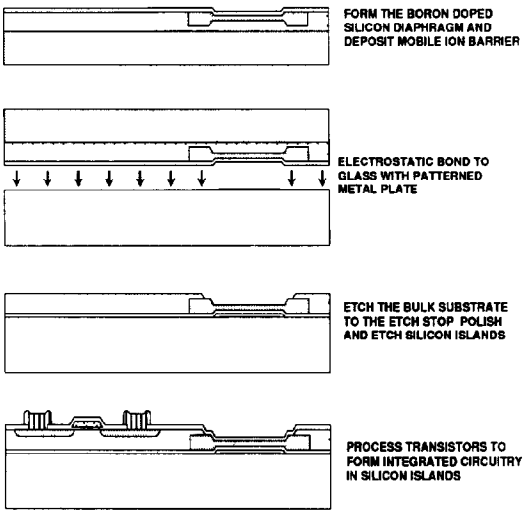

Fig 6 A proposed process for an active capacitive pressure sensor on glass

silicon, next to the glass In this case the electrostatic bond to the glass is accomplished via deposited pillars or other elevated areas on the silicon to protect the preformed devices from the electrostatic field encountered during the bonding process Such structures are more complex than the one illustrated in Fig 6, but they avoid the necessity of processing the glass wafers When an encapsulating layer of CVD silicon nitride is used over the glass, however, no cross-contamination problems have been observed, and the ability to perform double-sided processing on semiconducting SOI films of almost arbitrary thickness allows the formation of a number of structures that are impossible to realize using other SOI or sensor technologies

Conclusions

The use of electrostatic glass–silicon bonding, epitaxial and diffused etch-stops, and impurity-sensitive silicon etchants can be the basis for the creation of a variety of microstructures for sensing and actuation from the silicon bulk Where on-chip active circuitry is required, the most straightforward approach is to form this circuitry prior to bonding and etch-back, assuming a single-sided wafer process is employed The process described in this paper extends these possibilities, however, by showing it is possible to perform high-temperature device processing after silicon–glass bonding The resulting device characteristics are comparable to those found in normal bulk silicon, while the ability to perform double-sided film processing permits a variety of novel device structures to be formed which are not possible using more conventional technologies

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Biographies

Kensall D Wise received the BSEE degree with highest distinction from Purdue University in 1963 and the MS and Ph D degrees in electrical engineering from Stanford University in 1964 and 1969, respectively From 1963 to 1965 (on leave 1965–1969) and from 1972 to 1974, he was a member of technical staff at Bell Telephone Laboratories, where his work was concerned with the exploratory development of integrated electronics for use in telephone communications From 1965 to 1972 he was a research assistant and then a research associate and lecturer in the Department of Electrical Engineering at Stanford, working on the development of integrated circuit technology and its application to solid-state sensors In 1974 he joined the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, where he is now serving as professor and director of the Center for Integrated Sensors and Circuits His present research interests focus on the automated manufacturing of integrated circuits and on the development of solid-state sensors for health care, transporation, and industrial process control

Dr Wise organized and served as the first chairman of the Technical Subcommittee on Solid-State Sensors of the IEEE Electron Devices Society He served as general chairman of the 1984 IEEE Solid-State Sensor Conference, as technical program chairman of the 1985 International Conference on Solid-State Sensors and Actuators, and as IEEE–EDS National Lecturer for 1986 He has served on several program committees for both the International Electron Devices Meeting and the International Solid-State Circuits Conference and received outstanding paper awards from the ISSCC in 1971 and 1979 He is a fellow of the IEEE and a member of the Electrochemical Society, the AVS, Tau Beta Pi, Eta Kappa Nu, and Sigma Xi

Leland 'Chip' Spangler received the BSE(EE) and MSE(EE) from the University of Michigan in 1982 and 1984 respectively In 1988 he completed his Ph D in electrical engineering at the University of Michigan, where his research included the development of solid-state pressure sensors and silicon microprobes His thesis research involved the development of sensor technology for single-crystal silicon transistors on glass substrates

During the summer of 1984 he was employed by the General Motors Research Laboratories in Warren, Michigan, where he developed polysilicon thin-film transistor technology for active matrix liquid-crystal displays for dashboard applications From 1988 to 1990, he worked for Bell Northern Research, Inc where he was responsible for the development of advanced architectures and integrated circuit implementations of associative computers for data and telecommunication network systems Dr Spangler recently joined the staff of the Electronics Division of Ford Motor Company, where he is now involved in the development of sensors and sensor technology for automotive applications