Material related issues and their characterization with a view to III–V heterojunction device optimization

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Abstract

The impact of various material choices, *i.e.* InAlAs/InGaAs, AlGaAs/GaAs, GaInP/GaAs on device characteristics is analyzed. Traps located at various regions of the device impact its performance and can be identified by device characterization such as g_m, R_{ds} dispersion and low-frequency noise. Reliability characteristics can be related to material modifications under stress, *i.e.* traps and dopant diffusion and degradation can be minimized by growth optimization. Process induced damage due to dry-etching can be minimized by proper selection of etching conditions. A strong interaction between material and device research is necessary for best results in optimizing III–V technology.

1. Introduction

Device characterization depends strongly not only on design, process and characterization, but also on the profound understanding of material related issues. Trap related effects in many III–V devices can, for example, result in changes in electrical characteristics at low frequencies or upon cooling. The transconductance g_m and output resistance R_{ds} of FETs can differ at low and high frequencies, as shown by both MESFET and HEMT [1] studies. Evaluation of the low-frequency noise properties of devices at various temperatures also reveals trapping [2] and can be used for assessing the device quality.

The choice of material is very important for device engineering. At the time of device design, it is important to examine the material properties and their impact on device performance. Materials such as GaInP are, for example, preferable for HEMT donor layers compared with AlGaAs, since they contain less DX centers [3]. Pseudomorphic designs offer improved device performance compared with lattice-matched heterostructures but need to be carefully optimized in order to ensure good material quality.

Structural changes may occur during various processing steps, device operation or thermal stressing. Examples of these are generation of defects in various parts of the device, diffusion of dopants across the heterojunction and strain relaxation. Thermal stress of InAlAs/InGaAs HEMTs was found to result in current reduction and enhanced trapping [4]. Reactive ion-etching (RIE) employed at various processing steps, such as gate-recess of FETs and emitter etching to reach the base in HBTs, can induce material damage and may therefore impact the device performance. Substrate orientation is also crucial in certain cases such as, for example, reduced short channel effects and good threshold voltage V_T uniformity [5].

This paper reviews material related issues dictating the performance of III–V devices. Section 2 describes the material choices impacting device performance and impact of strain and growth related issues. Various characteristics related to material properties, such as transconductance/output resistance dispersion and low-frequency noise, are reviewed in Section 3. Short channel effects and the impact of substrate orientation, together with mobility impact by strain and neighboring layers are discussed in Section 4. Section 5 finally reports on material stress and impact on reliability, together with some considerations of material modifications by processing.

2. Material choices impacting device performance

A generic cross-section for a high electron mobility transistor (HEMT) is shown in Fig. 1, together with various regions of the device which determine its performance. Possible heterostructure materials for the realization of such devices include AlGaAs/GaAs, AlGaAs/InGaAs/GaAs, GaInP/GaAs on GaAs and InAlAs/InGaAs on InP. Lattice-matched or pseudomorphic (strained) designs are possible for both GaAs- and InP-based systems. Careful consideration of the

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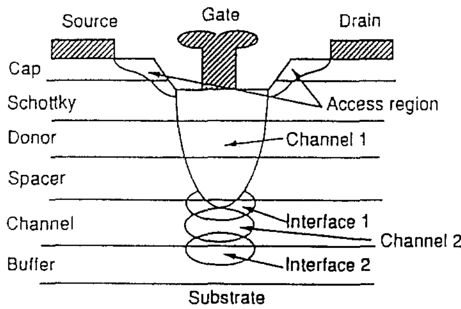

Fig. 1. Generic MESFET/HEMT cross-section and identification of regions impacting device performance.

material and device characteristics shows that they are strongly correlated to each other. Furthermore, some compromise is very often required in the choices made in order to achieve high device performance while at the same time preserving good material properties without parasitic effects in the device. The Al composition x of $Al_xGa_{1-x}As/GaAs$ has, for example, to be maintained below 20% in order to avoid DX-centers and related electron trapping effects in the device. At the same time, the conduction band discontinuity ($\Delta E_c = 0.16$ eV) for such low x value designs does not provide good carrier confinement.

To improve carrier confinement while avoiding DX-centers, one can use pseudomorphic $Al_xGa_{1-x}As/In_yGa_{1-y}As/GaAs$ designs. Here the low Al composition ($x = 0.20$) guarantees less DX-problems, while the high In percentage ($y = 0.15$) in the channel promises high mobility. For designs of this type ΔE_c is approximately 0.30 eV and a high barrier is therefore provided for thermoionic emission in AlGaAs. At the same time, one ends up, however, using a pseudomorphic approach and care has therefore to be taken to ensure good material quality. Similar considerations apply to AlInAs/InGaAs pseudomorphic devices. The In content of the channel is here even higher (greater than or equal to 53%) with the result of even better mobilities, while carrier confinement is excellent owing to the high $\Delta E_c = 0.50$ eV. Material quality attention is, however, again required owing to the pseudomorphic nature of the design.

Another option is $Ga_{0.51}In_{0.49}P/GaAs$ in both lattice-matched and pseudomorphic (with InGaAs instead of GaAs channel) designs. The high ΔE_v (about 0.20–0.24 eV) makes this system very suitable for p-channel FETs [6], but n-channel devices are also possible [3]. Since the Γ–X crossover of $Ga_xIn_{1-x}P$ occurs for $x \approx 0.74$, *i.e.* far away from the lattice-matched composition ($x = 0.51$), there are less DX-center problems.

Some common concerns regarding material issues impacting device characteristics are (i) defects in epitaxial layers, (ii) traps in epitaxial layers and heterointerfaces, (iii) heterointerface sharpness, (iv) thermodynamically metastable strained layers, and (v) dopant diffusivity upon growth or device operation. Many of these effects are evident by observing the device characteristics. This is a particularly attractive feature since instead of making independent material and device characterizations, it is possible to evaluate material characteristics and their impact using the device structures themselves. A better correlation between material properties and device characteristics can be achieved in this way since the same structure is used for all tests. Examples of device parameters evidencing material features are (i) C–V, I–V characteristics, providing mobility and velocity information (transport features), (ii) back- and/or side-gating, (iii) g_m, R_{ds} dispersion, (iv) $1/f$ (low-frequency) noise, (v) current–voltage collapse, (vi) V_T-shifts, and (vii) reliability. It is obvious that material choices and optimization go together with similar considerations for the devices to be built on them and that a continuous interaction is absolutely essential between material and device research.

Material growth is the key issue for successful device operation. A detailed analysis of growth modes proves to be very useful for this purpose [7]. The thermodynamic parameters (surface bond strength, substrate temperature) determine whether an MBE-grown surface is atomically flat or three-dimensional under equilibrium conditions. The factors deciding whether such an equilibrium is reached are kinetic parameters, namely surface migration and evaporation. Both themodynamics and kinetics therefore play an important role in growth quality. For lattice-matched systems growth occurs layer-by-layer, corresponding to an atomically flat surface, provided that surface kinetics are high. In the case of strained layers, once misfit strain exeeds about 1.5%, to 2.0%, the growth takes place in a three-dimensional (3D) mode, leading to a rough surface. Good material quality thus requires a smooth growth front or techniques such as alternate growth of group III and V monolayer (migration enhanced epitaxy, MEE) so that a layer-by-layer mode can be guaranteed even under high strain conditions.

An application of the above growth considerations to the case of InAlAs/InGaAs HEMTs showed clearly the way that device performance is impacted by strain and related growth considerations. Figure 2 shows such results for the mobility and cut-off frequency [8] of devices with 1 μm long gates. The mobility increases with excess In in the channel but starts decreasing above 20% excess In. A similar trend is observed for f_T. Both characteristics can be explained by an initial improvement due to superior transport properties in a high In-content channel, followed by degradation due

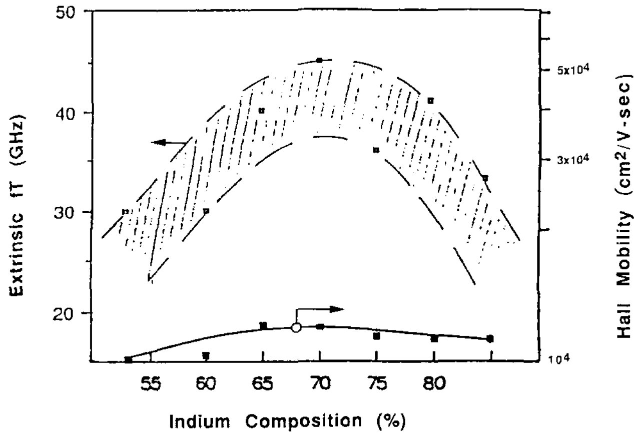

Fig. 2. Impact of strain on mobility and cut-off frequency f_T of InAlAs/InGaAs HEMTs.

to increased interface roughness. The latter is apparently caused by a change from 2D layer-by-layer to 3D island mode growth. MEE can be used to restore the feature of enhanced device properties at increasingly high In-content. This growth technique allows one to restore surface reconstruction in the layer-by-layer mode.

Another example of the impact of material quality on device characteristics is by means of results for the gate leakage reduction in InAlAs Schottky diodes grown by metal-organic vapor phase epitaxy (MOVPE). Studies at the University of Michigan have shown that the photoluminescence (PL) linewidth improves for higher growth temperatures; a change from 40 to 25 meV has been observed in full width at half-maximum (FWHM) by changing the growth temperature from 610 °C (670 °C) as shown by Fig. 3(a) [9]. This temperature change does not seem to affect the mobility, while the background doping density is found to increase slightly with temperature. Background and mobility improve, however, for higher AsH_3 flow. Figure 3(b) shows that the diode reverse characteristics follow similar trends to the PL FWHM, namely a reduced leakage at higher growth temperatures. Optimum AsH_3 flow is also important for low leakage.

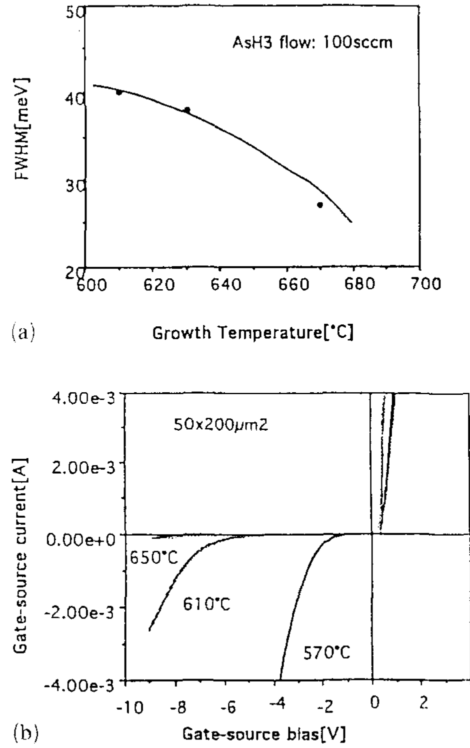

Fig. 3. (a) Photoluminescence (PL) FWHM as a function of temperature and (b) I–V characteristics showing reduced reverse leakage at higher growth temperature.

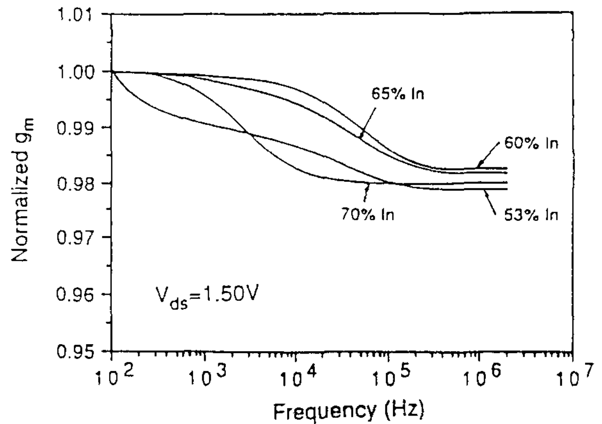

Fig. 4. Normalized transconductance $g_m(f)/g_{m0}$ for InAlAs/$In_xGa_{1-x}As$ HEMT with different In composition x channels ($V_{ds} = 1.5$ V, V_g for $g_{m,peak}$, $L_g = 1$ μm).

3. Low-frequency device characteristics and material correlations

The low-frequency characteristics of devices such as MESFETs and HEMTs are indicative of specific material properties. Examples of such parameters are frequency dispersion in g_m, R_{ds}, which occurs in the kilohertz to megahertz range, $1/f$ and generation–recombination (G–R) noise. The discussions below address the way that the excess In composition of strained designs reflects in the dispersion and low-frequency noise of InAlAs/InGaAs HEMTs.

Figure 4 shows the normalized transconductance characteristics of InAlAs/InGaAs HEMTs with different In channel composition x [1]. One observes that maximum dispersion occurs for $x = 0.53$, while the dispersion reduces for $x = 0.60$. This suggests that MBE

growth and the heterointerface quality are dictated by channel composition, as already mentioned in Section 2. A study of g_m dispersion in MESFETs shows that their dispersion is much larger (about 20%) than in HEMTs (maximum about 7% under ohmic operation of InAlAs/InGaAs devices). Trapping is responsible for g_m dispersion. In the case of MESFETs traps are located at the active-layer–substrate interface or exposed ohmic-Schottky surface (see Fig. 1). In the case of HEMTs, the 2DEG channel is protected by the top layers and is not directly exposed to surface effects. It turns out that the region under the gate rather than the access region determine the HEMT dispersion. This is further supported by the opposite bias dependence manifested for these effects by the two device types; the HEMT dispersion is increasing towards pinch-off in accordance with the fact that I_{ds} modulation in such devices takes place primarily under the channel and surface and access effects are minimal. Furthermore, g_{ds} dispersion is found to follow similar trends to g_m under variable excess In compositions. This suggests that a common trap mechanism is responsible for both g_m and g_{ds} effects. The minimum dispersion observed for 60% In channels is apparently related to the better material quality for small excess In, owing to the larger migration of InAs during growth. This results in better coverage of the growth islands and better heterojunction quality.

Experiments using the a.c. conductance method reveal that the highest and lowest trap density are observed for lattice-matched ($x=0.53$) and slightly strained ($x=0.60$) In composition respectively (see Fig. 5). These tendencies are similar to those observed by g_m,R_{ds} dispersion, as discussed earlier. Localized states in InAlAs near the heterostructure interface or interface states at the band edge of InGaAs may be responsible for the traps. It appears, however, that interfacial rather than bulk InAlAs traps are dictating the observed characteristics [1]. The studies also reveal that both material and device properties are highly sensitive to growth conditions.

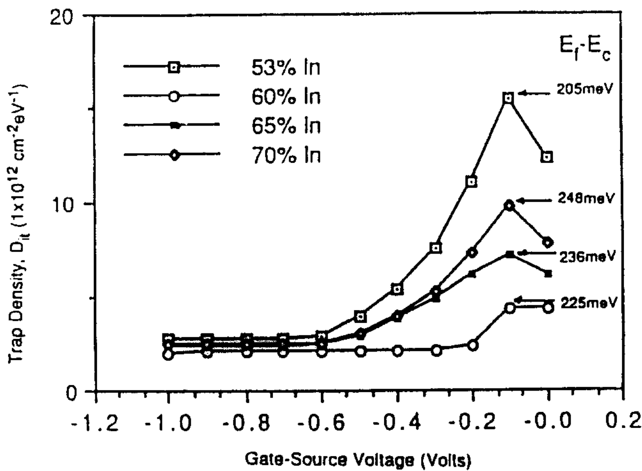

Fig. 5. Trap density D_{it} in InAlAs HEMTs for different channel In contents.

Low-frequency noise is observed in terms of $1/f$ and G–R noise characteristics. The former is related to microscopic changes of mobility or carrier number, while the latter is found superimposed on $1/f$ noise and is indicative of defects and crystal imperfections, resulting in discrete trap levels E_T. Overall, noise is found to be sensitive to process (recess profile, surface treatment) and material (bulk and interface quality). The origin of the low-frequency noise sources can vary according to the bias used for device operation. Distinct or mixed noise contributions can be seen in the overall characteristics of the device. Figure 6 shows schematically the location of noise mechanisms and the bias conditions under which their presence is enhanced and can therefore be more easily identified. The access region to the channel, the main channel (1), the parasitic HEMT channel (2), the top (1) and bottom (2) heterointerfaces can be sources of noise. Their distinct or mixed presence depends on the selected bias. It is evident from the discussion that the noise will be sensitive to the recess profile, the surface treatment and conditions, the quality and properties of each layer and the interface properties of the various layers. The noise characterization and analysis can therefore be used to reveal the signature of each of the above effects.

A study of the impact of channel composition on $1/f$ noise of InAlAs/InGaAs HEMTs revealed that the input noise characteristics are insensitive to In content [2]. $1/f$ transition frequencies are also found to be independent of In and have rather high values (200–300 MHz) compared with MESFETs. A focus on G–R, rather than pure $1/f$ noise characteristics can be much more useful in view of evaluating the material impact. G–R noise originates from fluctuations in carrier number in the FET channel by trapping and re-

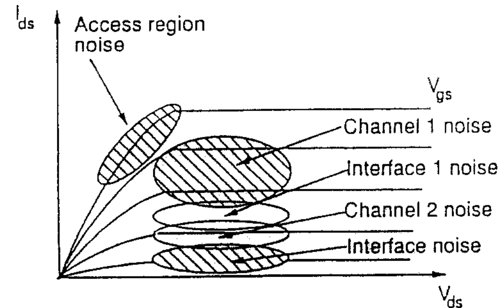

Fig. 6. I–V FET characteristics and their relation to various device regions (see also Fig. 1) in view of evaluating the origin of low-frequency effects.

emission. A study of G–R noise in InAlAs/InGaAs strained HEMTs revealed that the trap activation energy ΔE_i increases with In content. For example, ΔE_i is 0.11 eV, 0.15 eV and 0.18 eV for $x = 0.60, 0.65$ and 0.70 respectively. These trap levels are rather shallow compared with values reported by DLTS measurements for n-InAlAs/InP or low frequency noise characterization of n-InGaAs/p-InP. Overall, it appears that heterointerface rather than bulk InAlAs or InGaAs is responsible for the detected traps. This agrees with similar findings by g_m,R_d dispersion analysis.

The study of the AlGaAs/GaAs material also reveals some interesting features which confirm the importance of material choice on device performance. Figures 7(a) and 7(b) show the input noise voltage spectral density of AlGaAs/GaAs HEMTs and the normalized g_m dispersion as a function of temperature. Lorentz spectra can be observed at 200 K and 350 K respectively, indicating the presence of trap related effects at these temperatures (Fig. 7(a)). It is very interesting to confirm that maximum g_m dispersion also occurs at the same temperatures (Fig. 7(b)). It appears that common traps are related to both effects. These were extracted by Arrhenius plots of the time constants characteristic of the peak G–R spectrum and were found to have activation energies of $E_{a1}2 = 0.58$ eV and $E_{a2} = 0.27$ eV for operation at 350 K and 200 K respectively. The deep trap E_{a2} is also found to be responsible for a dramatic current drop in the I–V characteristic of HEMTs at 200 K. This is apparently related to DX-centers and is absent in GaInP/GaAs HEMTs operated cryogenically [10].

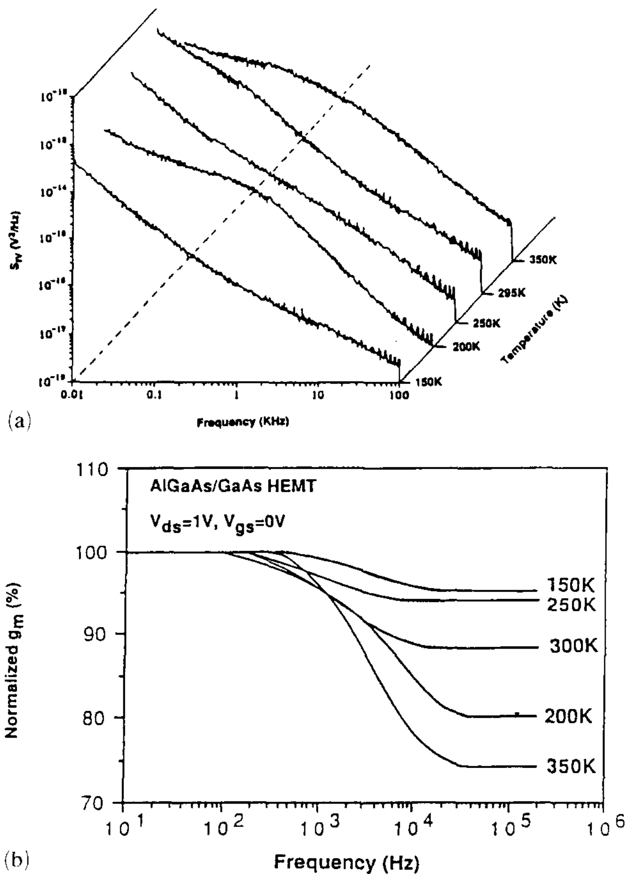

Fig. 7. Presence of trap related effects in AlGaAs/GaAs HEMTs at 200 K and 350 K as evidenced by temperature characteristics of input noise voltage spectral density (a) and transconductance dispersion (b).

4. D.c. characteristics and material correlations

The d.c. characteristics of devices are strongly related to material properties and can very often be used for identifying the impact that the material has on device performance. Hot electron trapping can, for example, result in threshold voltage shifts and I–V collapse at low temperature operation of HEMTs. The material, substrate orientation and induced piezoelectric effects also impact V_T. Transconductance enhancement in pseudomorphic designs is finally related to intrinsic but also adjacent layer material properties. The above d.c. properties therefore merit special attention and need to be investigated in view of material device optimization.

Figure 8 shows schematically how hot-electrons may transfer from the channel to the wider band gap donor layer near the drain of a HEMT. Under low temperature and dark operation conditions this mechanism results in a decrease in channel carrier density and current collapse which, combined with a threshold voltage shift, degrades the device performance. Electron trapping by deep levels in the doped donor layer is responsible for these effects. Deep donors are ionized at room temperature owing to sufficient thermal energy and space-change potential across the junctions. If cooling of the device takes place while a

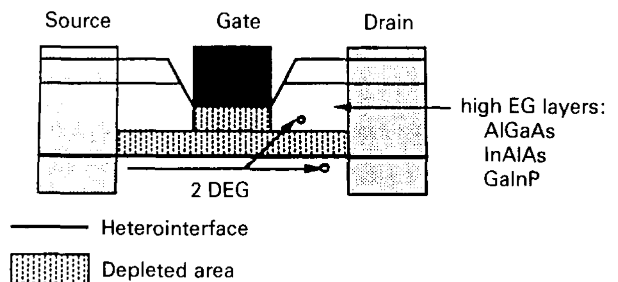

Fig. 8. Schematic representation of hot-electron trapping effects in HEMTs and resulting threshold voltage shift by 77 K operation of various material systems.

positive bias is applied to the gate, carriers are attracted towards the gate and will neutralize the deep donors. Since the trapped carriers are not released by the applied positive voltage, they remain trapped and neutralize the deep donors. The Fermi level is consequently pinned by deep traps and V_{th} becomes more positive as expected for less ionized deep donor traps. It is interesting to note that the devices which are less impacted by these effects are those based on GaInP/GaAs [3], as shown by the results of Fig. 8. The second material choice, next to GaInP/GaAs for reduced V_T-shift is InAlAs/InGaAs and the least preferred is AlGaAs/GaAs. It is interesting to note that similar trends are observed in current-collapse and $g_m - V_{gs}$ characteristics which are strongly degraded for AlGaAs/GaAs but not for GaInP/GaAs upon cryogenic operation. The choice of GaInP instead of AlGaAs can thus eliminate such undesirable effects.

Substrate orientation is known to impact the degree of short-channel effects. This is traditionally attributed to piezoelectric charges generated in the FET channel owing to the presence of the dielectric–material hetero-interface. It has recently been reported [5] that other mechanisms such as stress at the refractory gate-metal–material interface can also translate to similar characteristics. This is demonstrated by the characteristics of Fig. 9, which are obtained for 5500 Å thick $WSi_{0.5}$ gates deposited along different orientations on to InAlAs/InGaAs HIGFET structures. V_T is reduced with gate length, demonstrating the presence of short-channel effects. Although no stress-induced piezoelectric effect is expected along the [001] direction, the negative and positive ΔV_T shifts in $[01\bar{1}]$ and [011] directions respectively suggest the presence of tensile stress. Experiments as a function of metal thickness support the presence of gate-metal–material stress and its impact on V_T variations. The semiconductor crystal properties and subsequent processing consequently play a significant role in the observed device characteristics of threshold voltage.

As discussed earlier, excess In in the n-channel of HEMTs results in improved device characteristics by better carrier confinement. In the case of p-channel devices the introduction of strain produces biaxial stress which lifts the zone-center degeneracy of the heavy-hole (HH) and light-hole (LH) bands. This results in a reduction of the in-plane hole effective mass and thus enhanced mobility. Figure 10 shows the mobility enhancement observed by introducing 10% In in the p-channel of $GaInP/In_xGa_{1-x}/GaAs$ HEMTs [6]. These characteristics were extracted by measuring the intrinsic transconductance g_m and sheet-carrier density P_s of FATFETs; the latter ensures long-channel conditions. Provided the device is biased in the linear region, one can then extract μ using the relation

$$g_{mintr} = q\mu P_s(W_g/L_g)$$

where g_{mintr} and P_s are estimated from $I-V$ and $C-V$ data respectively. What is also very important in the results of Fig. 10, is that under increased reverse gate bias the mobility enhances even further for strained devices, while it reduces the lattice-matched HEMTs. These features can be explained by the fact that a longer percentage of carriers occupies the light-hole band in strained designs owing to the upward movement of the Fermi level. This is not, however, the case for lattice-matched designs where the heavy-hole band lies on top of the valance band. Screening effects, analogous to MESFETs operated close to depletion, accentuate these characteristics and are dictated by the channel-buffer interface. One sees therefore that both intrinsic material properties, *i.e.* lift-off of zone-degeneracy and band splitting in p-strained channels, as well as properties related to the characteristics of neighboring layers (*i.e.* screening) are responsible for the observed device properties.

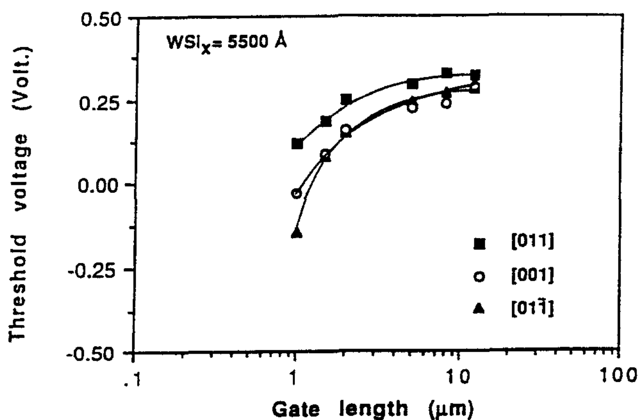

Fig. 9. Threshold voltage V_T shift as a function of gate-length for different gate orientations of InAlAs/InGaAs HIGFETs.

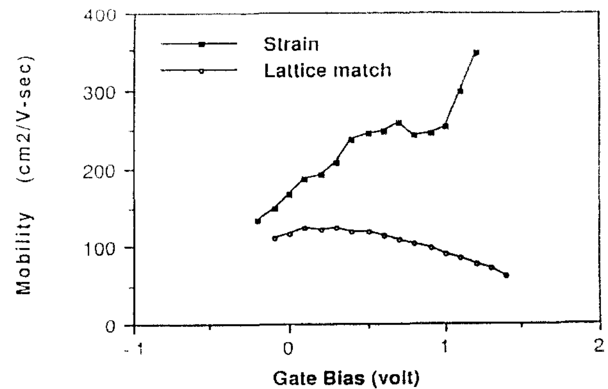

Fig. 10. Hole-mobility in lattice-matched ($x=0$) and pseudomorphic ($x=0.10$) $GaInP/In_xGa_{1-x}As/GaAs$ p-channel HEMTs as a function of gate-bias.

5. Reliability and processing issues

The device reliability is related to both material and processing. In the case of HEMTs gate metal diffusion may cause changes in ΔE_c and consequently changes in carrier confinement. Dopant diffusion from the donor layer to the channel can affect the transport properties as a result of increased impurity scattering. Trap generation at various layers and heterointerfaces may also affect the device performance.

Figure 11 shows the I_{ds}–V_{ds} characteristics of lattice-matched and strained InAlAs/InGaAs HEMTs before and after 1 h thermal storage 200 °C stress [4]. A substantial reduction in current is observed in both material systems and is accompanied by g_m degradation. Furthermore, an enhanced kink-effect is observed at low V_{ds}, particularly for the strained device. Studies of lattice-matched and strained devices suggest that the degradation mechanisms may differ in the two cases.

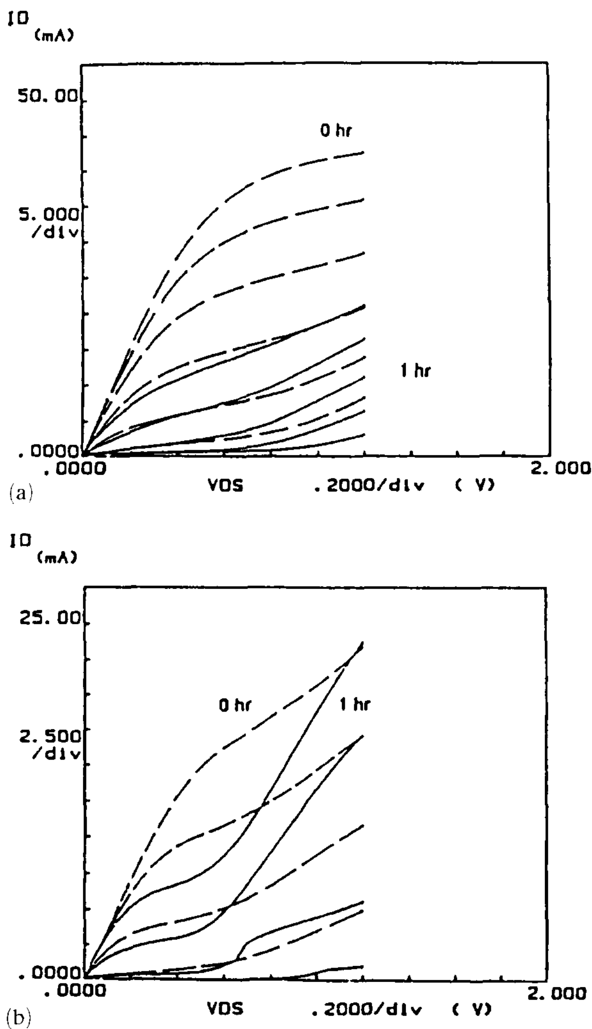

Fig. 11. I–V characteristics before (0 h) and after (1 h) stress of (a) lattice-matched and (b) strained InAlAs/InGaAs HEMTs.

For lattice-matched systems the mobility degradation was much more significant. This suggests a mechanism of degradation similar to that reported for AlGaAs/GaAs HEMTs by reduced carrier confinement due to a decrease in conduction band discontinuity [11]. In the case of strained HEMTs, it appears that enhanced trapping at the channel–buffer interface may be the main mechanism causing degradation.

The reliability study of devices such as AlGaAs/GaAs HBTs is a good example of how material growth and dopant choice can affect the device properties under stress. The prime HBT degradation mechanism is attributed to an electric-field assisted diffusion of interstitial Be dopant from the base into the emitter-base (E-B) heterojunction and is manifested by a decrease in d.c. current gain [12]. It is also interesting to note that such degradations are not observed in unbiased, temperature stressed devices. It turns out that the conditions of material growth and the choice of dopant can change significantly these characteristics. For example, reduced substrate temperature and increased As/Ga flux in MBE growth result in extremely stable HBT profiles [13]. Carbon instead of Be doping also seems to alleviate these problems.

As a final case, we discuss next the impact of RIE processing on material quality. Figure 12 shows the schematic diagram of an InP I-bar created by electron-beam lithography patterning for achieving I-bars with variable submicrometer dimensions and RIE etching using CH_4–H_2–Ar discharge [14]. Dry etching of this type is essential for reaching the base of InP/InGaAs HBTs. The creation of the I-bar (n-InP air-bridge) and absence of material under it allows elimination of parasitic conduction through undesired paths other than the InP itself and allows easier evaluation of side-damage by RIE. The study is based on current conduction through the I-bar and observation of drastic current flow changes for deeply damaged samples. The process parameters appear to have a significant impact on material quality and thus HBT characteristics. For

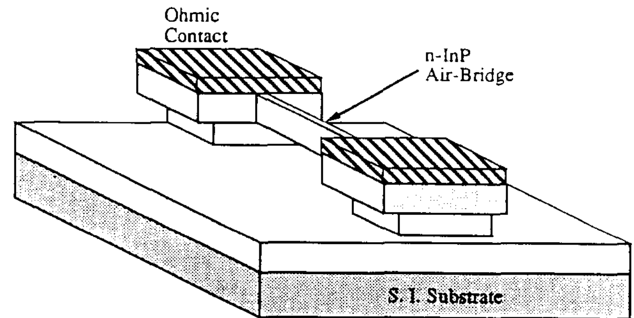

Fig. 12. Schematic diagram of submicrometer I-bar pattern used for evaluating RIE damage of InP during emitter etching of InP/InGaAs HBTs.

example, sidewall damage can be reduced by decreasing the RF power or increasing the power during the RIE process.

Overall reliability and processing are strongly correlated with material parameters as evidenced by studies of the properties of HEMTs and HBTs. Material growth, dopants and processing conditions therefore need to be optimized for best results.

6. Conclusions

Device optimization is strongly dependent on material properties which in their turn are determined, among other things, by the material system itself, growth conditions and processing. Device design should be strongly coupled with basic material considerations. Carrier confinement and improved performance can, for example, be accompanied by significant trapping related to DX-centers, as for example in the case of high Al-content AlGaAs. Cryogenic operation can be optimum (with no current-collapse or V_T shifts) using low DX-center content materials such as GaInP. Device structures are often the best choice for identifying the material properties responsible for their characteristics. Several examples of such use of devices have been presented and include g_m, R_{ds} dispersion and low-frequency noise. These parameters seem to be affected by common material properties, *i.e.* traps, the activation energies of which can be directly identified by device testing under variable temperature conditions. Electron trapping, substrate orientation and strain, together with substrate screening effects have been discussed. Reliability is dependent on material properties, as dictated by material choice and modification under stress, as well as growth conditions, dopants, etc. Finally, processing needs to be carefully optimized to avoid changes in material properties and thus device characteristics; RIE etching for reaching the HBT base is used as an example of the latter. Overall, material and device issues have to be treated together and strong interaction is necessary between the two areas for rapid advance and best results in semiconductor technology.

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