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NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
Section A

Characterization and radiation testing of the Harris HS9008RH flash analogue to digital converter

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Results from tests characterizing the performance and radiation hardness of the HS9008RH flash analog to digital convertor (FADC) are presented. These tests were performed primarily to evaluate the suitability of this device for use in the GEM Central Tracker at the SSC experiment. Basic performance characteristics and susceptibility of these characteristics to radiation were examined. Performance test results indicate that the device integral nonlinearity is sampling rate dependent and worsens rapidly above a sampling rate of 15 megasamples per second (MSPS). No degradation in performance of the device was observed after its exposure of up to 81 Mrad of 1.25 MeV γ radiation from a ^{60}Co source. Exposure of the device to a reactor fast neutron fluence ($E > 100$ keV) of $5 \times 10^{14}/\text{cm}^2$ resulted in no significant observed performance degradation as well.

1. Introduction

The Central Tracker of the GEM experiment at the Superconducting Super Collider (SSC) is currently in the design and development stage [1]. The Central Tracker is located within a radius of 1 m around the interaction region and consists of a silicon inner tracker surrounded by interpolating cathode pad chambers (IPC). Approximately 400 000 IPC channels of information must be processed at each 16 ns SSC beam crossing. Each channel is amplified and shaped. The charge from those channels containing information (the signal is above a certain threshold) is then placed upon holding capacitors for multiplexing to a FADC for digitization.

At least 8 bits are required to obtain the desired signal strength resolution. The FADC must also be able to operate at a sampling rate of 16 MSPS (one fourth of the 16 ns crossing time) in a harsh radiation environment and the devices should be able to withstand 10 years of operation at high luminosity ($L = 10^{34}/\text{cm}^2/\text{s}$). This is equivalent to a total of 2.5 Mrad of ionizing radiation and a fast neutron fluence of $5 \times 10^{14}/\text{cm}^2$.

It is important to test performance as a function of both ionizing and neutron radiation dose since the primary type of damage caused by the two forms of radiation is different. While both types of radiation contribute to both types of damage, neutron radiation is primarily responsible for displacement damage, and ionizing radiation is primarily responsible for electron–hole pair creation. The creation of electron–hole pairs by ionizing radiation results in a charge buildup at the insulator–charge carrier interface, causing threshold voltage offsets and/or shifts, leakage currents, and electron/hole mobility degradation. Displacement of the atomic components of the crystalline lattice occurs during neutron irradiation, resulting in increased dark current and charge carrier recombination. The macroscopic effects for this device would be a decrease in the signal-to-noise ratio and loss of resolution. Interestingly, the manufacturer expects some performance parameters to get better with irradiation due to the response of the AVLSI1RA rad-hard manufacturing process to radiation damage.

The Harris HS9008RH FADC is the only commercially available rad-hard device satisfying the number of bits and sampling rate requirements for which ready-to-test samples exist.

2. Device description

The HS9008RH is an eight-bit (255 counts, or "codes") conventional flash analog-to-digital convertor

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(FADC) rated initially at a maximum sampling rate of 25 MSPS, though partially as a result of our tests the manufacturer lowered this to 20 MSPS. It is fabricated in a radiation hard process called AVLSI1RA by Harris Semiconductor and described as a "dual level, twin well, thin EPI, 1.25 μm bulk CMOS process", and operates with a single fixed reference voltage, although a tap point at midscale is provided [2]. The device requires a single +5 V supply for power. All output signals are TTL compatible.

We obtained five of the devices in a standard 28 pin DIP package for initial testing. They were marked DV SAMPLE T22816-0 by the manufacturer and had serial numbers (S/N) 50, 51, 53, 54, and 55. Three additional samples were obtained later, and were marked DV SAMPLE R-21709, followed by a wafer number designation of 7, 10, or 11. These three chips come from a different wafer than the original five chips. Studying these chips was an opportunity to test wafer-to-wafer variations.

3. Test bench

The basic design of the Ames Laboratory/Iowa State University FADC test bench [3] is shown in Fig. 1. The VAXStation acts as the data processor and test initiator. It communicates via the GPIB interface with various signal generators and receives the digitized signal information from CAMAC modules via a SCSI data bus. The CAMAC clock/trigger module provides clock frequencies in the operating range of the HS9008RH of 10, 15, 17.5, 20, and 25 MSPS.

The device was tested with an evaluation board designed and built at the University of Michigan. The input signal was unbuffered and the ADC outputs were translated from TTL to ECL levels on the evaluation board. A digital-to-analog convertor (DAC) provided an analog signal for monitoring and debugging purposes.

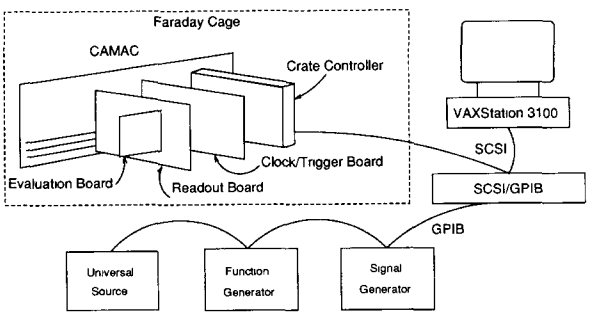

Fig. 1. Schematic drawing of the Ames Laboratory/Iowa State University FADC test bench. Tests are controlled by a VAXStation 3100, which communicates to a CAMAC data acquisition system and the signal generators via SCSI and GPIB data buses, respectively. The FADC is located on the evaluation board on the CAMAC readout module.

4. Tests performed

The test bench is designed to measure performance as proposed in IEEE Standard 1057, "IEEE Trial-Use Standard for Digitizing Waveform Recorders", July 1989. The tests we made on the devices can be categorized by the FADC input signal used to perform them. There are three major categories: DC tests, in which a DC signal is input to the device and the level varied slowly after each event record read; sine wave tests, in which the input consisted of a sine wave at various frequencies riding on a DC offset; and triangle wave tests, in which the input is a triangle wave on a DC offset. A fourth category of tests uses a variety of input signals and includes measurements of transient response and power consumption.

4.1. DC tests

The DC tests measure gain, offset, differential nonlinearity (DNL), maximum static error, integral nonlinearity (INL), monotonicity, and hysteresis. A series of event records are taken, each with a slightly increasing DC level input. The code transition points, the DC voltage at which the returned codes are distributed evenly between two adjacent values, are interpolated from the data. The ideal linear response for the device is determined by a straight line fit to the measured response. During these tests records are kept of individual code widths (in mV) and code transition point residuals from the ideal straight line response. The gain (in mV/ADC count) is the slope of the straight line fit, and the offset is determined from the fit as the lower edge of the first non-zero code. DNL is the deviation of the width of each code from the average width, expressed as a fraction of the average width. A DNL of zero means the code was of average width, a DNL of −1 means the code was missing, and a DNL of +1 means the code was twice as wide as the average. The maximum static error is the maximum deviation from linearity expressed in millivolts, and the integral nonlinearity (INL) is the maximum static error expressed as a percentage of full scale. Checks on monotonicity and hysteresis ensure that the response of the FADC is strictly increasing or decreasing.

4.2. Sine wave tests

In the sine wave tests a sine wave input is adjusted such that the sum of the sine wave and a DC offset covers 90% of the full scale of the FADC input range.

To obtain as pure a sine wave as possible, frequency filters are used on the signal generator output, limiting sine wave frequencies to certain discrete values. A single event scan is used to determine the signal-to-noise ratio, normalized peak error, number of effective bits, and total harmonic distortion. Multiple event records are used to determine fixed error in sample time and aperture uncertainty.

The signal-to-noise ratio is a measure of the accuracy of the reproduction of the input, and is found by a comparison of the data to a sine wave fit to the event record. In general, the value varies as a function of sampling rate and input frequency. The peak error is defined to be the largest difference in magnitude between the data and the fit, and is then normalized by three times the standard deviation of the fit. The number of effective bits and total harmonic distortion are other methods of expressing noise levels. The number of effective bits is less than the number of digitized bits, and is a useful way of expressing resolution with the effect of device noise and response included. The total harmonic distortion is a measurement of the component of harmonic signals in the measured signal, and is obtained from the results of a discrete Fourier transform on the data. The fixed error in sample time represents a nonrandom error in sampling time. The aperture uncertainty, or timing jitter, is the standard deviation of the repetitive sample time. The value reported is the standard deviation of the time errors computed from residuals of the sine fit, which represents an upper bound on the sampling time jitter. The actual timing jitter is less, since noise from sources other than timing jitter is included in the measurement.

The analog bandwidth is also measured with a sine wave input. The FADC has an analog bandwidth, which is defined as the input frequency range over which the gain of the device (output/input) is within -3 dB (a factor of 0.707) of its maximum value. A measurement of the gain is taken at several frequencies. As the frequency is increased, the frequency at which the gain has dropped by -3 dB of the maximum value is reported as the upper limit to the analog bandwidth. If no loss of signal at the -3 dB level is measured at the chosen frequencies, the largest frequency used is reported as the upper limit.

4.3. Triangle wave tests

The random noise level, word error rate, and another value for the DNL are measured with the triangle wave tests. The triangle wave is coupled with a DC input to provide the input signal. The DNL is measured by comparing the relative number of times each code is hit when the triangle wave covers the complete response range of the FADC. The random noise measurement is performed by comparing the code values returned by the FADC from two successive synchronized waveform digitizations.

The word error rate is an important measure of the fraction of digitizations which return an incorrect code value. In our tests, an incorrect code is defined to be a code which varies by more than two counts from the previous output code. A slowly varying triangle wave (varies by less than one count between digitizations) covering the complete response range of the device is used as input. A fixed number of digitizations and the number of incorrect codes are recorded. The word error rate is the ratio of errors to number of digitizations.

4.4. Other tests

Additional tests include measurements of the slew limit and short term settling time. Both of these tests are performed using a step function input. The slew limit is the point at which increased input voltage step causes no change in output code transition rate of change. The values are reported in volts per microsecond.

Short term settling time is found by measuring the time required for the device output to settle after a step function input to within one count of the output at a large time later.

Power consumption measurements are described in detail later.

5. Test conditions

We tested the device at sample rates of 10, 15, 20, and 25 MSPS using a symmetric clock. Some additional tests were performed on S/N 50 and 51 at 17.5 MSPS. Not all tests were done at all sample rates. For all tests the device was biased such that the input signals were kept within the range of 0.0 to 2.5 V. The data record length was 1024 samples and the analysis window covered samples 8 to 1022, inclusively. The midscale tap point was not used to set a bias, but tests showed that a 15 μF capacitor improved the INL near the tap point. Attempts to decrease the INL by tuning the tap point changed the shape of the FADC response but not the magnitude of the INL.

6. Performance tests results

At the start of our testing the Harris Corporation had not completely tested the device at sample rates greater than 10 MSPS. Some of these results were a surprise to them, and after performing their own tests they obtained similar results. Most of the sine wave

Table 1
Performance test results for HS9008RH S/N 50

Parameter	Units	10 MSPS	15 MSPS	20 MSPS	25 MSPS
Gain	mV/count	9.7736	9.6552	10.0958	10.17990
Offset	V	0.0118	0.0465	−0.0650	−0.0389
DNL (DC)	none	0.392	0.390	0.447	1.080
DNL (triangle)	none	0.237	0.320	0.397	0.614
Integral nonlinearity	% of f.s.	0.188	0.341	0.564	1.041
Maximum static error	mV	4.7083	8.4292	14.5791	27.1373
Code width RMS	counts	0.140	0.148	0.150	0.210
Monotonicity	none	yes	yes	yes	yes
Hysteresis	counts	0.000	0.000	0.000	0.25
Harmonic distortion	dBc	51.5	45.4	–	–
Signal-to-noise ratio	none	252.3	176.7	131.8	71.7
Effective bits	bits	7.9	7.3	6.9	6.0
Normal peak error	counts	0.906	1.175	0.948	1.071
Fixed error in sample time	ns	0.166	–	–	–
Aperture uncertainty	ns	< 0.324	–	–	–
Short-term settling time	ns	146.0	94.7	73.0	68.8
Slew limit	V/μs	19.9	29.1	41.1	51.1
Random noise	counts	0.062	0.061	0.069	0.095
Word error rate	none	0.00	0.00	0.6×10^{-6}	0.838×10^{-5}
Analog bandwidth	MHz	5.1	–	–	–

tests were performed only at 10 MSPS due to limitations in the linearity of the device (discussed below). Results of tests of a typical chip (S/N 50) are summarized in Table 1. Test results for chips 7, 10, and 11, which came from different wafers than chips 50–55, are similar.

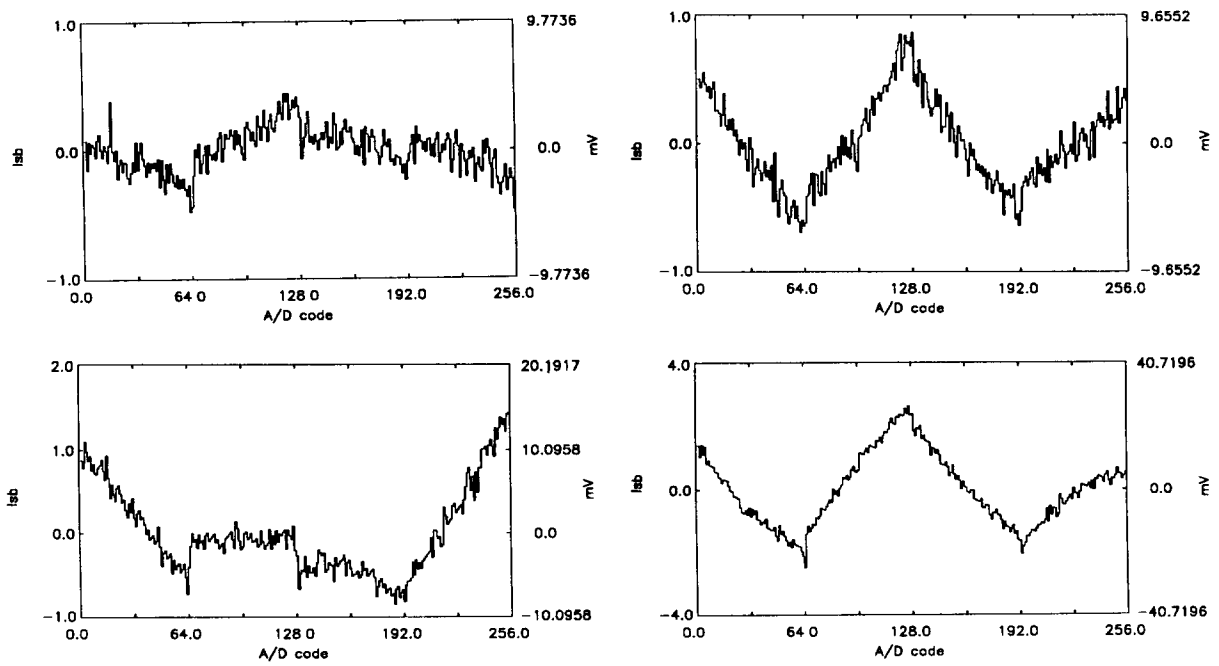

Fig. 2. The measured transition residuals for HS9008RH S/N 50 at (clockwise from top left) 10, 15, 25, and 20 MSPS in the DC tests. Note the changing response with sample rate. This behavior was observed in all samples. Note also the changing vertical scale.

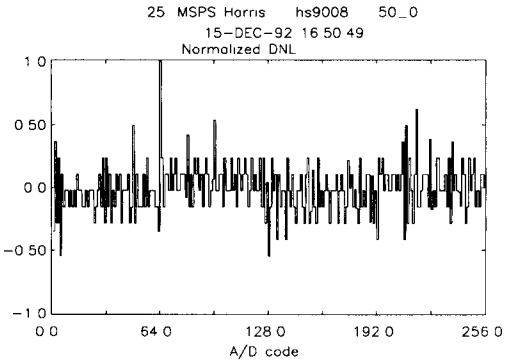

Fig. 3. A histogram of the measured differential nonlinearity (DNL) for the 255 code widths of chip S/N 50 measured in the DC tests at 25 MSPS.

6.1. Linearity

This device showed very peculiar behavior in the DC tests. The differential nonlinearity was excellent at low sampling rates and stayed that way for most codes even up to 25 MSPS. At the higher sampling rates a few codes, usually near a quadrant boundary, became bad and drove the worst case differential nonlinearity up to about one least significant bit (lsb, equivalent to one count or code). Despite this low DNL, the INL increased dramatically with sample rate due to the arrangement of the DNL. At 10 MSPS it had excellent linearity, both integral and differential. As we progressed to 15, 20 and 25 MSPS the shape changed dramatically and the worst case INL climbed to more than 1% of full scale. This can be seen in Fig. 2, which shows transition residuals from the linear fit. At 25 MSPS the worst values are wrong by more than 3.0 lsb. Close examination of the plots shows clearly that the response curve is broken into four very linear quadrants at each sample rate. Within each quadrant the code widths were very uniform, but there was a significant variation of the average width from quadrant to quadrant. A string of narrower than average codes accumulated over one quadrant is corrected for by a string of wider than average codes in another quadrant. The DNL plot (Fig. 3) for S/N 50 at a sample rate of 25 MSPS (where the effect is most pronounced) clearly shows the quadrant to quadrant average code width variations.

This nonlinearity could be corrected for in a hardware application in which offline processing of the data can take into account the response function. However, since at each sampling rate the response is different and unpredictable, and may vary from sample to sample, the response curves at the particular operating sample rate must be measured for each chip to insure proper correction. This nonlinearity severely affected our ability to perform tests which required a fit to an ideal input, such as the sine wave tests. This built-in nonlinear response at the higher sampling rates dominated function fitting errors.

No problems were observed with monotonicity or hysteresis.

6.2. Resolution

The number of effective bits was 7.9 for a low frequency input at 10 MSPS and decreased to about 6.0 at 25 MSPS for all input frequencies. The measured number of effective bits at the higher sampling rate is limited by the increasing nonlinearity discussed in the previous section. We also observed a loss of resolution with increasing signal frequency for fixed sample rate. This behavior is normal for flash ADCs, but the size of the effect was larger than for many other devices tested with this apparatus. We also observed that the total harmonic distortion became worse (i.e. the THD parameter decreased) at higher sample rates. Since the ratio of input frequency to sample rate is held constant during the THD measurement, a higher sample rate means a higher input frequency, so this decrease in THD is related to the loss of effective bits with increasing frequency.

The random noise from the triangle test was extremely low, less than 0.1 lsb at all sampling rates.

6.3. False codes

The qualified error level for this device was set to 2 counts, which means that steps of three or more counts were flagged as errors. We ran the word error rate test with an automatic stop at 100 errors or 2.0×10^7 samples, whichever came first. At low sample rates there were no word errors, but at 20 MSPS and above errors began to appear. A brief attempt to clock the chip at 30 MSPS (above the rated specification of 25 MSPS maximum) resulted in a 50% word error rate. In general, the errors were spread evenly among the ADC codes, but the size of the errors clustered around values that are powers of two, suggesting an incorrect bit in the answer to be the cause of the error. Typically, no errors were detected at 15 MSPS, while error rates varied from 0 to 10^{-6} at 20 MSPS.

One of the devices (S/N 51) had a weak code (number 69), which got worse as the sampling rate increased. At 25 MSPS this code was effectively dead and caused a large word error rate. An estimate of the word error rate could still be obtained by setting the qualified error level (QEL) to 3 counts, eliminating the errors flagged when the bad code was skipped. With the increased QEL the word error rate was comparable to that of the other devices.

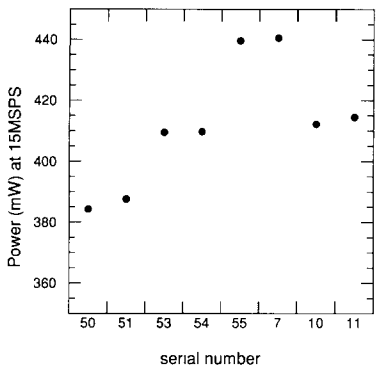

Fig. 4. Measured power consumption of the eight measured FADCs at 15 MSPS with a 2 MHz sine wave input.

6.4. Analog bandwidth

The analog bandwidth test was done only at 10 MSPS and showed the gain to be constant to within 10% up to a 5 MHz input signal frequency. (Note: 5 MHz is the Nyquist frequency for 10 MSPS. The Nyquist frequency is defined to be half the sampling rate. Input frequencies higher than the Nyquist frequency are not sampled frequently enough for tests utilizing a sine wave input to be meaningful.)

6.5. Transient response

The short term settling time at 25 MSPS was measured to be less than 70 ns. This must be treated as an upper bound because of limitations on the step signal source.

The maximum slew rate observed was 51 mV/ns. This should be regarded as a lower bound on the true value.

Sampling time jitter was only measured at the 10 MSPS rate due to the poor linearity of the device. The measurement places an upper limit of 0.337 ns on the sampling time jitter.

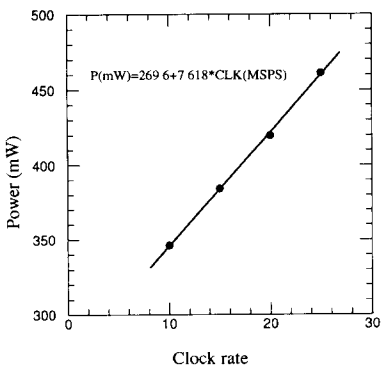

Fig. 5. Power consumption as a function of sample-rate with a 2 MHz sine wave input for S/N 50.

6.6. Power consumption

The power consumption of the chips was measured to see the effect of sample rate and radiation dose as well as to quantify chip-to-chip variations. Power was measured by monitoring the voltage drop V_R across a precision 2 Ω resistor placed in series with the 5 V power supply voltage. The power consumption of the chip was then determined as $P=(5-V_R)V_R/2$. For the eight chips measured, the average power required at 15 MSPS with a 2 MHz sine wave input covering the 10% to 90% code levels was 412.2 ± 20.5 mW (Fig. 4). Power consumption is very linear with sample rate between 10 and 25 MSPS (Fig. 5).

7. Radiation tests

The response of the device was measured with respect to radiation dose of both ionizing and neutron radiation. All irradiations were performed at the University of Michigan Phoenix Memorial Laboratory. Two of the devices (S/N 50 and 51) were tested for hardness against ionizing radiation utilizing an 18 kC ^{60}Co source. This source is able to deliver 2 Mrad per hour of radiation consisting chiefly of 1.25 MeV gamma rays. Tests were conducted at several irradiation steps between 0 and 81 Mrad. The maximum dose received by chip 50 was 36 Mrad, and that of chip 51 was 81 Mrad. These numbers are known to 5% accuracy. Neutron irradiation of the devices was performed at

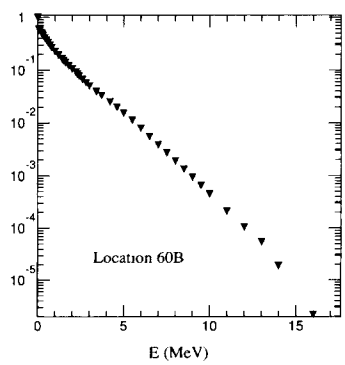

Fig. 6. Neutron integral kinetic energy spectrum $\Phi(E)=\int_E^\infty(\mathrm{d}\Phi(E')/\mathrm{d}E')\,\mathrm{d}E'$ for the Ford Reactor inside the MDRF as measured by the MDRF in the location used for the irradiations of chips 53 and 54. The spectrum is normalized to unity at 10^{-10} MeV. Note that approximately 56.6% of the total neutron flux has energy greater than 0.1 MeV.

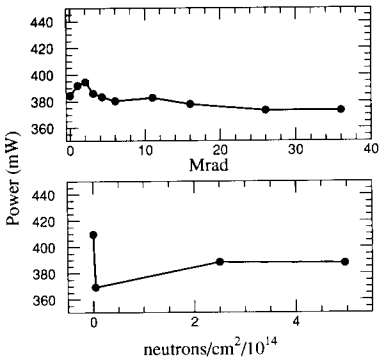

Fig. 7. Power consumption as a function of radiation dose at a sample rate of 15 MSPS and a 2 MHz sine wave input. Top: S/N 50 with ^{60}Co radiation; bottom: S/N 53 with neutron fluence.

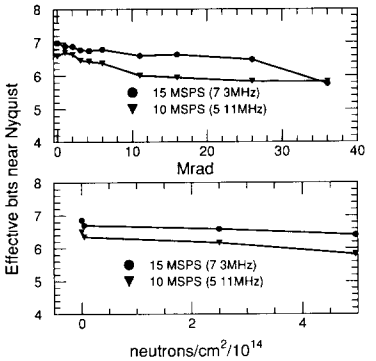

Fig. 8. Effective number of bits as a function of radiation dose at a sample rate of 10 and 15 MSPS and a 5.11 and 7.3 MHz sine wave input respectively. Top: S/N 50 with ^{60}Co radiation; bottom: S/N 53 with neutron fluence.

the Ford Nuclear Reactor, located in the Phoenix Memorial Laboratory. Two other FADC devices (S/N 53 and 54) received approximately 5×10^{14} fast neutrons/cm^2 ($E > 0.1$ MeV) in several steps.

The neutron irradiations were performed with the chips placed inside the Materials Dosimetry Reference Facility (MDRF) [4]. This facility has measured the neutron spectrum of the Ford Reactor in several locations near the reactor core. The displacement cross section of neutrons in silicon rises sharply to an essentially constant value at neutron energies of 0.1 MeV. The normalized neutron integral energy spectrum of the Ford Reactor as measured by the MDRF in the location for these irradiations is shown in Fig. 6. The total neutron flux above 0.1 MeV is 1.83×10^{11}/cm^2/s at a reactor power of 500 kW, the operating power for these irradiations, and is measured to an accuracy of about 10%. A total of approximately 1.5 Mrad of γ-ray background was received during the neutron irradiations [5].

The cumulative ^{60}Co irradiation steps for S/N 50 were 0, 1, 2, 3, 4, 6, 11, 16, 26, and 36 Mrad. For S/N 51, they were 0, 1, 2, 3, 4, 6, 11, 21, and 81 Mrad. The cumulative neutron fluence received by S/N 53 during the tests was 0, 4.2×10^{12}, 2.537×10^{14}, and 5.032×10^{14}/cm^2.

The tests showed that the devices are quite radiation hard. They were able to withstand all of the above radiation without significant degradation. The performance of the devices showed essentially no change after each irradiation step.

The power consumed by the chip did not change significantly with exposure to radiation. Fig. 7 shows measurements of the power consumption of chip 50 with increasing dose for ionizing radiation and chip 53 for neutron radiation. Power consumption decreases sharply for small neutron doses but increases to the original value with further irradiation.

Both the effective bits and the total harmonic distortion were measured as a function of radiation dose. The number of effective bits as a function of dose for chips 50 and 53 at 15 MSPS are shown in Fig. 8. No significant changes were observed, though a general loss of resolution seems evident. Note that at higher sampling rates measurements of effective bits and total harmonic distortion are limited by the INL.

It is extremely significant that the word error rate did not increase with radiation dose (Fig. 9). In fact, a slight decrease is noted for both the ^{60}Co and neutron irradiations at small doses with a gradual increase to the original value as dose increased. Also, for chip S/N 51, no change in the behavior of the bad code was noticed as dose level increased, even at 81 Mrad.

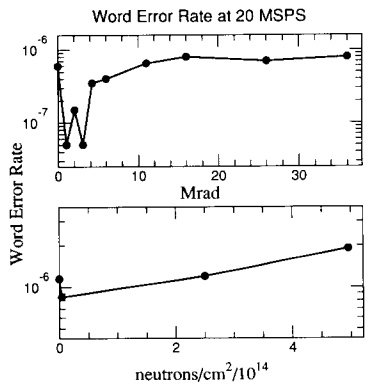

Fig. 9. Word error rate as a function of radiation dose at a sample rate of 20 MSPS. The measurement is the result of 100 errors or 2.0×10^7 digitizations, whichever came first. Top: S/N 50 with ^{60}Co radiation; bottom: S/N 53 with neutron fluence.

8. Conclusion

At 10 and 15 MSPS this device performed excellently. The INL, DNL, and effective number of bits were outstanding and there were no false codes in 2.0×10^7 digitizations. By 25 MSPS, however, the performance was terrible. The INL was at the level of 3 lsb and the effective number of bits had dropped to 6.0. The false code rate had climbed to one error per 10^5 digitizations. While the change in measured INL between sample rates was fairly consistent between chips, the mode of the change followed no simple pattern. It is probably not possible to predict the INL for a particular sample rate from data of surrounding sample rates.

The device is extremely radiation hard. It showed no significant changes in performance after 81 Mrad of 1.25 MeV γ radiation from ^{60}Co, nor after 5×10^{14} fast neutrons/cm^2.

Acknowledgements

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