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Section A

The CDF Silicon Vertex Detector

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A silicon strip vertex detector was designed, constructed and commissioned at the CDF experiment at the Tevatron collider at Fermilab. The mechanical design of the detector, its cooling and monitoring are presented. The front end electronics employing a custom VLSI chip, the readout electronics and various components of the SVX system are described. The system performance and the experience with the operation of the detector in the radiation environment are discussed. The device has been taking colliding beams data since May of 1992, performing at its best design specifications and enhancing the physics program of CDF.

1. Introduction

The CDF detector was built to study the collisions of protons and antiprotons at the Tevatron collider. It is a multipurpose detector dedicated for precise measurements of the particles produced at $\bar{p}p$ collisions. During the period between 1989 and 1992 the CDF detector was upgraded in order to extend its sensitivity to new physics. As part of this upgrade a new silicon microstrip vertex detector (SVX) was designed and constructed. The SVX is the first device of this kind to be operated at a hadron collider. It should allow identification of secondary vertices from the long lived particles ($\tau \approx 10^{-12}$ s). Of particular interest is a measurement of the properties of B mesons produced either directly in the proton–antiproton collision or from the subsequent decay of a top quark.

The mechanical design, front end electronics and cooling of the SVX are presented in section 2, the data acquisition electronics is discussed in section 3, the initial performance results are shown in section 4 and experience gained during almost 1 year operation in high radiation environment is presented in section 5.

2. SVX geometry and design

The CDF SVX detector [1–3] was designed under the rigid requirements imposed by operation at a

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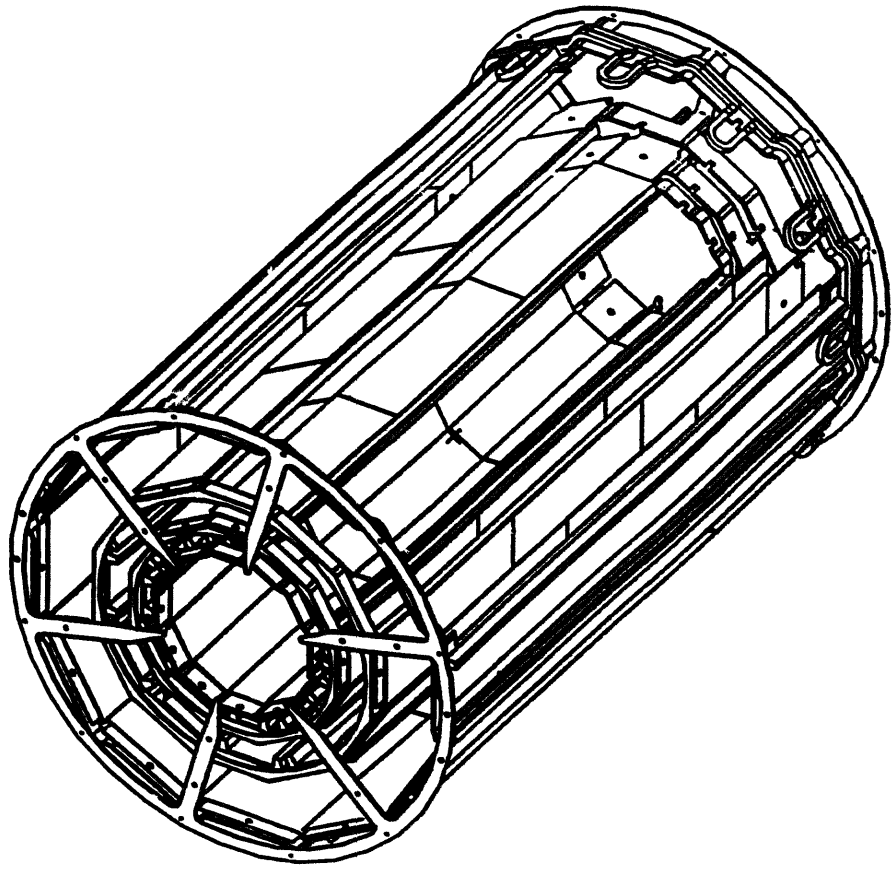

Fig. 1. Schematic view of one barrel of the SVX detector, showing the internal geometry.

hadron collider. These constraints immediately forced certain design choices. At the Tevatron collider, the $\bar{p}p$ interactions are distributed along the beam line with $\sigma = 35$ cm. Thus a long detector, shown in Fig. 1, is required for good event acceptance. The SVX detector is 51 cm in length and will contain $\sim 60\%$ of the $\bar{p}p$ collision vertices. The amount of material used to construct the SVX was kept to an absolute minimum, to reduce particle decays within the material and to decrease multiple scattering, both of which limit the accuracy of secondary vertex measurements and cause backgrounds to other detectors. The materials used

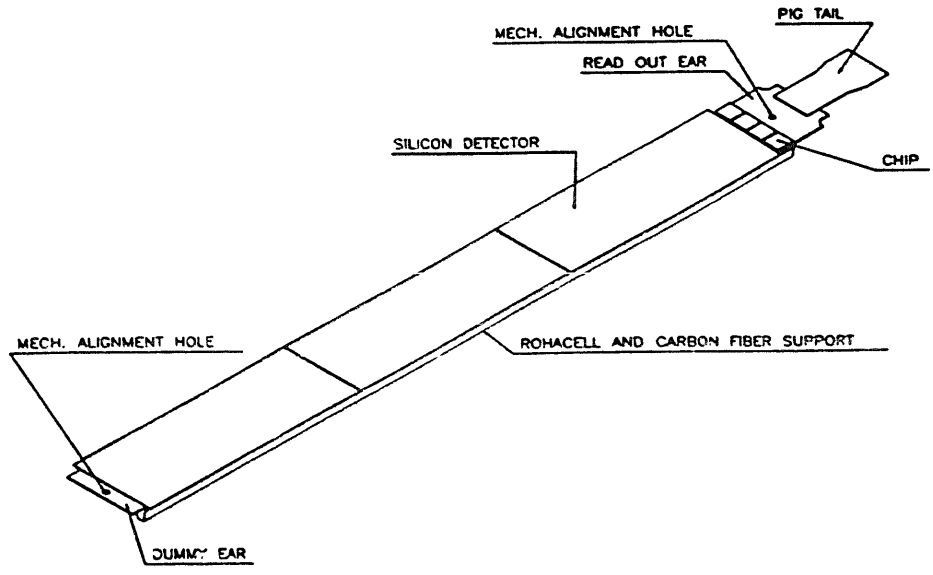

Fig. 2. Components of an SVX ladder.

also needed to be mechanically stable and resistant to the relatively high radiation in which the detector operates.

The SVX detector consists of two barrel modules placed end-to-end which are centered on the nominal interaction collision point and whose axes are coincident with the beam axis. One of the barrels is shown in Fig. 1. Each barrel consists of four concentric cylindrical layers. The layers are placed between 2.7 cm and 7.9 cm distance from the beam line. The inner layer was placed as close to the beam as allowed by the beam pipe.

The DC-coupled silicon microstrip detectors are 8.5 cm long and 300 μm thick and have a strip pitch of 60 μm for the three layers nearest to the beam and 55 μm for the fourth layer [4]. The detector width increases with radius to provide a wedge geometry which points back to the beam line. Three silicon microstrip crystals are glued to a low weight Rohacell [5] foam and carbon fiber support together with ceramic readout hybrid circuit board (an "ear card") and a passive hybrid. Such a structure is called a ladder, shown in Fig. 2. At the interface between the silicon microstrip detectors, wire bonds electrically connect the strips between the adjacent detectors. Silicon microstrips run along the length of the ladders and provide tracking in the r–ϕ plane. At the interface between the first silicon microstrip detector and the ear card, wire bonds connect each strip to an input of a custom designed integrated circuit (the SVX IC). The effective length of a ladder is 25.5 cm. The ladders are arranged in a 12-sided geometry. A 30° section is called a wedge. Ladders are supported at the ends by beryllium bulkheads. The total number of ladders in the SVX detector is 12 wedges × 4 layers × 2 ends = 96 ladders or 24 ladders for each layer. In its final mounted position in the barrel, each ladder is rotated by 3° around its length in order to allow overlap between adjacent ladders and to minimize azimuthal boundary gaps. Finally, an electrical shield closes the entire barrel assembly.

2.1. SVX front end electronics

The SVX IC has been described in detail elsewhere [6,7]. Its current version was fabricated using 3-μm feature size CMOS technology and has both digital and analog sections. The analog section contains 128 channels of charge integrating amplifiers followed by sample-and-hold and threshold storage stages. The digital section contains logic for data sparsification and serial readout. Digital lines are used bi-directionally to receive signals controlling the operation of the amplifiers and the switches, and to send signals containing channel address and chip identification. An analog signal line is used to send the pulse hight of channels during readout. The SVX IC allows the setting of a sparsification threshold by receiving a calibration pulse into 128 capacitors connected to the input of each channel and storing the associated charge on a threshold storage capacitor. The chip can be operated in double or quadruple correlated sample-and-hold integration schemes.

The ear circuit board mounted on the ladder contains the SVX ICs on a thick-film aluminum nitride substrate, which was used to provide good conduction of the heat from the chips to the cooling system. Ear cards carry signals to and from the SVX ICs and provide necessary interconnections which allow the chips within a wedge to be daisy chained. The ear cards also have resistors to set the bias current in the chips, and capacitors to filter noise on the bias voltage lines.

Other hybrid circuit boards (the port cards) are mounted on the bulkheads. These multilayered boards interface signals between the ear cards and the data acquisition electronics. The port card uses digital drivers and receivers for data transmission. An analog differential driver circuit drives the pulse height information from the microstrips. The port card has two circuits which provide pulses for setting the threshold or for chip calibrations.

The readout cable (a "pigtail") attached to the end of the readout ear board incorporates a "gold-dot technology" [8] to make electrical contact to a mating bus cable. This bus cable connects four ladders in a wedge to the port card. Small bumps of gold have been deposited on the traces at the end of the flexible Kapton pigtail cable. These bumps mate with pads on the bus cable, using a lightweight G-10 clamp fastened with a small bolt and nut. The interconnect pitch has traces on staggered 1-mm centers, giving an effective 0.5-mm pitch. This connection scheme allows easy assembly of the cables and works better than the conventional pin and socket arrangement by providing complete flexibility in the number of traces and in the cable layout.

2.2. SVX cooling system

The goal of the low mass SVX cooling system is to remove heat from the readout electronics in the SVX detector and to intercept heat from the surrounding tracking chamber electronics in order to keep the silicon strip detectors and the mechanical structure of the barrel at the ladder installation temperature of 20°C. This is necessary to avoid the increase in silicon strip leakage current from higher temperature operation and to minimize thermal gradients in the internal detector structure, so that the initial high-quality mechanical alignment can be maintained. Approximately 50 W of heat is generated by the electronics in each half of the SVX.

The cooling pipes carrying chilled water at 14°C are in thermal contact with the beryllium bulkhead and run underneath the ledge on which the readout circuit boards are mounted. An additional cooling circuit was used to remove heat from the port card.

In addition to the water cooling, gas cooling was introduced at the opposite end of the SVX detector in order to reduce thermal gradients across the detector, since most of the heating and cooling occurs only at the readout end. In order to be compatible with the surrounding tracking chamber gas, argon–ethane gas is pre-cooled to 7°C in a heat exchanger before delivery at a flow rate of 10 Standard Cubic Feet per Hour to each barrel. As a special safety measure, the system operates at sub-atmospheric pressure inside the CDF detector volume. If a water leak was to occur, the result would be the gas entering the system rather than water leaving it, which would be immediately detectable.

2.3. Monitoring and interlock systems

The SVX has extensive monitoring and interlock systems for its protection. Temperature probes are mounted at various locations on each barrel to monitor the temperature profile along the silicon detectors. Transducers are integrated into the system to monitor the flow rate of chilled water into the SVX barrels. Signals from the monitoring devices are fed into a programmable interlock computer which shuts off various components of the SVX system whenever an abnormality or a malfunction are detected.

3. Data acquistion system

The SVX DAQ system was required to integrate into the existing hardware, software and maintenance structure of CDF. It had to contain sufficiently parallel structure and bandwidth not to introduc any additional deadtime into the CDF readout. Finally it had to provide the required timing and control signals and diagnostic capabilities needed by the front end readout chips.

3.1. System architecture

The architecture of the SVX data acquisition system was determined by the SVX detector design, the operation of the SVX chips and their need for a variety

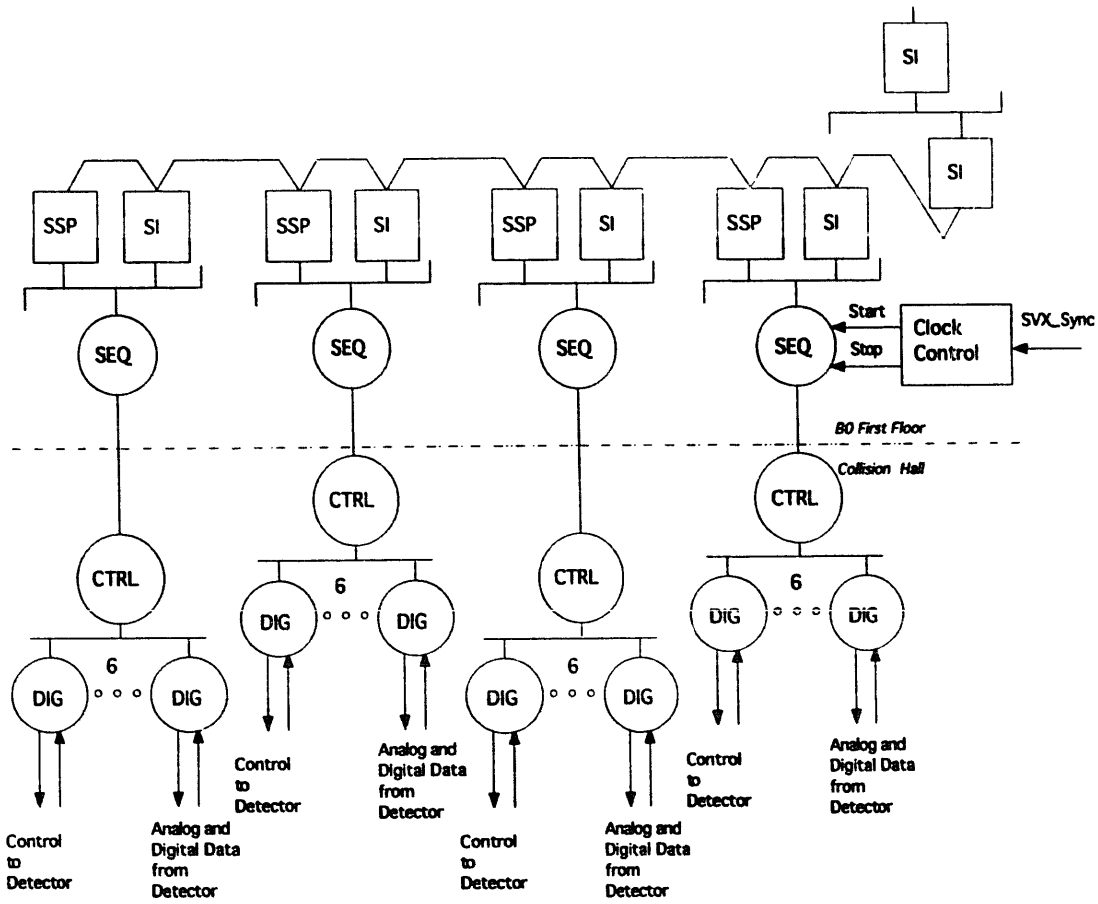

Fig. 3. SVX DAQ system diagram.

of clocking sequences, the required readout speed and the existing CDF data acquisition network [9]. The system consists of a Fastbus Sequencer, Crate Controller and Digitizer modules. Additional details can also be found in the literature [10–12].

The standard interface to the CDF data acquisition system is provided by a SLAC Scanner Processor (SSP) [14], a commercial product that is used extensively in the CDF network. It is a programmable Fastbus master that can reformat the event data and attach header information. It has adequate memory to buffer four events, a feature used in certain calibration modes.

The Sequencer, a Fastbus slave, is a programmable module which provides the clocking signals necessary to operate the SVX chips, synchronization logic to link to the CDF data acquisition system, and sufficient memory for one event as a pipeline to the SSP. The Controllers and Digitizers are housed in SVX Rabbit [13] crates on the CDF Central Detector. The Controller provides the interface between the Digitizers and the Sequencer. The Digitizers process analog data and buffer digital data from the wedges. They are read out by the Controller. The CDF SVX detector was instrumented with four Fastbus crates and four SVX Rabbit crates each with six Digitizers to accommodate 24 SVX wedges, as illustrated in Fig. 3.

3.2. Control and data flow

The Sequencer can read from and write to both the Digitizers and the Controller. It is also possible to direct the read information out a front panel port on the Digitizers so as to operate with a standalone online monitoring system. The primary mode for reading out wedge data is via automatic scans in which the Controller reads the wedge data register in each of its Digitizers reporting the presence of data.

Twelve signals control sample-and-hold operations within the amplifiers as well as the event readout. During beam crossings, the SVX timing signals pass from the Sequencer through the Controller and Digitizer to the wedge. Sample-and-hold operation is synchronized with the 3.5-μs beam crossing interval. During readout, the timing signal drivers turn off, and the digitizer accepts the chip and channel addresses along with the analog data from the wedge. The Sequencer also issues a convert signal telling the ADC on the Digitizers when to begin the hold and digitize cycle. Once the data for a channel have been prepared by the Digitizers, readout can commence. The Controller is commanded by the Sequencer to initiate a scan read. In this mode the Controller will poll each Digitizer and only send data to the Sequencer for those Digitizers

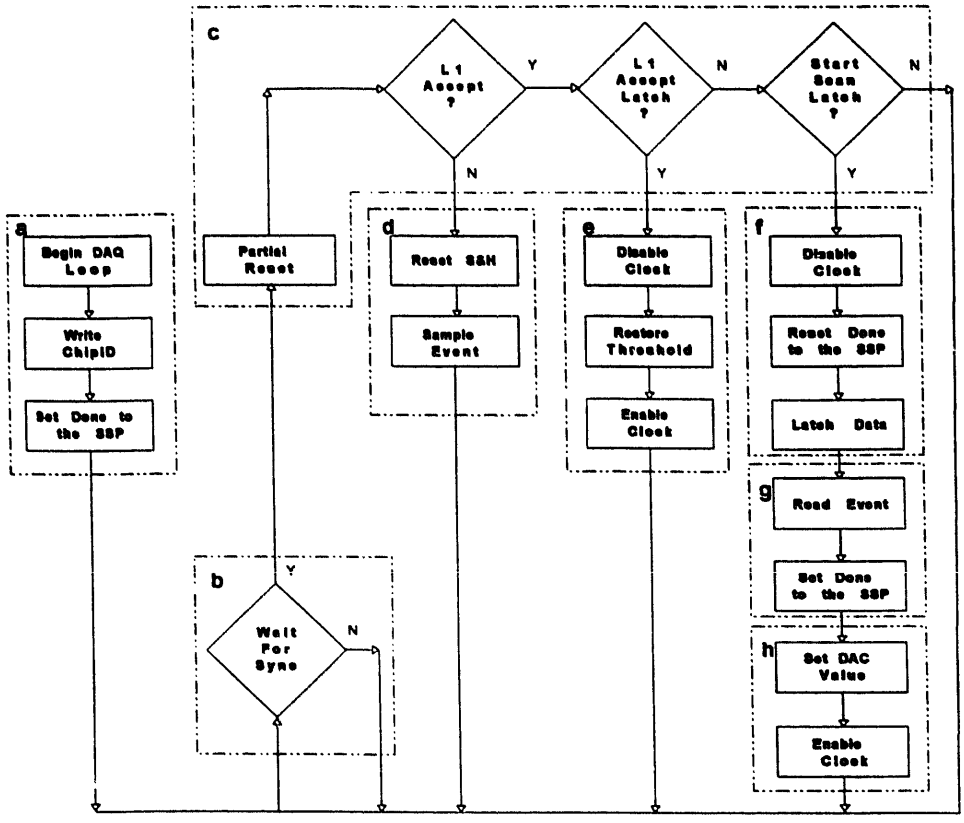

Fig. 4. The SVX microprogram functional block diagram. The dashed rectangles represent program modules used in the code generation. The module names are as follows: a: Initialize; b: Synchronize; c: Branch; d: Sample and Hold; e: Threshold; f: Latch; g: Readout; h: Injq.

which have responded that they have data. The SVX ICs will normally be programmed to provide sparsified data which will cause the Digitizers to stop responding as each wedge becomes empty. The Sequencer monitors the presence of data in the wedges and terminates the readout after all the wedges have been emptied. A 32-bit Read-Data path from the Digitizer to the Sequencer carries data during a read or presents data status from each Digitizer when a read is not in progress. Both the data and their status can be masked

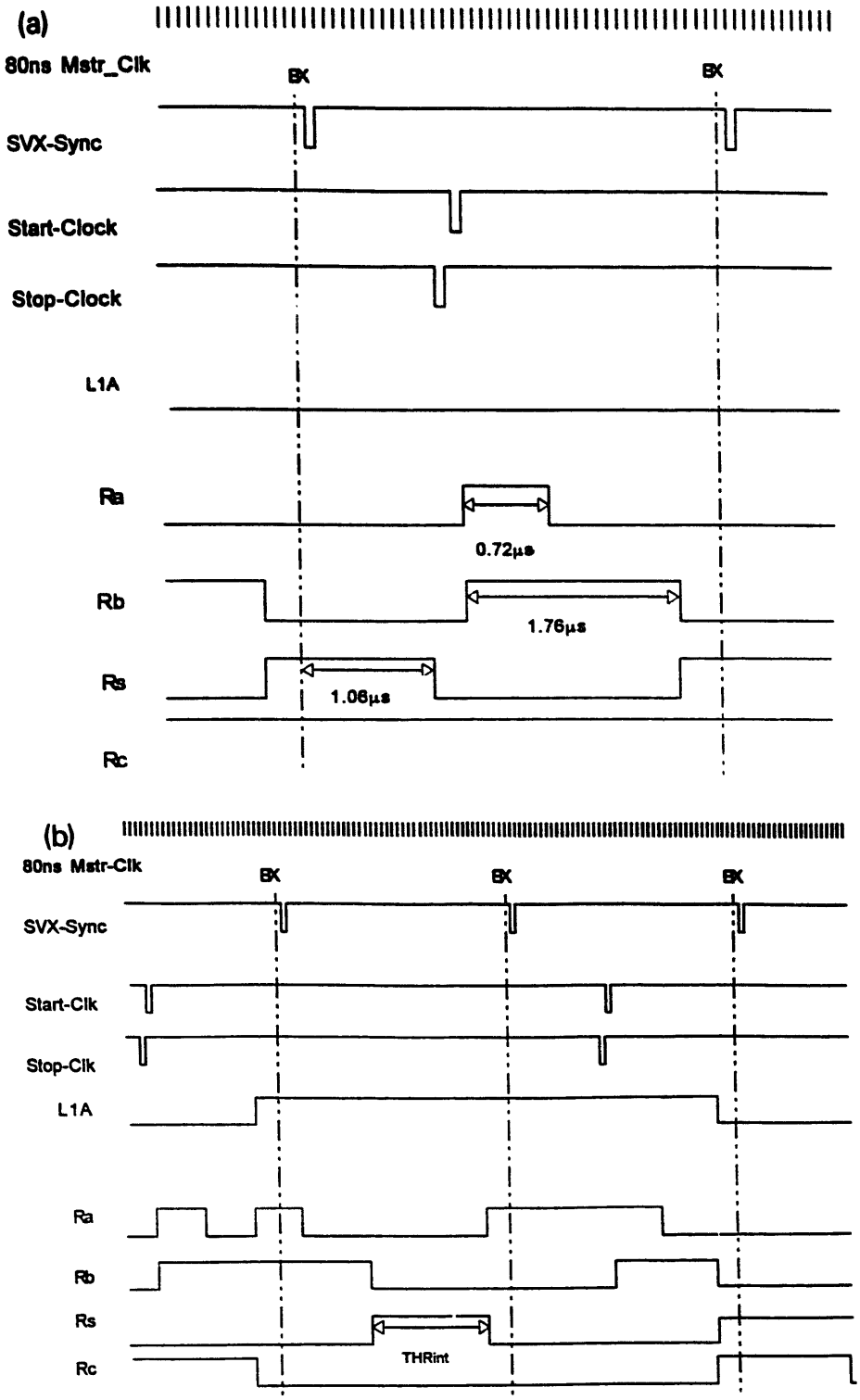

Fig. 5. (a) Synchronization of the Sequencer's operations with the beam crossings and the CDF DAQ network. (b) Threshold restoration cycle performed between the beam crossings.

off. The data from any wedge can be masked in the Controller and data status is maskable in the Sequencer.

A compact data format was used to describe the digital and digitized analog output from the SVX chip. Each hit is described by one 32-bit word. The control registers are read from the Digitizer or Controller modules using the same format as for the hit information. Data from all the Digitizer and Controller registers are read out with every event and appended to the raw data for diagnostics and calibration purposes.

The algorithms for the readout of the SVX Sequencer include data acquisition and data calibration modes. During data acquisition and data mode calibration every event is read out to a disk. In scanner mode calibration the raw data words from the Sequencers are sent only to the SSPs. For each channel the scanner accumulates the sums of relevant quantities as well as the number of events read. After collection of the predefined number of triggers, the data accumulated by the SSP are sent the rest of the way up the DAQ chain to be further analyzed by calibration consumer processes. This method of calibration runs much faster than in the data mode because it reduces the number of data transfers and uses the computing power of the SSP.

3.3. Synchronization with the CDF DAQ

The operation of the SVX chip is performed by an ensemble of timing signals generated by the Sequencer module in phase with the Tevatron bunch crossing times. For this reason the Sequencer has to be synchronized with every beam crossing. The method also minimizes the impact of the jitter of the Sequencer's internal clock on the precise timing of the event and threshold integration times. The operation of the SVX Sequencer is linked to the various level trigger decisions generated by the CDF data acquisition system [15].

In Fig. 4 an example of the microsequencer program block diagram is presented, performing an event acquisition during the collider run. The program starts with the downloading of the chip identification numbers to the chips' memories and reading them back for the diagnostic purposes. This part of the program is executed only once. Then the Sequencer's clock is shut off, waiting to be synchronized with the next beam crossing. After receiving the start clock signal, the Partial Reset procedure is executed in which only the chip integrator is reset and the events sampled in the previous crossing are kept on the Sample and Hold capacitor. Then a check is made of the first level, L1, trigger decision signal.

The absence of the L1 trigger signal is an indication to integrate a new sample. When the integration cycle is finished the Sequencer's internal clock is stopped by the next stop clock signal and the synchronization with the next beam crossing takes place. The following start clock signal enables the operation of the internal clock again and the Partial Reset is performed. There are 43 80-ns microsequencer's instructions executed between the Start-Clock and Stop-Clock sequence. The total number of instructions in that cycle is shared between the Partial Reset and the Integration subprocesses and the exact numbers depend on a particular implementation. In one of them the integration time requires 19 of these instructions, and low noise constraints applied to the reset operation demand another 22 instructions. In the remaining two instructions the Start-Clock and L1 trigger signals are checked. The Sequencer's ability to select and check the separate conditions on each microsequencer instruction allows us to execute the full event sampling cycle.

The presence of the L1 trigger signal indicates that the event stored during the previous crossing passed the L1 trigger conditions and the event may be prepared for readout. In this case a threshold sample is taken, which is used to cancel the leakage current component in the event sample. The event sampling and the threshold cycles must be executed with the full knowledge of the beam crossing. In the first case the beam crossing should appear inside the integration window (see Fig. 5a), and in the second one the integration must be performed between the beam crossings (see Fig. 5b). The threshold restoring subprocess requires two beam crossings to be performed with the constraints defined above. The microsequencer program inhibits generation of the Stop-Clock signal at the LRS4222 module during the threshold cycle. When the threshold is restored, the synchronization mechanism is enabled again.

In the next step a test of the Level 2 trigger decision is done. Its presence initiates the readout cycle and its absence directs control to the synchronization subprocess. For non-triggered events, a separate integration cycle is performed in the very next Start/Stop clock cycle.

3.4. Scan times

All detector elements in the CDF data acquistion system are required to be read out within 2 ms. Due to the large number of channels it was necessary to partition the SVX into four independently read branches (see Fig. 3). The scan time is defined as a sum of two components: the time required to read SVX chips in six wedges by the Sequencer and the time to move data from the Sequencer's Event Memory to the SSP's buffer.

The Sequencer scan time is proportional to the number of hits multiplied by the sum of the duration of the basic chip data cycle, called HiLo, the response of

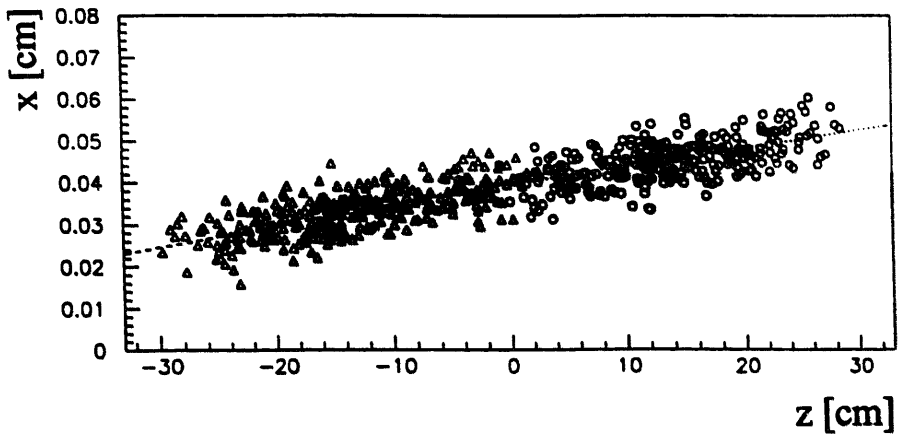

Fig. 6. Reconstruction of the beam profile using SVX tracks. The beam position along its direction is shown. Open circles (triangles) correspond to tracks found in East (West) barrel.

the front end modules, signal propagation delays and the time required by the Sequencer to check that all the data are read out from wedges. The time required to move data from the Sequencer to the SSP was measured and it corresponds to a block transfer rate equal to 200 ns per 32 bit word.

The SVX chip has the ability to sparsify the data and read only channels above the threshold. The number of hits per interaction is a function of the following factors: event multiplicity, noise fluctuations above the threshold settings, uniformity between chips in a wedge, number of low momentum spiral tracks and beam gas interactions. The average occupancy was estimated not to exceed 10% of channels which corresponds to a scan time of 0.77 ms, well below the maximum value allowed. For a fixed threshold, this number is expected to increase slowly as a function of the absorbed radiation dose by the detector components, mainly due to the increased number of noisy channels with high leakage current value that will result.

4. Detector performance

Trajectories in the SVX are found by extrapolating tracks reconstructed in the Central Tracking Chamber (CTC). The algorithm associates SVX hits, one at the time, to an existing track found in the CTC. At each iteration a new fit of track parameters is made including the contributions from the multiple Coulomb scattering. The algorithm progresses from the outer to the inner layers. Tracks having at least 3 hits associated with it are saved.

A great care was taken during the mechanical construction of the SVX detector to ensure high precision of assembly. The SVX detector was aligned to the CTC using a beam line as an external reference (global alignment) and the ladders were aligned internally within each barrel. In Fig. 6 a distribution of the x coordinate as a function of the z position of the primary vertex is shown. Independent fits to the beam line for each of the two barrels were performed and showed an agreement to be better than 5 μm between the barrels. The small slope of the beam lines (3 μm/cm) was also measurable.

The track residuals in the SVX obtained after application of the alignment constants are shown in Fig. 7. A sample of tracks with momentum greater than 3.5 GeV/c and having 4 hits registered in the same wedge of the SVX detector was selected. The width of the residual distribution was found to be close to 10 μm. It corresponds to a detector spatial resolution of 13 μm.

The tracks for which the SVX information was used improve the invariant mass distribution. In the case of

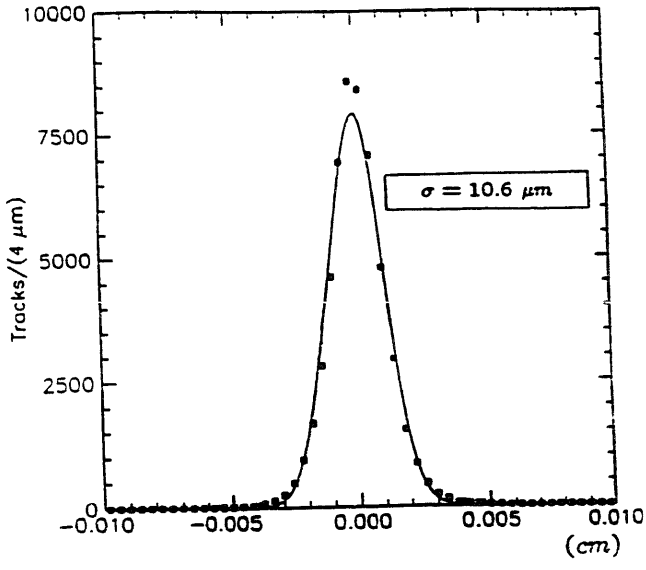

Fig. 7. Distribution of residuals for the tracks reconstructed using the SVX information.

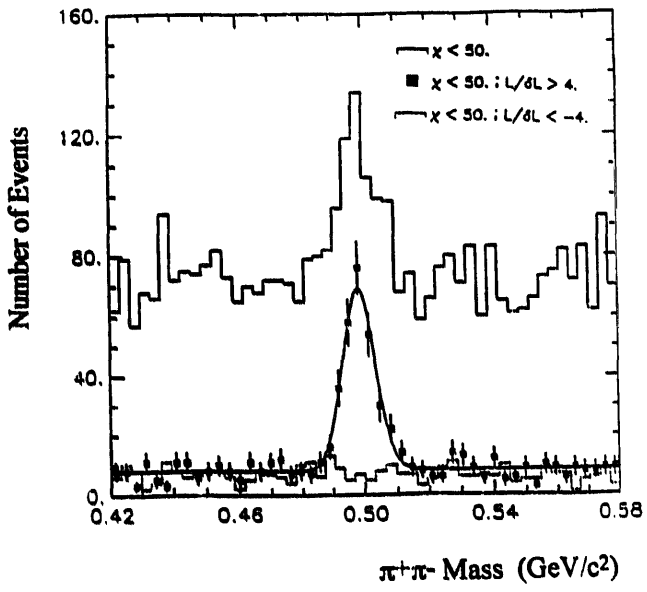

Fig. 8. Reduction of the combinatoric background using SVX tracks in the invariant mass distribution of pairs of tracks considered as decays of $K_s^0 \rightarrow \pi^+ \pi^-$.

J/ψ decays into a pair of muons the width was reduced by about 30%. The high precision of the SVX track information is shown in Fig. 8 where the combinatorial backgrounds are reduced after a 4σ cut was applied on the decay length, L, of the K_s^0 candidates. The continuous histogram represents the invariant mass distribution before the cut on L. Points (filled squares) with a fitted signal and background parametrizations correspond to the distribution after the cut was applied. The dashed histogram shows all combinations for which the calculated decay length is negative and smaller than 4σ.

5. Radiation monitoring of the SVX detector

The high luminosity and the proton antiproton cross section at a hadron collider mean that the SVX will be exposed to radiation coming from the physics processes and operational beam losses. The inner most layer, located at 3 cm from the beam axis, is the most vulnerable. The potential high beam loss conditions, in conjunction with the radiation soft technology used in construction of the SVX detector, required the design and implementation of a dedicated loss monitoring system which would minimize any accidental radiation dose.

Preliminary measurements of the radiation levels made in the CDF collision hall were already made during the 1988–1989 run. The results varied as a function of time and were approximately 900 rad/pb^{-1} at the early stages and declined to the level of 300 rad/pb^{-1} as the run condition stabilized. At the start of the 1992–1993 Tevatron Collider run, the expected 25 pb^{-1} of delivered luminosity would lead to an integrated dose of 12 krad. Such a dose could have an impact on the performance of the microstrip detectors and front end readout.

Radiation backgrounds are monitored with two systems [17] located symmetrically about 2.8 m from the interaction region and a distance of 5 cm from the beam axis. Silicon diodes are used to measure the minimum ionizing particle rates and the Tevatron Beam Loss Monitors [18] are used to measure the ionizing dose levels. In addition to the rate and dose information, arrays of thermoluminescent dosimeters (TLDs) are installed in the location of the other monitoring devices. The TLDs provide the radial dependence of the radiation dose, which drops off as $\sim r^{-1.75}$.

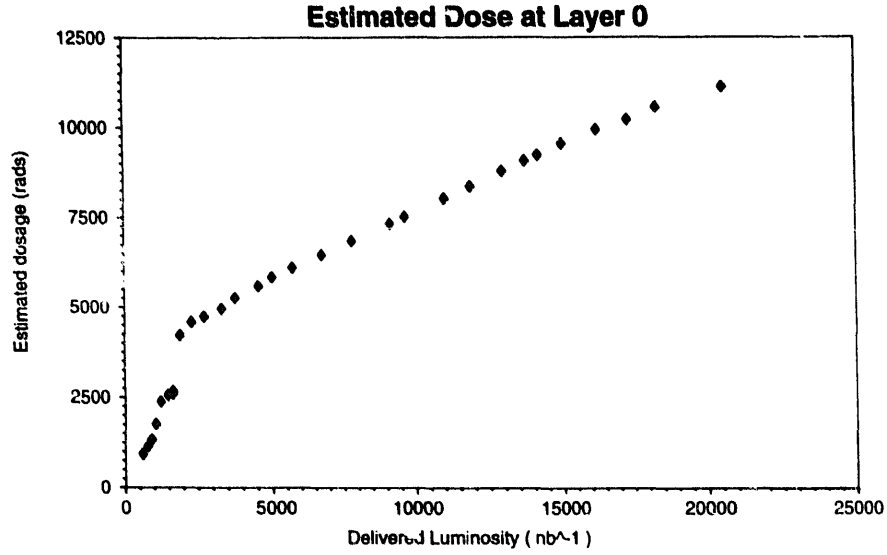

Fig. 9. Extrapolated inner layer radiation dose as a function of delivered luminosity.

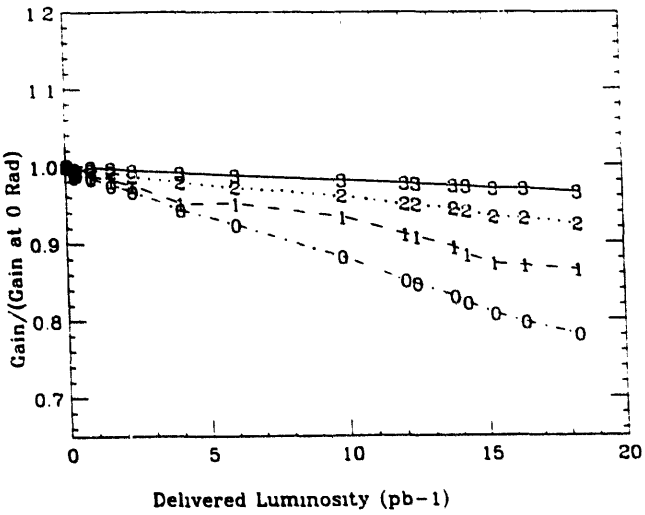

Fig. 10. The measured change in gain as a function of delivered luminosity for four layers of the SVX (0 labels the inner layer, 3 labels the outermost layer).

In Fig. 9 an estimated inner layer radiation dose is shown as a function of the delivered luminosity. This time history shows that the highest dose occurred in the early stages of the commissioning of the Tevatron, followed by a regular slope related to the optimized delivery of the luminosity. The slope value which can be determined from this plot shows a remarkable agreement with our earlier measurements from the 1988 run of 300 rad/pb^{-1}. The BLM and TLD data imply a total dose of approximately 12 krad absorbed by the SVX inner layer with 20 pb^{-1} of delivered luminosity.

During the operation of the SVX detector, the gain and noise of the SVX IC, as well as the detector leakage currents, were monitored. In Fig. 10 the average gain decrease for all SVX layers is displayed. The decreases in the gain show a similar radial dependence to what was measured with TLDs. By applying results of the earlier measurements of gain and noise degradation as a function of the radiation exposure [16], the inferred dose at the SVX inner layer was calculated. The dose determined from the overall change in gain was 22 krad, which is inconsistent with other measurements. The total noise increase at the inner layer predicts a radiation dose of 15 krad with 18 pb^{-1} of delivered luminosity as shown in Fig. 11. During stable operation of the Tevatron the gain and noise changed linearly with the delivered luminosity, which indicates that the predominant damage was caused by the flux of particles coming from the colliding beams, rather than accidents. The dependence of the leakage currents at the inner layer as a function of time indicates a radiation dose which is smaller than that inferred from the gain, but similar to that measured from noise degradation. These measurements may indicate that the time constant of annealing the silicon bulk is short compared to the radiation exposure rate. They may also show that there is a difference in response depending on the type of exposure. In this case the detector was exposed to a low-intensity flux of particles over a long period of time from hadronic collisions. The tests used to determine the relationship between radiation exposure and detector performance exposed the detector to high-intensity radiation sources for very short periods of time, which is the typical method applied for such procedures.

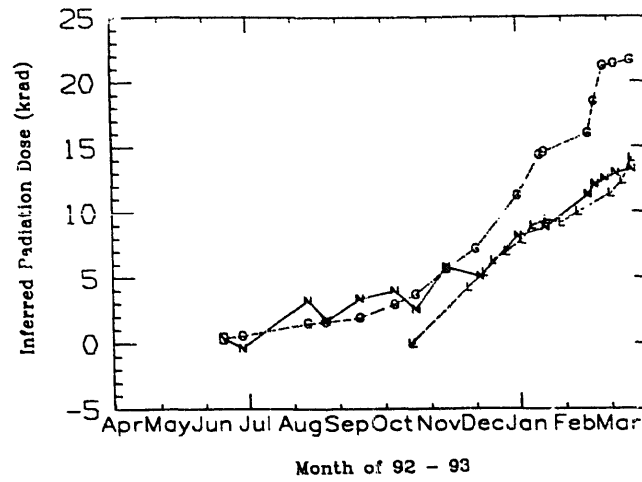

Fig. 11. Time history of the inferred dose at layer 0 obtained from the gain (G), noise (N) and leakage current (L) measurements.

6. Conclusions

The work on the construction of the CDF silicon vertex detector was completed. The silicon microstrip detectors were located to an accuracy of 10 μm and > 98.5% of the silicon strips are fully functional.

A new data acquisition readout electronics for the SVX was built and commissioned. The system was designed to help integrate a new detector into an existing CDF data acquisition network and provided flexibility necessary to operate the SVX IC within the 3.5 μs beam crossing intervals.

Using the specially commissioned radiation monitoring system the total radiation dose was measured and found to be fairly consistent with the expectations that it comes mainly from the luminosity related causes. The possibility of serious accidents associated with high radiation doses was reduced to a minimum by using this system.

The SVX detector is being successfully operated at the CDF experiment and its performance already reaches the design specifications. The preliminary results of the physics analyses already indicate that is a

powerful tool in high-precision tracking and identification of displaced vertices of long lived particles [19]. It gives CDF a great opportunity for a rich B physics program and a good perspective in the search for the top quark.

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