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NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

Electrical performance of the CDF silicon vertex detector *

D. Amidei [d], P. Azzi [f], N. Bacchetta [c], M. Bailey [h], B. Barnett [c], F. Bedeschi [g], D. Bisello [f], V. Bolognesi [g], C. Boswell [c], G. Busetto [f], W.C. Carithers [a], H. Carter [b], A. Castro [f], S. Dell'Agnello [g], P.F. Derwent [d], R. Ducar [b], A. Dunn [d], R.P. Ely [a], B. Flaugher [b], S. Galeotti [g], A. Barbaro-Galtieri [a], A.F. Garfinkel [h], C. Haber [a,**], S. Holland [a], M. Hrycyk [b], D. Herrup [b], R. Hughes [i], S. Kleinfelder [a], M. Loreti [f], M. Mariotti [f], J. Matthews [e], A. Menzione [g], T. Merrick [a], C. Nelson [b], L. Pescara [f], N. Produit [a], G. Punzi [g], F. Raffaelli [g], L. Ristori [g], O. Schneider [a], S. Segler [b], M.D. Shapiro [a], N.M. Shaw [h], T. Shaw [b], J. Skarha [c], F.R. Snider [c], T.Y. Song [d], A. Spies [c], F. Tartarelli [g], P. Tipton [i], S. Tkaczyk [b], J. Tseng [c], N. Turini [g], K. Turner [b], S. Vejcik [c], G. Watts [i], T.R. Wesson [b], W.C. Wester III [a], H. Wenzel [g], M. Wong [a], W. Yao [a], F. Zetti [g]

[a] *The University of California at Berkeley and Lawrence Berkeley Laboratory, Berkeley, California 94720, USA*
[b] *Fermi National Accelerator Laboratory, Batavia, Illinois 60510, USA*
[c] *The Johns Hopkins University, Baltimore, Maryland 21218, USA*
[d] *The University of Michigan, Ann Arbor, Michigan 48109, USA*
[e] *The University of New Mexico, Albuquerque, New Mexico 87131, USA*
[f] *University of Padova, I-35100 Padova Italy*
[g] *Istituto Nazionale di Fisica Nucleare, and University and Scuola Normale Superiore of Pisa, I-56100 Pisa, Italy*
[h] *Purdue University, West Lafayette, Indiana 47907, USA*
[i] *The University of Rochester, Rochester, New York 14627, USA*

1. Introduction

For the 1992–1993 run of the Fermilab Tevatron Collider a new silicon microstrip vertex detector (SVX) has been installed in the Collider Detector at Fermilab (CDF) spectrometer. A general description of the SVX is given in another contribution to these proceedings [1]. Here we will discuss the electrical performance of this new detector.

This paper is organized as follows. In section 2 we describe the electrical design of the SVX front end and silicon detectors. In section 3 we discuss electrical measurements made during construction and fabrication. In section 4 we discuss operating experience with noise, sparse readout, and leakage currents.

2. Electrical design

2.1. Front end electronics

A group of four radial layers subtending 30° of azimuth form a wedge of the SVX detector and are an independent readout unit. The full detector consists of 24 wedges. Each wedge contains 1920 silicon microstrips. The overall electrical layout of a wedge is shown in Fig. 1. The front end readout circuit is the SVX chip [2,3]. There are 2, 3, 4, and 6 of these per layer respectively. The chips are mounted on readout hybrids [4] and the four layers are bussed up to an interface hybrid called the "Port Card". Finally signals going into the port card are carried through an outer tracking detector (the VTX) on low mass etched copper on kapton cables. Readout proceeds from the outer most layer in.

2.1.1. The SVX readout integrated circuit

The SVX chip is a mixed analog and digital signal processing circuit. Revision D, which is used in the final SVX system, was fabricated in 3 μm CMOS technology. The CMOS process used was not radiation hard [5]. A block diagram of the SVX chip and timing pattern is shown in Fig. 2. The chip contains 128 identical channels of charge integration, voltage amplification, sample and hold, and comparator/latch. These are followed by a priority encoding circuit which allows a multiplexed analog readout to select only those channels for which the latch is set (or not set). This selective readout mode is called "sparse". Optionally, a global latch line may be asserted forcing a readout of all channels. This mode of readout is called "latch all".

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** Corresponding author.

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The SVX chip was designed to read out DC coupled silicon detectors. In order to have an unbiased threshold comparison on a channel by channel basis it is therefore necessary to subtract the baseline shift due to varying strip to strip leakage current which will be integrated during the sampling time. This process is accomplished in the SVX chip through a quadruple sample and hold process. In this process the charge is integrated twice (once "on beam" and once "off beam"). The results of these two integrations are subtracted. If any particles had passed through the detector "on beam" an excess would remain at the nearest strips.

The behavior of the comparator circuit in the SVX chip which controls the sparse readout will be affected by the electronic noise. Rather than having a perfectly sharp transition at threshold, the transition will be spread. The threshold value and its width can be measured by performing a quadruple sample and hold integration and observing the fraction of time a particular channel appears in the readout as the test input charge is varied for one of the two integration periods. The absolute value of the threshold itself is a quantity which will be affected by chip to chip variations in internal offsets, errors in the leakage current subtraction due to timing and preamplifier saturation, and parasitic charge injection related to the layout of the electrical system on the SVX. The requirement for efficient operation of the detector is to keep these variations at the same level as the threshold width. This is discussed further in section 4.

2.1.2. Interface circuits

Each readout wedge of the SVX is serviced by an interface card which sits at a radius of ~ 8 cm just beyond the outermost tracking layer. This "Port Card" is fabricated on 0.025 in. Alumina in multilayer thick film process. It is constructed with 7 electrical layers and a total of 35 separate photomasks. The discrete components on this card are surface mounted and all

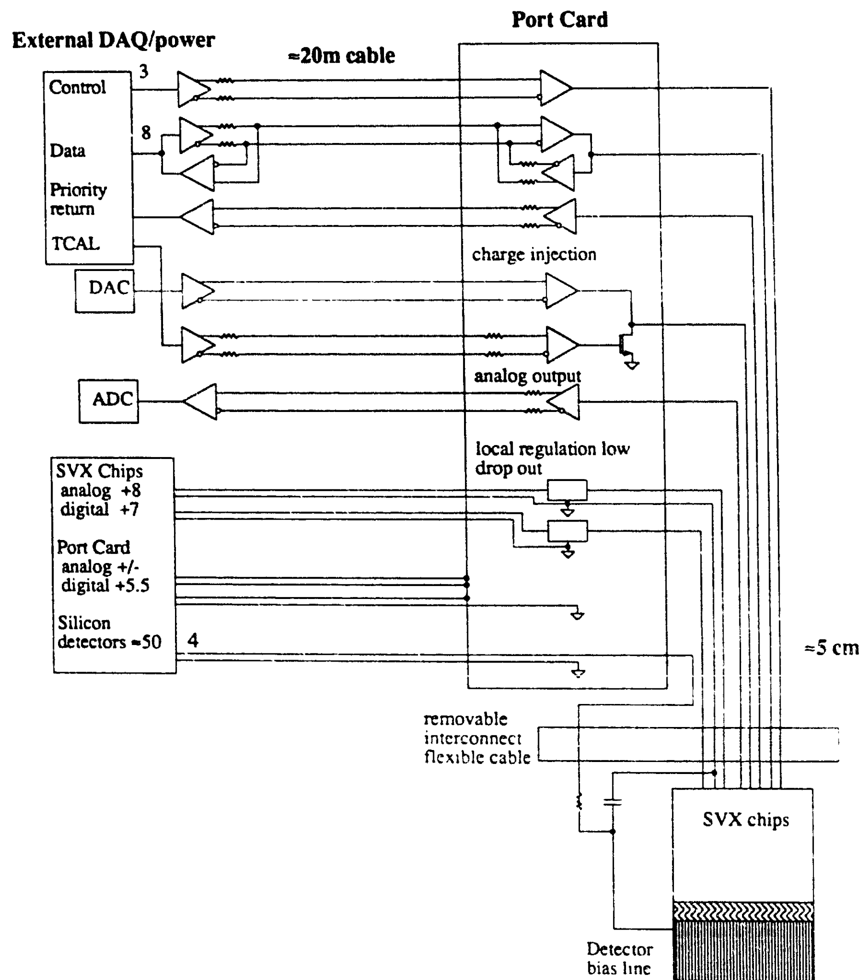


Fig. 1. Electrical layout of a wedge.

integrated circuits are bare die. A block diagram of the port card is indicated in Fig. 1. Lines coming out of the port card are distributed in parallel to the readout hybrids of the wedge and then to the SVX chips themselves. Each port card dissipates 1.8 W.

To provide operating voltages for the SVX readout chips a set of low dropout regulators are used. Based upon test measurements we determined that supplying regulated power nearby the SVX chips was very effective in minimizing noise in the system and controlling systematic variations in the behavior of thresholds and offsets chip to chip. The SVX chip requires two voltages to operate. One supplies the preamp only. The rest of the chip is supplied by the other.

All the digital signals used to control the SVX chips are received differentially by the port card and then converted to CMOS 5 VDC levels before leaving for the readout hybrids. The SVX chips have digital I/O pads which are bi-directional. The digital data output by the chip (channel addresses etc.) are converted to differential signals on the port card for transmission to the external DAQ system. The driver/receiver chip set used conformed to IEEE standards RS-422 and RS-485. To minimize power dissipated on the card we

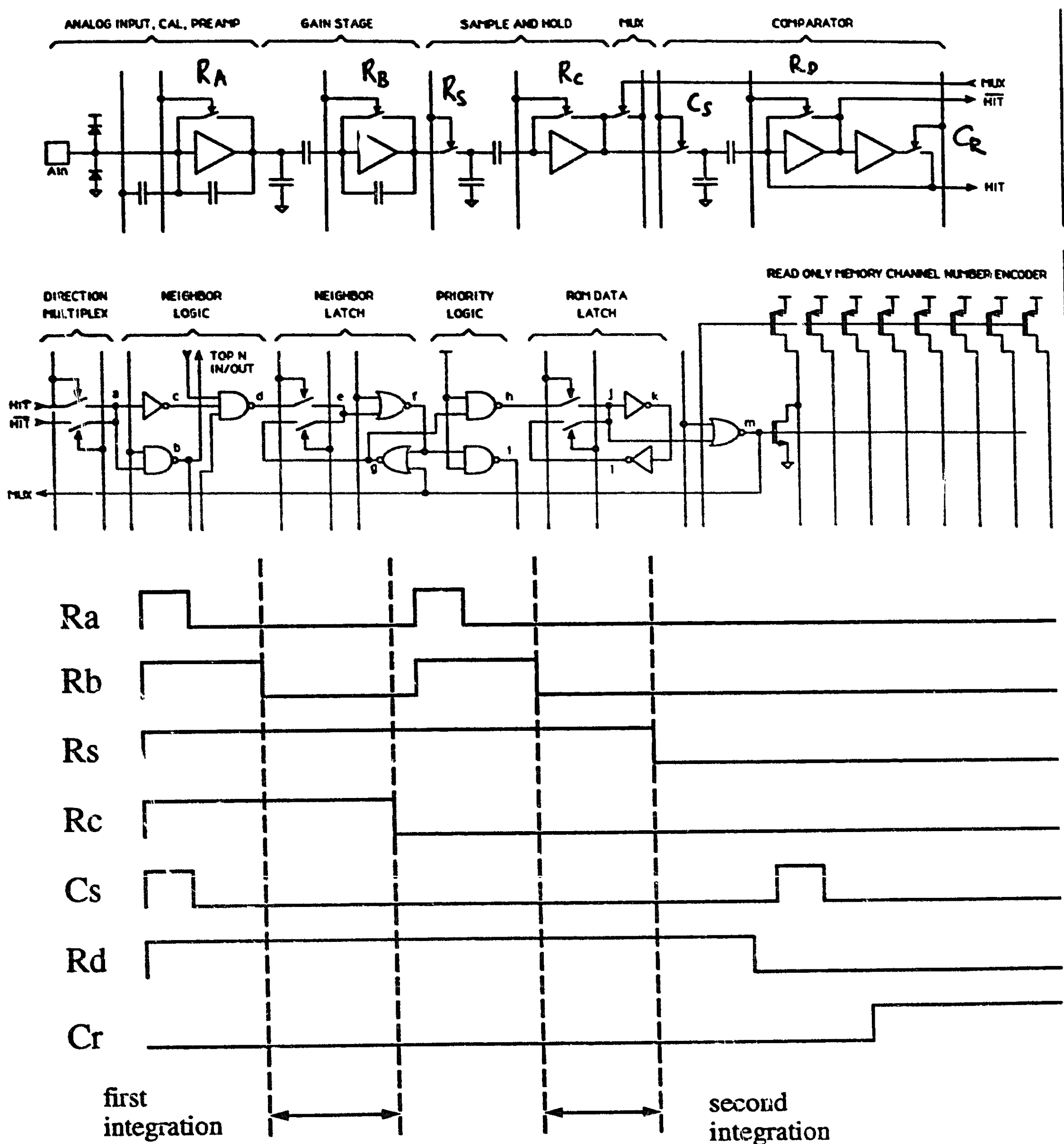


Fig. 2. Schematic of a single channel of the SVX readout chip and timing diagram.

chose to back terminate all the differential pairs serially. In this way standing current on the card was reduced significantly.

Analog data generated by the SVX chips is converted to differential voltages on the port card before transmission to the external DAQ system. These lines are also series back terminated. In order for the SVX chip to sparsify the sampled detector signals a threshold signal is required. This is a voltage step which is input to the preamps through an on-chip calibration capacitor, one per channel, of 60 fF. There is one calibration input on an SVX chip. It was impractical to provide calibration lines for each chip however. The choice was made to supply on the port card two identical calibration circuits. One provides the voltage step for the inner layer while the other serves the outer three layers. Radiation effects will be largest on the inner layer. The ability to set a single threshold for multiple layers and still have good efficiency for hits from tracks is clearly a critical requirement for such a restricted system. The threshold voltages are generated by DACs in the DAQ crates and transmitted differentially to the port cards. The calibration circuits receive, filter, and chop these levels before passing them to the readout hybrids.

3. Electrical assembly and testing

Preceding ladder mechanical assembly the separate electrical sub-units were processed and tested. These steps included detector probing, SVX chip probing, and readout hybrid assembly and test. All electrical tests on chips, hybrids, and ladders were performed with a set of readout and driving electronics developed for the prototyping of the SVX detector and SVX chip. This set consisted of a programmable pattern generator and a flash ADC/memory module [6].

At the time of installation the SVX detector had < 2.5% bad channels. To a large extent these could be traced to problems which occurred during the wirebonding process. This was a major quality control factor in the construction of the full detector. Most of problems were due to cases where the bonder either lost the wire, bonded in the wrong place, or struck the oxide between strips. Procedures were developed which allowed certain damaged regions to be substantially recovered. A total of 125 ladders were put on the bonding machine, 108 ended up to be working ladders. The electrical ladder assembly and testing had an overall yield of 86.4%. The losses were due to electrical failures observed after wirebonding (8.8%), accidents during which ladders were damaged or broken (3.2%), and situations where the wirebonding failed to work (1.6%).

The ladder testing procedure involved measurements of pedestal, gain, noise, and sparse threshold. The data collected was used to select good ladders and sort ladders into wedges with similar electrical properties. Using this data bad regions were scattered around the detector to maximize the acceptance.

During ladder testing dry air was always circulated inside the testing chamber. This was necessary in order to obtain consistent measurements of the ladder properties (some ladders are very sensitive to air moisture). In particular a subset of the ladders showed particular sensitivity to moisture. These ladders would have large leakage currents, especially near the edges, which persisted for up to one hour in a dry atmosphere. After that drying out period they behaved more like typical good ladders. Because of this easy improvement we never used this moisture sensitivity as a criterium for rejecting a ladder. Later, during operation of the SVX detector in the collider, most of these ladders showed anomalous surface currents again. This effect, which in the end was more annoying than significant in terms of the successful operation of the detector, will be discussed in section 4.3 below.

4. Operating performance

4.1. Noise

The noise performance of the SVX chip is shown in Fig. 3. Measured under ideal test conditions with discrete input capacitors, this can be considered a performance standard. To what extent this can be met in a real strip detector system depends upon a number of factors. These include coherent noise, or baseline shifts, interstrip capacitive coupling [7], and effects of the finite risetime of the readout chip analog output. In the strip detector system these effects can be studied

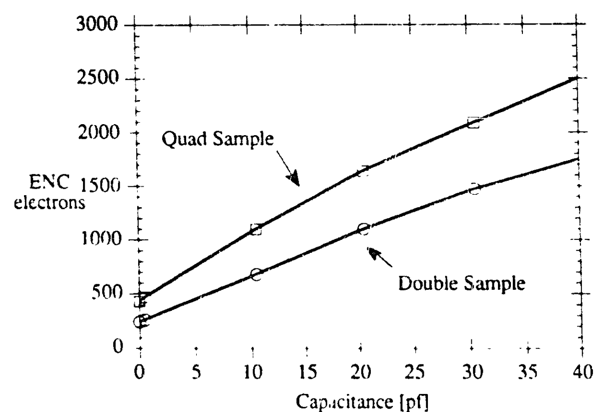


Fig. 3. Equivalent noise charge versus external capacitance for the SVX readout chip as measured on the test bench.

by varying readout timing and by analyzing instantaneous correlations between separate or adjacent strips.

In general the noise performance of the SVX detector was well within specification. Typically the average MIP to noise ratio was 11–12 and the most probable MIP to noise ratio about 1.5 times smaller. With proper off-line clustering and pedestal subtractions the detector was very efficient (~ 98% after acceptance cuts) before radiation damage effects became large on the inner layer. Furthermore, coherent noise contribution was very small. For these reasons it is possible here to discuss the factors listed above which actually represent second order issues.

Coherent noise effects are due either to low frequency pickup during readout ($\tau \sim 1$–1.5 ms) or to high frequency noise which occurs during charge integration and is then fed down by the readout sequence. The detector bias line is susceptible as the latter source. Consequently we have been careful to filter it on the readout hybrid and wire its ground line close to the others. Coherent noise can be measured by studying the correlation between one channel and another non-adjacent. We define the "Hnoise" to be that correlation with a five strip separation:

$$\text{Noise} = \sigma(V_i),$$

$$\text{Hnoise} = \frac{\sigma(V_i - V_{i+5})}{\sqrt{2}}.$$

Here V_i is the instantaneous output level of channel i and σ is its root mean square fluctuation (RMS). The correlation is given by

$$\rho = 1 - \left(\frac{\text{Hnoise}}{\text{Noise}}\right)^2.$$

The Hnoise should always be less than or equal to the Noise. The correlation is therefore positive. By comparing these quantities we could determine that the coherent contribution was less than 600 electrons (which is added in quadrature to the intrinsic noise of 2400).

Unlike the coherent noise, the interstrip capacitance gives rise to a negative correlation between adjacent channels. Similar to Hnoise we defined Dnoise as

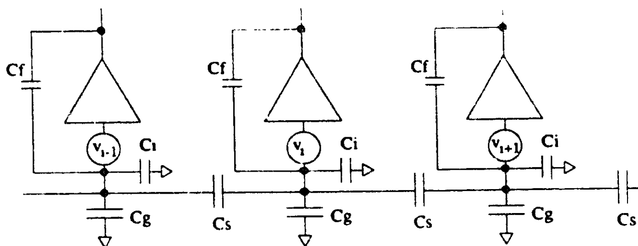


Fig. 4. Electrical model of silicon strip inputs to a set of preamplifiers.

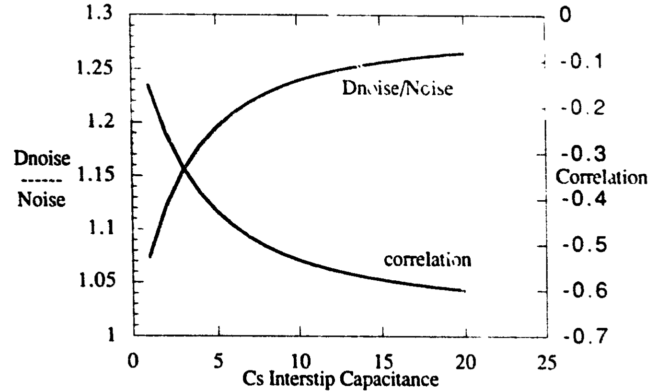


Fig. 5. Noise correlations versus inter strip capacitance assuming $C_a = 6$ pF and $C_g = 5$ pF.

the difference between a channel and its neighbor. A simple model of this effect is shown in Fig. 4. With V_i equal to the instantaneous noise voltage at the input to channel i, σ_V the RMS of V_i (assumed independent of i), Q_i the instantaneous noise charge at the input to i, and σ_{Q_i} the RMS we have

$$Q_i = C_s V_{i-1} - (2C_s + C_g + C_i + C_f)V_i + C_s V_{i+1},$$

$$\sigma_{Q_i} = \sigma_V \sqrt{2C_s^2 + (2C_s + C_g + C_a)^2}$$

with $C_a = C_i + C_f$,

and

$$Q_i - Q_{i+1} = C_s V_{i-1} - (3C_s + C_g + C_a)V_i + (3C_s + C_g + C_a)V_{i+1} - C_s V_{i+2},$$

$$\sigma_{Q_i - Q_{i+1}} = \sigma_V \sqrt{2C_s^2 + 2(3C_s + C_g + C_a)^2},$$

$$\text{Dnoise} = \frac{\sigma_{Q_i - Q_{i+1}}}{\sqrt{2}}.$$

In Fig. 5 we shown the relationship between these quantities as a function of the inter strip capacitance.

The third effect which plays a role in the noise analysis is due to the finite risetime of the analog output bus. In the case of the SVX we had $\tau = 800$ ns. During readout we clocked at 2400 ns in order to keep the readout time within CDF specification for the maximum expected occupancy. Because of this there will be a small positive correlation between a channel and its preceding neighbor in readout order.

$$V_{\text{out}}^i = V_{\text{out}}^{i-1\,\text{TRUE}} e^{-t/\tau} + V_{\text{out}}^{i\,\text{TRUE}} (1 - e^{-t/\tau}).$$

For the purpose of noise analysis this effect can be removed by reading out with a very long cycle. The results of a full analysis of all these effects is shown in Fig. 6. For the SVX the measured interstrip correlation is about −0.3 which is less than would be expected for the simple model of Fig. 4 given a reasonable guess of our inter strip capacitance. This may be

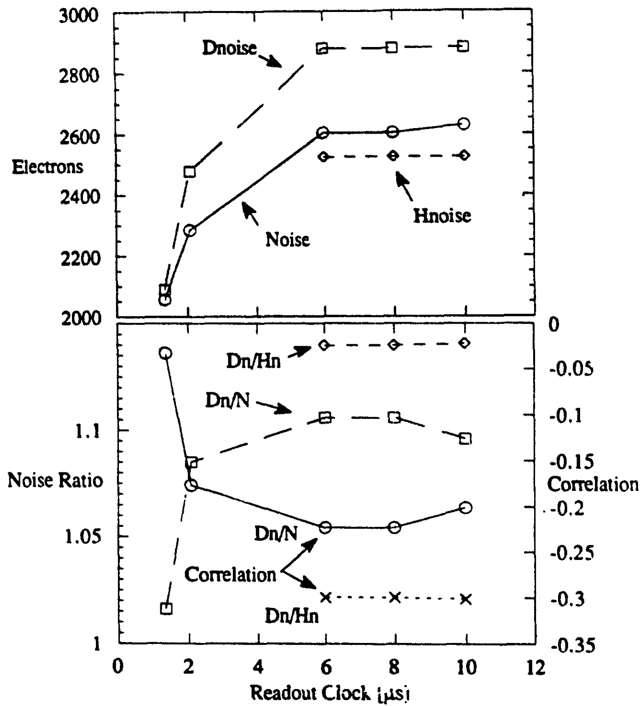


Fig. 6. Noise measures and correlations versus readout clock timing period.

due to additional frequency dependent effects in the real preamplifier plus microstrip system not included in the model. On the practical side, the effect of finite risetime will in principle cause shifts in the reconstructed cluster position for tracking. In our case these are small and we take them out as part of the alignment procedure using track data. For other systems which have position resolution of a few microns the effect may be more significant.

4.2. Sparse readout

The sparse threshold measurement determines, for each channel, the mean value and the RMS of the amount of charge needed at the input of the front-end amplifier to set the latch. The results of this fundamental measurement allows us to decide which operating threshold voltage step $VCAL_{op}$ should be set on the calibration line when taking data with the SVX. The value of $VCAL_{op}$ should be chosen to satisfy two requirements. The efficiency of sparse readout for the detection of particles crossing the silicon should be maximized. The number of noise hits (occupancy) readout should be minimized.

The sparsification threshold measurement consists of measuring a finite number of points on the "efficiency curve" of each channel (which is effectively the integral of the pedestal distribution, assumed here to be a Gaussian distribution). The probability to latch is measured for various values of the injected charge. To perform these measurements, the calibration voltage pulse is stepped through N different values, equally spaced between a value $VCAL_{low}$, where (almost) all the channels do not latch, and a value $VCAL_{high}$, where (almost) all the channels do latch. At each step i, the calibration voltage pulse is set to

$$VCAL_i = VCAL_{low} + \left(i - \tfrac{1}{2}\right)\Delta V,$$
$$i = 1, \ldots, N.$$

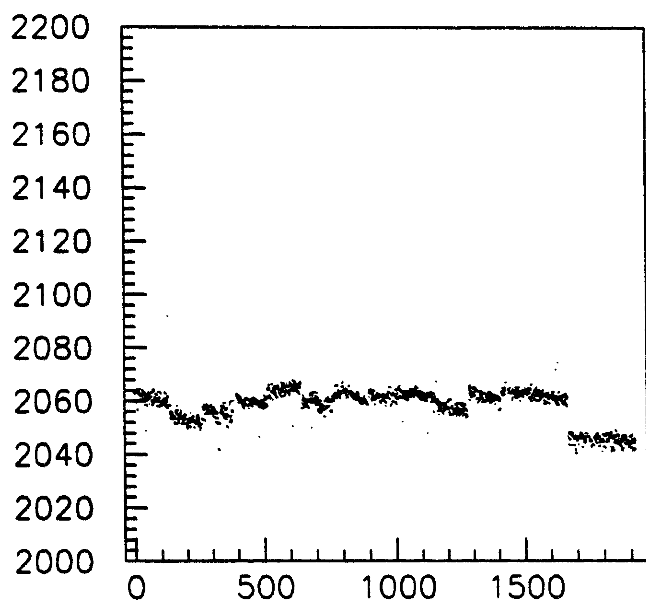
where ΔV is the voltage step size. A data acquisition program performing a quadruple sample and hold and enabling the sparse logic is run, and a number N_{evts} of events are read out during a given step i; for each channel, the probability to latch, ϵ_i, is estimated as the fraction of events for which that channel is readout (note that the analog data is not used). At the end, the sparsification threshold, $VCAL_{thresh}$, (corresponding to a 50% latching efficiency), and its RMS value, σ_{thresh}, are estimated using the following formulae:

$$VCAL_{thresh} = VCAL_{low} + \Delta V \sum_{i=1}^{N} (1 - \epsilon_i);$$

$$\sigma_{thresh} = \Delta V \sqrt{\sum_{i=1}^{N} (2i - 1)(1 - \epsilon_i) - \left(\sum_{i=1}^{N} (1 - \epsilon_i)\right)^2}.$$

In practice this measurement is performed on-line as a standard calibration of the detector. From this we determined 48 values of $VCAL_{op}$ to use during data taking. Reliable operation of sparse readout required short term stability of these operating points, small variations of $VCAL_{thresh}$ within the segmentation set by the fixed number of threshold inputs, and no significant coherent noise in the system. As discussed in section 4.1 the coherent contribution was small. In Fig. 7 we show a scatter plot of the thresholds (50% efficiency points) and RMS (σ_{thresh}) for all channels in a wedge. The units are arbitrary but the scale is set by the RMS. All threshold variations should be of that order. Finally in Fig. 8 we show the variation in the threshold and σ_{thresh} over the full course of the collider run. The thresholds were remarkably stable.

The threshold uniformity and the segmentation of the threshold loading inputs determines what occupancy can be established for a given hit efficiency. For SVX, chip to chip variations due to parasitic charge injection was a limiting factor in minimizing the occupancy. While we operated within the CDF specified event size and readout time it is worthy to note here this effect. Before incurring radiation damage we operated with typically 5-6% occupancy mostly due to the threshold variation along the wedge. After radiation damage we purposely lowered the operating points to increase our efficiency. By the end of the run we had 15-20% occupancy dominated by the inner most layer.



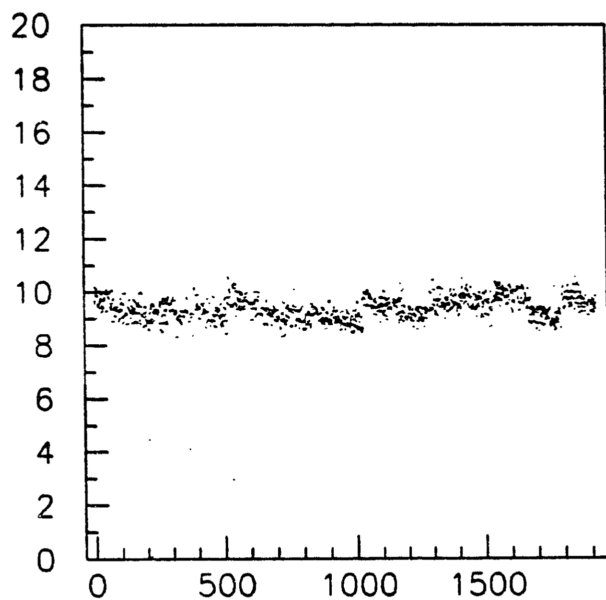


Fig. 7. Value of 50% efficiency point and RMS versus channel number for a wedge. Channels run from the outer layer in. The first 768 channels correspond to the outer layer, followed by 512, 384, and 256 channels for the other three layers. The small shifts correspond to individual SVX chips in the readout chain.

In Fig. 9 we show a plot of occupancy on an inner layer (beam off) versus $VCAL_{op}$ (plotted here in electrons) before and after radiation. Also shown is simultaneously a measure of inefficiency. This quantity is defined somewhat arbitrarily. Here it is the probability for a signal of half an average MIP to latch. The true inefficiency is given by this convoluted with the pulse height distribution for all tracks and is therefore much smaller. Our operating points before irradiation were determined by minimizing the sum of the two low dose curves shown in the plot.

4.3. Leakage currents

In late October 1992, certain ladders in the SVX began to experience sharp increases in leakage current. The increase was large enough to bring the preamps close to their saturation point, thus decreasing the effective gain. These drops in gain resulted in isolated low-efficiency regions in the detector. The redundancy provided by four tracking layers enabled the SVX to continue operation despite these problems. However, the currents were increasing, and continuing to operate with these high leakage ladders was questionable.

The cause of the change in leakage current is not understood. It is believed to be due to surface effects on the silicon wafers. In Fig. 10 we show an example of this effect. The pattern of larger current at the edges is typical of surface leakage. One hypothesis is beam particles ionize the argon-ethane gas surrounding the SVX. Charge then collects on the surface of the detec-

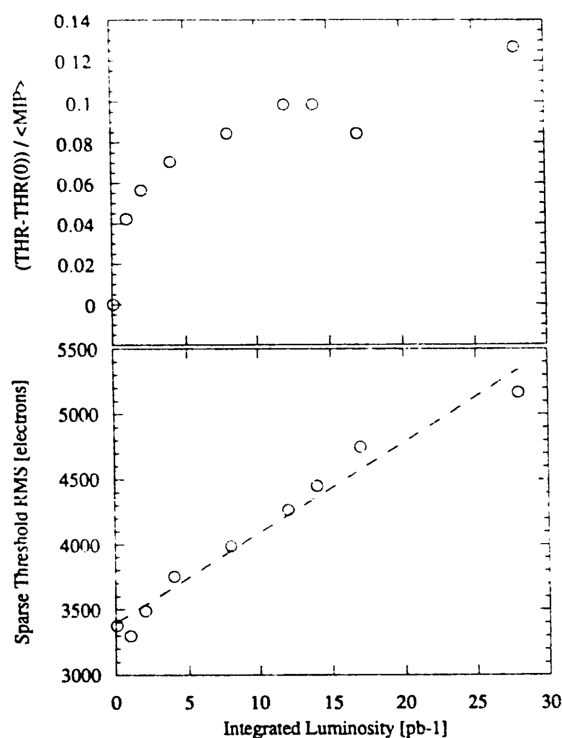


Fig. 8. Variation of 50% efficiency point for an inner layer ladder relative to the signal from a MIP over the course of the entire data run (~1 year). Variation of the RMS showing clear increase in noise due to radiation damage.

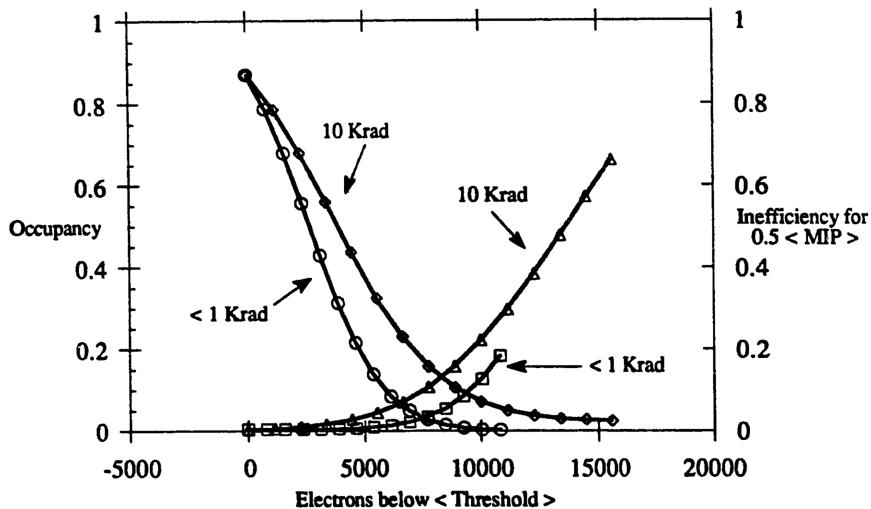


Fig. 9. Occupancy and inefficiency (see text for definition) versus operating point before and after irradiation. Note that neighbors of latched channels are read out giving roughly a factor of three increase in occupancy.

tors, enhancing the surface depletion layer and producing high leakage currents. The increase in leakage current is correlated with beam activity in the Tevatron. Leakage currents seem to increase most during Tevatron beam squeeze, when the particle loss is high.

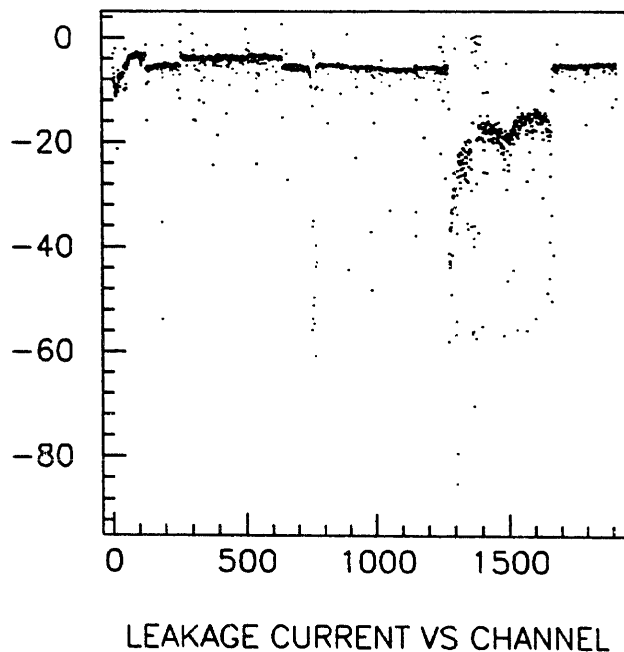


Fig. 10. Leakage current per strip versus channel number for a particular wedge which exhibited anomalous surface currents on one ladder. (See caption of Fig. 7 for additional explanation of horizontal scale.)

Without beam, the currents tend to decrease. The rate of decrease is greater when the silicon is left at full bias voltage, possibly because the surface charge is then being dissipated.

Until November 1992, the silicon bias voltages were ramped down to 4 V when not taking data. This was done to minimize the chance of tripping the bias supplies during Tevatron studies, beam injection, and tuning. In mid-November 1992, this procedure was modified to help control the currents on the high leakage ladders. The high leakage ladders were thereafter kept at full bias at all times.

The ladders which showed the increased leakage currents were in general the same set which were sensitive to moisture during initial testing. No moisture was present in the operating gas volume. Furthermore no clear relationship could be established between the operating gas and these leakage effects.

Certain ladders continue to show higher than average leakage currents, but not enough to seriously affect the performance of the SVX. By keeping the affected ladders at full bias all of the time, the problem has been kept under control.

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