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Accurate Characterization of Silicon-On-Insulator MOSFETs for the Design of Low-Voltage, Low-Power RF Integrated Circuits

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Abstract. The maturation of low cost Silicon-on-Insulator (SOI) MOSFET technology in the microwave domain has brought about a need to develop specific characterization techniques. An original scheme is presented, which, by combining careful design of probing and calibration structures, rigorous *in-situ* calibration, and a new powerful direct extraction method, allows reliable identification of the parameters of the non-quasi-static small-signal model and the high-frequency noise parameters for MOSFETs. The extracted model is shown to be valid up to 40 GHz.

Key Words: integrated circuit measurements, microwave measurements, MOSFETs, scattering parameters measurements, silicon-on-insulator technology

1. Introduction

Silicon-based technologies for RF front-end circuits have recently been developed to produce highly integrated portable personal digital RF communication terminals. The key issue is that it must be possible to integrate these Si-based microwaves into VLSIs. For this purpose, the use of a conventional digital CMOS technology is very attractive [30,39,43]. Microwave integrated circuits need very high performance active devices (high f_T, $f_{\max}$, etc.) that perform well even in the multi-gigahertz range. These last years the interest of SOI MOSFETs in the microwave domain has been reported in the literature [4]–[8]. Actually, SOI MOSFETs exhibit interesting features such as higher current drive [45] and lower parasitic source and drain capacitances [4] compared to bulk silicon MOSFETs, which allow SOI circuits to offer excellent high-frequency performances. MMIC technologies offering a complete range of active and

passive devices have been developed combining CMOS processing with high-resistivity wafers (5000 and 10,000 $\Omega \cdot$ cm) [2,7]. The maturation of low cost SOI MOSFET technology in the microwave domain has brought about a need to develop specific characterization techniques. Characterization at microwave frequencies relies on scattering (S-) parameters measurements. However, description of the measured frequency response in terms of an equivalent circuit is much more useful, both for analog design and performance analysis. In particular, choosing the equivalent circuit topology so as to reflect the underlying physics of the device, one may significantly simplify the characterization and the modeling tasks. This approach is advocated by several authors [5,13] and one of the most striking examples of it is the F_{50} method from Dambrine et al. [14], which allows to fully characterize the noise behavior of FETs, using only one noise measurement at the bias point of interest together with a ''physical'' equivalent circuit. To benefit from the advantages of physical modeling using on-wafer S-parameters measurements, one must be able to identify correctly the equivalent circuit elements of a device that is representative of what will be used in functional circuitry. This imposes constraints on the design of the probing structure, on the de-embedding and the parameter-extraction procedures. It is the purpose of this paper to present the original solutions that were developed for the characterization of SOI MOSFETs up to 40 GHZ.

2. Device Fabrication and Modeling

Thin-Film SOI MOSFETs are fabricated with a CMOS-compatible process on low-resistivity (20 $\Omega \cdot$ cm) SIMOX wafers. The initial 200 nm silicon film is thinned down to about 100 nm by oxidation and oxide strip. After a semi-recessed LOCOS isolation step, a 30 nm gate oxide is grown and boron is implanted to adjust the *n*- and *p*-channel threshold voltages. A 340 nm thick polysilicon is then deposited, doped (implantation, *As*, 100 keV, $1 \times 10^{16}\,\mathrm{cm}^{-2}$) and patterned. Arsenic (80 keV, $4 \times 10^{15}\,\mathrm{cm}^{-2}$) and boron (20 keV, $5 \times 10^{15}\,\mathrm{cm}^{-2}$) are implanted to form the source/drain regions, followed by a RTA (950°C, 40 s) activation step. Then, a 150 nm thick $Si0_2$-layer is deposited and etched by RIE to form spacers. After a short-time 2% HF dip, either a titanium or a nickel layer, or a titanium/cobalt stack layer is deposited using an-egun system with thicknesses of 30, 25 or 7 nm/13 nm, respectively. The conventional two-step SALICIDE process is used for titanium [3,26,27] and cobalt [31] silicidation (Ti: 675°C, 45 s and 900°C, 15 s; Ti/Co bilayer: 675°C 45 s and 900°C, 30 s. Nickel monosilicide [33,34] is formed with a one-step annealing at 550°C for 40 s. Unreacted metals are selectively removed by a $H_2SO_4 + H_2O_2(2:1)$ mixture. A nitride/oxide layer is then deposited and contact holes are opened to access the devices. An aluminum metallization is used to complete the process. The gate sheet resistance of the wafers with $TiSi_2$, $CoSi_2$ and NiSi are 6.2, 4.4 and 2.8 $\Omega/\square$ respectively.

In order to obtain optimized high-frequency performances, a multi-fingers comb-like gate structure is used for the microwave MOSFET design. Fig. 1 shows a common source MOSFET embedded in the microwave probing structure. The coplanar waveguide structure is designed to minimize the series inductance in the source, L_{se}, and to meet the requirements of the de-embedding method described in Section 3. The method allows to set the boundaries of the de-embedded MOSFET at a very precise location along the feeding CPW, so that probe-pad parasitics are very well under control.

The model used for the common-source SOI MOSFET in saturation is shown in Fig. 2. According to the physical meaning attributed to the elements, the circuit can be split into three parts:

- Index ''i'' denotes the intrinsic elements which model the useful transistor effect, and are thus dependent on the bias conditions and on the size of the active zone. In agreement with the theory from [48] and the experimental evidence from Eggermont et al. [17], a non-quasi-static (NQS) formulation is adopted, in order to account for channel propagation delays, and thus extend the validity of the model at least up to the cut-off frequency of the MOSFETs.
- Index ''e'' denotes the extrinsic elements, which are independent of bias, but scale with the active zone. In particular, R_{se} and R_{de} can be expected to be constant versus bias in view of the drain and source fabrication technology used. R_{ge} accounts for the resistance of the gate poly silicon and contacts. C_{gde} and C_{gse} account for the outer-

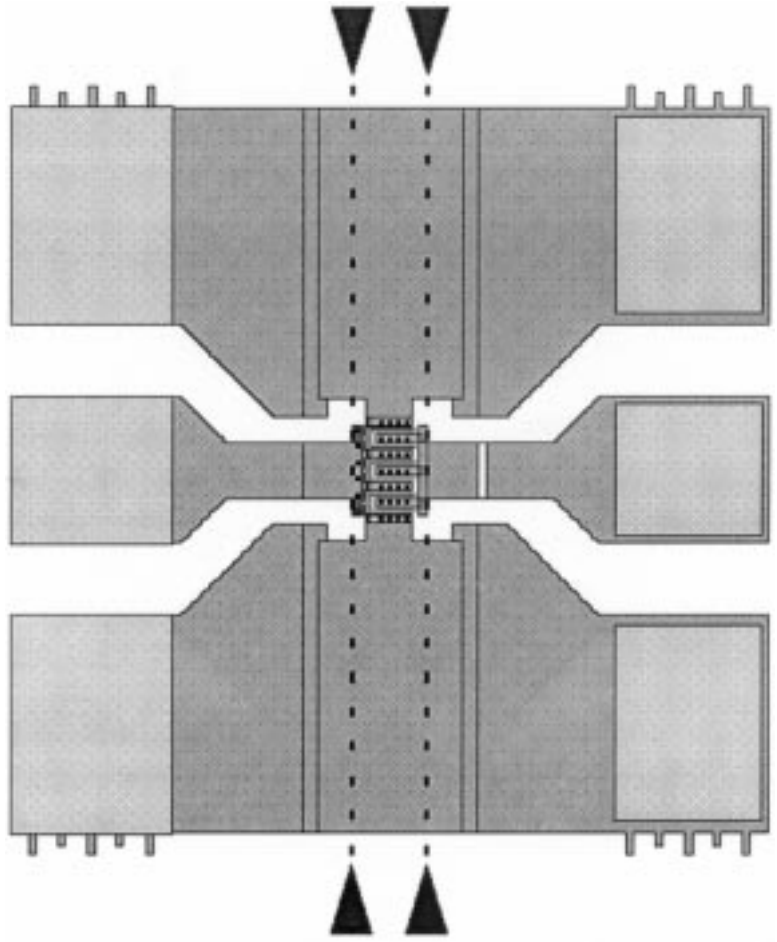


Fig. 1. Layout view showing a MOSFET embedded in the probing structure. The reference planes are materialized by the vertical dotted lines.

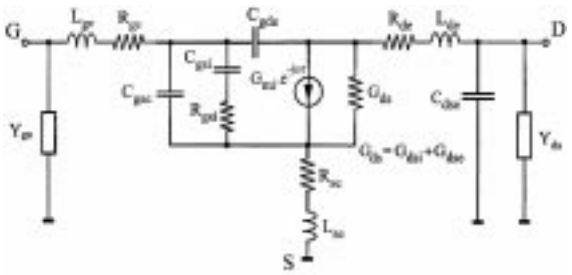


Fig. 2. Small-signal equivalent circuit for a common-source MOSFET in saturation.

fringing and overlap capacitances. C_{dse} and G_{dse} account for substrate coupling between the source and drain.

- Index ''a'' denotes the shunt admittances caused by the metal connections just outside of (adjacent to) the active zone. The frequency behavior of these admittances is essentially capacitive, as the effect of the feeding lines is cancelled by the de-embedding method, and dominating contributions thus emanate from localized inter-metal capacitances. Adjacent parasitics are constant under normal biasing conditions, and not dependent on the width of the active zone.

The source-drain coupling elements, C_{dse} and

G_{dse} are classically connected inside of R_{se} and R_{de}. To keep the theoretical developments of Section 4.2 at a tractable level, the source-drain coupling capacitance C_{dse} has been connected in parallel with the adjacent parasitics at the drain, while the associated loss-conductance is lumped together with the intrinsic output conductance G_{dsi}. These modifications have a negligible influence on the predicted frequency response, up to the limit of the measurement band.

In agreement with these considerations, the equations corresponding to the circuit of Fig. 2 are shed into the following form for subsequent developments:

$$[\mathbf{Y}_\mu - \mathbf{Y}_\alpha - \mathbf{Y}_\varepsilon]^{-1} = \mathbf{Z}_\sigma + \mathbf{Y}_\pi^{-1} \triangleq \mathbf{Z}_{\sigma\pi} \tag{1a}$$

$$\mathbf{Y}_\alpha \triangleq \jmath\omega \begin{bmatrix} C_{ga} & 0 \\ 0 & C_{da} \end{bmatrix} \tag{1b}$$

$$\mathbf{Y}_\varepsilon \triangleq \begin{bmatrix} 0 & 0 \\ 0 & \jmath\omega C_{dse} \end{bmatrix} \tag{1c}$$

$$\mathbf{Z}_\sigma \triangleq \begin{bmatrix} R_{ge}+R_{se} & R_{se} \\ R_{se} & R_{de}+R_{se} \end{bmatrix} + \jmath\omega \begin{bmatrix} L_{ge}+L_{se} & L_{se} \\ L_{se} & L_{de}+L_{se} \end{bmatrix} \tag{1d}$$

$$\mathbf{Y}_\pi \triangleq \begin{bmatrix} \jmath\omega\left(\frac{C_{gsi}}{1+\jmath\omega R_{gsi}C_{gsi}} + C_{gse} + C_{gde}\right) - \jmath\omega C_{gde} \\ \frac{G_{mi}e^{-\jmath\omega\tau}}{1+j\omega R_{gsi}C_{gsi}} - \jmath\omega C_{gde}G_{dsi} + G_{dse} + \jmath\omega C_{gde} \end{bmatrix} \tag{1e}$$

where $\mathbf{Y}_\mu$ is the admittance matrix measured at the reference planes.

3. De-embedding

To correct for the overwhelming influence of cables and probes on the S-parameters measurements, a calibration of the network analyzer is performed using a commercially available impedance standards substrates (ISS). These calibration substrates are usually fabricated on an alumina substrate with a thick gold metallization. To measure the MOS devices, the probes must then be moved onto the silicon wafer. Due to the different substrate materials and probe-pad geometries, additional corrections must be applied to obtain the characteristics of the *DuT* in conditions corresponding closely to normal use inside a circuit. The most commonly used approach for this second de-embedding step is the immitance correction method—also known as dummy de-embedding.

This method was first proposed by van Wijnen for bipolar devices [50]. It was later enhanced by Fraser [19] and by Cho [10]. The method uses three reference two-port structures to determine the parameters of an equivalent circuit model representing the pad parasitics. The model consists of shunt admittances and series impedances loading the device-under-test (DuT). The reference structures are:

1. A two-port open circuit, obtained by removing the DuT and leaving the lines at both ports open.
2. A short circuit, obtained by replacing the DuT by metal lines connecting both ports to ground.
3. A through connection, obtained by replacing the DuT by a metal line connecting the ports together.

The method is, however, unable to determine the true characteristics of the three reference devices, so that ideal characteristics are assumed: There is no fringing capacitance for the open ends, the metal lines of the short and thru have neither inductance nor resistance. These assumptions limit the applicability of the method to small device geometries where the parasitics of the short, the open and the thru are negligible. These assumptions also result in a general overestimation of the corrections to apply which, in the case of transistors, may result in artificially high apparent values for several characteristics, such as the current-gain transit frequency and can lead to systematic offset between actual circuit performance and the design targets, as discovered by Kim [25] and Lee [28].

To attain the high accuracy levels required for the direct extraction of NQS equivalent circuit parameters demonstrated in Section 4, an alternative de-embedding strategy has been introduced in this work: in-situ calibration.

3.1. *In-Situ Calibration*

This de-embedding method is based on scattering parameter calibration techniques belonging the TAN-family of algorithms described by Heuermann and Schiek [23]. These techniques are renown for their accuracy, well documented and enjoy a sound

theoretical foundation [32]. The error-model used consists of a pair of two-port transfer matrices, that can model any waveguide transition where only a single waveguide-mode is propagating.

The underlying assumptions are thus:

- that the on-wafer probes support only a single mode, which is the case if they are used within the bandwidth specified by the manufacturer;
- that the on-wafer coplanar waveguide (CPW) structures themselves operate with a single mode. In the case of the present work, the cut-off frequency of higher order CPW modes and surface waves were estimated to be higher than 60 GHz;
- that no direct coupling exists between the on-wafer probes. In the case of probes based on micro-coaxial waveguides, the direct coupling can be made negligibly small if the spacing between probes is kept sufficiently wide, $\approx 400\,\mu$m.

Within the TAN-family, the thru-reflect-line (TRL) and the thru-reflect-match (TRM) algorithms are widely used for the calibration of on-wafer probes using commercial ISS. For the present de-embedding purposes, TRL was found to give the best results, because it has the least stringent requirements for the characteristics of the calibration structures. Fig. 3 shows the layout of the calibration structures implemented on the wafers in the immediate vicinity of the DuTs, hence the name *in situ*.

Aside from the comprehensive model for the transitions at both ports, the *in-situ* TRL calibration also yields the propagation constant of the CPW-line as a by-product. This allows to locate the reference planes at precise positions along the CPWs feeding the test devices, so that the input and output adjacent parasitics can be minimized, while avoiding the pitfall of overestimated corrections. Being able to move the reference planes along the feeding lines gives also some flexibility in the design of the RF probing structures, so that one single calibration set can be used for all devices, transistors, resistors, inductors, capacitors.

The practical implementation of the *in-situ* calibration for the de-embedding of devices is organized as follows:

1. Make a reference calibration on a commercial ISS.
2. Load the silicon wafer and measure the calibration structures shown in Fig. 3.
3. Apply the TRL algorithm to get the transier matrices for each port.
4. Measure the DuT and apply the correction [22].

The result of this procedure are the de-embedded S-parameters of the DuT referenced to the characteristic impedance of the CPW Line standard, Z_c, [32].

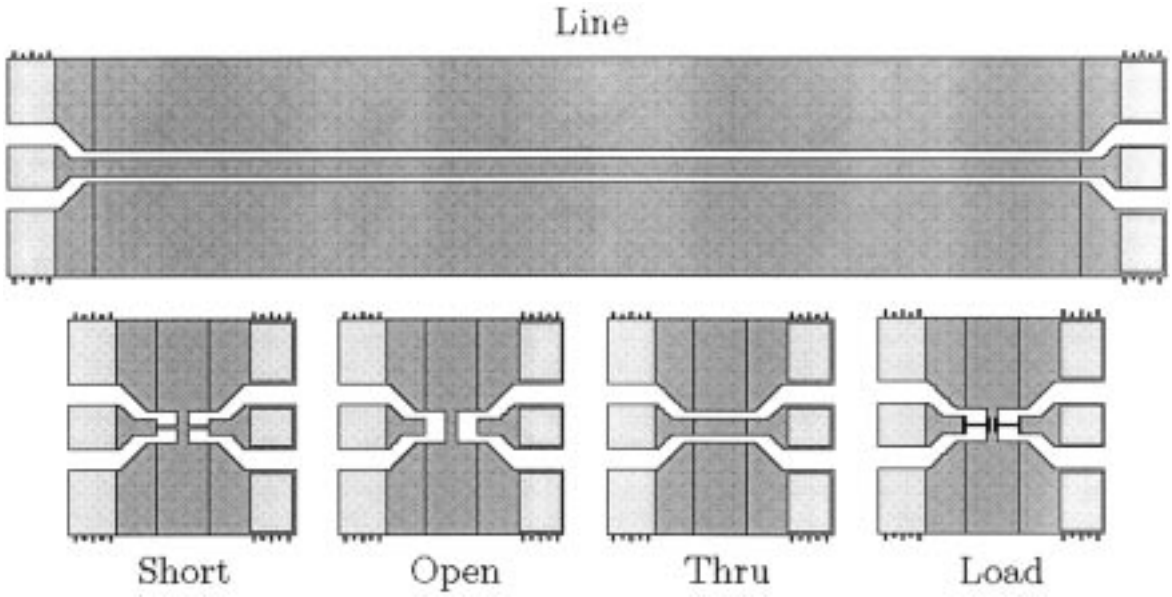


Fig. 3. Calibration structures for the *in-situ* calibration.

However Z_c is *a priori* unknown, as it is a very complex function of substrate resistivity, metallization and insulation layers thicknesses and actual layout of the CPW line. In order to use the de-embedded S-parameters it is necessary to know Z_c accurately to be able to apply transforms yielding admittance or impedance parameters or S-parameters referenced to the classical 50 Ω value [32].

3.2. Reference Impedance Determination

Two schemes have been tested for the determination of the characteristic impedance Z_c. The load measurement method developed by the authors [20], relies on the comparison between S-parameters and DC-resistance measurement of a resistor. The calibration comparison method [53], extracts Z_c from the error-boxes relating the *in-situ* calibration to the preceding ISS calibration. This latter method requires a precise knowledge of the reference impedance of the ISS calibration. Both methods were found to agree well and finally the load measurement method was preferred as it is more likely to ensure a coherent DC and RF measurements.

The *in-situ* calibration procedure together with the characteristic impedance determination have been used successfully for more than 4 years on several projects aiming at the development of microwave SOI technologies. Fig. 4 shows a typical evolution of Z_c across the 40 GHz band on a low-resistivity substrate.

4. Extraction of the NQS Equivalent Circuit Parameters

4.1. Adjacent and Extrinsic Capacitances

Extraction of shunt adjacent and extrinsic parameters is best performed in deep depletion when all intrinsic parameters tend to vanish. To distinguish between the adjacent and extrinsic contributions to parasitic capacitance, the specific scaling dependencies are exploited. As explained in Section 2, the adjacent capacitances C_{ga} and C_{da} are independent of the active zone width W (the total device width divided by the number of gate fingers), while extrinsic capacitances C_{gse}, C_{gde}, C_{dse} are proportional to W. For the series extrinsic elements the picture is somewhat more involved: R_{ge} is linear in W but has some fixed part due to metal contacts; R_{de} and R_{se} are inversely proportional to W, while inductances can be

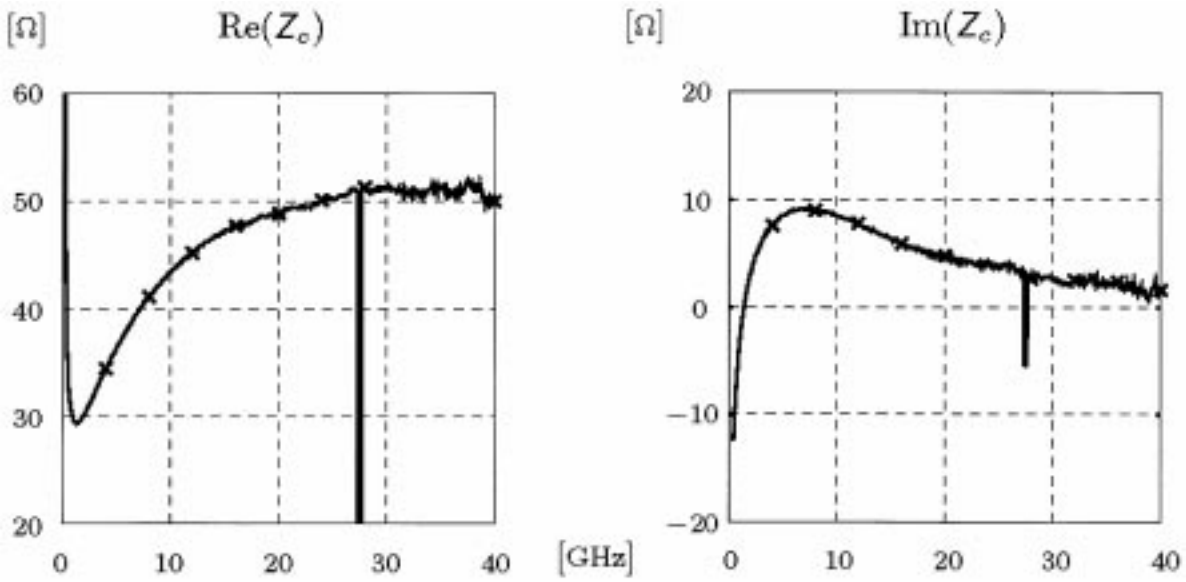


Fig. 4. Z_c from a CPW on a 20 Ω · cm SOI substrate.

expected to have both a fixed part and one that is proportional to W.

Starting from equation (1a), one may write the following expression for the admittance matrix associated with the active zone:

$$\begin{aligned}\mathbf{Y}_{\mu} &= [\mathbf{Z}_{\sigma} + \mathbf{Y}_{\pi}^{-1}]^{-1} + \mathbf{Y}_{\varepsilon} + \mathbf{Y}_{\alpha} \\ &= \mathbf{Y}_{\pi}\underbrace{[\mathbf{I} + \mathrm{Re}(\mathbf{Z}_{\sigma}\mathbf{Y}_{\pi})}_{\triangleq \mathbf{A}} + \jmath\underbrace{\mathrm{Im}(\mathbf{Z}_{\sigma}\mathbf{Y}_{\pi})]^{-1}}_{\triangleq \mathbf{B}} + \mathbf{Y}_{\varepsilon} + \mathbf{Y}_{\alpha}\end{aligned} \tag{2}$$

In deep depletion, the MOSFET behaves as a passive device, so that matrices **A** and **B** are symmetric, being themselves products of symmetric matrices. Exploiting this property, equation (2) can transformed using simple matricial algebra into:

$$\mathbf{Y}_{\mu} = \mathbf{Y}_{\pi}[\mathbf{A} - \jmath\mathbf{B}][\mathbf{A}\mathbf{A} + \mathbf{B}\mathbf{B}]^{-1} + \mathbf{Y}_{\varepsilon} + \mathbf{Y}_{\alpha} \tag{3}$$

This equation shows that in all generality, the elements of $\mathbf{Y}_{\mu}$ are rational functions of W, with numerator and denominator polynomials of order higher than 6. From equation (2) one can see that matrix **A** can be expanded as the sum of the identity matrix and a matrix of $\omega^2 LC$ products, while matrix **B** consists purely of ωRC products. Neglecting the $\omega^2 LC$ and ωRC products with respect to 1, yields the following simple equation:

$$\mathbf{Y}_{\mu} \cong \mathbf{Y}_{\pi}[\mathbf{I} - \jmath\mathbf{B}] + \mathbf{Y}_{\varepsilon} + \mathbf{Y}_{\alpha} \tag{4}$$

This equation is accurate within the 5% at 20 GHz. It shows that the imaginary part of the as-measured admittance matrix is linear in W and that the regression coefficients can be linked to the extrinsic and adjacent capacitances. Equation (4) shows also that for the real part of $\mathbf{Y}_{\mu}$ the picture is more involved, up to the point that extraction of conductances using regression methods is hardly feasible. This allows to stress again the importance of proper de-embedding.

Fig. 5 illustrates the application of regressions inspired from equation (4) to discriminate between adjacent and extrinsic parasitics. The plotted capacitances $C_{\mu g}, C_{\mu d}, C_{\mu gd}$ were obtained by fitting the slope of, respectively, $\mathrm{Im}(Y_{\mu 11} + Y_{\mu 12})$, $\mathrm{Im}(Y_{\mu 22} + Y_{\mu 12})$ and $\mathrm{Im}(-Y_{\mu 11})$ versus frequency, in the band from 3 to 20 GHz. The evolution of capacitances is almost exactly linear in W. The fact that the intercept of $C_{\mu gd}$ virtually crosses the origin, corroborates the assumption that the off-diagonal elements of $\mathbf{Y}_{\alpha}$ are zero.

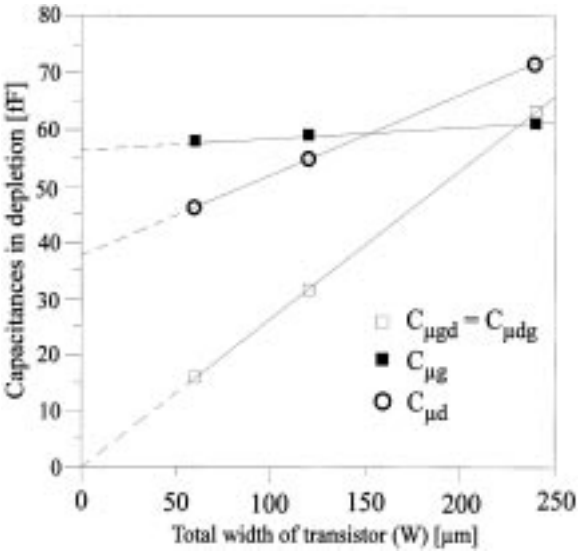


Fig. 5. Total capacitances measured in depletion for various active zone widths (W).

4.2. NQS Intrinsic Device Model

In a previous paper [38] the authors demonstrated a direct extraction scheme applicable to the quasi-static equivalent-circuit model ($R_{gsi} \equiv 0, \tau \equiv 0$). This extraction scheme is based on the formulation of the $\mathbf{Z}_{\sigma\pi ij}$-elements first published by Lee [29]:

$$\mathrm{Re}(\mathbf{Z}_{\sigma\pi ij}) = \mathrm{Re}(\mathbf{Z}_{\sigma ij}) + \frac{A'_{ij}}{\omega^2 + B'} \quad \text{for } i, j \in \{1, 2\} \tag{5}$$

$$\frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma\pi ij}) = \frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma ij}) - \frac{E'_{ij}}{\omega^2 + B'} - \frac{F'_{ij}}{\omega^2(\omega^2 + B')} \quad \text{for } i, j \in \{1, 2\} \tag{6}$$

where B, the A'_{ij}, E'_{ij} and F'_{ij} are real and frequency independent coefficients involving only the intrinsinc and shunt extrinsic equivalent circuit parameters. The common frequency dependency of the equations generated from (5) and (6) ensures that the parametric curves built in a two-dimensional plane according to equations (7) or (8) are straight lines:

$$\begin{bmatrix} x_1(\omega) \\ x_2(\omega) \end{bmatrix} = \begin{bmatrix} \mathrm{Re}(\mathbf{Z}_{\sigma\pi ij}(\omega)) \\ \mathrm{Re}(\mathbf{Z}_{\sigma\pi kl}(\omega)) \end{bmatrix} \quad \text{where } \{i,j\} \neq \{k,l\} \qquad (7)$$

$$\begin{bmatrix} x_1(\omega) \\ x_2(\omega) \end{bmatrix} = \begin{bmatrix} \frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma\pi ij}(\omega)) \\ \frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma\pi kl}(\omega)) \end{bmatrix} \quad \text{where } \{i,j\} \neq \{k,l\} \qquad (8)$$

It is shown in Raskin et al. [38], that both the series resistances and inductances can be obtained from the intercepts and slopes of the parametric impedance curves plotted from measurement data at a single bias-point in saturation. Once these elements are known, all intrinsic parameters can be computed from the simple procedure described by Berroth [5]. Interestingly, this QS extraction procedure works well, independently of the experimental evidence of the influence of NQS effects [17]. The parametric plots are well fitted by straight lines, and the S-parameter curves predicted from the extracted model agree quite well with the measurements over a broad frequency range.

However, when looking at the bias dependency of the extracted QS parameters, results appear to be less satisfactory because the extrinsic resistances R_{ge}, R_{de} and R_{se} show a variation which is not expected from technological and physical considerations, see Fig. 6 and Table 1. Further, some intrinsic parameters obtained according to Berroth and Boschi [5] show a residual frequency dependence indicating that the QS model topology is not fully adequate. In Raskin et al. [37], the authors showed that introducing NQS circuit parameters in the model allowed the remedy to the above problems. However, at that time they were not able to propose a direct extraction scheme for the complete NQS model, and an optimizer-based method was used.

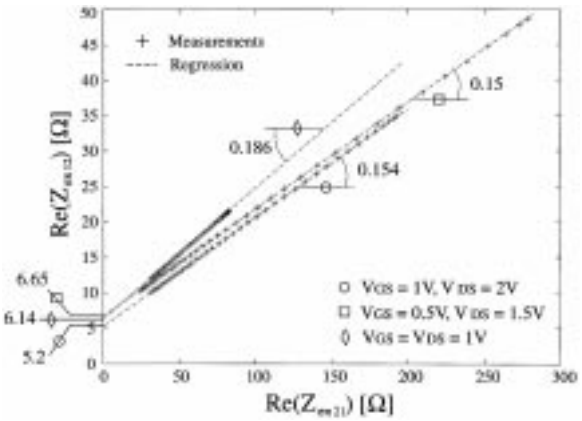


Fig. 6. Parametric plot of resistances in the 0.5–40 GHz range for a $10 \times (24\,\mu\mathrm{m}/0.75\,\mu\mathrm{m})$ *n*-MOSFET in different biasing conditions.

With the minimal adaptations of the equivalent circuit topology described in Section 2, it is however possible to explain the paradox of getting straight parametric curves in the presence of NQS effects and to develop a direct extraction method for all circuit parameters. It is shown in Appendix A that equations in (1a) can be cast in the following form:

$$\mathrm{Re}(\mathbf{Z}_{\sigma\pi ij}) = \mathbf{R}_{\sigma ij} + \Delta\mathbf{R}_{\sigma ij} + \frac{A''_{ij}}{\omega^2 + B''}$$

$$\text{where } \mathbf{R}_{\sigma ij} \triangleq \mathrm{Re}(\mathbf{Z}_{\sigma ij}) \quad \text{and} \quad i,j \in \{1,2\} \qquad (9)$$

$$\frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma\pi ij}) = \mathbf{L}_{\sigma ij} + \Delta\mathbf{L}_{\sigma ij} - \frac{E''}{\omega^2 + B''} - \frac{F''_{ij}}{\omega^2(\omega^2 + B'')}$$

$$\text{where } \mathbf{L}_{\sigma ij} \triangleq \frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma ij}) \quad \text{and} \quad i,j \in \{1,2\} \qquad (10)$$

These new equations have basically the same structure as equations (5) and (6). As a result, the shape the parametric impedance curves is still a straight line, but with modified intercept and slope. The originality of (9) and (10) relies on the fact that the influence of the NQS circuit parameters τ and R_{gsi} is now explicitly accounted for by the $\Delta R_{\sigma ij}$ and $\Delta L_{\sigma ij}$ terms. To identify the series extrinsic equivalent circuit parameters correctly, one must somehow estimate the contribution of these NQS error terms.

In order to obtain initial estimates of the error terms, the matrix $\mathbf{Z}_\pi \triangleq \mathbf{Y}_\pi^{-1}$ is reconstructed on the basis of parameter values extracted using the QS approach (single primes). Using computer simulations, the authors were indeed able to show that reasonably accurate estimates of the QS intrinsic elements $(C'_{gsi}, G'_{mi}, G'_{dsi})$ as well as of the channel delay τ' could be obtained in this manner [37]. The QS extraction scheme fails however to yield an adequate value for R_{gsi}, which is preferably estimated using the relationship predicted theoretically by Tsividis [48]: $R'_{gsi} = \tau'/(2C'_{gsi})$. Once $\mathbf{Z}_\pi$ has been reconstructed at all frequency points, the error terms $\Delta R_{\sigma ij}$ and $\Delta L_{\sigma ij}$ are obtained by considering the intercepts and slopes of the parametric curves defined from the elements of $\mathbf{Z}_\pi$, in a similar fashion as for $\mathbf{Z}_{\sigma\pi}$, in (7) and (8). Fig. 7 illustrates the quality of the linear regressions

Table 1. Comparing QS and NQS extraction results.

V_{gs} [V]	V_{ds} [V]	R_{ge} [Ω]	R_{de} [Ω]	R_{se} [Ω]	L_{ge} [pH]	L_{de} [pH]	τ [ps]	R_{gsi} [Ω]
				QS extraction				
1.0	2.0	13.0	4.2	6.2	37.0	47.6	0.0	0.0
1.0	1.0	13.0	6.6	7.5	41.4	53.0	0.0	0.0
0.5	1.5	14.5	3.4	7.8	38.0	56.8	0.0	0.0
				NQS extraction				
1.0	2.0	11.20	3.80	3.50	36.1	44.0	1.95	8.50
1.0	1.0	11.24	3.78	3.46	36.4	44.2	2.07	10.8
0.5	1.5	11.28	3.68	3.57	36.0	44.7	2.16	15.6

performed on data in the 500 MHz to 400 GHz band to extract the error term related to R_{se}.

Using the error terms, corrections can be applied to the QS series extrinsic elements: $\mathbf{R}''_{\sigma ij} = \mathbf{R}'_{\sigma ij} - \Delta\mathbf{R}'_{\sigma ij}$ and $\mathbf{L}''_{\sigma ij} = \mathbf{L}'_{\sigma ij} - \Delta\mathbf{L}'_{\sigma ij}$. Using the corrected values of the extrinsic series resistances and inductances (double quotes), the matrix $\mathbf{Z}_{\sigma}$ is reconstructed and substracted from the measured matrix $\mathbf{Z}_{\sigma\pi}$, to allow the extraction of the new estimates of the intrinsic elements according to the method of Berroth [5]. This method allows to determine individual values for the circuit parameters at every frequency point, so that the validity of the model can be assessed by checking whether the extracted parameters are constant across the measurement band. G''_{mi} proved to be very sensitive to variations of the initial value of R'_{gsi}. As shown in Fig. 8, an overestimated R'_{gsi} causes an upward bend of the G''_{mi}, while underestimation results in a downward bend, while a flat curve indicates a correct R'_{gsi} value. This feature can be exploited to guide an iterative bisection process where, at each step, a new value R''_{gsi} is chosen according to the observed profile of $G''_{mi}(\omega)$ over the measurement band. Using the new R'_{gsi} a better estimate of $\mathbf{Z}_{\pi}$ is reconstructed, yielding new extrinsic series resistances and inductances and finally the intrinsic parameters. The process is repeated until the G''_{mi}-profile is sufficiently flat.

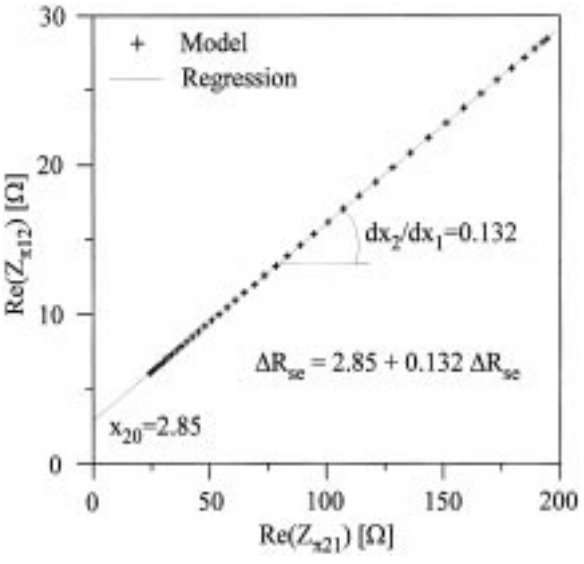


Fig. 7. Determining the NQS error terms related to R_{se} for $R_{gsi} = 10\,\Omega$.

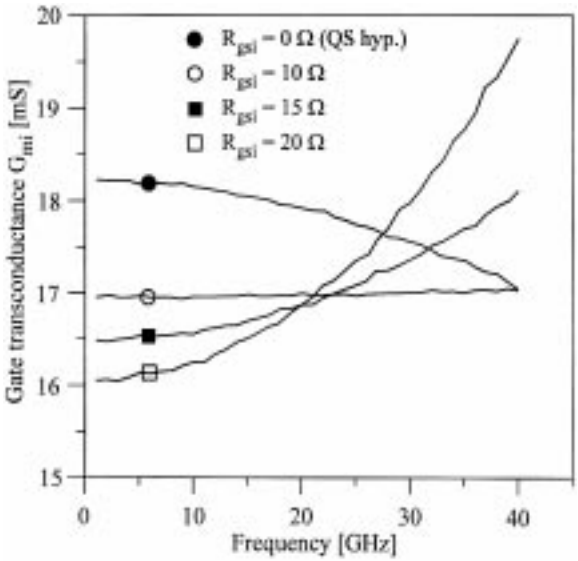


Fig. 8. G''_{mi} vs. frequency for various values of R'_{gsi}.

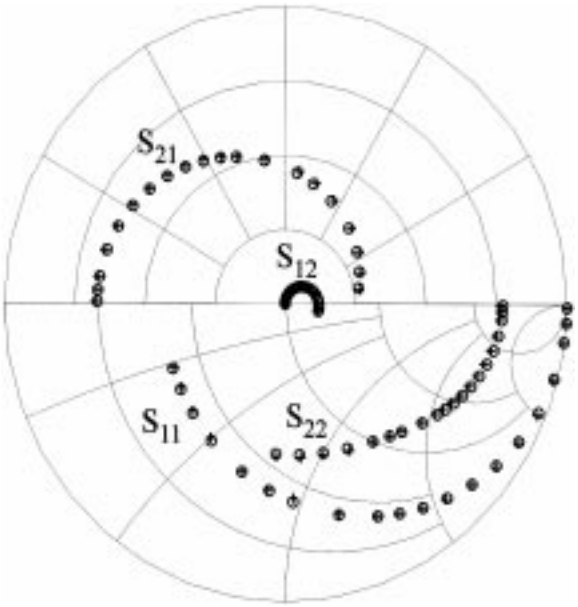


Fig. 9. Measured (○) and modeled (+) S-parameters from 500 MHz to 40 GHz for a 10 × (24 μm/0.75 μm) *n*-MOSFET, at $V_{gs} = 1$ V and $V_{ds} = 2$ V. The extracted circuit parameters are: $G_{mi} = 17$ mΩ, $\tau = 2.07$ ps, $C_{gsi} = 109$ fF, $R_{gsi} = 8.5$ Ω, $G_{ds} = 2.9$ mΩ, $C_{gse} = 40.5$ fF, $C_{dse} = 37$ fF, $R_{ge} = 11.2$ Ω, $R_{de} = 3.8$ Ω, $R_{se} = 3.5$ Ω, $L_{ge} = 36$ pH, $L_{de} = 44$ pH, $L_{se} = 0$ pH.

4.3. Results

The extraction procedure described above has been successfully applied to both enhancement-mode *n*-channel and accumulation-mode *p* channel SOI MOSFETs of various sizes. Fig. 9 shows the good agreement which is typically obtained between the measured S-parameters and the modeled response up to 40 GHz. The ability of the extraction procedure to identify correctly R_{gsi} and τ has been tested by performing extractions on a single device at different bias points. The results are summarized in Table 1. Despite important variations of R_{gsi} vs. bias, the series extrinsic resistances remain constant, as anticipated from technological considerations.

Taking into account the NQS effects allows to extract series resitance values which are very well correlated with technological data.

During the development of our SALICIDE processes [9], the new extraction procedure was used to monitor the impact of the various resistance lowering schemes. Table 2 illustrates the good correlation between the DC-measured resistivity of the various silicide materials and the series resistances extracted on the device themselves.

5. Noise Characterization

The recently published articles in the literature [2,7,11,16,21] and the extraction results presented in the previous section clearly show the potentialities of fully depleted SOI MOSFETs to provide high-quality microwave circuits needed in the new generation of portable personal digital RF communications terminals. The communication receiver sensitivity is mostly linked to the quality of the input low noise amplifier (LNA). The design of a LNA consists of many trade-offs between low noise figure, high gain, low input VSWR, high linearity and low power consumption assuming, of course, stability. Many recent works about the fabrication and optimization of LNAs in Si-based technologies (MOSFET or BJT) have been carried out. More particularly, concerning the CMOS noise performances, experimental and simulation results for the flicker noise (called also 1/*f* noise) are presented in the literature [42,44,51], but an accurate analysis of high frequency noise usually is omitted. Indeed, only the minimum noise figure $(F_{\min})$ is generally used for characterizing the high frequency noise performances of CMOS [2,16]. However, a recent work of Shaeffer [43] has demonstrated that high frequency noise properties (including drain and gate noise sources and their cross-correlation) of CMOS have to be taken into account to perform good LNA design. To achieve this aim, the extracted NQS small-signal model, as described in Section 4, and

Table 2. Extracted series resistances for various silicidation processes.

[Ω]	$TiSi_2$(6.2 Ω/□) R_{ge}	$CoSi_2$(4.4 Ω□) R_{de}	Nisi (2.8 Ω/□) R_{se}	R_{ge}	R_{de}	R_{se}	R_{se}	R_{ge}	R_{de}	R_{se}
n-MOS	11.2	3.8	3.5	8.1	2.1	1.5	4.2	1.0	1.2	
p-MOS				8.4	2.5	2.4	3.4	1.8	1.3	

the F_{50} method presented in [14] are applied together to characterize the high frequency noise of SOI MOSFETs.

Rothe et al. [40] have demonstrated that noise figure (F) of a noisy device is expressed completely by the four real terms: $F_{\min}, R_n, |\Gamma_{opt}|$ and $\mathrm{Arg}(\Gamma_{opt})$. For any generator reflection coefficient Γ_g the noise figure of the noisy device is given by:

$$F = F_{\min} + \frac{4R_n|\Gamma_g - \Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_g|^2)} \qquad (11)$$

$F_{\min}$ (minimum noise figure) represents the noise figure of the transistor when the input reflection coefficient Γ_g is tuned to the optimum input reflection coefficient Γ_{opt}. The noise resistance R_n measures the sensitivity of the noise figure to the mismatch ($\Gamma_g \neq \Gamma_{opt}$) at the input. In other words, R_n measures the sensitivity of the noise figure to changes in the source impedance and thus is an important parameter for optimizing microwave noise performances of MOSFETs. Different processes were run to study the influence of the effective channel length, the gate width and the gate sheet resistivity on the noise properties of MOSFETs developed in SOI technology.

5.1. *High Frequency Noise Model of Field Effect Transistor*

Since the beginning of the sixties, a large number of theorical and experimental studies about the high frequency noise mechanism of FETs have been published. In 1963, Van der Ziel calculated the gate and drain noise sources of the intrinsic FET (Fig. 10), respectively, $\overline{i_d^2}$, $\overline{i_g^2}$, and their correlation $\overline{i_g i_d^*}$ [49]. He showed the importance of the gate noise source even in moderate frequencies and demonstrated these two important features of his model:

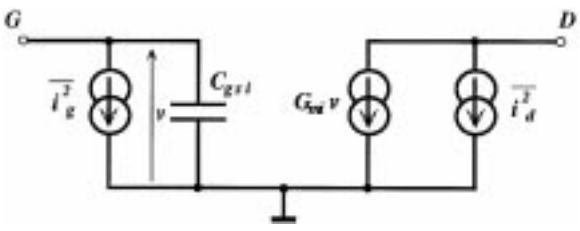


Fig. 10. Noise equivalent circuit of intrinsic FET: Van der Ziel's noise model.

1. The power spectral density of the drain current noise source $\overline{i_d^2}$ is frequency-independent. In fact, at high frequency, the FETs noise is a diffusion noise linked to the conducting channel and, therefore, the power spectrum of such a noise is ''white'' in the commonly used operating frequency band.
2. The real part of the correlation between the gate and drain current noise sources, $\overline{i_g i_d^*}$ is small compared to the imaginary part. Thus, the complex correlation coefficient C can be considered mainly imaginary (14).

From the noisy equivalent circuit represented in Fig. 10, the gate and drain current noise sources can be expressed by:

$$\overline{i_g^2} = 4kT\beta\frac{\omega^2 C_{gsi}^2}{G_{mi}}\Delta f \qquad (12)$$

$$\overline{i_d^2} = 4kT\alpha G_{mi}\Delta f \qquad (13)$$

$$C = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\cdot\overline{i_d^2}}} \approx j\,\mathrm{Im}(C) \qquad (14)$$

where T is the ambient temperature and α, β are dimensionless coefficients.

From this noise model, Van der Ziel defines the minimum noise figure by:

$$F_{\min} = 1 + 2\frac{f}{f_c}\sqrt{\alpha\beta(1-Im(C)^2)} \qquad (15)$$

where f is the operating frequency and f_c is the intrinsic cut-off frequency equal to $G_{mi}/2\pi C_{gsi}$.

Some authors [18,41,47], neglect the gate noise current source ($\overline{i_g^2}$), i.e. $\beta = 0$. Introducing this assumption in equation (15), we obtain an intrinsic minimum noise factor equal to 1. It means that the intrinsic minimum noise factor of any FETs is independent of the bias conditions, of the operation frequency, and even of the material properties composing the active layer of the transistor. This simple consideration clearly shows the physical nonsense of this assumption and therefore the importance of the accurate extraction of the high frequency noise parameters. Pucel [36] and Cappy [6] improved the FETs noise model proposed by Van der Ziel in taking into account the extrinsic noise sources. The resulting high frequency noise model for FETs, called PRC, is now available in the most of the microwave simulators. Following these pioneering works,

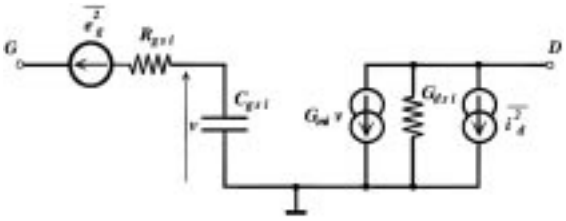


Fig. 11. Noise equivalent circuit of intrinsic FET: Popieszalski's noise model.

Pospieszalski [35] proposed the high frequency noise model presented in Fig. 11. The aim of this model is the dissociation of the noise sources at the gate and at the drain. The correlation between the noisy voltage-source at the input, $\overline{e_g'^2}$, and the noisy current-source at the output, $\overline{i_d'^2}$ is assumed to be zero: $e_g i_d'^* = 0$.

From these noise sources, Pospieszalski defined two equivalent noise temperatures T_g, and T_d:

$$T_g = \frac{\overline{e_g^2}}{4kR_{gsi}\Delta f} \tag{16}$$

$$T_d = \frac{\overline{i_d^2}}{4kG_{dsi}\Delta f} \tag{17}$$

Introducing the extrinsic noise sources (due to mainly the extrinsic resistances needed to assess until the intrinsic active part of the FET), by the same way, two uncorrelated noise sources called ''$T_{in} - T_{out}$'' are defined. Because all of the high frequency parameters ($F_{\min}, R_n$ and Γ_{opt}) can be defined from these two equivelent noise temperatures, this model is very suitable for the design of LNAs.

5.2. Characterization Procedure

All of the small-signal and noise parameters were measured by using a HP8510 network analyzer, a HP8971 noise measurement set-up and tungsten contact Cascade microwave probes. The parameters were measured up to 40 GHz and the noise figure parameters for a frequency band from 2 to 12 Hz. To increase the sensitivity of the noise measurement set-up, high quality isolators have been used to minimize the parasitic noise source coming from the receiver.

The noise equivalent circuit of the SOI MOSFET is presented in Fig. 12. The noise sources $\overline{e_{in}^2}$ and $\overline{i_{out}^2}$ are based on the Pospieszalski noise model and applied to the extrinsic device. The small-signal equivalent circuit elements are extracted from the S-parameters measurements as described in Section 4 of the paper. The four noise parameters ($F_{min}, R_n, |\Gamma_{opt}|$ and $Arg(\Gamma_{opt})$) are deduced by using the characterization method called ''F_{50}'' and described by Dambrine [14]. This method allows to extract all of the high frequency noise parameters from the noise figure of the transistor, measured with a single 50 Ω generator impedance, vs. frequency and the use of the two-uncorrelated noise temperatures as defined below in equations (18)–(20). Indeed, it can be shown that the parametric curve defined in a two dimensional plane by the FETs noise figure measured for a 50 Ω generator impedance and the frequency squared is a

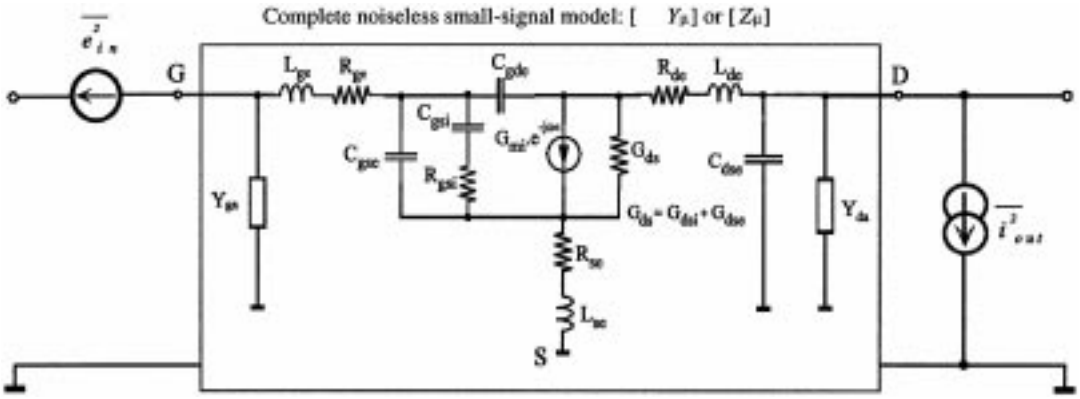


Fig. 12. Complete equivalent circuit of SOI MOSFET including two-uncorrelated noise sources.

straight line. It can be demonstrated that $|\Gamma_{opt}|$ and R_n are, respectively, related to the slope and the intercept at the origin of this measured linear function [14]. Two more equations are obtained by using the two uncorrelated noise sources $\overline{e_{in}^2}$ and $\overline{i_{out}^2}$ and thus, the four FETs noise parameters are extracted. The two equivalent noise temperatures T_{in} and T_{out} are given by:

$$T_{in} = \frac{\overline{e_{in}^2}}{4k\mathrm{Re}(1/Y_{\mu 11})\Delta f} \tag{18}$$

$$T_{out} = \frac{\overline{i_{out}^2}}{4k\mathrm{Re}(1/Z_{\mu 22})\Delta f} \tag{19}$$

$$\overline{e_{in} i_{out}^*} = 0 \tag{20}$$

with k the Bolzmann constant, Δf the noise measurements band-width, $\mathrm{Re}(\frac{1}{Y_{\mu 11}})$ the input Thevenin equivalent resistance and $\mathrm{Re}(\frac{1}{Z_{\mu 22}})$ the output Norton equivalent conductance. It is interesting to note that the experimental and theorical results presented, respectively, in Dambrine [12] and Danneville et al. [15] show that the value of T_{in} is close to the ambient temperature and almost independent of the bias drain current while T_{out} is strongly dependent on the drain current and its value can be as high as 1000–2000 K due to the hot electron effect. These references show also that the assumption of two uncorrelated noise sources remains valid under highly biased conditions. Using this noise measurement technique, the precision of the four extracted noise parameters depends on the noise measurement set-up sensitivity including a 50 Ω generator impedance (about $\pm$ 0.1 dB in the 2–12 GHz frequency range), the validity of the noise model and the accuracy of the extracted small-signal elements (described in Section 4).

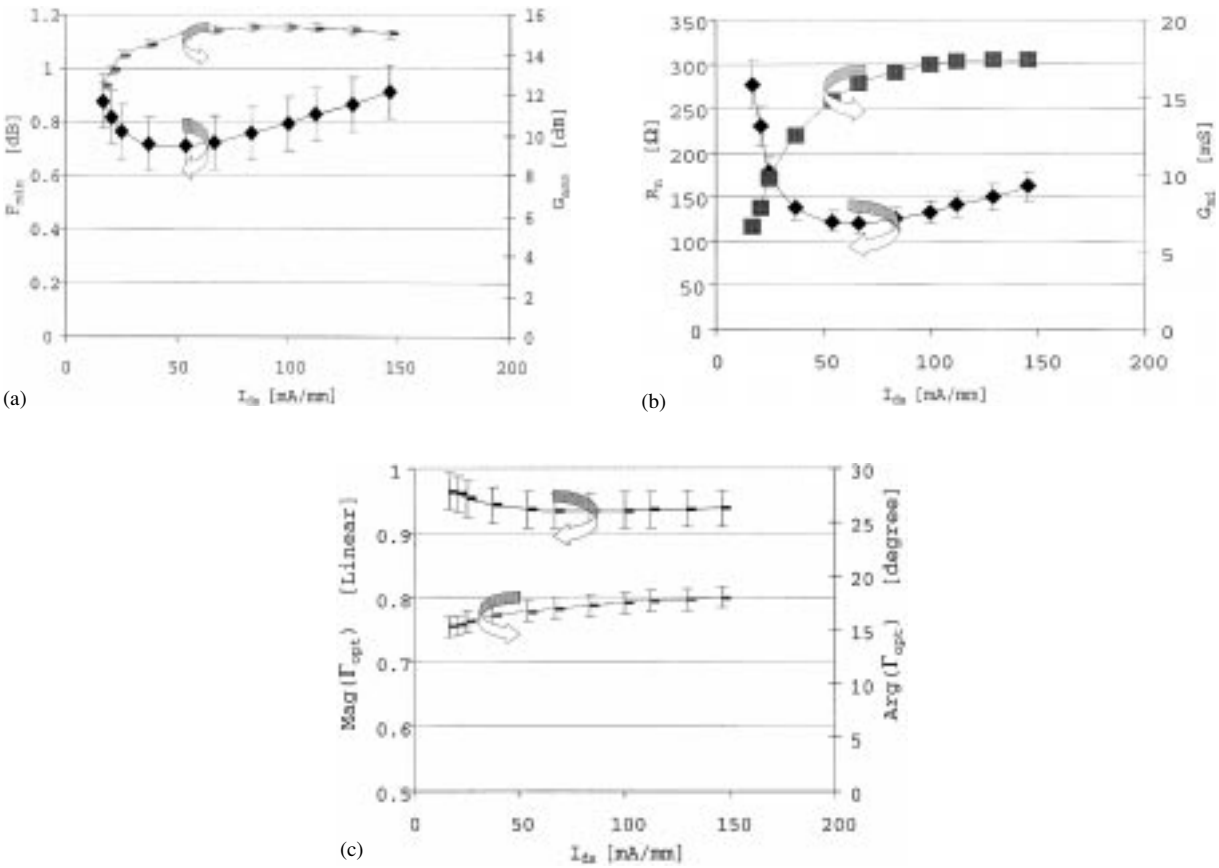


Fig. 13. Evolution of noise parameters vs. the drain-current density: $F_{\min}$ and $G_{ass}(a), R_n$ and $G_{mi}(b), |\Gamma_{opt}|$ and $Arg\ (\Gamma_{opt})(c)$.

5.3. Results

Fig. 13(a) shows the variation of the minimum noise figure (F_{min}) and the available associated gain (G_{ass}) as a function of the DC drain current (I_{ds}) at 2 GHz. G_{ass} is the available gain of the transistor when it is matched for minimum noise figure ($F_{\min}$). A minimum noise figure of about 0.7 dB and an associated available gain of 15 dB are obtained at 2 GHz for a drain current density close to 60 mA/mm ($V_{ds} = 2V$). For a 0.75 μm gate length MOSFET using a completely conventional and CMOS-compatible fabrication process, this minimum noise figure is one of the best reported in the literature.

Fig. 13(b) presents the variation of the equivalent noise resistance R_n and the intrinsic gate transconductance G_{mi} as a function of the drain current. A minimum value of R_n (122 Ω) is obtained for a drain current density close to 60 mA/mm. At lower current density, the high value of R_n is due to the low value of the intrinsic gate transconductance according to the following approximate equation:

$$R_n \approx (R_{ge} + R_{se} + R_{gsi})\frac{T_g}{T_o} + \frac{T_d}{T_o}\frac{G_{dsi}}{G_{mi}^2} \qquad (21)$$

where $R_{ge}, R_{se}, R_{gsi}, G_{mi}$ and G_{dsi} are, respectively, the extrinsic gate and source resistances, the intrinsic resistance, gate transconductance and output conductance (as defined in Section 4), T_g and T_d are the gate and drain equivalent noise temperatures defined previously and $T_0 = 290\,K$.

It will be shown hereafter that the reduction of this equivalent resistance will be one of the major preoccupation faced when trying to perform low noise matching conditions. As compared with III-V MESFET or HEMT, this equivalent resistance is three to ten times higher. Fig. 13(c) shows the variation of the magnitude and the argument of the optimal reflection coefficient Γ_{opt} vs. the drain current. The magnitude of Γ_{opt} is close to the unity and almost independent of the bias conditions. The value of this noise parameter is also a strong hindrance to obtain the minimum noise condition for LNAs design.

5.3.1. Noise Parameters Versus Gate Length L_{eff}. Fig. 14 show the variation of the four noise parameters for the operation frequency of 2 GHz as a function of the effective gate length (L_{eff}) for various

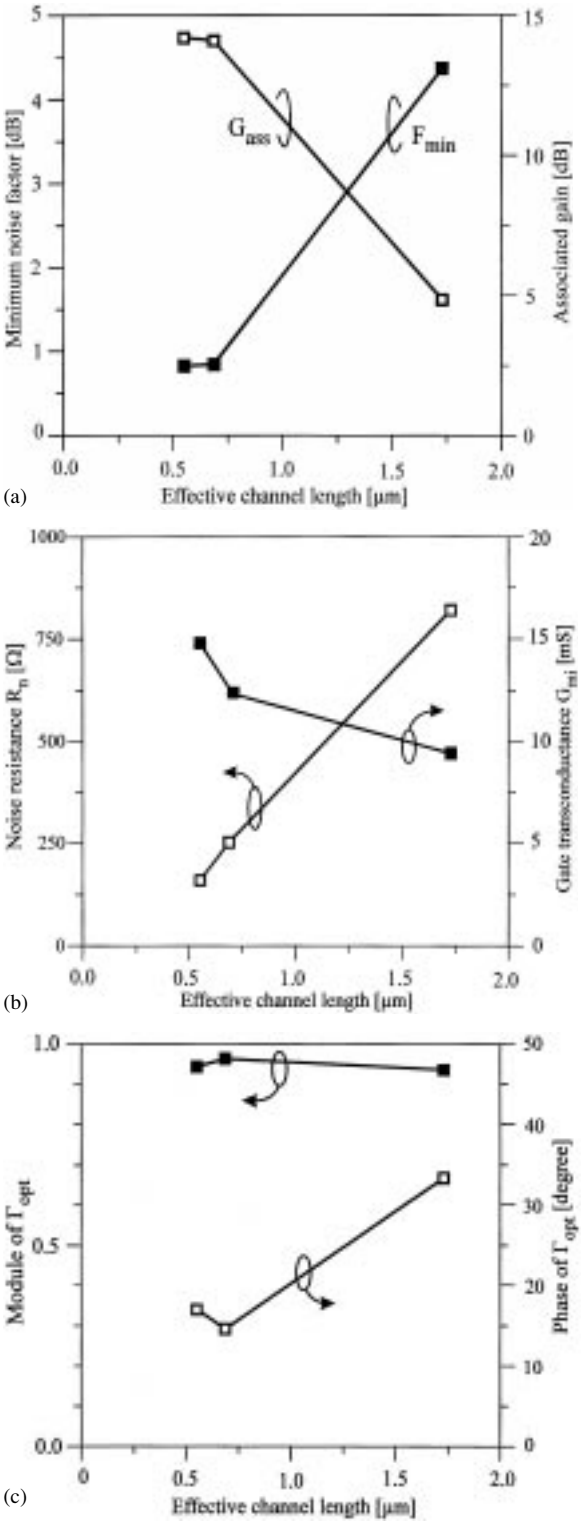


Fig. 14. Evolution of noise parameters vs. the channel gate length: $F_{\min}$ and $G_{ass}(a), R_n$ and $G_{mi}(b), |\Gamma_{opt}|$ and $Arg(\Gamma_{opt})(c)$.

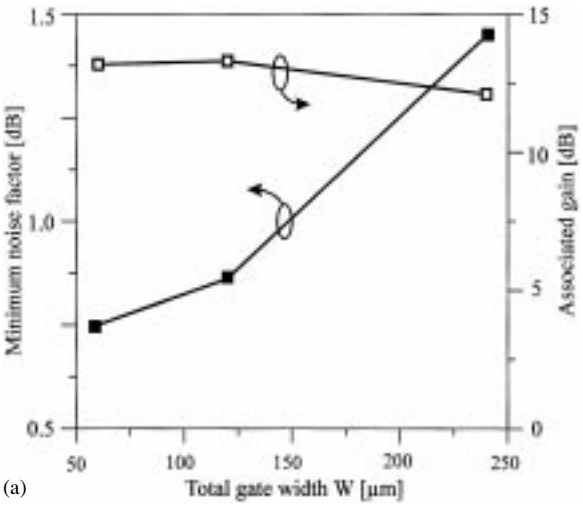
SOI MOSFETs from the same process. Each transistor is biased under low noise conditions, the drain current density is 55 nA/mm and the drain voltage is 2 V. As shown in Fig. 14, the minimum noise figure decreases with the gate length. As it is well known [6,35], this variation is strongly linked to the increase of the intrinsic cutoff frequency (f_c) when the gate length decreases, according to the following approximate relations:

$$F_{\min} \approx 1 + \frac{2}{T_o}\frac{f}{f_c}\left[\sqrt{(Rge + R_{se} + R_{gsi})T_g G_{dsi} Td} + \frac{f}{f_c}(R_{ge} + R_{se} + R_{gsi})T_g G_{dsi}\right]$$

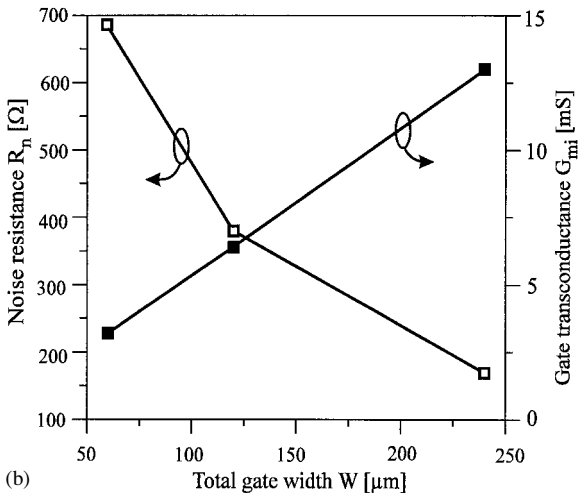
with

$$f_c = \frac{G_{mi}}{2\pi C_{gsi}} \propto \frac{1}{L_{eff}^2} \tag{22}$$

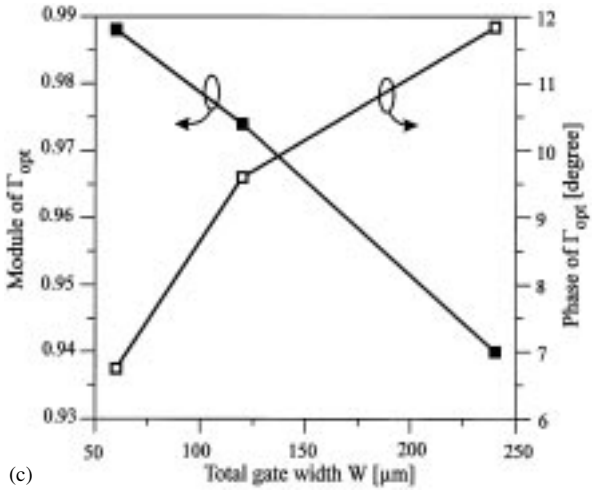
However, the decrease rate of $F_{\min}$, diminishes for L_{eff} smaller than 0.7 μm because the increase of R_{ge} with the reduction of L_{eff} becomes dominant in (22). Fig. 14(b) shows the evolution of equivalent noise resistance (R_n) and intrinsic transconductance (G_{mi}) as a function of effective gate length. The variation of R_n agrees well with expression (21) and is due to the increase of G_{mi} when the effective gate length decreases. On the other hand, Fig. 14(c) shows that



(a)



(b)



(c)

Fig. 15. Evolution of noise parameters vs. the channel gate length W: $F_{\min}$ and $G_{ass}(a), R_n$ and $G_{mi}(b), |\Gamma_{opt}|$ and $Arg(\Gamma_{opt})(c)$.

the magnitude of Γ_{opt} is almost independent of the effective gate length and close to the unity.

5.3.2. Noise Parameters vs. Gate Width W. Fig. 15 show the evolutions of noise parameters at the operating frequency of 2 GHz vs. the total gate width for various SOI nMOS-FETs. The bias conditions are a drain voltage of 2 V and a drain current density of 25 mA/mm. Fig. 15(a) presents the variation of the minimum noise figure and the available associated gain as a function of gate width. From a theoretical point of view, if we consider the intrinsic equivalent circuit only, it can be proved that $F_{\min}$ is independent of gate width (W) [6,15]. The increase of $F_{\min}$ in the case of the largest width device is due partly to the access resistance and, more particularly, to the gate resistance R_{ge} (22). As shown in Fig. 15(b), the intrinsic transconductance G_{mi} increases with the gate width (in fact, $G_{mi} \propto W/L$) while the equivalent noise resistance R_n decreases. This evolution agrees quite well with expression (21). Fig. 15(c) shows the slight reduction of $|\Gamma_{opt}|$ while its argument increases with the total gate width of the transistor (W). The intrinsic optimal admittance Y_{opt} proposed by Pospieszalski [35] allows us to explain the evolutions of Γ_{opt} vs. the transistor width:

$$Y_{opt} \approx \frac{f}{f_c}\left[\sqrt{\frac{G_{dsi}T_d}{R_{gsi}T_g}} + j\left(\frac{G_{dsi}T_d}{G_{mi}R_{gsi}T_g}\right)\right] \quad (23)$$

The intrinsic gate transconductance (G_{mi}) and the ouput conductance (G_{dsi}) are proportional to the gate width (W) while the intrinsic resistance (R_{gsi}) is proportional to $1/W$. As a consequence, Y_{opt} is proportional to the gate width, which explains the slight decrease in the magnitude of Γ_{opt} when the transistor gate width increases. This feature is interesting to improve the matching conditions at the transistor input. Also, it is interesting to note that Y_{opt} (23) and $F_{\min}$ (22) are both of them proportional to the ratio f/f_c. Therefore, a decrease of $|\Gamma_{opt}|$ is obtained by reducing f_c whereas the improvement of $F_{\min}$ needs high values of f_c. This trade-off has to be considered for optimizing the LNAs performances.

5.3.3. Noise Parameters for Various SALICIDE Processes. Various SALICIDE processes described in Section 2 are tested to reduce the sheet gate, drain and source resistances and thus improve the high frequency performances of SOI MOSFETs. In opposition to the dedicated MOS process, called ''MICROX'' [2], which uses non-standard CMOS features, such as a metal (gold) gate and air-bridge metallization, the salicide process is a fabrication step compatible with a standard fully-depleted SOI CMOS process [8]. The gate sheet resistance before the SALICIDE process is of about 30 Ω/□. This value corresponds to the resistivity of the heavily doped *n*-polysilicon. After the salicide process with $TiSi_2$, $CoSi_2$ and NiSi, the sheet gate resistance are 6.2, 4.4 and 2.8 Ω/□, respectively [9]. Fig. 16 presents $F_{\min}$ and R_n of SOI *n*-MOSFETs with a total gate width W of 240 μm and channel length of 0.75 μm vs. the gate resistivity in Ω/□. The values of $F_{\min}$ and R_n are measured at 2 GHz and for fixed drain current density of 50 mA/mm. The experimental results obtained for $F_{\min}$ and R_n are in accordance with the relations (22) and (21), respectively. $F_{\min}$ and R_n decrease with a reduction of the extrinsic series resistances R_{ge} and R_{se}. The best noise performances are obtained with the nickel silicidation because which presents the smallest sheet gate resistance (2.8 Ω/□).

5.3.4. Summary and Discussion. First, through the relations (21)–(23) the importance of an accurate and physical extraction procedure for the small-signal elements on the noise performances modeling is clearly shown.

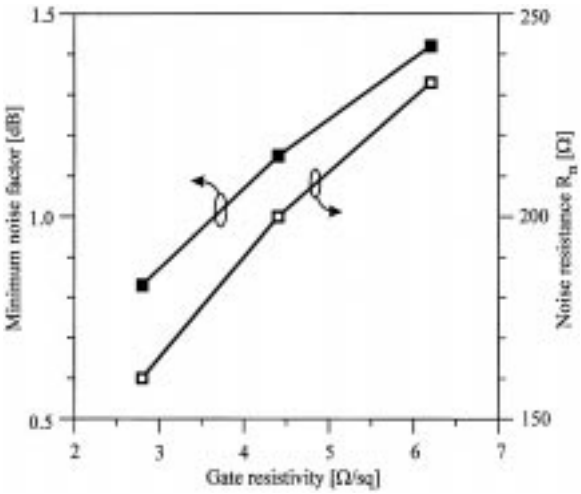


Fig. 16. Evolution of minimum noise figure and equivalent noise resistance vs. sheet gate resistance.

Second, this study underlines two important useful points for the design of microwave low noise circuits:

1. MOSFETs processed on SOI technology can be used as very low noise device for the realization of multi-gigahertz radio communication receivers. Indeed, a minimum noise figure of 0.7 dB at 2 GHz, with an associated available gain of 15 dB, has been obtained in the case of a 0.75 μm gate length standard MOSFET process. This noise performance is very promising for lower gate length processes for applications in upper frequency ranges.
2. The main limitation of MOSFETs for the realization of ultra low noise circuits comes from the difficulty of obtaining the noise-matching condition. The equivalent noise resistance (R_n) of MOSFET may be three to ten times higher than comparable III-V devices due to the relatively low value of the intrinsic transconductance in the case of silicon MOS devices. Then, when $|\Gamma_{opt}|$ is close to unity, the noise-matching condition is difficult to meet and the high value of R_n means that the noise figure of LNA degrades rapidly as the admittance of the generator departs from $|\Gamma_{opt}|$. This sensitivity of the LNA noise figure to the input loads is shown in Fig. 17 which represents the constant noise figure circles of a SOI MOSFET with a channel length of 0.65 μm and a gate width of 240 μm. Although the minimum noise figure of this device is less than 1 dB at 2 GHz the noise figure of an hypothetical LNA, using such a device with an integrated spiral inductor [25] (for instance 10 nH), would be at least 3 dB at 2 GHz. One of the best-published results is 2.8 dB [1] at 2.4 GHz for a 0.5 μm Silicon-On-Sapphire CMOS process LNA. This difficulty to implement optimal balding conditions for a minimum noise figure using CMOS devices gives a slight advantage to bipolar based LNA designs [24,46,52].

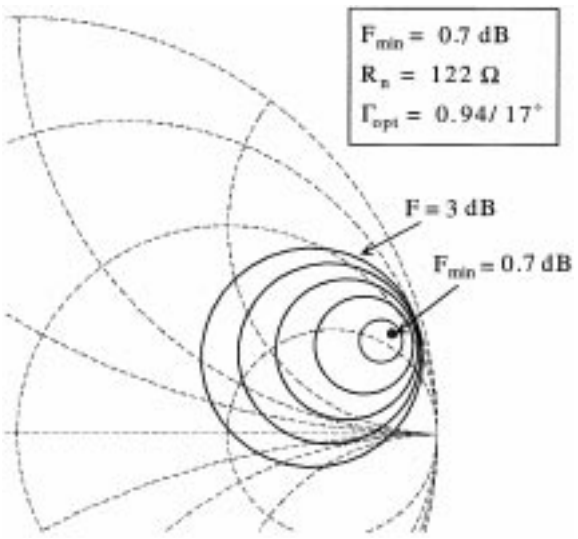


Fig. 17. Constant noise figure circles at 2 GHz for a 0.65 μm channel length transistor composed of 10 gate fingers having 24 μm each. The values of the noise parameters are: $G_{ass} = 15\,\text{dB}, F_{\min} = 0.7\,\text{dB}, R_n = 122\,\Omega, |\Gamma_{opt}| = 0.94$ and $Arg(\Gamma_{opt}) = 17°$).

Table 3. Comparing noise parameters for a 10 × (24 μm/0.75 μm) *n*-MOSFET (measured) and for a 20 × (24 μm/0.75 μm) *n*-MOSFET (calculated).

Device	F_{min} (dB)	R_n (Ω)	$\lvert\Gamma_{opt}\rvert$	$Arg(\Gamma_{opt})$	G_{ass} (dB)
10 × (24 μm/0.75 μm)	1.1	143	0.92	15°	13.2
20 × (21 μm/0.75 μm)	1.2	72	0.84	33°	12.5

The present work shows some solutions for improving this matching difficulty. For instance, using the experimental results obtained for W equal to 60, 120, and 240 μm, it is straightforward to calculate the noise characteristics of hypothetical 0.75 μm SOI MOSFETs composed of 20 fingers having a length of 24 μm each $(W = 480\,\mu\text{m})$. The calculated noise parameters are given in Table 3.

Table 3 shows that R_n is twice lower for the large device and $|\Gamma_{opt}|$ is slightly lower while $F_{\min}$ keeps almost the same value. Similarly, Fig. 18 shows the

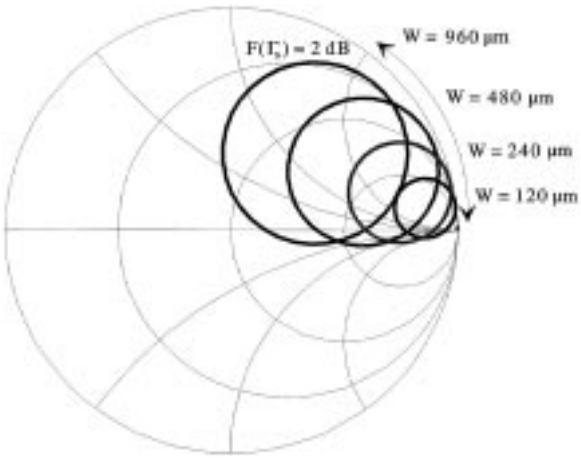


Fig. 18. Calculated constant 2 dB noise figure circles at 2 GHz, for hypothetical 120–960 μm gate-width devices.

calculated constant noise figure circles ($F = 2$ dB) for gate width devices from 120 to 960 μm. It appears clearly that the trade off between the noise figure and, for instance, the input reflection coefficient of a LNA is easier to obtain in the case of a larger gate-width device than a lower gate-width one. Moreover, the inductance values needed to design the input and output matching networks are lower, therefore less noisy, in the case of a larger device.

6. Conclusion

An accurate characterization procedure for MOSFETs has been demonstrated. After correction of the residual shunt admittances, all the small-signal circuit elements values are determined from S-parameters measurements at a single bias point in saturation. By splitting the extraction into simple linear regression problems, the new scheme manages to achieve high efficiency and accuracy at the cost of very little sophistication. This new characterization scheme, has proven to be an efficient tool for analog modeling and for the optimization of device performances (including the high frequency noise parameters). The importance of the NQS elements extraction for obtaining an accurate and physical MOSFET model has been demonstrated. Using a characterization procedure based on the extracted NQS small-signal FET model and its noise temperatures measured under 50 Ω, the four high frequency noise parameters have been determined for different topologies of SOI MOSFETs. It has been shown that the main limitation of MOSFETs for the realization of ultra low noise circuits comes from the difficulty to satisfy the no matching condition.

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Appendix

A. NQS Impedance Equations

The starting point is the circuit equation shown in (1a). Using the analytical expression for the elements of $\mathbf{Y}_\pi$ (1e), the matrix inverse is expanded in function of the circuit parameters. After some simplifications, a set of equations is obtained which can be mapped onto the following generic notations:

$$\mathrm{Re}(\mathbf{Z}_{\sigma\pi ij}) = \mathrm{Re}(\mathbf{Z}_{\sigma ij}) + \frac{P_{ij(0)} + P_{ij(2)}\omega^2}{N_{(0)} + N_{(2)}\omega^2} \quad \text{for } i, j \in \{1,2\} \tag{24}$$

$$\frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma\pi ij}) = \frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma ij}) + \frac{Q_{ij(0)} + Q_{ij(2)}\omega^2 + Q_{ij(4)}\omega^4}{\omega^2(N_{(0)} + N_{(2)}\omega^2)} \quad \text{for } i, j \in \{1,2\} \tag{25}$$

Performing a simple polynomial division, equations (24) and (25) are transformed into (26) and (27). In the latter equations, all terms are in a one-to-one correspondance with those from equations (9) and (10). These equations shown that the parametric curves must be straight lines and that the NQS effects are affecting the extracted of series resistances and inductances:

$$\mathrm{Re}(\mathbf{Z}_{\sigma\pi ij}) = \mathrm{Re}(\mathbf{Z}_{\sigma ij}) + \frac{P_{ij(2)}}{N_{(2)}} + \frac{P_{ij(0)} + P_{ij(2)}/N_{(2)}N_{(0)}}{N_{(0)} + N_{(2)}\omega^2} \quad \text{for } i, j \in \{1,2\} \tag{26}$$

$$\frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma\pi ij}) = \frac{1}{\omega}\mathrm{Im}(\mathbf{Z}_{\sigma ij}) + \frac{Q_{ij(4)}}{N_{(2)}} + \frac{Q_{ij(2)} - Q_{ij(4)}/N_{(2)}N_{(0)}}{N_{(0)} + N_{(2)}\omega^2} + \frac{Q_{ij(0)}}{\omega^2(N_{(0)} + N_{(2)}\omega^2)} \quad \text{for } i, j \in \{1,2\} \tag{27}$$

Equations below are the analytical expressions of all the polynomial coefficients involved in equations (24) and (25). All these coefficients are frequency independent. In the equations below $G_{ds} \triangleq (G_{dsi} + G_{dse})$

$$P_{11(2)} = C_{gde}^2(R_{gsi}^2 C_{gsi}^2 G_{ds} + R_{gsi} C_{gsi}^2 - R_{gsi} C_{gsi} G_{mi}\tau - \frac{1}{2} G_{mi}\tau^2) - \frac{1}{2} R_{gsi} C_{gsi} G_{mi}\tau^2 C_{gse} G_{ds} \quad (28)$$

$$P_{12(2)} = C_{gde}^2 R_{gsi}^2 C_{gsi}^2 G_{ds} + (C_{gse} C_{gde}) + C_{gde}^2 \left(R_{gsi} C_{gsi}^2 - G_{mi}\tau R_{gsi} C_{gsi} - \frac{1}{2} G_{mi}\tau^2 \right) \quad (29)$$

$$P_{21(2)} = C_{gde} R_{gsi}^2 C_{gsi}^2 G_{ds}(C_{gse} + C_{gde}) + C_{gde}^2 \left(R_{gsi} C_{gsi}^2 - G_{mi}\tau R_{gsi} C_{gsi} - \frac{1}{2} G_{mi}\tau^2 \right) - \frac{1}{2} R_{gsi} C_{gsi} G_{mi}\tau(C_{gde} G_{ds}\tau + 2C_{gse} C_{gde} + \tau C_{gse} G_{ds}) - \frac{1}{2} G_{mi}\tau^2 C_{gde}(C_{gsi} + C_{gse}) \quad (30)$$

$$P_{22(2)} = R_{gsi}^2 C_{gsi}^2 G_{ds}(C_{gde} + C_{gse})^2 + C_{gde}^2 R_{gsi} C_{gsi}^2 - R_{gsi} C_{gsi} G_{mi}\tau C_{gde}(C_{gde} + C_{gse}) - \frac{1}{2} C_{gde} G_{mi}\tau^2 (C_{gsi} + C_{gse} + c_{gde}) \quad (31)$$

$$P_{11(0)} = G_{ds}^2 R_{gsi}^2 C_{gsi}^2 + R_{gsi} C_{gsi} G_{mi} G_{ds} C_{gde} + C_{gde}^2(G_{ds} + G_{mi}) + G_{mi}\tau C_{gde} G_{ds} \quad (32)$$

$$P_{12(0)} = C_{gde} G_{ds}(C_{gse} + C_{gsi} + C_{gde}) + C_{gde}^2 G_{mi} \quad (33)$$

$$P_{21(0)} = C_{gde}(C_{gsi} + C_{gse} + C_{gde})(G_{mi} + G_{ds}) + G_{mi}\tau G_{ds}(C_{gsi} + C_{gse} + C_{gde}) + G_{mi} R_{gsi} C_{gsi} G_{ds}(C_{gse} + C_{gde}) \quad (34)$$

$$P_{22(0)} = C_{gde}^2(G_{mi} + G_{ds}) + G_{ds}(C_{gse} + C_{gsi})^2 + C_{gde}(G_{mi} + 2G_{ds})(C_{gse} + C_{gsi}) \quad (35)$$

$$N_{(0)} = G_{ds}^2(C_{gde} + C_{gse} + C_{gsi})^2 + C_{gde}^2 G_{mi}^2 + 2C_{gde} G_{ds} G_{mi}(C_{gde} + C_{gse} + C_{gsi}) \quad (36)$$

$$N_{(2)} = C_{gde}^2[(C_{gse} + C_{gsi})^2 - 2G_{mi}\tau(C_{gse} + C_{gsi}) + 2G_{ds} C_{gsi}^2 R_{gsi}] - 2C_{gde} G_{mi} R_{gsi} C_{gsi} \times [C_{gse} C_{gde} + (C_{gse} + C_{gde}) G_{ds}\tau] - G_{ds} C_{gde} G_{mi}\tau^2(C_{gde} + C_{gse} + C_{gsi}) + G_{ds}^2 R_{gsi}^2 C_{gsi}^2 (C_{gde} + C_{gse})^2 \quad (37)$$

$$Q_{11(0)} = -G_{ds}^2(C_{gde} + C_{gse} + C_{gsi}) - G_{mi} C_{gde} G_{ds} \quad (38)$$

$$Q_{12(0)} = 0 \quad (39)$$

$$Q_{21(0)} = G_{mi} G_{ds}(C_{gde} + C_{gse} + C_{gsi}) + C_{gde} G_{mi}^2 \quad (40)$$

$$Q_{22(0)} = 0 \quad (41)$$

$$Q_{11(2)} = C_{gde}^2(R_{gsi} C_{gsi} G_{mi} - C_{gsi} - C_{gse} + G_{mi}\tau) - R_{gsi}^2 C_{gsi}^2 G_{ds}^2(C_{gse} + C_{gde}) + G_{mi}\tau C_{gde} G_{ds} \times \left(R_{gsi} C_{gsi} + \frac{1}{2\tau} \right) \quad (42)$$

$$Q_{12(2)} = C_{gsi}^2 C_{gde} G_{ds} R_{gsi} - C_{gde}^2 \times [C_{gse} + C_{gsi} - G_{mi}(R_{gsi} C_{gsi} + \tau)] \quad (43)$$

$$Q_{21(2)} = C_{gde} R_{gsi} C_{gsi}^2 G_{ds} - R_{gsi} C_{gsi} G_{mi} \times [\tau G_{ds}(C_{gde} + C_{gse}) - C_{gde}^2 + C_{gse} C_{gde}] - \frac{1}{2} G_{mi}\tau^2 G_{ds}(C_{gde} + C_{gse} + C_{gsi}) - G_{mi}\tau C_{gde}(C_{gsi} + C_{gse} - C_{gde}) - C_{gde}^2(C_{gsi} + C_{gse}) \quad (44)$$

$$Q_{22(2)} = C_{gde}^2(G_{mi}\tau - C_{gsi} - C_{gse}) - C_{gde})C_{gse} + C_{gsi}(C_{gse} + C_{gsi} - G_{mi}\tau) + R_{gsi} C_{gsi} C_{gde} G_{mi}(C_{gse} + C_{gde}) \quad (45)$$

$$Q_{11(4)} = -R_{gsi}^2 C_{gsi}^2 C_{gde}^2 C_{gse} - \frac{1}{2} R_{gsi} C_{gsi} C_{gsi}^2 G_{mi}\tau^2 \quad (46)$$

$$Q_{12(4)} = -C_{gde}^2 R_{gsi} C_{gsi} (C_{gse} R_{gsi} C_{gsi} + \frac{1}{2} G_{mi} \tau^2) \quad (47)$$

$$Q_{21(4)} = \frac{1}{4} G_{mi}^2 \tau^4 C_{gde} - \frac{1}{2} R_{gsi} C_{gsi} G_{mi} \tau^2 C_{gde} \times (C_{gde} - C_{gse}) - C_{gde}^2 R_{gsi}^2 C_{gsi}^2 C_{gse} \quad (48)$$

$$Q_{22(4)} = -R_{gsi}^2 C_{gsi}^2 C_{gse} C_{gde} (C_{gse} + C_{gde}) - \frac{1}{2} R_{gsi} C_{gsi} \times G_{mi} \tau^2 C_{gde} (C_{gse} + C_{gde}) \quad (49)$$

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