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A generic micromachined silicon platform for high-performance RF passive components

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Abstract. This paper describes the development of a micromachined silicon platform fabricated using the dissolved wafer process that supports: (1) high self-resonance frequency and quality factor inductors suspended on a dielectric membrane, (2) low-loss thin-film capacitors, and (3) polysilicon resistors. The process uses deep boron diffusion to create silicon anchors, which support a stress compensated dielectric membrane. A thick resist mold is used to gold electroplate the inductor, top capacitor plate, and bonding pads. This platform can be used to build miniature high-performance transceivers or other RF subsystems using either hybrid-attached surface-mount components or flip-chip bonded RF circuits. Using this technique, a Colpitts transmitter with a five-turn dielectric suspended inductor was designed and fabricated. The transmitter oscillates in the frequency band of 275–375 MHz, consumes 200 μA when operated continuously and 100 μA when amplitude modulated (on–off keying) at a rate of 1 Mbps (50% duty cycle).

1. Introduction

Wireless personal communications and instrumentation microsystems are in high demand [1, 2]. Their scope of applications is wide and includes consumer electronics, military, manufacturing, biomedical, security, transportation, and environmental monitoring. High-performance low-power RF transceivers are an integral part of many of these emerging microsystems. The current technological trend is towards using silicon to implement many of the RF subsystems previously realized with compound semiconductor materials [3, 4]. This will eventually lead to lower costs, higher levels of integration, and the ability to include both the sensing and actuating components with the signal processing and RF circuitry. Recent improvements in Si/SiGe heterojunction bipolar transistors (HBT) have pushed their cutoff frequencies to beyond 200 GHz [3, 5]. In addition, the state-of-the-art bulk CMOS technology can offer a viable option for RF designs into the 2 GHz range [4]. However, integration of high-performance lumped or distributed passive components on the silicon substrate remains a challenging task due to the substrate loss and various parasitics [6]. For example, the limiting factors in achieving integrated inductors with high self-resonance frequency and quality factor fabricated on silicon are: substrate and metal series resistance loss (limiting the Q), and parasitic capacitance to the substrate (reducing the self-resonance frequency and the Q). Various techniques have been used to overcome these shortcomings, including: (1) selective removal of the substrate under the inductor [7], (2) using thick dielectric layers [8], (3) multilevel metallization [9, 10], and (4) electroplating [11]. Incorporating these techniques into integrated circuits requires added process complexity associated with multilevel metallization, thick dielectric deposition, and front-side etching which is dependent on crystal orientation.

In this paper, we present the development and application of a generic micromachined silicon platform that supports high-performance lumped-element RF passive components. These include: high self-resonance frequency and quality factor inductors, low-loss thin-film capacitors, and polysilicon resistors. With proper design, these components can be used at frequencies up to about 20 GHz where the lumped-element approximation is still valid (i.e. the dimensions $<\lambda/10$). Section 2 describes the overall structure of the silicon platform followed by the component design and models in section 3. Section 4 discusses the fabrication process followed by the measurement and test results in section 5. Finally, section 6 draws some conclusions from the results of this work.

2. Overall platform structure

Figure 1 shows the micromachined silicon platform mounted on a glass back-plate for mechanical support. As can be seen, all the passive elements are fabricated on the silicon substrate and electroplated bonding pads are provided for

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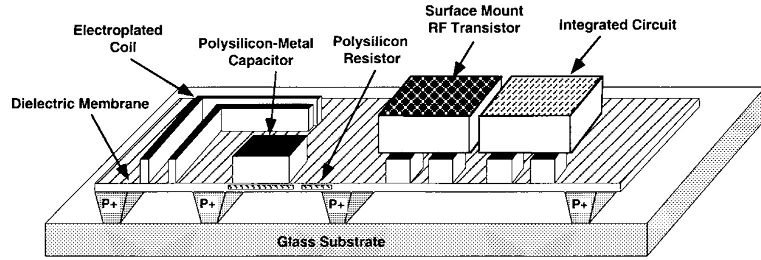

Figure 1. Micromachined silicon platform with surface mount RF transistor, RF integrated circuit, and glass back-plate support.

attachment of discrete active components or flip-chip bonded RF circuits. This platform is fabricated by the dissolved wafer process (see section 4), which uses a deep boron diffusion step to create silicon anchors supporting a stress compensated dielectric membrane. Various passive components including: (1) high self-resonant frequency and quality factor inductors, (2) low-loss thin-film capacitors, and (3) polysilicon resistors, are fabricated on top of the membrane. This technique is simple, saves area, alleviates the need for front-side etching, and does not require multilevel metallization. In addition, various components can be optimized independently for the required application. The capacitive parasitics associated with the surface mount device pads can also be minimized by suspending them on the membrane. The removal of the silicon from underneath the inductor reduces the substrate loss and parasitic capacitances to the substrate. This, in addition to electroplating a thick gold layer, increases the quality factor and self-resonance frequency of the inductor. Thin-film capacitors can achieve low loss through the deposition of high-quality LPCVD dielectric layers and low-resistivity metal plates. Polysilicon resistors can be used to design high-value resistors in low-power applications. This platform can be used to build miniature transceivers or other RF subsystems, either stand-alone to support hybrid attached surface-mount transistors, or flip-chip bonded to RF circuits on an integrated chip, thus saving valuable area.

3. Components design and models

In order to accurately design and predict the behavior of various passive components, lumped-element circuit models were used. Figure 2 shows the physical models used to design the inductor, and the capacitor [12]. The inductor is modeled by L_s, representing the low-frequency inductance, R_s modeling the series resistance having a frequency dependence related to the skin effect and other high frequency effects, C_o and C_{ox} representing the fringing and the metal layer to the substrate capacitances, and finally R_{sub} and C_{sub} modeling the substrate resistance (due to the eddy currents) and capacitance. Removing the semiconducting substrate from underneath the inductor eliminates the effects of C_{ox}, C_{sub}, and R_{sub}. Therefore, one only needs to optimize the values of L_s, R_s, and C_o in order to achieve the required self-resonance frequency and quality factor. Figure 3 shows the layout geometry and cross section of the coil. Equation (1) can be used to calculate the low-frequency inductance of an air-core rectangular planar inductor [13].

$$L \approx \frac{45\mu_o n^2 a^2}{22r - 14a}. \tag{1}$$

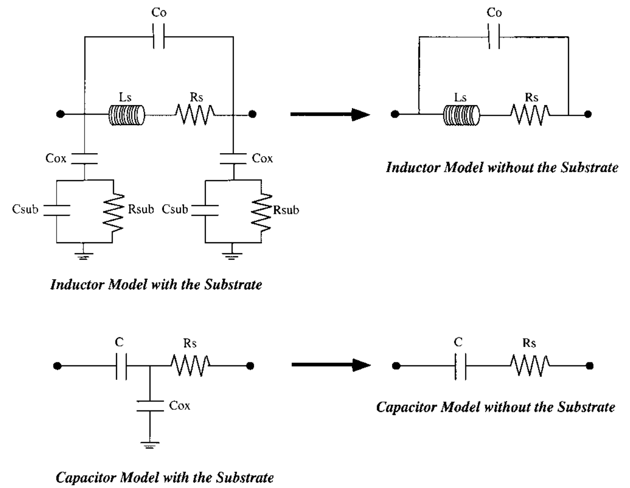

Figure 2. Lumped element circuit models for an inductor and a thin-film capacitor with and without the substrate.

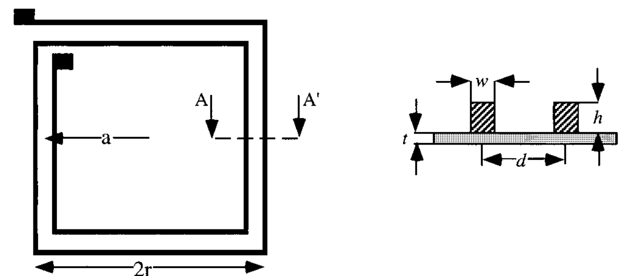

Figure 3. Layout geometry and cross section of an integrated coil.

In this equation, μ_o is the permeability, n is the number of turns, a is the square spiral's mean radius, and r is the outer radius of the spiral (see figure 3). Measurement and simulation results indicate that the formula is accurate to within 5%, which is adequate for most applications [14]. The series resistance R_s includes a dc and a frequency dependent component. The dc component can be easily calculated by knowing the coil dimensions and metal resistivity. The frequency dependent component has to account for the skin effect (equation (2)), and magnetic fields. The combined effects can be modeled by equation (3) [15].

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{2}$$

$$R_s = \frac{\rho l}{w\delta(1 - \mathrm{e}^{-h/\delta})} \tag{3}$$

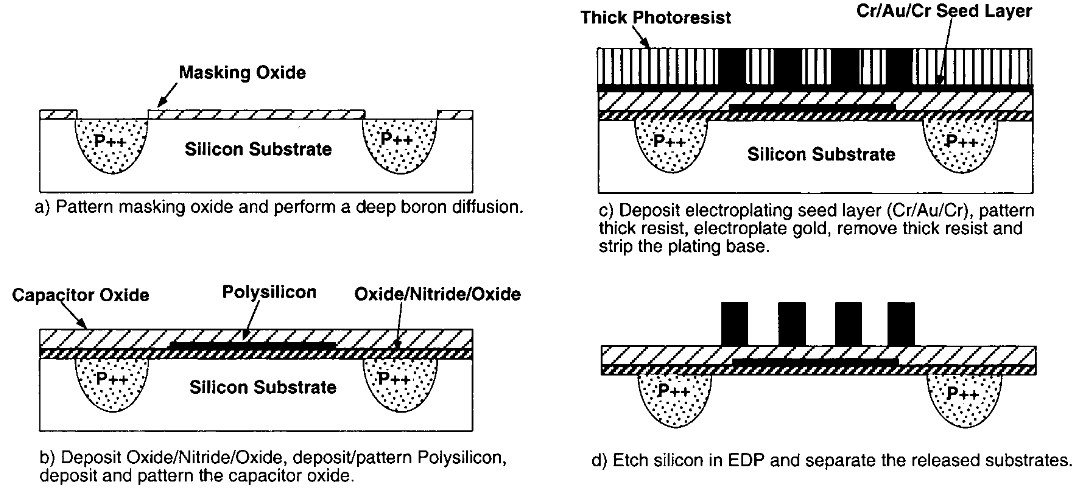

Figure 4. Cross section of the silicon platform fabrication sequence.

where ρ is the metal resistivity, μ is the permeability, ω is the angular frequency, l is the length, w is the line width, h is the metal thickness, and δ is the metal skin depth. The fringing capacitor between the electroplated turns determines the resonant frequency and can be calculated by using equation (4) (this is the capacitance per unit length) [16]. In this equation, h is the metal thickness, w is the line width, d is the center-to-center distance of adjacent lines, and ε_{reff} is the effective dielectric constant ($\varepsilon_{reff} \sim 1$ for $d/t \gg 1$ and $\varepsilon_{reff} = (1 + \varepsilon_r)/2$ for $d/t \sim 1$, where t is the dielectric thickness).

$$\frac{C_o}{l} = \frac{27.8\varepsilon_{reff}}{\ln\left(\frac{\pi(d-w)}{w+h} + 1\right)} \text{ (pF m}^{-1}\text{)}. \tag{4}$$

The thin-film capacitor is modeled by C representing the low frequency capacitance, R_s modeling the effective series resistance, and C_{ox} representing the capacitance from the bottom electrode to the silicon substrate (see figure 2). The effect of C_{ox} is eliminated by removing the substrate. The effective series resistance represents a combination of the dielectric loss, and the resistance in the capacitor electrodes and leads. The driving point impedance (Z) and dissipation factor (D) of the capacitor can be written as:

$$Z = \frac{\tan\delta}{\omega C} + R_s - \frac{j}{\omega C} \tag{5}$$

$$D = \omega R_s C \tag{6}$$

where $\tan\delta$ is the dielectric loss and R_s is the equivalent electrode and lead resistance. The dielectric loss is the dominant loss mechanism at low frequencies, whereas at high frequencies the lead and electrode resistances dominate. In many RF applications the equivalent series resistance has to be rather low (e.g. $<1\ \Omega$). This can be achieved by process modification (i.e. using low sheet resistance metals) and/or layout techniques (multiple capacitors in parallel or minimum resistance patterns) [17]. This is particularly an important consideration if polysilicon is used as the bottom electrode material.

4. Fabrication process

Figure 4 shows the fabrication sequence of the silicon platform. The process starts with a deep boron diffusion step (1175 °C for 7 h+1200 °C drive-in for 5 h) to form the support anchors (10 μm deep) for the substrate. This is followed by the deposition of a stress relieved LPCVD dielectric sandwich layer SiO_2 (4000 Å)/Si_3N_4 (2000 Å)/SiO_2 (4000 Å), which will form the membrane over which the integrated coil and transistor mounting pads are suspended. Next a polysilicon layer is deposited, doped (10–15 Ω/square), and patterned to define the resistor and the bottom plate of the capacitors. The capacitor dielectric LPCVD oxide (∼5000 Å) is then deposited and contacts are opened to the polysilicon layer. A Cr (400 Å)/Au (3000 Å)/Cr (200 Å) electroplating seed layer is then deposited followed by patterning a thick photoresist (PR4620, spin at 2500 rpm, 250 s exposure time, 8 min development, ∼9 μm thickness) mold layer. The coil and top capacitor plates are electroplated (55 °C plating bath, 2 mA cm^{-2} current density) and the seed layer is etched after removing the resist mold. Finally, the wafer is etched in ethylene diamine pyrocatechol (EDP) [18] and individual dies are separated. Depending on the application and design, the dies can be attached with epoxy to a glass back-plate for mechanical support and discrete RF components or integrated RF chips connected to the substrate with silver epoxy or the flip-chip bonding technique (the latter requires an additional solder paste placement step). The micromachined platform is rugged and its fabrication does not depend on the silicon crystal orientation for selective substrate removal. It can support active hybrid components while reducing the large capacitances associated with their bond pads by suspending them on dielectric membranes. Figure 5 shows a photograph of the fabricated substrate with on-chip-electroplated coil, thin-film capacitors, and polysilicon resistors. Figure 6 is an SEM of the cross section of a 6 μm electroplated coil, suspended on the dielectric membrane.

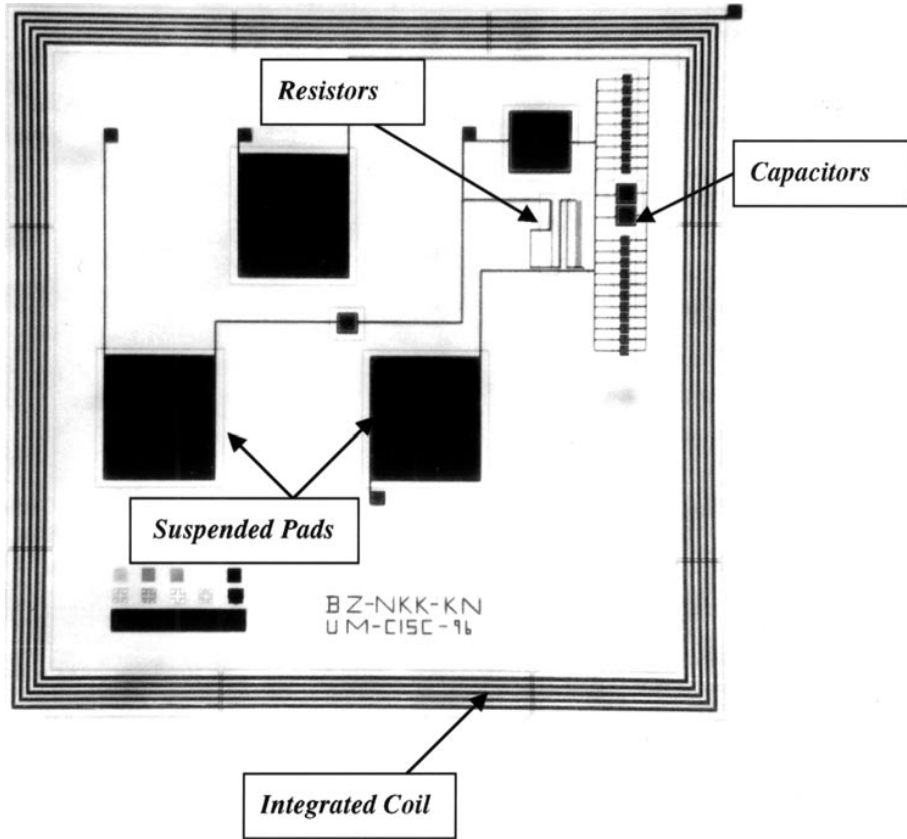

Figure 5. Photograph of a fabricated platform with an on-chip coil, thin-film capacitances and polysilicon resistors.

5. Test results

We have used this platform to design and implement a Colpitts oscillator. The oscillator is the transmitter part of a biotelemetry microsystem designed for long-term recording of a number of physiological parameters, figure 7. The recorded and digitized physiological data is used to amplitude modulate (on–off switching) the Colpitts transmitter. The transmitter is built by attaching a surface mount hybrid RF transistor on the silicon platform. An inductor with a high-quality factor reduces the power consumption and phase-noise in the Colpitts transmitter [19]. Equation (7) describes the oscillation condition (loop gain > 1):

$$g_m Q^2 r_s \frac{C_1}{C_1 + C_2} \geqslant 1 \tag{7}$$

where g_m (I_c/V_T) is the transconductance, Q is the quality factor of the coil, r_s is the series resistance of the coil, and $C_1/C_1 + C_2$ is the capacitance feedback ratio. As can be seen, a high Q allows a reduction in the quiescent current of the transistor. In order to design the transmitter, one starts with the desired current consumption and designs the coil (dimension, number of turns, conductor width spacing and thickness) in order to achieve the required Q and satisfy the oscillation condition. Capacitors C_1 and C_2 are next chosen to set the transmission frequency. Many iterations might be necessary to optimize the design. Capacitor C_1 is trimmable to allow fine-tuning of the oscillation frequency. Emitter resistance (R) along with the driving voltage set the power consumption. Figure 8 shows a SEM of a transmitter chip with electroplated coil and surface mount RF transistor.

Following the platform fabrication, important parameters for various passive components were measured using an RF impedance analyzer (HP4195A). Equivalent series resistance for a typical thin-film polysilicon–metal capacitor was measured to be $\sim$3 Ω at 300 MHz. Multiple capacitors connected in parallel were used in the actual transmitter circuitry to reduce the series resistance to below 1 Ω. A five-turn inductor with 25 μm linewidth and separation, 5 μm metal thickness, and 2.5 mm outer radius was designed for the transmitter coil. The inductance and the quality factor for the coil were measured at 300 MHz before and after the substrate removal. The measured inductance was 350 nH in both cases, which was within 5% of the designed value (370 nH using equation (1)). However, the quality factor showed a dramatic increase from 3 to 18 after the substrate removal. This clearly demonstrates the effectiveness of removing the substrate in reducing the eddy current losses and increasing the quality factor. Table 1 summarizes the measurement results for an integrated coil and capacitor suspended on a dielectric membrane.

Following the characterization of passive components, a surface mount RF transistor (Motorola MMBR931LT1) was mounted on the substrate using silver epoxy and the transmitter was operated with a 3 V battery. Figure 9 shows the output spectrum of a transmitter being switched at 1 Mbps. As can be seen, the oscillation frequency is at $\sim$315 MHz and

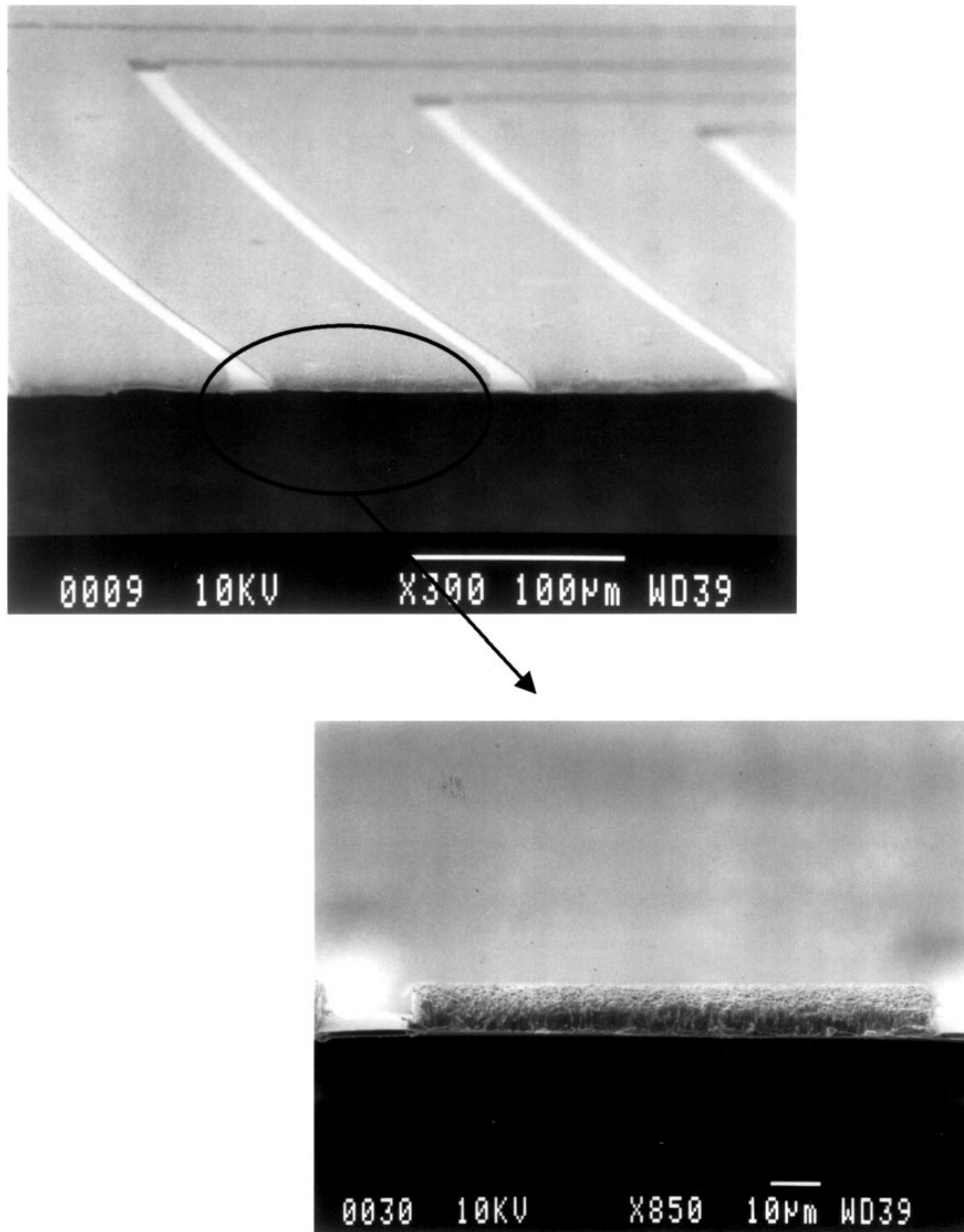

Figure 6. SEM of the cross section of a 6 μm electroplated coil suspended on the dielectric membrane.

Table 1. The measurement results for an integrated coil and capacitor suspended on a dielectric membrane.

Component	Measured value at 300 MHz
Coil	
L_o	350 nH
R_S (AC)	36 Ω
Q (at 300 MHz)	18
f_{rs}	>500 MHz
Capacitors	
C/area	6.9×10^{-9} F cm^{-2}
Equivalent series resistance	3 Ω
Dissipation factor	0.015

the spectrum is spread according to the incoming pulse rate and duty cycle. The transmitter consumes ~100 μA and has a transmission range of ~3 ft. The power consumption in the pulsed mode of operation is determined by the emitter resistance and the driver pulse amplitude and duty cycle (one can reduce the current drain either by lowering the pulse amplitude, ~60 μA if the pulse amplitude is 2 V, or using a lower duty cycle pulse stream). Table 2 summarizes important characteristics and test results of the Colpitts transmitter.

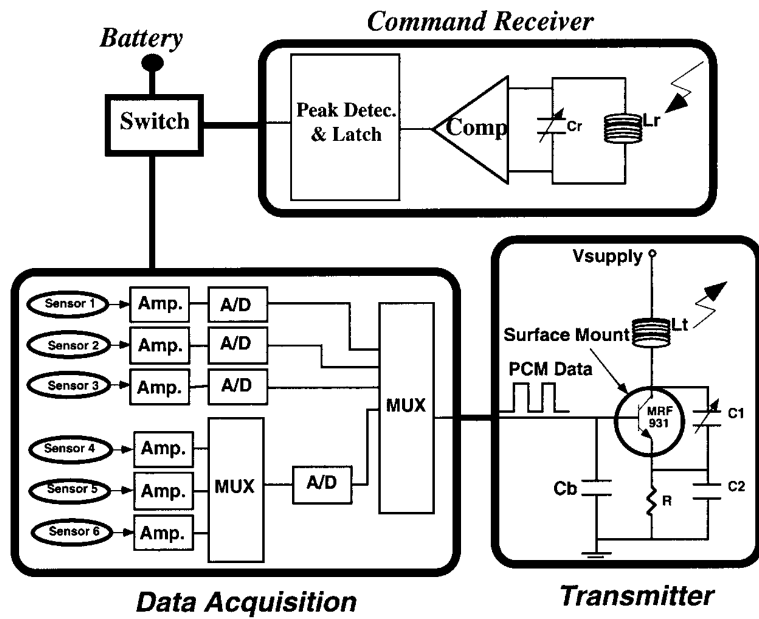

Figure 7. Biotelemetry microsystem with Colpitts transmitter for measuring multiple physiological parameters.

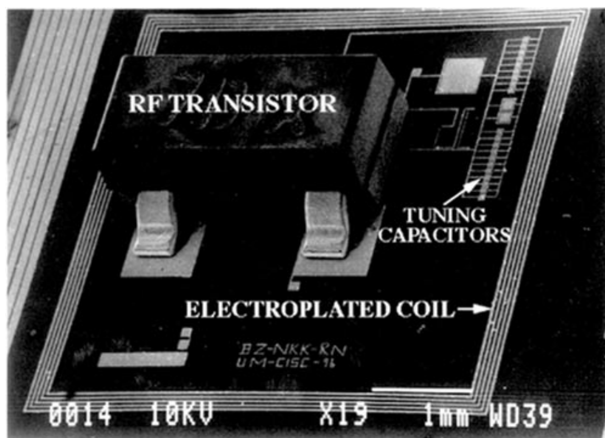

Figure 8. SEM of a transmitter platform with a surface mount RF transistor.

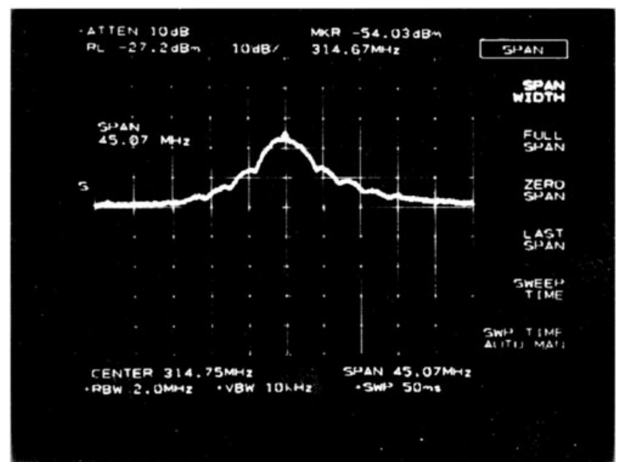

Figure 9. The output spectrum of a transmitter operating at ~315 MHz and being modulated at 1 Mbps.

Table 2. Important characteristics and test results of the Colpitts transmitter.

Area	5×5 mm^2
Power consumption	200 μA continuous/100 μA at 1 Mbps data rate
Range	~3 ft
Operating frequency	275–375 MHz
Modulation rate	up to 1 Mbps

6. Conclusion

We have developed a generic micromachined silicon platform for high-performance RF passive components. This platform is fabricated by the dissolved wafer process and supports: (1) high self-resonant frequency and quality factor inductors suspended on a dielectric membrane, (2) low-loss thin-film capacitors, and (3) polysilicon resistors. By suspending an electroplated coil on a dielectric membrane, we were able to increase the self-resonance frequency and the quality factor of the inductor without using multilevel metallization and front-side selective substrate removal which adds to the process complexity. This technique allows full optimization of various passive components without the need for any modifications to the foundry available CMOS or BiCMOS circuitries. This platform can be used to build miniature, lightweight, high-performance (low-power and low-noise) transceivers or other RF subsystems using hybrid-attached surface-mount or flip-chip bonded RF circuits.

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References

[1] Gray P R and Meyer R G 1995 Future directions in silicon IC's for RF personal communications *Proc. Custom Integrated Circuits Conf.* pp 83–9

[2] Mason A, Yazdi N, Chavan A V, Najafi K and Wise K D 1998 A generic multielement microsystem for portable wireless applications *Proc. IEEE* **86** 1733–46

[3] Luy J F *et al* 1995 Si/SiGe MMIC's *IEEE Trans. Microwave Theory Techniques* **43** 705–14

[4] Voinigescu S P, Tarasewiscz S W, MacElwee T and Ilowski J 1995 An assessment of the state-of-the-art 0.5 μm bulk CMOS technology for RF applications *Proc. IEDM* pp 721–4

[5] Harame D L *et al* 1994 A 200 mm SiGe-HBT technology for wireless and mixed-signal applications *Proc. IEDM* pp 437–40

[6] Warner R M 1965 *Integrated Circuits: Design Principles and Fabrication* (New York: McGraw-Hill)

[7] Chang J Y C, Abidi A A and Gaitan M 1993 Large suspended inductors on silicon and their use in a 2-μm CMOS RF amplifier *IEEE Electron Device Lett.* **14** 246–8

[8] Case M 1997 SiGe MMICs and flip-chip MICs for low cost microwave systems *Microwave J.* **40** 264–76

[9] Burghartz J N *et al* 1995 High-Q inductors in standard silicon interconnect technology and its application to an integrated RF power amplifier *Proc. IEDM* pp 1015–17

[10] Ashby K B *et al* 1996 High Q inductors for wireless applications in a complementary silicon bipolar process *IEEE J. Solid-State Circuits* **31** 4–9

[11] Watanabe Y *et al* 1995 A new fabrication process of a planar coil using photosensitive polyimide and electroplating *Proc. Transducers '95* pp 268–71

[12] Long J R and Copeland M A 1996 The modeling, characterization, and design of monolithic inductors for silicon RF IC's *IEEE J. Solid-State Circuits* **32** 357–69

[13] Wheeler H A 1928 Simple inductance formulas for radio coils *IRE Proc.* p 1398

[14] Lee T H 1998 *The Design of CMOS Radio-Frequency Integrated Circuits* (Cambridge: Cambridge University Press)

[15] Yue C P, Ryu C, Lee T H and Wong S S 1996 A physical model for planar spiral inductors on silicon *Proc. IEDM* pp 155–8

[16] Walker C S 1990 *Capacitance, Inductance and Crosstalk Analysis* (Boston: Artech House)

[17] Glaser A B and Subak-Sharpe G E 1977 *Integrated Circuit Engineering* (Reading, MA: Addison-Wesley)

[18] Raley N F, Ugiyama Y and Van Duzer T 1984 (100) Silicon etch rate dependence on boron concentration in ehtylenediamine–pyrocatechol–water solution *J. Electrochem. Soc.* **131** 161

[19] Rhea R W 1997 *Oscillator Design and Computer Simulation* (New York: McGraw-Hill)