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A geometric etch-stop technology for bulk micromachining

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Abstract

This paper describes a new fabrication method for the simultaneous creation of multi-level single-crystalline silicon structures, each with a different thickness. The method combines deep dry etching and wet anisotropic etching of silicon in order to avoid multiple back-side alignment steps and timed etches. The levels are defined in a single lithographic step from the front side. The fabrication involves etching of deep trenches from the front side of the wafer followed by a refill and etch back process. The final structure is defined by maskless wet etching of the bulk silicon. The progress of the anisotropic wet etch is impeded by the geometric pattern at the bottom of the trenches, and thus structures with various thickness ranging from ten to a few hundred micrometres can be implemented. The effect of various design parameters, such as trench geometry, refill material and reactive ion etching lag, are discussed and design rules are established. The capabilities of the method are demonstrated by the fabrication of a number of devices, such as $1200 \times 1200 \times 3.5$ μm diaphragms supported by a 40 μm thick rim and ($1800 \times 10 \times 3$ μm) embedded hot-wire anemometers suspended by a 0.2 μm thick dielectric bridge.

1. Introduction

A number of bulk micromachining techniques have been demonstrated for the simultaneous fabrication of thin layers and thick supporting regions on silicon wafer. Typically the formation of the thick regions is accomplished by anisotropic wet etching of silicon [1, 2] or controlled deep dry etching. The first method limits the geometry to the exposed crystalline planes, after the etching, and predefined angles. Also, the final etched thickness is a function of the thickness of the starting wafer and is thus limited. As the industry standard moves towards 8 inch wafers and beyond, processing wafers with thicknesses less than 300 μm becomes exceedingly difficult. The second method, using deep dry etching from the back side, calls for multiple back-side alignment, deposition and lithography (the number depends on the number of layers and thickness needed in the final structure), and close control of the etch rate and timing, which can complicate the process significantly.

In this paper, we present a simple method involving only a single masking step for defining multi-level structures. In this method, the thin regions ($\sim$3 μm) are defined by a short diffusion step and the thick structures are defined by lithography from the front side of the wafer, eliminating the need for back-side alignment. Also, the final thickness of the structure ($<$500 μm) can be defined by controlling the depth and the width, considering the reactive ion etching (RIE) lag effect, of the trenches etched from the front side. Thus, the fabricated structure thickness is independent of the initial wafer thickness. In many applications, the microelectromechanical system (MEMS) is integrated with circuitry. This method allows for the formation of single-crystalline silicon islands on the structure, which facilitate integration, and the simultaneous fabrication of the MEMS and supporting circuit.

In the next section, we outline the fabrication process and introduce some of the parameters affecting the results. In section 3, we discuss design parameters and the rules established for this fabrication method. In section 4, we present some of the structures fabricated by using the method, and concluding remarks follow in section 5.

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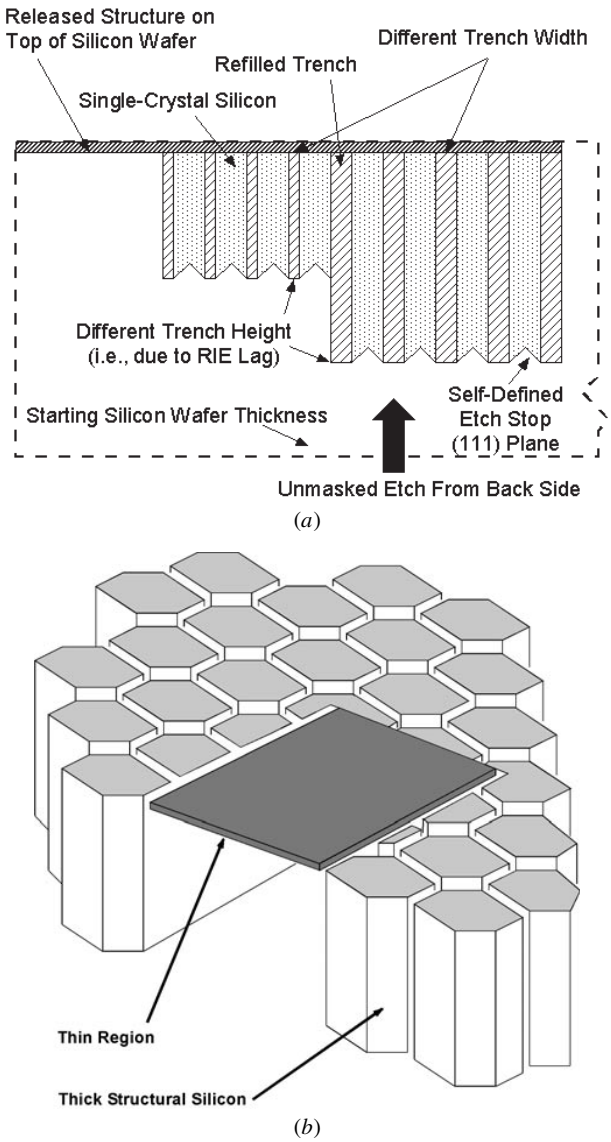


Figure 1. (*a*) Cross-sectional and (*b*) three-dimensional views of the trench-assisted etch stop technique.

2. Fabrication process

Cross-sectional and three-dimensional (3D) views of the proposed technique are shown in figure 1. Deep and narrow trenches are etched in the front side of a silicon wafer, and then refilled with thin films, such as polysilicon or silicon dioxide [3]. The thin microstructures are formed in the area surrounded by the trench pattern, either with diffusion or ion implantation. The doping is done in order to create a p^{++} profile and thus stopping the final anisotropic etch from attacking the thin region. The trenches are capped using an oxide film and then the silicon wafer is etched in a wet anisotropic etchant, such as ethylenediamine pyrocatechol (EDP), which removes all of the silicon under the microstructure and under the trenches, until it reaches the bottom plane of the trench region. The etch proceeds inside the silicon areas bounded by trenches and eventually stops when an inverted pyramid is formed by the (111) planes of silicon as shown. Note that the height of the pyramid depends on trench spacing, which

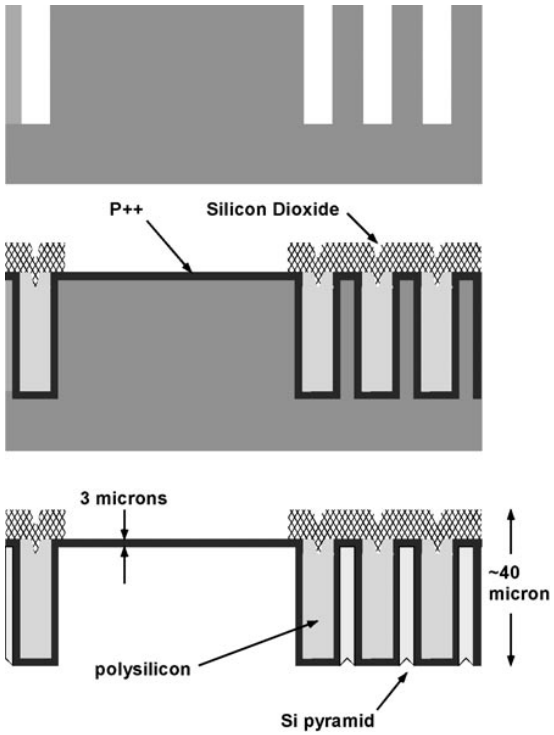
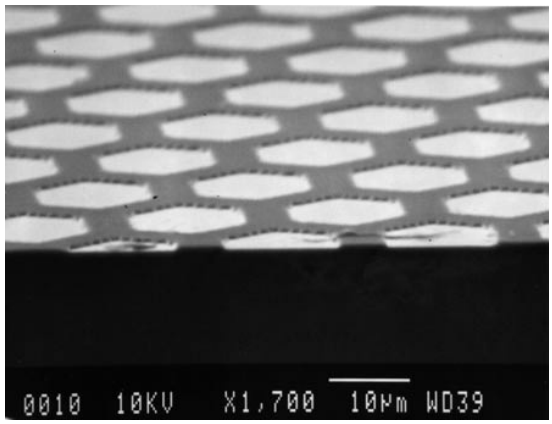


Figure 2. Simplified process flow.

can be controlled by the layout. As mentioned before, there is no need for double-sided processing, the thickness of the remaining silicon is independent of the starting silicon wafer thickness, and different trench heights can be created in a single etch by taking advantage of the RIE lag effect.

The fabrication process is shown in figure 2. Firstly, deep trenches are etched in a blank (100) silicon wafer using a photoresist mask and a time-multiplexed deep etcher [4]. The trench lateral mask pattern includes a unit cell which is repeated and covers the entire surface. The unit cell could be a triangle, a square, a hexagon or any other shape that could cover a surface by repetition. The trench pattern consists of lines with specific widths surrounding the unit cell island and providing an opening for deep RIE etching. The etch depth can vary from a few micrometres to a few hundred micrometres, depending on the aspect ratio achievable by the etching system. Then a boron diffusion step is performed. This step defines the thin regions in the structure, such as diaphragms. The heavily boron-doped region will not be attacked in the subsequent EDP etch [5] and thus the thickness of the region can be controlled by the adjustment of diffusion conditions. After boron diffusion, the trenches are refilled. Polysilicon is used as the main refill material because of its conformal deposition, although it is possible to use other materials, such as tetraethoxysilane (TEOS) silicon dioxide [6] or doped glass [7]. The surface polysilicon layer is etched back through a maskless blanket RIE etch. This step is carried out to help isolate the polysilicon in trenches after capping. If the polysilicon is exposed along the edges of the structure or the dicing lines, the entire layer will be attacked in the subsequent wet etch step and the structural integrity of the device will be lost. The last deposition step is for the capping silicon dioxide layer which seals the trenches. The devices are subsequently etched in EDP where most of the



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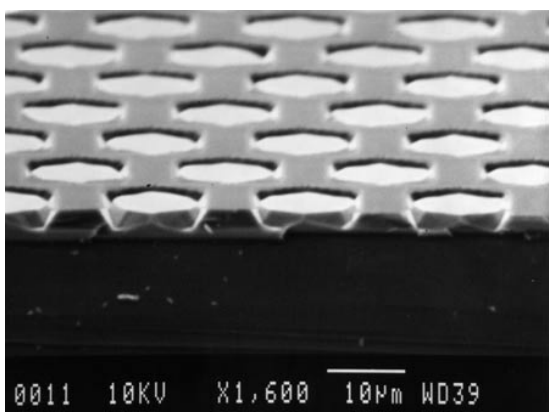

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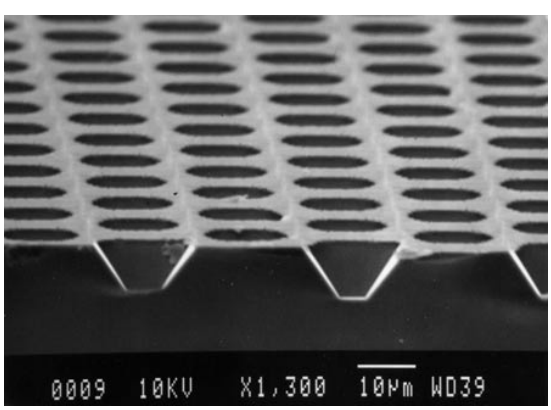


(*c*)

Figure 3. Pyramid formation in EDP etch solution. The hexagonal areas are exposed and the rest of the surface is protected by 0.2 μm of silicon nitride. The etch rate is $\sim$80 μm h^{-1}: (*a*) before etch; (*b*) after 5 min; (*c*) after 10 min.

undoped silicon is dissolved away. The etch starts from the back side and proceeds until the etch front meets the bottom of the trenches. At this point, etching continues along the $\langle 111 \rangle$ crystal planes inside the areas surrounded by the refilled trenches, and eventually the etching stops when the planes meet at the apex. This is the depth to which the etch proceeds inside the bounded regions and determines the final thickness of the structure. Note that by adding an extra masking step and proper front side protection, islands of undoped single-crystal silicon can be formed in the structure, which can be used to integrate circuitry with the MEMS device.

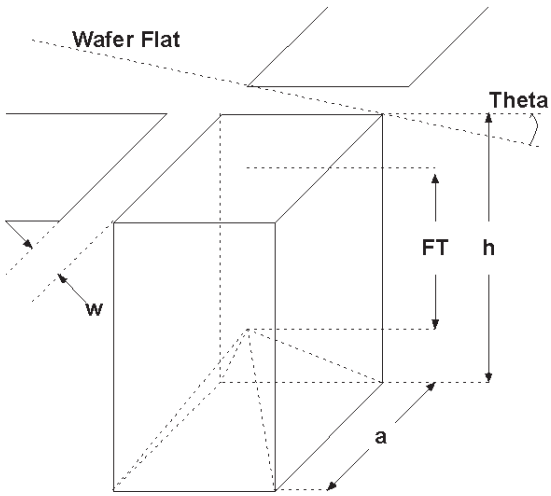


Figure 4. Parameter definition. Note that the unit cell here is a square: a, unit cell chord length; w, trench width; h, trench depth; FT, final thickness; θ, misalignment angle between the unit cell chord and the wafer flat on a (100) silicon wafer.

In order to study the formation of the inverted pyramids a front side etch was performed. This simulated etching from the back side at the bottom of the trenches. Then, 0.2 μm of silicon nitride was deposited and patterned with a hexagonal pattern (chord = 8 μm) resembling the pattern seen by the etch front at the bottom of the trenches. Figure 3 shows how the EDP etch proceeds inside the openings with time, after 0, 5 and 10 min.

3. Design issues

A number of process and layout parameters can be modified to control the final outcome of the fabrication. In this section we briefly describe some of the important issues for a successful design. Figure 4 introduces the parameters used in the section.

3.1. Final structure thickness

As mentioned earlier, the final thickness (FT) of the structure in the supporting area is a function of the trench depth and mask geometry, and is independent of the initial wafer thickness. The trench depth is, in turn, determined by the trench width and the aspect ratio achievable by the deep dry etching process. Table 1 summarizes the final thickness of the structure as a function of this depth and the unit cell island shape. Note that in table 1, the final thickness depicts the distance between the apex of the inverted pyramid in the unit cell island and the wafer surface.

3.2. Lateral mask pattern

The lateral mask pattern provides the most freedom for the designer to change the geometry. Assuming a simple line shape for trenches, only three shapes can be used for the unit cell since these should be able to cover the wafer surface by simple repetition. These shapes are triangle, square and hexagon. Figure 1(*b*) shows a 3D view of a sample structure made with hexagonal unit cells. Since the EDP etch is very sensitive to crystal orientation, any initial misalignment to the $\langle 100 \rangle$ planes could result in an error in the final thickness of

Table 1. Summary of unit cell shapes and design parameters.

Unit cell shape	Chord-⟨100⟩ plane angle	Final thickness	Maximum misalignment angle	Minimum refill thickness	Figure of merit
Triangle	0°	$h - \frac{a}{4}\left[\sqrt{3}\cos\theta + \sin\theta\right]\tan(54.7)$	15°	$\frac{w}{\sqrt{3}}$	130.05°
Square	0°	$h - \frac{a}{2}\left[\sin\theta + \cos\theta\right]\tan(54.7)$	45°	$\frac{w}{\sqrt{2}}$	108.45°
Tilted square (45°)	45°	$h - \frac{a}{\sqrt{2}}\cos\theta\tan(54.7)$	45°	$\frac{w}{\sqrt{2}}$	153.63°
Hexagon	0°	$h - a\cos(30-\theta)\tan(54.7)$	15°	$\frac{2w}{3}$	440.25°

h, trench depth; a, unit cell chord length; w, trench width; θ, misalignment angle.

the structure. Table 1 also shows the final thicknesses as a function of the initial misalignment angle θ. To remedy this problem, a short EDP etch can be performed prior to the trench lithography step to mark the proper crystal planes. The marks can be used to align subsequent layers; however, this results in further complexity of the process and may introduce ion contamination. A better way to circumvent the problem is to design the mask pattern (i.e. the shape of the unit cell) for minimal sensitivity to misalignment. We define a figure of merit for each of the possible unit cell shapes as

$$f = \frac{h_0 \times \theta_{\text{ext}}}{|h_{\text{ext}} - h_0|} \tag{1}$$

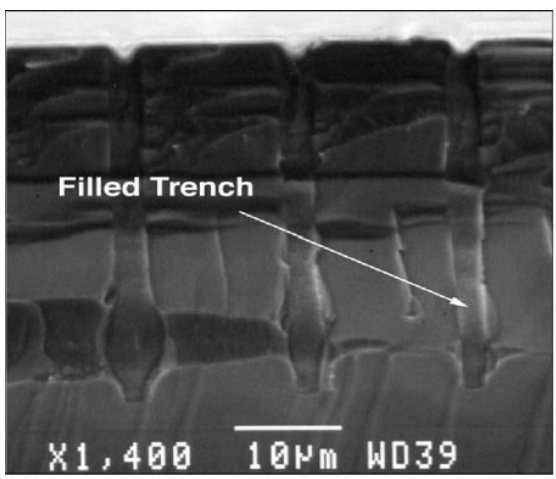
where h_0 is the inverted pyramid height with no misalignment, θ_{ext} is the misalignment angle at which the maximum change in FT occurs and h_{ext} is the pyramid height at this angle. It can be shown that a hexagonal unit cell provides the least sensitivity to misalignment and thus is recommended for pattern design. Non-idealities in lithography, and also loss of critical dimensions during the deep RIE etch, should be taken into account in order to ensure the complete refilling of the trenches.

3.3. Trench refill

Conformal deposition is a basic requirement for the thin film used in trench refill. Void formation [8, 9] can result in loss of structural integrity and attack by the etchant. If polysilicon is used as the fill material, it should be sealed from the etchant. The total thickness of the refill film inside the trenches should exceed the width. It should be noted that, at the intersection of the trenches, the maximum distance between the opposite sides of the trench is more than half of the trench width and thus a thicker film is required. Table 1 shows the minimum thickness required for the complete refill of the trenches, as a function of trench width and unit cell shape. In the sample devices fabricated here, a diffusion process prior to trench refill added to the protection of the refill polysilicon. If silicon dioxide only is used for this purpose, special care should be taken in order to avoid cracking of the film at the bottom of the trenches. The micro-cracks can provide an access route for the wet etchant to attack the refill material and thus disintegrate the device.

3.4. RIE lag effect

In order to simultaneously fabricate structures with different thicknesses, the RIE lag effect can be used, as illustrated in figure 1. The etch rate of silicon inside the trenches depends on the trench width during the deep dry etch step [10–12]. This



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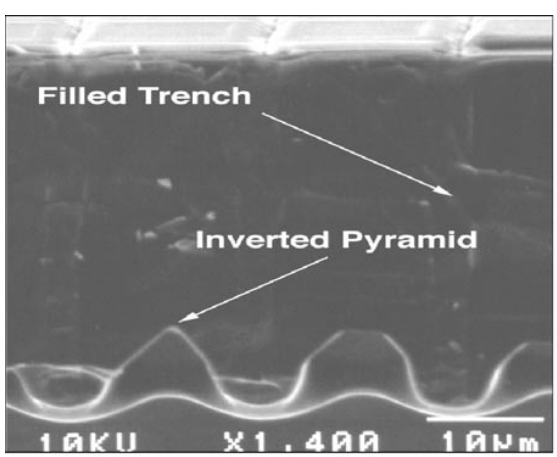

(*b*)

Figure 5. SEM pictures of the refilled trenches (*a*) prior to EDP etching and (*b*) after the formation of the inverted pyramids and completion of the etch. Note that the unit cells are squares in this experiment.

is usually an undesired effect; however, it can be utilized here to fabricate versatile structures. Although at the intersection of trenches this effect produces unwanted non-uniformity, by varying the trench width across the pattern, height variations of the order of ∼10% or more are achievable. The trench width variation is limited by the maximum refill material thickness deposition. According to table 1, the triangular unit cell design allows for the widest trenches and the square unit cell has the narrowest trench, considering that the maximum refill material thickness is the same for both cases. If the lateral unit cell

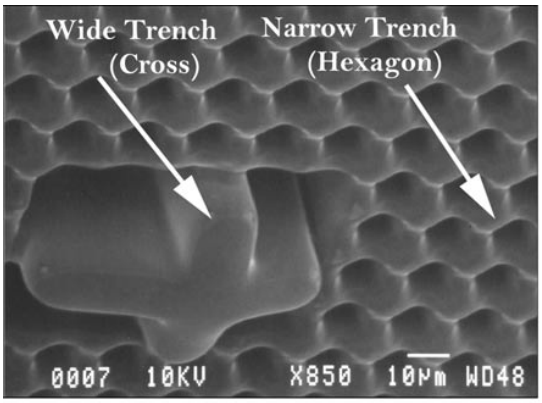

Figure 6. The effect of RIE lag on trench depth and thickness of the structure. The cross is made of wider trenches compared to the ones in the hexagonal area (width ratio of 5/2). The wide trenches are more than 10% deeper than the narrower ones (40 μm).

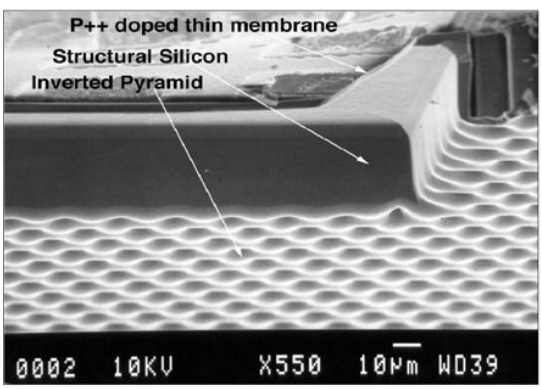

Figure 7. Simultaneous formation of a 3.5 μm thick diaphragm and 40 μm thick supporting structure [13]. Part of the diaphragm is removed to show the cross section.

design is changed from square to rectangular on the same mask, a wider thickness range can be achieved by using the RIE lag effect.

4. Fabricated devices and structures

A number of devices and test structures have been fabricated to demonstrate the merits of the new fabrication method. Both square and hexagonal patterns were tried and the most promising results were achieved by using the latter. Figure 5 shows scanning electron microscopy (SEM) pictures of the refilled trenches prior to and after completion of the EDP etch. It verifies the conformal deposition of polysilicon and the successful prevention of void formation for most trenches. The trenches are 40 μm deep, filled with 2 μm of polysilicon. In figure 5(*b*), it can be seen that the inverted pyramids are formed at the bottom of the trenches and the progress of the etch front has been instantaneously impeded by intersecting the $\langle 111 \rangle$ crystal planes. The same process can be used to easily fabricate deeper trenches. Figure 6 shows the effect of RIE lag on the trench depth and structure thickness. Variations of up to 10% can be expected by controlling the lag effect due to changes in trench width.

The fabrication method has been successfully used in the making of a number of devices. Figure 7 shows the simultaneous formation of a thin region (diaphragm) and a thick structural supporting rim. A drawing of this structure is provided in figure 1(*b*). This was done as a part of the fabrication process for a Helmholtz resonator, which has been described in detail elsewhere [13]. The membrane is 3.5 μm thick and the supporting structure is 40 μm. Figure 8 shows an in-plane integrated hot-wire anemometer. The conductive part is made by heavy boron diffusion (3 μm) and is suspended by an extension of the capping silicon dioxide (0.2 μm) from the thick (40 μm) supporting structure with a hexagonal trench pattern. This suspension structure reduces the thermal conductance between the sensor and the supporting structure and improves the sensitivity of the device. Figure 9 shows a drawing of the cross-sectional view of this device.

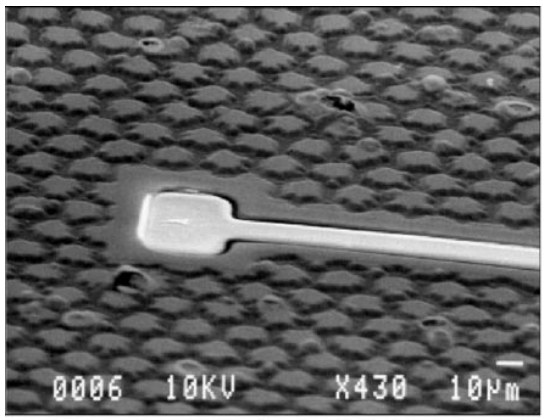

Figure 8. An in-plane integrated suspended hot-wire anemometer flow sensor. The supporting structure is made of a hexagonal pattern with ($a = 8$ μm).

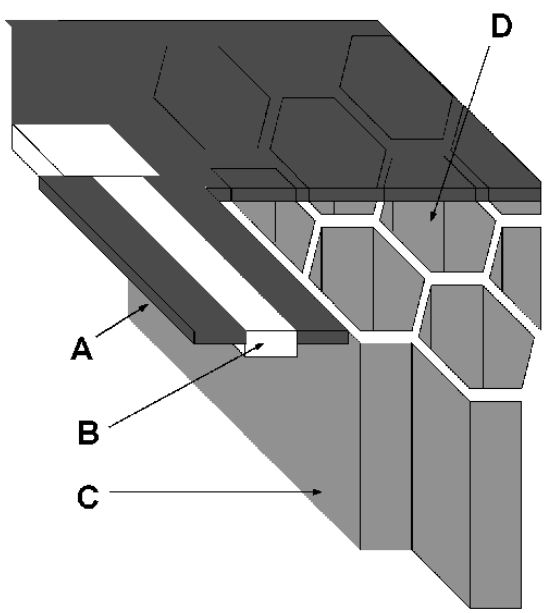

Figure 9. Cross-sectional view of the suspended hot-wire anemometer and the supporting structure: A, suspension extension made of the capping dielectric for trenches; B, p^{++} Si hot-wire anemometer; C, supporting thick silicon structure; D, the capping dielectric partially removed to show the hexagonal trench pattern more clearly.

5. Conclusions

A new fabrication technology is introduced for the fabrication of multi-level bulk silicon structures. By combining dry and wet anisotropic etching, the need for multiple and back-side lithographic steps is eliminated. The thickness of the final structure is determined by a number of design factors, such as lateral trench pattern and size, initial misalignment to the crystalline planes, refill process and RIE lag. Design rules are established and it has been determined that the height variation is limited and is of the order of 10%. A number of test structures and devices including a Helmholtz resonator and an integrated hot-wire anemometer were successfully fabricated using the proposed technology.

Acknowledgments

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