

Self-consistent analysis of lattice-matched and pseudomorphic quantum-well emission transistors

Kyushik Hong and Dimitris Pavlidis

Center for Space Terahertz Technology, Solid State Electronics Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, Michigan 48109-2122

(Received 13 August 1990; accepted for publication 1 November 1990)

A self-consistent analysis of the quantum-well emission transistor (QWET) is presented allowing an exact calculation of the device quantum properties. Poisson's and Schrödinger's equation are solved numerically using a finite-difference method on a self-consistent basis. Pseudomorphic AlGaAs/InGaAs designs with 15%–20% excess In are suggested for improving the device performance. Design with doping in various parts of the QWET are also studied. This analysis reveals that the device performance is less optimistic than previously predicted by analytic approaches. By introducing the pseudomorphic channel principle, while maintaining a reasonably low Al content for the gate and collector layers, it is, however, possible to obtain satisfactory performance. Optimum pseudomorphic designs showed high current driving capability (2×10^5 A/cm²), high transconductance (3S/mm) and small intrinsic delay time (2 ps).

I. INTRODUCTION

The principle of quantum-well emission transistor (QWET) has been discussed elsewhere.¹⁻³ Its schematic cross section and band diagram are shown in Fig. 1. By appropriate biasing of the gate (G) the quasi-Fermi level and the energy states of a small band-gap material (quantum well, QW) are positioned in a way that the energy barrier ϕ_2 [see Fig. 1 (b)] between the QW and the collector is lowered. In the presence of a collector (C) bias, carrier transport and conduction takes place between the QW and the collector. The mechanism for this is thermionic emission for single collector barrier^{1,2} or tunneling for double collector barrier³ (with a thin layer/high-energy barrier next to the QW followed by a thick layer/low energy barrier). Unlike other devices such as negative-resistance-field-effect transistor (NERFET)⁴ and charge-injection transistor (CHINT)⁵ where thermionic emission takes place after electrons are heated up with the help of an electric field parallel to the channel, the QWET employs a different principle. Here the barrier is controlled by a remote electrode (gate) via the quantum properties of a two-dimensional-electron-gas (2DEG) system. The features of this device include: (i) majority carrier operation, (ii) vertical rather than parallel to a heterointerface transport; this translates to smaller sensitivity to surface conditions and defects, (iii) isolation of the control electrode from the channel and thus high input impedance, (iv) high current and transconductance due to the exponential nature of the thermionic emission.

This paper presents an accurate theoretical approach for analyzing the QWET properties. Pseudomorphic, as well as lattice-matched QW designs are considered. Section II presents the theoretical approach used in this work and compares it to previous analysis. Results of the device performance using different designs are presented in Sec. III.

II. THEORETICAL APPROACH FOR DEVICE ANALYSIS

The QWET theory presented by Grinberg *et al.*² employs an analytical solution of Poisson's equation in the gate barrier and QW layer of the device with the wave function included in a form of quantum mechanical parameters. A variational method is then used to solve Schrödinger's equation with a potential energy expression obtained from Poisson's equation. A trial wave function $\chi(z) = Az(L - z) \exp(-az/2)$, justified for triangular quantum well was

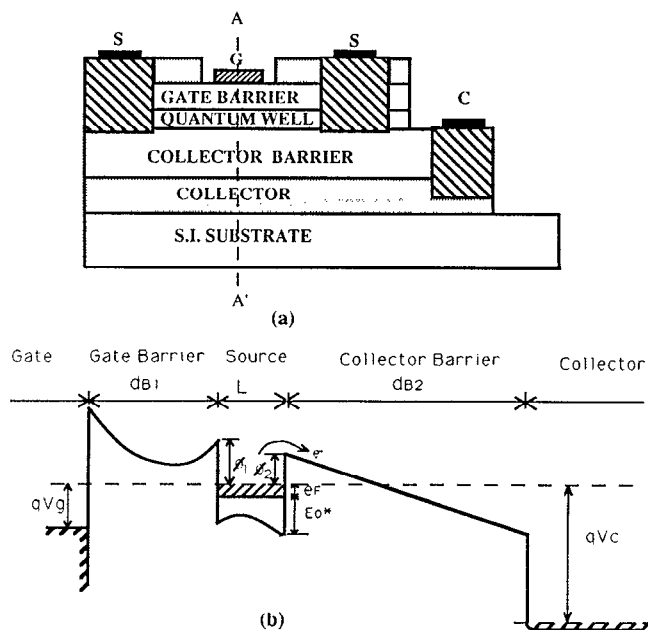


FIG. 1. (a) Cross-section and (b) conduction-band diagram along the $A-A'$ reference plane of the quantum-well emission transistor.

used; A is the normalization coefficient, L is the length of QW (Fig. 1), and α the variational parameter. Numerical analysis was used to find the value of α giving minimum energy and being consistent with Poisson's equation through a monitoring parameter. Some of the assumptions used in the above analysis are: (i) the layers above the QW are always depleted for the sake of an analytical expression for Poisson's equation, (ii) the quasirectangular shaped QW is represented by a triangular-type trial function, (iii) all energy states above the ground state are neglected, (iv) Schrödinger's equation is solved only in the QW, (v) a sheet-carrier density (n_s) is first assumed and then the gate bias (V_{gs}) is calculated rather than considering arbitrary gate (V_{gs}) and collector bias (V_{cs}) values.

The numerical approach used in this paper overcomes some of the limitations introduced by the assumptions of previous theories. The approach is based on the theory developed by the authors for lattice-matched and strained high-electron-mobility transistors (HEMTs)⁶ and its features regarding the QW analysis are listed below:

(1) Poisson's equation and Schrödinger's equation are solved numerically (one-dimensional finite-difference method) on a self-consistent basis.

(2) No depletion approximations are made for the layers above the QW; Poisson's equation is self-consistently solved between potential and electron distribution through a Fermi-Dirac distribution function.

(3) The Schrödinger's equation is solved in the gate barrier as well as the QW.

(4) Five subbands are considered.

(5) External parameters V_{gs} and V_{cs} are used as input parameters for device simulation.

(6) The effect of strain in the QW is taken into account. To solve Poisson's equation self-consistently, a piecewise linear quasi-Fermi level is assumed. In the gate barrier and QW, the quasi-Fermi level is kept constant provided that the strong electron-electron interaction maintains the two regions in equilibrium state. In the degenerate collector region, the quasi-Fermi level is also assumed constant and separated from that of the grounded quantum well by an amount corresponding to the applied collector voltage. Between the QW and the collector, i.e., in the collector barrier, it is assumed that the quasi-Fermi level varies linearly and is continuous at the interfaces. After solving Poisson's and Schrödinger's equation self-consistently, one can obtain the values of quantum mechanical variables such as electron subband energies and electron wavefunctions from which the sheet-charge density $n_s(I)$ and the effective barrier height $\phi_2(I)$ can be calculated at I th gate bias.

Given the barrier height, the thermionic current density at the particular bias point can be found from:

$$j_c(I) = A_0 \frac{m^*}{m_0} T^2 \exp[-\phi_2(I)/kT], \quad (1)$$

where A_0 is the Richardson constant ($120 \text{ A/cm}^2/\text{K}^2$), m^*/m_0 is the ratio of effective mass to free electron mass, k is a Boltzmann constant, and T is the electron temperature which is assumed the same as the lattice temperature (300 K). The QWET operation by tunneling can also be considered as a special case of the theory. The results presented here correspond, however, to designs where operation is based on thermionic emission.

The transconductance g_m can be calculated by

$$g_m(I) = \frac{\partial I_c}{\partial V_{gs}} \frac{1}{W} = \frac{L_g j_c(I)}{kT} \frac{[\epsilon_F(I) + E_0^*(I)] - [\epsilon_F(I-1) + E_0^*(I-1)]}{V_{gs}(I) - V_{gs}(I-1)} \quad (2)$$

where L_g is gate length, $\epsilon_F(I)$ is quasi-Fermi level with respect to first subband edge and $E_0^*(I)$ is the ground-state energy with respect to conduction band edge at the QW-collector barrier interface at I th gate bias.

The intrinsic time delay τ at I th gate bias is finally calculated by

$$\tau(I) = \frac{C_{gs}(I)L_g}{g'_m(I)} + \frac{d_{B2}}{v_s}, \quad (3)$$

where

$$C_{gs}(I) = \frac{q[n_s(I) - n_s(I-1)]}{V_{gs}(I) - V_{gs}(I-1)}. \quad (4)$$

g'_m in Eq. (3) is an external transconductance with nonzero source resistance R_s as defined by Grinberg *et al.*² In the expression of τ , the first term is interpreted as a channel charging time through the gate-source capacitance and source resistance, and the second term is the electron traveling time through the collector barrier of length d_{B2} . The saturation electron velocity v_s is assumed to be 10^7 cm/s .

III. DEVICE PERFORMANCE AND DESIGN COMPARISONS

The theoretical approach described in Sec. II was applied to QWET designs employing different material combinations. These include lattice-matched AlGaAs/GaAs/AlGaAs, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ and strained AlGaAs/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x = 0.15, 0.2$)/AlGaAs heterostructures for the gate barrier/quantum-well/collector barrier regions. The first two designs were also reported earlier.² The introduction of excess indium in the QW leads to a strained QWET design. This has certain attractive features related to its electrical performance and technology of fabrication. These are discussed later on in this section.

A comparison is made first between this theory and the results by Grinberg *et al.* The simulations were based on the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}/\text{GaAs}/\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ design. Doping is provided only in the top $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ layer (structure IV in Fig. 5).

The self-consistent results for the conduction-band pro-

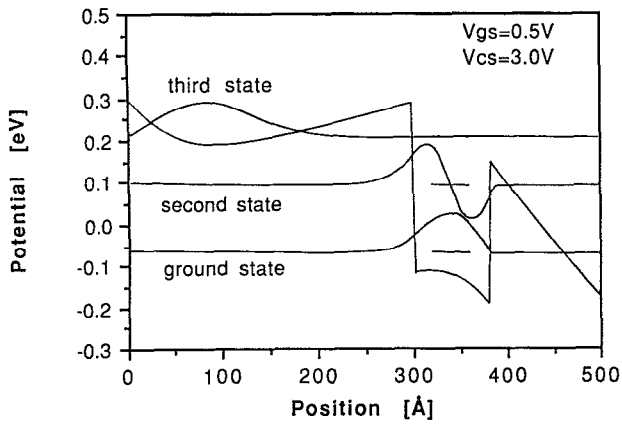


FIG. 2. Self-consistent calculation of the conduction-band profile, energy states and wave functions for $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}(300 \text{ \AA})/\text{GaAs}(80 \text{ \AA})/\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}(1000 \text{ \AA})$ QWET at $V_{gs} = 0.5 \text{ V}$ and $V_{cs} = 3 \text{ V}$.

file and first three subband energies and wave functions are shown in Fig. 2. The potential energy is measured with respect to the quasi-Fermi level in the gate barrier and the QW. The results show the exact solution for the QW potential shape without assuming triangular type trial function and include several subbands. No depletion approximations were made as explained earlier.

The results for the sheet carrier density n_s , energies E_0^* and $E_0^* + \epsilon_F$, collector current density (j_c) and transconductance (g_m) are given in Fig. 3 as a function of gate voltage V_{gs} . The theory presented in this paper predicts lower n_s under strong bias V_{gs} . An inverse tendency is found at low bias. The ground-state lowering $|\Delta E_0^*|$ predicted in this work is also smaller. Finally, the transit time estimated by our theory is longer. The discrepancies result from various reasons such as, the assumption of complete depletion of the doped layers and the neglect of charge built-up in the gate barrier layer. These assumptions give rise to an overestimation of carrier modulation in the QW. In particular the ground-state lowering $|\Delta E_0^*|$ is overestimated by previous theories, and so is the n_s modulation (which is equivalent to an overestimation of ϵ_F). The barrier height change $\Delta\phi_2$ is equal to $-(\Delta E_0^* + \Delta\epsilon_F)$, where $\Delta E_0^* < 0$, $\Delta\epsilon_F > 0$ and $|\Delta E_0^*| < |\Delta\epsilon_F|$. Both $|\Delta E_0^*|$ and $|\Delta\epsilon_F|$ are overestimated in the analytical approach with a net result of a smaller value (more negative) for the predicted $\Delta\phi_2$. Although the $|\Delta\phi_2|$ difference between the theories is small, it results to a very large difference in j_c and g_m (see Fig. 3) because of the exponential dependence of these parameters on $\Delta\phi_2$. Since g_m is lower in our theory, the transit time (τ) through the barrier [Eq. (3)] becomes larger and the true device performance of the material systems suggested earlier is less optimistic than initially thought. By way of example, the minimum τ of the $\text{AlGaAs}/\text{GaAs}$ ($L = 50 \text{ \AA}$) device is calculated around 40 ps instead of 3.5 ps as expected by previous work.²

Various heterostructure designs based on lattice-matched $\text{AlGaAs}/\text{GaAs}$, $\text{InAlAs}/\text{InGaAs}$ and pseudomorphic $\text{AlGaAs}/\text{InGaAs}$ systems are considered next in view of an optimization of QWET performance. For the gate bar-

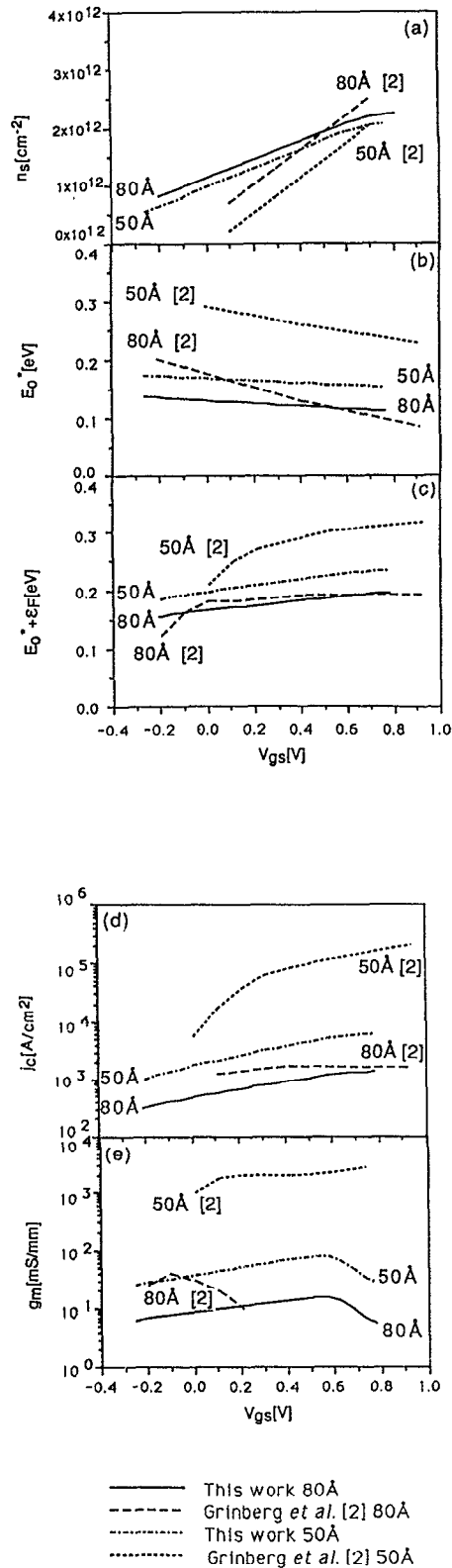


FIG. 3. Comparison of QWET ($\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}/\text{GaAs}/\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$) results with QW length of 50 and 80 Å as obtained by the self-consistent analysis (this work) and previous approaches² (see ref. 2): (a) Sheet carrier concentration, (b) ground-state energy E_0^* , (c) energy $E_0^* + \epsilon_F$, (d) collector current density j_c , and (e) transconductance g_m . Parameters are plotted as function of gate voltage V_{gs} .

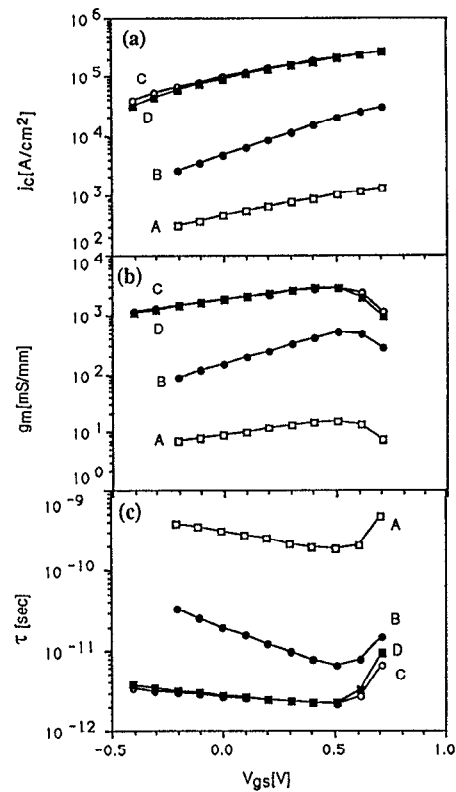
rier of the lattice-matched AlGaAs/GaAs, $\text{Al}_x\text{Ga}_{1-x}\text{As}$ with $x = 0.4$ allows a large conduction band offset between gate barrier and QW and reduces electron transfer from the QW. However, it is desirable to maintain the Al mole fraction below $x = 0.3$ in order to avoid problems arising by the presence of the DX-center. AlGaAs/InGaAs pseudomorphic designs have an advantage from this aspect because they offer larger conduction band offset than lattice-matched designs with the same Al mole fraction. For the collector barrier, the material chosen should present a small conduction band offset with respect to the QW in order to enhance the thermionic emission. For given QW thickness, the conduction band offset has to be chosen so that the ground-state energy of the QW is lower than the barrier energy ϕ_2 by at least an order of kT . This ensures that the current can be controlled by thermionic emission over the whole operation range ($< 0.8 \text{ V}$).

In view of these considerations device designs of different material compositions were studied. All structures had only a thin region of the gate barrier layer doped as suggested by Grinberg *et al.* (structure IV in Fig. 5) for optimum QWET design. The simulation results are discussed below.

Figure 4 shows the j_c , g_m , and τ dependence on gate bias for the various designs. The collector voltage was assumed in all cases to be fixed at $V_{c_s} = 3 \text{ V}$. The following designs were considered;

- A: $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}/\text{GaAs}/\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$,
- B: $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$,
- C: $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}/\text{In}_{0.15}\text{Ga}_{0.85}\text{As}/\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ and
- D: $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{Al}_{0.17}\text{Ga}_{0.83}\text{As}$

Designs A and B correspond to those proposed earlier^{1,2} and are lattice-matched QWET structures on GaAs and InP substrates, respectively. Designs C and D employ the pseudomorphic approach on GaAs. A technological advantage of the pseudomorphic design is the possibility of selective removal of the AlGaAs material over the InGaAs QW by reactive-ion-etching techniques. This allows to contact the thin QW region in a controlled fashion unlike the other designs. Furthermore, the high In content of the pseudomorphic QWET allows a reduction of the resistance along the QW. As discussed earlier² this permits a smaller potential drop along the QW and therefore a smaller transconductance degradation and, in turn smaller intrinsic delay time can be achieved. The pseudomorphic QW also allows a reasonable electron barrier from the QW to the gate barrier while maintaining the Al mole fraction in the AlGaAs layer low. An estimation of the effective thermionic emission barrier from the QW to the gate barrier (ϕ_1) reveals the following values for the structures; 0.36 eV for A, 0.30 eV for B, 0.34 eV for C and 0.29 eV for D at gate bias $V_{gs} = 0 \text{ V}$. Since a large ΔE_c is necessary to reduce electron transfer from the QW to the gate barrier, design A is preferable. Design D has, however, acceptable values, which resemble those of design B. The simulations of Fig. 4 reveal that optimum performance, i.e., maximum j_c , g_m and minimum τ is obtained by design C. Design D gives satisfactory performance too, slightly degraded compared to C but still improved compared to A and B. Its Al composition is, however, maintained at a maximum of 30% which is an important design factor for avoiding



	Gate Barrier 300Å	Quantum well 80Å	Collector barrier 1000Å
A —□—	$\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$	GaAs	$\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$
B —●—	$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$
C —○—	$\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$	$\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$	$\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$
D —■—	$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$	$\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$	$\text{Al}_{0.17}\text{Ga}_{0.83}\text{As}$

FIG. 4. Influence of QWET material choice on device performance. (a) collector current density j_c , (b) transconductance g_m , (c) intrinsic delay time τ . (d) QWET material choices: lattice-matched AlGaAs/GaAs, InAlAs/InGaAs and pseudomorphic AlGaAs/InGaAs designs.

DX-center related problems.

The pseudomorphic design D was selected for a final optimization of the QWET from the point of view of doping layer placement. As suggested by Grinberg *et al.*² doping can be provided in the top (gate) layer (I), the QW itself (II), the bottom collector barrier (III) or in a thin region at the top of the device separated from the QW by an undoped material of same composition (IV). The simulation results for devices (I) to (IV) are shown in Fig. 5 together with the various device cross sections. Design III exhibits the best performance because it bends the electron potential of the bottom layer and reduces consequently directly the effective barrier height from QW to collector. This design is however, impractical since it can enhance tunneling current leakage between the source and collector terminals and also give rise to early breakdown by the electric field peak near the QW/collector barrier interface. It will therefore not be considered in the discussion below. The highest current density is obtained with design (I) but larger current modulation over the applied V_{gs} is possible with structure (II) or (IV).

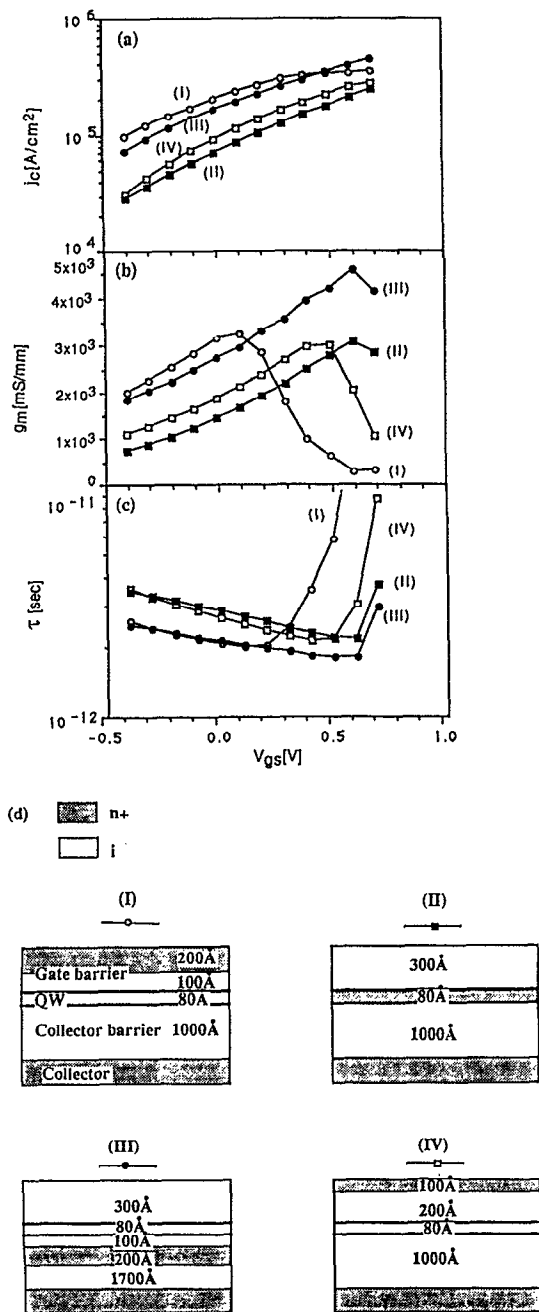


FIG. 5. (a): Collector current density j_c , (b): transconductance g_m , (c): intrinsic delay time τ of different design choices (doping position optimization). (d) QWET design choices: (I) Gate barrier-doped design with spacer, (II) QW doped design, (III) collector barrier doped design with spacer, and (IV) doping only in the top region of the gate barrier.

The small voltage swing of (I) arises from the electron transfer from the QW to the gate barrier which limits further the carrier modulation. The peak g_m values are almost the same in the three cases (I, II, IV) but shifted with respect to each other. The lowest intrinsic delay time is shown by device (I) but this is unfortunately done over a limited V_{gs} bias range. Among the various designs the QW doped device (II) shows probably the best compromise in g_m and τ over a large bias range. This design also provides less gate leakage current compared to those of gate barrier doped designs. Unlike the

lattice-matched AlGaAs/GaAs designs the pseudomorphic approach using doped QW is also suffering less from QW conductivity degradation. This is due to the high In content of the QW channel which reduces the importance of this effect. Summarizing the results, the pseudomorphic doped channel QWET designs offer the possibility of achieving high current drive (2×10^5 A/cm²), high transconductance (3 S/mm) and high speed (2 ps) while combining the technological advantage of selective QW contact and low Al content layers.

IV. CONCLUSIONS

A self-consistent analysis of the quantum-well emission transistor (QWET) was presented in which Poisson's equation and Schrödinger's equation are solved self-consistently. The numerical approach allows exact calculation of the ground-state energy in the QW, which is most essential for determining the device characteristics. The limitations imposed by the analytic approach of previous work are also overcome. The simulation results show that the AlGaAs/GaAs and InAlAs/InGaAs lattice-matched systems suggested earlier are less optimistic than initially thought. A pseudomorphic AlGaAs/InGaAs QWET design is presented as alternative material system. The introduction of excess In in the QW of this design offers comparable conduction band offset with smaller Al mole fraction in the adjacent AlGaAs layers. Furthermore, a higher mobility is achieved along the strained interface leading to small source resistance and improved transit time. Pseudomorphic Al_{0.4}Ga_{0.6}As/In_{0.15}Ga_{0.85}As/Al_{0.2}Ga_{0.8}As and Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As/Al_{0.17}Ga_{0.83}As systems offer almost the same conduction band offset between gate barrier and QW and show comparable electrical performance. The latter is adopted because it uses lower than 30% Al mole fraction in the AlGaAs layers and offers higher electron mobility along the QW due to the high In content. Among the various QWET structures the QW doped design shows the best compromise in device performance and over a large bias range. The analysis shows that optimum structures of this type exhibit high current driving capability (2×10^5 A/cm²), high transconductance (3-s/mm) and high speed (2 ps). Along with its high input impedance the QWET can be considered as an attractive device for many very high-speed applications.

ACKNOWLEDGMENTS

The authors would like to thank Professor J. Singh and Dr. M. Jaffe for extremely useful discussions and help in the simulations. This work was supported by NASA under contract No. NAGW-1334.

- ¹ A. Kastalsky and A. A. Grinberg, Appl. Phys. Lett. **52**, 904 (1988).
- ² A. A. Grinberg and A. Kastalsky, J. Appl. Phys. **65**, 821 (1989).
- ³ A. A. Grinberg, A. Kastalsky, and L. G. Shantarama, J. Appl. Phys. **66**, 425 (1989).
- ⁴ A. Kastalsky and S. Luryi, IEEE Electron. Dev. Lett. **EDL-4**, 334 (1983).
- ⁵ S. Luryi, A. Kastalsky, A. Gossard, and R. Hendel, IEEE Trans. Electron Devices **ED-31**, 832 (1984).
- ⁶ G. I. Ng, D. Pavlidis, M. Jaffe, J. Singh, and H. F. Chau, IEEE Trans. Electron Devices **ED-36**, 2249 (1989).