CCD-based reflection high-energy electron diffraction detection and analysis system

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A CCD-based, computer controlled RHEED detection and analysis system that utilizes an on-chip integration technique and on-board data manipulation is described. The system is capable of *in situ* time-resolved measurements of specular and integral-order intensity oscillations, their phase differences, streak linewidths, and epitaxial layer lattice constants. The digital RHEED techniques are described in the context of Co/Au bilayer, GaAs/GaAs, and $In_xGa_{1-x}As$/GaAs MBE growth. The system is compared to other RHEED detection devices.

I. INTRODUCTION

The demand for highly ordered, low-dimensional semiconductor materials for use in optoelectronic devices has resulted in the development of advanced thin film crystalline growth methods, the most well known of which is molecular beam epitaxy (MBE).[1-4] The UHV conditions under which MBE is performed permits the use of various surface science probes for monitoring and controlling the growth at the atomic level.[5] In this paper we describe the application of CCD (charge-coupled device) imaging technology to one of the most widely employed *in situ* surface structure probes, reflection high-energy electron diffraction (RHEED). The developments presented here offer a significant improvement in the recording, analysis and storage of RHEED data, extending the probe into the domain of time-resolved measurements.

RHEED is a very useful and practical means to analyze surface structure during MBE growth. By observing the diffracted streak positions and shapes one obtains information on surface reconstruction and morphology, as well as strain for heteroepitaxial systems.[6-8] For deposition that proceeds in a nucleation and growth mode, it is well known that by recording the diffracted streak intensity oscillations one can accurately determine the epitaxial growth rate.[9-11] This information can in turn be used to calibrate beam fluxes and regulate growth rates. By monitoring the linewidth during growth the surface dynamics can be studied,[12] and recently interest has been directed to the phase relationships between various diffraction streak intensity oscillations.[13]

Many techniques have been developed to extract the wealth of information contained in the RHEED pattern during growth. The most common method for monitoring intensity oscillations is via an optical fiber coupled to a photodiode or photomultiplier tube (PMT).[11,14,15] This method allows only the intensity detection of a preselected spot on the screen. In order to scan an extended streak, or image an entire RHEED pattern, the optical fiber is mounted on an XY stage. Alternatively, the diffracted electrons are magnetically deflected such that the peaks are scanned over a fixed PMT mounted on the phosphor screen.[11]

For measurements that require monitoring of more than one spot region of the RHEED pattern, the PMT or photodiode based systems are inherently slow and awkward. More recently, several research groups have developed video-data-acquisition RHEED imaging systems.[16-20] These systems typically employ a vidicon-tube video camera for RHEED pattern detection. The video signal is then recorded by a VCR for later playback or digitized by electronic hardware typically mounted in the backplane of a desktop computer.

The video-based systems have many advantages over conventional PMT systems. They are area detection devices, so one can simultaneously analyze multiple regions of the RHEED pattern. Video transfer rates are quite fast (typically 30 frames per second), so time-resolved studies are possible. The video signals (typically RS170 format) are serial and linearly related to the optical position on the detector, so data acquisition is not difficult. Finally, there are many commercially available "digitizing" boards that perform high speed A/D conversion and make data acquisition with a personal computer relatively easy.

However, there are some drawbacks to video-based detection systems. RHEED analysis by VCR playback is not ideal. Besides being tedious, the VCR output synchronization signal in the still-frame mode is choppy, and digitizing boards cannot synchronize properly with the incoming signal, thus creating a noisy digitized image. One may avoid this by "frame grabbing" during VCR playback (without using the still-frame function), but then time resolution is lost because the interval between frame grabbing, and thus the timing of the data points, cannot be accurately determined. Digitizing the diffraction pattern during growth is usually more convenient and is accurately time-resolved. However, the digitized images are typically 128–256 kbytes, so hard disk memory is used quickly during growth runs. Also, considerable time is spent writing these large files to disk, and thus temporal resolution is lost. Hence, data reduction techniques must be developed. A system developed by Resh *et al.*[16] records only data from selected "windows" of interest from the RHEED pattern, reducing data collection and processing times.

For many calculations, such as lattice constant variations[18-21] and strain[8] during heteroepitaxial growth, it is necessary to determine time-resolved peak position and

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linewidth of first order and other integral-order diffraction streaks, while still monitoring the intensity oscillations in order to determine deposition rates and thicknesses. Not only does this require an area detection device with sophisticated data extraction and reduction capabilities, but the detector must have high sensitivity and large dynamic range. For some growth processes, e.g., MBE of metals, the integral-order streaks are of very low light intensity during various stages of growth. The signal-to-noise ratio (S/N) is so low that quantitative analysis cannot be performed using typical vidicon tubes. Furthermore, the dynamic range required for these measurements and RHEED rocking curves, typically 10^3, is too high for vidicons.

In this paper we discuss a comparatively inexpensive CCD-based RHEED detection and analysis system that eliminates the afore-mentioned difficulties. By utilizing an on-chip integration technique and a sophisticated data reduction scheme, we can measure *in situ*, simultaneous, time-resolved specular and integral-order intensity oscillations, their phase differences, and streak linewidths. Also, lattice constant and strain variations may be determined from peak positions. We have demonstrated such measurements on both semiconductor- and metal-based MBE growth.

II. EXPERIMENTAL CONSIDERATIONS

There are three main features of our system that allow the above-mentioned measurements: (1) use of a CCD detector, (2) computer controlled on-chip time integration, and (3) rapid data acquisition and manipulation using a "frame grabber" board and its on-board memory. These features will be discussed in the next three sections.

A schematic of our setup is shown in Fig. 1. The components consist of a 15 keV electron gun (VG LEG 110 RHEED gun designed for UHV operation in semiconductor and metal MBE systems), phosphor screen, light-gathering lens system, Fairchild CCD5000 detector, Data Translation DT2853 8-bit frame grabber board, charge transfer inhibit line, black and white analog monitor, and IBM compatible desktop computer. The 15 keV electrons impinge on the surface of the sample at a grazing angle and the diffracted electrons strike the phosphor screen at the opposite side of the growth chamber. A light-gathering lens system consisting of an f/1.4 adjustable focal length 35 mm lens and three wide-angle lenses focus the RHEED pattern onto the CCD chip. The chip has a resolution of 488 (vert.) $\times$ 380 (hor.) pixels, each pixel being 18 μm (vert.) by 30 μm (hor.), of which 18 μm $\times$ 12 μm is optically active (due to the opaque vertical shift register design of this CCD). The clocking is three-phase, and the chip is thermoelectrically cooled to 20° below ambient in order to reduce thermal noise. The RS170 format video signal from the CCD is digitized by the DT2853 frame grabber board and stored in one of two 256 kbyte on-board memory buffers. The digitizing board is an 8-bit A/D flash converter, operating at 10 MHz. We plan to upgrade to a 12-bit board in order to utilize the dynamic range of the detector. The board digitizes entire images at normal video rates (30 frames/s). The frame grabber is mounted in the backplane of an IBM/AT compatible computer, which controls data manipulation and reduction, as well as triggers the on-chip time integration and any delays needed during growth.

By placing a piece of graph paper on the RHEED screen and counting the number of pixels per centimeter, we have determined the demagnification of our lens system to be 3.1. Knowing the distance between the sample and the screen and using the demagnification factor above we have determined the vertical and horizontal angular resolution to be 0.015 and 0.025 deg/pixel, respectively.

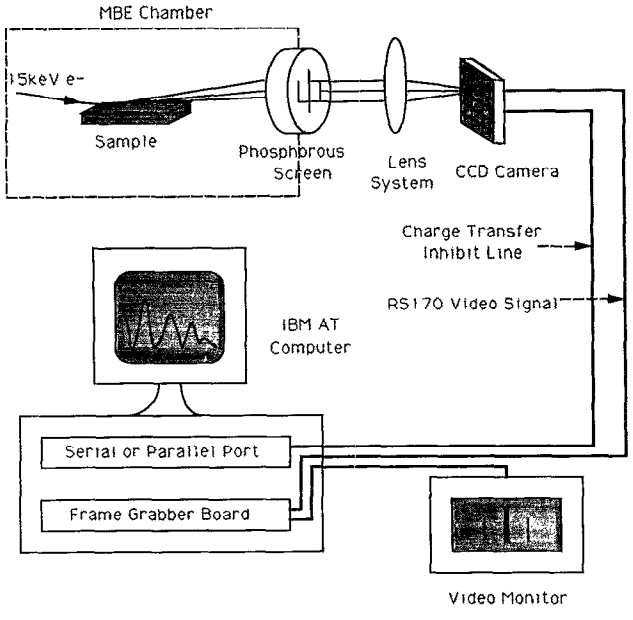

FIG. 1. Schematic diagram of RHEED detection system.

III. CCD DETECTOR

The main component of a CCD is the photosensitive silicon chip. The chip is effectively divided into a two-dimensional array of photosites, or pixels, by the application of periodic potential wells. As photons strike the silicon, electrons are excited to the conduction band and trapped in their respective photosites by the potential wells. The number of carriers created is directly proportional to the number of incident photons. After a given exposure time (typically 1/60 s for each field, odd and even, at normal video rates) the wells are rapidly varied, or "clocked," transferring the charge packets to vertical shift registers where the packets are read out, amplified, and converted to a serial analog signal.

There are many advantages to using a CCD for RHEED imaging. CCDs are area imaging devices, and thus multiple regions of interest may be recorded during growth. They are highly linear devices, much more so than vidicons. This makes data interpretation as well as absolute intensity calculations much easier. There is a precisely linear relationship between the serial video signal and the corresponding real space photosite. This is not true for vidicons, where the rastering of the photosensitive element can result in spatial error in the corresponding image. CCDs cannot be damaged by high light levels like PMTs and vidicons can: the wells are

simply saturated with electrons and the image becomes "white." The dynamic range of CCDs is typically 10^4; hence RHEED rocking curves and lattice constant calculations, which require a dynamic range on the order of 10^3, can easily be done with CCDs, whereas this type of measurement is impossible with a vidicon camera. For low light level applications and on-chip time integration (discussed below), the CCD is by far the best detection device. Quantum efficiency of CCDs at optical wavelengths is greater than PMTs and vidicons, and the inherent background noise is very low, due mostly to thermal noise. The typical background noise for a vidicon is much higher, and increases the longer imaging continues and the more intense the image becomes.[17]

A. Signal-to-noise considerations

The most important quality of the CCD for the present application is the ability to perform on-chip time integration. By inhibiting the charge transfer signal in the CCD electronics, i.e., by inhibiting the clocking of the potential wells for a given time period, the individual photosites will be exposed to the image for a correspondingly longer time, thus increasing the amount of electronic charge in each well. Since the number of e^- created is proportional to the number of photons, the number of e^- created is directly proportional to the exposure time, or on-chip integration time. This is a much more effective manner to build up the S/N ratio compared to conventional "time integration" techniques, which are the coaddition of a series of images whose exposure time is the typical video rate (1/30 s).

As a simplified explanation of the difference between frame coaddition and on-chip integration, consider frame coaddition using a vidicon and on-chip integration using a CCD. The background and noise for the vidicon are designated by $B_{\rm vid}$ and $\Delta B_{\rm vid}$, respectively. Both $B_{\rm vid}$ and $\Delta B_{\rm vid}$ will depend on the signal strength and operation time, but we will neglect this dependence for clarity. For the CCD the background and noise are $B_{\rm ccd}$ and $\Delta B_{\rm ccd}$, respectively. Both $B_{\rm ccd}$ and $\Delta B_{\rm ccd}$ will have a slight exposure time dependence. (For a CCD $\Delta B_{\rm ccd}$ is due mostly to thermal noise, it is inherently small, and can be decreased by cooling the chip, as in our case. For a vidicon $\Delta B_{\rm vid}$ is due to both thermal and electronic noise, and is typically much greater than $\Delta B_{\rm ccd}$). The total signal is designated by S. The actual signal is then $S-\langle B_{\rm vid}\rangle$ and $S-\langle B_{\rm ccd}\rangle$ for the vidicon and CCD, respectively.

The S/N ratio for an N frame coadd, where N is the number of frames, is then

$$(\mathrm{S/N}) = \frac{N(S-\langle B_{\rm vid}\rangle)}{\Delta B_{\rm vid}\sqrt{N}} \quad (N \text{ frame coadd}).$$

Since each frame has a $\frac{1}{30}$th second exposure time, for the on-chip time integration we integrate for $N/30$ seconds to obtain the same time resolution as the N frame coadd. N now represents the integer multiple of $\frac{1}{30}$th second that corresponds to the desired integration time. The S/N ratio is

$$(\mathrm{S/N}) = \frac{NS-\langle B_{\rm ccd}\rangle-\alpha N}{\Delta B_{\rm ccd}+\beta\sqrt{N}}$$

($N/30$ second on-chip integration),

where we have explicitly included the integration time dependence of the background (αN) and the noise ($\beta\sqrt{N}$). For our system $\alpha = 0.16$ DN and $\beta = 0.02$ DN (DN = digital number, range 0–255). Hence for typical integration times ($\leqslant 2$ s) αN and $\beta\sqrt{N}$ are negligible. We see the fundamental difference between the two techniques is that the background is not built up, or coadded, for the on-chip time integration. Hence for a low signal (comparable to the background), an on-chip integration is very effective in rapidly increasing the S/N ratio, whereas a frame coadd over many frames is required before significantly increasing S/N. For a strong signal ($S \gg \langle B\rangle$) S/N is increased by a factor of N for an $N/30$ s on-chip integration, compared to $\sqrt{N}$ for an N frame coadd. We note that when N becomes large the noise ($\beta\sqrt{\mathrm{N}}$) accumulated during on-chip integration becomes significant and S/N increases as $\sqrt{N}$.

Due to the sensitivity of the CCD, adequate S/N ratio can be obtained with very short integration times, typically $\frac{1}{5}$–$\frac{1}{2}$ s for lattice constant and linewidth calculations for semiconductor growth. Thus time resolution is still high. For similar calculations on metal grown surfaces, the integration required may be 1–2 s at the longest. Figure 2 shows the intensity profile for a typical GaAs RHEED pattern for two different integration times. The e^- beam was incident along the [110] direction and the substrate temperature was 530 °C. The integration times were $\frac{12}{30}$ and $\frac{1}{30}$ s for the top and bottom profiles, respectively. The S/N ratio for the $\frac{12}{30}$ s integration time is thereby increased by a factor of ≈ 10. Half-order streaks from the 2×4 GaAs surface reconstruction may be resolved. As described below, we have a resolution of

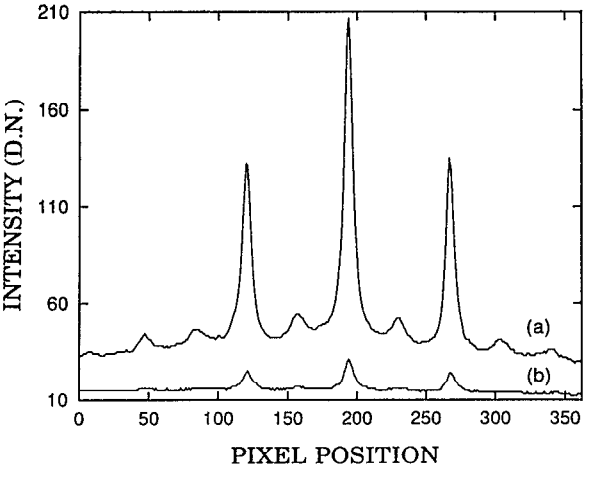

FIG. 2. Typical GaAs RHEED intensity profile for two different integration times: (a) $\frac{12}{30}$ s; (b) $\frac{1}{30}$ s. The e^- beam was incident along the [110] direction and the substrate temperature was 530 °C. The S/N ratio in (a) is increased by a factor of ≈ 10 relative to (b) due to the time integration, and the $\frac{1}{2}$-order streaks from the 2×4 GaAs surface reconstruction may be resolved.

1/30 s in time integration, and thus we may tailor the time integration to the particular data that need to be extracted from the RHEED pattern. We believe this is a most efficient way to monitor the RHEED pattern during growth.

Additional improvements in S/N are suggested by the use of digital lock-in techniques, but these would require modification of the CCD chip architecture, specifically the inclusion of a difference amplifier. We note the related technique of correlated double sampling has been used to reduce amplification fluctuations in some low-noise scientific CCD applications.[22-24]

IV. COMPUTER CONTROLLED ON-CHIP TIME INTEGRATION

By using the computer to trigger integration start and stop times, time integration can be precisely controlled ($\frac{1}{30}$ s resolution) and time resolution maintained. There are three components that constitute the time integration technique: (1) output control/status register on the DT2853 board; (2) 0–5 V high/low pin on the parallel or serial port of the computer; (3) charge transfer inhibit line. The DT2853 has an output control/status register that can be read to determine if vertical synchronization is occurring, and which frame field (odd or even) is being digitized from the video signal. At the beginning of each frame (both odd and even) the DT2853 strips a vertical "sync" signal from the composite video signal and, via a phase-locked loop circuit, synchronizes with the video input. This process takes about 630 μs, during which time "blanking" occurs. While synchronization is taking place, the vertical sync bit on the output control/status register is set.

The on-chip integration is performed as follows. When the field bit is set, the odd field is being digitized, and therefore the even field is accumulating signal. We read this bit initially via the software until it goes high, and continue to read it while it remains high ($\frac{1}{60}$ s). Once the field bit goes low, indicating the even field is being digitized, we pull the charge transfer line low via a 0–5 V bit in the computer serial or parallel port. Because of the vertical sync that occurs at the beginning of each frame, the field is not output for 630 μs after the field bit goes low. This is sufficient time to short the charge transfer line and inhibit the potential wells from clocking. By continuously reading the field bit and counting the number of times it is set high, the integration time can be precisely regulated (to within $\frac{1}{30}$ s), and any integration period can be achieved (any multiple of $\frac{1}{30}$ s). Once the desired integration time is elapsed, i.e., the number of times the field bit is set high equals the multiple of $\frac{1}{30}$ s desired, the field bit is read until it goes low, indicating both odd and even fields have been time-integrated for the same time period. The charge transfer pin is immediately set high (during vertical sync), and the resultant time-integrated image is digitized after the vertical sync is set. The image is stored in one of two on-board 256 kbyte frame buffers. A block diagram of the on-chip integration technique is shown in Fig. 3.

We note here that the charge transfer line is a simple switch that does not need any filters, etc. Even though the 0–5 V line from the computer typically has high frequency

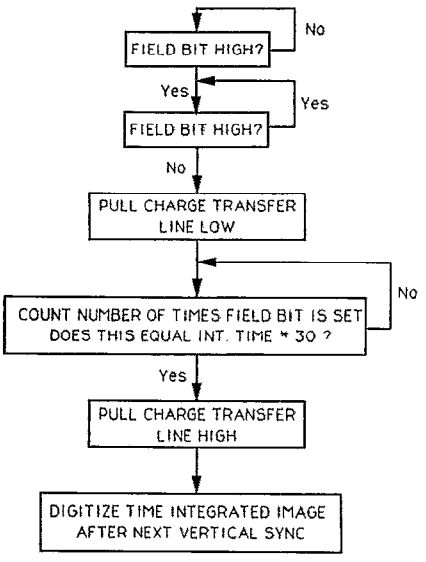

FIG. 3. Block diagram of computer controlled on-chip time integration technique.

transients, this does not affect the charge transfer line. If the line is open (> 2.5 V), charge transfer is not inhibited; if it is closed (0 V), charge transfer is inhibited, and charge is built up at each photosite. For many commercial CCD systems the charge transfer control is conveniently accessed via a single pin on the electronic control box. For other systems a brief reading of the electronic control board schematic will indicate the charge transfer line, and thus a simple tap will allow the time integration to run properly. Note the charge transfer line should be a floating line. If the circuit is completed via ground from the electronic control box to the computer ground, the image will be of very poor quality.

By the above-described method we are able to perform on-chip time integration for any integration period (accurate to $\frac{1}{30}$ s), and the time integration may be performed repeatedly to obtain any number of time integrated images. As a simple example, Fig. 4 shows a time-integrated, digitized image of a typical RHEED pattern for a 2×4 reconstructed GaAs surface. The e^- beam was along the [110] direction. A 4.0 s integration time with a background subtraction was performed to enhance the half-order and higher-order diffraction streaks. These streaks could not be detected at video-rate exposure times. A neutral density filter was placed over the intense specular streak so it could be monitored without saturating.

V. DATA ACQUISITION AND REDUCTION

Once the (time-integrated) image is stored in an on-board memory buffer, the relevant data must be extracted from it. This must proceed without sacrificing time resolution. We utilize the two on-board memory buffers and the high-speed data transfer between buffers to perform time-resolved data manipulation, extraction, and reduction.

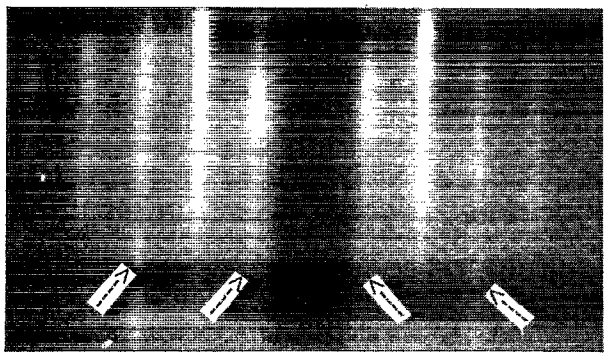

FIG. 4. Time-integrated, digitized image of a typical RHEED pattern for a 2×4 reconstructed GaAs surface. The e^- beam was incident along the [110] direction. A 4.0 s integration time with a background subtraction was performed to enhance the half-order and higher-order diffraction streaks. These streaks could not be detected using video-rate exposure times. A neutral density filter was placed over the intense specular streak so it could be monitored without saturating. The half-order streaks are denoted with arrows.

One buffer, designated the "image" buffer, receives each time-integrated image. The region(s) of interest are then copied to the remaining buffer, designated the "data" buffer. Since the buffers are located in extended memory, any data transfer, including the copying of an entire 256 kbyte image from one buffer to the other, takes essentially zero time to complete. The next time-integrated image is stored in the image buffer, thus overwriting the previous image. The relevant data are again transferred to the data buffer and placed underneath or next to, but not overlapping, the previous set of data. In this manner the growth is recorded. Once the entire 256 kbyte region is occupied with data, the data image must be stored on hard disk.

For time-resolved lattice constant and strain determination, as well as intensity and linewidth oscillation measurements, we find a "linescan" mode of operation most efficient. Before growth we determine a particular row of the CCD chip on which to perform the linescans. For simple specular and first-order intensity and linewidth monitoring, this row will bisect the specular and first-order streaks. A time-integrated RHEED image is scanned for the proper row using the cursor overlay utility of the frame grabber board, which overlays a cursor cross hair on the video monitor and allows the user to move the cross hair to any row and column position on the image.

To aid in row scan determination, intensity plots of any row may be performed. Row and column plots can also be used to focus the image and determine RHEED symmetry (e^- beam azimuth angle). By performing row scan plots on images of varying time integration, the integration time needed to maximize S/N without saturating the specular beam is determined.

Once the proper row and integration time are determined, growth is started. Each time-integrated image is momentarily stored in the image buffer while the proper row is transferred to the data buffer. The first image linescan is stored in row one of the data buffer, the second in row two, etc. A maximum of 512 linescans may be taken before the data buffer must be stored on hard disk (512 lines by 512 pixels per line). This "linescan" mode offers significant data reduction with no loss of time resolution.

VI. SYSTEM PERFORMANCE

As a simple example of this operation, the specular beam intensity and linewidth oscillations for the growth of GaAs on GaAs at 545 °C are shown in Fig. 5(b). The e^- beam was along the [110] direction. No time integration was needed for this run. Figure 5(a) is the data image, which contains the linescans "stacked" vertically in time (corre-

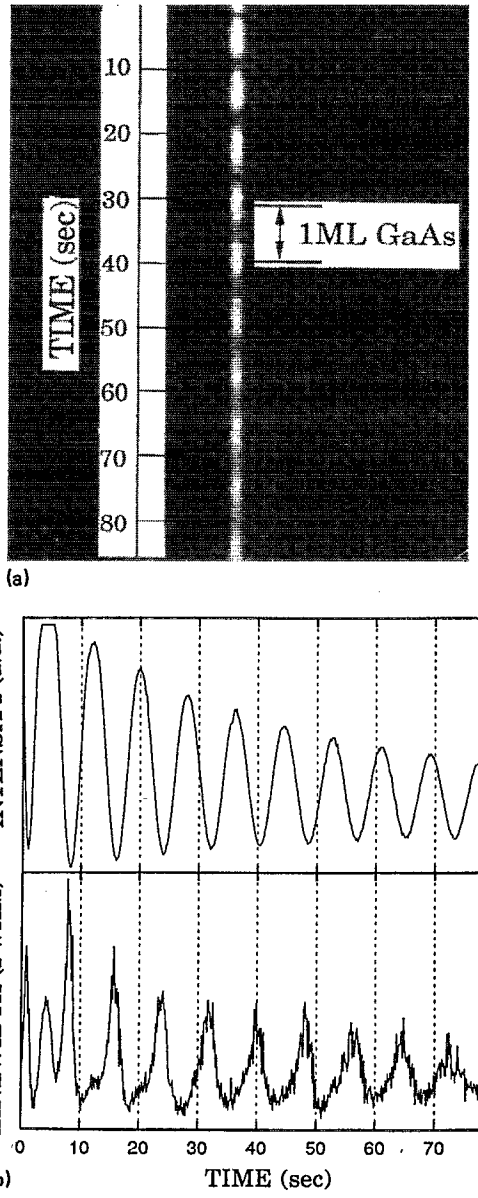

FIG. 5(a) Specular beam "data" image (see discussion in text) for growth of GaAs on GaAs at 545 °C. The e^- beam was incident along the [110] direction. The linescans are "stacked" vertically in time (film thickness). 510 linescans were performed, with a delay of 0.15 s between scans. Integration time: $\frac{1}{30}$ s. (b) Specular beam intensity and linewidth (FWHM) oscillations for the data image in (a).

sponding to film thickness). One can clearly see the intensity oscillations as growth progresses. A column scan of the image streak yields the intensity oscillations, and a FWHM analysis of each row yields the linewidth oscillations.

The linescan mode has also been used to perform time-resolved RHEED streak width and spacing determination during metal heteroepitaxial growth. Shown in Fig. 6 are intensity profiles across the specular and first-order streaks at different stages during the growth of a Co/Au bilayer. The e^- beam was along the Co [1120] and Au [110] axes, and the deposition rates were 0.2 Å/s Co and 0.05 Å/s Au. The integration time required was 2.0 s and the substrate temperature was 50 °C. Although submonolayer resolution was achieved, for clarity only selected scans during growth are plotted. We see the RHEED streak spacing and linewidth development are very different during the growth of Co layers and Au layers. By analyzing the change in first-order streak spacing during the growth of the bilayer, we have estimated the strain at the Co/Au interface to be 5.5%.[8]

We have also used the linescan method to determine phase relations between specular and integral-order intensity oscillations. By performing multiple column plots of the linescanned image, we obtain the phase-lag between specular (00 beam) and first-order (01 beam) streak oscillations (Fig. 7) for GaAs on GaAs growth at 545 °C. The e^- beam was in the [110] direction, $\pm$ 1°. The integration time required here was 0.5 s.

Recently we have also investigated the growth of $In_xGa_{1-x}As$ on GaAs.[21] The abrupt change in surface morphology at a certain critical thickness has been the focus of study for several research groups.[18-21] The RHEED pattern is clearly different before and after critical thickness: streaky before and spotty after. Consequently, the positions of the specular and first-order streaks (spots) change significantly during growth, and hence multiple regions must be monitored or "windowed."

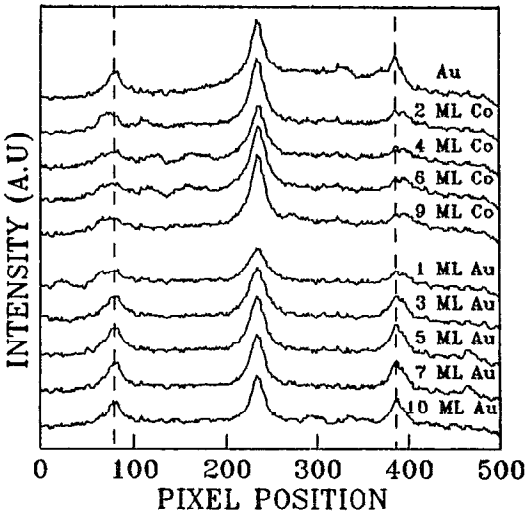

FIG. 6. Representative RHEED streak intensity profiles recorded at various stages of Co/Au bilayer growth. The e^- beam was along the Co [1120] and Au [110] axes, and the substrate temperature was 50 °C. The central peak is the specular beam. Not all profiles are shown. Integration time: 2.0 s.

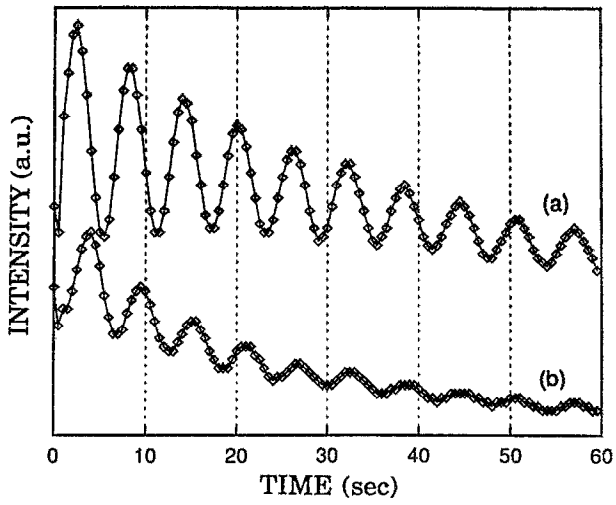

FIG. 7. Phase difference between (a) specular (00 beam) and (b) first-order (01 beam) streak oscillations for GaAs on GaAs growth at 545 °C. The e^- beam was along the [110] direction $\pm$ 1°. The data were smoothed using a five-point boxcar average. Integration time: 0.5 s.

We use a modified linescan mode to extract time-resolved lattice constant and intensity oscillation/deposition thickness data. The position of the first-order streaks before and after critical thickness is different, as well as the specular beam position. The positions of these regions also shift during growth. To monitor the specular beam intensity (the specular beam is generally not colinear with the first-order streaks for this growth) we choose an adjustable window, typically a 10×10 pixel region, to "track" the specular beam. For each time-integrated image the 10×10 window is scanned for the maximum intensity value. This value is stored in a software array. The extra processing time required for tracking on our current system (286 machine) is 0.06 s per data point. To monitor the first-order streaks two separate rowscans are performed. The scanning row for the spotty pattern first-order streaks must be determined by a trial run. The streaky pattern linescans are stored in data buffer rows 1–256, and the spotty pattern linescans in rows 257–512. Thus for this type of operation only 256 data points may be taken before the data buffer must be stored to hard disk. We have also implemented a routine that averages a multiple linescan area for both the streaky and spotty pattern regions (after time integration and typically over five linescans for each region) in order to compensate for shifts in vertical position of the streaks. However, we have found this unnecessary for accurate lattice constant determination.

Simultaneous time-resolved intensity oscillations and lattice constant measurement for the growth of $In_{0.45}Ga_{0.55}As$ on GaAs at 535 °C with the e^- beam in the [110] direction is shown in Fig. 8. The required integration time was 0.5 s. We see that the lattice constant abruptly changes from that of GaAs to that of bulk InGaAs at an epilayer thickness of 4.5 ml. The change in lattice constant

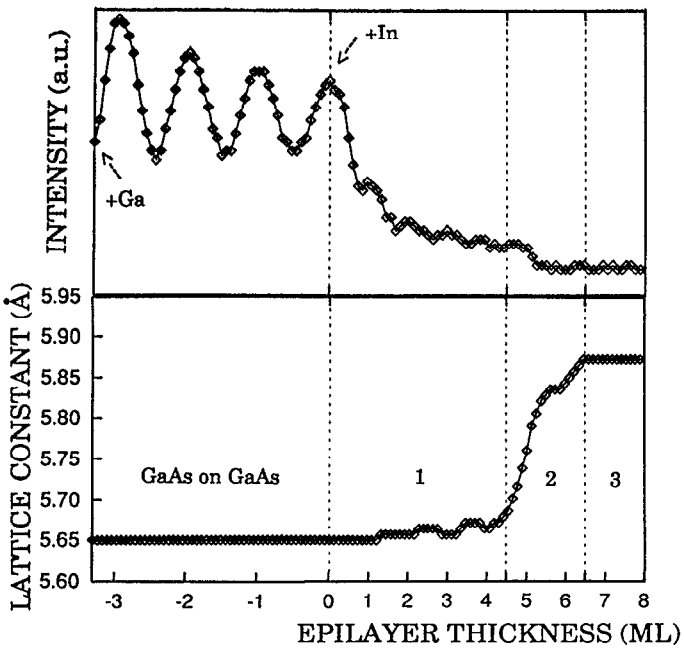

FIG. 8. Intensity oscillations and lattice constant measurement for the growth of $In_{0.45}Ga_{0.55}As$ on GaAs at 535 °C. The e beam was in the [110] direction. The lattice constant changes slowly in region 1, and the start of region 2 marks the onset of an abrupt change in the lattice constant to the bulk $In_{0.45}Ga_{0.55}As$ value. The lattice constant data was smoothed using a five-point boxcar average to smooth the discrete steps in lattice constant value due to the minimum detectable change of 0.7% for our system. Integration time: 0.5 s.

for this growth is 4% (the minimum detectable change by our system is 0.7%). We are using this method to arrest growth in each of the three regimes labeled, in order to perform TEM and STM on the sample for each regime. From this analysis we hope to develop a model for this growth process.

VII. SOFTWARE AND SCOPE

We have combined the on-chip time integration and data extraction techniques described above into a single menu-driven software driver. The software is written in C, with calls made to the frame grabber board driver within C. The software driver allows the user to select the appropriate growth analysis mode: single image, multiple image, linescan, multiple linescan, or multiple region mode. The integration time, delays between data acquisition (accurate to 18 ms), and total number of data points are user selectable for all growth modes. The specular beam is tracked via a 10×10 window array, and the maximum intensity within this window is plotted in real-time on the monitor screen. This facilitates surface quality determination during growth, and allows commencement of heteroepitaxial growth on a smooth surface (intensity maximum). The elapsed time of the run is displayed at the end of growth, and the user is prompted for a filename in which to store the data. An analysis section allows the user to call up, display, and analyze any data image or on-board buffer. Analysis includes row scans, column scans, FFT's, linewidth and streak spacing determination.

The implementation of a CCD detector with the on-chip time integration and data extraction techniques described in this paper allows time-resolved measurement of virtually any RHEED parameter. This versatility, combined with the relatively low cost of the off-the-shelf components used to build this system, makes it an attractive method for RHEED growth analysis.

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