Integration of Functional Oxides With The Semiconductor Zinc Oxide

by

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ABSTRACT

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Ferroelectric/semiconductor heterostructures are desirable for multifunctional devices using the charge of a ferroelectric material to manipulate the conductivity of a semiconductor. The quality of the ferroelectric/semiconductor interface is critical for maintaining a significant ferroelectric polarization charge density, and coupling this charge density into the semiconductor. Therefore, materials must have excellent chemical and structural compatibility. The semiconductor ZnO is a promising candidate for integration with ferroelectric oxides, due to its excellent structural and chemical compatibility with such materials.

This report discusses the thin film growth of select ferroelectric and semiconductor materials, the fabrication of heterostructures and basic capacitor devices using such materials, and the characterization of structural and electrical properties thereof. Pulsed laser deposition (PLD) and molecular beam epitaxy (MBE) are used to obtain thin films of desired materials. Standard lithographic methods were used to pattern the materials and to deposit electrical contacts for subsequent testing.

Polycrystalline thin films of $Pb(Zr,Ti)O_3$ (PZT) were achieved through solution processing, and they exhibited ferroelectric behavior in polarization-electric field and capacitance-voltage measurements. Single crystal substrates of ferroelectric $LiNbO_3$ (LN) were purchased in bulk form. Weak c-plane preferential orientation of ZnO thin films was achieved using PLD on PZT films. Highly preferentially oriented c-plane ZnO films were obtained by PLD on LN substrates.

Ferroelectric/ZnO heterostructures using PZT and LN as prototype ferroelectric materials were studied. Pt/PZT/ZnO capacitors showed a memory window of 2V in capacitance-voltage and AC conductance measurements. An RLC circuit constructed using the PZT/ZnO capacitor shows a resonant peak shift of 30kHz, which is consistent with the expected change in capacitance with switching ferroelectric polarization. $LiNbO_3$/ZnO heterostructures show evidence of carrier concentration modulation in the semiconductor attributed to the ferroelectric polarization charge. Hall effect measurements revealed an order of magnitude reduction in measured carrier concentration in the ZnO thin film consistent with expected depletion caused by the ferroelectric polarization charge. The pyroelectric effect in LN substrates was exploited using a basic voltage divider circuit where the change in ZnO conductivity could be observed. Upon application of heat, the ferroelectric polarization charge increased, thereby causing further depletion of the ZnO film.

CHAPTER I

Introduction

This project studies several ferroelectric materials, the semiconductor zinc oxide (ZnO), and heterostructures of ferroelectric and semiconductor layers. The primary goal of this effort is to demonstrate charge modulation in the semiconducting layer via the switchable polarization in the ferroelectric layer. Successful integration will enhance performance of current devices based on either material system, and enable design of new multifunctional devices based on heterostructures.

Ferroelectricity was first discovered by J. Valasik in the Rochelle salt[1], and the interest in the effect remained purely academic for a long period. Our improved understanding of ferroelectric materials, the increased number of known and studied materials, and progress in processing technology led to the eventual commercial success currently enjoyed by ferroelectrics. These materials are now competitive especially in fast, low power memory devices that find use in smart cards, video games, and metrology tools. The applications and the understanding of ferroelectric materials stand to expand further through full integration with semiconductors; devices using ferroelectrics along with semiconductors are expected to penetrate the memory and sensor markets more effectively. Furthermore, voltage tunable dielectric constants of many ferroelectrics make them suitable for use in tunable components for

microwave circuits. These applications, along with applications that take advantage of piezoelectric, pyroelectric and electrooptic properties of this material family will benefit from full integration of ferroelectrics with semiconductors.

ZnO is a fast maturing semiconductor with significant research effort invested in it over the past decade. Even though this material has long been used in surface acoustic wave devices for its piezoelectric properties, interest in ZnO as a material for electronic and optoelectric applications came much later. Advances in material growth and deposition techniques are credited with the higher quality material now available, and thus with the renewed interest[2]. As a semiconductor ZnO is attractive firstly due to its large bandgap (3.4eV at room temperature) corresponding to the ultraviolet wavelength range. The large bandgap means ZnO is transparent to visible light; so, it is currently in use as a transparent conductor and channel material for transparent thin film transistors in display applications. Furthermore, there is progress in understanding the transport and doping mechanisms in ZnO. The persisting challenge of growing stable p-type ZnO is likely to be surmounted given the number of groups recently reporting sustained p-type behavior in ZnO films[2][3]. Achieving ZnO homojunctions will enable high performance UV emitters, detectors, and solid state white light sources.

ZnO has additional advantages that make it an attractive semiconductor for integration with ferroelectric materials. Most of the well-studied high performance ferroelectrics are complex oxides, and they are not chemically stable when in contact with traditional semiconductors. ZnO is chemically compatible and stable in contact with other metal oxides and complex oxides. It follows that a high quality interface with low defect density can be expected. ZnO also offers a favorable band line-up with several ferroelectric materials, as will be detailed in the following sections. There-

fore, ZnO is a promising candidate for ferroelectric/semiconductor integration. Once high quality interfacees are achieved the ferroelectric polarization charge can modulate charge in the semiconductor layer, and many new field effect devices can be designed. Among those, the most interesting ones are multifunctional devices such as sensor-transistors[4], and highly integrated memory cells. Successful ferroelectric/semiconductor interfaces mean further integration of ferroelectrics into electronics applications, as functional dielectrics in transistors, and microwave applications, are improved electro-optic modulators.

The rest of this chapter details the current and potential applications of both ferroelectric materials and ZnO semiconductor, along with progress and challenges on the way to ferroelectric/semiconductor integration. An overview of the physical properties of materials under study is provided. It must be noted that this is not a comprehensive list of potential applications, since new devices not yet conceived will emerge as the technology matures.

1.1 Ferroelectric Materials

Ferroelectric materials are a set of functional materials, which demonstrate multiple beneficial properties for use in electronics applications. A smart material is defined as one in which an external stimulus (pressure, heat, light, etc.) produces a detectable response. These are polar materials where the magnitude and the direction of the polarization charge is determined by an external electric field. Switchable polarization is the signature property of ferroelectric materials, many of which also exhibit significant piezoelectric, electrooptic, and pyroelectric properties, and DC tunable dielectric constants. Furthermore, ferroelectric materials often exhibit very high dielectric constants, because of which they are under study for gate layers in transistor applications.

The spontaneous polarization, P_s, can be controlled via an external electric field. This is in contrast to other polar materials, such as crystals in the wurtzite form, where the spontanous polarization is fixed. An important metric characterizing ferroelectric materials is the polarization charge present in the material in the absence of an applied electric field. This is called the remnant polarization, P_r, of the material. The electric field value at which the polarization changes sign is called the coercive field, E_c. E_c is a significant material metric especially for memory applications, since it determines the voltage window in which the material shows hysteresis. The range of values from -E_c to +E_c is called the memory window. Fig. 1.1 shows a polarization-electric field loop of a typical ferroelectric material.

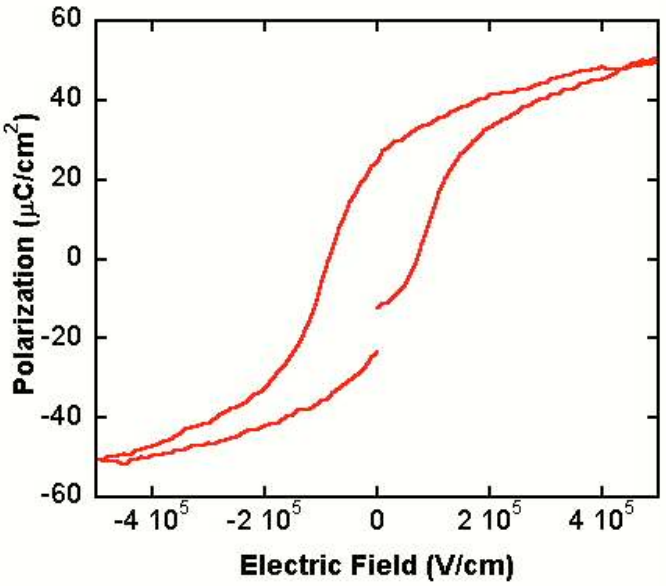

Figure 1.1: Hysteresis loop of a typical ferroelectric material

The formulation commonly used to write the polarization charge in the positive electric field direction is[5]:

$$P(E) = P_s \tanh(\frac{E - E_c}{2\sigma})$$

where

$$\sigma = E_c[ln(\frac{1 + P_r/P_s}{1 - P_r/P_s})^{-1}]$$

Ferroelectric materials find wide use in non-volatile ferroelectric random access memory (FeRAM) applications, and have enjoyed growing success since their commercialization in 1992. FeRAMs have found applications such as electrical power meters, smartcards, video games, data loggers. Fast switching (<100ns) and low power consumption make FeRAM an attractive choice for such applications[6][7]. Simple cell designs, some of which employ only one capacitor and one transistor, are typical for FeRAMs[8]. $Pb(Zr,Ti)O_3$ (PZT) is the current leading ferroelectric material for FeRAMs, primarily because it has very high P_r ($> 25\mu$ C/cm^2) and P_s($> 40\mu$ C/cm^2) values. These high values ensure the non-volatile nature of the memory capacitors. Increased spontaneous polarization of up to 40μ C/cm^2 has been observed through optimization of PZT growth parameters[9].

Continued commercial success of FeRAM devices has been possible through aggressive scaling. FeRAM based on sputtered PZT is expected to scale down to 0.18μm capacitor size before modifications to the ferroelectric material composition become necessary[10]. Advances towards a 3-dimensional memory stack are made through the use of metal oxide chemical vapor deposition (MOCVD) for 200nm thick PZT films, and atomic layer deposition (ALD) of Ir electrodes[11]. Challenges related to FeRAM remain; namely, endurance problems limit the read/write cycles possible before a memory cell degrades, and retention problems hinder the development of a nondestructive readout. Having to use a desctructive readout furthers the endurance problem of FRAMs, the two main challenges therefore being intertwined[12].

Many ferroelectric materials are used in radio-frequency (rf) devices in their paraelectric phase, in which the material shows no hysteresis. The main material property

exploited for rf devices is the tunable dielectric constant. Examples of such applications are tunable capacitors for filters, tunable phase shifters, delay lines, surface acoustic wave (SAW) and film bulk acoustic wave (FBAR) devices. Ferroelectric materials provide high speed tuning and relatively high quality factors (Q)[13].

The piezoelectric and pyroelectric properies of ferroelectric materials, especially of PZT, are employed for many transducers in micro electromechanical systems (MEMS). Pressure and temperature sensors, actuators, membranes, diaphrams are among examples of devices making use of these materials. PZT is used in many microvalves, micropumps, gyroscopes, and accelerometers. All ferroelectric materials are pyroelectric as well (the reverse is not true). This property leads to interest in ferroelectrics for temperature sensing and, more recently, for electronics cooling[14]. A 12K temperature change was reported as result of an applied electric field of 714kV/cm using PZT as the prototype pyroelectric material[15]. The effect exploited here is the electrocaloric effect, by which the temperature of the film changes due to an external electric field.

All of the applications given in this section can benefit greatly from full integration of ferroelectric materials with semiconductors. Memory cells where a single device can serve as the capacitor and the transistor will scale down fast, while circumventing many of the challenges listed. Memory applications present one area where the highly sought-after ferroelectric field effect transistor (FeFET) will make a great impact on the market. Integrated piezoelectric/ or pyroelectric/semiconductor sensor-transistors will modulate the semiconductor channel through polarization charge in the ferroelectric. The electrocaloric effect will be exploited more effectively when the applied electric field is fully translated to temperature change in the ferroelectric. For each of these applications, a low defect density ferroelectric/semiconductor interface

is the key to high performance. Given the promise of ferroelectric oxides for significant progress in memory, sensor, cooling, and MEMS applications, it is not surprising that there is significant research interest in these materials. Interfacing ferroelectric oxides with the semiconductor ZnO can provide a path to stable, low defect density interfaces with ferroelectrics. ZnO is chemically compatible with these functional oxides, therefore gradual degradation of devices at the ferroelectric/semiconductor interface is avoided. This will lead to higher reliability, thus longer lifetime of the memory device.

1.2 Zinc Oxide Semiconductor

Zinc oxide (ZnO) is an abundant II-VI compound semiconductor with a direct bandgap of 3.4eV at room temperature, corresponding to the ultraviolet wavelength range. Even though ZnO was already investigated and partially characterized in the 1930s, there has been renewed interest in the material within the last two decades. Development of bulk ZnO crystals and high quality thin films led to a resurgence in research into this semiconductor for electronic and optoelectric applications. Fig. 1.2 provides insight into the interest ZnO has attracted in terms of published papers with respect to decade. Several advantages make ZnO a semiconductor of intense research interest; for example, the availability of native substrates (in contrast to GaN), a large exciton binding energy (60meV), resistance to radiation damage, and compatibility with CMOS processing as well as with other oxide materials. Additionally, the large bandgap energy makes ZnO a good candidate for use in high-temperature and high-power applications.

Photodetectors and light emitters in the ultraviolet wavelength regime are highly desirable for systems to read/write ever-denser memory devices, solid state lighting, solar blind UV detectors, and lasers for medical applications. Light emitters are the

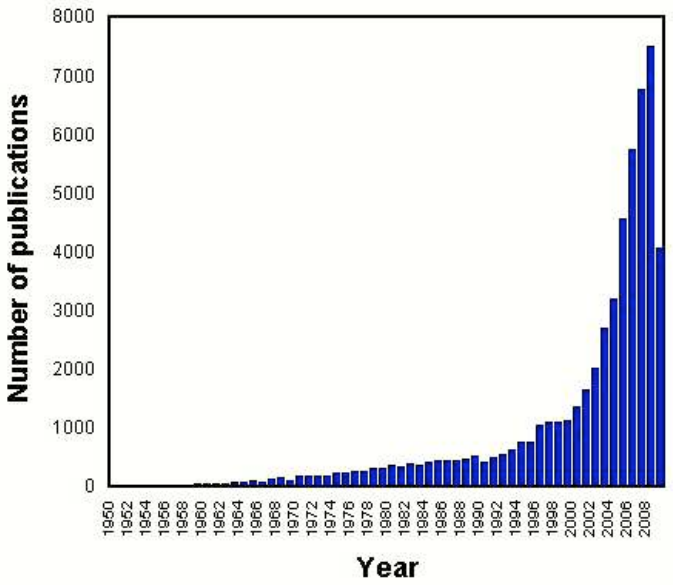

Figure 1.2: Number of publications on ZnO with respect to year

primary motivation for pursuing pn-junctions of ZnO, currently hampered by a lack of stable and repeatable p-type ZnO growth[3]. Light emitter work with ZnO is progressing with the use of heterostructures[16], while effort towards p-type doping of ZnO is yielding increasing success[3]. As-grown ZnO is n-type due to native defects that act as donors. The exact nature of these defects is being debated; the most likely sources of donors are zinc vacancies[17] (especially under oxygen-rich growth conditions), zinc interstitials[3], and hydrogen as an impurity[18][19][20][21]. Vacancies and interstitials are very difficult to avoid, and hydrogen is unavoidable in most growth and deposition techniques. Therefore, p-type doping requires not only the introduction of acceptors, but optimization of the growth technique and compensation for the n-type behavior. Carrier mobilities in p-type ZnO films have consequently been relatively low so far[3].

Alloys of ZnO present exciting opportunities for bandgap engineering, which is very important for optoelectronics applications. CdO and MgO are suitable materials for alloying with ZnO due to their bandgaps and similar growth and deposition re-

quirements as ZnO. Alloying ZnO and CdO results in the reduced bandgap compound $Cd_xZn_{1-x}O$ and alloying with MgO results in the increased bandgap compound $Mg_xZn_{1-x}O$. Small bandgap alloys are of interest for photodetectors and visible light emitters. Bandgaps as small as 2.99eV have been achieved through incorporation of Cd into ZnO, with x up to 0.07[22]. Alloys with MgO are primarily desirable to create barrier materials for quantum well structures for ultraviolet light emitters and detectors[23]. Single phase $Mg_xZn_{1-x}O$ has been reported with $x \leq 0.33$ before phase segragation is observed[24]. This x results in a bandgap of 3.9eV. Further engineering of wavelengths in luminescence are possible through quantum confinement. Blue shifts in photoluminescence of ZnO are observed through the construction of quantum wells[23].

Growth and deposition of high quality ZnO is studied thoroughly, and our understanding of the material is improving continuously. As the ability to grow device quality material is now within reach, ZnO becomes a realistic candidate for high-frequency high-power transistor applications. High field effect mobilities ($>100cm^2/Vs$), high on/off ratios (10^{12}), and high operating frequencies ($\sim$400MHz) have been reported[25]. These results were achieved via pulsed laser deposition (PLD) of ZnO followed by careful annealing, as opposed to the more costly molecular beam epitaxy (MBE) or metal oxide chemical vapor deposition (MOCVD) methods. Details on the deposition of ZnO using the PLD method are included in Chapter IV. ZnO thin film transistors hold additional promise because alternative gate dielectrics can be explored using ZnO as the channel material. (Ba,Sr)TiO_3[26], Al_2O_3, and HfO[27] gate dielectrics on ZnO channels have given researchers the opportunity to investigate both the high-k alternative dielectrics and the emerging semiconductor together. Results show improved sub-threshold behavior and help develop the understanding of both kinds of materials further.

ZnO is transparent to visible light, and has therefore found use as a channel material for thin film transistors for display applications. Furthermore, low-temperature growth or gallium or aluminum doping of ZnO leads to highly conductive transparent films[28]. So, doped ZnO is a low cost alternative to indium tin oxide (ITO) in producing high quality transparent contacts for displays and solar cells. The transparency of ZnO to visible light also makes it a good material for applications in solar blind photodetectors, contact materials for solar cells and transistors for display applications.

The attractiveness of ZnO for electronic and optoelectronic applications is further helped by its suitability to integration with other oxides. A distinct advantage of ZnO for this purpose over traditional semiconductors is its chemical compatibility with other oxide materials. Specifically, it is highly desirable (including in this project) to integrate ZnO with ferroelectrics such that we can use the ferroelectric polarization charge to modulate the conductivity of ZnO. We expect ZnO to form thermally and chemically stable heterostructures with ferroelectrics, with low defect densities at the ferroelectric/semiconductor interface. Effective coupling of the ferroelectric polarization charge into the semiconductor is expected to follow from a high quality interface.

1.3 Ferroelectric/Semiconductor Heterostructures

Given the desirable qualities that both ferroelectrics and semiconductors have, it is of high interest to integrate the two types of materials in a way that takes advantage of both. The goal in this project is to use the ferroelectric polarization to modulate the conductivity of the semiconductor; therefore, effective coupling of the ferroelecric polarization charge into the semiconductor is crucial. Losses due to interface defects

must be minimized for full integration to be beneficial. Fig. 1.3 shows this effect: The top layer is a ferroelectric material where positive and negative charges are separated due to polarization. Negative charges near the interface attract positive charges in the semiconductor, thus creating a positive sheet charge at the interface, whose density will depend on the magnitude of the polarization charge in the ferroelectric and the interface quality.

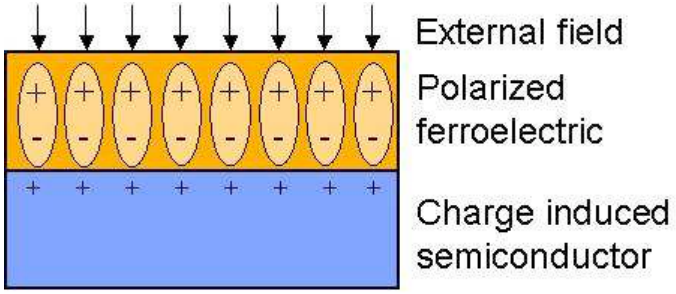

Figure 1.3: Schematic representation of ferroelectric polarization coupling into a semiconductor

Majority of ferroelectrics currently under study are oxide materials, and are not chemically compatible with traditional semiconductors such as Si and GaAs. Often, an interfacial oxide layer with undesirable properties (low dielectric constant, no spontaneous polarization) is observed upon deposition of a ferroelectric oxide on a semiconductor, resulting from oxidation of the semiconductor. This layer decouples the semiconductor and the ferroelectric, and therefore reduces the efficiency with which the semiconductor can be modulated. Even if an interfacial layer is not immediately present when the heterostructure is fabricated, further temperature treatment can lead to gradual degradation of the interface, making the use of buffer layers necessary[29]. The effect of the interfacial layer is shown in Fig. 1.4.

The formation of an interfacial SiO_x layer has been a barrier to the integration of ferroelectrics as alternative high-k dielectric materials in complementary metal oxide

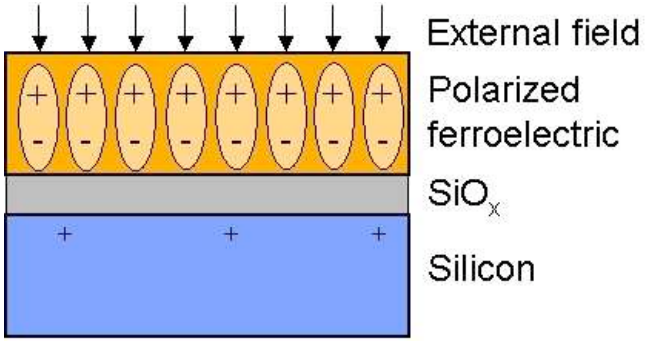

Figure 1.4: Schematic representation of a ferroelectric decoupled from silicon

semiconductor (CMOS) processes. Ferroelectric oxides are often thermodynamically unstable in contact with silicon, and indeed act as catalysts to silicate formation[30]. Ferroelectric oxides have been studied in detail on semiconductors such as Si[31],[32] and AlGaN/GaN[33]. The interfacial oxide layer is observed to be amorphous and it is shown in the cross sectional transmission electron microscopy (TEM) image from Hu et. al. in Fig. 1.5. We note that a new interface, the ferroelectric/amorphous oxide interface, is introduced in this case, where a high density of traps exist. The interface traps provide a tunneling path for carriers leading to leakage currents. Additionally, the properties of the interfacial oxide layer and the trap densities change over time with use, thereby causing instabilities in the electrical properties of devices using a such a heterostructure[30]. For example, a heterostructure such as shown in Fig. 1.5 can be used as the gate and the channel of a transistor. The threshold voltage of this transistor would shift over time, as changes in the interface continue to degrade the device.

Success in growing $SrTiO_3$ (STO) on Si was reported through the growth of 1 monolayer of Sr followed by a 4 monolayer thick BaSrO buffer layer[34]. Similarly, a very thin layer of Ti was used as a buffer layer for successful $BaTiO_3$ (BTO) and STO growth on GaAs[35]. A cross sectional TEM image of an BTO layer epitaxially grown on GaAs is shown in Fig. 1.6. In this case the interface is abrupt, and there is no

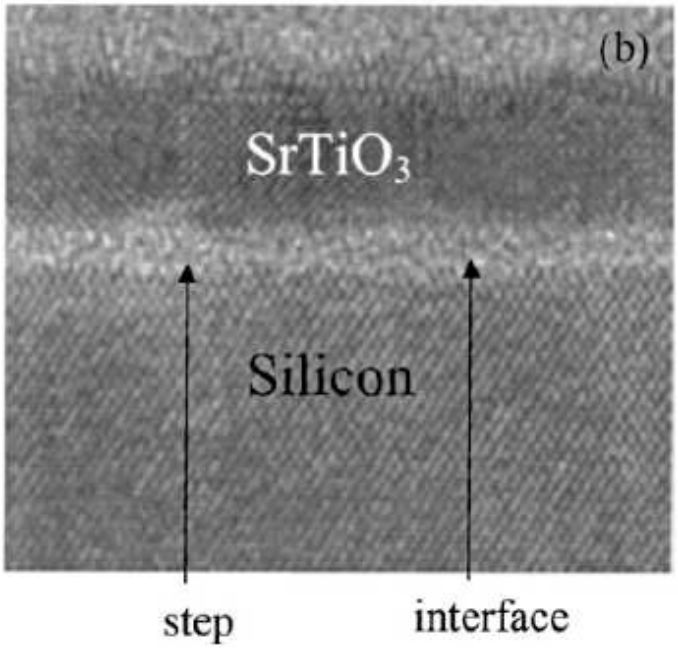

Figure 1.5: Cross sectional TEM image of a $SrTiO_3$/Si interface, sample and image by X. Hu, et. al.[32]

amorphous interfacial layer observed. These recent advances are encouraging for the integration of functional oxides with elemental and III-V semiconductors. However, reproducing results between different laboratories and different growth equpiment has been a major challenge. In addition, these methods cannot be expanded to growing thin films of semiconductors on ferroelectrics. So far, there is no successful method for growing Si, GaAs or GaN on a ferroelectric oxide, even though this ability is required for many devices and for superlattice structures.

Ferroelectric/semiconductor heterostructures are desired for several applications, among which memory devices are a leading example. Currently available FeRAM devices hold a significant market share especially in smart cards, metrology tools, and video games. However, their continued success depends on overcoming three problems from which they suffer: Fatigue, imprint, and limited endurance. The latter two are directly addressed with ferroelectric/semiconductor integration. Imprint, which refers

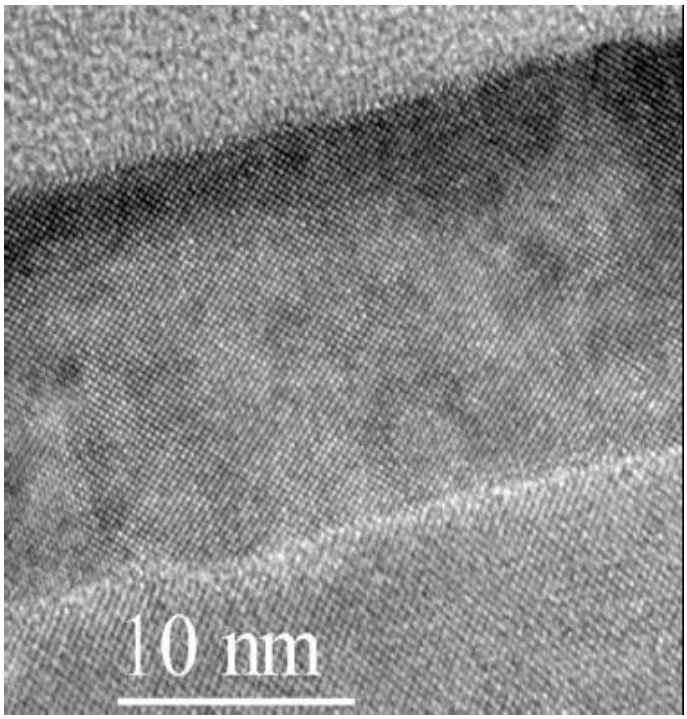

Figure 1.6: Cross sectional TEM image of a $BaTiO_3$/Si interface, sample and image by Y. Liang, et al. [35]

to a ferroelectric film gradually deteriorating to prefer one polarization direction, is thought to be caused or worsened by charge injection into the ferroelectric film [36]. Endurance of FeRAM devices can be improved by a non-destructive readout scheme, through which each cell would be read and written many fewer times than currently done by destructive readout followed by re-writing. Currently available devices use destructive readout schemes, which worsen the endurance problem by doubling the operations each cell has to undergo per use[37]. A non-destructive readout is possible through integration of the storage and addressing functionalities of the memory cell into a single device.

The need for separate devices for a storage capacitor and an addressing transistor in each memory cell comes from the difficulties in integrating the ferroelectric material with the semiconductor channel of the addressing transistor. Advances and challenges

in growing and depositing ferroelectrics on traditional semiconductors are summarized in Chapter III. Ferroelectric/semiconductor integration can play a significant role in increasing memory densities without a need to use 3-dimensional designs, by enabling the functions of storage, switching, and addressing to be performed by a single device.

A ferroelectric field effect transistor (FeFET) is a FET that uses a ferroelectric material as the gate dielectric. This device has been the subject of significant research activity, since it is expected to address both the density and the endurance issues related to memory devices. An FeFET-based memory device will automatically have a non-destructive readout mechanism, and will therefore effect less degradation on the ferroelectric film in terms of fatigue and imprint. Endurance of the memory cell is thus improved. Various geometries involving buffer layers[38],[8], and metal-ferroelectric-metal-insulator stacks for gate dielectrics have been proposed. Bistable memory behavior with PZT on Si has been reported [38] using Al_2O_3 as a buffer layer. Even though advances are being made, the performance of single transistor memory cells are not yet competitive with the one capacitor one transistor architechture due to poor ferroelectric-semiconductor interface characteristics.

The interface between the ferroelectric and the semiconductor has so far been the inhibiting factor in the performance of FeFETs. There are two main problems with FeFETS: charge injection at the ferroelectric/semiconductor interface, and chemical degradation at the interface. Charge injection at the interface is due to defects and low energy barriers to injection when ferroelectrics are interfaced with traditional semiconductors at the interface. Chemical degradation of the ferroelectric/semiconductor interface is caused by oxygen diffusion into the semiconductor from the oxide ferroelectric. In the case of silicon, a thin silicate is thus created at the interface, decoupling the gate from the channel. Similar low dielectric constant "dead layers" from with

GaAs, as well. For full and stable integration of ferroelectrics with semiconductors, a semiconductor that is chemically compatible with ferroelectric oxides is required. ZnO is an excellent candidate for such integration, since it is not expected to suffer from interfacial oxidation (forming an interfacial dead layer). ZnO further provides a favorable band line-up with many ferroelectric materials such as PZT and BTO, whereby there is a large ($\sim$1eV) energy barrier to electron leakage. In addition, thin films of ZnO can be deposited or grown on other oxides; therefore, there is a path to supperlattice structures to complete integration.

Memory devices are only one example among many possibilities that will follow from the ability to modulate a semiconductor using the ferroelectric polarization of a ferroelectric material. Stable ferroelectric/semiconductor heterostructures with low defect density interfaces will enable an array of new or improved electronic and optoelectronic designs such as:

- Temperature and pressure sensors with high sensitivity and short response times: A large polarization charge is induced into the semiconductor when an optimized ferroelectric thin film is grown on ZnO. Large changes in the ZnO conductivity are expected near the ferroelectric/semiconductor interface.

- Improved field effect transistors with ferroelectric gate dielectrics: Thick and robust gate stacks can be built without sacrificing gate modulation.

- Electronics cooling systems: Cooling techniques using the electrocaloric effect in many ferroelectric materials is currently under investigation[15].

- Highly integrated tunable capacitors, phase shifters, and modulators for radio frequency circuits: This application uses the DC tunable dielectric constant of ferroelectric materials in their paraelectric phase.

- Highly integrated transducers and actuators for MEMS applications: The piezoelectric or pyroelectric properties of the functional oxides are exploited for MEMS components such as membranes and cantilevers.

1.4 Investigating Students' Learning of Semiconductor Device Fundamentals

Continuity of research and innovation in the field of semiconductor devices requires that we recruit and educate talented students into advanced study of the materials and the underlying physics. However, many students find semiconductor physics intimidating and unattractive after taking an introductory course. There are many cases where students have a preconceived notion that the course will be an esoteric study in topics disconnected to the rest of the electrical engineering curriculum. There are multiple benefits to motivating students to learn more about semiconductors, and to teach the fundamentals very well. Therefore, we investigate alternative methods for teaching a first course in semiconductor devices. We propose inquiry based teaching and learning as a candidate method for effectively teaching semiconductor device fundamentals while stirring the students' curiousity to motivate them to enroll in follow-up courses and to participate in research projects. The hypothesis we evaluated was:

> Does inquiry based learning improve student interest, condence, and performance in an introductory semiconductors course and similar courses based on abstract or unfamiliar foundations?

Inquiry based learning is a technique where learning starts by asking questions and guessing answers based on previous experience[39]. We implemented this method in EECS 320 in the Winter 2009 semester. We chose three topics to teach using inquiry based learning, rather than applying the new method to the entire course.

We assessed the effectiveness of the inquiry based approach through surveys and focus group interviews conducted throughout the semester. Our results showed that students had a high level of interest and motivation at the end of the course, and that many of them were considering further study of semiconductor devices.

1.5 Overview

The remainder of this thesis discusses modeling of ferroelectric/semiconductor heterostructures, ferroelectric and zinc oxide thin film growth, fabrication and characterization. Conclusions are drawn from the comparison of the models and experimental results, which lead to suggestions for future work. Chapter II outlines a model for explaining the electrical behavior of ferroelectric/semiconductor heterostructures. The model is kept general in order to allow application of it to material systems not covered in this project. A charge control model is used, and hysteresis in capacitance-voltage behavior of heterostructures is predicted.

Chapter III details growth and deposition techniques we used to obtain ferroelectric thin films. Structural and electrical properties are explained through x-ray diffraction scans, and capacitance-voltage, and polarization-electric field measurements.

Chapter IV provides growth and deposition information on semiconducting zinc oxide, complete with structural and typical electrical data. The connection between the structural and electrical properties of zinc oxide thin films are observed for polycrystalline films on ferroelectric materials. The growth of non-polar m-plane zinc oxide is investigated through molecular beam epitaxy and transmission electron microscopy.

Chapter V discusses the electrical properties of $Pb(Zr,Ti)O_3$/ZnO heterostructures, where the capacitance-voltage measurements, as well as the AC conductance mea-

surements showed hysteretic behavior. The observed behavior was as expected from our modeling. Therefore, we have a first proof of concept that we can modulate a semiconductor using a ferroelectric material. Chapter VI further tests our hypotheses by showing the electrical characteristics of $LiNbO_3$/ZnO heterostructures. The carrier concentration in the semiconductor film is used as an indicator of modulation observed in $LiNbO_3$/ZnO heterostructures.

Chapter VII details a study in effectively teaching semiconductor physics in an introductory course. Inquiry based learning methods are applied to EECS 320 to investigate the benefits to the students. The technique, the course, the methodology, and the results are discussed. Many benefits, especially towards increasing students' interest and motivation towards semiconductor device physics are observed.

Chapter VIII summarizes the work and the results, as well as listing ideas for directions in which the project can progress. Fig. 1.7 depicts the flow of this thesis:

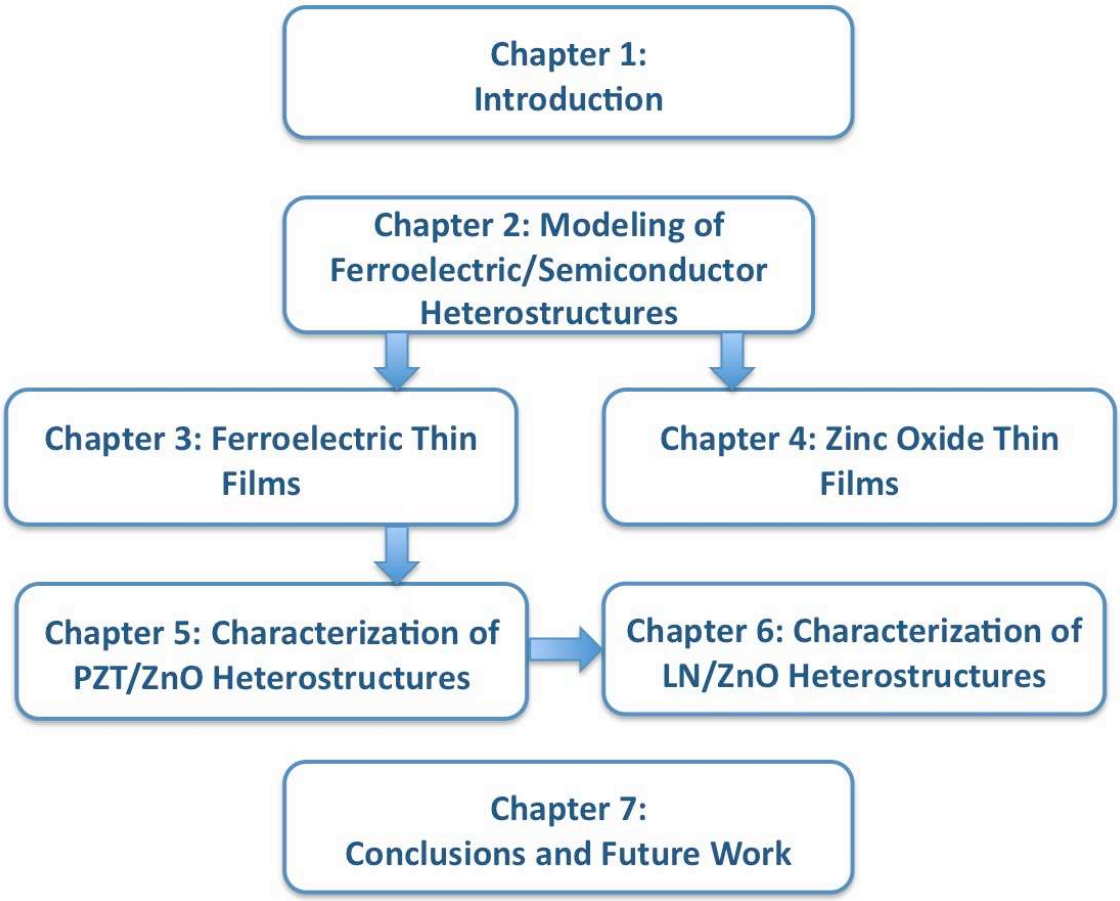

Figure 1.7: Flow of this thesis document

CHAPTER II

Modeling of Ferroelectric/Semiconductor Heterostructures

In this chapter we present a model to describe the switchable polarization charge in a ferroelectric material. We then further use the polarization charge description in a model to examine ferroelectric/semiconductor interfaces. The purpose of using a theoretical model to describe ferroelectric materials and ferroelectric/semiconductor heterostructures is to predict the electrical behavior of such heterostructures, and to explain deviations from the expected behavior. The model calculates the band diagram of a ferroelectric/semiconductor heterostructure starting with the band bending induced in the semiconductor layer. Full band diagrams can be drawn in cases where the band line ups are known.

2.1 Ferroelectric Polarization

Ferroelectric materials exhibit a nonzero polarization charge even after an applied electric field is removed. This polarization charge can be reversed by applying a large electric field in the direction opposite to the previous applied electric field. The behavior of the ferroelectric polarization is therefore dependent on both the applied

electric field and the history of the material. The polarization charge can be caused by two different phenomena, depending on the material under study[5]. Order-disorder phenomenon is applicable when the polarization is a result of dipoles in the material aligning in the same direction to cause a nonzero net polarization charge. Fig. 2.1 shows a schematic representation of order-disorder polarization. Displacive polarization phenomenon is applicable when a sublattice in the crystal shifts in relation to the rest of the crystal, thereby creating a nonzero net polarization charge. Fig. 2.2 shows a unit cell of a perovskite crystal with polarization, where the shifted sublattice is represented by the center atom. Displacive polarization is the relevant polarization mechanism for all ferroelectric materials studied in this project.

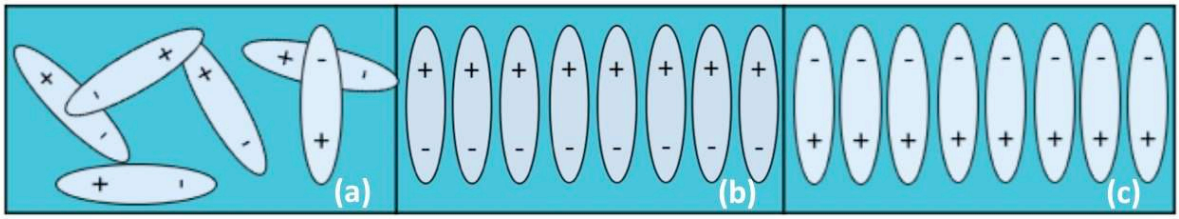

Figure 2.1: Schematic of a ferroelectric material where order-disorder polarization is observed. Crystal is shown with (a)no net polarization, (b)positive net polarization, (c)negative net polarization.

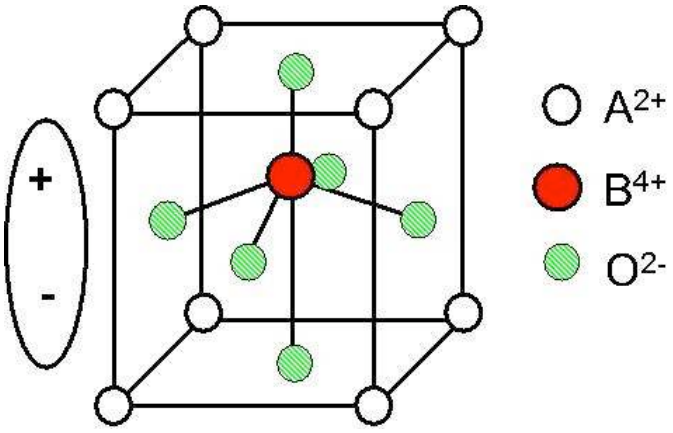

Figure 2.2: Schematic of a perovskite crystal unit cell showing displacive polarization

Ferroelectric polarization charge density follows a hyperbolic tangent relationship to applied electric field until saturation. It can be written as follows when the electric field is sweeped from a negative value to a positive value:

$$P^{+}(E) = P_s \tanh(\frac{E - E_c}{2\sigma})$$

where

$$\sigma = E_c[ln(\frac{1 + P_r/P_s}{1 - P_r/P_s})^{-1}]$$

Here P_s is spontaneous polarization, E_c is the coercive field (at which the sign of the polarization charge switches), and P_r is the remnant polarization. In the reverse sweep direction, with electric field going from a positive value to a negative value, the polarization charge is:

$$P^{-}(E) = P_s(-E)$$

The ferroelectric hysteresis curve is therefore predicted to have the shape shown in Fig. 2.3. The saturation and remnant polarization values, and the coercive field are observed in the figure.

Many ferroelectric materials exhibit DC-tunable dielectric constants, and they are therefore conducive to observing the effects of polarization on the capacitance-voltage behavior of the material. The capacitance value varies with the dielectric constant, creating a bell shaped curve. The voltage where the dielectric constant peaks depends on the direction of the ferroelectric charge, and therefore on the history of the electric field applied on the material. A typical C-V curve of a ferroelectric material therefore produces a butterfly shape symmetric around zero electric field, as shown in Fig. 2.4.

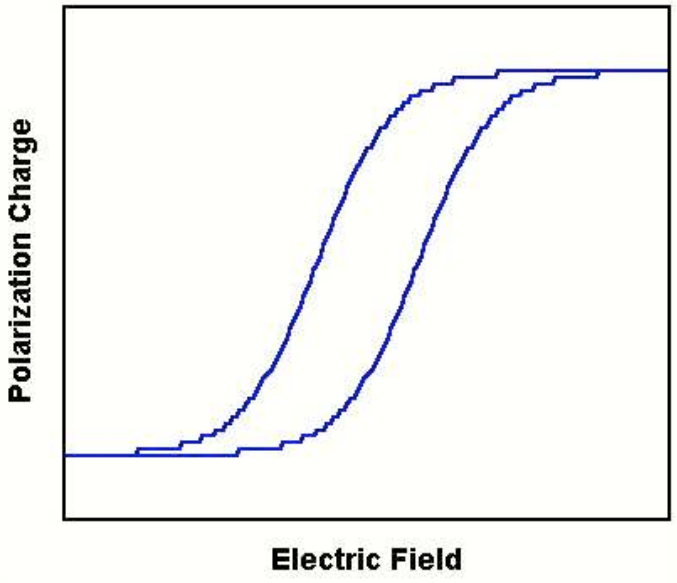

Figure 2.3: Polarization hysteresis behavior of a ferroelectric material

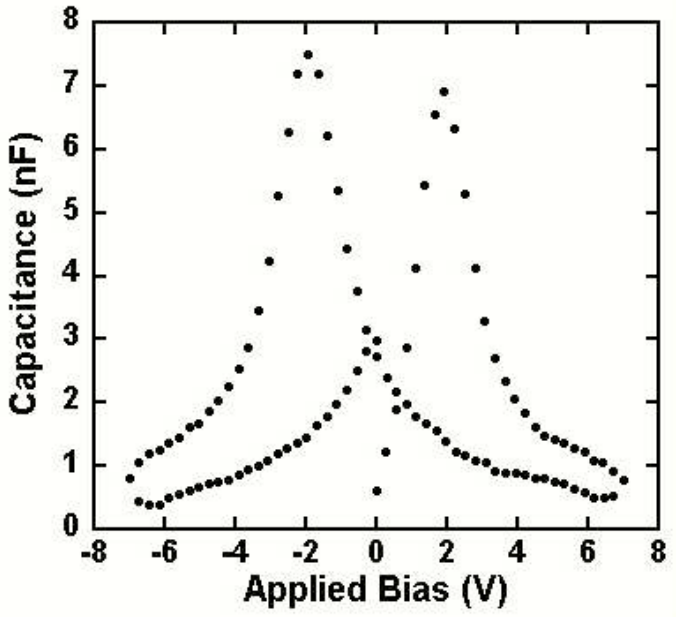

Figure 2.4: Typical capacitance-voltage behavior of a ferroelectric material

2.2 Ferroelectric/Semiconductor Heterostructures

It is important to have a model ferroelectric/semiconductor heterostructures, through which we can understand and predict the electrical behavior of the heterostructures. The goal of building ferroelectric/semiconductor heterostructures is

primarily to modulate the semiconductor using the ferroelectric polarization charge. Calculating band diagrams to explain the modulation is useful in understanding the expected and observed effects on the conductivity of the semiconductor. In constructing our model we focused on the interface of the ferroelectric material with the semiconductor, because the polarization charge and the relevant band bending will both occur at the junction. We started with a charge control model that is detailed by several other researchers[5][40][41]. The model starts with the relationship between the ferroelectric polarization charge density, P_f, electric field across the ferroelectric film, E_f, the dielectric constant of the ferroelectric film, ϵ_f, the electric field across the semiconductor film, E_s, and the dielectric constant of the semiconductor film, ϵ_s. This relationship is the boundary condition for subsequent calculations defining the ferroelectric/semiconductor junction.

$$\epsilon_f E_f + P_f = \epsilon_2 E_2$$

A charge neutrality equation now follows, including the doping in the semiconductor, the free carrier concentrations, and the polarization charge. Since the charge in which we are interested is only in the direction perpendicular to the ferroelectric/semiconductor interface, we can use Poisson's equation in one dimension to obtain the energy band profile for the heterostructure. We use Gummel's iterative method to solve the equation, and we produce band diagrams for varying magnitudes and directions of polarization charge densities as a result.

$$\rho(z) = q(N_d(z) - N_a(z) + p_{free} - n_{free} + P_s)$$
$$\frac{d^2}{dz^2}E(z) = -\frac{\rho(z)}{\epsilon(z)}$$

Fig. 2.5 shows the calculated band bending in the semiconductor with respect to the

direction of the ferroelectric polarization charge. The accumulation and depletion labels assume an n-type semicondunductor, since we worked with n-type ZnO as our prototype semiconductor in this project. A more complete band diagram including the ferroelectric material is presented for the specific case of $Pb(Zr,Ti)O_3$/ZnO heterostructures in Chapter V. We must note that efforts towards accurately determining the band offsets in such heterostructures is ongoing, as a result of which full band diagrams will be possible to draw.

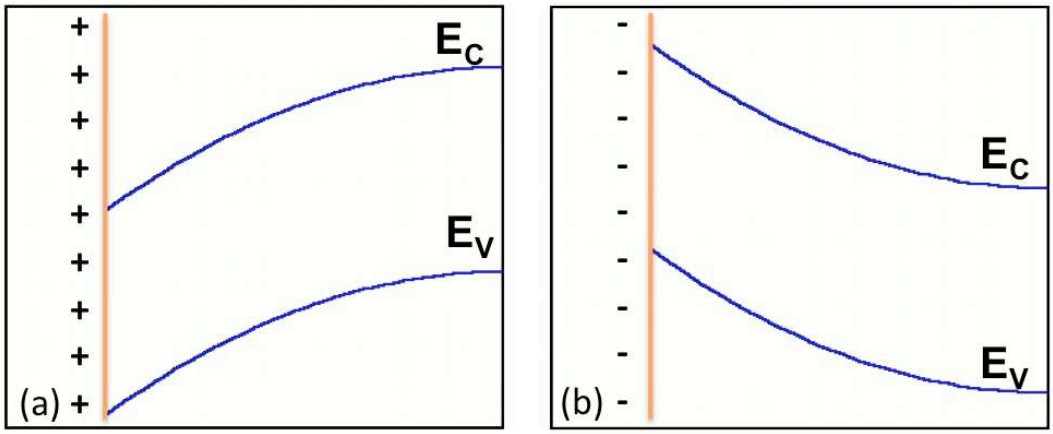

Figure 2.5: Band bending in the semiconductor in (a)accumulation and (b)depletion induced by ferroelectric polarization

The capacitance-voltage (C-V) behavior of ferroelectric-semiconductor heterostructures is a further tool through which to understand the interface quality. We simulated metal-ferroelectric-semiconductor (MFS) capacitors using the software package Medici in order to study relevant heterostructures, and compare their behavior to metal-insulator-semiconductor (MIS) and metal-ferroelectric-metal (MFM) stacks. We took the DC tunable dielectric constant of the ferroelectric thin film into account, and superposed it with the effects of band bending in the semiconductor on the observed capacitance. Since we focused on n-type ZnO, we did not simulate the case in which the semiconductor is in inversion: The lifetime of p-type minority carri-

ers is very low, inhibiting the onset of inversion. Fig. 2.6 shows the simulated C-V behavior of an MFS heterostructure with the DC tunable dielectric constant taken into account. Fig. 2.7 shows the simulated C-V characteristic with hysteresis due to ferroelectric polarization inducing band bending in the semiconductor. We observe varying threshold voltages depending on the direction and history of the applied bias. If the ferroelectric material is already poled in the positive direction, then accumulation in the semiconductor occurs more easily. Similarly, if the ferroelectric material is already poled in the negative direction, then depletion in the semiconductor occurs more easily. The amount of polarization charge that is effectively induced into the semiconductor determines the value by which the threshold voltage will shift.

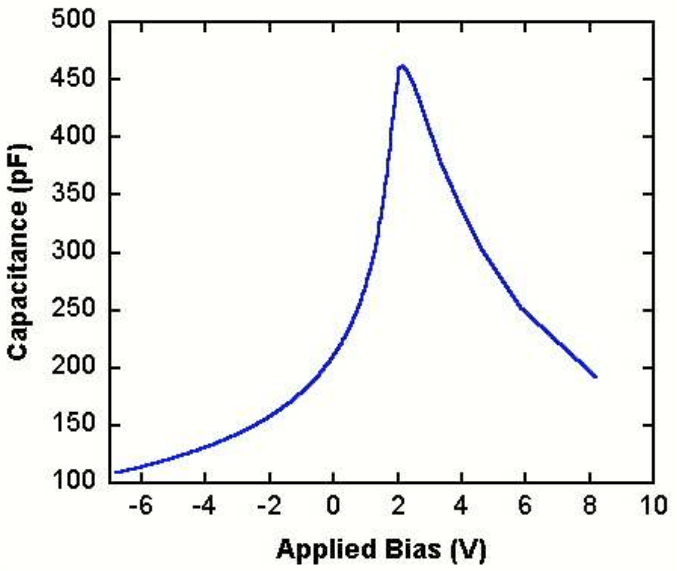

Figure 2.6: C-V behavior of an MFS structure considering the DC tunable dielectric constant of the ferroelectric material

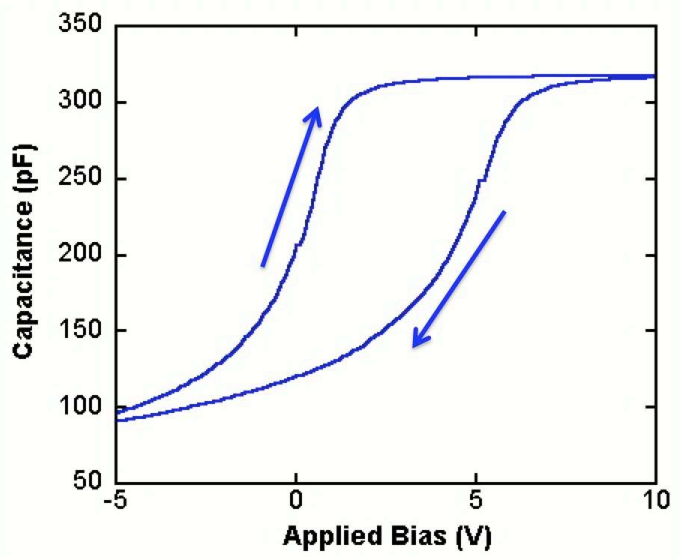

Figure 2.7: Hysteretic CV behavior of an MFS capacitor

CHAPTER III

Ferroelectric Materials

Ferroelectric materials are a subset of polar materials where the polarization charge is switchable by an external electric field as opposed to polar crystals in the Wurtzite form (with fixed spontaneous polarization values). Additionally, the polarization charge remains observed in ferroelectric materials even after the external electric field is removed. As outlined in Chapter I, these two properties are characterized by the metrics spontaneous polarization (P_s) and remnant polarization (P_r) respectively. All ferroelectric materials are also piezoelectric and pyroelectric. Electrooptic and electrocaloric effects are readily observed in many ferroelectrics. Therefore, these multifunctional materials attract a considerable research interest and effort. A large number of research groups are working on manipulating ferroelectric materials, and on integrating such materials with semiconductors in order to widen their applications. In this project, ferroelectric materials are of interest primarily for the ferroelectric polarization charge, through which we strive to modulate conductivity of semiconductor thin films.

3.1 Ferroelectric Thin Films

Many well studied ferroelectric oxides have the ABO_3 composition, and they crystallize in the perovskite structure. $BaTiO_3$ (BTO), (Ba, Sr)TiO_3 (BST), Pb(Zr,Ti)O_3 (PZT), and $BiFeO_3$ are examples of perovskite ferroelectric oxides. Therefore, developing the ability to grow ZnO on perovskite structures, and vice versa is an important step towards integrating ferroelectrics with ZnO. Two main mechanisms can lead to ferroelectric polarization: Ordering of all dipole moments in the same direction (order-disorder polarization); and the displacement of ions within crystals causing a permanent dipole moment (displacive polarization)[5]. All ferroelectric materials in this study show displacive polarization. The perovskite structure is shown in its unpolarized and polarized states in Fig. 3.1 and in Fig. 3.2 respectively. The B^{4+} ion has moved upward, leaving behind negative charge in its previous location. Downward displacement of the B^{4+} ion causes the opposite direction polarization. The polarization charge results, because the displacement causes an electric field that acts faster than the elastic restoring force of the crystal[42].

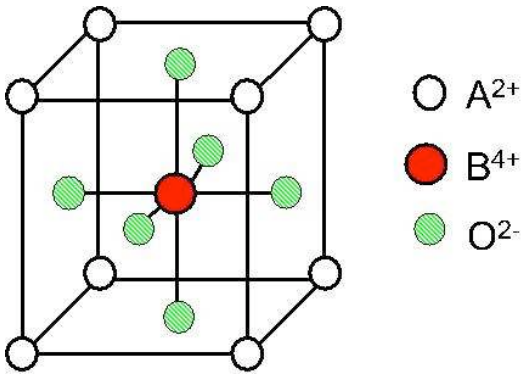

Figure 3.1: The perovskite unit cell in its unpolarized state

There are multiple metrics of ferroelectric materials we must consider when choosing a suitable material for each application. Clear hysteretic behavior as shown in Figure 1.1 is desired for memory applications, where it is detrimental to applications that

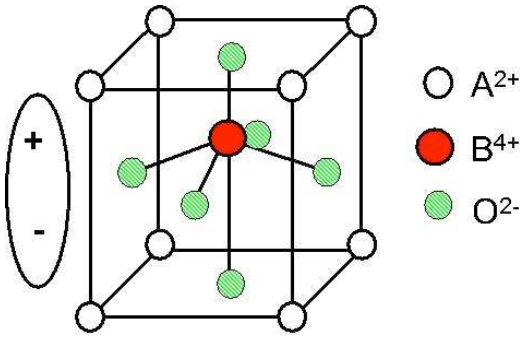

Figure 3.2: Displacive polarization in the perovskite unit cell

take advantage of the material's dielectric tunability. Large spontaneous and remnant polarization are generally desirable for electronics applications. A large pyroelectric constant is advantageous for temperature sensing and cooling applications, and a nuisance for electronics and optoelectronics applications. In this study we are trying to modulate the conductivity of a semiconductor using the polarization charge of a ferroelectric material; therefore, we look for large P_s and P_r. PZT has been a popular material choice for research and commercial applications similar to this project due to the high polarization values it offers. Another important material property to keep in mind is the Curie temperature, T_C, above which the material does not exhibit ferroelectric behavior. T_C marks the phase transition point for the material, and it is therefore carefully noted for applications benefiting from piezoelectric, pyroelectric and electrocaloric effects(these effects are strongest at temperatures near phase transitions). For electronics applications, one usually only needs to ensure that the operation temperature is well below T_C. The following table lists typical Curie temperature and the spontaneous polarization values for relevant ferroelectric materials.

The rest of this chapter provides details of three thin film deposition/growth techniques we used in this study. Pulsed laser deposition (PLD) is a straightforward technique that most often yields polycrystalline thin films. Sol-gel processing offers the

Material	T_C (K)	P_s ($\mu C/cm^2$)
$Pb(Zr,Ti)O_3$	515	>30
$BaTiO_3$	393	26
$LiNbO_3$	1150-1250	300
$PbTiO_3$	763	>50

Table 3.1: Key parameters for ferroelectric materials relevant to this project

ability to transfer complex oxides from nanocrystals to polycrystalline form. Molecular beam epitaxy (MBE) yield high quality single crystal epitaxial films through stringent control of the growth conditions. Structural properties of the resulting thin films from each method are studied and presented using x-ray diffraction. Electrical properties of select films where ferroelectric behavior was observed are presented through capacitance vs. voltage and polarization vs. electric field measurements. Finally, structural and pyroelectric properties of bulk $LiNbO_3$ substrates are summarized using x-ray diffraction and temperature vs. voltage measurements.

3.1.1 Pulsed Laser Deposition

Pulsed laser deposition (PLD) is a material deposition technique that offers many advantages for researching emerging material systems. The method is straightforward in that the required vacuum levels and temperature ranges are moderate. A typical deposition we used in this project required that we pump the deposition chamber down to 1x10^{-6}Torr base pressure and we heat the substrate to 600°C. The user has control over key deposition parameters such as oxygen partial pressure, temperature, laser pulse energy and laser pulse frequency. In addition, the available target materials are limited only by the ability to synthesize or purchase high purity powders of desired materials. Resulting film stochiometry is ideally directly controlled by the target composition; therefore, once the target material is availble repeatable deposition of even complex oxides is possible. Fig. 3.3 shows results of a Raman backscattering

study done on a (Ba,Sr)TiO_3 thin film deposited using PLD(courtesy of Xinen Zhu). The data show that the stochiometry of the thin film follows that of the target closely.

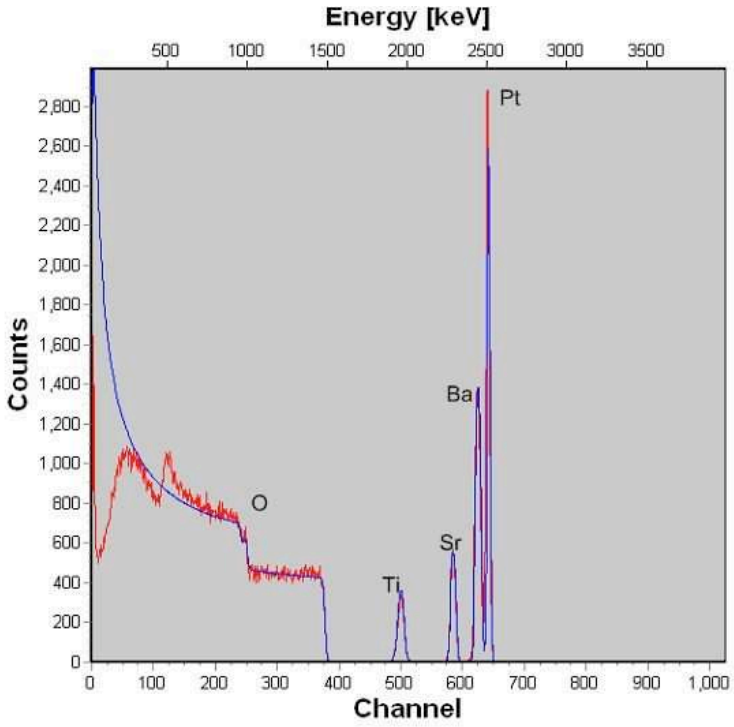

Figure 3.3: Raman backscattering data for BST deposited by PLD, courtesy of Xinen Zhu

The deposition chamber for the PLD system we used for this project is pumped down to high vacuum using a turbo pump backed by a mechanical pump. The substrate is fixed onto a heated chuck using silver paint, which provides high and uniform thermal conduction.The substrate chuck can be heated up to 950°C; however, all depositions discussed in this report were done between room temperature and 600°C. The highest temperature used in this project was 800°C, which was reserved for baking out the chamber during cleaning procedures between depositions. The target material is set on a rotating fixture, and it is placed directly in front of the substrate holder, 4-12cm apart. The laser beam is aligned and focused on to hit the target material, and the area of the spot where the laser beam hits the target is controlled and documented.

The pulsed beam energy and frequency are controlled via firmware controlled pre-programming of the excimer laser. The PLD system is shown in a schematic courtesy of Tim Murphy in Fig. 3.4. A photograph of the PLD system during a deposition is included in Fig. 3.5.

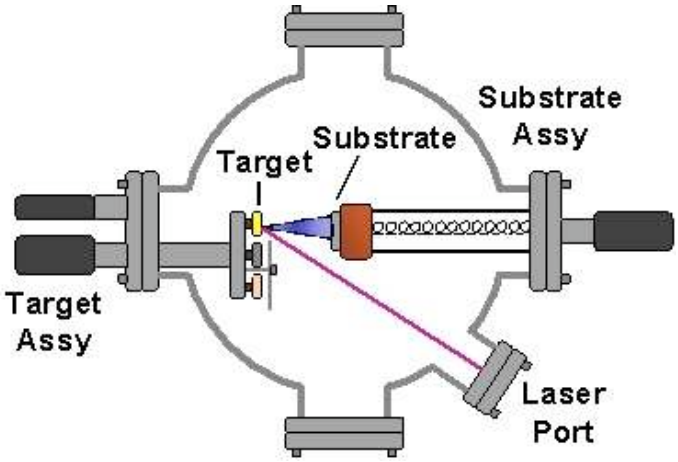

Figure 3.4: Schematic of the pulsed laser deposition system

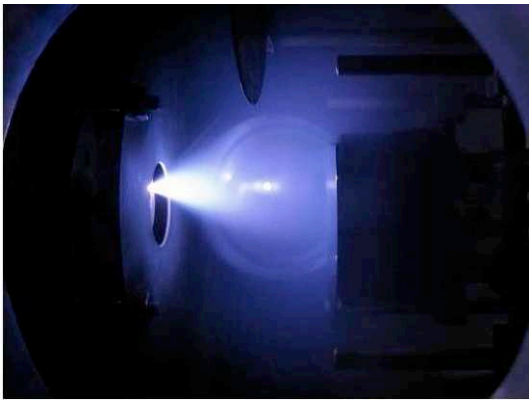

Figure 3.5: Pulsed laser deposition system during operation

The excimer laser used in the PLD system is a KrF laser that emits at a wavelength of 248nm. Typical deposition conditions call for 150-300mJ pulse energy and 6-10 pulses per second. The pulse duration is 25ns. When the laser beam hits the target material it energizes ions and particulates off the target, thereby forming a plume between the target and the substrate. At high vacuum the mean free path

of the energized ions and particulates is longer than the distance between the target and the substrate; so, the particules bombard the substrate to form a crystalline or polycrystalline film[43]. In Fig. 3.5 the plume is observed in the middle as the bright ellipse. The shape of the plume helps optimize deposition conditions; the plume should look as shown in Fig. 3.5. If the plume is too short (substrate is outside the plume), majority of the particles will not reach the substrate; therefore, the deposition rate will be very low. If the plume is too long (substrate is in the center of the ellipse), majority of the particles will bombard the substrate with very high energy, thereby forming a high density of defects in the film. The oxygen partial pressure in the chamber, the target-to-substrate distance and the laser energy density determine the energy of the ablated particles when they reach the substrate. The oxygen partial pressure is determined by controlled flow of oxygen into the chamber, with typical flow rates ranging between 10sccm and 20sccm. The target-to-substrate distance is set by positioning the substrate holder to the desired location. The laser energy density impinged on the target should depend only on the set laser pule energy, since the beam is focused on the target and the beam area recorded. The energy density, or fluence is calculated as follows, and typical fluence values range from 0.5J/cm^2 to 2J/cm^2.

$$Fluence(J/cm^2) = \frac{Laser\ energy(J)}{Beam\ area(cm^2)}$$

There are two main limitations to the PLD technique that are relevant to this project. Firstly, the excimer laser wavelength 248nm corresponds to a 5eV beam. We observed that materials with bandgaps larger than 5eV are challenging to deposit using PLD. The challenge arises from difficulty ionizing the target, since the material is transparent to the laser beam. Secondly, most thin films deposited through this technique will be polycrystalline, even if they are highly preferentially oriented in one direction. The grain boundaries in the film will act as paths for leakage currents in insulators,

Film	Substrate	Lattice mismatch	Annealing temperature
BTO	MgO	5.2% tensile	Not annealed[44]
BTO	p^+-Si	26% tensile	Not annealed
BTO	ZnO	22.8% compressive	Not annealed
PZT	Pt	1.8% compressive	800°
PZT	ZnO	23% compressive	800°

Table 3.2: Substrate and temperature treatment information for BTO and PZT films

while highly insulating behavior is desirable for ferroelectric films. Leakage current can overshadow ferroelectric polarization, and render it very difficult if not impossible to measure. Grain boundaries are also a hinderance to high mobility when thin films of semiconductors are deposited using the PLD technique. Therefore, when high quality single crystal films are necessary, it is beneficial to look for alternative techniques such as molecular beam epitaxy.

We started our study by depositing $BaTiO_3$ (BTO) and $Pb(Zr,Ti)O_3$ (PZT) using the PLD technique. We chose these two materials because they are well-studied, and they both exhibit high P_s and P_r values. When depositing thin films of ferroelectric materials we must keep in mind that ferroelectricity will be exhibited most strongly when the crystalline orientation of the film is correct. In the case of BTO and PZT the desired crystalline structure is the perovskite structure shown in Fig. 3.1. We experimented with substrate choice, deposition conditions and post-deposition annealing to achieve perovskite polycrystalline films of BTO and PZT. Our substrate choices were motivated by lattice matching (e.g.: for BTO on MgO), by convenience of subsequent electrical characterization (e.g.: PZT on Pt), and by our end goal (i.e.: ZnO). Table 3.2 summarizes relevant BTO and PZT thin films depositions carried out in our laboratory.

X-ray diffraction helped us characterize the structural properties of the thin films deposited in this series of samples. Wide range $\theta - 2\theta$ scans of BTO films show the

orientation of the films as well as giving us insight into the insulating and ferroelectric properties of the films. BTO films on MgO were highly preferentially oriented in the c-direction, as we observed by the strong (001) and (002) diffraction peaks at 2θ=22.0° and 2θ=44.9° respectively, as shown in Fig. 3.6. With such clear preferential orientation and strong diffraction peaks, we could expect that the film is highly insulating and ferroelectric. However, since MgO substrates are also highly insulating, characterization of these thin films was limited to structural properties. When we moved to degenerately doped p-type silicon substrates we were able to deposit polycrystalline BTO thin films with multiple crystalline orientations. A $\theta - 2\theta$ scan of a BTO film on p^+-Si is shown in Fig. 3.7, where the substrate peak is excluded in order to get a clear view of the BTO peaks. Unlike the BTO films on MgO substrates, those on Si showed much weaker diffraction peaks. BTO films on Si showed very high leakage currents, which dwarfed any other effects that could exist in the films. Grain boundaries in the polycrsytalline film can be an effective path for leakage current. The encouraging observation in these films was that all of the BTO diffraction peaks corresponded to perovskite peaks, showing us we are able to deposit the desired crystalline phase, even though the crystalline quality needs further optimization.

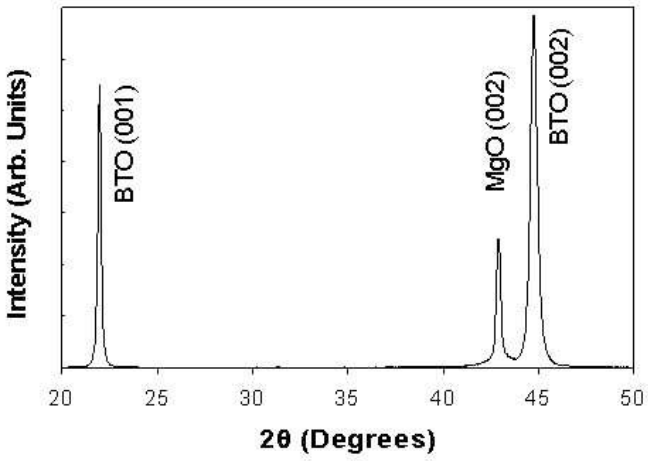

Figure 3.6: $\theta - 2\theta$ scan of a BTO thin film on bulk MgO

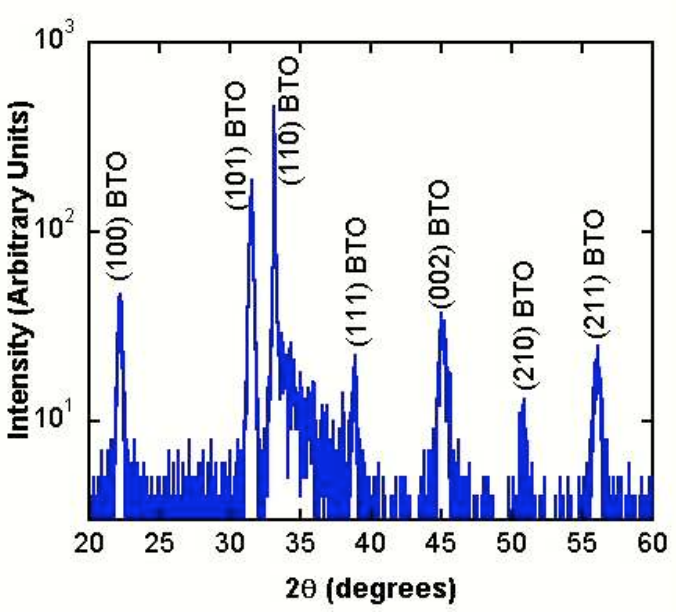

Figure 3.7: $\theta - 2\theta$ scan of a BTO thin film on bulk p^+-Si

As the last step in our study of BTO thin films using PLD, we deposited films on bulk ZnO substrates. The results are similar to those on p^+-Si substrates, with multiple diffraction peaks showing no preferential orientation. Fig. 3.8 shows a wide range $\theta - 2\theta$ scan of one such thin film. An additional challenge with depositing BTO on ZnO was the mismatch between the thermal expansion coefficients of BTO(9.8ppm/°) and ZnO(6.5ppm/°). We observed severe cracking upon cooling the films from deposition temperature to room temperature, even when the cooling was as slow as 0.5°C/min (typical cooling speed is 2.5°C/min). Cracking led to direct current paths through the thin film; therefore, the leakage current was too high for further electrical characterization. Once again, all of the diffraction peaks we observed belonged to the perovskite phase of BTO, which is encouraging in establishing an ability to deposit BTO and interface it with ZnO. However, stricter control over the orientation of the film is required. Growth of BTO with molecular beam epitaxy provides much increased control and quality, and it is discussed later in this chapter.

Deposition of PZT thin films using PLD was very challenging due to the large

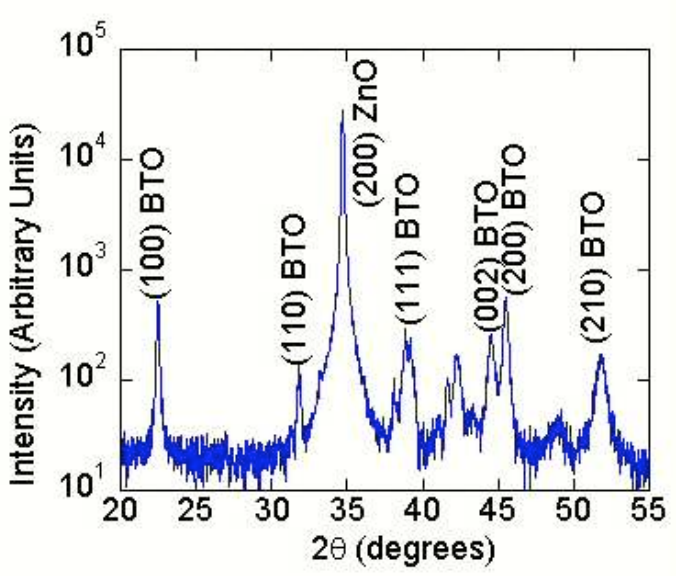

Figure 3.8: $\theta - 2\theta$ scan of a BTO thin film on bulk ZnO

bandgap of the material (3.7eV at room temperature). High laser energy, ranging between 400mJ and 500mJ, was necessary to ionize the PZT target, which made for conditions that were difficult to maintain and repeat. X-ray diffraction of the PZT thin films showed that polycrystalline films with no preferential orientations resulted from our best-case depositions. Fig. 3.9 and Fig. 3.10 show wide range $\theta - 2\theta$ scans of PZT thin films on Pt and ZnO substrates respectively. It is important to note that two relatively strong diffraction peaks observed in Fig. 3.9, at 2θ=29.2^{circ} and 2θ=32.8°, belong to the pyrochlore phase of PZT. PZT is not ferroelectric in the pyrochlore phase; therefore, these crystalline orientations are undesirable for our application. The (222) plane diffraction peak at 2θ=22.0° was also observed in the thin film on ZnO, where it was the strongest peak. PZT films on both kinds of substrates suffer from lack of control over the crstalline orientation, and lack of preferential orientation in the desired direction. The thin films were therefore not ferroelectric.

In order to promote recrystallization in the PZT thin films, we annealed them using a rapid thermal annealing (RTA) process. The process took the films from room

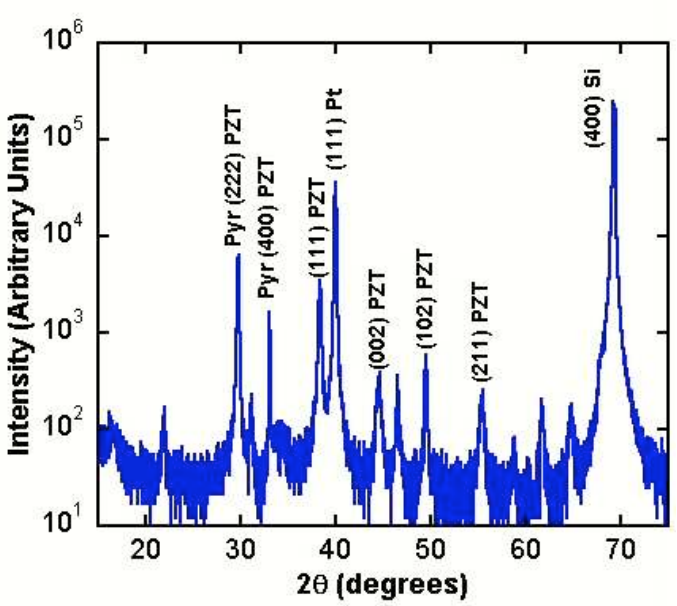

Figure 3.9: $\theta - 2\theta$ scan of an as-deposited PZT thin film on Pt

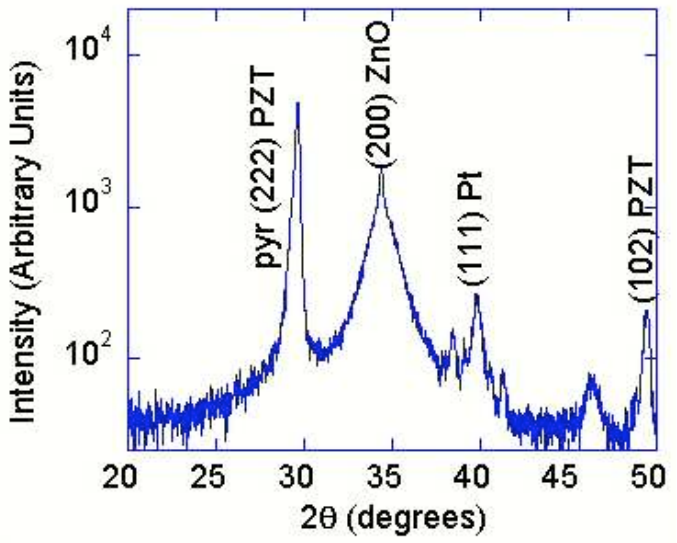

Figure 3.10: $\theta - 2\theta$ scan of an as-deposited PZT thin film on bulk ZnO

temperature to 800°C in 1min and remained at high temperature for 3mins. Fig. 3.11 and Fig. 3.12 show $\theta - 2\theta$ scans of the samples after annealing. We observe that in both films new perovskite peaks appeared, and previously observed perovskite peaks became stronger. The pyrochlore peaks were weaker in all of the films that we characterized. Therefore, we learned that a path to perovskite PZT on ZnO exists, even

though PLD is not the optimal way to deposit this material. We explored sol-gel processing of PZT in order to study this material further without the need for energizing the heavy ions in it. Details of that process are included in the following section.

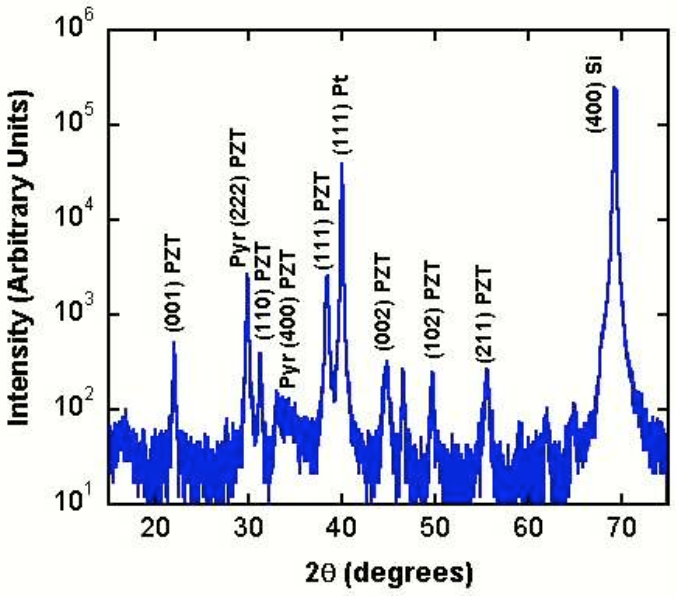

Figure 3.11: $\theta - 2\theta$ scan of an annealed PZT thin film on Pt

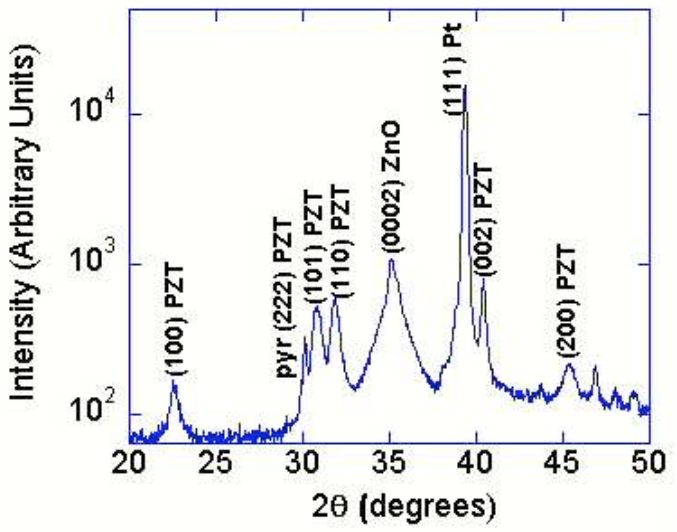

Figure 3.12: $\theta - 2\theta$ scan of an annealed PZT thin film on bulk ZnO

3.1.2 Sol-Gel Deposition

We deposited thin films of $Pb(Zr,Ti)O_3$ (PZT) using a solution based process starting from a suspension of nanocrystals. The processing steps are cleaning, spin coating, and high temperature annealing; therefore, we can incorporate sol-gel processing easily into standard fabrication laboratories. We deposited PZT thin films starting with a suspension of PZT nanocrystals purchased from Nippon FerroTechnology Corporation. We chose this particular solution because it provides nanocrystals of correct stochiometry that do no precipitate to the bottom. The thin films were deposited on platinum coated silicon substrates purchased from Radiant Technologies, Inc. The substrates were first cleaned through a solvent-clean sequence that consisted of acetone and isopropanol soaks followed by a deionized water quench. A rapid thermal annealing (RTA) step at 700°C in oxygen and nitrogen for 2 minutes was then carried out prior to film deposition. The annealing step increased the yield of our process, presumably by rendering the substrate surface more reactive. Films deposited on substrates without annealing peeled off from the surface during subsequent processing steps. The PZT nanocrystal suspension was then spin-coated at 3000rpm for 30 seconds. The samples were dry baked at 1150°C for 15 minutes, and annealed at 700°C for 2 minutes in oxygen and nitrogen through an RTA step. Repeating this process twice yielded ferroelectric films of thickness 400nm, as measured using a FilmMetrics reflectometer. Fig. 3.13 shows a flowchart of the sol-gel process, each iteration of which results in a 200nm-thick film.

We investigated the effects of the separate processing steps on the structural characteristics of the film by interrupting the process at each step, and carrying out an x-ray scan on the sample. Fig. 3.14 shows a $\theta - 2\theta$ scan of a PZT film immediately after spin coating. The x-ray scan looks identical to this figure after dry baking, as well. There is a single diffraction peak corresponding to PZT, at 2θ=46.7°, showing

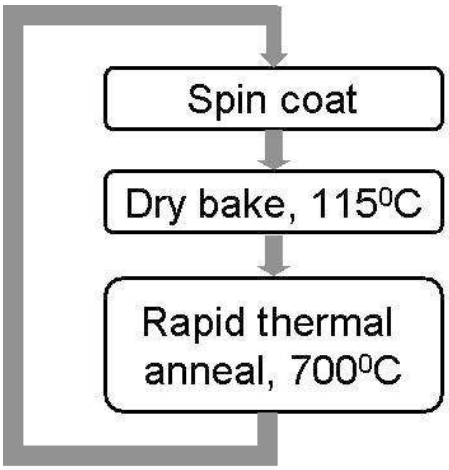

Figure 3.13: Process flowchart for sol-gel deposition of PZT

that this film is preferentially oriented along the [012] direction. The (012) peak tells us that PZT is crystallizing in the perovskite phase. However, the diffraction peak, thus the crystallinity, is quite weak at this stage in the processing. Consistent with this scan, no ferroelectric polarization was observed on the sample at this stage in polarization-electric field (P-E) measurements.

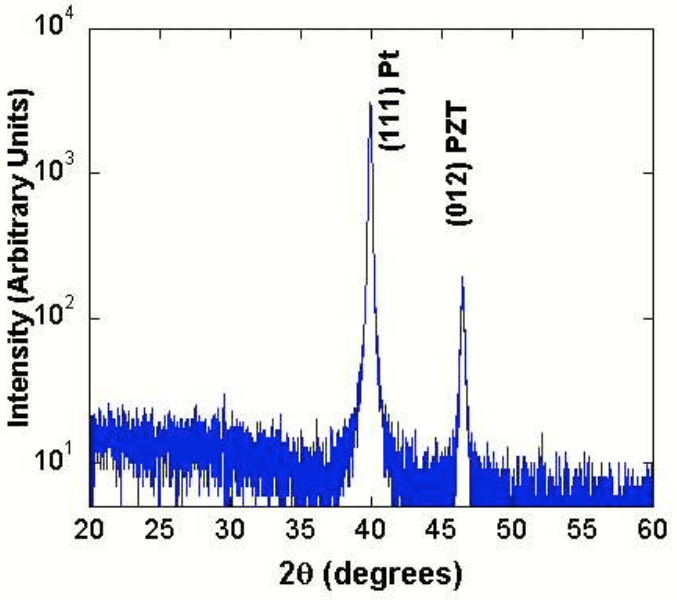

Figure 3.14: $\theta - 2\theta$ scan of of sol-gel processed PZT immediately upon spin coating

We repeated the $\theta - 2\theta$ scan after the RTA step at 700°C, as shown in Fig. 3.15. The film is now polycrystalline; several new diffraction peaks, all corresponding to the perovskite phase, have formed through the high temperature treatment. It is particularly encouraging to observe the (001) and (002) planes upon annealing, since these planes predict polarization in the direction of film deposition. Recrsytallization through the RTA is not surprising, because the RTA temperature is much higher than the previous bake temperatures. All samples that showed ferroelectric polarization were annealed at 700°C.

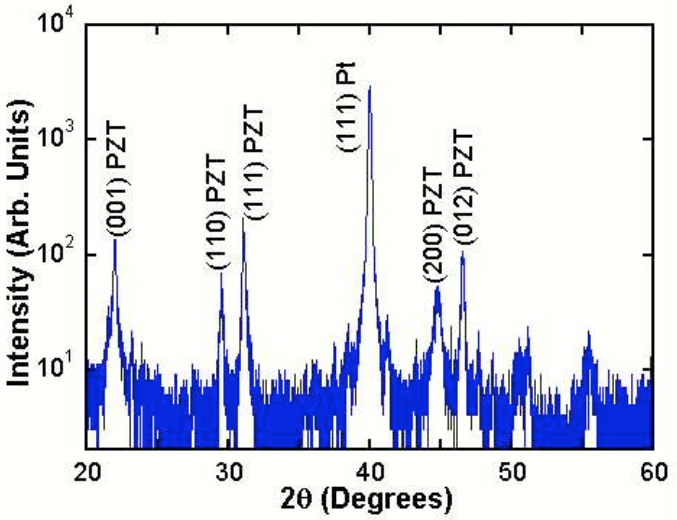

Figure 3.15: $\theta - 2\theta$ scan of of sol-gel processed PZT upon annealing

We evaluated the electrical properties of sol-gel deposited PZT thin films through metal- insulator-metal (MIM) capacitor devices. The Pt substrate acted as a blanket bottom electrode, and we used circular Pt top electrodes (r=115μm, A=4.1x10^{-4}cm^2) evaporated through a shadow mask to complete a symmetric 2-terminal MIM structure. We carried out polarization-electric field (P-E) and capacitance-voltage (C-V) measurements using a Radiant RT66A Ferroelectric Characterization System. PZT thin films deposited via sol-gel processing exhibited highly insulating behavior: The leakage current measured from the bottom to the top electrode in these devices ranged

between 10 and 30nA/cm^2. The films had favorable ferroelectric properties, as shown by the P-E results in Fig. 3.16. The Pt/PZT/Pt capacitors showed a remnant polarization, Pr, of 30μC/cm^2 and a coercive field of 60kV/cm corresponding to an applied bias of 2.5V. The P_r value is comparable to that of bulk PZT. The P-E behavior is symmetric around the polarization and the bias axes, signifying symmetric top- and bottom-electrodes. The P-E behavior maps to a memory window of slightly over 4V, which we study further in Chapter V.

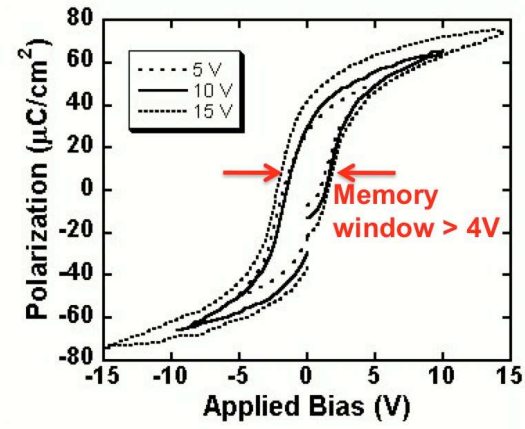

Figure 3.16: Polarization-electric field behavior of a sol-gel processed PZT thin film

Fig. 3.17 shows the capacitance-voltage (C-V) characteristics of the Pt/PZT/Pt capacitors, demonstrating the characteristic butterfly shape associated with ferroelectric thin films. This shape is a superposition of the DC tunable dielectric constant of PZT with the ferroelectric polarization. The tunability of the dielectric constant leads to the peaking in the capacitance values, and the ferroelectric polarization causes the peaking to occur at different applied biases depending on the direction of the bias sweep. (The bias sweep is done from 0V to +7V; +7V to 7V; then from 7V to 0V.) The electric-field dependent dielectric constant of the PZT film ranges from $\varepsilon_r = 82\varepsilon_0$ to $330\varepsilon_0$. The peak capacitance value occurs at an applied bias of $\pm$2.5 V, which corresponds directly to the coercive field, 60kV/cm.

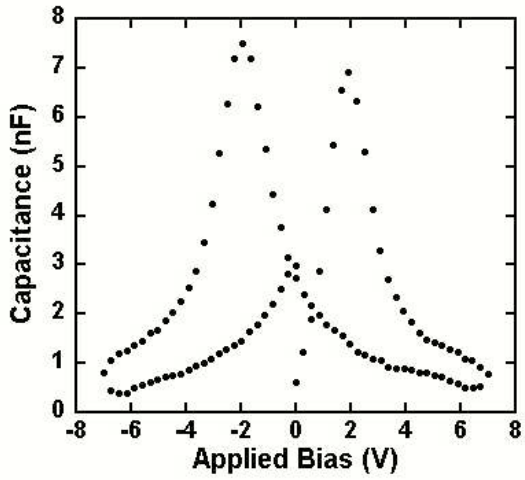

Figure 3.17: Capacitance-voltage behavior of a sol-gel processed PZT thin film

The electrical properties achieved through the sol-gel processing of PZT are very promising for integration with semiconductors. The high P_r value, and the readily observable hysteresis in the P-E and C-V measurements gives reason to expect clear coupling of the ferroelectric charge into the semiconductor. The next requirement is to deposit ZnO on top of these PZT thin films with high enough quality interfaces to couple the ferroelectric charge into the ZnO layer. We deposited ZnO on PZT thin films to fabricate and characterize metal-ferroelectric-semiconductor capacitors. The properties of PZT/ZnO capacitors are detailed in Chapter V. The reverse geometry for the structure, where PZT is deposited on top of ZnO is equally desirable, especially if we are to experiment with superlattices. However, the sol-gel films on bulk ZnO did not adhere to the substrate. The films peeled off upon RTA treatments. There is more process development necessary before the reverse geometry can be achieved. Our expectation that having purely perovskite crystalline films of PZT will lead to the observation of ferroelectric polarization, is confirmed by the observations that are summarized here and detailed in Chapter V.

3.1.3 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) yields high crystalline quality epitaxial thin films when the growth conditions are optimal. We used MBE with the goal of growing high quality $BaTiO_3$ (BTO) films, which we can subsequently interface with ZnO. A home built dedicated oxide MBE system, which belongs to Professor Ahn's group at Yale University, was used in the preparations of the samples in this study. Barium, strontium and titanium were provided through effusion cells, and oxygen was provided through a leak valve. An in-situ reflected high energy electron diffraction (RHEED) tool enabled the operator to monitor thin film crystalline structure in real time. The growth rate was observed using a quartz crystal monitor (QCM). Degenerately doped p-type silicon substrates were used with two benefits: The conducting substrates provided a bottom electrode for metal-ferroelectric-metal structures to follow, and we were able to explore growth of a perovskite oxide on silicon. A very thin layer (2 monolayers) of $SrTiO_3$ (STO) was grown directly on the silicon to provide a stable interface with silicon. STO has been used to provide a stable template for epitaxial oxide growth on silicon previously[45], including studying STO as a gate dielectric for silicon MOSFETs[46].

STO growth on silicon was done in multiple high and low temperature steps. Following desorption of the native oxide on silicon, 0.5 monolayer (ML) of Sr was grown at 600°C, creating a strontium silicide at the surface. This was followed by a low temperature (50°C) 0.5ML growth of Sr, then by growth of SrO. Oxygen flow was introduced when the substrate was at only 50°C in order to prevent oxidation of silicon, and further reaction of Sr and Si. A streaky 2x1 RHEED pattern was observed upon the growth of 0.5ML SrO. The streaky pattern disappeared upon growth of 2ML of STO at 50°C, since the low temperature growth was amorphous. The thin STO buffer layer crystallized upon heating to 600°C, and it produced a streaky 2x1

RHEED pattern again. The growth process of STO and the corresponding RHEED patterns are shown in Fig. 3.18. At the end of the 600°C step the interface of silicon and STO is stable, and we now have a surface that is conducive to epitaxial BTO growth.

Figure 3.18: RHEED patterns (a)upon growth of 0.5ML SrO at 50°C (b)upon growth of 2ML $SrTiO_3$ at 50°C (c)upon recrystallizing $SrTiO_3$ at 600°C

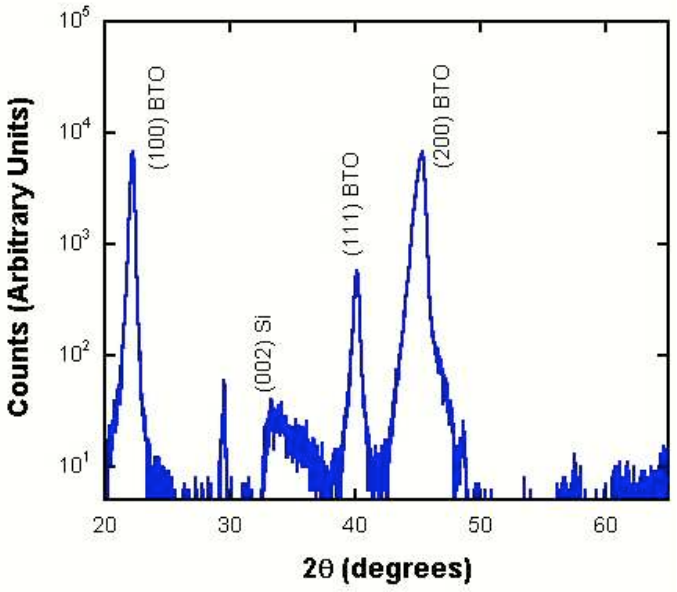

Figure 3.19: $\theta - 2\theta$ scan of BTO thin film as grown on p^+-Si

BTO growth was carried out at 600°C. The growth rate was 20 seconds per monolayer, which is equivalent to $\sim 12\mathring{A}$ per minute for BTO. Thickness measurements with a Dektak profilometer gave a range of 35-40nm for the thickness of this film. BTO crystallized in the perovskite phase, as evidenced by the $\theta - 2\theta$ x-ray diffraction scan in Fig. 3.19. The c-plane of BTO is expected to be parallel to the substrate in this

growth, putting ferroelectric polarization perpendicular to the direction of growth. Since the (001) and (100) diffraction peaks are at 2θ angles very close to each other, our scan is insufficient in confirming whether or not the (001) plane is indeed parallel to the substrate. We note the lack of secondary (002) diffraction peak in support of this expectation. Due to high leakage in the as-grown films, we could not measure P-E behavior. The resistivity of the film was 150Ω·cm, which we attribute to oxygen vacancies. In order to test this attribution, we carried out an oxygen anneal study on these films. The first rapid thermal anneal (RTA) treatment was done at 800°C in oxygen for 5minutes. The RTA yielded a film free of cracking or peeling. A 20X magnified optical microscope image is included in Fig. 3.20. The crystalline orientations on the film did not change significantly, except for a slight narrowing on the BTO peaks. A $\theta - 2\theta$ scan of the annealed film is shown in overlaid with a scan of the as-deposited film for comparison in Fig. 3.21.

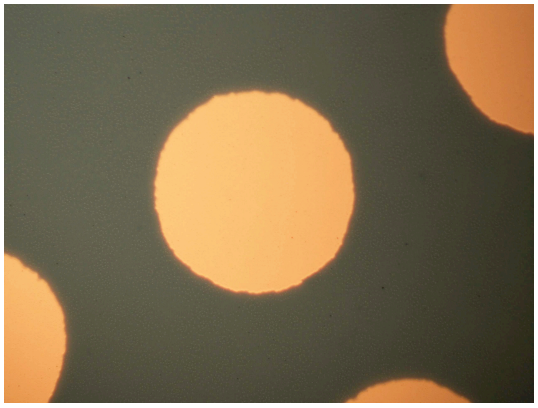

Figure 3.20: 20X magnified optical microscope image of BTO thin film annealed in oxygen

We carried out a second two-step anneal process as an alternative, where we first annealed the sample in forming gas (5% hydrogen, 95% inert gas) for 2minutes followed by oxygen for 3minutes, both at 800°C. The crystalline structure once again remained steady, as shown in the $\theta - 2\theta$ scan in Fig. 3.22. During the two-step anneal

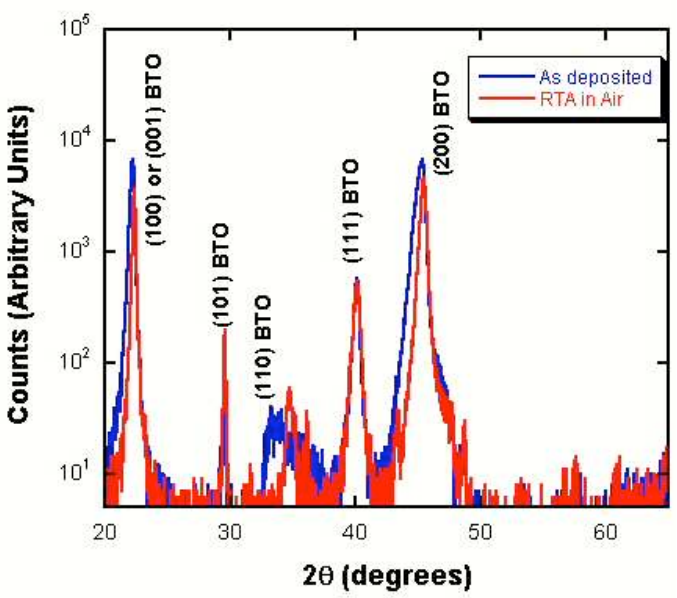

Figure 3.21: $\theta - 2\theta$ scan of BTO thin film annealed in oxygen

the sample was twice heated to 800°C and cooled back down to room temperature rapidly due to equipment limitations. This decreased the yield among these samples significantly. Areas on the samples showed peeling, though we did not observe any cracking. A 20X magnified image of the sample surface after two anneals is shown in Fig. 3.23.

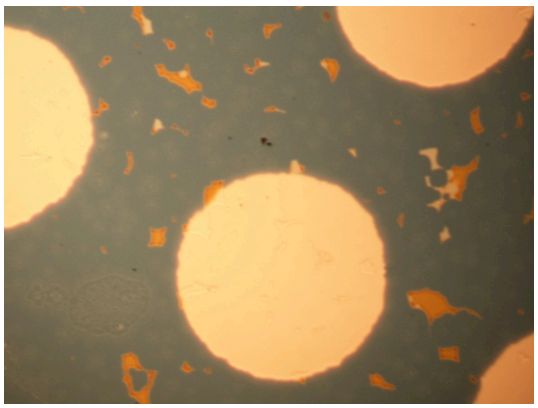

Figure 3.22: $\theta - 2\theta$ scan of BTO thin film annealed in forming gas and oxygen

The leakage current through the BTO films decreased dramatically after oxygen annealing with and without the forming gas pre-anneal step. The resistivity of the

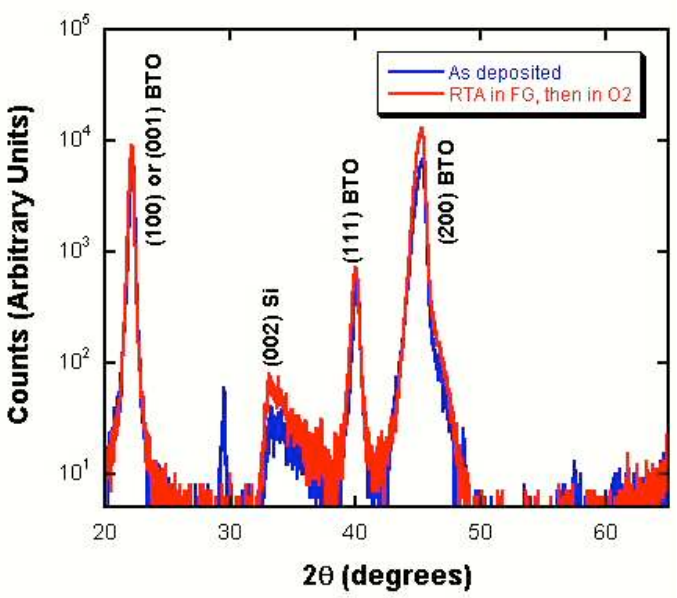

Figure 3.23: 20X magnified optical microscope image of BTO thin film annealed in forming gas and oxygen

samples increased to $10^9\Omega$·cm. We expect ferroelectric polarization on these films to be in-plane, because the substrate choice is made to promote the orientation (001)BTO‖(100)Si. Therefore, vertical metal-BTO-metal capacitors are not expected to show hysteresis in P-E measurements. P-E is still a valuable tool to evaluate the material; hysteresis observed in these films would indicate a high density of defects. Fig. 3.24 shows the P-E measurement results for both annealed samples, neither one of which shows hysteretic behavior. The dielectric constant of BTO thin films also increased with annealing. We observed a very low dielectric constant of ε_r=4ε_0 in the as-deposited films (likely due to high leakage). ε_r increased to 26.6ε_0 after the single step oxygen anneal, and 36.6ε_0 after the two-step forming gas and oxygen anneal. We believe that the hydrogen content of the forming gas causes the film surface to become more reactant, thereby facilitating oxygen incorporation into the film in the subsequent anneal.

We must note that all of the dielectric constant values we measured and reported are

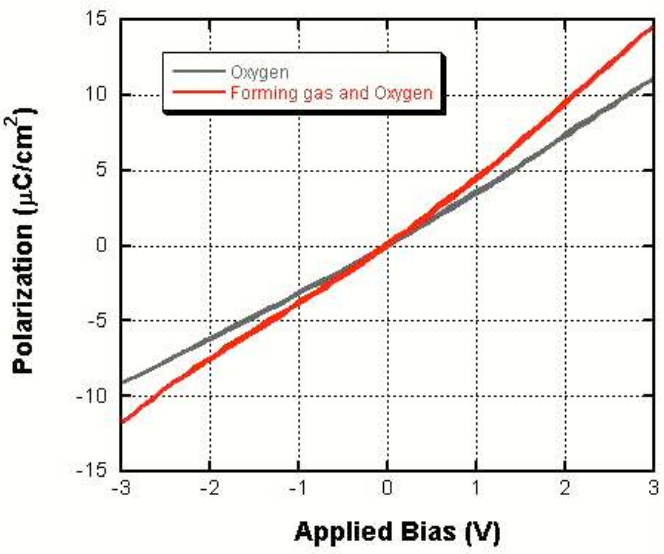

Figure 3.24: Polarization-electric field behavior of BTO films on p^+-Si

low compared to the near-bulk dielectric constant of BTO, measured in large-grain thick films. The near-bulk dielectric constant is reported to be $>100\varepsilon_0$[47]. In the as-grown samples high leakage current makes the measured capacitance artificially low due to equipment limitations. In the annealed samples the capacitance of the entire stack must be taken into consideration. A low dielectric constant silica layer of just a few nanometeres can cause the total capacitance to be low, thereby making the apparent dielectric constant of the stack lower than its actual value. The schematic in Fig. 3.25 summarizes this effect. This observation reinforces the need for a semiconductor with which we can integrate ferroelectric oxides. A fully integrated ferroelectric/semiconductor heterostructure will not suffer from an amorphous interfacial layer. Measuring the in-plane ferroelectric polarization can be achieved using lateral capacitors (parallel to the substrate), where we expect the capacitors will not suffer from the effects of a low dielectric constant silica layer. The true dielectric constant of the BTO layer free of the STO/SiO_x stack's effect can be measured using lateral capacitors, as well.

Figure 3.25: Schematic showing lowered apparent dielectric constant due to an interfacial SiO_x layer

3.2 Bulk Ferroelectric Lithium Niobate

We used bulk single crystal ferroelectric substrates for experiments with integrating them with the semiconductor ZnO, in order to be able to focus our study on the ferroelectric/semiconductor interface and on the semiconductor film. The bulk substrate removed unknowns related to the polycrystalline structure of thin films we deposited with techniques described in Section 2.1. We chose $LiNbO_3$ (LN) as the material to study in bulk form. LN is a very attractive ferroelectric material for the high spontaneous and remnant polarization, the high Curie temperature it exhbitis. Additionally, LN is a strong pyroelectric material. Therefore, we have an alternative stimulus, heat, to characterize our heterostructures. LN is a particularly good candidate for integration with ZnO, because it crystallizes in a trigonal structure. Therefore, it offers a favorable fit with the hexagonal structure of ZnO. ZnO thin films are expected to grow preferentially in a c-plane orientation on (0001)LN. A high quality interface between the semiconductor and the ferroelectric material is expected, which is key to modulating conductivity in the ZnO layer. Fig. 3.26 shows the (0001) plane of LN, with a visual guide of a triangle and a hexagon.

The ferroelectric charge in LN is caused by displacive polarization, in the same way as described for perovskite structures in section 2.1. The displaced ions are Li^{+1} and Nb^{+5}[48]. In this study we chose the bulk substrates we used such that the ferroelectric polariation is perpendicular to the $LiNbO_3$/ZnO interface, maximizing the

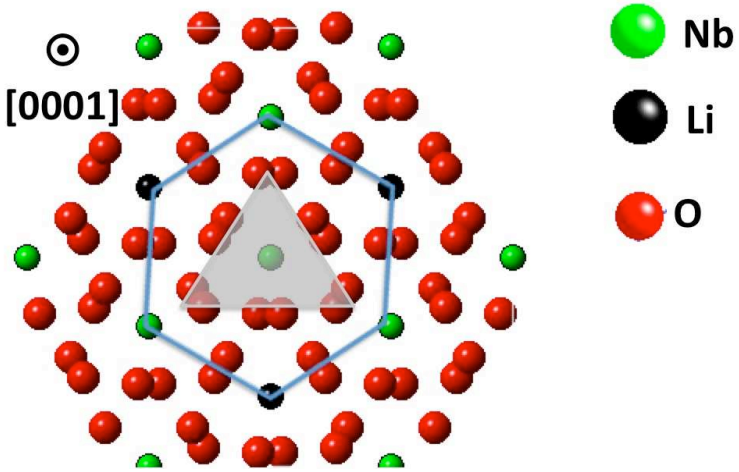

Figure 3.26: (0001) plane of $LiNbO_3$

amount of polarization charge available for coupling into the semiconductor. Fig. 3.27 shows a rendering of the LN crystal where we can see the ions that are displaced when the material is polarized.

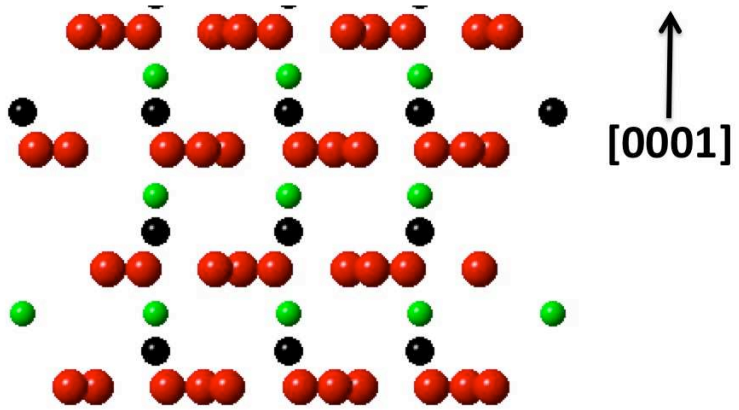

Figure 3.27: $LiNbO_3$ crystal with all ions

We purchased optical grade single crystal Z-cut lithium niobate wafers from Crystal Technology, Inc. and MTI Technology, Inc. We characterized their crystalline qualities using x-ray diffraction. Fig. 3.28 shows a $\theta - 2\theta$ scan centered around the lithium niobate (0006) diffraction peak.

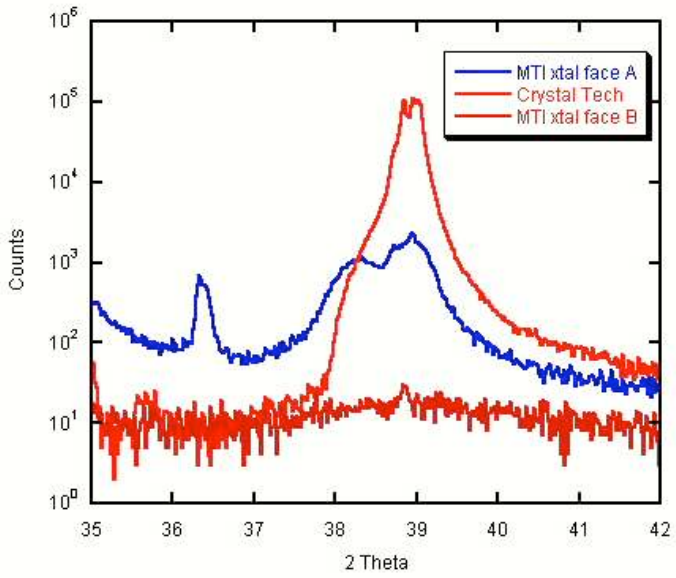

Figure 3.28: $\theta - 2\theta$ scan of bulk lithium niobate substrates

CHAPTER IV

Zinc Oxide Thin Films

Zinc oxide (ZnO) is a wide bandgap II-VI compound semiconductor that is abundant in nature, and is non-hazardous to humans and animals. It is of increasing interest as a semiconductor due to its bandgap in the ultraviolet (UV) wavelength range (3.4eV at room temperature), its radiation hardness, availability of its native substrates, and its large exciton binding energy (60meV). We are interested in this material for its chemical and thermodynamic compatibility with other oxides, namely, ferroelectric oxide materials. ZnO is an attractive material for integration with ferroelectrics with the purpose of building multifunctional devices such as sensor-transistors and storage-transistors. With this end-goal in mind, in this project we focus on manipulating the conductivity of the semiconductor through the polarization charge in the ferroelectric material. We therefore need to control the structural properties of the ZnO thin films very well, and to use them to subsequently fabricate high quality ferroelectric/ZnO heterostructures. Furthermore, we are interested in achieving a reasonably low background carrier concentration in the semiconductor, so that we can efficiently observe coupling of the ferroelectric charge into the semiconductor.

ZnO crystallizes in the heaxagonal Wurtzite structure, which is shown in Fig. 4.1.

It is intrinsically n-type in both its single crystal and polycrsytalline forms. There are continuing studies and debate on the sources of the n-type behavior aimed at determining whether the cause is oxygen vacancies, zinc interstitials, unintentional hydrogen incorporation into the film into the crystal[49], or a combination of mutiple mechanisms[50]. These native defects act as shallow donors in the crystal, and they lead to an intrinsic n-type behavior in ZnO thin films and ZnO bulk substrates. The intrinsic n-type behavior presents a challenge to growing p-type ZnO in a reliable and reproducible way. The challenges in achieving p-type ZnO have kept it from becoming a material of choice in optoelectronics applications so far. Recent progress has been reported in surmounting this difficulty[3], even though p-ZnO with high enough carrier mobility for light emitting ZnO homojunctions is yet to be achieved. With the advancement of p-type ZnO, UV/visible photodiodes and lasers, as well as solar blind UV detectors can be achieved. Diode behavior has been observed in heterojunctions of ZnO with p-type silicon[51], NiO[52], and ZnTe[53]; however, light emission with ZnO in the UV range remains out of reach.

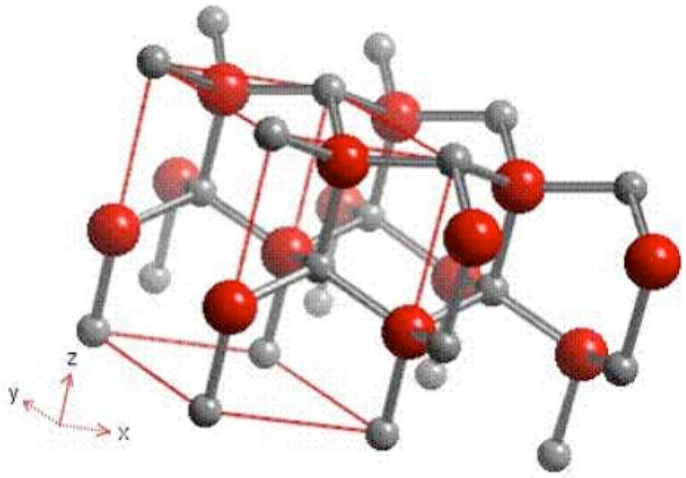

Figure 4.1: ZnO crystal structure

The high exciton binding energy of ZnO is a major factor making the material very

attractive; it makes high efficiency optoelectronic devices based on excitonic transitions plausible. Even though excitonic transitions have not been observed at room temperature so far, these transitions are evident at low temperatures through photoluminescence (PL) studies. Fig. 4.2 shows low temperature PL spectra for doped and undoped ZnO thin films. Both films show strong near bandedge transitions at at 3.36eV. The doped film exhibits excitonic transitions seen on a broadened peak centered around 3.3eV. Excitonic transitions are often related to defects acting as shallow donors, as well.

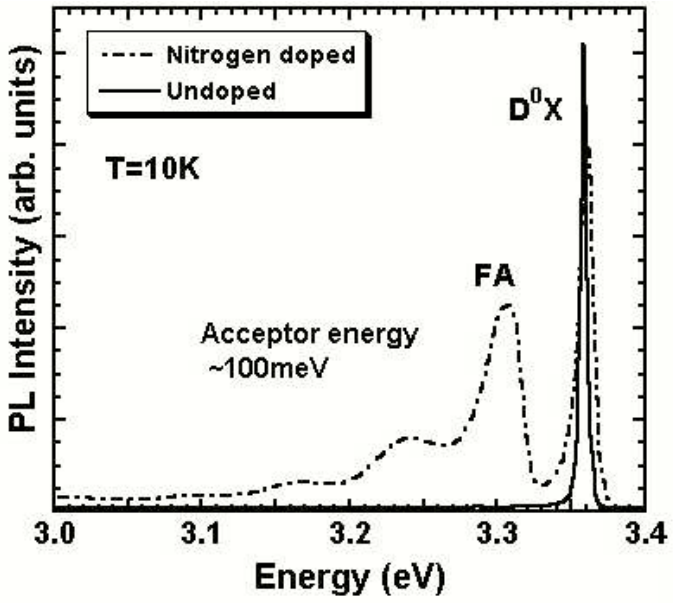

Figure 4.2: Low temperature PL spectra of doped and undoped ZnO thin films showing near bandedge and excitonic transitions

Room temperature PL studies give insight to the effects of increased point defect density. PL spectra of two ZnO thin films grown with molecular beam epitaxy are shown in Fig. 4.3. Strong bandedge emission is observed at room temperature, which is indicative of high quality crystalline material. Additionally, emission in the range 2.0-2.8eV is observed, to which we refer as green band emission. Deep acceptor levels linked to oxygen vacancies[54, 55], and O_{Zn} anti-site defects[56] are likely causes of

green band emission. As expected, the effects of these point defects become more pronounced with lower temperature growth, shown by the higher green band emission on the sample grown at 400°C compared to the sample grown at 600°C.

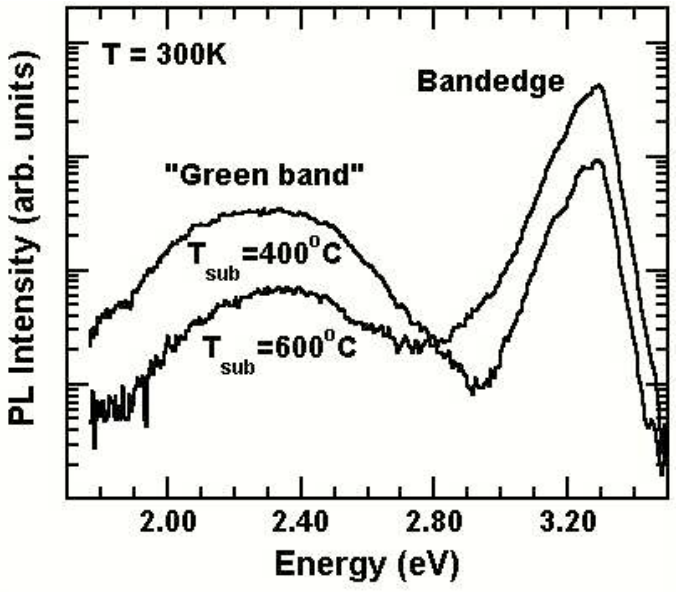

Figure 4.3: Room temperature PL spectrum of ZnO thin films grown at different temperatures

There are several methods through which ZnO thin films are grown or deposited in a variety of substrates. In this study we focus on pulsed laser deposition (PLD) and molecular beam epitaxy (MBE). Two methods that also yield favorable results are rf magnetron sputtering and atomic layer deposition (ALD) of ZnO. Device quality ZnO is achieved via sputtering, and thin film transistors are fabricated using sputtered ZnO channels[57, 58]. ALD has the advantage of being conducive to low temperature deposition of ZnO. For example, high resistivity buffer layers for solar cell applications are reported[59, 60]. Low temperature deposition by ALD has also shown favorable optical characteristics such as a free exciton binding energy of 67meV[61]. We chose PLD for experiments where a polycrystalline film is sufficient for electrical properties, and a high throughput is advantageous. We used MBE for experiments on single

crystal epitaxial ZnO thin films.

We deposited semiconducting thin films of ZnO using PLD and MBE on sapphire, $LiNbO_3$ (LN) and MgO bulk substrates, and on $Pb(Zr,Ti)O_3$ (PZT) thin films. Our substrate choices were based on an array of experimental and design concerns: Sapphire is a good match as a substrate, because it has a hexagonal structure like Wurtzite ZnO. Even though the lattice mismatch between c-plane sapphire and c-plane ZnO is 16%, single crystal epitaxial films have been achieved repeatably[62, 63]. LN substrates have an even larger mismatch with ZnO; however, we have observed strongly preferential c-plane orientation of ZnO thin films on LN substrates. Given that we are interested in integrating ZnO with perovskite ferroelectric oxides, growth of ZnO on cubic crystalline materials is a major step towards ferroelectric/ZnO heterojunctions. We used rock-salt (001) MgO as a substrate for epitaxial growth of non-polar ZnO to integrate the hexagonal ZnO structure with cubic structures. Our ultimate goal is to integrate ZnO with ferroelectrics; therefore, we used PLD to deposit ZnO on PTZ thin films that showed ferroelectric behavior. The ZnO thin films exhibited a wide range of electrical qualities depending on the substrate choice, and the growth or deposition technique. Background carrier concentration and carrier mobility are two important metrics for evaluating the electrical properties of the thin films, and they are strongly interdependent. Fig. 4.4 shows this interdependence and the varying material quality with deposition technique. 4.1 lists key electronic and structural properties of ZnO:

4.1 Pulsed Laser Deposition of ZnO Thin Films

Pulsed laser deposition (PLD) is conducive to studying ZnO deposition on many different substrates, because preferential orientation can be achieved through careful optimizatio of the laser beam energy, oxygen partial pressure, and substrate tem-

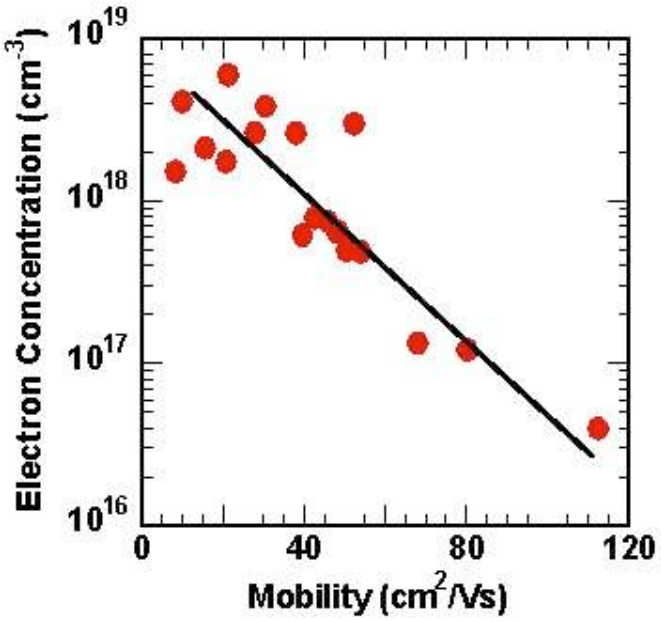

Figure 4.4: Carrier concentration vs mobility in ZnO thin films

perature during deposition. The operator has control over all of these deposition conditions. We deposited ZnO with laser energies ranging from 150mJ to 200mJ, which are moderate energy values for the system we use. The oxygen partial pressure was typically 10mTorr, and the substrate temperature for device quality ZnO was typically 600°C. Structural characterization of ZnO films was done primarily through x-ray diffraction. A Wide range $\theta - 2\theta$ scan of ZnO on c-plane sapphire is shown in Fig. 4.5, where ZnO is observed crystallizing preferentially in the (0002) orientation.

Energy bandgap	3.4eV
Exciton binding energy	60meV
Electron effective mass	$0.24m_o$
Hole effective mass	$0.78m_o$
Refractive index	∼2
Crystal structure	Wurtzite
Lattice constants	a=3.26$\mathring{A}$, c=5.21$\mathring{A}$
Electron saturation velocity	3x10^{7}cm/s[19]
E_{sat}	260kV/cm
Absorption coefficient	2x10^5/cm[64, 65]

Table 4.1: Summary of key ZnO material properties[2, 16, 50, 66]

Similar observations hold for ZnO deposited on MgO substrates under comparable conditions. Fig. 4.6 shows a $\theta - 2\theta$ scan of a ZnO film no MgO, where ZnO is once again preferentially oriented in the c-plane, (0002).

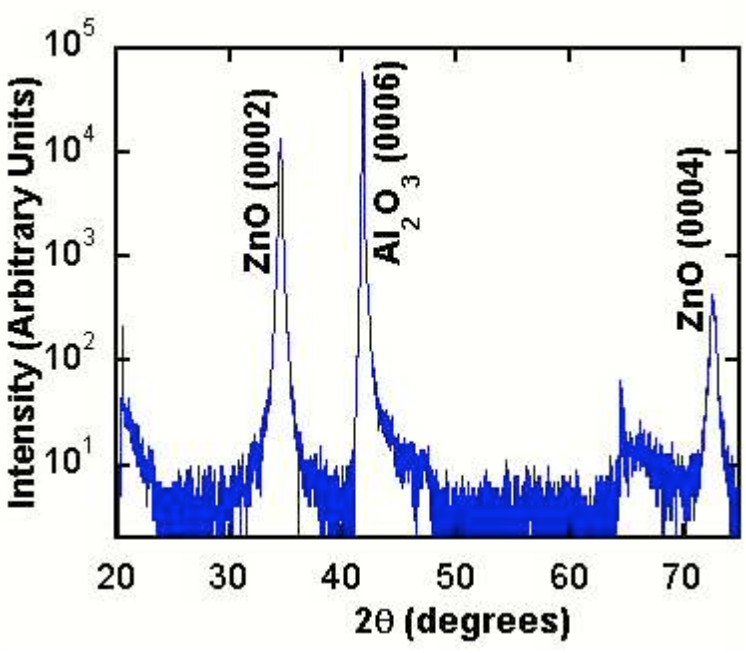

Figure 4.5: $\theta - 2\theta$ scan of ZnO on c-plane sapphire

The difference between a preferentially oriented film and a single crystal film must be noted here. The ZnO films are expected to be polycrystalline, in this case with all grains oriented in the same direction. The average grain size can be calculated using[67]:

$$B = \frac{0.9\lambda}{t\cos\theta},$$

where B is the broadening of the diffraction peak (in radians), λ is the x-ray wavelength used ($1.541\mathring{A}$ in our studies), t is the grain diameter, and θ is the diffraction angle. The broadening used for the calculation must be the peak broadening due only to the finite grain size. Therefore, we must account for other sources of broadening

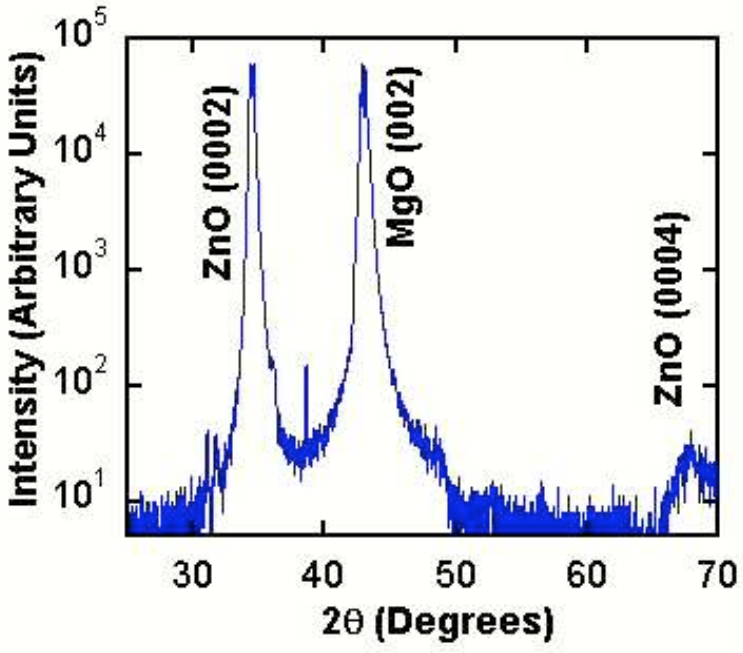

Figure 4.6: $\theta - 2\theta$ scan of ZnO on MgO

such as the x-ray beam divergence and the width fo the x-ray source. We used a single crystal ZnO film as a standard, with the broadening defining our standard broadening, B_S. The value for the broadening in the standard sample was 3.493x10^{-3}rad, obtained from the half width at full maximum of (0002) diffraction peak of a bulk single crystal ZnO substrate. We calculate the peak broadening for a typical ZnO PLD thin film calculated using the standard and measured broadening values, B_M and B_S, is calculated as follows:

$$\begin{aligned} B^2 &= B_M^2 - B_S^2 = (3.839 \times 10^{-3} rad)^2 - (3.493 \times 10^{-3} rad)^2 \\ B &= 1.60 \times 10^{-3} rad \end{aligned}$$

The average grain diamaeter, t, is therefore:

$$t = \frac{0.9\lambda}{B\cos(0.30rad)} = 87.2nm$$

Hall effect measurements were used to determine the mobility and the carrier concentration of the ZnO films. Typical PLD films had Hall mobility μ_H=10^2/V·s and carrier concentration n=10^{18}cm^{-3}. Lower carrier concentrations down to n=10^{17}cm^{-3} were achieved through optimization of the deposition conditions. Once we established PLD conditions to obtain these mobility and carrier concentration values repeatably, the next step was to integrate the well-studied ZnO thin films with ferroelectric thin films. The deposition conditions for ZnO via PLD are less harsh than the processing steps for sol-gel deposited Pb(Zr,Ti)O_3 (PZT): T_{PLD} is 600°C whereas the PZT films are annealed at 900°C. Both processes are done in oxygen environments. Therefore, we were able to deposit ZnO on the ferroelectric thin films without process related problems. Fig. 4.7 shows a wide range $\theta - 2\theta$ scan of the sample, where ZnO peaks corresponding to the (0002) and (10$\bar{1}$2) planes are observed.

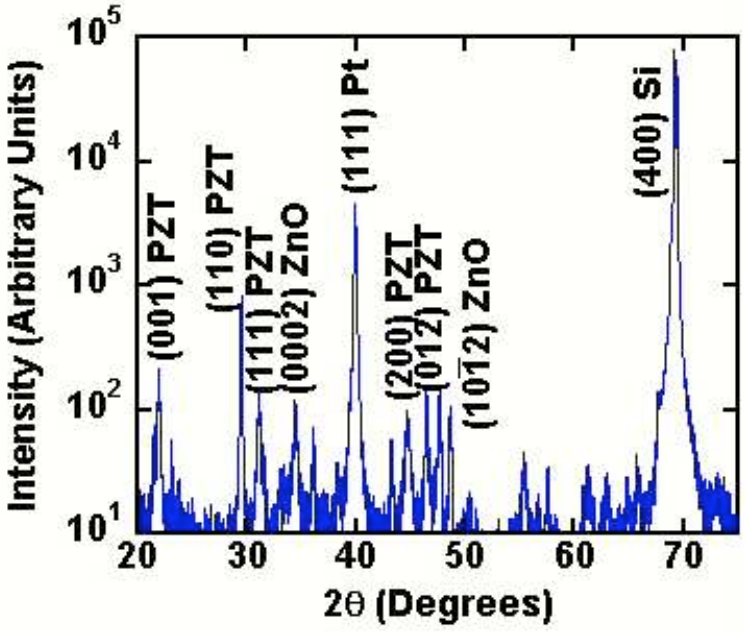

Figure 4.7: $\theta - 2\theta$ scan of ZnO on sol-gel processed PZT

While the crystallinity of the ZnO thin film was not as good as those on sapphire and MgO substrates, the electronic properties did not suffer considerably. Electrical characterization of the PZT/ZnO heterostructure is detailed in Chapter V. We see

that the efficiency with which the polarization charge in the PZT film modulates the ZnO film is low. The structural characteristics of the heterstructure give us insight into the reasons of the low efficiency. We observe in the $\theta-2\theta$ scans of the sol-gel PZT films that multiple orientations of PZT grains are present in the polycrystalline films. Visualizing three of the most readily observed PZT planes from the x-ray studies, the (111), the (110), and the (001) planes helps us understand the effect better. Comparing these planes to (0001)ZnO gives us insight into how good an interface we can expect. Fig. 4.8 compares (111)PZT to (0001)ZnO, where we see that the PZT structure is a reasonable fit. We can expect that the majority of the polarization induced modulation in the semiconductor occurs in areas where the combination (111)PZT‖(0001)ZnO is present.

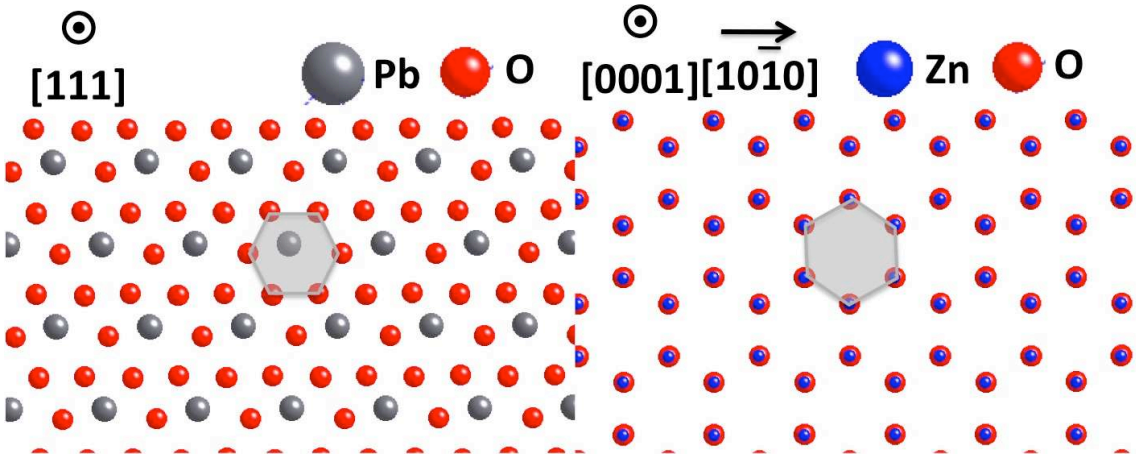

Figure 4.8: (111)PZT compared to (0001)ZnO

In contrast, comparing the (110)PZT and (001)PZT planes to the (0001)ZnO plane shows a much weaker fit. We expect a high density of defects at the ferroelectric/semiconductor interface on areas where the in-plane relationship is (110)PZT‖(0001)ZnO or (001)PZT‖(0001)ZnO. These areas will therefore have a much lower efficiency with which the ferroelectric polarization charge can modulate the semiconductor. The defects are also expected to contribute to leakage current. Fig. 4.9 and Fig. 4.10 provide

visualizations of the (110)PZT‖(0001)ZnO and (001)PZT‖(0001)ZnO arrangements respectively.

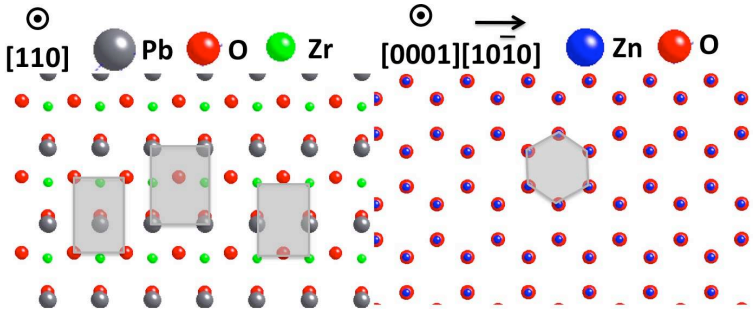

Figure 4.9: (110)PZT compared to (0001)ZnO

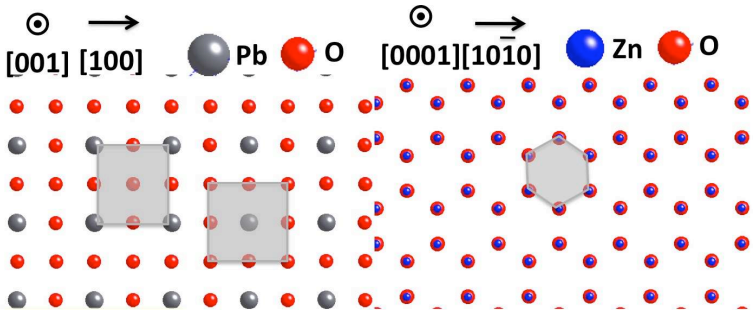

Figure 4.10: (001)PZT compared to (0001)ZnO

We used deposition conditions similar to those used for ZnO films of PZT thin films in order to deposit ZnO on bulk LN substrates. This was another step towards integrating ZnO thin films with ferroelectric materials. LN has the additional advantage of being a more compatible with the hexagonal ZnO structure, therefore we can expect to see high quality ZnO film form on LN substrates. Fig. 4.11 shows highly preferential orientation of ZnO on LN. Properties of the ZnO/LN heterostructures are detailed in Chapter VI.

There is a large lattice mismatch between LN and ZnO crystals: LN has the lattice constants a=5.14$\mathring{A}$ and c=13.86$\mathring{A}$, whereas ZnO has much smaller lattice constants a=3.25$\mathring{A}$ and c=5.20$\mathring{A}$. The exact in-plane orientation is not established, even though it is plausible that multiple rotations of the (0001)ZnO plane are present.

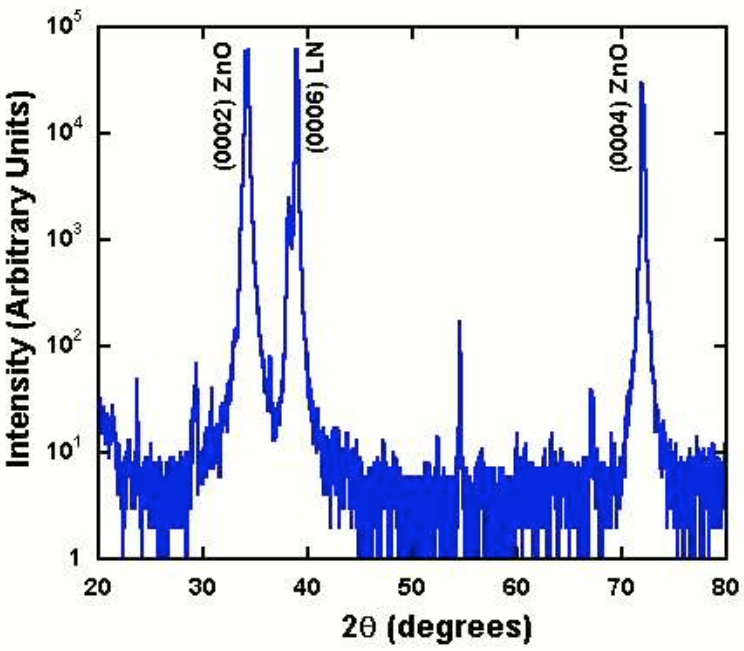

Figure 4.11: $\theta - 2\theta$ scan of ZnO on bulk $LiNbO_3$

Off-axis x-ray diffration scans (such as Φ scans) of the ZnO thin films on LN substrates show no detectable ZnO peaks, consistent with no single dominant in-plane orientation. Fig. 4.12 shows the LN crystal structure compared to the ZnO c-plane with no rotation, and with two different rotations.

4.2 Molecular Beam Epitaxy of ZnO Thin Films

High quality epitaxial crystals can be grown using molecular beam epitaxy (MBE) when an appropriate substrate is chosen, and the growth is controlled carefully. ZnO growth was done in our laboratory using a Riber 32 MBE machine with an oxygen plasma source module. Zinc was supplied through an effusion cell, and growth took place in an oxygen plasma. Growth was monitored in real time using an in-situ reflected high energy electron diffraction (RHEED) tool. High crystalline quality ZnO layers with low background carrier concentration are desired for effective coupling of ferroelectric polarization charge into the semiconductor. Electrical properties of

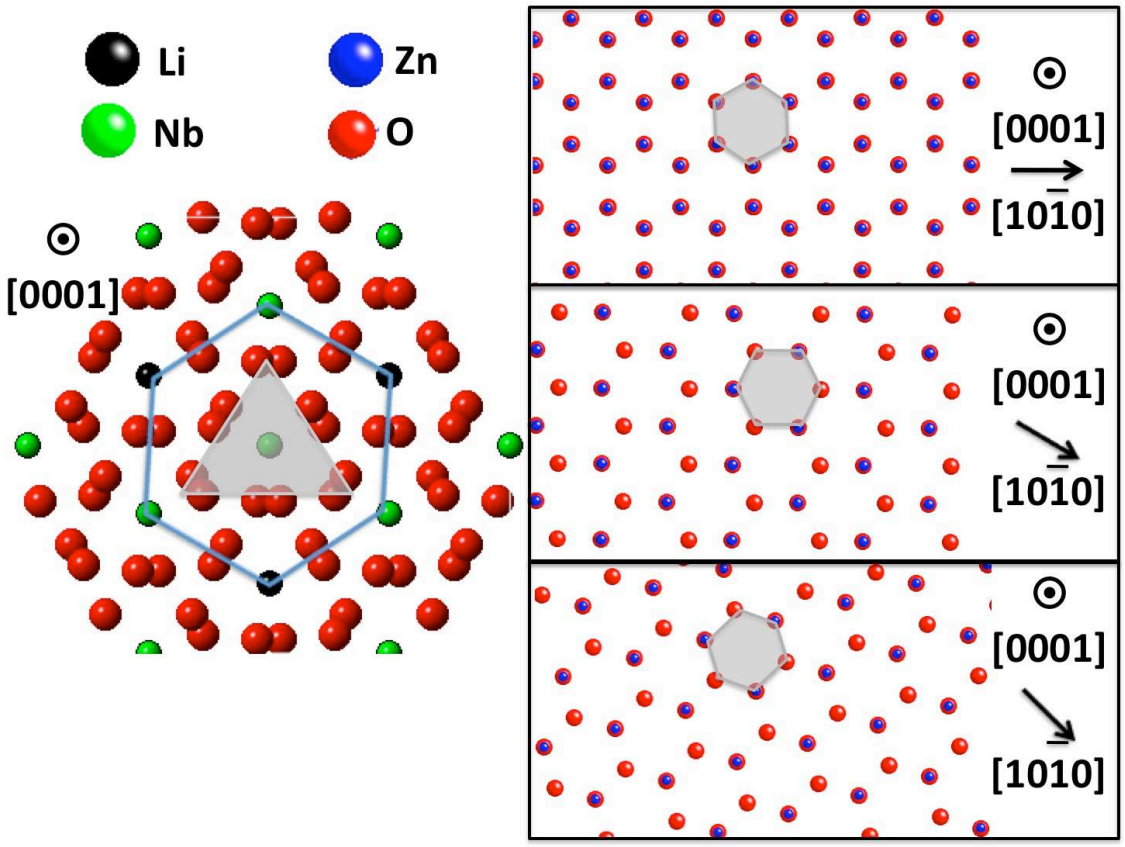

Figure 4.12: Crystal structures of ZnO and LN compared

epitaxial ZnO surpass those of pulsed laser deposited material due to the lower defect densities. Mobilities up to 80cm^2/V·s are achieved on the system used in this project. Lowest carrier concentration was n=10^{17}cm^{-3}. The substrate choice is crucial in determining the crystalline orientation and quality of the ZnO thin film, since the underlying template will determine the lattice mismatch, and the lowest free energy orientation for crystal growth. ZnO growth on hexagonal substrates has been studied extensively[63], focusing on sapphire as a substrate of choice. In this study we focus on the growth of ZnO on cubic substrates, since many ferroelectric materials with which we want to integrate ZnO are cubic structures. The epitaxial growth of wurtzite structures on cubic substrates typically uses the (111) orientation of the substrate due to the hexagonal symmetry resulting in polar growth with c-plane

orientation[68, 69]. In contrast, we used (001) rock-salt MgO substrates with the goal of having the c-ZnO in-plane, therefore simulating ZnO growth on perovskite oxides.

The cyrstalline orientation of the ZnO thin film grown on (001) MgO as determined by $\theta - 2\theta$ scans is shown in Fig. 4.13. A preferential orientation of ZnO in the $(10\bar{1}0)$ orientation is inferred for the MBE sampe based on the strong diffraction peak at 2θ=31.8°. A weak diffraction peak corresonding to the commonly observed (0002) ZnO diffraction peak is present at 2θ=34.4°. The origin of the weak c-plane diffraction for the MBE sample is believed to be select nucleation sites at particulates on the substrate surface, or substrate defects. Polycrystalline growth with preferential c-plane orientation would dominate on such sites. A high resolution transmission electron microscopy (TEM) image near the ZnO/MgO interface is shown in Fig. 4.14, where an abrupt interface is observed. Additionally, a very high level of crystalline order is observed in teh ZnO film. Insets in Fig. 4.14 show digital diffraction patterns (DDPs), which indicate interplanar spacing and phase for the ZnO and MgO layers. The DDPs are obtained by taking the fast Fourier transforms of the marked square regions in the TEM micrograph.

A selected area diffraction pattern (SADP) including both the ZnO thin film and the MgO substrate is shown in Fig. 4.15. Strong diffraction spots are observed for $(10\bar{1}0)$ ZnO and $(00\bar{2})$ MgO, with clear indication of the m-plane ZnO orientation on MgO (001), as suggested by x-ray diffraction. We therefore have supporting evidence that we have achieved non-polar ZnO growth on rock-salt MgO. We can further investigate the epitaxial relationships and the crystalline orientation of ZnO through comparison of the x-ray and TEM data. We calculate the interplanar spacing for m-plane ZnO using Bragg's Law[67] and taking into account the diffraction peak we observed at 2θ=31.9°:

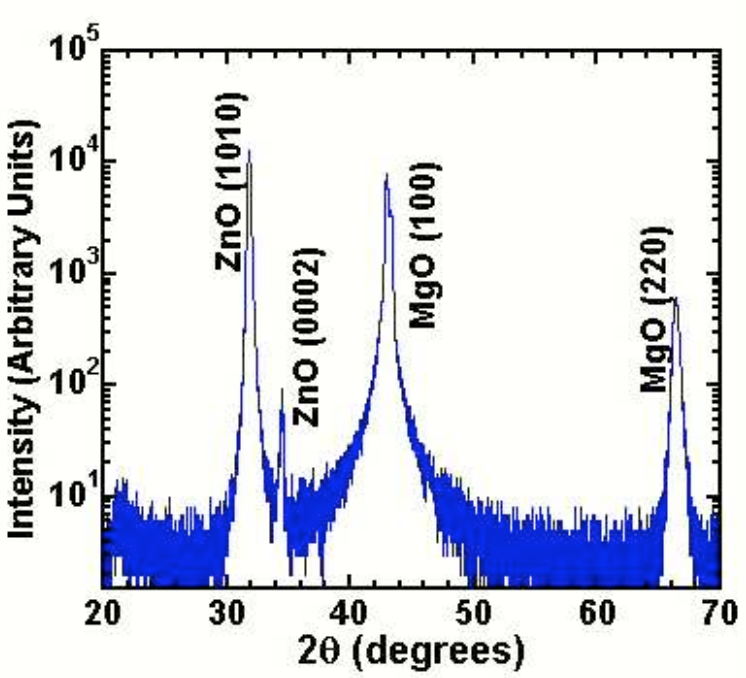

Figure 4.13: $\theta - 2\theta$ scan of epitaxial ZnO on (001) MgO

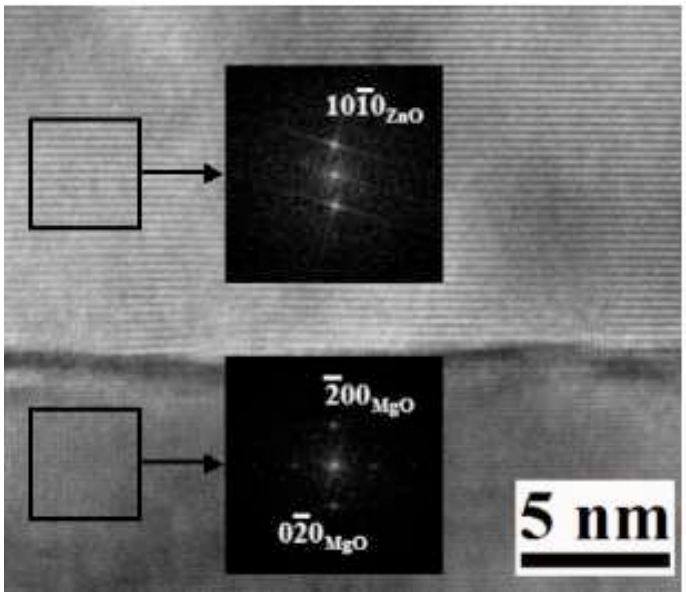

Figure 4.14: High resolution TEM image of epitaxial ZnO on MgO near the interface. Insets show DDPs in each layer.

$$\lambda = 2d\sin\theta$$

$$d = \frac{\lambda}{2\sin\theta} = 2.81x10^{-10}m$$

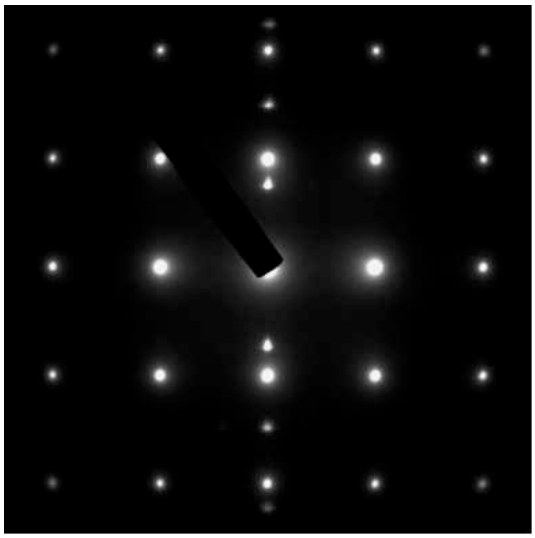

Figure 4.15: SADP of the epitaxial ZnO film on (001) MgO

We next calculate the interplanar spacing using the SADP in Fig. 4.15. We treat the diffraction peaks from MgO as known parameters, referring to a known interplanar spacing. We can do this since we are using a well-characerized bulk material as our substrate. We start with calculating the camera constant, CC, for the SADP we are using the following relationship:

$$CC = \lambda x L = Rxd$$

where λ is the electron beam wavelength; L is the distance between the sample and the flourescent plate of the TEM system; R is the distance between the transmitted electron beam and the diffraction peak (on the SADP); and d is the interplanar spacing of the sample crystal. Note that a shutter covers the transmitted electron beam in Fig. 4.15 in order to allow clear observation of the much weaker diffraction peaks from the sample. The center of the transmitted beam is marked with a T on the image.

$$
\begin{aligned}
R_{(\bar{2}00)MgO} &= 36.52nm^{-1} \\
d_{(\bar{2}00)MgO} &= 0.474nm \\
R_{(10\bar{1}0)ZnO} &= 26.88nm^{-1} \\
CC &= R_{(\bar{2}00)MgO} x d_{(\bar{2}00)MgO} = 7.66 \\
d_{(10\bar{1}0)ZnO} &= \frac{CC}{R_{(10\bar{1}0)ZnO}} = 0.285nm
\end{aligned}
$$

The two calculations for the $(10\bar{1}0)$ ZnO interplanar spacing agree with each other very well; therefore, we use the average of the two values for the rest of our calculations. We take d=2.83$\mathring{A}$. The lattice constants, a and c, of ZnO are the next indicators of m-plane growth. We calculate the lattice constant a using the bulk lattice constant c=5.21$\mathring{A}$ in order to further test our m-plane growth hypothesis. The lattice constants of a hexagonal crystal are related to the interplanar spacing through[67]:

$$
\begin{aligned}
\frac{1}{d} = \frac{3}{4}\left(\frac{h^2 + hk + k^2}{a^2}\right) + \frac{l^2}{c^2}\,. \\
for\ c = 5.21\mathring{A},\ h = 1,\ k = 0,\ l = 1 \\
a = 3.25\mathring{A}
\end{aligned}
$$

The calculated value for the lattice constant a is very close to that of bulk ZnO, a=3.26$\mathring{A}$. We therefore have observations that are consistent with m-plane growth. We established a well-understood method to grow epitaxial ZnO with the polar c-plane of the material parallel to the substrate. In this case, the spontaneous polarization of ZnO is expected to be in-plane. The material is non-polar in the direction of growth. The non-polar $(10\bar{1}0)$ plane was characterized and evidenced by detailed

x-ray diffraction and TEM studies, and the empirically determined epitaxial relationships matched the theoretical calculations.

CHAPTER V

Pb(Zr,Ti)O_3/ZnO Heterostructures

Ferroelectric and semiconductor materials both have highly desirable properties, as detailed in previous chapters of this dissertation. We would like to integrate the two types of materials in order to take advantage of both, and achieve devices with enhanced functionality. Our goal in this project was to use the ferroelectric polarization charge to modulate the conductivity in the semiconductor layer. To that end, we required a ferroelectric layer with strong polarization charge, and a semiconductor with low enough background carrier concentration for the charge modulation to be discernible. Prototype ferroelectric/semiconductor heterostructures helped us characterize the electrical behavior of the materials under study. We fabricated metal-ferroelectric-semiconductor (MFS) capacitors using Pb(Zr,Ti)O_3/ZnO heterostructures and Pt electrodes.

This chapter discusses fabrication and characterization of PZT/ZnO capacitors. We use calculated band diagrams to review the electrical performance we expect from the capacitors. The heterostructure model we presented in Chapter II is used to draw band diagrams for PZT/ZnO structures. Capacitance-voltage, AC conductance-voltage, and circuit performance of the heterostructures are presented in order to understand the capabilities and the limitations of the MSF capacitors.

We fabricated PT/PZT/ZnO capacitors as initial prototypes of metal-ferroelectric-semiconductor heterostructures. We started with Pt/Ti/SiO_2/Si substrate, which provided a blanket bottom contact. We deposited ferroelectric PZT thin films through sol-gel processing, as detailed in Chapter III, on these substrates. ZnO thin films then followed through pulsed laser deposition, as explained in Chapter IV. Finally, circular top electrodes (d=230μm) were evaporated through a shadow mask to provide Ohmic contacts to the ZnO layer. The top electrode metal stack was Ti/Al/Au, which was shown to give Ohmic contacts to n-ZnO[70]. Fig. 5.1 shows a schematic of the capacitor under study. Both PZT and ZnO thin films were wet etched in a small area on each sample to provide direct probe access to the bottom Pt electrode. The etchant was dilute buffered hydroflouric acid (1:10 ratio acid:de-ionized water), and the etch rate was approximately 30nm/sec for both layers. A 30sec etch followed by an oxygen plasma clean for 60sec resulted in a residue-free area for probing.

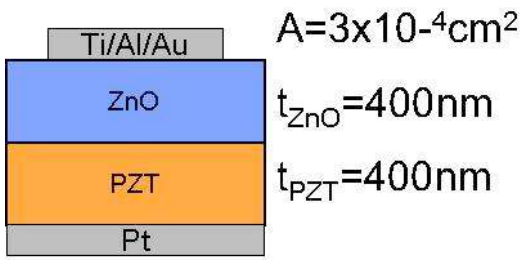

Figure 5.1: Schematic of prototype metal-ferroelectric-semiconductor-metal capacitor

5.1 Band Diagrams in Depletion and Accumulation

Prior to measuring the electrical properties of the capacitors, we calculated the band diagram using the charge control model given in Chapter II. The band lineup is approximated using the electron affinities of the different layers. A type-II heterostructure arrangement is assumed using the electron affinities of PZT and ZnO.

The electron affinity values for PZT and ZnO we used are 3.50eV and 4.35eV respectively. The bandgap energies used are 3.70eV for PZT and 3.34eV for ZnO. The bottom electrode is included in the calculation, with the electron affinity of Pt taken as 5.3eV. The carrier concentration in ZnO is assumed to be 10^{18}cm^{-3}, which is a typical value measured through Hall effect measurements on comparable ZnO thin films deposited on high resistivity silicon substrates.

The resulting conduction band discontinuity between PZT and ZnO is 0.85eV. This value is also the barrier to electron transport from ZnO into PZT, which is a possible contributor to leakage current in Pt/PZT/ZnO structures. The valence band discontinuity is only 0.49eV; however, the low barrier is not a significant concern regarding leakage current. This is because hole concentrations in ZnO films in this study are very low, and therefore, not a large portion of leakage current is caused by holes. The leakage current density for Pt/PZT/Pt was measured in order to establish the insulating properties of the PZT films. The leakage current density at 5V_{DC} applied bias was on the order of $10\mu\text{A/cm}^2$. The leakage current density for Pt/PZT/ZnO capacitors varied among different samples, as well as varying among different capacitors on the same sample. In all cases, leakage current on the Pt/PZT/ZnO capacitors was significantly larger than the Pt/PZT/Pt capacitors, ranging from a factor of 10 to several orders of magnitude larger than the Pt/PZT/Pt current density. The source of the leakage current is likely grain boundaries in the polycrystalline films, rathan than low barriers in the band structure.

We must note that heterojunction band discontinuities can have large deviations from the electron affinity model, and can also be strongly influenced by the defects at the interface. Consequently, calculated band diagrams included here are approximations, which nevertheless give valuable insight into the capacitor characteristics. Fig. 5.2

shows the heterostructure in depletion, and Fig. 5.3 shows the heterostructure in accumulation.

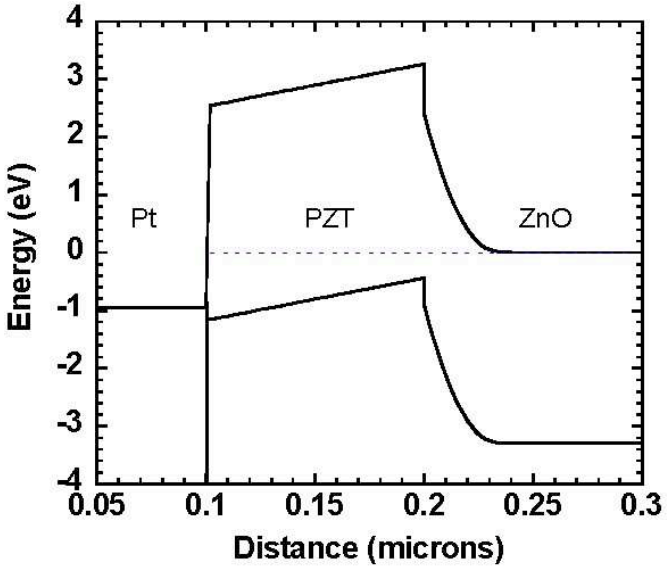

Figure 5.2: Band diagram of PZT/ZnO heterojunction in depletion

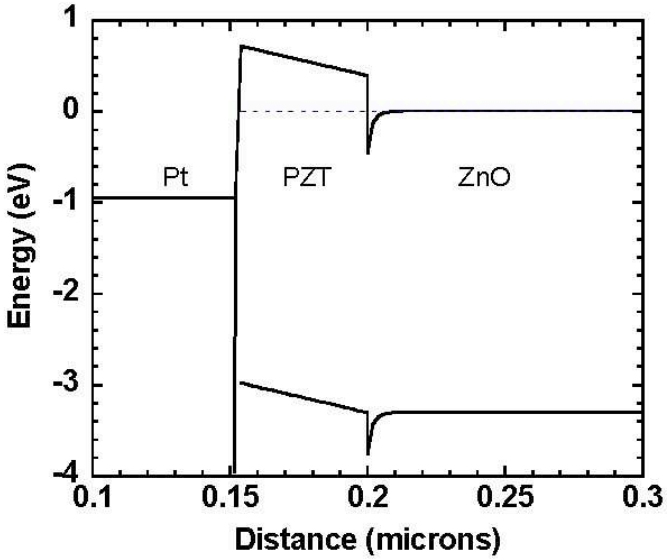

Figure 5.3: Band diagram of PZT/ZnO heterojunction in accumulation

5.2 Capacitance-Voltage Behavior

We measured the capacitance-voltage (C-V) characteristics of the Pt/PZT/ZnO capacitors for a frequency range of 5kHz-1MHz using an Agilent/HP 4284A inductance-capacitance-resistance (LCR) meter. The AC amplitude of the applied voltage across the capacitors was 10mV and the DC voltage sweep was carried out with a step size of 100mV, at a rate of 100ms per step. Fig. 5.4 shows the internal circuitry of the LCR meter. Our sample was the device under test (DUT), and it was connected between the low potential and high potential connection points shown in the figure. The equipment was controlled by custom data collection software provided by Agilent.

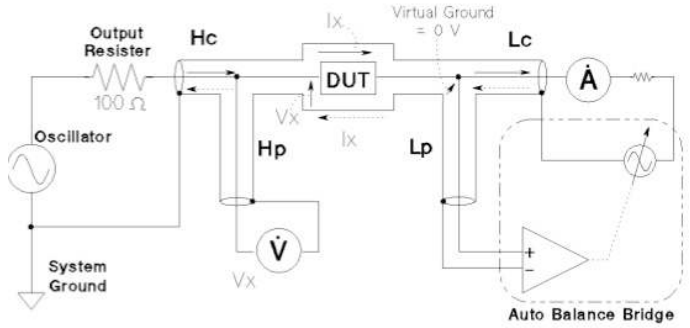

Figure 5.4: Internal circuitry of the Agilent/HP 4284A LCR meter, from the equipment operator's manual [71]

Fig. 5.5 shows the C-V measurement results, depicting only a small variance in capacitance values with frequency. While the frequency increased by two orders of magnitude, the change in corresponding capacitance measurements was limited to 20%.

There are three effects that are readily observed on Fig. 5.5. Firstly, the expected MIS capacitor behavior is most readily evident in the positive-to-negative sweep direction on the plot. Between -3V and 2V we observe accumulation; above 2V the capacitor enters depletion. Inversion is not observed due to the short minority carrier lifetime of holes in ZnO. Secondly, the hysteretic behavior in the C-V curves is at-

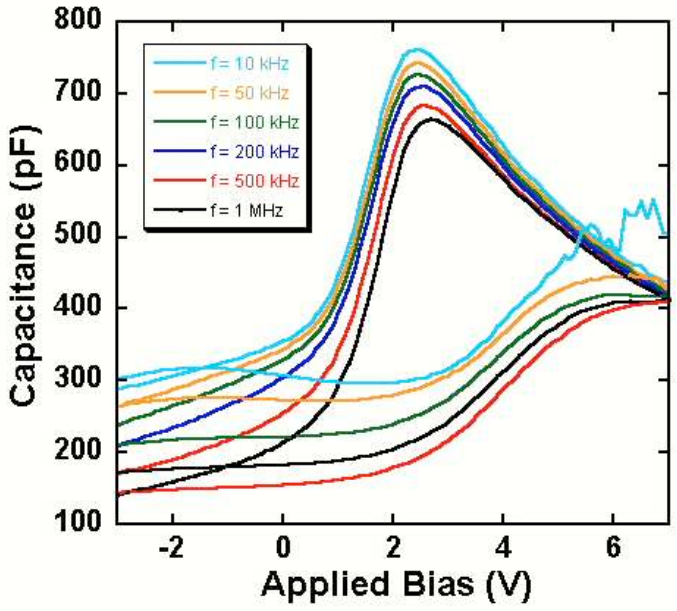

Figure 5.5: Capacitance-voltage measurement result for a Pt/PZT/ZnO structure

tibuted to the ferroelectric polarization charge of PZT being coupled into ZnO at the ferroelectric/semiconductor interface. The hysteresis leads to a memory window of approximately 3.5V. Thirdly, the field dependence of the dielectric constant of PZT causes the peaking in capacitance evident in the negative-to-positive sweep direction. The field dependence of ϵ is described for a similar material, (Ba,Sr)TiO_3[72], and predicted by the same relationship for PZT as follows:

$$C(V) = \frac{C_{max}}{[1 + (\frac{2V}{V^2})^2]^{0.42}}$$

Fig. 5.6 shows a comparison of the observed C-V behavior to that we calculated using a superposition of the standard MIS C-V characteristics and the variation in the PZT dielectric constant. The calculation shows that the measured C-V behavior results from a density of sheet charges at the PZT/ZnO interface with a magnitude of 3×10^{12}cm^{-2}. This charge corresponds to a very small fraction of the polarization charge measured in Pt/PZT/Pt capacitors, 1.3×10^{14}cm^{-2}, being coupled into the semiconductor. The stability of the C-V results lead us to believe that interface

trap states are not significantly affecting the C-V behavior of the capacitors. The slope of the C-V characteristics also closely follows C-V characteristics neglecting interface traps. This suggests that energetically distributed traps at the interface are not strongly affecting C-V behavior, where such traps would be expected to result in a shallower slope in the C-V curve. The low efficiency in coupling the ferroelectric charge into the semiconductor is attributed primarily to the leakage current.

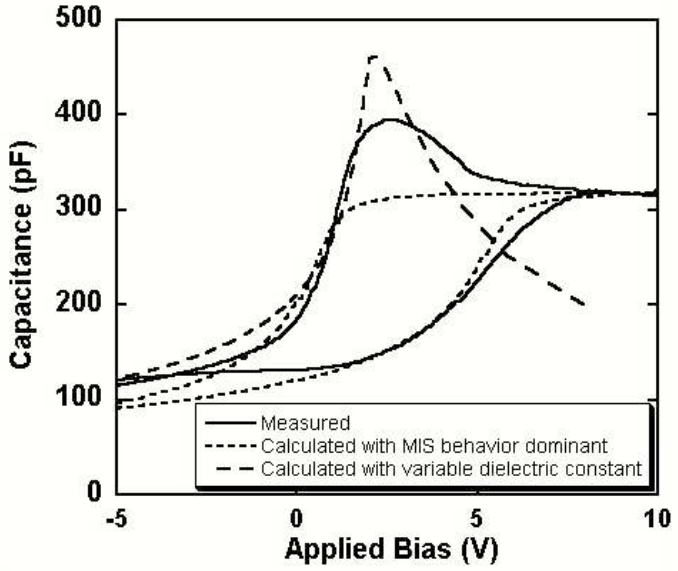

Figure 5.6: Calculated and measured C-V behavior of Pt/PZT/ZnO capacitors at 1MHz

5.3 Hysteretic AC Conductance

AC conductance characteristics of the Pt/PZT/ZnO capacitors measured using an Agilent/HP 4284A LCR meter. This was the same equipment as the LCR meter used for C-V measurements. The circuitry is shown in Fig. 5.4. For AC conductance measurements the sample was connected between the low current and the high current points. The measurement was carried out with an applied sinusoid of frequency 1MHz. The hysteretic behavior we observed as a result is shown in Fig. 5.7. The hysteresis we observe on the AC conductance is consistent with the C-V behavior;

AC conductance demonstrates a significant change with applied bias, and a memory window of ∼3.5V. Conduction through the Pt/PZT/ZnO capacitor is largely due to leakage current through the device. As the bias is swept in the negative-to-positive direction, the heterostructure goes into accumulation mode. We can see from the band diagram in Fig. 5.3 that the barrier to electron conduction is lowered in accumulation. Consequently, the conductance increases by one order of magnitude as bias increases in the negative-to-positive direction. In the reverse direction the heterostructure goes into depletion mode, with the barrier to electron conduction increased. In this case the leakage current becomes much smaller, and the measured conductance falls.

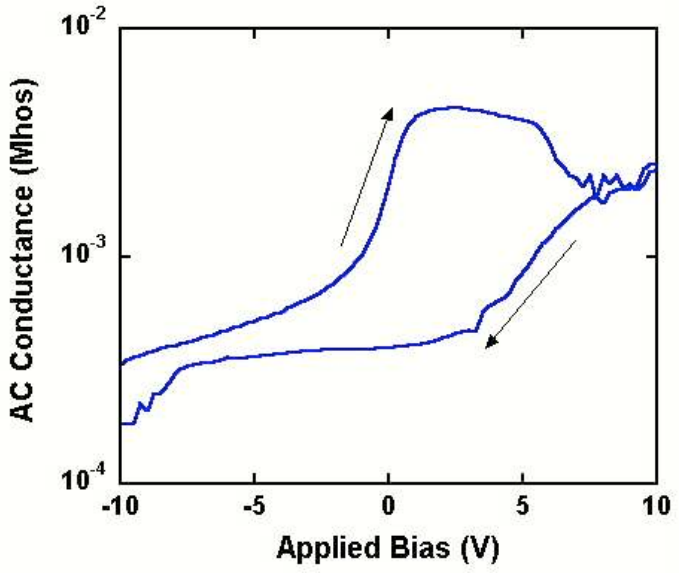

Figure 5.7: AC conductance of Pt/PZT/ZnO capacitors measured at 1MHz

5.4 PZT/ZnO Heterostructures in a Series RLC Circuit

We built the PZT/ZnO a basic passive resonant circuit to further demonstrate the hysteretic behavior and potential utility of the MFS structures. We used a series resistor-inductor-capacitor (RLC) configuration for this purpose, as shown in Fig. 5.8. The circuit values were chosen to provide a resonance frequency within the range where C-V data were measured. The input consisted of a $2V_{DC}$ bias and a

sinusoidal input signal with peak-to-peak amplitude of 100mV. The PZT/ZnO capacitors were poled at $\pm$ 2V$_{DC}$ prior to the measurement using a DC power supply. An input sinusoid was provided ot the series RLC circuit using an Agilent/HP 33120 function generator. The input wave, as well as the output sinusoid from the circuit were monitored using an Agilent 3000-series oscilloscope. The frequency response of the circuit was thus created by varying the input frequency and recording the output/input magnitude ratio with respect to frequency.

The frequency response of the series RLC circuit is shown in Fig. 5.9, and it demonstrates peak resonance frequencies of 180kHz and 210kHz for opposing polarization directions, therefore, a total resonant frequency shift of 30kHz. The values of the PZT/ZnO capacitor corresponding to the 2V$_{DC}$ operating point are 145pF and 390pF for opposing polarization states. For these values the resonance frequencies are expected to be at 80kHz and 130kHz, a shift of 50kHz. The expected bandwidth of the RLC circuit is 1kHz, which is much smaller than the measured value of 30kHz. These differences are attributed to the series resistance and parasitic capacitances from the test setup.

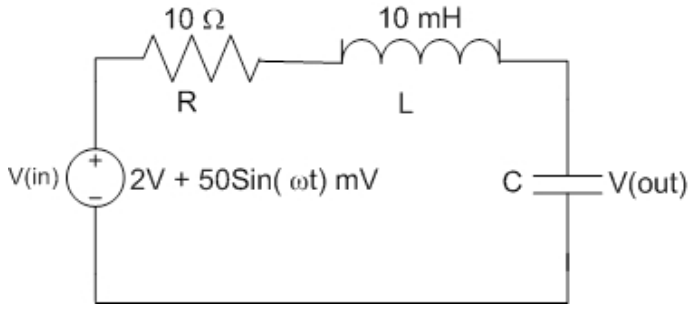

Figure 5.8: Series RLC circuit used for characterizing Pt/PZT/ZnO capacitors

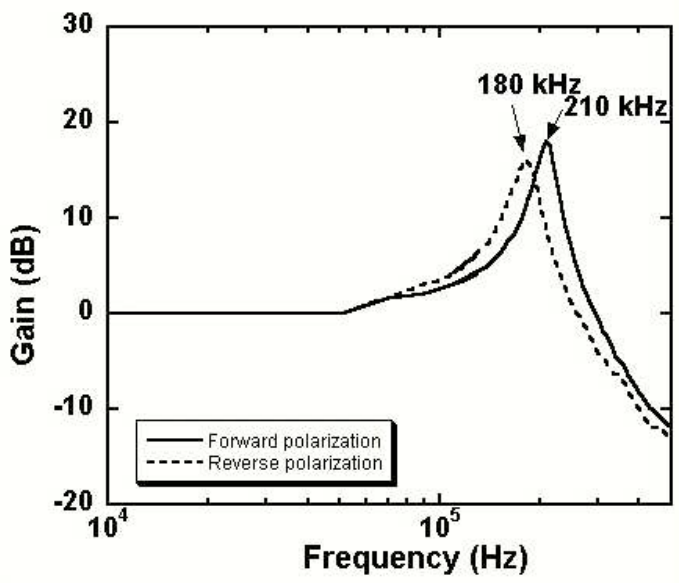

Figure 5.9: Frequency response of series RLC circuit with Pt/PZT/ZnO capacitors

5.5 Conclusions

In our study of ferroelectric/semiconductor heterostructures so far, we showed that we can deposit ferroelectric thin films of PZT in the perovskite phase using sol-gel deposition; that we can deposit ZnO thin layers with acceptable electronic properties on PZT layers, and that we can modulate the semiconductor layer through the ferroelectric polarization charge. We fabricated metal-ferroelectric-semiconductor (MSF) capacitors using Pt/PZT/ZnO stacks, and we characterized them using capacitance-voltage (C-V) and AC conductance measurements. We compare these measurements to the polarization-electric field characteristics of the PZT layers alone, presented in Chapter III. The comparison shows that the memory window of the ferroelectric material is preserved at $\sim$3.5V for all measurements. Especially encouraging is that the memory window does not change significantly during variable frequency C-V measurements on the MSF capacitor.

There are multiple challenges that remain upon studying ferroelectric/semiconductor

integration using Pt/PZT/ZnO capacitors. Firstly, we observe high leakage currents, as evidenced by the AC conductance results. Both the ferroelectric and the semiconductor layer are polycrystalline; therefore, grain boundaries in the films are available as conduction paths for leakage current. The polycrystalline structure of ZnO stems largely from the mismatch between the crystal structures of PZT and ZnO. A better matched crystal pair is desirable. Secondly, the polarization values in the ferroelectric layer vary significantly between samples. The yield in the sol-gel process is low, leading to a need to individually characterize each sample for polarization and permittivity values. We would like to be able to design MFS capacitors with known electrical properties in order to achieve practical devices.

We investigated heterostructures fabricated using $LiNbO_3$ as the ferroelectric material in order to address the challenges we still face. $LiNbO_3$ structure and properties are outlined in Chapter III. $LiNbO_3$/ZnO heterostructures are detailed in Chapter VI.

CHAPTER VI

LiNbO_3/ZnO Heterostructures

$LiNbO_3$ (LN) is a highly promising candidate for integration with ZnO, because it offers a high level of structural and electrical compatibility. We learn from the Pb(Zr,Ti)O_3/ZnO heterostructures investigated in Chapter V that a closer crystal structure fit is desirable in order to obtain a low defect density ferroelectric/semiconductor interface. Additionally, a large bandgap (E_G(LN)=4.0eV is beneficial for the band line-up to ZnO to offer large barriers to electron and hole conduction. We therefore expected that the use of LN as the ferroelectric material would help reduce the leakage current we observed with PZT/ZnO heterostructures. The large pyroelectric coefficient of LN (-4×10^{-5}C/$\circ$Km^2)[73] provided another advantage, allowing an alternative method to test for modulation of the semiconductor layer.

There are challenges to growing thin films of LN, especially in achieving the correct stochiometry. Furthermore, the large bandgap of the material necessitates large beam energies when a method such as pulsed laser deposition is used. Often, noninsulating layers with oxygen deficiencies or incorrect chemical make-up result. We chose instead to use bulk single crystal LN substrates for our experiments, thereby ensuring that we start with a high quality ferroelectric material. However, bulk substrates mean that carrying out capacitance-voltage or polarization-electric field measurements require

very high voltages. The coercive field of LN (typically 15kV/cm) would require that we apply 750V or more across a 500μm substrate in order to switch the polarization direction. Since these voltages were not practical in our laboratory, we designed different experiments to characterize the LN/ZnO heterostructures. We used Hall effect measurements to measure the conductivities and the carrier concentrations of ZnO thin films on LN substrates of known polarizations.

We fabricated LN/ZnO heterostructures through pulsed laser deposition of ZnO thin films. We co-deposited ZnO thin films on sapphire substrates in order to have control samples. The properties of ZnO thin films on sapphire substrates are studied in detail, and explained in Chapter IV. The ferroelectric LN substrates provided an ability to select the sign of the polarization charge on which we deposited the ZnO films. All substrates were Z-cut. In the discussion and the figures in this chapter, the samples where ZnO film was deposited on the surface with negative polarization charge are labelled $-Z$ face; the samples where the ZnO film was deposited on the surface with positive polarization charge are labelled $+Z$ face.

The ferroelectric polarization charge in the LN substrate is expected to induce band bending in the ZnO film, causing either accumulation or depletion. The band bending in the semiconductor is calculated using the charge control model detailed in Chapter II, and representing the ferroelectric polarization charge as a sheet charge at the LN/ZnO interface. The bandgap value used for ZnO is 3.34eV. Fig. 6.1 shows the results of the calculation. Interfacing n-type ZnO with the +Z face and the -Z face of LN is expected to cause accumulation and depletion respectively.

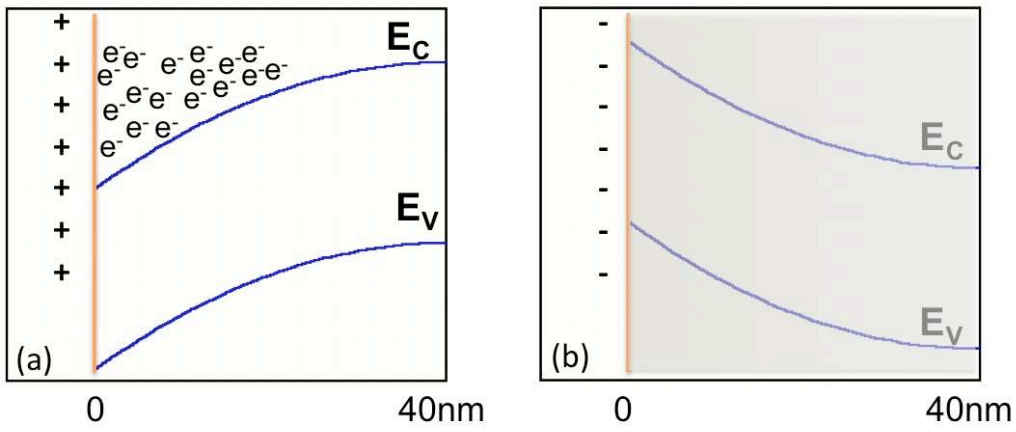

Figure 6.1: Band bending in ZnO thin films on $LiNbO_3$ in (a)accumulation, (b)depletion

6.1 Hall Effect Measurements

Our expectation is that the conductivity of the ZnO thin film will be modulated by the ferroelectric charge direction and magnitude. We therefore use Hall effect measurements to obtain the carrier concentration and Hall mobility of the ZnO films. The resistivity of the film is also measured through Hall effect, and provides additional insight. The measured carrier concentration, Hall mobility, and resistivity values are compared to those measured on the control samples. We further verified that the values measured on the control samples are consistent with typical ZnO/sapphire properties achieved in our laboratory. Fig. 6.2 compares the carrier concentrations of ZnO films of different thicknesses on different LN and sapphire substrates. Fig. 6.3 and Fig. 6.4 show the Hall mobility and the resistivity measured on the same samples with respect to ZnO film thickness.

There are multiple observations from the Hall effect measurements that help us analyze the effect of the ferroelectric polarization charge on the semiconductor layer. The carrier concentration and resistivity are affected significantly for thin ZnO layers, whereas they both stay roughly unchanged for layers thicker than 50nm. In contrast, Hall mobilities for ZnO films on the -Z and the +Z faces of LN are very close to each

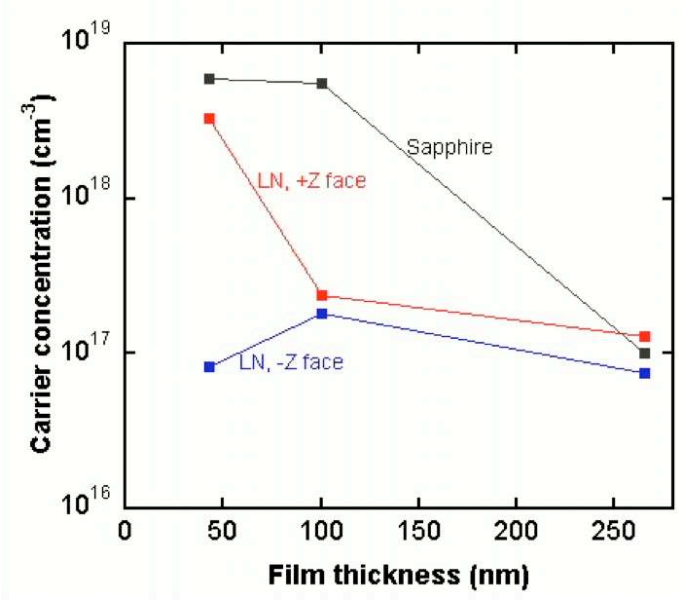

Figure 6.2: Carrier concentration vs thickness of ZnO thin films on $LiNbO_3$ substrates

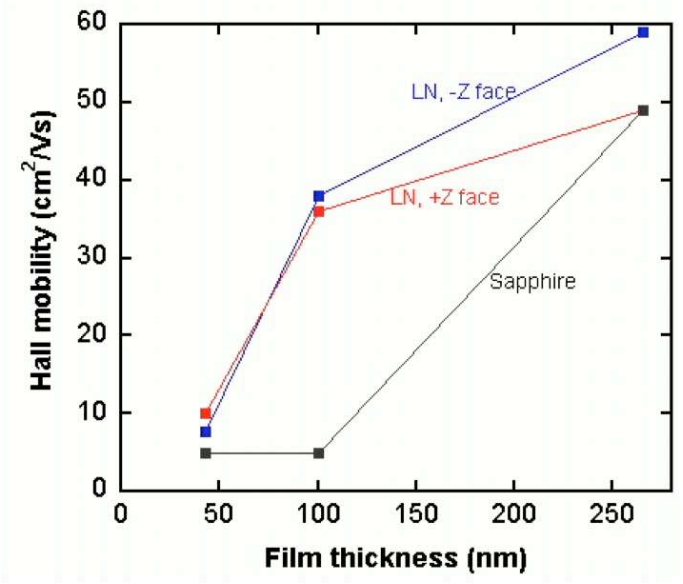

Figure 6.3: Hall mobility vs thickness of ZnO thin films on $LiNbO_3$ substrates

other regardless of the film thickness. When mobility and carrier concentration are determined primarily by defect density, then the two properties will be parallel to each other, unlike our observation in this case. Our observation for very thin films (<50nm) is instead consistent with the ZnO film on the -Z face of LN exhibiting depletion effects. Accumulation effects would be very difficult to discern, since the

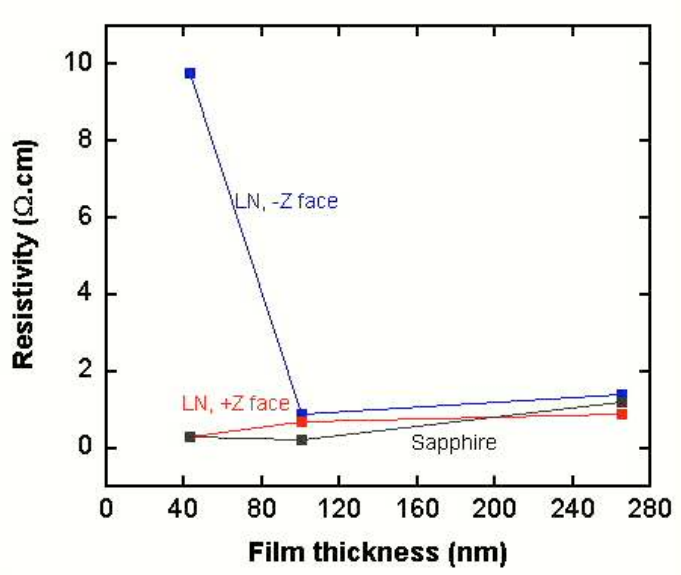

Figure 6.4: Resistivity vs thickness of ZnO thin films on $LiNbO_3$ substrates

background concentration is already high. However, the direction of the polarization causes a difference of larger than an order of magnitude for very thin ZnO films on LN.

The next observation to address is that the difference in carrier concentration and resistivity values is only seen in very thin films. We note that Hall effect is measured on the surface of the film, where contacts are made. In the case of our samples, the distance between the ferroelectric/semiconductor interface and the measurement point is equal to the thickness of the film. Therefore, the thicker the film gets, the farther the measurement gets from the region where band bending occurs. As a result, any band bending that is limited to a region near the interface is not observed using Hall effect measurements. Fig. 6.5 summarizes the case where the film thickness is much larger than the depletion width.

6.2 Pyroelectric Effect

$LiNbO_3$ exhibits pyroelectric effect, through which the polarization charge increases when the temperature increases. Therefore, an increase in temperature can

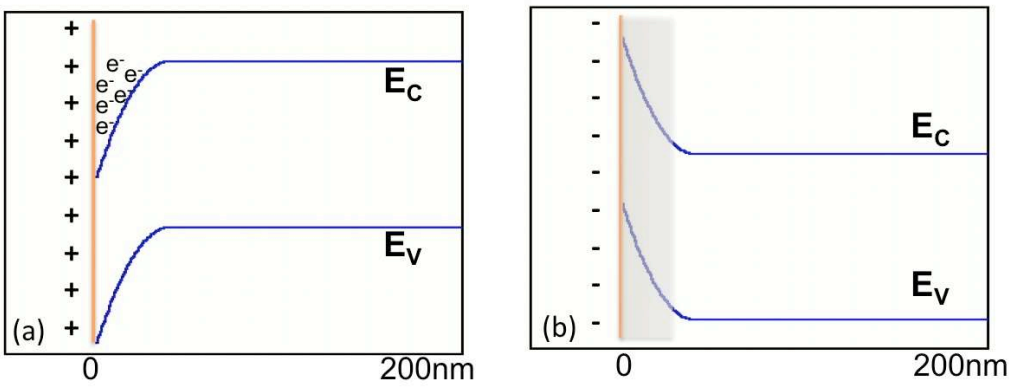

Figure 6.5: Band diagrams of thick ZnO thin films on LN in (a)accumulation, (b)depletion

induce a change in the conductivity of a ZnO thin film, if the polarization charge is indeed modulating the semiconductor. We exploited the pyroelectric effect in LN in order to further characterize the LN/ZnO heterostructures. We constructed a basic voltage divider circuit, shown in Fig. 6.6, where one of the resistors was the ZnO thin film on a -Z face LN surface. When the heterostructure is heated, the polarization charge should increase, further depleting the ZnO film, increasing its resistivity. In that case, the voltage dropping across R_{ZnO} should increase.

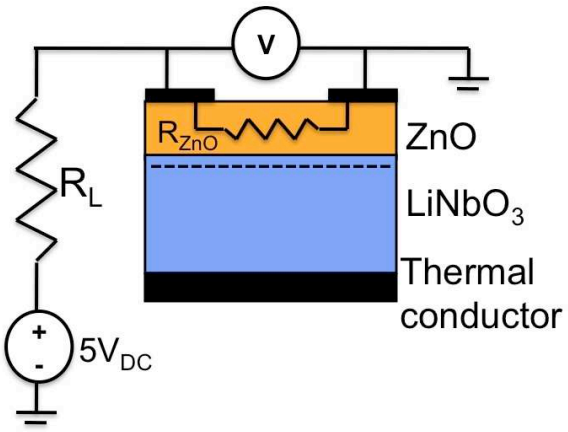

Figure 6.6: Voltage divider circuit used to characterize the pyroelectric response from LN/ZnO heterostructure

We monitored the voltage across R_{ZnO} while applying and removing a heat source to

the LN/ZnO heterostructure. Fig. 6.7 shows the response we recorded as a function of time, with timestamps denoting the application and removal of the heat source marked. The predicted behavior is evident in the plot, where the voltage across R_{ZnO} increases when the resistivity of the ZnO thin film is expected to increase.

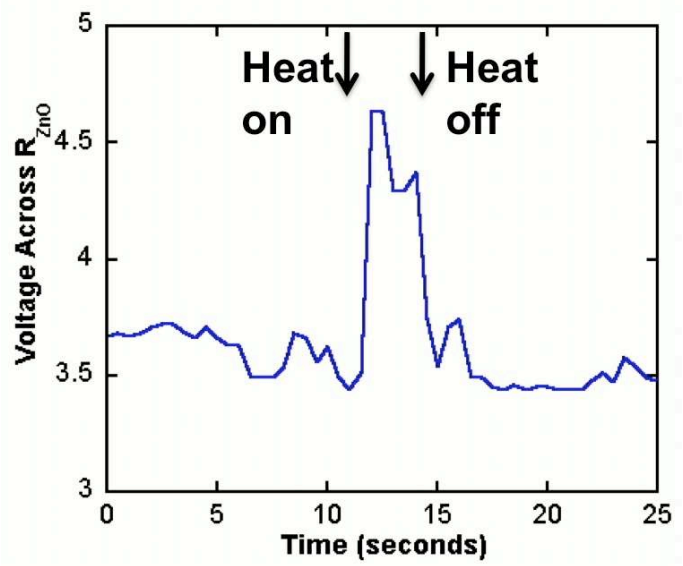

Figure 6.7: Voltage response in ZnO thin film on $LiNbO_3$ substrate tracking temperature stimulus

CHAPTER VII

Inquiry Based Teaching in an Introductory Semiconductor Device Course

It has been the experience of many primary instructors and teaching assistants that teaching an introductory course in semiconductor devices is a very challenging task. At the University of Michigan, this course is EECS 320. The majority of students admit to taking the course only because it is required for their degree, or because it is the only one that fits in their schedule. Once finished with the introductory course, very few undergraduates continue studying the topic in more advanced level courses. Many choose to move away from semiconductors to areas where they report being able to see applications more readily. While a few students become very interested in the field, and pursue advanced study or a career in semiconductors, many students with a high aptitude for the subject lose interest after their first encounter with the abstract foundations of semiconductor physics. We want to address the situation of students losing interest by introducting semiconductor device concepts in alternative ways.

Traditionally, a semiconductor device physics course will begin with the foundations of a blank piece of semiconducting material, and progress step by step building one piece at a time. The transistor is often introduced late in the semester. We encouraged

students to keep in mind that the transistor is a device with which they are already familiar, before they even set foot in the EECS 320 classroom. Then, we took an inquiry based approach to teaching the course, through which the students and the instructors asked many questions and guessed many answers before a lecture revealed the full picture. Our research question in this project was:

> Does inquiry based learning improve student interest, confidence, and performance in EECS 320 and similar courses based on abstract or unfamiliar foundations?

In this chapter we explain the inquiry based learning techniques used, we provide details of the course EECS 320 and our methodology, and our findings. We draw conclusions from both qualitative and quantitative data we collected. Our research question guided the methodology, in that we were addressing the interest and confidence levels of students separately, and we closely tracked student performance in the class.

7.1 Inquiry Based Learning

Inquiry based learning is a method through which the students are encouraged to ask and answer many questions about a new topic prior to in-depth discussion of the topic by an instructor[39]. The questions asked are often shaped by previous experiences or knowledge of the students; therefore, the answers will be connected with existing understanding in their background. Ideally, the new concept under study will be integrated into a network of concepts in the students' mind seamlessly; linked by the questions and answers that lead the student to full comprehension. It is expected that the concepts learned through an inquiry based approach will be retained better, since there will be several triggers to help recall them later[74].

The instructor can choose to provide some questions to get the students started with the inquiry, or can allow students to come up with the questions themselves. A combination approach can be used, where the instructor provides a broad question, and students then ask many detailed questions to divide the concept into smaller pieces. Students can then investigate each piece separately, and then combine their understanding into a larger picture in the end. Students can ponder or research the topic on their own, discuss with each other, and then finally with the instructor. It is important to recognize and to share with the students that some of the answers that the students come up with will be incorrect. Students may be apprehensive to use inquiry based learning, since the value of incorrectly answering seemingly impossible questions is not immediately clear to them.

An inquiry such as described here is often followed by a lecture that explores the new concept in depth. The questions and answers from students help the instructor construct this lecture by providing insight into the first reactions of the students, and their common misperceptions. All students, including those who did not make the common mistakes, can benefit from the misperceptions being addressed by the instructor. It is important to have the new concept detailed by the instructor in order to fill any gaps in understanding, and to give the students a chance to inquire further. The lecture can be followed by an opportunity for the students to revisit the initial questions, and increase their confidence in the new concept.

7.2 EECS 320: Introduction to Semiconductors

At the University of Michigan all electrical engineering students take an introductory course on semiconductor devices, EECS 320. The course typically follows basic circuits and classical mechanics courses. Therefore, instructors can expect students to be familiar with the end use of semiconductor devices in circuits (e.g.: transistor

circuits, diodes, photodetectors). However, students will most likely not have any familiarity with quantum mechanics, from which semiconductor devices use many results. The underlying physics governing the operation of the devices under study are, therefore, not yet intuitive to students in EECS 320. Furthermore, the course deals with the behavior of particles such as electron and holes, which make a hands-on demonstration of the concepts very difficult. In the electrical engineering curriculum at the University of Michigan, as with many other institutions, an introductory course in semiconductors tends to be the first time students encounter abstract concepts that are not conducive to directly exhibiting in a laboratory. This shift in the way students need to think about the concepts, combined with their unfamiliarity with the background material, makes EECS 320 a challenging course for both the instructor and the students.

Traditionally, EECS 320 or a similar course is taught with a bottom-up approach, where each concept builds on the previous one. The instruction begins with a blank piece of semiconductor, on which a diode is subsequently built. This is followed by a bipolar junction transistor or a field effect transistor. Therefore, students are introduced to transistors in the second half of the semester at the earliest. The disadvantage of this method is that the beginning of the semester features material that is not connected to any prior learning; therefore, many students decide early on that semiconductors are irrelevant and uninteresting.

Alternatively, an inquiry based approach can be employed in EECS 320 or a similar course. In this case, semiconductor devices with which the students are already familiar will be discussed in the beginning of the semester. After the initial discussion, the instructor and the students will ask many questions to investigate the inner workings of the devices, eventually unveiling the fundamental physics of the device

and the material. Students link new concepts to their previous courses in circuits as they acquire them. Fig. 7.1 depicts the traditional and the inquiry based methods of teaching an introductory semiconductors course. The order in which concepts are introduced is the primary difference in the overall organization of the semester.

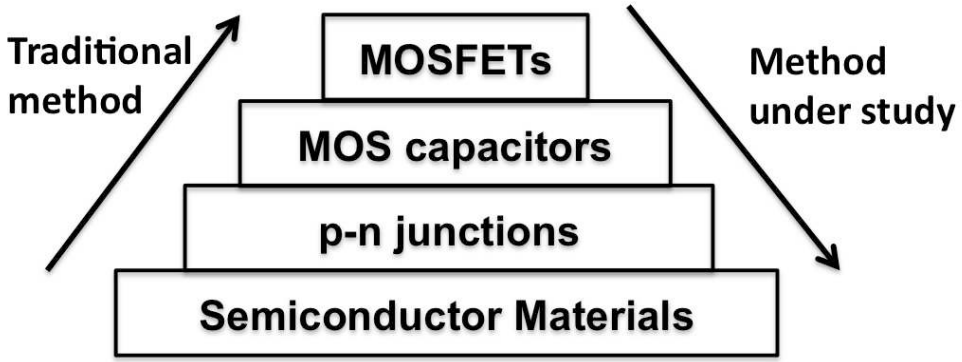

Figure 7.1: Schematic representation of the traditional approach and the inquiry based approach to teaching an introductory semiconductors course

7.3 Methodology

We identified inquiry based learning as a method likely to benefit students in EECS 320 by helping them link new concepts to those they have already learned. We expected this method to increase student comprehension and motivation, as well as to help students better retain their understanding. We then chose specific topics within the course syllabus, to introduce using inquiry. We chose to apply the change in teaching technique only to a fraction of the topics instead of reorganizing the class in its entirety. This way, we were able to introduce changes in a controlled and well organized manner. Furthermore, we were able to assess how well the students learned and retained the chosen topics compared to topics taught in the traditional way. The topics we chose for inquiry based learning were doping, p-n junction formation, and field effect transistor operation.

We used just in time teaching techniques to help students start asking and answering questions about the chosen topics. Before the class meeting where one of these topics was handled, students spent approximately 15 minutes taking an online quiz on the new concept. We communicated to the students that how they did on the quiz had no effect on their grade, or how we perceive their abilities. They were able to see the correct answers upon completing the quiz, and therefore had a chance to reflect on the answers. Quizzes were hosted on two different systems, um.lessons and CTools, both of which are parts of the infrastructure available to all University of Michigan instructors. There wasn't a discernible change in how easily the students were able to take the quizzes on the two sites; however, we found CTools helped instructors organize all class material under one site. The quizzes consisted of questions with varying levels of difficulty; they started with questions where the answer could be easily obtained by glancing at the book, and proceeded to questions where a deep understanding of the concept would be required for a full and correct answer. Each student could therefore find a question where he or she was guessing with help from previous classes and intuition.

Once in class, we invited the students to pretend that they are electrons or holes in a doped semiconductor, or in a p-n junction, or in a transistor. Each of these role playing sessions took place during a lecture time that coincided with the first introduction of the relevant structure. The students asked questions that led them to figure out how a charge carrier would behave in each of these situations. We provided the general question of where a charge carrier would go in the structure at hand. Students in turn asked more detailed questions such as "`What`forces are acting on the particle?"; "To what is particle attracted?"; "How heavy is the particle?"; "What kind of obstacles are in the particle's way?" Through these questions, and partial answers to them, the class realized that they indeed have some information on elec-

trons and holes already. The initial thought that these charge carriers and structures are completely unfamiliar to them is incorrect for most students. We followed the question, answer, and role playing session with a lecture where the behavior of each device was qualitatively explained. Quantitative descriptions came last.

We assessed the effectiveness of the inquiry based approach in three ways: We used written test results, surveys, and focus group interviews. We compared the performance of the students in mid-term and final tests for topics that were taught using inquiry and those using direct lecturing. In surveys we asked students about their confidence and motivation levels for the course in general, and for specific topics. A sample survey, conducted halfway through the semester, follows:

1. Please explain your reason(s) for enrolling in EECS 320.
2. (Rate from 1 to 5) How confident are you in the following areas?
    - Fitting equations/expressions on a data plot
    - Solving problems using iterative methods
    - Explaining the basic operation of a MOSFET
    - Explaining the properties of an MOS capacitor
    - Explaining the basic operation of p-n diodes
3. (Rate from 1 to 5) How likely are you to do the following?
    - Apply for internships related to semiconductors during this summer
    - Apply for undergraduate research programs related to semiconductors during this summer
    - Apply to a graduate program in semiconductors upon finishing your degree
    - Sell your textbook at the end of the semester

4. Please list the classes you are planning to take next semester.

5. What grade do you expect to receive in EECS 320?

Focus group interviews were conducted to get a deeper understanding of the students' perception of inquiry based learning and its effectiveness. Interview questions were on motivation and confidence levels, as well as on how well the students could recall topics from early in the semester. 10 students, selected at random, participated in the focus group. 7 students from a previous offering of EECS 320 formed a separate focus group that answered the same interview questions, therefore providing us with a control group. Questions used in these interviews follow. We must note that these questions only started the interviews, and then a moderated conversation continued for qualitative data collection:

1. How enthusiastic are you about the material in EECS 320?

2. How confident are you about the pre-requisite material leading up to this course?

3. Have you used any of the just in time teaching (JiTT) exercises? Did you find them helpful?

4. How confident are you about (material covered by JiTT)?

5. How confident are you about (the materials not covered by JiTT)?

6. How likely are you to take an internship/go to graduate school/participate in a research program related to semiconductors? Why? Why not?

7.4 Findings

We addressed our research question using the assessment techniques explained in the methodology, and we present the results in this section. Our research question was:

> Does inquiry based learning improve student interest, confidence, and performance in EECS 320 and similar courses based on abstract or unfamiliar foundations?

We collected both qualitative and quantitative data towards answering this question. We collected survey responses (quantitative), test scores (quantitative), and focus group interview responses (qualitative). Our analysis showed that students' test performance on a specific topic had a weak correlation with whether or not the inquiry based learning technique was used in teaching that topic. Students overall performed very well in the semester under study; however, our data are not sufficient to ascertain the reason for the high performance. Nevertheless we can learn a significant amount about the confidence and motivation of students from our data. This section details the results regarding student confidence and motivation.

We found that students in EECS 320 in the semester during which we implemented this project were highly interested in the subject matter upon completing the course. Students self-reported being `"interested"`or `"veryinterested"`in semiconductor device physics in the final survey of the semester. The results of this survey are presented in Fig. 7.2. Students' interest in the subject matter is very encouraging, since we also found that their interest level directly correlates to whether or not they choose to study semiconductors further. Fig. 7.3 shows combined survey results depicting the relationship between students' interest level and how likely they self-report to carry out specific actions such as taking an internship or applying to a graduate program related to semiconductors.

We found that students had a high level of confidence in the topics which they studied using inquiry based learning. Fig. 7.4 shows how confident students felt about transistor operation, and Fig. 7.5 shows how confident students felt about diode and MOS capacitor operation. All three of these topics were taught using an inquiry

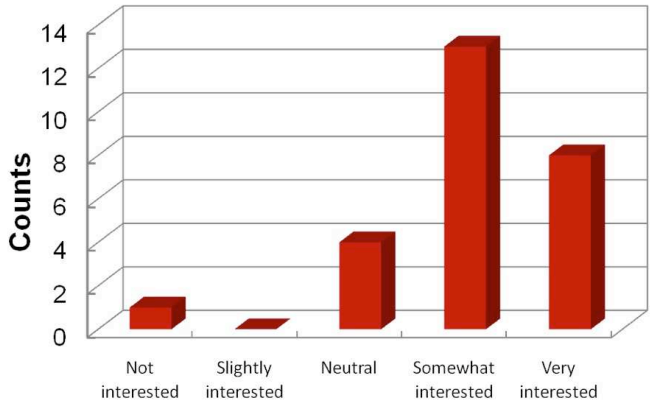

Figure 7.2: Students' interest level in semiconductor devices at end of the semester

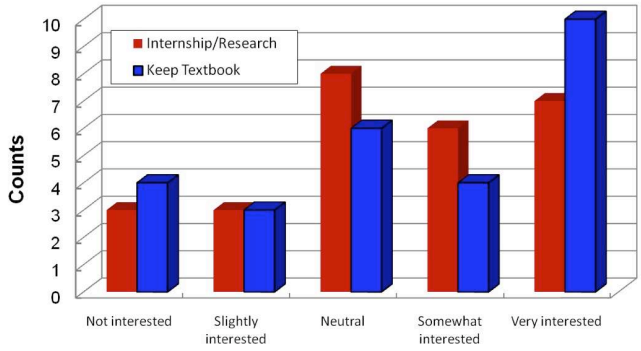

Figure 7.3: Students' interest level corresponding to their future actions

based approach. Students also directly reported finding the inquiry based learning activities (role playing in the classroom and just in time teaching units prior to class time) very useful. Fig. 7.6 shows the survey results where the majority of the class reported finding these activities valueable to their understanding of the material.

The quantitative survey results were corroborated by the qualitative data we collected using focus group interviews. Participants indicated that the activities helped them master the topics by digging into the physics first at their own pace, becoming curious, and looking forward to class time. The common themes of the responses we collected from interviews were:

- Students were not confident that they had sufficient preparation for EECS 320,

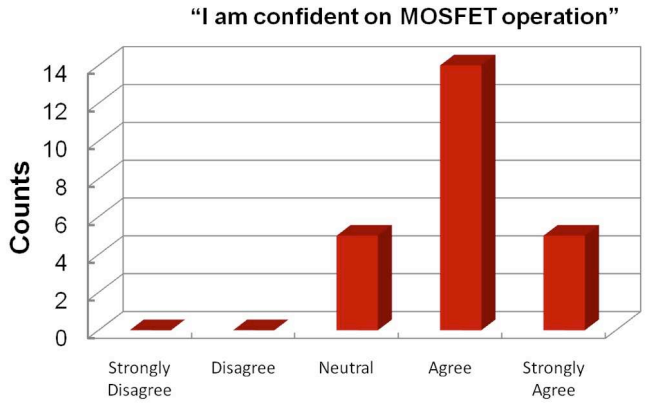

Figure 7.4: Students' confidence level in field effect transistor operation

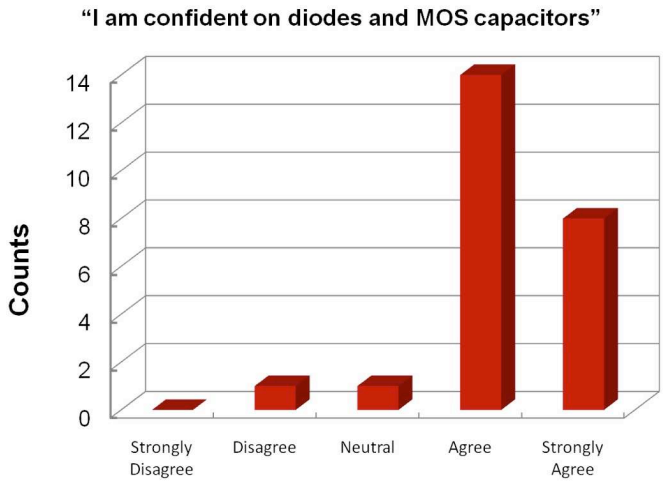

Figure 7.5: Students' confidence level in p-n diode formation and MOS capacitor operation

even if they did well in the pre-requisite courses.

- The just in time teaching and role playing activities helped them become familiar and confident with the chosen topics.

- At the end of the semester, they were able to demonstrate that they retained their undestanding of p-n diode formation, which was studied in the first several weeks of the semester.

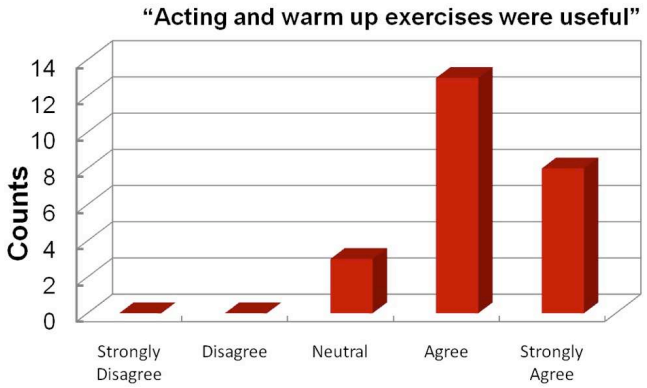

Figure 7.6: Students found the inquiry based learning activities valuable

- They were interested, but not likely to take internships in the semiconductors industry.

Several direct quotes from students collected in the focus group interviews give us further insight into the response of the class to the newly introduced teaching technique:

- "I was ready to learn, and somewhat curious when I arrived in lecture following an online quiz."
- "I understood the material better in cases where I was initially wrong in my guess."
- "It all came together and clicked when we acted out the MOSFET."
- "I got in the head of an electron."

7.5 Conclusions

We implemented and evaluated changes in the method for teaching an introductory semiconductor device course, where we used inquiry based teaching and learning

techniques. Our hypothesis was that the new technique would improve student performance, confidence and interest in the subject matter. Our data were inconclusive on the effect of inquiry based learning on performance, but showed that inquiry based learning increased students' interest and confidence. Through surveys and interviews we learned that the inquiry based approach helps students visualize abstract concepts, come up with their own narrative of complex and unfamiliar topics, and to retain their understanding well. New concepts were successfully linked to the students' prior knowledge, therefore, they were more easily applied and remembered.

Student motivation and interest emerged as very important factors in near-term recruitment for the semiconductors field. We found that the immediate decisions made by students, such as their summer plans and subsequent course choices, were affected by whether or not they found semiconductors relevant to their career. Teaching EECS 320 or an equivalent course effectively is therefore crucial to not only our program, but to the field of semiconductor physics in general. We learned that the first encouter students have with the topics is an opportunity to get them curious and interested, rather than intimidated. Several students indicated disappointment in discovering semiconductors too late in their undergraduate career. Since they had heard from their peers that EECS 320 is a very difficult and dry course, they delayed taking it until their senior year. Once they found that they were in fact interested in studying semiconductors further, they no longer had the chance to take the more advanced courses offered before they graduated. Therefore, advising students to carefully plan their course schedules in order to keep their options open is also important for recruitment of highly motivated students into the field.

It is important to investigate a newly applied teaching method over several offerings of the course in order to get a full understanding of its effectiveness. We can benefit

from studying inquiry based teaching and learning techniques repeatedly, and by applying them to a larger portion of EECS 320, as well as to similar courses. The assessment techniques for confidence and motivation are sufficiently established, and can be repeated in their current form for following semesters. Assessing effects of a new technique on student performance, however, is very difficult, and it is a research topic for many educators. This is where comparing the performance of students from many different semesters can be helpful, where their test scores and subsequent course and career choices can help us understand the full benefits of inquiry based learning.

CHAPTER VIII

Conclusions

8.1 Ferroelectric Materials

Ferroelectric materials exhibit multiple desirable properties such as switchable polarization, piezoelectricity, pyroelectricity, and electrooptic effect. Additionally, they have high dielectric constants, which make them potential materials in several electronics applications. The current uses of ferroelectrics include memory devices in smart cards, video game cards, power meters, etc., as well as microwave devices that exploit the electrooptic effect and the DC tunable dielectric constants in ferroelectrics. The application field of ferroelectrics can be broadened via integrating them with semiconductor materials and applicable processes. Such integration will lead to multifunctional devices such as memory-transistors, sensor-transistors, and DC tunable filters for microwave applications.

We studied ferroelectric perovskite materials in thin films that we deposited using pulsed laser deposition and sol-gel processing. We established the ability to deposit thin films of $Pb(Zr,Ti)O_3$ and $BaTiO_3$ in the desired perovskite crystal structure using pulsed laser deposition and sol-gel processing. Polycrstalline perovskite films with no strong preferential orientation were obtained on several different substrates. Sol-gel processed films on $Pt/SiO_2/Si$ substrates showed ferroelectric polarization in

a repeatable way, allowing further processing of the thin films into capacitor devices. The ferroelectric behavior was evident in capacitance-voltage and polarization-electric field measurements, which are detailed in Chapter III. We studied ferroelectric materials further using single crystal bulk substrates of $LiNbO_3$, which provided a well characterized template for heterostructures in this project.

8.2 The Semiconductor Zinc Oxide

Zinc oxide is a very attractive semiconductor material for many reasons, including its large bandgap (3.34eV at room temperature), its large exciton binding energy (60meV at room temperature), and its compatibility with other oxide materials. The latter is of particular importance to this project, where we sought a semiconductor material that can be integrated with ferroelectric materials. Since most ferroelectrics are oxide materials, the chemical and thermal compatibility is seldom as high as it is with ZnO. We deposited ZnO thin films by pulsed laser deposition (PLD), through which polycrystalline material was achieved. We were able to deposit c-plane ZnO films on ferroelectric materials, which allowed us to observe the structural and electrical characterstics of the semiconductor in contact with the functional oxide. The structural characteristics of ZnO on ferroelectrics were studied using x-ray diffraction. We found that polycrystalline ZnO films resulted on sol-gel processed PZT, where a very high degree of highly preferential orientation resulted on bulk $LiNbO_3$. The electrical properties of ZnO on ferroelectric substrates was comparable to control films on sapphire. This was encouraging, since sapphire is regarded as the benchmark substrate material for studying ZnO growth and deposition.

We further studied ZnO growth using molecular beam epitaxy (MBE) on several substrates. The goal of the epitaxial growth was to control the orientation of ZnO, such that the spontaneous polarization of the material would be in-plane. Coltrolling

the direction of the polarization is desirable for devices such as surface acoustic wave devices, and thin film acoustic resonators. Additionally, it is beneficial to have control over the polarization charge for devices that use superlattices. We achieved non-polar m-plane growth of ZnO on MgO, as verified by tranmission electron microscopy and x-ray diffraction studies. The polar c-plane of ZnO was therefore parallel to the substrate.

8.3 Ferroelectric/ZnO Heterostructures

Heterostructures of ferroelectric materials with semiconductors are desirable for multifunctional devices, and for allowing ferroelectrics to penetrate the electronics markets more effectively. Our goal in this project was to create heterostructructures where we can modulate the semiconductor layer through the ferroelectric polarization charge. Towards this goal we needed high quality, low defect density junctions at ferroelectric/semiconductor interfaces. Interface issues have been the most significant inhibiting factor to the integration of ferroelectrics with semiconductors so far, because growing ferroelectric oxides on traditional semiconductors often results in an amorphous interfacial layer. This amorphous layer decouples the ferroelectric polarization charge from the semiconductor, therefore reducing the efficiency with which modulation can occur. Additionally, it is very difficult to grow or deposit traditional semiconductors on top of ferroelectric oxides; therefore, there is a significant obstacle to devices that use superlattices. In this project we used an alternative material, ZnO, which is emerging as a serious contender as a wide-bandgap semiconductor. We took advantage of the high level of compatibility ZnO has with ferroelectric materials as far as their chemical, structural, and thermal properties are concerned. We fabricated heterostructures that showed satisfactory structural and electrical properties in order to demonstrate modulation of the ZnO conductivity through the ferroelectric polarization charge.

We fabricated Pt/PZT/ZnO capacitors using sol-gel processed PZT and pulse laser deposited ZnO. The modulation of ZnO was characterized through capacitance-voltage measurements, where we observed hysteretic behavior with a 3.5V memory window. The hysteresis was preserved in AC conductance behavior of the capacitors, as well, where the conductance changed by an order of magnitude depending on the polarization direction in the ferroelectric layer. We built a prototype series resistor-inductor-capacitor circuit using the Pt/PZT/ZnO capacitor, where the frequency response changed depending on the ferroelectric polarization. A shift of 30kHz was achieved in the resonant frequency of the circuit.

We sought a higher level of structural compatibility than PZT (a perovskite) and ZnO (a hexagonal structure) offered. Therefore, we fabricated heterostructures using the hexagonal ferroelectric $LiNbO_3$. We used Hall effect measurements on $LiNbO_3$/ZnO heterostructures to directly observe the modulation of the carrier concentration in the semiconductor layer. We deposited varying thicknesses of ZnO films on bulk $LiNbO_3$ substrates using pulsed laser deposition. The effect was readily discernible in thin layers, where the measured carrier concentration in ZnO changed by over an order of magnitude depending on the polarization charge direction in the ferroelectric substrate. The effect was especially visible when the ferroelectric charge provided a negative sheet charge density at the interface, therefore causing depletion in the n-type ZnO layer. The high background concentration in the as-deposited ZnO layers (typically 10^{17}) made accumulation difficult to observe. We used a basic voltage divider circuit to demonstrate the effect of depletion on the resitivity of the ZnO layer, and also to exploit the pyroelectric effect in $LiNbO_3$. Through the pyroelectric effect, we expect the polarization charge to increase with increasing temperature, and therefore further depletion of the ZnO layer. This expectation was confirmed when

we observed that the resistance provided by the ZnO thin film increased when we applied heat to the $LiNbO_3$ substrate.

8.4 Future Work

This project establishes the proof of concept that we can modulate charge density in a semiconductor through the polarization charge in a ferroelectric material. This step puts us closer to achieving ferroelectric/semiconductor integration fully, and it encourages us to investigate the interfaces between these materials further. There are three major directions in which this work can expand.

1. Developing a full understanding of ferroelectric/semiconductor band line-ups: The band diagrams presented here start with an electron affinity approach. They do not take into account deviations from the electron affinity approach that could result from defects, surface absorption of charges, and variations in the polarization charge densities. Band discontinuities between ferroelectrics and semiconductors are not well understood, even though such understanding is vital to designing successful devices using these materials. Fig. 8.1 [75] shows a sample data set from a report by Bersch et. al., where the authors studied band offsets of non-ferroelectric high-k dielectrics interfaced with Si. X-ray photoemission spectroscopy (XPS) is a method through which significant insight into the band offsets in these heterostructures, as well as structures of interest to us. The main difference in the proposed study is the inclusion of polar charges, and the built-in electric field resulting from the polar charges.

2. Designing and fabricating field effect transistors with ferroelectric gate dielectrics and ZnO channels: Sensing, memory, and electronics applications can all benefit from a successfully integrated ferroelectric gate dielectric into a thin film

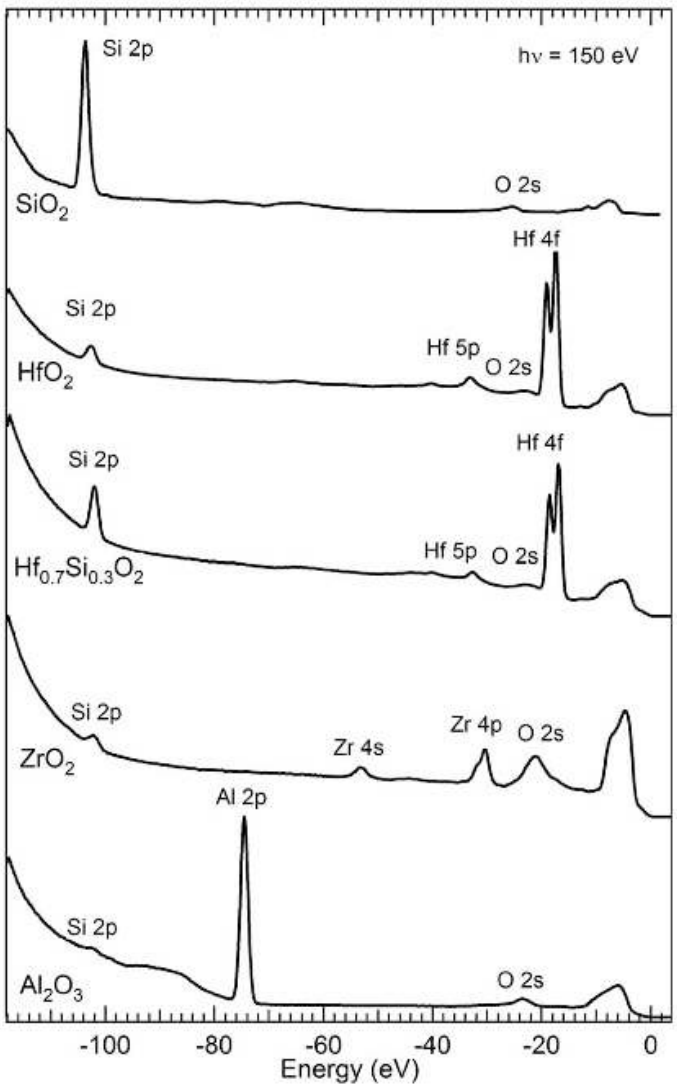

Figure 8.1: XPS data for various oxide films, by E. Bersch, et al. [75]

transistor. Using ZnO as the channel material makes it possible to envision very low defect density interfaces where the gate and the channel meet. Therefore, we can use the ferroelectric polarization charge to modulate the channel conductivity, as proven possible in this project. We can exploit the multifuncitonal nature of ferroelectric materials when we incorporate gate stacks with high pyroelectric or piezoelectric coefficients. We can therefore turn the transistor on and off based on an external stimuli of heat, pressure, etc.

Achieving the desirable gate modulation requires the ability to grow high quality

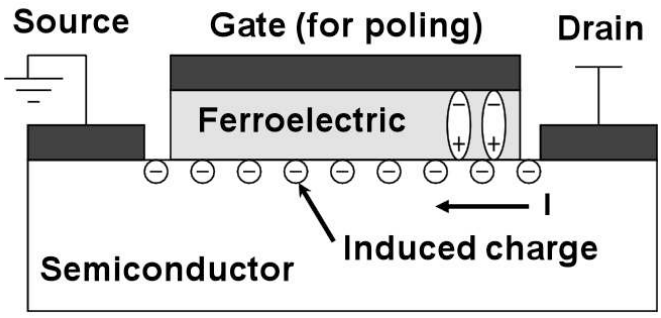

Figure 8.2: A ferroelectric field effect transistor, where the proposed semiconductor channel material is ZnO

thin films of ferroelectric materials on ZnO. We propose a study to optimize growth very low defect density ferroelectric thin films on ZnO to expand on the growth and deposition studies in this project. Ferroelectrics have already been grown on semiconductors with buffer layers, and with careful refining of growth conditions[50]. Further work is required to develop the ability to grow them on ZnO, ideally without the need for buffer layers that could decouple the polarization charge from the semiconductor. Challenges with the repeatability of high quality ferroelectric thin film growth also need to be addressed; and using ZnO in the heterjunction is expected to make a significant difference towards that goal.

3. Developing ferroelectric/semiconductor confined structures and superlattices: We seek a high level of control over the band structure of sets of films we use in the design of new devices. The ability to precisely describe the band offsets of ferroelectric/semiconductor heterostructures, and that to grow thin ferroelectric films on ZnO will open the path to our next proposed research direction. The structural and chemical compatibility of ZnO with ferroelectrics makes it a good candidate for creating multiple heterojunctions or superlattices of alternating ferroelectric and ZnO layers. The switchable polarization in the ferroelectric layer determines the direction of the band bending in ZnO, where the thick-

ness and background carrier concentration determine the amount by which the bands will bend. Fig. 8.3 and Fig. 8.4 show a simple band diagram describing this phenomenon with opposing polarization directions in the ferroelectric layer.

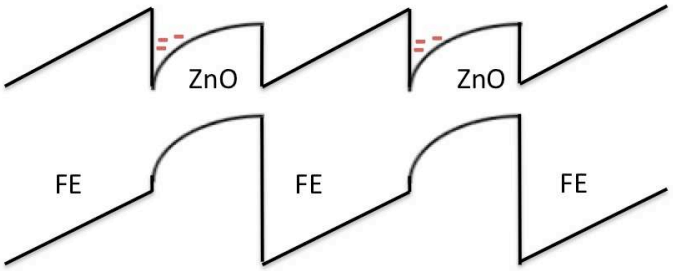

Figure 8.3: Band diagram of a ferroelectric/ZnO multijunction structure

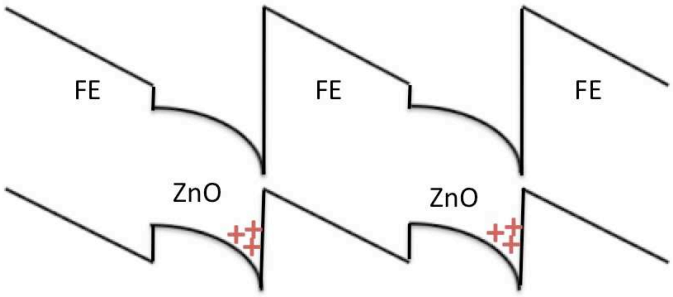

Figure 8.4: Band diagram of a ferroelectric/ZnO multijunction structure with switched polarization

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