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Stress test measurements of lattice-matched InAlN/AlN/GaN HFET structures

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InAlN/GaN heterostructures offer some benefits over existing AlGaN/GaN heterostructures for HFET device applications. In addition to having a larger bandgap than typical AlGaN compounds used in HFET devices (with Al < 30%), which leads to better confinement and subsequent larger power carrying capacity, InAlN can be grown lattice-matched to GaN, resulting in strain-free heterostructures. As such, lattice-matched InAlN provides a unique system wherein the reliability of the devices may exceed that of the strained AlGaN/GaN devices as a result of being able to decouple the hot electron/hot phonon effects on the reliability from the strain related issues. In this work, we subjected lattice-matched InAlN-based HFETs to electrical stress and observed the corresponding degradation in maximum drain current. We found that the degradation rates are lower only for a narrow range of moderate gate biases, corresponding to low field average 2-dimensional electron gas (2DEG) densities of 9–10 $\times$ 10^{12} cm^{-2}. We propose that the degradation is attributable to the buildup of hot phonons since the degradation rates as a function of electron density generally follow the hot phonon lifetime *versus* electron density. This provides evidence that hot phonons have a significant role in device degradation and there exists an optimal 2DEG density to minimize hot phonon related degradation. We did not observe any correlation between the degradation rate and the gate leakage.

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1 Introduction GaN based heterostructure field effect transistors (HFETs) exhibit remarkable performance in the high frequency-high power arena. Currently, research is focused on substitution of the AlGaN barrier with an $In_xAl_{1-x}N$ barrier [1–5]. The reason is twofold. First, InAlN can be grown lattice-matched to the GaN although the exact composition for lattice matching is not precisely known due to the controversial values of the lattice parameters of InN, the bowing parameter of InAlN, and the strain state of the underlying GaN [4, 5]. Nevertheless, the use of InAlN is important since the strain typically present in AlGaN-based HFETs could be eliminated, which bodes well for reliability of the devices [6–8]. Second, the difference in spontaneous polarization between GaN and InAlN provides these devices with a high density 2DEG (>2.5 $\times$ 10^{13} cm^{-2}), which translates to higher current densities compared to AlGaN-based HFETs. Although touted as a blessing, recent measurements of hot phonon lifetimes (τ_{ph}) in InAlN-based structures have provided evidence for an optimal 2DEG density [9], lower than the density attainable with an InAlN HFET, where the phonon lifetime, τ_{ph}, is at a minimum, apparently due to the phonon–plasmon coupling [10, 11]. The performance, and we believe the reliability, of HFETs with GaN channels will depend on the 2DEG density.

Figure 1 shows the measured τ_{ph} for bulk GaN (circles) and for a number of GaN-based 2DEGs (utilizing AlGaN barriers – triangles, and utilizing InAlN barriers – upside down triangles). The existence of an optimal 2DEG density means that that τ_{ph} increases at electron densities greater or less than that at phonon–plasmon resonance. We aim to demonstrate that the measured τ_{ph} correlates with the reliability as a function of electron density, measured in

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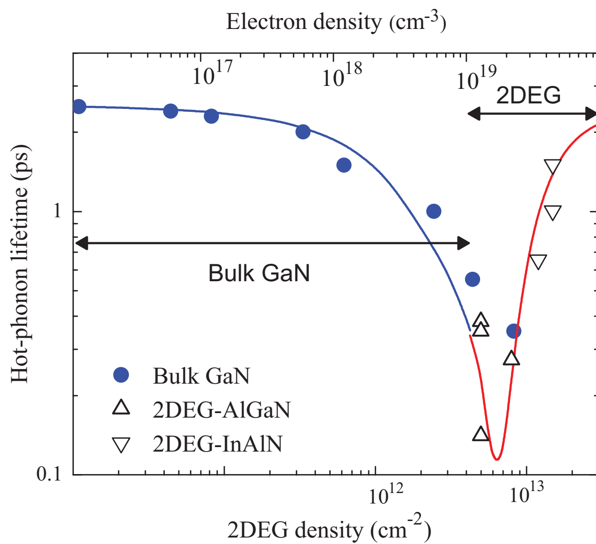

Figure 1 (online color at: www.pss-a.com) Measured hot phonon lifetimes *versus* electron density for 3D (solid circles) and 2DEGs (open triangles) in GaN at low fields. The existence of a minimum around $6.5 \times 10^{12}\,\mathrm{cm}^{-2}$ is attributed to the phonon-plasmon resonance. From Ref. [9].

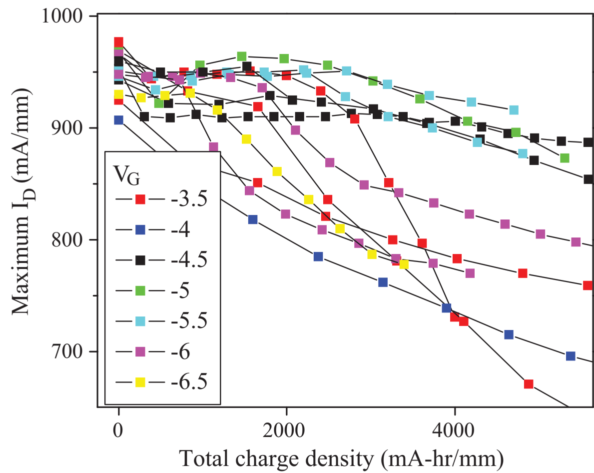

Figure 2 (online color at: www.pss-a.com) Change in the maximum drain current as a function of the total charge that has passed through the devices. Qualitatively, one can see that the lowest and highest gate biases tend to be associated with the most severe degradation.

terms of the degradation rate of devices subjected to high drain bias. In this work, we use a gate bias to control τ_{ph} through control of the average electron density in the channel.

2 Experiment InAlN/AlN/GaN HFET structures were grown on sapphire in a low-pressure custom-designed Organo-Metallic Vapor Phase Epitaxy (OMVPE) system using trimethylgallium (TMGa), trimethylaluminum (TMAl), trimethylindium (TMIn), and ammonia as the Ga, Al, In, and N sources, respectively. The layer consisted of a 250 nm AlN initiation layer, 3 μm of undoped GaN, a 1 nm AlN spacer layer, a 20 nm $In_{0.15}Al_{0.85}N$ barrier layer, and a 2 nm GaN cap layer. The HFETs employed Ti/Al/Ni/Au Ohmic and Pt/Au Schottky contacts. Details of the growth procedure as well as the fabrication can be found in Ref [4].

Unpassivated (90 × 2 μm) devices were subjected to electrical stress: high bias ($V_{DS} = 20$ V) was applied in the dark for up to 20 h at room temperature, and various gate voltages were used to control the electron density in the channel, which was initially measured using a gated Hall bar. During the stress, we monitored the drain current as well as the gate leakage, and every hour or half hour we measured I_D vs. V_{DS} in order to quantify the amount of degradation.

3 Results and discussion We observed a degradation rate dependent on the electron density in the channel (experimentally accessible through the applied gate bias) in such a way as to follow the hot phonon lifetime of Fig. 1. This implies that the hot phonons do in fact represent an effective degradation mechanism, and additionally that the application of gate potential allows us to change the electron density, in turn changing τ_{ph} and subsequently the degradation rate. In Fig. 2, we plot the maximum drain current (I_{Dmax} at $V_G = 0$ V) throughout the course of stressing for devices which have been stressed at $V_{DS} = 20$ V with V_G varied from −3.5 to −6.5 V. We plot I_{Dmax} not as a function of time at which stress has been applied, but *versus* the total amount of charge that has passed through the device. This way, we can fairly compare devices which have been subjected to low and high levels of current. One can see from Fig. 2 that the greatest change in I_{Dmax} occurs for the devices subjected to the highest and lowest gate biases, corresponding to the lowest and highest average electron densities in the channel.

Next, we quantified the amount of degradation by calculating the percent change in I_{Dmax} after an amount of charge of 2000 mA h/mm had passed through the device. We plot this number as a function of the low field electron density, measured for the gated Hall bar, in Fig. 3. We see that the smallest amount of degradation occurs for devices subjected to gate voltages of −3.5 to −4.5 V, corresponding to electron densities around $1 \times 10^{13}\,\mathrm{cm}^{-2}$. The electron density expected to be associated with the shortest τ_{ph} is around 6.5×10^{12}, as seen in Fig. 1. Our stress measurements show the minimum in degradation for slightly higher electron densities. This can be understood in light of the fact that, the position of the phonon–plasmon resonance shifts as the electric field in the channel increases. As the field increases, the electrons gain energy, therefore spreading the electron density over a larger volume, decreasing the "bulk" density of the electrons in the channel.

Thus, when the channel is subjected to high fields, the resonance is achieved at a larger electron density than the optimum value measured at low fields. Such a phenomenon has been directly observed in gateless channels and reported in Ref. [9].

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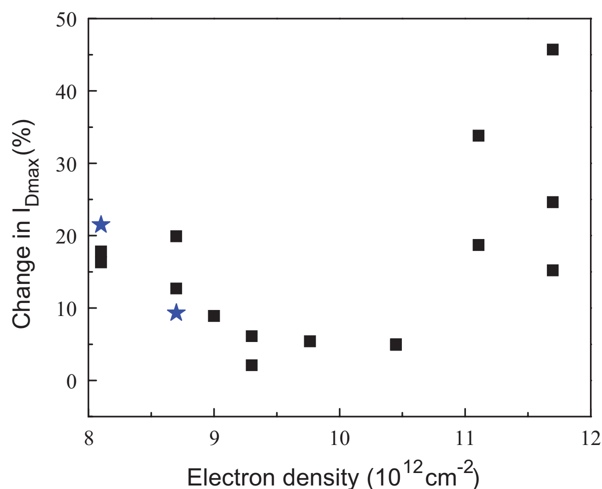

Figure 3 (online color at: www.pss-a.com) Change in maximum drain current (at $V_G = 0$ V) after subjecting devices to high field electrical stress. The change is given for devices which have passed 2000 mA h/mm of current. The electron density is controlled by the gate bias. The stars represent devices that were stressed using a reduced drain voltage in order to maintain $V_{DG} = 24.5$ V. The trend qualitatively follows the hot phonon lifetime presented in Fig. 1.

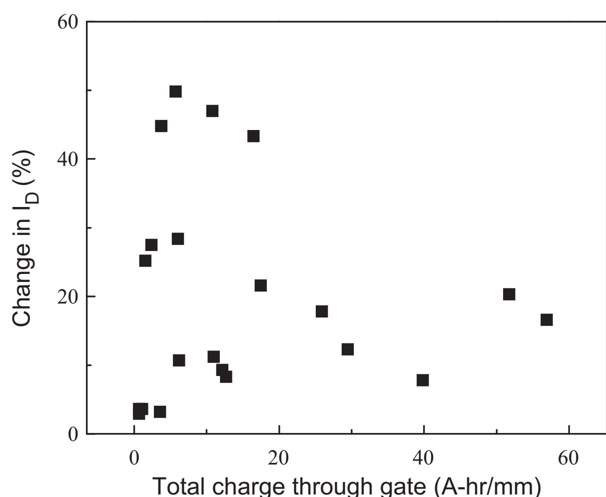

Figure 4 The total change in drain current for all devices in this study *versus* the total charge passed through the gate. The lack of any discernable dependence of degradation on the gate leakage indicates that the primary degradation mechanism is not related to the gate leakage.

To ensure that degradation is in fact attributable to a hot phonon related mechanism as opposed to a gate leakage mechanism, we plot in Fig. 4 the total change in I_{Dmax} after stress *versus* the total amount of charge that has leaked through the gate during the stress (Fig. 4). No systematic degradation with the gate leakage is found; some devices suffer high degradation with little gate leakage, some do little degradation with high leakage. The lack of expected dependence leads us to conclude that gate leakage is not a major contributor to the degradation for these devices.

Additionally, we reduced the drain voltage from 20 to 18 V in order to ensure that the total drain-to-gate voltage was not responsible for the degradation in devices with high V_{DG} (stars in Fig. 3). Under these stress conditions, the V_{DG} was maintained at 24.5 V, which is the same used when degradation is minimized. The fact that under these conditions we still observe high degradation indicates that the high V_{DG} is not contributing to the degradation.

4 Conclusion We investigated degradation in lattice-matched InAlN-based HFETs through changes in I_{Dmax} after subjected to long-term stress at room temperature. We observed a minimum degradation for devices subjected to gate biases which correspond to electron densities near the expected phonon–plasmon resonance density. Therefore, we conclude that the hot phonons constitute a significant degradation mechanism and that fast removal of hot phonons is crucial for achieving high reliability of GaN-based HFETs, regardless of the barrier used.

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