ANALOG TO DIGITAL CONVERSION TECHNIQUES FOR

NANOMETER CMOS

by

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LIST OF ABBREVIATIONS

ADC   analog-to-digital-converter

BER   bit error rate

CLSA   current latch sense amplifier

CMFB   common mode feedback

CMOS   complementary metal-oxide-semiconductor

DAC   digital-to-analog-converter

DNL   differential non-linearity

DSP   digital signal processor

ENOB   effective number of bits

FET   field effect transistor

GS/s   giga-samples per second

IC   integrated circuit

INL   integral non-linearity

LDO   low drop-out regulator

LSB   least significant bit

LTE-A   Long Term Evolution Advanced

MDAC   multiplying digital-to-analog-converter

MS/s   mega-samples per second

RMS   root mean square

SAH   sample and hold

SAR   successive approximation register

SFDR   spurious free dynamic range

SNDR   signal-to-noise and distortion ratio

SNR   signal-to-noise ratio

SoC   System on Chip

SOI   silicon on insulator

TAH   track and hold

ABSTRACT

ANALOG-TO-DIGITAL CONVERSION TECHNIQUES
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Jorge Pernillo

Chair: Michael P. Flynn

This work investigates new approaches to analog-to-digital conversion that are suited for end-of-the-roadmap CMOS, and which also deliver orders-of-magnitude improvements in speed and energy efficiency. We break analog-to-digital conversion down to its essence and simplify the process of analog-to-digital conversion to its most basic form. This allows us to take advantage of the tremendous digital capability of nanometer processes and then implement the analog circuitry in the simplest way. We propose three ADC structures that enable high performance with low transistor gain and, low-precision comparators aided by digital processing.

First, a 1.5GS/s 7b flash ADC is presented. We advance a comparator redundancy technique by employing random and deliberate mismatch to set the comparator thresholds and eliminate the need for a low-impedance high-precision resistor reference ladder. Unusually, the proposed technique exploits large random variation in comparator offset. This enables the use of low precision dynamic comparators that can be optimized

for speed. The ADC prototype, fabricated in 90nm digital CMOS process, achieves an ENOB and SFDR of 6.05 bits and 46.6dB at Nyquist and consumes a total of 204mW from 1.2V analog and 0.9V digital supplies.

Second, a 9b 1GS/s two-stage pipeline ADC is presented. This architecture achieves high performance with a low-gain op-amp and low accuracy comparators. A reduced MDAC gain relaxes the op-amp gain and bandwidth requirements and trades MDAC output swing for reduced op-amp power. This technique is assisted by a comparator redundancy scheme that decouples the 2nd stage sub-ADC performance from comparator matching requirements. A simple code-search algorithm calibrates the redundancy-based sub-ADCs and at the same time eliminates the need for complex calibration techniques to correct ADC errors from finite op-amp gain, offset and non-linearity. Digital trimming of a delay chain eliminates mismatch in the sampling paths to provide a simple, low power alternative to a dedicated front-end S/H. The prototype ADC, fabricated in a 45nm SOI-CMOS process, achieves an ENOB and SFDR of 7.4 bits and 52.7 dB at Nyquist and consumes a total of 27mW from a 1V supply.

Finally, a 9b 2GS/s two-times interleaved pipeline ADC is described. This architecture leverages op-amp sharing as well as 2nd stage sub-ADC sharing between two time-interleaved MDACs to reduce power and area. Furthermore, this technique eliminates the need for complex calibration algorithms that correct ADC errors due to gain and offset mismatch between channels. Digital trimming corrects for timing mismatch between channels. The prototype ADC, fabricated in a 45nm SOI-CMOS process, achieves an ENOB and SFDR of 7.07 bits and 56 dB at Nyquist and consumes a total of 45mW from a 1V supply.

CHAPTER 1 Introduction

1.1 Background

The goal of this research is to develop new approaches to analog-to-digital conversion that are suited for sub-micron, digital complementary metal oxide semiconductor (CMOS) processes. Semiconductor economics dictate that digital CMOS processes follow the trend towards finer line-widths to increase the number of transistors that can be fabricated on a silicon wafer. This results in increased production efficiency at finer line-widths [1] as illustrated in Figure 1-1.
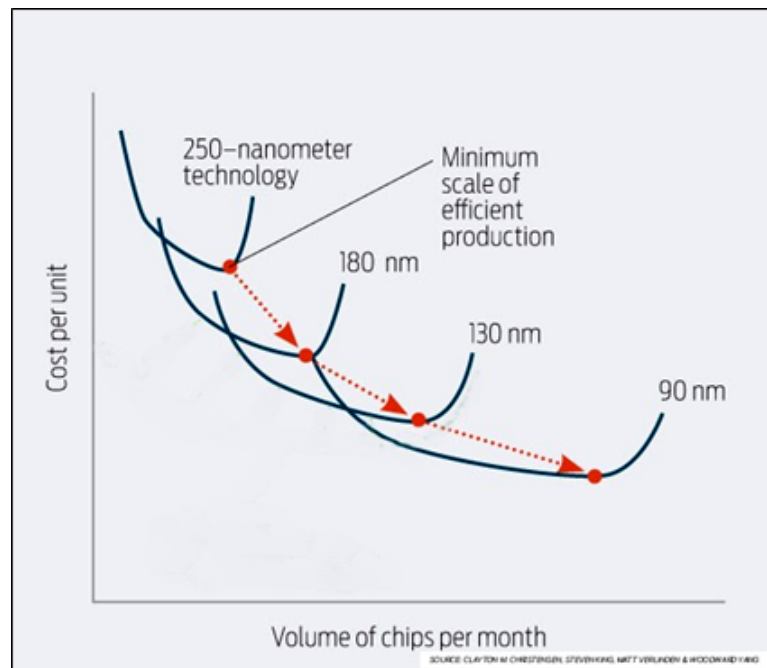
Figure 1-1 Production efficiency and scaling in the semiconductor industry [1].

Decreasing line-widths are accompanied by increased transistor speed, density and power efficiency all which are conducive to system-on-chip (SoC) integration of digital

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integrated circuits (ICs). SoC design (see Figure 1-2) is a concept where chips are designed with increasing amounts of functionality to reach a point where one chip represents an entire "system". One chip means lower manufacturing costs, lower power consumption, smaller area and enhanced performance.

Figure 1-2 System on Chip (SoC) technology combines multiple chips into one chip.

However, the trend towards finer line-widths is not conducive to the advancement of analog integrated circuit design where accuracy requirements are more stringent. Finer line-widths lead to increased process variation. When coupled with the reduction in power supply levels, short-channel effects and temperature gradients, this makes robust analog circuit designs difficult to achieve. The drawbacks of technology scaling are more significant for analog circuits and impede the advancement of mixed-signal SoCs. Therefore, analog chips are manufactured using tailored analog manufacturing technologies that are more expensive than standard digital manufacturing technologies.
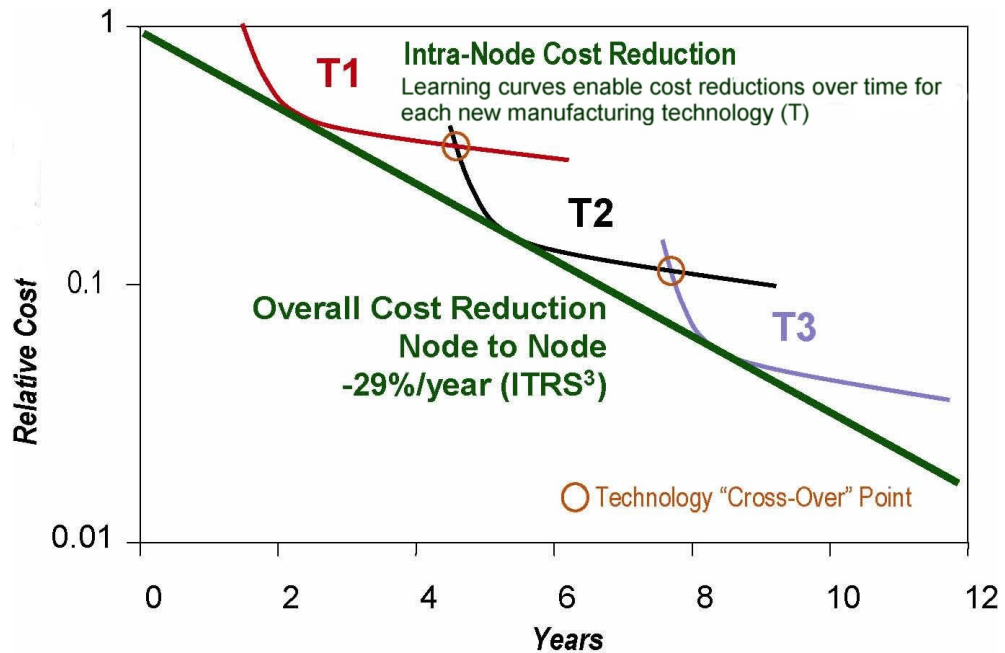
Figure 1-3 Relative Cost decreases with time and technology introductions (T) [2].

NOTE: As a given technology matures, it becomes the most cost effective solution until the next technology introduction passes the "Cross-Over" point.

SoCs can be implemented in older digital manufacturing technologies. However, although this solution allows proven analog design techniques to be employed, it is neither as cost effective (see Figure 1-3) nor does it scale with volume (see Figure 1-1). Reducing the complexity of analog functions by substituting them with digital processing greatly reduces the required accuracy. This concept is explored in this work and applied in the context of high-speed analog-to-digital converters (ADCs).

1.2   Analog to Digital Converters for Broadband Communications

Future high-speed communications systems and emerging communication standards require analog to digital converters with both high bandwidth and high dynamic range. For example, emerging broadband wireless technologies such as LTE-Advanced (LTE-A) [3] and 60GHz [4] will deliver Giga-bit per second data rates as early as 2015 and

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require Giga-Sample per second (GS/s) ADCs with resolution of 8 bits and above. Incorporating GS/s ADCs will enable sufficient receiver performance to deliver these data rates.

In current macro-cell base stations, a receiver is required for each channel and the RF-band-pass filtering, channel-selection and image rejection are all done in analog domain. Furthermore multiple analog-to-digital converters (ADCs) and digital signal processors (DSPs) are required as shown in Figure 1-4. Furthermore, since a receiver is duplicated once for each channel, this results in an overly redundant design. Also, each added analog stage in receiver increases cost due to yield and therefore the sooner the signal is digitized the better.
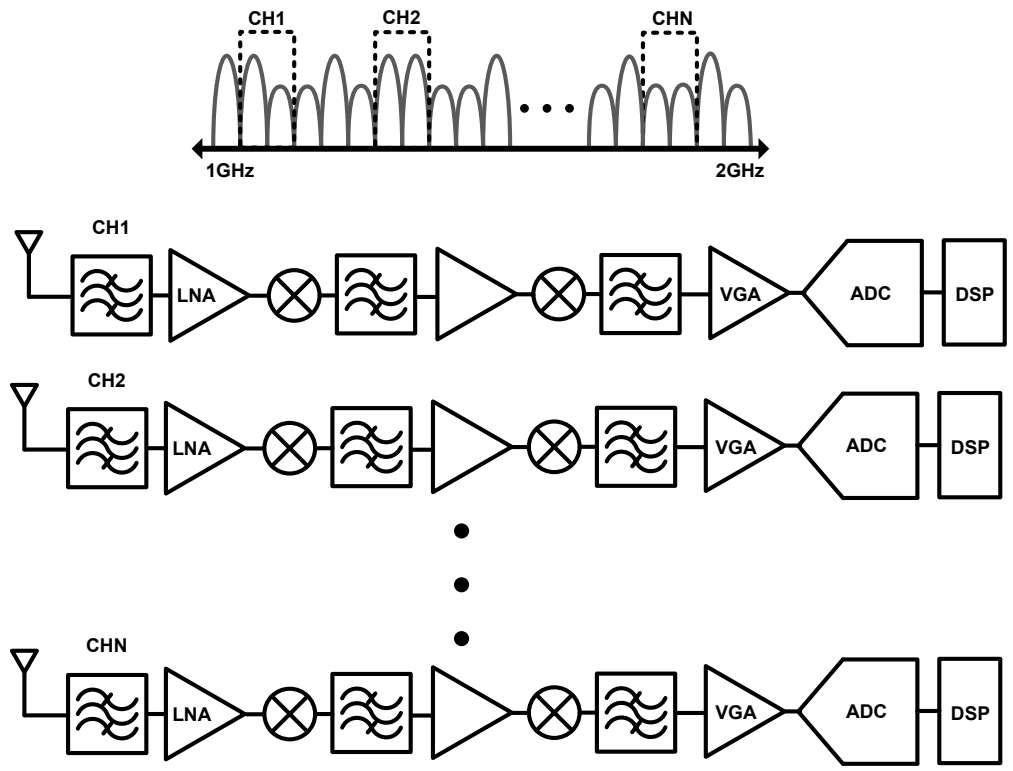
Figure 1-4 Example of a multi-channel receiver for cellular base stations. In this implementation, an analog front end, a narrowband ADC and DSP is required for each channel.

With a fast and accurate ADC, it would be possible to digitize the whole spectrum of interest and channel selection can then be done in the digital domain as shown in Figure 1-5. This implementation eliminates the multiple front-ends and lowers cost and complexity. Furthermore, it would be desirable to implement the ADC in nanometer CMOS for SOC integration with digital filter and signal processor. This requires an ADC architecture that scales with advanced CMOS and that is fast enough to digitize the entire spectrum of interest. However, current ADCs are not power efficient at the multi Giga-Sample per second (GS/s) speeds required to digitize the Gigahertz bandwidths and rely on architectures that do not scale well to advanced CMOS processes.
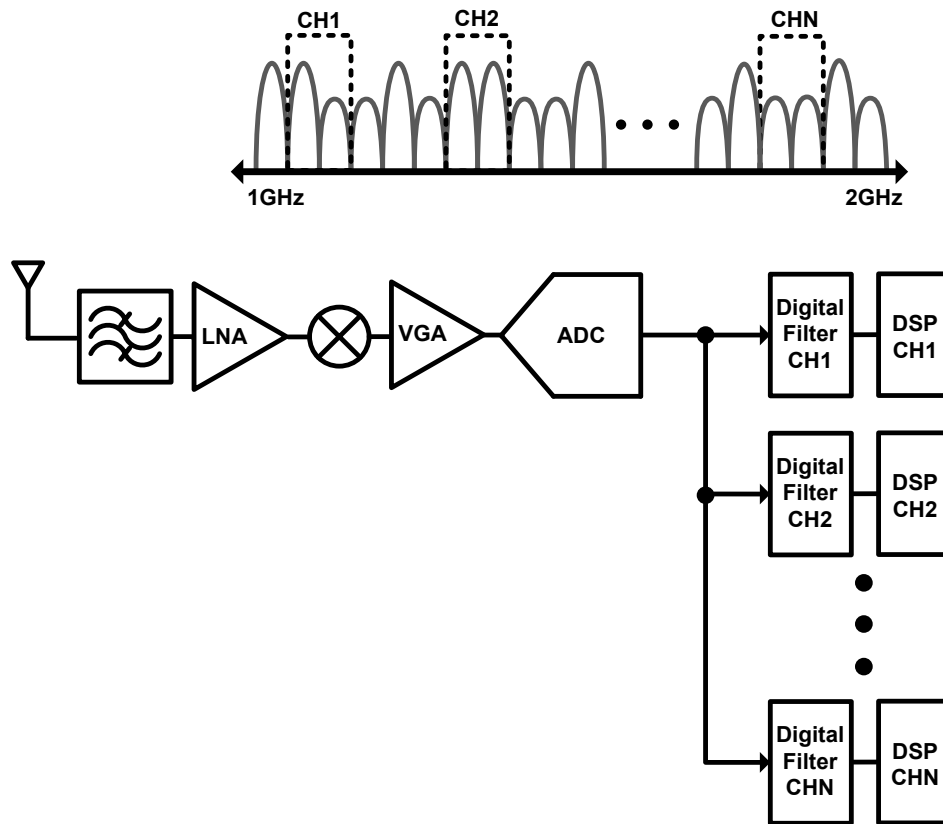
Figure 1-5 Example of a multi-channel receiver for cellular base stations. In this implementation, a single analog front end and wideband ADC is utilized and channel selection is done in the digital domain.

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Micro-cell base stations aim to alleviate the cell bandwidth capacity crunch due to increased demand for picture and video intensive networking and social networking [5]. A high speed (i.e. GS/s+), low power ADC would enable multiple channels to be digitized simultaneously so that channel selection can be done in the digital domain. This results in a reduced component count and reduced complexity in receiver design, both of which reduce cost and size of the micro-cell. However, current, commercial GS/s ADCs are not energy efficient and consume considerable die area.

The flash ADC architecture offers the best solution for Giga-sample per second conversion rates. Furthermore, at its core are circuits whose speed improves with CMOS scaling. However, the exponential dependence of power and area on resolution limits efficient GS/s operation to 6 bits and below. This makes it unsuitable for future broadband communications systems where resolutions of 8 bits and above are required. Therefore new techniques or architectures that decouple this speed-power-resolution tradeoff are needed.

1.3   Flash ADCs

The Flash ADCs is one the fastest types of ADC converter and is well suited for high bandwidth applications. However, power and area implications due to the nature of the architecture put a limit on the maximum practical resolution. Typical applications where flash converters are employed include disk-drive read channels, satellite communication, radar/sonar and oscilloscopes. This section discusses the flash ADC architecture, its speed-accuracy-bandwidth tradeoff and techniques that are employed relax this tradeoff.

1.3.1 Architecture

In a traditional N-bit flash converter, 2^N-1 comparators are employed to compare an input signal with 2^N-1 known references and outputs 2^N-1 one-bit digital signals, which are subsequently encoded into an N-bit digital output. It has the unique advantage of doing a full conversion in a single clock cycle. Figure 1-6 shows the general architecture. The comparator element consists of a latch, and a pre-amplifier that attenuates the input referred offset and noise of the latch. A track-and-hold (*TAH*) circuit tracks the analog input and holds a sampled input on a capacitor while a buffer drives the comparator inputs and the comparators make a decision.
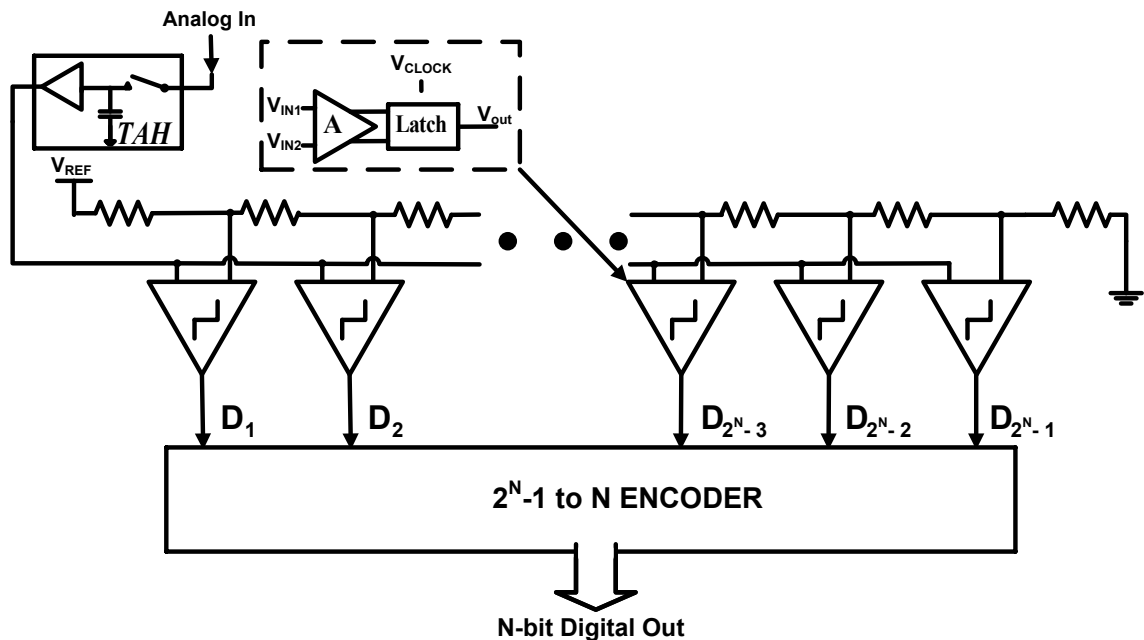
Figure 1-6 N-bit flash ADC architecture.

1.3.2 Random Offset

One of the main disadvantages of the flash ADC architecture is the exponential dependence of the number of comparators with respect to resolution. Additionally, these comparators need to be properly matched and biased in order to convert an analog signal to a digital signal with good linearity.

The current-voltage behavior of MOSFETs shows random variation after fabrication. This random variation is called device mismatch. In the Pelgrom model [6] there are two mismatch terms, one for current factor $K=\mu \cdot C_{ox} \cdot W/L$ mismatch and a second for threshold voltage V_T mismatch. Both terms are given below and are modeled as a normal distribution with zero mean and a variance that is dependent on device dimensions and distance between the devices.

$$\sigma^2(\Delta K)=\frac{A_K^2}{WL}+S_K^2 D^2 \qquad 1.1$$

$$\sigma^2(\Delta V_T)=\frac{A_{V_t}^2}{WL}+S_{V_T}^2 D^2 \qquad 1.2$$

Coefficients A_K, A_{V_T}, S_K, and S_{V_T} are process dependent parameters. The current factor mismatch term accounts for the variation in drawn width and length as well as variation in gate oxide C_{ox} and mobility μ. The V_T mismatch term accounts for variation in the threshold voltage of a device primarily caused by statistical variation of the number of dopants under the gate. The second term in equations 1.1 and 1.2 models the long distance effect. Devices that must match are generally laid out close together so D becomes small and will be neglected.

The input referred offset of a comparator is the differential input voltage that causes the currents in each leg of the source-coupled pair in Figure 1-7 to be equal to half the tail current.
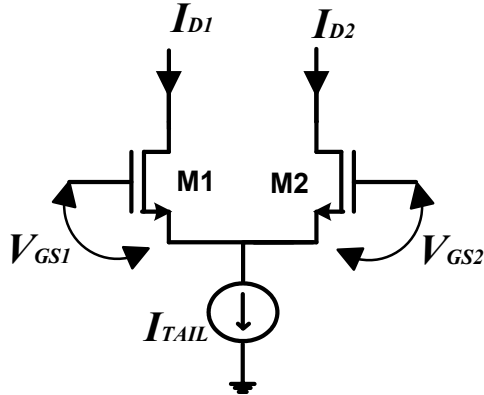
Figure 1-7 Source-coupled pair.

This voltage can be approximated using equation 1.3 below which gives the variance of the offset.

$$\sigma^2(\Delta V_{GS}) = \sigma^2(\Delta V_T) + \frac{V_{dsat}^2}{4} \frac{\sigma^2(\Delta K)}{K^2} \qquad 1.3$$

In practice the V_T mismatch term is dominant in most analog design. This is generally the case for overdrive voltage V_{dsat} values less than 200mV. In [7], the impact of scaling on analog performance is addressed. Considering the fundamental tradeoff between "transconductor efficiency" (i.e. g_m/I_D) and intrinsic bandwidth (i.e. f_T) of a transistor reveals an optimum biasing point. Figure 1-8 below illustrates this tradeoff and shows an optimum biasing point between 100mV and 150mV for 90nm, 65nm and 45nm digital CMOS technologies.
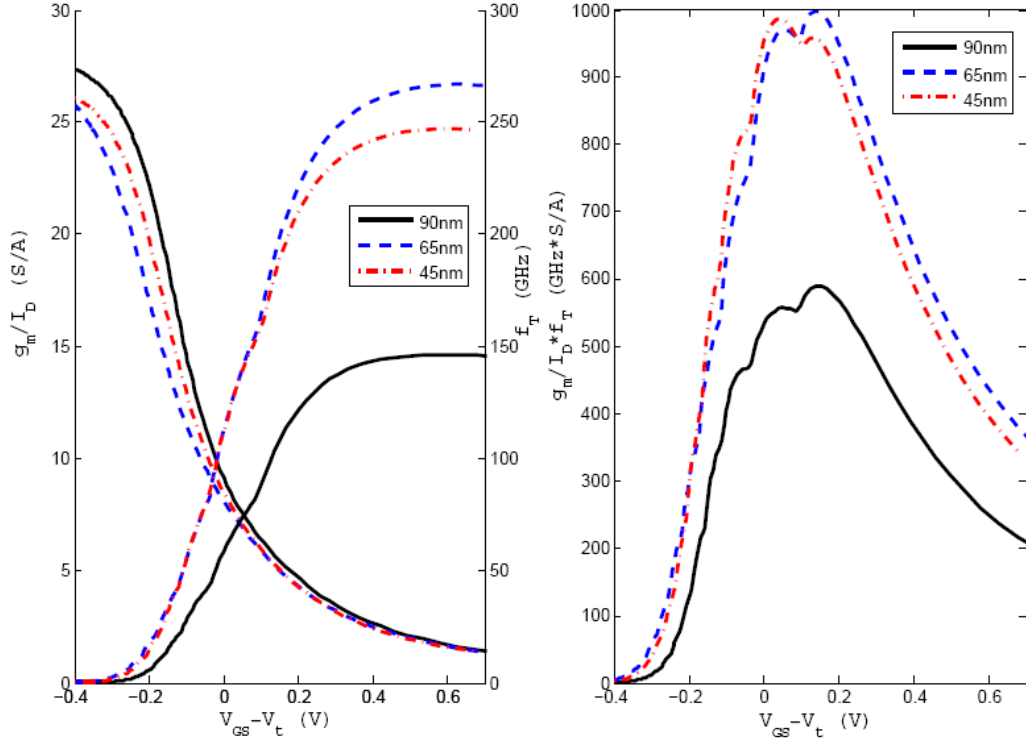
Figure 1-8 Simulation data for minimum length NFET in recent CMOS technologies

Therefore, the second term in equation 1.3 is neglected and the input referred offset of a comparator can be approximated by equation 1.4 below:

$$\sigma_{comp} \approx \frac{A_{V_T}}{\sqrt{(WL)}} \qquad 1.4$$

Figure 1-9 illustrates the effects of V_T mismatch in recent CMOS technologies. The data corresponds to minimum length NMOS source-coupled pairs biased at V_{dsat}=150mV. Although Figure 1-9 shows that the process dependent mismatch coefficient factor A_{V_T} does not vary much from one nanometer process node to the next, the effect of scaling on

comparator offset is apparent and an increase in the standard deviation is observed as we go to finer line-widths.
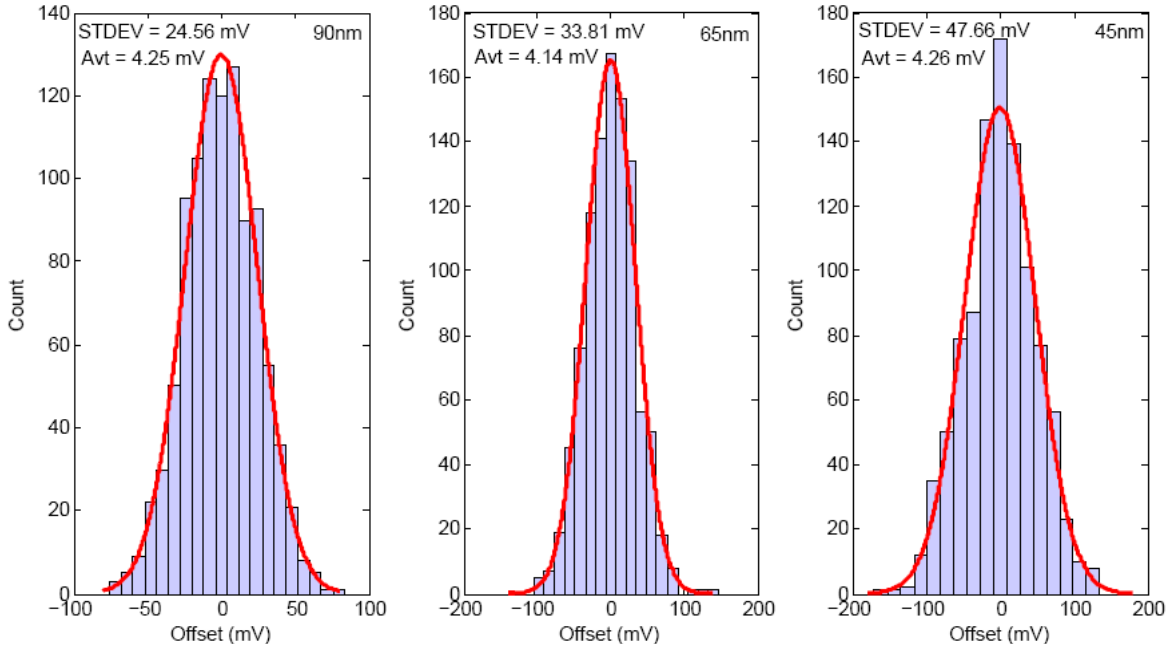
Figure 1-9 Simulation data on the effects of V_T mismatch in recent CMOS technologies. Data corresponds to minimum length NMOS source-coupled pairs biased at V_{dsat}=150mV.

1.3.3 Bandwidth-Accuracy-Power Tradeoff

Device mismatch limits the accuracy of ADCs because of its effect on comparator offsets. Figure 1-10 illustrates the impact of device mismatch on yield of ADCs ranging from 5 to 9 bits of resolution. The data shows that for each additional bit, the maximum offset $\sigma_{comp}(mV)$, required to maintain a ~90% yield goes down by approximately 1/2X.
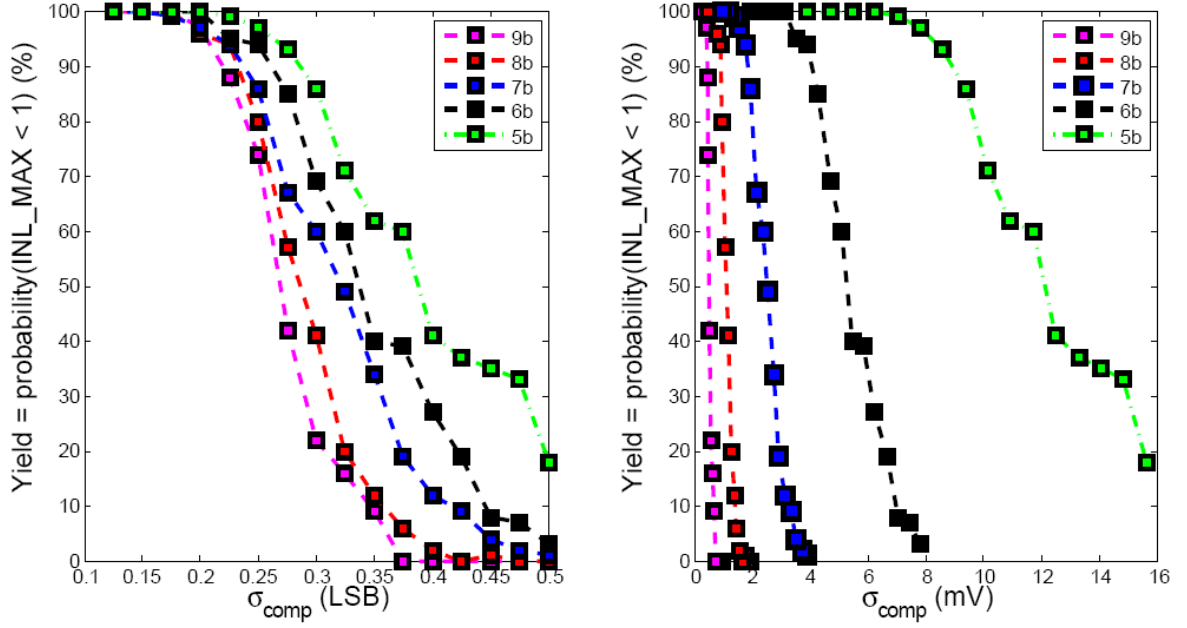
Figure 1-10 Simulation data on yield vs. comparator offset for 5-9b flash ADCs with 1V input signal range.

A traditional N-bit flash ADC requires 2^N-1 comparators which means that the number of comparators roughly double for each additional bit. The large number of comparators required at higher resolutions coupled with more stringent matching requirements, create a tradeoff between bandwidth and accuracy in flash ADCs.

The bandwidth of flash ADCs is limited by comparator input capacitance and is typically dictated by the gate capacitance of the source coupled pair shown in Figure 1-7. Assuming devices are properly biased in saturation, the total comparator input capacitance of an N-bit flash ADC is given by,

$$C_{in} = \frac{2}{3}C_{ox}WL(2^N - 1) + C_{Wire} \qquad 1.5$$

where C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the comparator input pair, respectively and C_{wire} is the interconnect capacitance. TABLE I

below shows that for resolutions greater than 6 bits, the device widths required for 90%

yield results in an input capacitance C_{in} in the tens to hundreds of pico-farads. To drive

such a large capacitance, a buffer would be required. An on-chip buffer would be difficult

to design and would undoubtedly consume a lot of power.

TABLE I Comparator input capacitance C_{in} as a function of matching requirements
for 5-9b flash ADCs with 1V input range in recent CMOS technologies.

Resolution	σ (LSB)	σ (mV)	W (μm) 90nm	W (μm) 65nm	W (μm) 45nm	Cin (pF) 90nm	Cin (pF) 65nm	Cin (pF) 45nm
9	0.22	0.43	978	1547	2457	333.27	474.37	669.69
8	0.23	0.91	220	348	552	37.39	53.22	75.13
7	0.24	1.86	52	83	131	4.42	6.30	8.89
6	0.26	4.08	11	17	27	0.46	0.65	0.92
5	0.29	8.94	2	4	6	0.05	0.07	0.09

In [8] it was shown that for a full-scale input to settle within 1/2LSB at an N-bit level

requires $N \cdot ln(2)$ time constants. The time constant is a function of the transconductance

(Gm) of the buffer and input capacitance of the comparators. To relax the jitter

requirements on the sampling clock, the buffer is typically preceded by a sampling switch

and a hold capacitor to form a Track-and-Hold (TAH) circuit (Figure 1-6). The TAH

circuit tracks the analog input and holds the sampled input on a capacitor for half the

clock period T_{clk} while the comparators make a decision. Assuming a unity gain buffer

for the TAH, the settling requirement t_{settle} at the buffer output is given by,

$$\frac{T_{clk}}{2} \geq t_{settle} = N\left(\frac{C_{in}}{G_m}\right)ln(2). \quad 1.6$$

Assuming the G_m of the buffer is equal to the small signal $g_m = 2 \cdot I_D/V_{dsat}$ of a device,

for a fixed V_{dsat}=150mV, the plot in Figure 1-11 gives the total current requirements for

the buffer as a function of resolution at various sample rates. The plot uses data from

TABLE I for a 90nm CMOS process and assumes no slewing. Setting a current budget of

10mA, the tradeoff between power, bandwidth and accuracy in flash ADCs limit sample rates at 1GHz and above to 6bit converters and below.

Figure 1-11 Speed-Power-Accuracy tradeoff for flash ADCs in 90nm CMOS with V_{dsat}=150mV.

Figure 1-9 and Figure 1-10 illustrates that the bit accuracy of flash ADCs in CMOS is related to the matching quality of the technology. Furthermore, to achieve good accuracy requires large devices for the input pair of the comparator. As a result, the comparator input capacitance increases and more power is needed to achieve high bandwidth.

1.3.4 Area

For resolutions greater than 6bits, TABLE I shows that the accuracy requirements for the comparators require device widths greater than 50μm. Furthermore, TABLE I also shows that for the same accuracy, device widths increase at finer line-widths. Since the

number of comparators approximately doubles for each additional bit of resolution, the flash ADC architecture presents area implications for moderate resolutions and above.

In conclusion, matching requirements limit the performance of flash ADCs and high speed and high accuracy can only be achieved by consuming large amounts of power and area. Therefore, decoupling comparator performance from device matching requirements is desirable.

1.3.5   Resistive Offset Averaging

To relax comparator offset requirements in flash ADCs, resistive offset averaging [9] and interpolation [10] have been used to average out mismatch error sources and to reduce the number of pre-amplifiers at the ADC input. Resistive averaging involves connecting resistors between adjacent pre-amplifier outputs as shown in Figure 1-12. Interpolation involves generating zero crossings between two reference levels as shown in Figure 1-13.
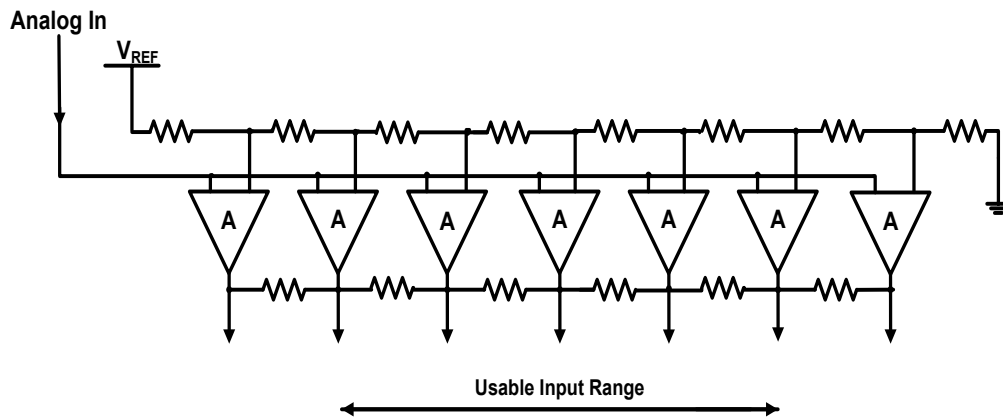
Figure 1-12 Resistive offset averaging.
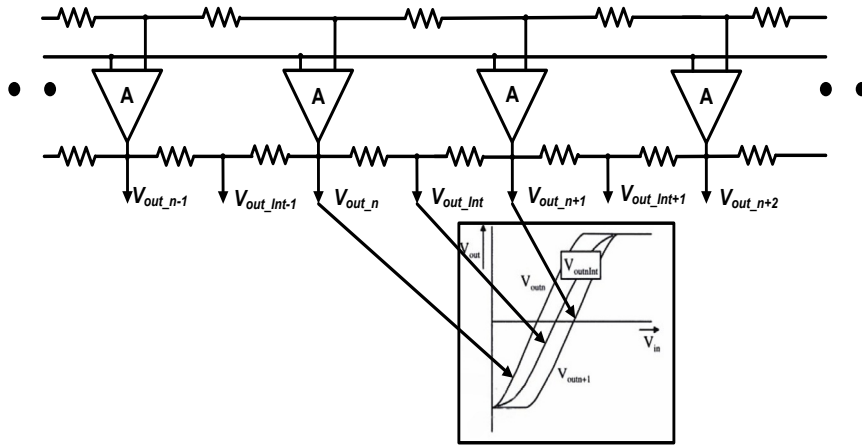
Figure 1-13 Resistive Interpolation.

Although these techniques reduce power and ADC input capacitance, averaging causes a boundary effect, where systematic nonlinearity at the edges of the ADC transfer curve degrades INL [11]. To circumvent these boundary effects, an over-ranging technique [12] incorporates dummy pre-amplifiers at the edges that connect to reference taps extending beyond the input signal range as shown in Figure 1-14. A resistive termination technique in [13] alters the values of the averaging resistors at the edges to reduce the over-range voltage required as shown in Figure 1-15. However, the requirement for the value of the termination resistor limits the value of averaging resistors which in turn limits the allowable offset reduction.
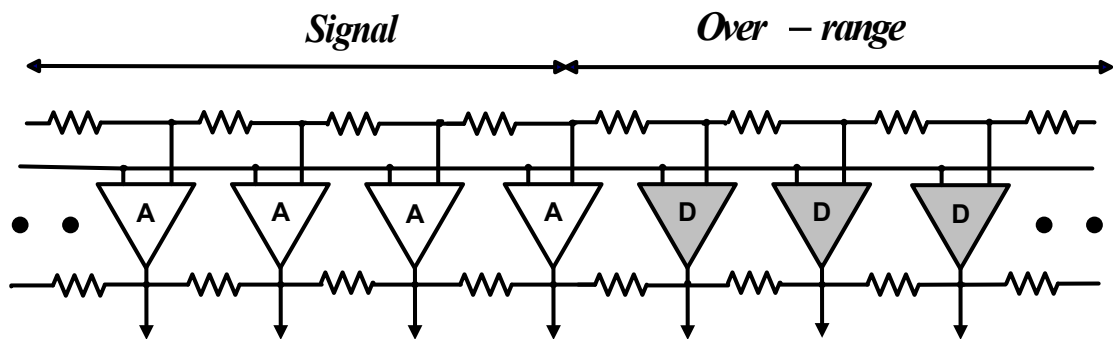
Figure 1-14 Over-ranging.
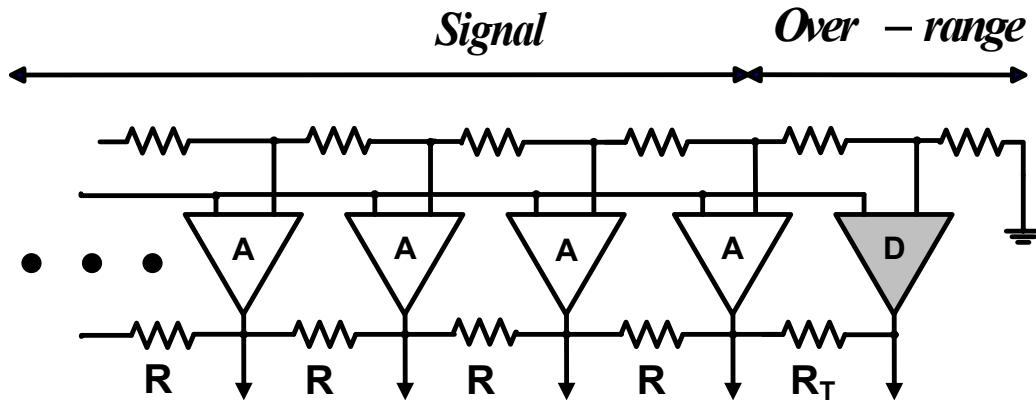
Figure 1-15 Termination.

Both methods however, require dummy pre-amplifiers which result in a loss of usable voltage range, increased power, input capacitance and area. A triple-cross connection method in [14], cross-connects the outputs of the dummy pre-amplifiers with adjacent preamplifiers and with dummy preamplifiers at opposite edges as shown in Figure 1-16. This eliminates the over-range references and maintains uniform averaging over the entire input range. However, this method introduces negative transconductance at the edges reducing the effective transconductance, gain and bandwidth at the edges. In [15], a reference voltage extrapolation technique eliminates the over-ranging requirements but still requires the use of dummy pre-amplifiers. Area and power constraints limit these techniques to 6 bits and offset requirement can be relaxed by up to 3X [12].
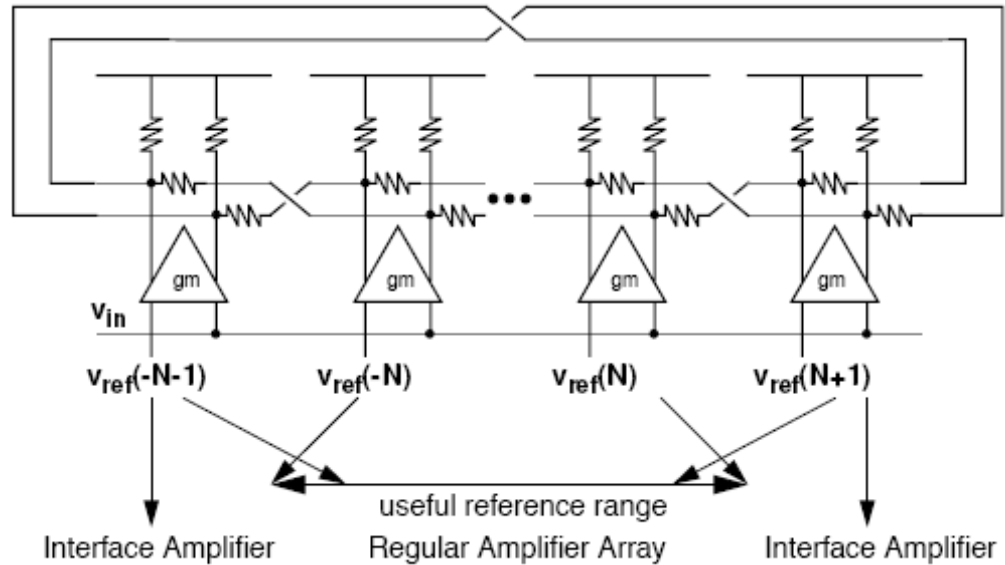
Figure 1-16 Triple-Cross connection

1.3.6 Comparator Redundancy and Reassignment

By exploiting the effects of V_T mismatch with digital correction, the accuracy requirements for comparators can be significantly relaxed to allow flash ADCs to leverage the benefits of scaling. In [16], digital calibration in combination with comparator redundancy and reassignment are used to decouple comparator performance from device matching requirements. This enables the use of low precision comparators that were optimized for speed, power and area.

Reassignment

Comparator reassignment involves reassigning a comparator that was originally designated to a specific code, to one in which it is more suited to. This guarantees monotonicity regardless of the offset magnitude. Figure 1-17a shows the trip points for an ideal and actual 3-bit flash ADC with offsets. In the latter case, large comparator offsets

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have caused the trip-points of all the comparators to deviate significantly from their nominal trip-points. Furthermore, comparators one and six have become interchanged with three and four respectively. The sequence of trip-points is no longer monotonic. This causes large DNL errors, missing codes and results in poor linearity when employing basic encoding schemes. Figure 1-18a illustrates the resulting transfer curve.

With reassignment, all comparators are reassigned to codes that are close to their actual trip-points. The comparators for the actual case in figure 2.2.a will therefore be reassigned as follows:

TABLE **II** **Reassignment for comparators of Figure 1-17a**

Comparator	Reassignment
1	3
2	1
3	2
4	5
5	6
6	4
7	7

Figure 1-18b illustrates the resulting transfer curve. Reassignment has ensured monotonicity however large DNL errors still exist.

Redundancy

To correct for DNL errors, redundancy is introduced. Redundancy involves assignment of multiple comparators to each code. This increases the probability of finding a comparator close to each ideal trip-point. Figure 1-17b shows the trip points for an ideal and actual 3-bit flash ADC with redundancy. In the actual case, large comparator offsets have caused the trip-points of all the comparators to deviate significantly from

their nominal trip-points. However, because more than one comparator was assigned to each code, there exist comparators with actual trip-points near every nominal trip-point. A search can performed to find the trip-point closest to each nominal trip-point. The comparators for the actual case in Figure 1-17b will therefore be assigned as follows:

Table III Reassignment for comparators of Figure 1-17b.

Comparator	Reassignment
1a	3
3a	1
3b	2
3c	5
4b	4
5a	6
7c	7

Figure 1-18c illustrates the resulting transfer curve. Reassignment has ensured monotonicity and redundancy has reduced DNL errors.

Degree of Redundancy

Yield is a function of comparator offset and redundancy. Comparator offsets cause non-uniform quantization that degrades signal-to-noise ratio (SNR). Therefore, to achieve good performance based on a target SNR, sufficient comparator redundancy must be employed. In [17], it was shown that redundancies of 4 and greater exhibit yields greater than 90% for comparator offsets up to 10LSB. The yield criteria used was a maximum of 3dB attenuation in SNR of an ideal flash ADC.

Calibration Algorithm

At power-on, a calibration engine (i.e. finite state machine) initiates a search algorithm. With aide from a digital-to-analog converter (DAC), known references

spanning the ideal trip voltages are applied to the input of the comparator bank. Changing the input voltage about an ideal trip-point triggers near-by comparators. The calibration engine processes the outputs of each comparator and allows the most suitable comparators to be selected. Un-selected comparators are powered off. For an N-bit ADC, the search finishes when 2^N-1 comparators are selected. Figure 1-19 shows the state-diagram for the code search algorithm.

Figure 1-20 illustrates an example of a comparator search. Here comparators "a", "b" and "c" are within "4Δ" of the desired "nominal trip-point". The calibration engine coordinates the DAC to output voltages within the range: "Nominal trip-point" ± "4Δ" in "Δ" increments beginning at the nominal trip-point. Therefore, on the sixth search comparator "a" triggers and will be detected by the calibration engine. However, because of circuit noise, comparators "b" and "c" may also trigger even though their trip-points were not reached. To compensate for circuit noise, the calibration engine will coordinate multiple sweeps at the same DAC output. In this case the region "+2Δ→+3Δ" will be searched multiple times. The calibration engine will record all triggers and select the comparator that triggered the most number of times. This effectively averages out the noise.

Encoding

Conventional encoding schemes for flash ADCs are susceptible to comparator offsets which cause errors at the thermometer decoder output. Figure 1-21a shows a 3-bit flash ADC where comparator offsets lead to a "bubble" in the thermometer code. The result is an error of 3LSBs at the binary encoder output. Such errors result in non-monotonic behavior like the one observed in Figure 1-17a. An encoding scheme that achieves local

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and global bubble suppression to limit the maximum error to one LSB was presented in [18]. It is based on a "Wallace tree" architecture [19] used to implement high-speed multipliers. Figure 1-21b shows the architecture and gives an example where a bubble in the thermometer code output of the comparators is corrected by simply counting the number of logical ONEs present at the output of the comparators.

The encoding scheme is inherently independent of comparator assignment. Therefore it is suitable for flash ADCs incorporating redundancy and reassignment since unselected comparators are powered off, and do not contribute to the summation.
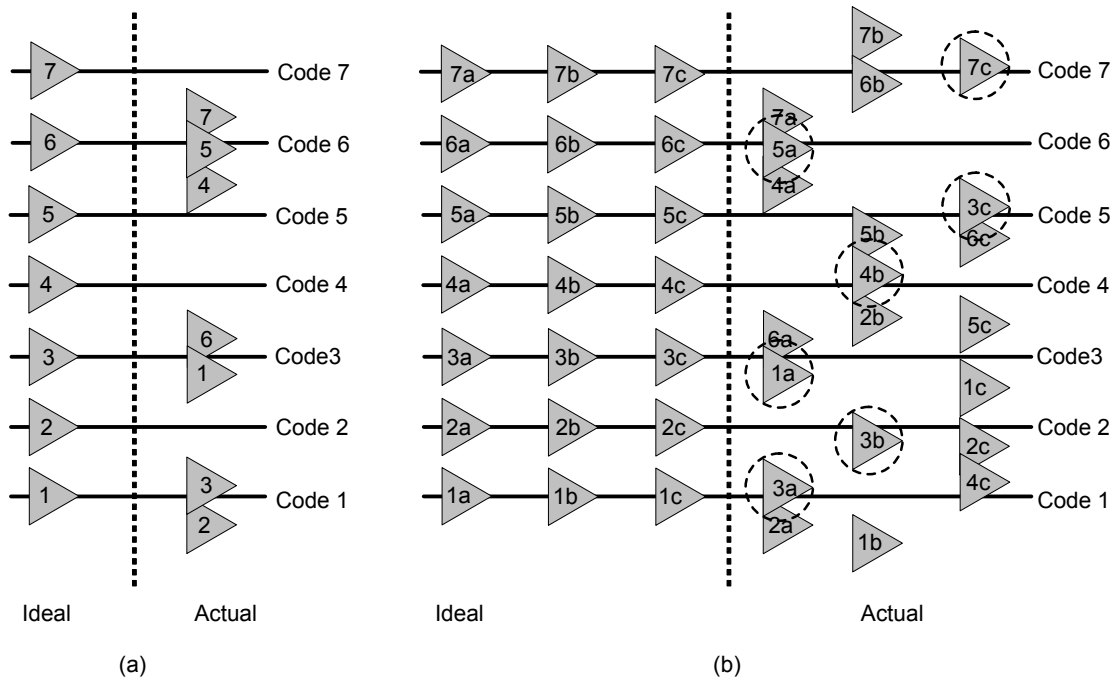
Figure 1-17 Comparator Redundancy and Reassignment. (a) 3b ADC ideal and actual with reassignment. (b) 3b ADC ideal with redundancy and actual with reassignment.
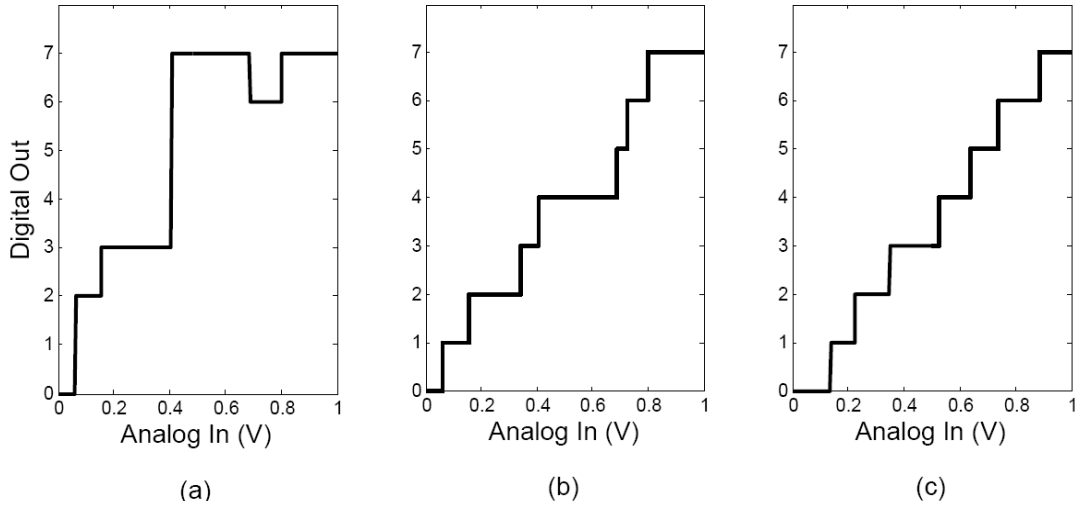
Figure 1-18 Trip-points for 3b flash ADC with offsets. (a) No reassignment. (b) With reassignment. (c) With reassignment and redundancy.
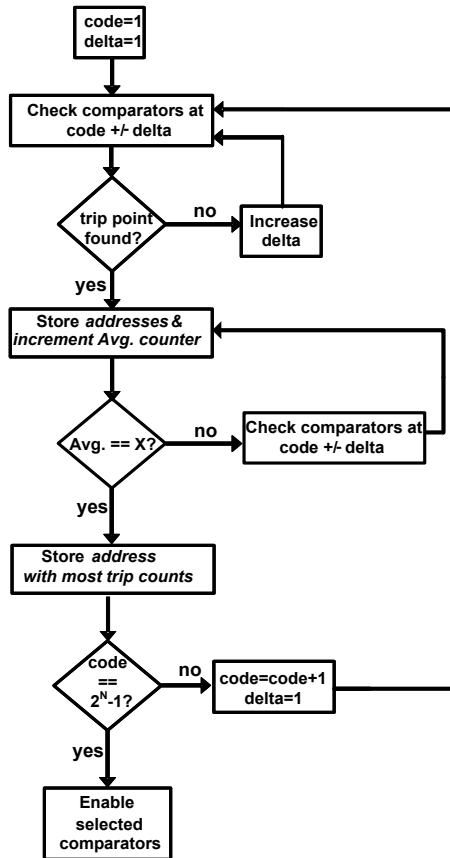
Figure 1-19 Code search algorithm.
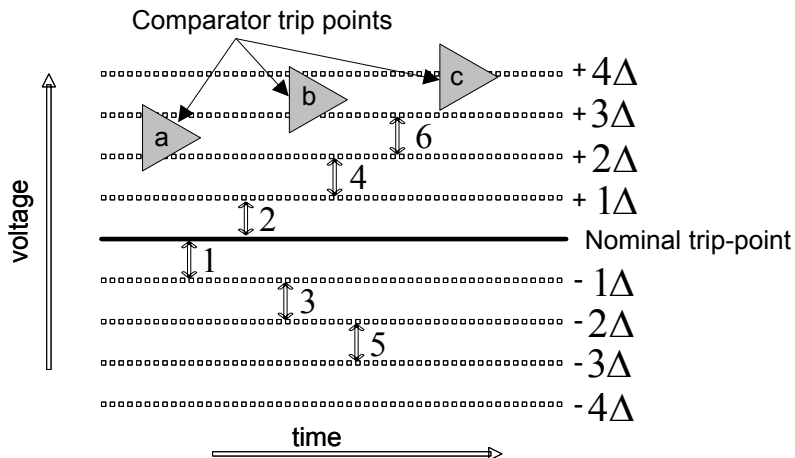
Figure 1-20 Example of an ADC comparator search where three comparators trip on the sixth search. Noise averaging will result in the selection of comparator "a".

(a)   **(b)**
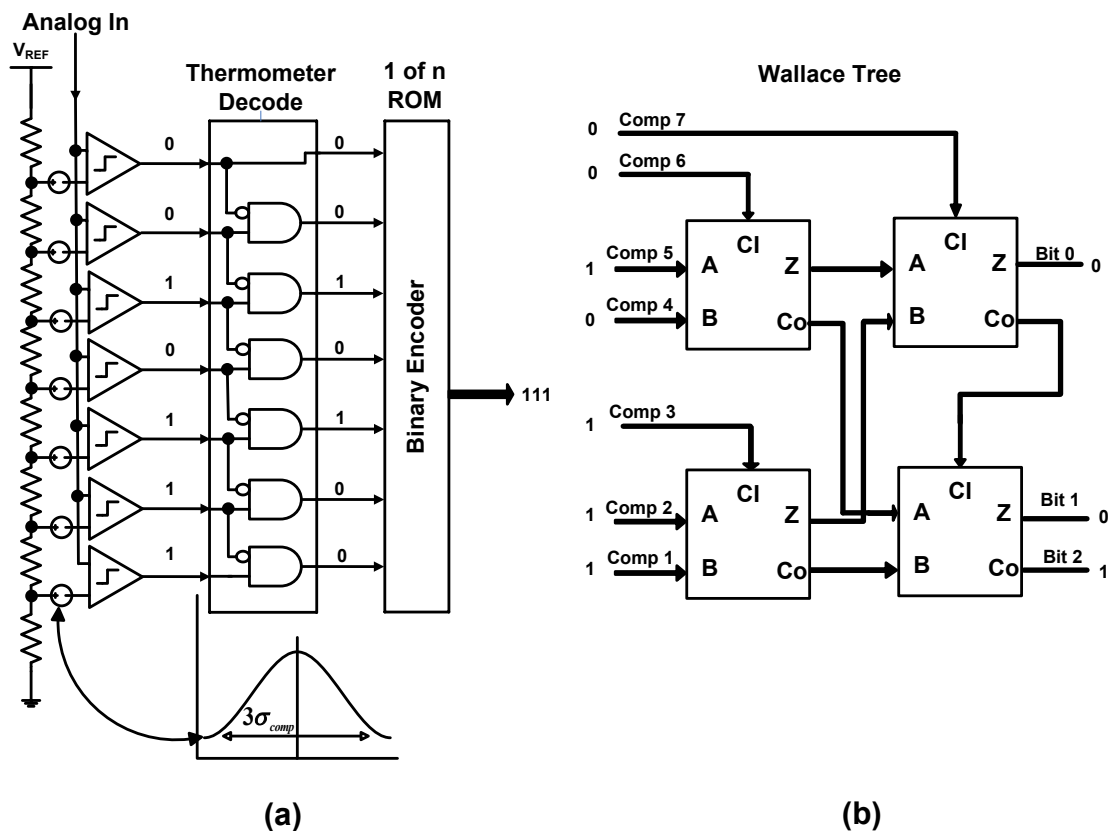
Figure 1-21 (a) Conventional encoding scheme for flash ADCs where bubbles in the thermometer code lead to errors in the ADC output. (b) Encoding scheme based on Wallace tree architecture.

1.4   Recent work on flash-based ADCs

GS/s, moderate resolution ADCs incorporating a flash architecture with statistical selection [20] or a sub-ranging architecture that eliminates the reference switching network [21], employ small, compact comparators to leverage the speed, area and power advantages of nanometer CMOS. Furthermore, they can rely on statistical selection or offset calibration techniques to limit SNR degradation from non-uniform quantization noise. However, the advantages of small device sizes for speed, power, area and low input capacitance are offset by circuit noise which limits overall ADC performance to less than 7 bits in [21] and less than 6 bits in [20].

1.5   Recent work on Time-Interleaved ADCs

The time-interleaved architecture is popular for high sample-rates because it shifts the speed requirement to the sampled-and-hold circuits. For moderate resolution, Giga-Sample per second conversion (GS/s) the time-interleaved pipeline and SAR architectures are extensively employed. However, interleaving of sampling is challenging, and complex calibration algorithms are required to correct for gain, offset [22], [23], [24], [25] and sometimes timing mismatch between channels [22], [25].

Time-interleaved pipeline ADCs with both GS/s performance and moderate resolution have been achieved using conventional op-amp designs in 0.13μm CMOS. In [23], a double sampling technique is leveraged to reduce the number of T/Hs, maximize active op-amp power with op-amp sharing, and increase the throughput of each sub-ADC. In [26], extensive interleaving was employed to relax the op-amp bandwidth requirements. However, the high op-amp gain required even in conventional moderate-

resolution pipeline ADCs is challenging in 45nm CMOS and below where the transistor self-gain is ~10 and supply voltage is 1V.

In [15], both high gain and bandwidth are achieved in the MDAC op-amp with increased levels of cascoding, gain boosting and the leveraging the f_T of 40nm thin-oxide MOS transistors in the differential pair. Although this technique enables greater than 9 bit linearity and 1.5GS/s operation in each pipeline ADC, thick-oxide devices and a 2.5V supply were required to maximize the op-amp signal swing. Furthermore, low drop-out regulators (LDOs) were required to adapt the subsequent circuit blocks, which employed thin-oxide devices, to the common mode of the op-amp. A dual-residue technique in [27] relaxes the op-amp gain and bandwidth requirements enabling simple gain stages in a 40nm CMOS with a 1V supply to achieve greater than 9 bit linearity. However, 4X interleaving was required for only 800MS/s performance. In [28], 1-bit folding sub-ADCs incorporating open loop amplifiers enabled single-channel 7b GS/s performance in 45nm CMOS. However, settling errors from full-scale transitions severely degrade SNDR at high frequencies.

On the other hand, the power efficiency of the SAR ADC architecture, coupled with advances in CMOS, has enabled moderate resolution SAR ADCs up to 100 Mega-Samples per second (MS/s) when incorporating error compensation techniques [29]. For GS/s performance and moderate amount of interleaving, the resolution is limited to around 7 bits [25], [30]. For higher resolutions, recent architectures leverage the power efficiency of SAR ADCs either with extensive parallelization [26] or in a hierarchical structure by connecting many SAR sub-ADCs to a single track and hold (TAH) [31]. A hierarchical structure maintains the interleaving factor and number of Track and Hold

(TAH) circuits to moderate levels. However, these approaches yield a large active area, require gain and offset calibration, and consume power in the hundreds of milli-Watts.

1.6 Thesis Outline

This work focuses on power efficient, Giga-Sample per second (GS/s), moderate resolution ADCs in nanometer CMOS technologies. The following chapters describe the theoretical background, describe circuit prototypes and present measurement results for three ADC architectures. Chapter 2 describes work on the advancement of a comparator redundancy scheme based on probability and digital correction techniques to compensate for accuracy in flash ADCs [32]. Chapter 3 describes a high feedback factor approach to the pipeline ADC architecture to relax the gain and bandwidth requirements in the multiplying digital to analog converter (MDAC) [33]. Chapter 4 describes a novel technique that employs op-amp and sub-ADC sharing in a 2X time-interleaved pipeline ADC to increase throughput, and at the same time reduce power dissipation and area [34]. Finally, chapter 5 offers concluding remarks, a comparison with state of the art and suggests future research projects.

CHAPTER 2 Deliberate and Random Offset for Setting Comparator Thresholds

2.1   Introduction

For flash ADCs, the bandwidth-accuracy-power tradeoff becomes more stringent in finer line-width technologies, because this relationship is determined by process-dependent parameters that characterize transistor matching [35]. Unlike conventional designs, this work exploits the effects of V_T mismatch. The accuracy requirements for comparators can be significantly relaxed, allowing the ADC design to leverage the benefits of digital scaling. In [16] [17] [36], a comparator redundancy scheme is introduced to decouple performance from matching requirements. We advance this technique by employing random and deliberate mismatch to set the desired trip-points of the comparators and thus eliminate the need for a low-impedance high-precision resistor ladder. Unusually, the proposed technique exploits large random variation in comparator offset. This enables the use of low precision dynamic comparators that can be optimized for speed.

Section 2.2 presents an outline of the ADC architecture and discusses the implementation of key blocks. A challenge in this design is to achieve a large random variation in comparator offset and at the same time, satisfy the input-referred noise requirement of the comparators. Section 2.3 considers this tradeoff and the implications for energy efficiency of the comparator. Measurement results are presented in section 2.4.

2.2 Architecture and Implementation

Figure 2-1 shows a block diagram of the proposed ADC architecture. A track-and-hold (TAH) circuit samples a differential input signal (single-ended shown), which is subsequently processed by a subset of a bank of redundant comparators. No reference ladder is required since the comparator trip-points are set by a combination of deliberate and random mismatch. At startup, a calibration routine finds the comparators closest to the desired trip points. Sufficient redundancy ensures that enough variation exists about a pre-defined set of deliberate mismatches to ensure the comparator bank spans the desired input range. Furthermore, because this technique decouples comparator performance from matching requirements, the comparators can be made small and fast. Only useful comparators are enabled. Each comparator can be enabled or disabled independently and a memory element associated with each comparator stores the comparator on/off states. The memory elements are connected serially forming a memory block that is accessible through an SPI interface. An encoder block, comprised of full adders, resolves the comparator outputs to the 7-bit ADC output code.
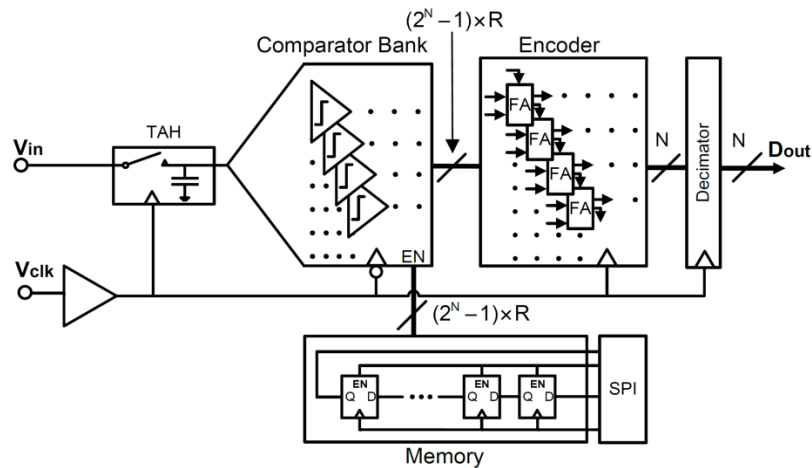
Figure 2-1 N-bit ADC architecture with redundancy of R comparators per code.

2.2.1 Comparator Bank

The comparator bank incorporates redundancy and reassignment to correct DNL errors [16], [17]. A conservative value of ten was chosen for comparator redundancy in this proof of concept design. In this scheme, multiple redundant comparators are assigned to each code to increase the probability of finding a comparator with a trip-point close to each ideal trip-point. Furthermore, by allowing comparators with large random offsets, originally designated to specific codes, to be reassigned to more suitable codes, offset do not compromise ADC accuracy, regardless of their magnitude.

Since this ADC architecture does not employ a resistor ladder, comparator thresholds are determined by a combination of deliberate and random offsets. Random offsets alone would limit the dynamic range of the ADC. This is because large random offsets require small devices, which in turn leads to higher noise, degrading SNR. Therefore, deliberate offsets are introduced to the comparators to increase dynamic range. Increasing the dynamic range increases the LSB size for a given resolution therefore improving SNR. The minimum input range is dictated by the input referred noise value that allows the ADC design to meet a target SNR. On the other hand, it is also necessary that random offsets adequately cover the desired range between deliberate offsets and this limits the maximum input range. In section 2.3 we show that only a small number of deliberate offsets needs to be introduced.

2.2.2 Comparator

The comparator, based on [37], is modified to introduce a deliberate offset. This current latch sense amplifier (CLSA), shown in Figure 2-2, leverages small devices for

power and speed and also exhibits large offsets suited for redundancy and reassignment. Deliberate offsets are introduced by asymmetric sizing of the input pair and by the use of FETs with differing threshold voltages. The input differential pair of the comparator is formed as composite devices, M1a-c and M2a-c. M1a-c and M2a-c are formed by combinations of low, medium and high V_T devices. The use of devices with different threshold voltages for the input pair limits the amount of asymmetrical sizing needed for a given offset. Different V_T combinations are assigned to different comparators during layout. Furthermore, asymmetric sizing is introduced with switches SW1-4 which hardwire the programming of the widths of the input pair. A standard unit cell (Figure 2-2) is used to implement all comparators in the comparator bank. This allows programming of the deliberate offsets to be achieved with automated schematic design, layout and simulation. Increasing the input range by adding branches to the composite devices M1-2 of the comparator in Figure 2-2 increases the input capacitance of the comparator bank and puts a heavier burden on the input sampling switch for a given settling time requirement. Therefore comparator input capacitance, along with noise and offset, dictate the input range and 600mVpp was found to be optimal.

The comparator, including the SR latch, buffers and enable/disable functionality, occupies an area of $100\mu m^2$, of which 30% is the input FETs, SW1-4 and M3.

Figure 2-3 shows the circuit waveforms for the comparator in Figure 2-2. The circuit operation is as follows: When V_{clk} is low, all internal nodes including V_{dn-p} and V_{op-n} are preset to V_{DD} by switches SW5-8. When V_{clk} goes high, the input pair senses the input voltages, V_{ip} and V_{in}, and induces differential currents I_p and I_n through M1a-c and M2a-c respectively. The current difference is converted to a large voltage difference through

regeneration and latching of the cross-coupled inverters at nodes V_{op-n}. The final output voltage difference, V_{op}-V_{on}, reaches $\pm V_{DD}$ and is subsequently latched by an SR latch to retain the decision during the reset phase.
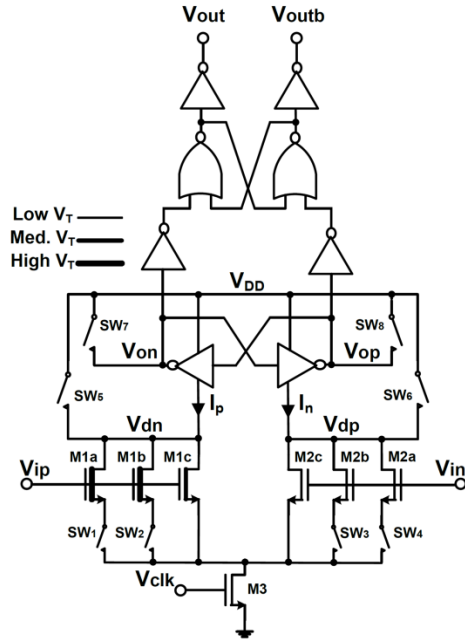
Figure 2-2 Comparator circuit with programmable offset.
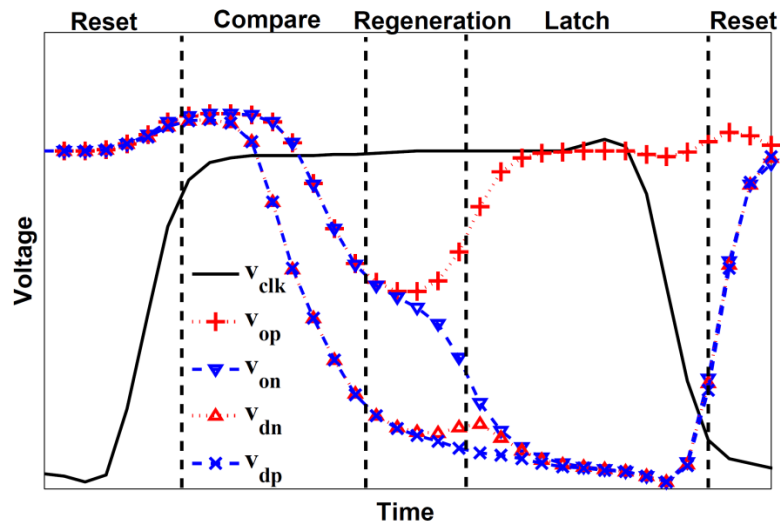
Figure 2-3 Waveforms illustrating regions of operation of the comparator.

2.2.3   Boot-strapped Track-and-Hold

A track-and-hold (TAH) circuit is used to reduce the jitter requirements for the comparator sampling clock and to minimize the effects of skew in the clock-path of the comparator bank. The TAH circuit consists of an NMOS switch and a hold capacitor, comprised of the routing capacitance and the input capacitance of the comparator bank. Furthermore, the TAH is boot-strapped [38] in order to operate at a 1.2V supply and to reduce input signal dependence.

The circuit, shown in Figure 2-4, uses a charge pump consisting of capacitors C_{1-2} and devices M5-6, to charge capacitor C_3 to V_{DD} during the hold mode (i.e. v_{clk} is low). In track mode, the gate of switch M3 is coupled to capacitor C3 via M8. During this time, M3 allows the gate of M4 to track the input signal v_{in} offset by V_{DD} and thus allowing a constant voltage across its gate-source during the entire track mode.

By maintaining a constant Vgs, switch linearity is improved and signal-dependent charge-injection is reduced. A differential TAH is used for suppression of second order effects [11]. Figure 2-5 shows extracted simulation waveforms and switch linearity for a ~1GHz input signal sampled at 2GHz. The simulation use a 1V V_{DD} and uses load models based on extracted data on the comparator bank and signal path. The lower plot corresponds to ENOB vs. Time based on 512 point FFTs over one clock cycle. Data shows that 10-bit linearity is maintained during the hold phase and up to 13-bit linearity is seen during the track phase.
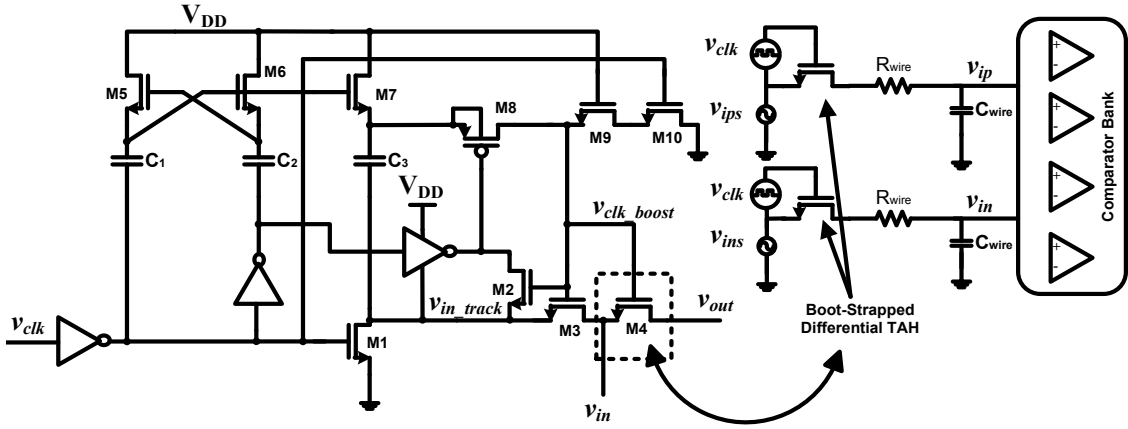
Figure 2-4 Differential boot-strapped TAH.
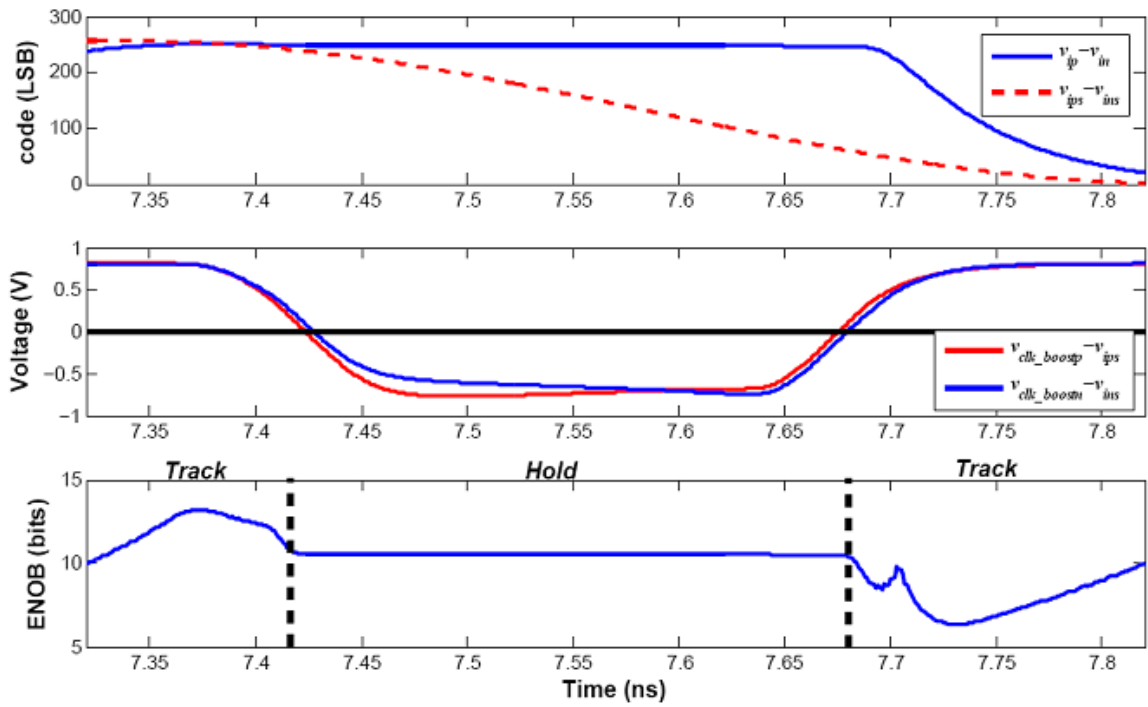
Figure 2-5 Differential boot-strapped TAH waveforms and linearity for ~1GHz input signal sampled at 2GHz.

2.2.4 Encoder

The outputs of all the comparators are routed to an encoding block and summed to form a 7-bit output word. Addition permits comparators to be easily reassigned to any code and eliminates non-monotonicity. The encoder uses a Wallace tree architecture [18], in combination with carry-select adders and pipelining, to resolve ~1500 comparator outputs at 1.5GS/s. Figure 2-6 shows the block diagram. This encoding scheme is inherently independent of comparator assignment since it adds the number of logic highs present at its input. Furthermore, since only 127 comparators are enabled after calibration and disabled comparators do not contribute to the encoded result, 7-bit encoding is guaranteed.
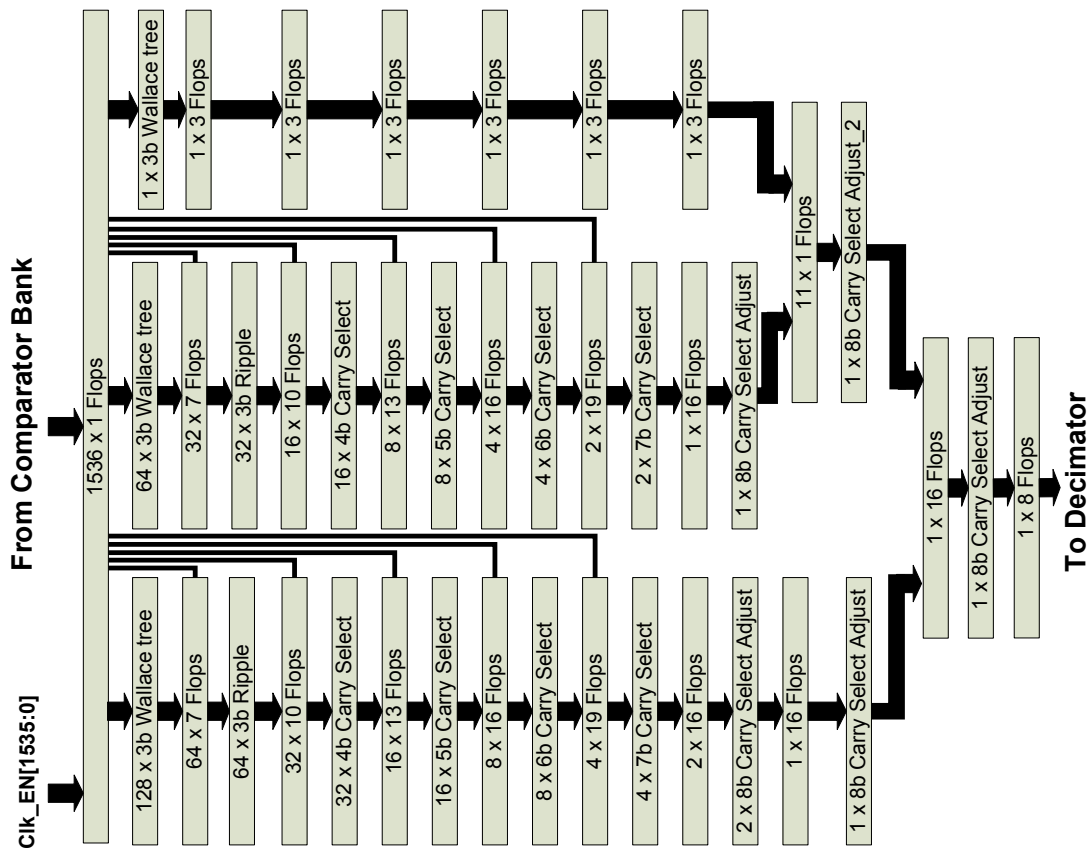
Figure 2-6 Encoder block diagram.

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2.2.5 Calibration Algorithm

At power-on, an off-chip calibration engine initiates a comparator search algorithm [36]. With the aid of an off-chip digital-to-analog converter (DAC), input voltages spanning the desired trip voltages are applied to the input of the comparator bank to search for the optimum comparator to assign to each code. During the search, the calibration engine enables a trial comparator. Comparators that have already been selected during earlier searches are also enabled. This mimics the effects of comparator kickback seen during normal operation and minimizes any differences between IR drops on the supply lines during calibration and normal operation. The calibration engine then instructs the DAC to sweep the input voltage about the desired trip-voltage. If the trial comparator is suitable its output will toggle causing the output of the encoder to transition between X and X-1 where X is the total number of comparators enabled. For a 7-bit ADC, the search finishes when 127 (i.e. 2^7-1) comparators are selected. Unselected comparators remain powered off[1]. Finally, it should be noted that the input range is set by the maximum deliberate comparator offset and is hardwired into the design. Sweeping the calibration DAC beyond this input range reduces the effectiveness of random comparator offset and degrades DNL.

2.3 Comparator Analysis

A challenge in the design of the comparators is to achieve a large random variation in offset, beneficial for redundancy and reassignment, and at the same time to satisfy the input-referred noise requirement. This design employs small, low-precision comparators

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[1] The clock input to each comparator is preceded by a series switch that disconnects the local clock buffer to any disabled comparator.

with large random offsets. Equation (1.4) shows that the use of small devices results in a large random offset which in turn enables a wider distribution of trip voltages for the redundancy and reassignment scheme. However, the use of small devices also tends to increase the input referred noise of the comparators which in turn limits the ADC SNR. In [39] it is shown that thermal noise from the input pair and kT/C noise from switches SW7-8 during reset are the dominant sources of noise. To first order, the input-referred noise equivalents of these sources, validated with Spectre transient noise simulations, are given by [39],

$$\overline{\delta v^2_{eq\_M1-2}} \approx \frac{2kT\gamma \cdot v_{dsat1}}{C_d V_{TN}} \qquad 2.1$$

$$\overline{\delta v^2_{eq\_sw7-8}} \approx \frac{kT \cdot v_{dsat1}^2}{2C_o V_{TN}^2} \qquad 2.2$$

where v_{dsat1} is the overdrive voltage of the input pair, V_{TN} is the threshold voltage of the NFETs of the cross-coupled inverter pair, γ is the MOS noise factor, and C_d and C_o are the capacitances at nodes V_{dn-p} and V_{op-n}, respectively. Equations 2.2 and 2.3 show that increasing the capacitance at nodes V_{dn-p} and V_{op-n} or reducing v_{dsat1} by increasing the widths of the input pair, reduces noise.

Figure 2-7 plots comparator input-referred offset and noise versus device width, using data obtained from Spectre simulations. The x-axis is the width of M1-3 and of the cross-coupled inverters of the comparator in Figure 2-2[2]. The comparator is clocked at 2GHz and the circuit uses a 1V V_{DD}. Power is plotted alongside noise and offset to illustrate the tradeoff between power, offset and accuracy. Figure 2-7a shows the advantages of small

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[2] These simulations consider composite devices M1a,b,c and M2a,b,c as single nominal V_T devices. Switches SW5-8 are sized to ensure reset functionality at 2GHz. Switches SW1-4 are not included.

width in terms of power consumption and increased spread of input offset which is beneficial for comparator redundancy and reassignment. On the other hand, Figure 2-7b shows the input referred noise also increases for small transistor widths. Figure 2-7 illustrates a tradeoff between noise and offset that is unique to the proposed ADC architecture. The use of large device widths results in lower noise, which improves ADC SNR but also reduces comparator random offset. A smaller random offset requires the ADC to utilize more deliberate offsets, to compensate for the lack of spread from random offset, to achieve sufficiently small granularity for a given dynamic range. In doing so, the amount of SNR degradation due to both thermal noise and non-uniform quantization noise can be minimized but at the expense of increased complexity in comparator design. The choice of device dimensions therefore depends on the target ADC SNR and the number of deliberate offsets employed.
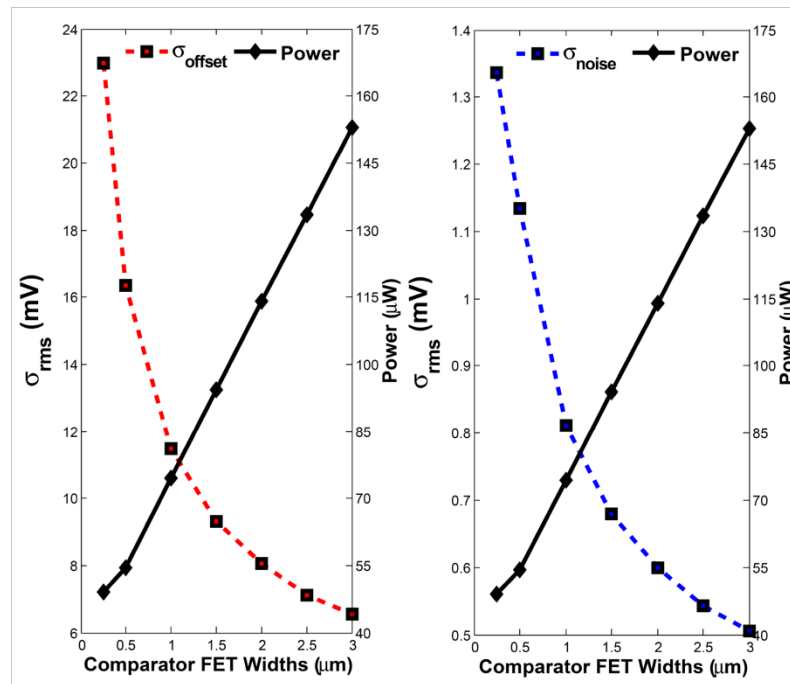
Figure 2-7 Spectre simulated comparator (a) offset, (b) noise and (a & b) power (@ 2GHz, 1V VDD) vs. comparator FET widths for the comparator in Figure 2-2.

Figure 2-8 shows a plot of the effective number of bits (ENOB) of a 7-bit Flash ADC versus the comparator device widths. The data is generated by a Monte-Carlo model of a bank of comparators with a redundancy of five comparators per code and with the most suitable comparator selected for each code. The offset and noise data from Figure 2-7 are used in this model. Each data point in Figure 2-8 is the average ENOB observed for 100 randomly generated ADCs and each of the five curves corresponds to a different number of deliberate offsets employed. For small device widths, the plot shows a low ENOB that is largely independent of the number of deliberate offsets used. A low ENOB at small device widths indicates that ADC performance is dominated by thermal noise. On the other hand for large widths, insufficient random variation in offset results in fewer trip-voltages between deliberate offsets so that ENOB degradation from non-uniform quantization dominates. This effect is more apparent for ADCs employing a small number of deliberate offsets.

For a given target ENOB there exists an optimum combination of the number of deliberate offsets and comparator device size. Figure 2-7 shows that increasing the comparator device widths to mitigate noise and random offset also increases power consumption. Furthermore, Figure 2-8 shows that for a given number of deliberate offsets, there exists a device width that maximizes ADC ENOB. Beyond this point, the power consumption increases with increased device width and unlike traditional flash ADCs, the ADC accuracy for the proposed architecture degrades. This is because there is no longer a large enough random variation in comparator offset to cover the gap between deliberate offsets, causing an increase in quantization noise.

As an example, for device widths of 1μm, Figure 2-7 shows that there is sufficient random variation in comparator offset to require only 16 deliberate offsets to achieve an average ENOB of 6.58 bits. Simulations also indicate that 90% of ADCs achieve an ENOB greater than 6.5 bits. Increasing device widths up to 2μm further improves ENOB but also increases power consumption. Beyond 2μm as shown in Figure 2-8, ADC ENOB degrades because of increasing non-uniform quantization noise. In conclusion, for a target ENOB there exists an optimum combination of the number of deliberate offsets and comparator device size that minimizes design complexity and power.
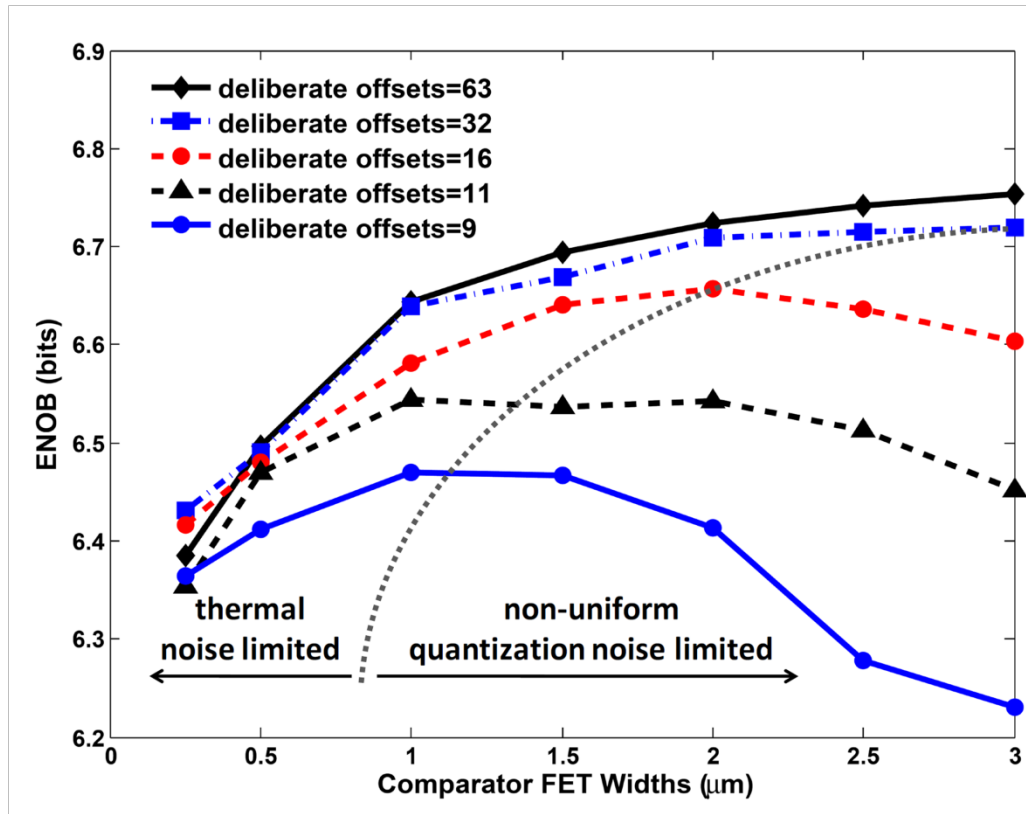
Figure 2-8 Monte-Carlo simulation of ENOB vs. FET widths for 7-bit ADCs using data from Fig. 4 and a redundancy of 5.

2.4 Measurement Results

The prototype, fabricated in a 90nm digital CMOS process, occupies a core area of 1.2mm^2. A die micrograph is shown in Figure 2-9. The prototype is tested as a chip-on-board device to reduce the effects of bond-wire inductance. The prototype ADC has a differential input signal range of 600mVpp and 700mV common mode[3].

Figure 2-10 shows the experimentally measured input referred noise of the proposed comparator. The equivalent input noise is determined by sweeping a differential voltage at the ADC input about a comparator's threshold and averaging the number of logic ones. The data are fitted to a Gaussian distribution. The measurements show 0.3LSB of input-referred RMS comparator noise.

The maximum measured DNL/INL values are 0.70/0.64LSB (Figure 2-11). Figure 2-12 shows a 4096 point FFT spectrum for an input frequency of 750.4MHz sampled at 1.5GHz[4]. Figure 2-13 shows the measured SNDR and SFDR as a function of input frequency at 1.5GS/s. The ADC achieves an ENOB and SFDR of 6.4 bits and 57.7dB at low frequency and 6.05 bits and 46.6dB at Nyquist. There is no measurable degradation in SNDR over 24 hours of operation and the measured BER at 1.5GS/s is less than 2.7x10$^{-15.}$ The ADC consumes a total of 204mW at Nyquist from 1.2V analog and 0.9V digital supplies. The comparator bank and repeaters, TAH and clock buffers, and encoder consume 23%, 25% and 52% of the power, respectively. Table IV shows the performance summary of the prototype ADC.

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[3] The common mode is set by a single off-chip ADC driver that conditions the input signal from both the test equipment and off-chip calibration DAC. This eliminates any common-mode variation between normal operation and calibration.

[4] The output data is decimated by 16X for reliable transmission off-chip. Decimation also explains why the near Nyquist tone falls in a low numbered bin in Figure 2-12.

Table IV ADC ADC PERFORMANCE SUMMARY

Technology	90nm CMOS
Supply Analog/Digital	1.2V/0.9V
Resolution	7bit
Input Range (Differential)	600mV$_{PP}$
Sampling Rate	1.5GS/s
Power Consumption	204mW
DNL/INL	0.7/0.64LSB
SFDR @ Nyquist	46.6dB
SNDR @ Nyquist	38.2dB
ENOB @ Nyquist	6.05
FOM	2pJ/Conv-step
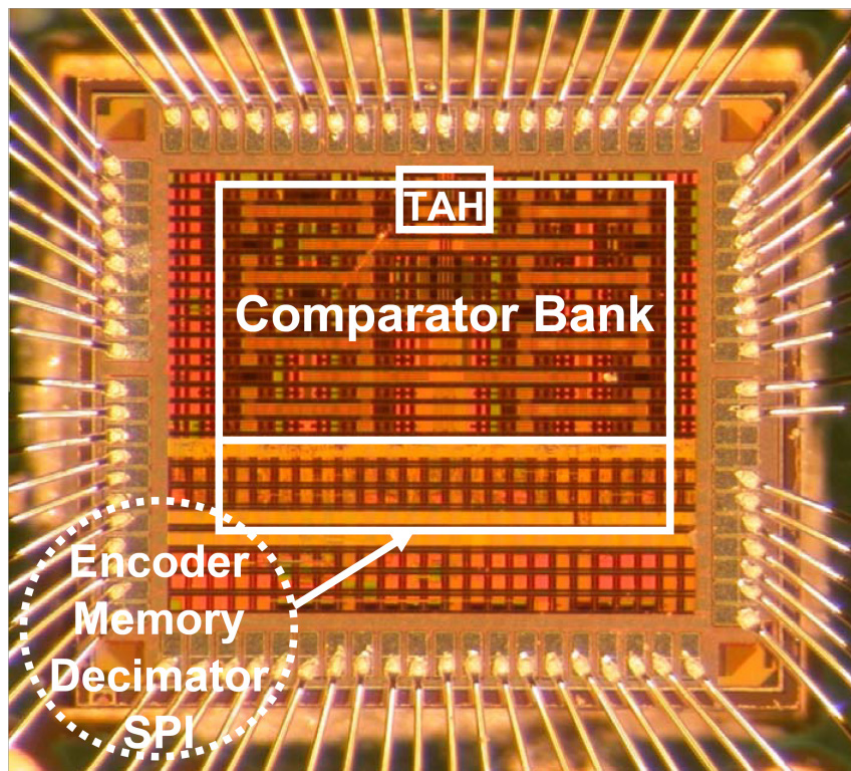
Figure 2-9 Die micrograph of 90nm CMOS ADC.
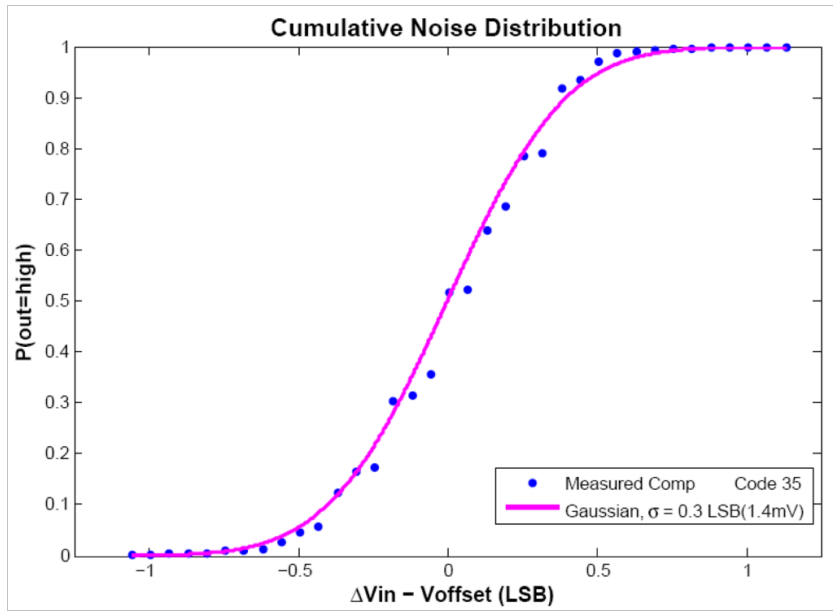
Figure 2-10 Experimental data on comparator cumulative noise distribution and Gaussian fit.
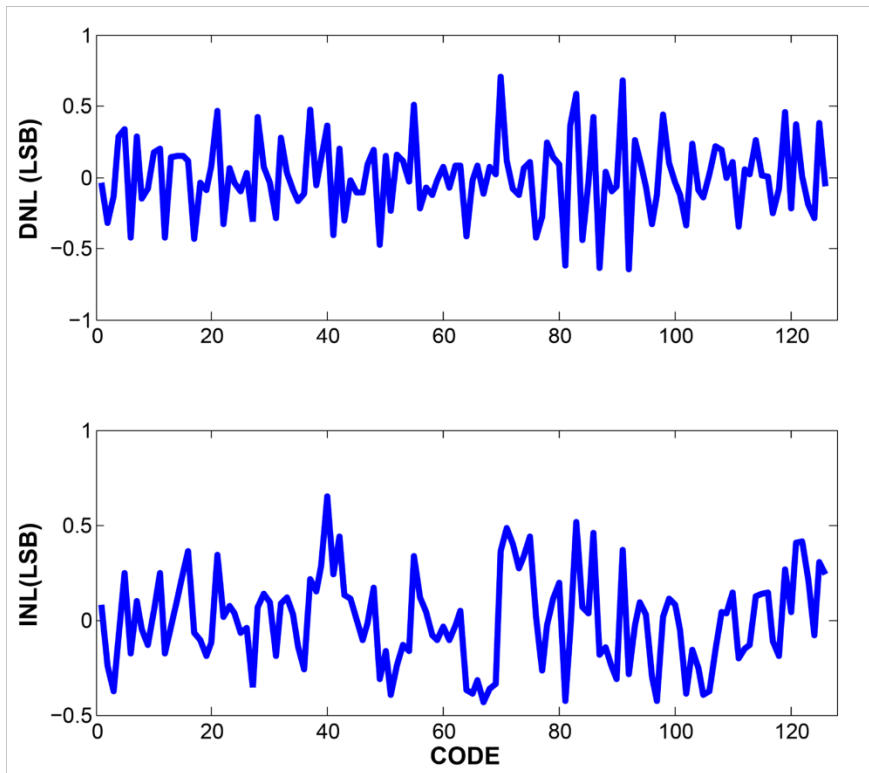
Figure 2-11 Measured DNL and INL.
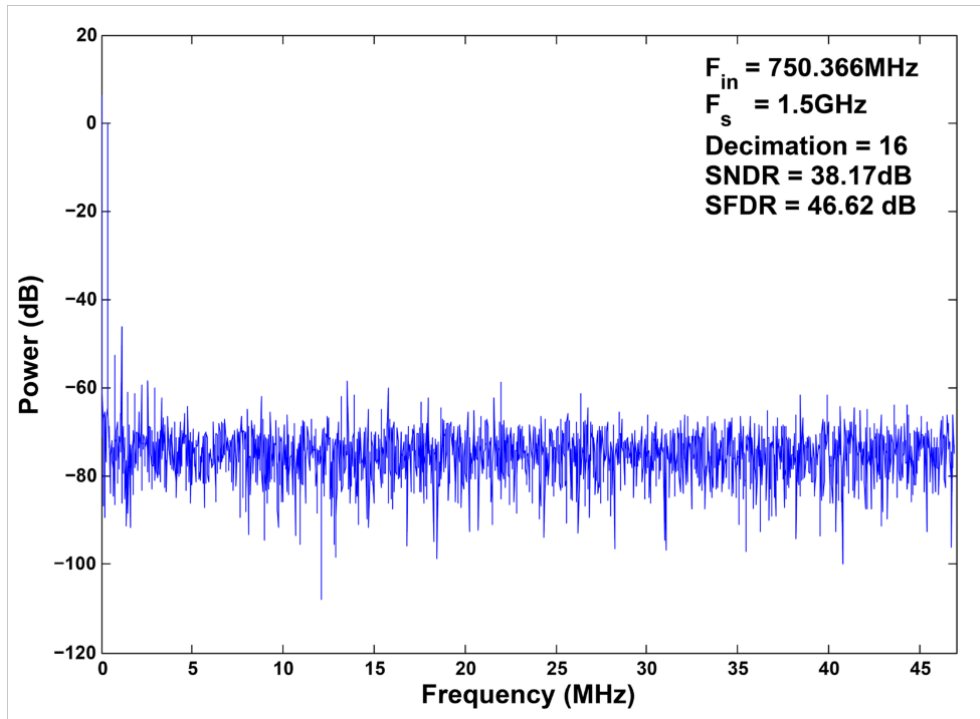
Figure 2-12 4096 point FFT for 750.36 MHz input and 16X decimation.
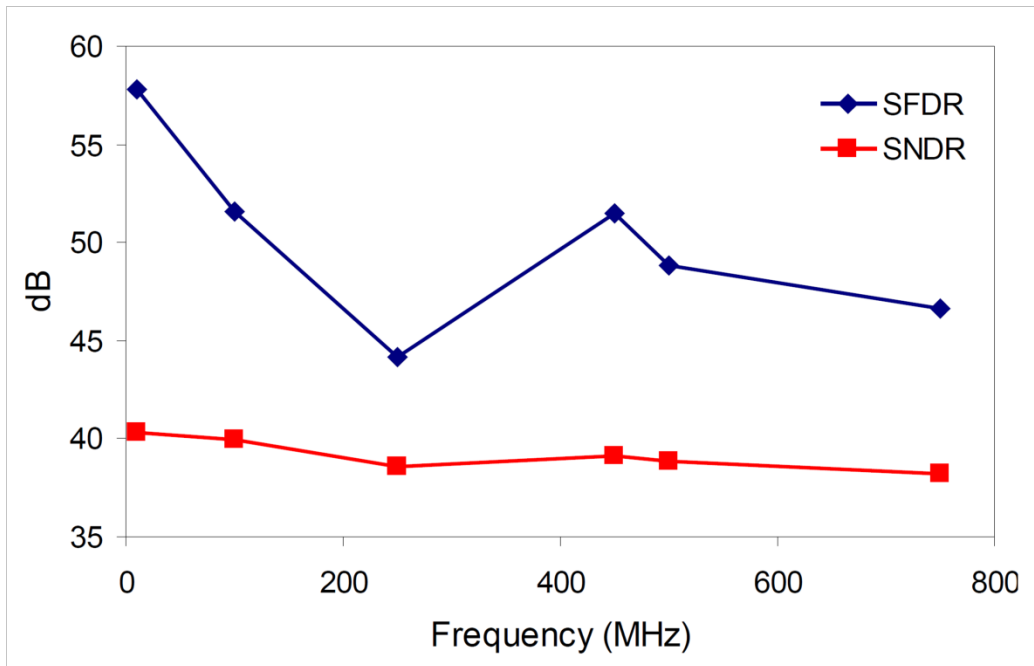
Figure 2-13 SNDR & SFDR vs. Fin (Fs = 1.5GS/s).

CHAPTER 3 A High Feedback Factor Approach for GS/s Pipelining

3.1   Introduction

The flash ADC architecture offers the best solution for Giga-sample per second conversion rates due to the parallel nature of operation. Furthermore, at its core are comparator circuits whose comparison times benefit from the speed advantages of CMOS scaling. However, the exponential dependence of power and area on resolution makes flash ADCs unsuitable for moderate resolutions (i.e. 7-10 bits). On the other hand, the pipeline ADC architecture breaks the conversion processes into stages where each stage resolves a portion of the total resolution. This approach can offer both high speed and moderate resolution with only a linear dependence on area but requires accurate amplification and settling. Furthermore, the high op-amp gain required even in conventional moderate-resolution pipeline ADCs is challenging in 45nm CMOS and finer technologies where the transistor self-gain is ~10 and supply voltage is 1V.

We introduce a new combination of redundancy and pipelining that relaxes the op-amp gain and bandwidth requirements and at the same time facilitates the use of an efficient low-resolution redundancy based flash sub-ADC. This pipelined architecture exploits redundancy to take advantage of compact energy-efficient, digital-like dynamic comparators. The two-stage pipeline reduces the required resolution of the 2nd stage flash sub-ADC to 6 bits so that it can benefit from a redundant comparator design. Pipelining in 45nm CMOS is enabled by a high feedback factor approach, which allows the use of a

simple, low-gain op-amp. This technique enables low power, GS/s performance and moderate resolution with a 1V supply. Furthermore, the front-end sample and hold (SAH) is eliminated to further improve energy efficiency. A 9bit, 1GS/s 45nm SOI-CMOS prototype achieves an ENOB of 7.4b at Nyquist, no missing codes at 9b resolution and consumes only 27mW at 1GS/s from a 1V supply. This non-interleaved 9bit ADC occupies only 0.125mm^2 and achieves a figure of merit (FOM = Power/2^{ENOB} x Fs) of 160fJ/conversion-step at Nyquist.

The chapter is organized as follows. Section 3.2 discusses the benefits of comparator redundancy in a high feedback approach to pipelining in nanometer CMOS. Section 3.3 describes the prototype ADC in detail and discusses its advantages over conventional pipeline ADCs. Section 3.4 describes the circuit details and Section 3.5 presents the measured results of the prototype ADC.

3.2 Comparator redundancy in flash-based pipeline ADCs

Figure 3-1 shows a block diagram of a generic N-bit two-stage pipeline ADC that pipelines an M-bit flash-based MDAC with an (N-M)-bit flash based sub-ADC. In [40] it is shown that a high 1st stage resolution improves ADC linearity because it decreases sensitivity to capacitor mismatch. ADC DNL as a function of capacitor mismatch in the 1st stage is given by [40],

$$DNL = \frac{k \cdot 2^{N - \frac{M}{2}}}{\sqrt{C_{total}}} \qquad 3.1$$

where C_{total} is the sampling capacitance of the 1st stage digital-to-analog (DAC) sub-converter array, k is a technology-dependent parameter [41], and N and M is the total

ADC resolution and 1st stage resolution respectively. For every bit increase in M equation

3.1 shows that ADC DNL improves by $\sqrt{2}$ and illustrates the benefits of a large 1st stage

resolution. A large 1st stage resolution also reduces power, noise and non-linearity

contributions from subsequent stages [42]. For the two-stage pipeline ADC in Figure 3-1,

any noise and non-linearity from the 2nd stage sub-ADC is attenuated by the MDAC gain

2^{M} when referred to the ADC input. Therefore, for every bit increase in M, the 2nd stage

can be scaled for power efficiency. Consequently, a large 1st stage resolution puts the

most stringent gain and bandwidth requirements on the 1st stage MDAC and consumes

the most power. This section discusses the advantages of a high feedback factor approach

in a pipeline ADC for relaxing the 1st stage MDAC gain and bandwidth requirements and

the benefits of combining the technique with a comparator redundancy scheme.
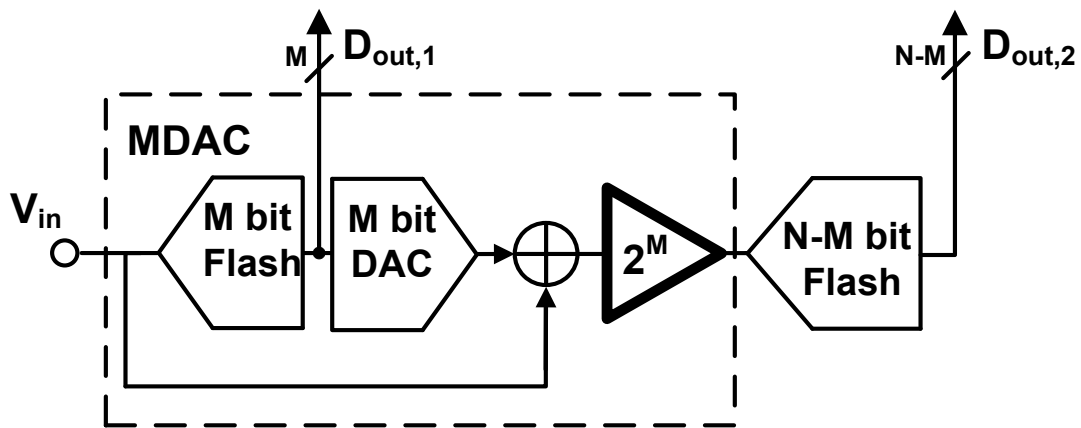
Figure 3-1 Conventional N bit two-stage flash-based pipeline ADC

3.2.1 High feedback factor approach to pipelining

Figure 3-1 shows that for an N-bit pipeline ADC where M bits are resolved in the 1st

stage, an ideal MDAC gain of 2^{M} is required to reuse the entire signal range in the

following stage. Furthermore, assuming 1st order settling behavior at the output, the MDAC gain G as a function of time can be approximated by [43],

$$G(t) \approx 2^M\left(1 - e^{-t \cdot 2\pi f_u \cdot \beta}\right) \quad 3.2$$

where f_u is the unity gain frequency of the MDAC op-amp and β is the MDAC feedback factor. The first term in equation 3.2 is the ideal MDAC gain and the second is the error due to incomplete settling. Since M bits are resolved in the 1st stage, the linearity requirement of the MDAC is dictated by the remaining resolution N-M. To ensure N-M bit linearity at the input to the next stage, the following constraint must hold,

$$e^{-t/(2\pi f_u \cdot \beta)} \leq \frac{1}{2^{N-M}}. \quad 3.3$$

Solving for t in equation 3.2 and defining t_{settle} as the time required to satisfy this constraint gives,

$$t_{settle} \geq (N - M) \cdot \ln(2) \cdot 1/(2\pi f_u \cdot \beta). \quad 3.4$$

To account for the 1st stage sub-ADC decision time, the settling time t_{settle} must be met within a fraction K of the MDAC hold phase. This phase is generally equal to half the clock period of the sampling clock with period T_{clk}. Therefore, for $\beta = 1/(1+2^M)$ where 2^M is the MDAC gain, the op-amp bandwidth requirement is given by,

$$f_u \geq (N - M) \cdot (1 + 2^M) \ln(2) \cdot 2F_S/(2\pi \cdot K) \quad 3.5$$

where $Fs = 1/T_{clk}$ is the ADC sampling rate. Equation 3.5 shows that for a given sampling rate and ADC resolution, the required bandwidth for the front-end MDAC op-amp depends on the number of bits resolved in the 1st stage. This is because although

remaining stage resolution N-M decreases linearly for every bit resolved in the 1st stage, the MDAC gain requirement of 2^M increases exponentially. Therefore the increase in the MDAC gain requirement is not offset by the lower bit-accuracy requirement. A unity gain frequency ranging from 16GHz to 32GHz is required for a 1GS/s 7-10b pipeline ADC (i.e. moderate resolution) where 4 bits are resolved in the 1st stage and 150ps (i.e. K = 0.7) is allocated to the sub-ADC decision time. Although this may be conceivable in nanometer CMOS where the device f_T ranges in the hundreds of gigahertz, power concerns may prohibit a practical implementation. Furthermore, a low supply voltage coupled with op-amp gain requirements prohibits sufficient signal swing to the subsequent stage. This in turn prohibits a conventional pipeline approach where it is desirable to reuse the entire signal range in the subsequent stage.

For an N-bit pipeline ADC where M bits are resolved in the 1st stage, the op-amp gain (a_o) requirement is determined by the following relation that limits ADC errors from finite gain to within 1/2 LSB of the remaining stage resolution [43],

$$1/2^{N-M} \geq 1/(1 + a_o\beta). \qquad 3.6$$

Solving for a_o and using feedback factor $\beta = 1/(1+2^M)$ gives,

$$a_o \geq (2^{N-M} - 1) \cdot (1 + 2^M). \qquad 3.7$$

For a 4b 1st stage MDAC, equation 3.7 yields an op-amp gain requirement between 40dB and 60dB for pipeline ADCs with 7-10b resolution (i.e. moderate resolution). Furthermore, the 1st stage gain requirement is roughly independent of the stage resolution [43]. This is because the exponential increase in the allowed gain error $1/2^{N-M}$ is

approximately offset by the exponential decrease in the feedback factor $\beta = 1/(1+2^M)$. For a nanometer CMOS processes with low supply voltage, a multi-stage op-amp approach can be employed to achieve the required gain and at the same time maintain sufficient MDAC output swing. However, complex compensation schemes prohibit GS/s operation [44].

Equations 3.5 and 3.7 shows that the op-amp gain and bandwidth requirement is inversely proportional to the feedback factor (i.e. $1/\beta=1+2^M$). Therefore, a high feedback approach [45] can be used to relax the op-amp gain and bandwidth requirements. For example, resolving 4bits in the 1st stage yields a feedback factor $\beta = 1/(1+2^4) = 1/17$ in the conventional approach. However in a high feedback factor approach, reducing the MDAC gain from 16 (i.e. 2^4) to 2 increases the feedback factor to $1/(1+2) = 1/3$. Therefore, for the same settling time t_{settle} (equation 3.4) the op-amp bandwidth can be reduced by 5.7X. Similarly, for the same gain error (equation 3.6) the op-amp gain can be reduced by 5.7X. This makes a single-stage op-amp implementation realizable for GS/s pipelining in nanometer CMOS with a low supply voltage [33]. Furthermore, the reduced MDAC swing enables extensive cascoding in the op-amp design for enhanced gain.

3.2.2 Comparator redundancy

Offset from device mismatch is discussed in section 1.3.2 and equation (1.4) quantifies its value based on device dimensions and process-dependent mismatch coefficient factor A_{VT}. For a 6b flash sub-ADC with a 64LSB input range and a target ADC ENOB of 5.5b[5], a limit on the input referred comparator offset is be given by,

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[5] Based on MATLAB simulations that determine the yield of a 6b flash ADC with respect to offset.

$$\sigma_{offset} \approx \frac{A_{V_T}}{\sqrt{W \cdot L}} \leq 1/4 \cdot LSB \qquad \textbf{3.8}$$

In section 1.3.5, a resistive averaging scheme for averaging out mismatch error sources is discussed. Section 1.3.5 also discussed a resistive interpolation scheme for reducing the number of pre-amplifiers at the ADC input. These commonly employed[6] techniques relax the input referred offset requirements of the pre-amplifiers by up to 3X [12] and ADC input capacitance by a factor that is inversely proportional to the interpolation factor. The total comparator input capacitance of an N-bit sub-ADC with resistive averaging and interpolation is given by,

$$C_{in\_avg} \approx \frac{2}{3} C_{ox} WL \left(2^N / \eta + D \right) \qquad \textbf{3.9}$$

where W and L are the dimensions of the preamplifier input pair, D is the number of dummy preamplifiers at the reference edges, η is the interpolation factor and C_{ox} is the gate capacitance per unit area. In a typical 45nm CMOS process, C_{ox} is ~20fF/μm^2 and A_{VT} is ~4.3mV (Figure 1-9). TABLE V gives input pair widths and total comparator input capacitance (in fF) for different input signal ranges (in milli-volts) for a 6b flash ADC. In this example, the ADC employs resistive averaging, 4X interpolation (i.e. $\eta = 4$) and 6 dummy pre-amplifiers (i.e. $D = 6$) for over-ranging[7]. The data uses minimum length devices (i.e. 45nm) for the input pair (see Figure 1-7) which is desirable for high speed operation. TABLE V shows that the total input capacitance increases significantly at input ranges less than 400mV because of increased offset requirements dictated by equation

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[6] In this chapter, a conventional flash ADC is a regarded as a flash ADC that incorporates resistive averaging and interpolation.
[7] These parameters are in-line with recent work on 6b flash ADCs [15].

(3.8)[8] and the LSB dependence on the input signal range (i.e. LSB $= V_S/2^N$). For example, an input capacitance of ~1pF results for a 6b flash ADC with a 200mV input range.

TABLE V INPUT PAIR WIDTHS AND TOTAL INPUT CAPACITANCE OF A 6b FLASH ADC WITH 5.5 ENOB FOR DIFFERENT INPUT RANGES

Vs (mV)	200	400	600	800	1000
W (µm)	75	19	8	5	3
Cin (fF)	972	243	108	61	39

On the other hand, exploiting the effects of V_T mismatch by leveraging comparator redundancy eliminates the comparator matching requirements. This enables the use of low precision comparators with small device widths to reduce input capacitance, and to increase offsets enough for redundancy and reassignment. A conceptual block diagram is shown in Figure 3-2. Redundancy and reassignment [16], [17] involve the assignment of multiple comparators, from a bank of low precision comparators, to each ADC code and using a code search calibration algorithm to find comparators that are closest to the desired trip-points.

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[8] This includes a 3X reduction [12] in the offset requirement that results from resistive averaging.
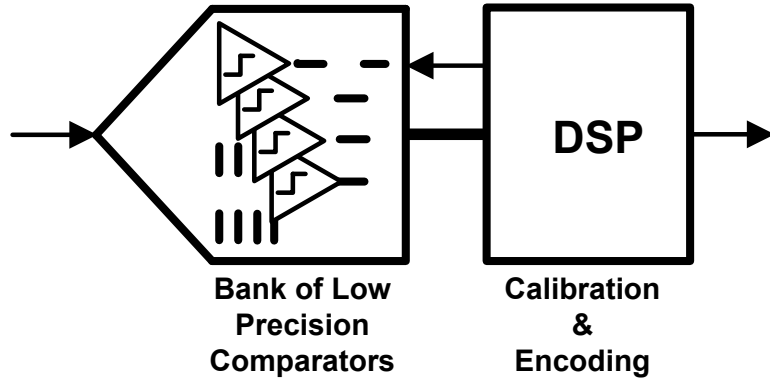
Figure 3-2 Conceptual block diagram of comparator redundancy.

The total comparator input capacitance of an N-bit sub-ADC with comparator redundancy is given by[9],

$$C_{in\_redun} = C_{ox}WL(2^N - 1) \cdot R \qquad 3.10$$

where R is the amount of redundancy. Comparing the input capacitance of a redundancy-based flash ADC with a conventional flash ADC by taking the ratio of equations 3.10 and 3.9 gives,

$$C_{in\_redun}/C_{in\_avg} = W_{redun}/W_{avg} \cdot 3/2 \cdot R \cdot \eta/(1 + D \cdot \eta \cdot 2^{-N}) \; 3.11$$

For a 6b flash ADC with comparator redundancy of $R=4$, setting $C_{in\_redun}/C_{in\_avg} = 1$ in equation 3.11 shows that the input pair widths W_{redun} can be 17.4X smaller than W_{avg} for the same ADC input capacitances shown in TABLE V. For the case of a 200mV input range, a ratio of 1 in equation 3.11 yields a comparator input pair width of 4.3μm for W_{redun} compared to 75μm for W_{avg}. However, with comparator redundancy only thermal

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[9] Assumes dynamic comparators in the reset phase where total gate capacitance (i.e. $C_{ox} \cdot WL$) applies.

noise limits ADC performance [32]. Therefore, device widths can be scaled down even further as long as the target ADC SNR is maintained and as long as device widths are above the minimum value as dictated by the technology. In practice and for the case of a 6b redundancy-based flash ADC with redundancy of four and a 200mV input range, this leads to an additional 6.4X reduction in device widths for a 110X total reduction (i.e. 17.4 x 6.4 ≈ 110) when compared to a device width of 75μm for the conventional case shown in TABLE V. Furthermore, this translates to a 6.4X lower input capacitance when compared to the conventional case of ~1pF.

3.2.3 A new combination of pipelining and redundancy

In this section it will be shown that a 2nd stage 6b redundancy-based flash sub-ADC facilitates a high feedback factor approach in a 1st stage 4b MDAC. This new combination of pipelining and redundancy can be leveraged to enable 1GS/s pipelining and a moderate resolution of 9 bits with only a two stages. In this scheme, the conventional architecture of Figure 3-1 is replaced with the 9-bit two-stage pipeline ADC architecture shown in Figure 3-3. This architecture pipelines a 4-bit flash-based MDAC with a 6-bit redundancy-based flash second stage sub-ADC[10]. Furthermore, the MDAC is implemented with a gain of 2 instead of 16. The benefits of this architecture are discussed next.

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[10] 1-bit 2nd stage over-ranging is assumed.
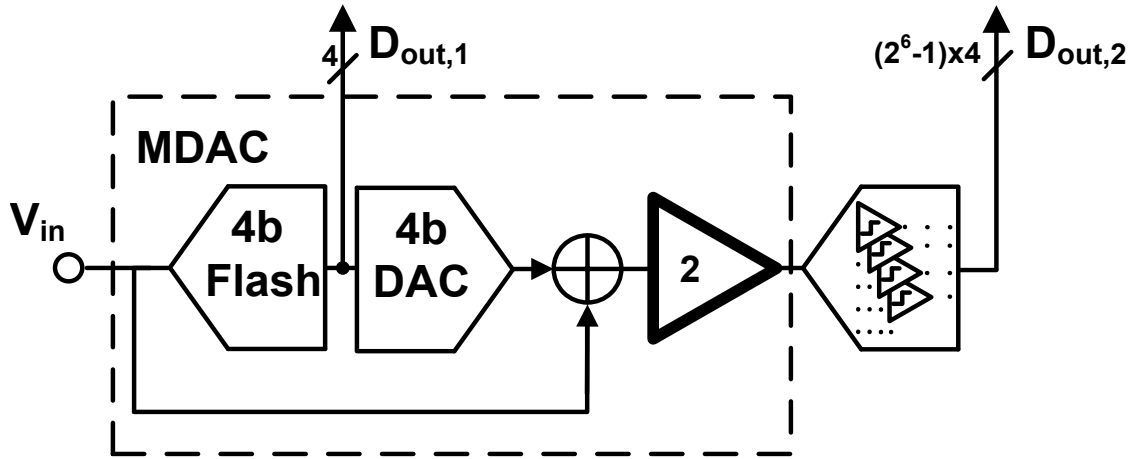
Figure 3-3 A 9b two-stage pipeline ADC with reduced MDAC gain and redundancy-based flash sub-ADC.

Equation 3.6 in section 3.2.1 shows that for a conventional 9 bit pipeline ADC (i.e. N=9 bits), the op-amp in the 1st stage 4b MDAC should achieve a gain of 527 (54.4dB) to limit the ADC error due to finite op-amp gain to within 1/2 LSB of the remaining stage resolution. A gain of this magnitude is difficult to achieve with a single-stage op-amp in a nanometer CMOS process because of the low supply voltage and low intrinsic device gain in these nodes. This is exacerbated by leading edge processes that do not allow channel lengths to be increased (for increased r_o) beyond the minimum dimension defined by the technology. However, equation 3.6 also shows that increasing the feedback factor $\beta=1/(1+2^M)$, where M is the 1st stage resolution (i.e. 4 bits), relaxes the op-amp gain requirement for the same gain error $1/2^{N-M}$, where N-M is the remaining ADC resolution (i.e. 5 bits).

Therefore, implementing the 1st stage 4b MDAC with a gain of 2 instead of 16 and increases the feedback factor (β) from 1/17 to 1/3. This high feedback factor approach

[45] has two advantages with regards to op-amp gain. First, the op-amp gain can be relaxed by 5.7X to 93 (39.4dB) for the same gain error. Second, the reduced MDAC gain yields a reduction in the op-amp output swing and enables extensive cascoding in the op-amp design for enhanced gain. These benefits enable a single-stage op-amp design to achieve the required gain even in 45nm CMOS where the self gain is ~10 and supply voltage is 1V.

Increasing the feedback factor (β) from 1/17 to 1/3 also relaxes the op-amp bandwidth requirement f_u by 5.7X. Equation 3.5 in section 3.2.1 shows that for a 1GHz sample rate and 5-bit settling[11] at the op-amp output, the required op-amp unity gain frequency is reduced from 26.8GHz to 4.7GHz. For the same settling accuracy and for $f_u = G_m/C_L$, this enables up to a 5.7X reduction in op-amp transconductance G_m and translates to reduced op-amp power dissipation.

However, the 5.7X reduction in the MDAC feedback factor reduces its output swing by 4X[12]. Therefore, the 2nd stage sub-ADC no longer utilizes the entire reference range. For a conventional 2nd stage flash sub-ADC, this would lead to more stringent comparator offsets requirements and in turn to increased sub-ADC input capacitance. For a 6b flash ADC that incorporates resistive averaging, interpolation and a nominal input-range of 800mV, TABLE V in section 3.2.2 shows that a 4X reduction in input range yields 16X increase in input capacitance. This is because the 4X reduction in the MDAC output swing increases the sub-ADC offset requirement by 4X as dictated by equation 3.8. This in turn yields a 16X increase in comparator input pair widths W (in equation 3.8) which

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[11] 150ps is allocated to 1st stage sub-ADC decision time in equation 3.5 (i.e. $K = 0.7$).
[12] 1b over-ranging in the 2nd stage sub-ADC doubles the 1st stage MDAC output swing resulting in a 4X output swing reduction instead of 8X.

translates to a 16X increase in sub-ADC input capacitance C_{in_avg} (in equation 3.9) as shown in TABLE V. Therefore, a conventional 6b flash ADC with a 200mV input range requires the same accuracy as a conventional 8b flash ADC with 800mV input range (i.e. $\frac{200mV}{2^6} = \frac{800mV}{2^8}$).

For a 1st stage MDAC op-amp unity gain frequency $f_u = G_m/(2\pi C_L)$, a 5.7X reduction in the bandwidth requirement (f_u) is offset by a 16X increase in 2nd stage sub-ADC input capacitance (C_L) if a conventional flash ADC is used. Therefore, for the same bandwidth[13], the op-amp transconductance G_m must be increased by almost 3X (i.e. 16/5.7). This translates to a ~3X increase in op-amp power. Therefore, a conventional flash architecture is not suitable as a high-resolution 2nd stage sub-ADC when a high feedback factor is utilized in the 1st stage MDAC.

On the other hand, by leveraging redundancy and reassignment in a flash ADC, comparator, matching requirements are eliminated altogether and only thermal noise limits ADC SNR. For example, a 6b flash ADC incorporating a comparator redundancy of R=4 with a 200mV input range yields a 6.4X lower input capacitance compared to the conventional case in TABLE V. Therefore, for the same bandwidth, the op-amp transconductance G_m can be decreased by more than 2X (i.e. (16.5/6.4)/5.7). This translates to more than a 2X reduction in op-amp power. Therefore, a flash architecture incorporating comparator redundancy is suitable as a 6b 2nd stage sub-ADC when a high feedback factor is utilized in the 1st stage MDAC. Another advantage of comparator redundancy is the simplification in the sub-ADC architecture. Since no pre-amplifiers or averaging networks are required, simple dynamic comparators optimized for speed, area

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[13] For simplicity, it is assumed that the C_L dominates the total capacitance at the MDAC output.

and power efficiency can be used. Finally, the use deliberate and random offsets to set comparator trip-points [32] eliminates the need to generate the 2nd stage references.

3.3   Proposed ADC Architecture
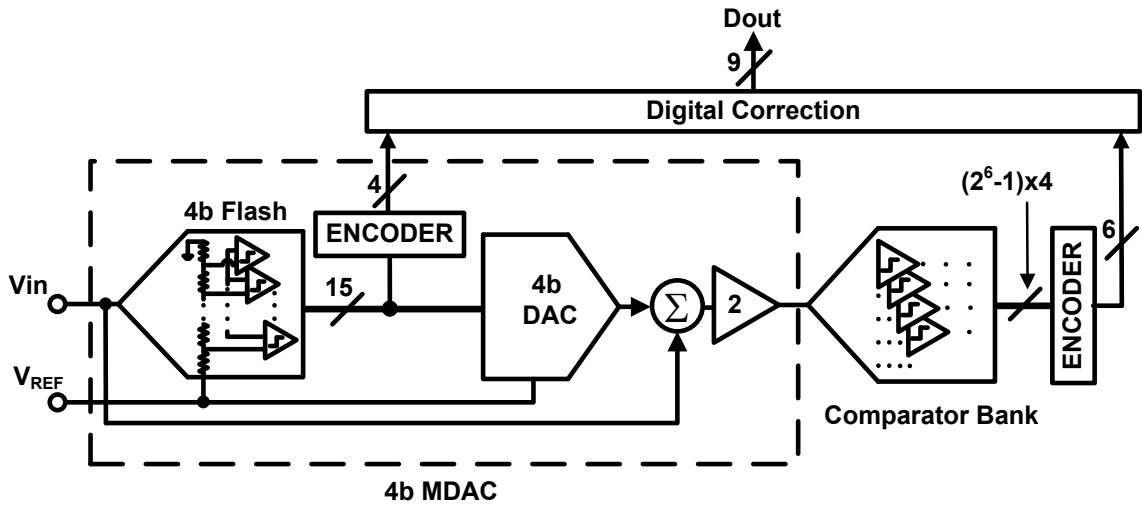
Figure 3-4 Simplified single-ended representation of proposed ADC architecture.

The proposed pipeline ADC architecture leverages the linearity and power advantages of a high-resolution front-end stage [40], [42] as well as the power efficiency of a 6b redundancy based flash ADC. Figure 3-4 shows the proposed two-stage pipeline ADC architecture. A 4b flash-based MDAC is pipelined with a 6b flash ADC sub-converter. Unlike the conventional approach, the 1st stage MDAC has a gain of only two instead of sixteen and relaxes the op-amp gain and bandwidth requirement. A high feedback factor in the 1st stage MDAC and the resulting reduction in op-amp power consumptions are

enabled by an efficient 2nd stage redundancy-based flash sub-ADC. This approach is key to exploiting the performance of a 45nm SOI process to enable GS/s moderate resolution conversion with two stages and thus avoid the need for additional pipeline stages. The 2nd stage 6bit flash sub-ADC requires no reference ladder and employs redundancy and re-assignment to achieve a low second-stage FOM of only 170fJ/conversion-step. Similarly, comparator redundancy improves the energy efficiency and presents a low input capacitance of the 1st stage sub-ADC. A 1bit over-range in the 2nd stage sub-ADC compensates for 1st stage comparator offsets. Finally, a simple clock skew correction block corrects timing mismatch in the sampling paths of the MDAC and its sub-ADC, allowing the elimination of a power-hungry conventional front-end sample and hold (SAH). This section analyzes the individual sub-blocks.

3.3.1   1st stage 4b flash-based MDAC

Figure 3-5 shows a simplified schematic of the 1st stage 4b MDAC, its 4b sub-ADC and timing waveforms. An array of unit capacitor, C_S, serves as the input sampling capacitance for the 4b MDAC. Similarly, a second array of capacitors C_S serves as the input sampling capacitors for the comparators that form the 4b flash sub-ADC. The sub-ADC utilizes a 15-tap resistor reference ladder for generating the 1st stage comparator trip-points.
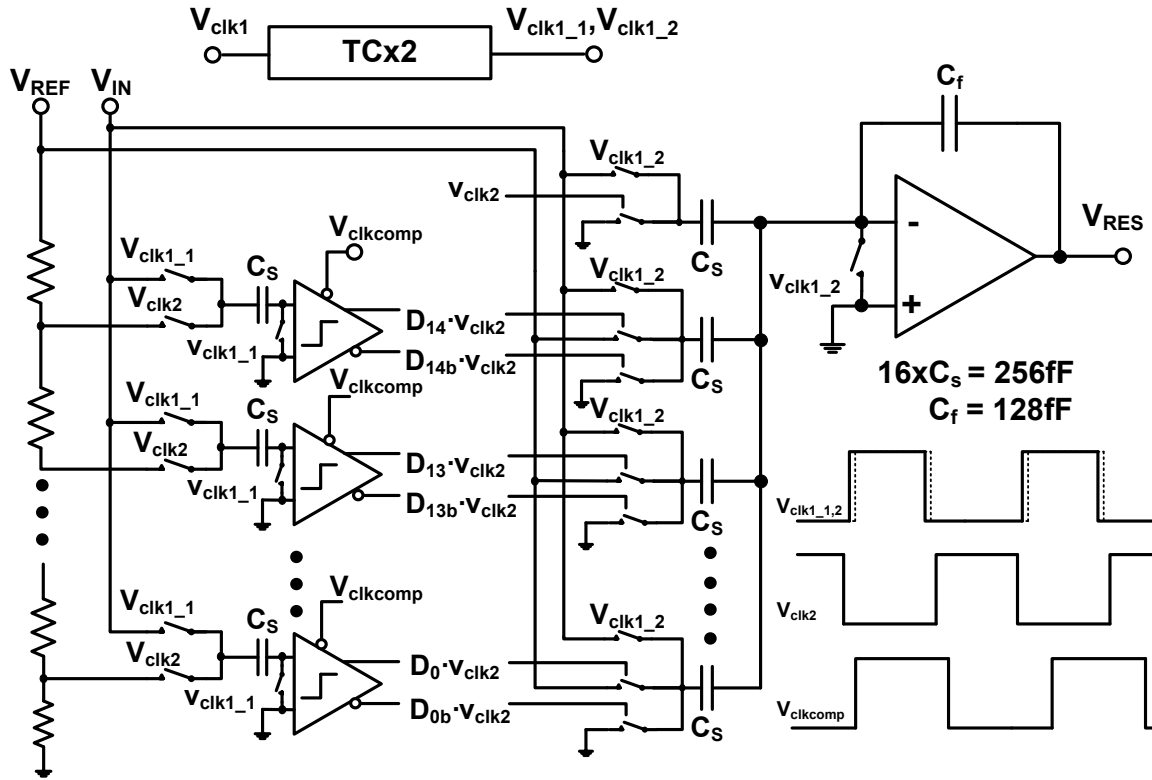
Figure 3-5 Simplified single-ended representation of differential 4-bit MDAC.

When V_{clk1} is high, the sampling capacitors C_S in both the MDAC and its sub-ADC track the input via their respective input sampling switches. The input sampling switches in both the MDAC and its sub-ADC are not boot-strapped. Instead, simple pass gates and a low ADC common-mode input enable sufficiently low on-resistance to achieve 10-bit linearity for a 1GHz, 800mVpp differential input signal. The track-to-hold instant occurs at the falling edge of V_{clk1}. Since this design does not utilize a dedicated front-end sample and hold (SAH), two techniques are implemented to mitigate timing mismatch between the MDAC and its sub-ADC. First, aperture errors due to bandwidth mismatch in the input signal paths are minimized by matching the sampling networks of the 1st stage MDAC and its sub-ADC. Second, any clock skew between the 1st stage MDAC and its sub-ADC is corrected with simple digital trimming of a delay chain in the clock paths

and will be described in detail in section 3.3.4. The rising edge of V_{clk2} couples the flash sub-ADC reference voltages onto each of the comparator's sampling capacitors. The difference between the comparator reference voltages and sampled input signal are then coupled to the sub-ADC comparator inputs. A short delay between the rising edge of V_{clk2} and the falling edge of V_{clk_comp} allows adequate settling of the resistor ladder prior to the sub-ADC comparison. The sub-ADC comparator outputs then drive the MDAC reference switches to produce the residue V_{RES} at the output.

3.3.2 1st stage 4b flash sub-ADC

1bit redundancy in the 2nd stage sub-ADC enables a maximum 1st stage comparator offset of ±1/2LSB where the LSB is the resolution of the 1st stage sub-ADC. In this design, the 1st stage 4b sub-ADC incorporates a redundancy of two comparators per level instead of the conventional one per level as shown in Figure 3-6. The advantage of this approach are discussed next.
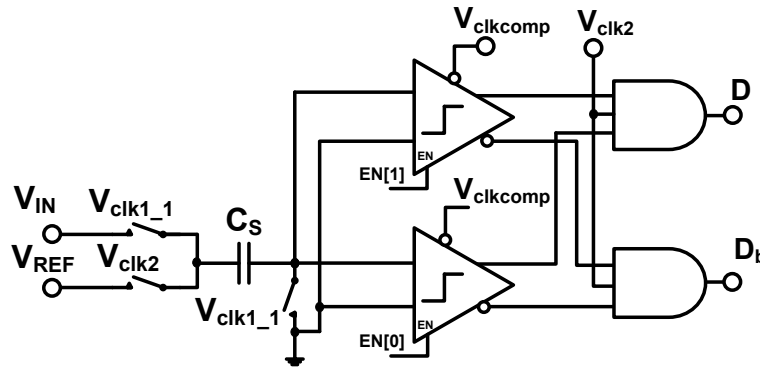
Figure 3-6 Simplified single-ended representation of 1st stage sub-ADC comparator with a redundancy of two comparators per code.

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Figure 3-7 shows a plot of the yield of a 1st stage 4bit MDAC versus 1st stage sub-ADC comparator offset. The three curves in Figure 3-7 represent three different implementations for the 1st stage sub-ADC. These implementations consist of a conventional 4bit flash sub-ADC, a redundancy-based 4bit flash sub-ADC with redundancy of two, and a redundancy-based 4bit flash sub-ADC with redundancy of three. The data is generated with a Monte-Carlo model of three banks of comparators with one, two and three comparators per code. For the case of the redundancy-based flash sub-ADCs, the most suitable comparator is selected for each code. The comparator offset is normalized to the resolution of the sub-ADC and each point in Figure 3-7 is the number of ADCs observed for 100 randomly generated ADCs whose offsets result in a MDAC residue that does not exceed the 2nd stage correction range.
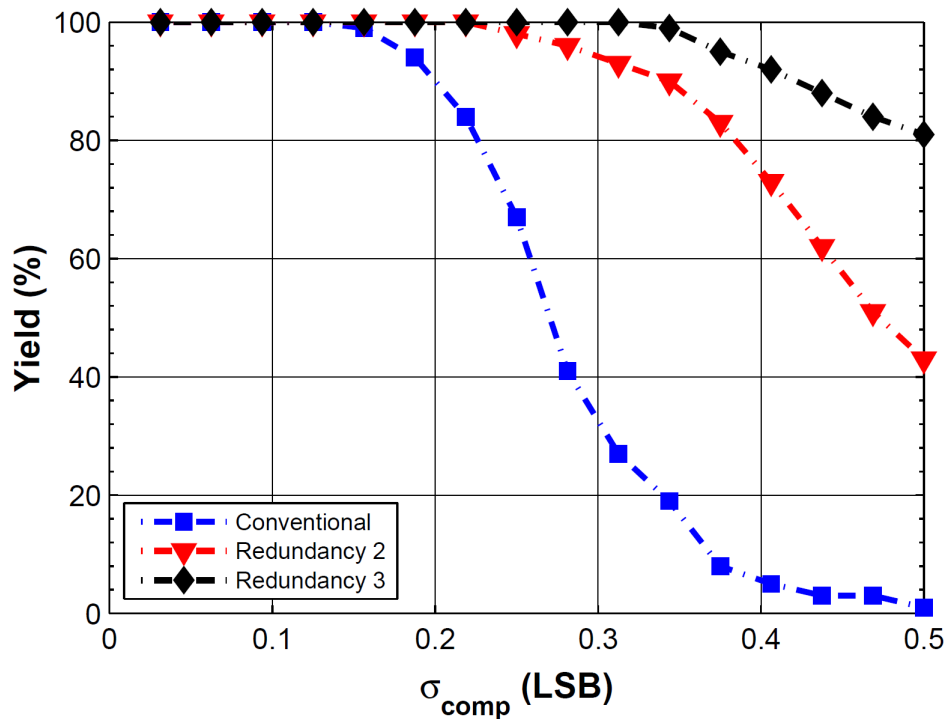
Figure 3-7 Monte-Carlo simulation of Yield of a 4bit MDAC vs. Comparator Offset.

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For a 90% yield, Figure 3-7 shows that the conventional approach requires an offset less than 0.2LSB. For a redundancy of two, the offset can be as high as 0.35LSB for the same yield. This translates to a 33% reduction in total capacitance and area of the input pair when compared to the conventional approach. For a sampling capacitor C_S and comparator input capacitance C_{comp}, an attenuation of the sampled input signal by a factor of $C_S/(C_{S+}\ C_{comp})$ occurs and is due to charge sharing when transitioning from track-to-hold. Therefore, for the same attenuation, a redundancy of two enables the use of smaller sampling capacitors in the 1st stage sub-ADC. Comparators with the lowest offset are chosen at startup.

3.3.3   2nd stage 6b redundancy-based flash sub-ADC
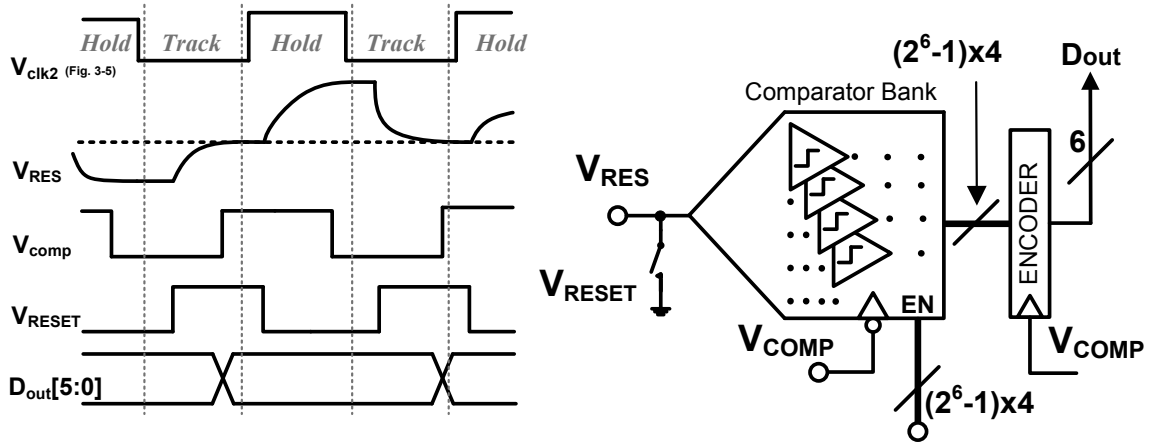
Figure 3-8 Simplified single-ended representation of 2nd stage 6b sub-ADC architecture with redundancy of four comparators per code.

Figure 3-8 shows a simplified block diagram of the 2nd stage sub-ADC and timing waveforms. At the falling edge of V_{COMP}, the 1st stage MDAC residue is processed by a flash ADC that incorporates redundancy and reassignment to correct DNL errors [16].

Furthermore, no reference ladder is required since the comparators trip-points are set by a combination of deliberate and random mismatch [32]. At startup, a calibration routine finds the comparators closest to the desired trip-points. An encoder block, comprised of full adders, resolves the comparator outputs to the 6-bit sub-ADC output code. The signal V_{RESET} shorts the differential inputs of the 2nd stage sub-ADC and the differential outputs of the 1st stage MDAC. This serves three purposes. First, it mitigates SOI memory effects stemming from the comparator input pair which consists of floating body devices. Second, it prevents any slewing at the op-amp outputs that may occur between the rising edge of V_{clk2} and the 1st stage sub-ADC decision. During this time, the 1st stage comparator outputs have not made a decision and the residue that is generated may cause the op-amp outputs to slew. Third, it mitigates signal dependent settling errors at the MDAC output and allows any incomplete settling to be corrected when calibrating the 2nd stage sub-ADC through the 1st stage MDAC. This will be discussed in detail in section 3.3.5.

To minimize the load of the 1st stage MDAC, it is beneficial to minimize both the amount of comparator redundancy R (in equation 3.10) and the comparator input pair the device widths W (in equation 3.10). Furthermore, relying more on random offset to cover the spread in between deliberate offsets facilitates the design of the 2nd stage sub-ADC comparators because fewer deliberate offsets need to be employed. However, these parameters are dictated by a target ADC SNR. A 1st stage MDAC gain of two relaxes the thermal noise requirements of the 2nd stage sub-ADC by a factor of two for the same degradation in ADC SNR. Therefore, further reduction in device widths can be employed

for increasing comparator random offset[14] and for reducing comparator input capacitance. For a 6b flash ADC, 0.25LSB of input referred comparator noise yields 2.4dB degradation in ADC SNR[15]. With an MDAC gain of two, thermal noise from the 2nd stage sub-ADC can be up to 0.5 ADC-LSB for the same ADC SNR.

For an 800mVpp ADC input range, a 4X reduction in the MDAC output swing yields a 2nd stage sub-ADC input range of 200mVpp. Furthermore, because the 2nd stage sub-ADC resolution is 6bits, this means that 1 sub-ADC LSB is equivalent 2 ADC-LSBs (i.e. $1\text{LSB} = \frac{800mV/4}{2^6} = \frac{800mV}{2^8} = \frac{2 \cdot 800mV}{2^9} = 2\text{ADC-LSBs}$). For the comparator circuit used in the 2nd stage sub-ADC, Spectre Monte-Carlo simulations indicate a comparator offset of 17 ADC-LSBs (i.e. 8.5 sub-ADC LSBs) when sized for 0.5 ADC-LSB of circuit noise[16]. Figure 3-9 shows a plot of the yield of a 6 bit redundancy-based flash sub-ADC that incorporates deliberate and random offset for setting comparator trip point versus the number of deliberate offsets employed. The data is generated by a Monte-Carlo model of three banks of comparators with three, four and five comparators per code and 7.5LSB[17] of input referred random offset. Each point in Figure 3-9 is the percentage of 100 randomly generated ADCs with ENOB greater than 5.6 for a given redundancy and number of deliberate offsets. The data shows that a comparator redundancy of four and only eight deliberate offsets are sufficient to ensure SNR degradation from non-uniform quantization noise to less than 2.4dB with 90% yield.

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[14] A large random variation in comparator offset is beneficial for a redundancy and reassignment scheme.
[15] Quantization noise for an N bit ADC is 0.288LSB. For a 6b ADC, 0.25LSB of input referred thermal noise equates to an $SNR = 20\log\left(\frac{64LSB/2\sqrt{2}}{\sqrt{(0.288LSB)^2+(0.25LSB)^2}}\right) = 35.47dB$, a 2.4dB reduction from the ideal ADC SNR.
[16] Based on Spectre transient noise simulations.
[17] 2nd stage comparator offset of 15 ADC-LSBs is attenuated by an MDAC gain of two when referred to the ADC input (i.e. 15 ADC-LSBs = 7.5 sub-ADC LSBs).

In this design, a comparator redundancy of four is utilized in the 2nd stage redundancy-based flash sub-ADC, yielding only 180fF of gate capacitance from 288 comparators[18]. Therefore, the proposed sub-ADC architecture effectively decouples comparator performance from device matching requirements to yield a sub-ADC input capacitance that is ~6X lower than a conventional 6b flash ADC incorporating resistive averaging and interpolation and at the same time limits SNR degradation from thermal and non-uniform quantization noise to less than 4dB (i.e. 5.35 ENOB).
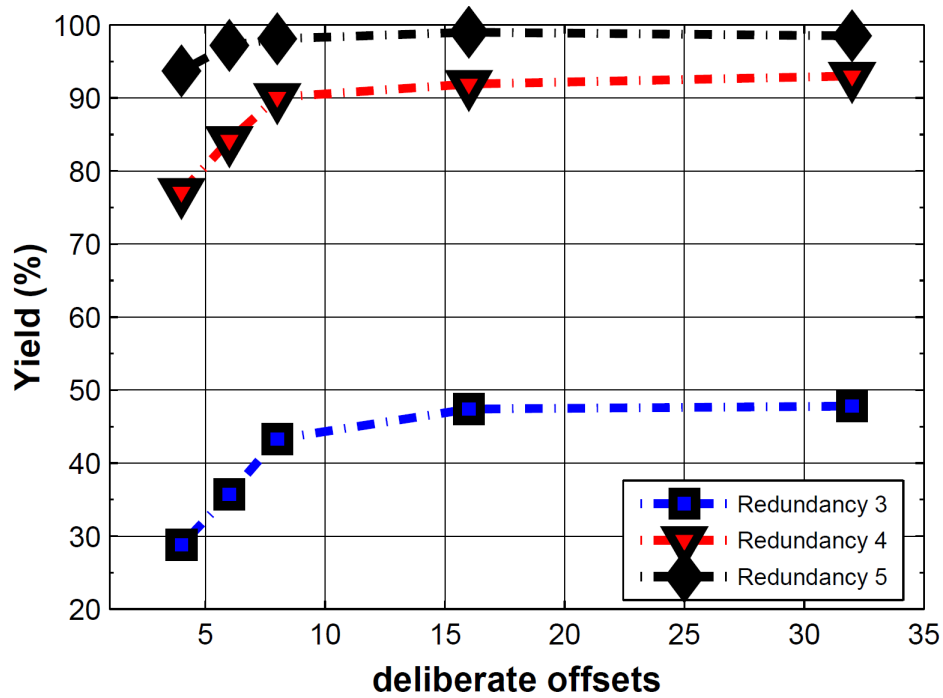
Figure 3-9 Monte-Carlo simulation of Yield of a 6bit redundancy-based flash ADC vs. number of deliberate offsets for setting comparator trip-points.

3.3.4 Elimination of SAH

In a SAH-less pipeline ADC architecture, phase mismatch and clock skew in the sampling paths between the 1st stage MDAC and its sub-ADC must be minimized to

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[18] The architecture utilizes additional comparators at the end codes for mitigating edge effects [16].

prevent sub-ADC decision errors that cause the MDAC residue to exceed the 2nd stage

sub-ADC correction range. If the correction range is exceeded, missing codes in the ADC

will occur and results in ADC SNDR degradation. An input signal bandwidth that is

much larger than the maximum input signal frequency makes any phase errors due to

mismatch in the signal paths to be negligible. Furthermore, matching the signal paths of

the 1st stage MDAC and sub-ADC in layout also reduces the effects of phase errors.

However 1st stage comparator decision errors from clock skew between the MDAC and

sub-ADC are more difficult to reduce. This is because V_T mismatch in the sampling

switches, coupled with slow clock edges, cause variations in the track-to-hold instants

between the sub-ADC and MDAC. These variations result in voltage differences in their

sampled input signals and consume a portion of the available 2nd stage correction range.

These effects are further exacerbated with high frequency input signals.

Figure 3-10 shows a plot of ADC ENOB versus clock skew for an otherwise ideal

9bit two-stage pipeline ADC with a 4bit 1st stage and 6 bit 2nd stage with 1bit over-range.

The data is for a 502MHz input signal sampled at 1GHz. For an ENOB greater than 8.5,

the data shows that the clock skew must be kept below ±24ps. However, the pipeline

ADC model assumes no offsets in the 1st stage sub-ADC and therefore the entire 2nd stage

correction range is available for mitigating clock skew. With 1bit 2nd stage over-range,

the available correction range referred to the input is ±25mV. To prevent missing codes

in the ADC, the contributions from both 1st stage comparator offsets and clock skew

should not exceed 25mV (i.e. |1st Stage Offsets + Sampling Mismatch| < 25mV) [42].
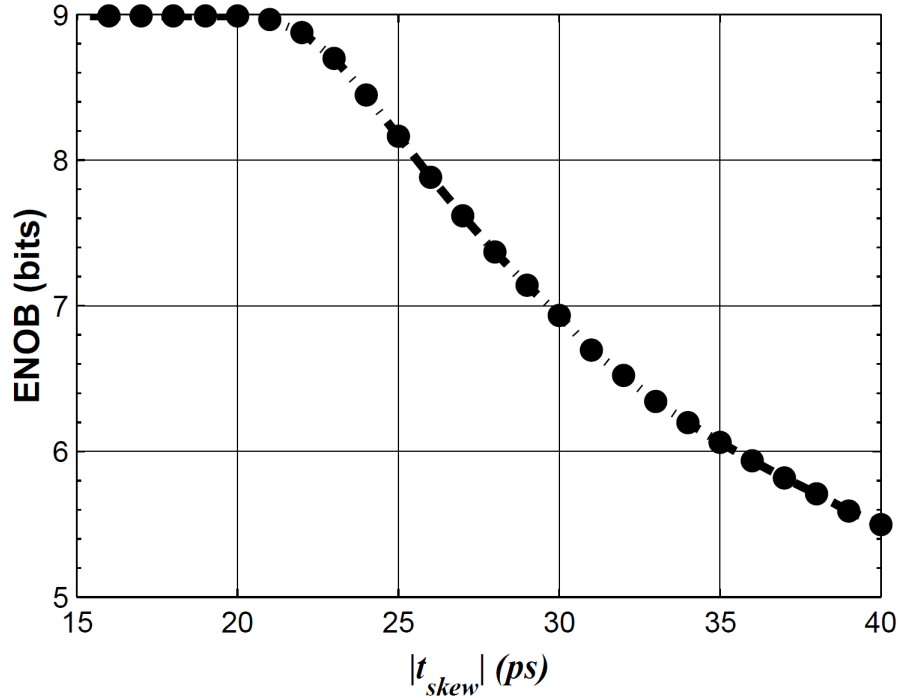
Figure 3-10 ADC ENOB versus clock skew for an otherwise ideal 9bit two-stage SAH-less pipeline ADC with a 4bit 1st stage and 6bit 2nd stage with 1bit over-range. The data is with respect to a 502MHz input signal sampled at 1GHz.

Figure 3-11 shows a plot of ADC Yield versus clock skew for the same two-stage architecture as in Figure 3-10 but incorporating comparator redundancy in the sub-ADCs. In this model, the 2nd stage 6bit sub-ADC is modeled as a redundancy-based flash ADC with a redundancy of four and a random comparator offset of 15 ADC-LSBs. The 1st stage 4bit sub-ADC is modeled as a redundancy-based flash ADC with a redundancy of two. Furthermore, to observe the effects of varying degrees of random 1st stage comparator offset, the 4bit sub-ADC is modeled with random offsets of 6, 8 and 10 ADC-LSBs and shown as three different curves in Figure 3-11. Each point in Figure 3-11 represents the percentage of 100 randomly generated ADCs with ENOB greater than 8.5 for a given clock skew (in absolute value) and 1st stage comparator offset (in ADC-

LSBs). For 90% yield, the data shows that clock skew must be kept below ±6ps, ±9ps and ±15ps for a 1st stage comparator offset of 10, 8 and 6 ADC-LSBs (32 ADC-LSBs = 1 LSB) respectively. In this design, the random 1st stage comparator offset is 8 ADC-LSBs and dictates that clock skew must be kept within an 18ps window for 90% yield.
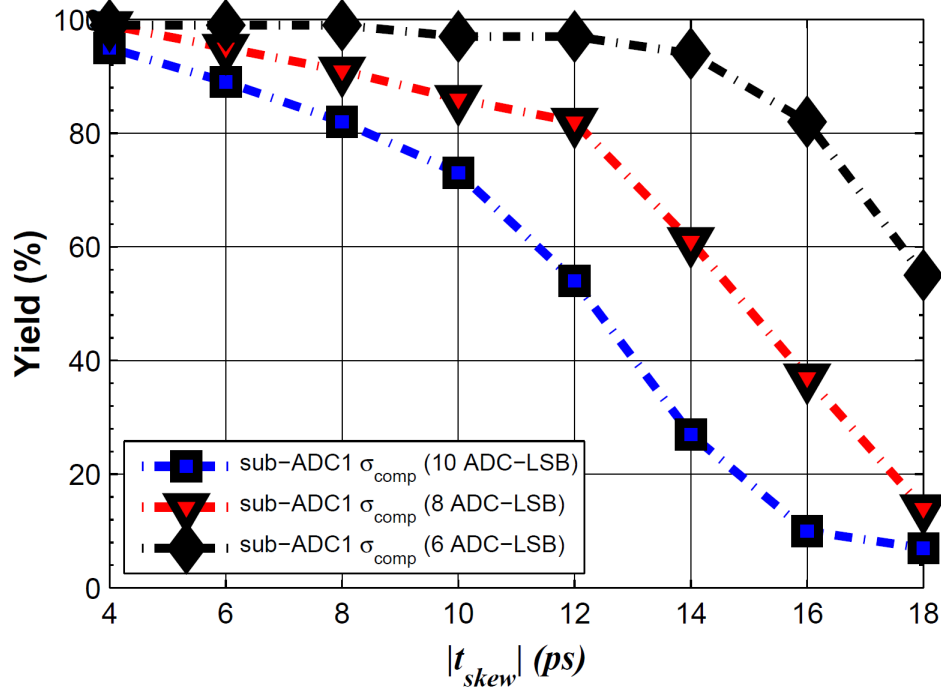
Figure 3-11 Monte Carlo simulation of Yield versus clock skew for the same ADC architecture as in Figure 3-10 but incorporating comparator redundancy in the sub-ADCs. The 1st stage 4bit sub-ADC and the 2nd stage 6bit sub-ADC incorporates a redundancy of two and four respectively. Yield is defined as the percentage of 100 randomly generated ADCs whose ENOB is greater than 8.5.

This is achieved with simple digital trimming of a delay chain in the sampling paths and allows the elimination of a dedicated front-end sample and hold circuit. The delay consists of programmable inverter delay chains (Figure 3-12) that are implemented with floating body devices and inserted in the clock paths of the MDAC and its sub-ADC.

Delay increments of 6.5ps provide sufficient granularity within an 18ps window to correct for sampling skew and prevent ADC performance degradation at high input frequencies.
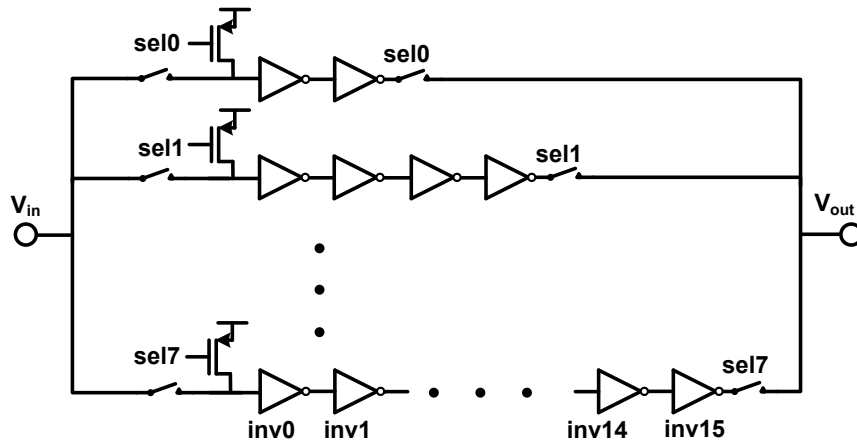
Figure 3-12 Tunable Delay Circuit used for 1st stage Clock Skew Correction.

3.3.5 Calibration

At power-on, an off-chip calibration engine initiates a search algorithm to select comparators closest to the desired trip points for both 1st and 2nd stage sub-ADCs. For each sub-ADC code, the algorithm sequentially enables trial comparators and instructs an off-chip digital-to-analog converter (DAC) to apply input voltages about a desired sub-ADC trip voltage. When a comparator with an actual trip-point near the ideal trip-point is located, the algorithm assigns the comparator to the sub-ADC code and proceeds to the next code. The process continues until a comparator for each sub-ADC code is found. Each sub-ADC comparator can be enabled or disabled independently and a memory element associated with each comparator stores the comparator on/off states. The

memory elements are connected serially forming a memory block that is accessible through an SPI interface.

Tying the MDAC reference switches to $V_{REF}/2$ instead of V_{REF} and ground, as shown in Figure 3-5, yields a residue that is independent of the 1st stage sub-ADC decision. This allows the 2nd stage sub-ADC comparator bank to be calibrated through the ADC input as shown in Figure 3-13. In this configuration, the MDAC operates as a conventional switched-capacitor amplifier with a gain of C_s/C_f.
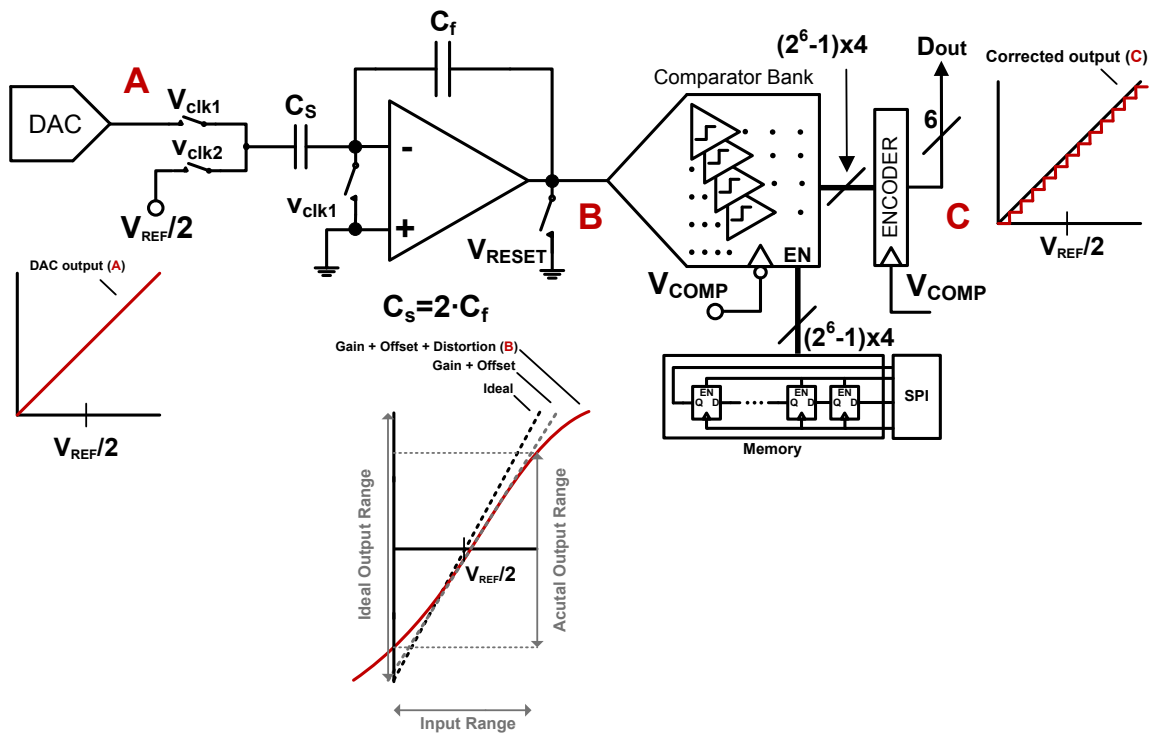
Figure 3-13 Calibration scheme for 2nd stage redundancy-based flash sub-ADC to account for op-amp non-linearity, finite gain and offset.

This is beneficial because it allows calibration of two op-amp non-idealities that degrade ADC performance. First, any non-linearity in the op-amp causes the switched-capacitor amplifier to present a distorted output voltage to the comparator bank. Second, any gain error and offset due to finite op-amp gain and offset causes the switched-capacitor amplifier to present an output voltage to the comparator bank that is offset from its zero input value and with an error term [43] that causes the gain to deviate from the ideal switched-capacitor amplifier gain. Since the calibration algorithm instructs the DAC to sweep an input voltage about a desired sub-ADC trip-voltage based on a closed-loop gain of two (A in Figure 3-13), but instead a comparator with a trip-voltage nearest a distorted output voltage is selected (B in Figure 3-13), any ADC non-linearity attributed to op-amp distortion, finite gain and offset is corrected (C in Figure 3-13). Furthermore, because the 2nd stage sub-ADC is calibrated at the 1GHz sample rate and the switched-capacitor amplifier output is reset after every sample, errors due to incomplete settling are also corrected during calibration.

Figure 3-14 shows three plots relating to a Matlab-simulated 1GS/s 9bit two-stage pipeline ADC with a 4bit 1st stage and 6bit 2nd stage with 1bit over-range. The 1st stage 4bit sub-ADC is modeled as a redundancy-based flash ADC with a redundancy of two and a random comparator offset of 8 ADC-LSBs. The 2nd stage 6bit sub-ADC is modeled as a redundancy-based flash ADC with a redundancy of four and a random comparator offset of 15 ADC-LSBs. The 1st stage 4b MDAC model employs a high feedback factor of 1/3 and incorporates 2 ADC-LSBs of gain error, 2 ADC-LSBs of settling error, 1 ADC-LSB of input referred offset and a THD of -35.25dB. Figure 10 (a) shows the transfer function of the non-ideal 4bit MDAC. Figure 10 (b) and (c) each show a spectral

analysis of the 9bit two-stage pipeline ADC incorporating the non-ideal MDAC in the Matlab model. However, in Figure 10 (b) the non-ideal MDAC is excluded in the calibration path of the 2nd stage sub-ADC and in Figure 10 (c) the non-ideal MDAC is included in the calibration path and yields an 8.8dB improvement in SNDR. The simplicity of this calibration approach not only corrects DNL errors, but also eliminates the need for complex calibration algorithms to correct for ADC errors from finite op-amp gain and offset.
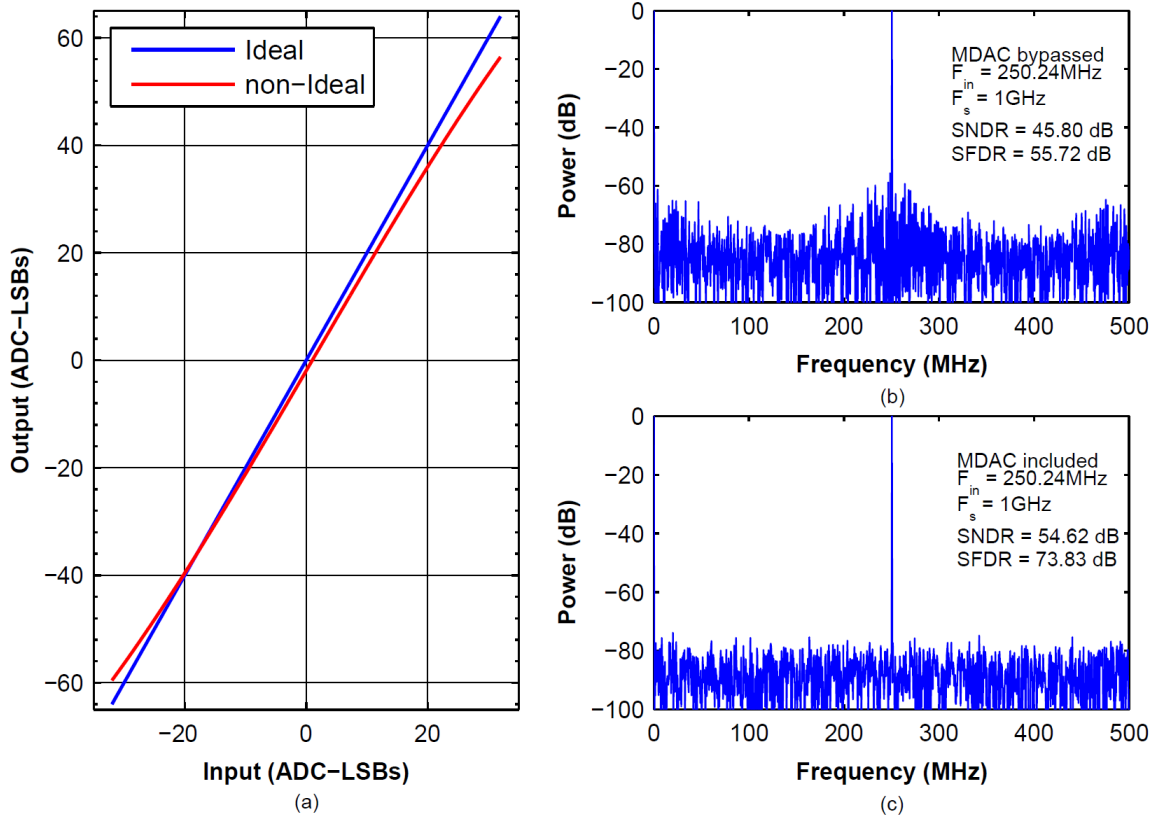
Figure 3-14 (a) Transfer function of an ideal and non-ideal 4b MDAC with nominal gain of 2. (b), (c) Spectral analysis of a Matlab-simulated 9bit two-stage pipeline ADC with (b) and without (c) the non-Ideal MDAC in the calibration path of the 2nd stage 6bit redundancy based flash sub-ADC.

3.3.6 Encoder

The outputs of the 1st and 2nd stage sub-ADCs are routed to dedicated encoding blocks and summed to form a 4-bit and 6-bit word respectively. Summation of logic ones at the encoder inputs guarantees monotonicity and permits comparators to seamlessly be re-assigned to any code. The encoder uses a Wallace tree architecture, in combination with carry-select adders and pipelining, to resolve the comparator outputs at 1GS/s. This encoding scheme is inherently independent of comparator assignment since it adds the number of logic highs present at its input. Digital correction is done off-chip. Figure 3-15 shows the block diagram of the 2nd stage encoding scheme.

From Comparator Bank

4 X Clk_EN[71:0]

4 x 72 Flops

4 x 2 x 5b Wallace   4 x 4b Wallace tree

4 x 11 x 1 Flops   4 x 4 Flops

4 x 1 x 5b Ripple

4 x 5 Flops   4 x 4 Flops

4 x 5b Ripple

4 x 5 Flops

2 X 5b Ripple

6b Ripple Carry Select

6 Flops

To Decimator
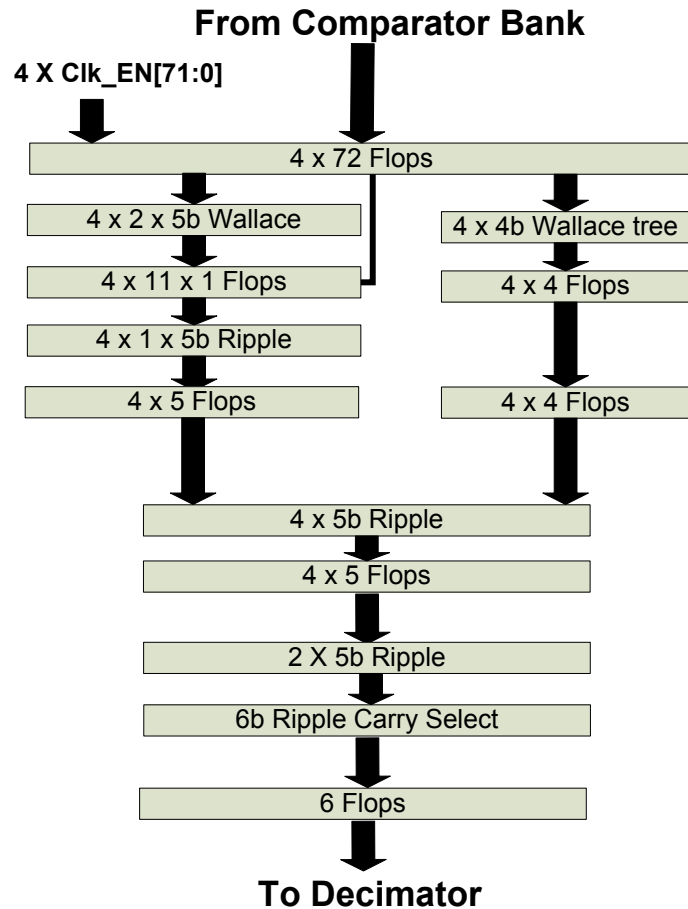
Figure 3-15 2nd stage sub-ADC Encoder block diagram.

3.4   Circuit Details

3.4.1   1st Stage Op-Amp
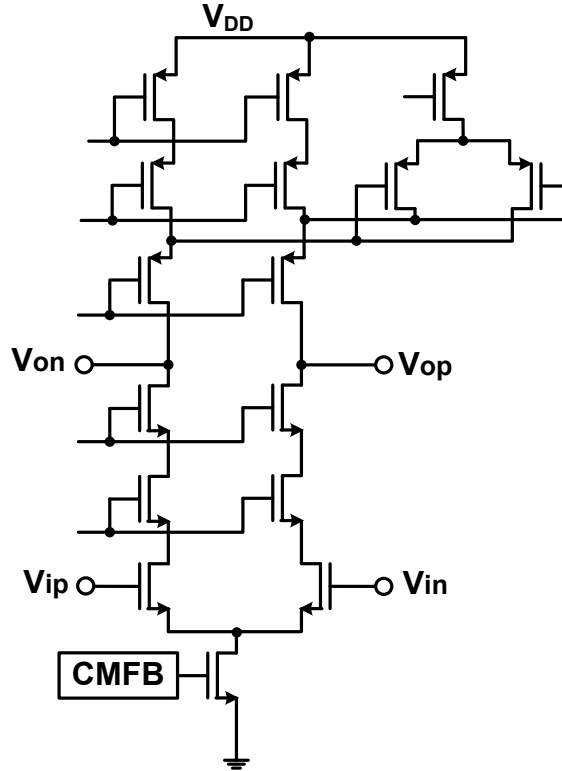
Figure 3-16 1st stage MDAC op-amp with gain enhancement.

A low feedback factor of 1/3 and 1bit 2nd stage over-ranging yields an MDAC output swing requirement of only 200mVpp. This enables the op-amp to be implemented as an NMOS-input, triple-cascode amplifier as shown in Figure 3-16. The circuit leverages body-contacted, 56nm channel length FETs for all devices in order to avoid memory effects associated with floating-body transistors. The tail transistor is biased in triode with a 40mV V_{DS} while all other FETS are biased in saturation with a constant 160mV V_{DS}. An 85mV V_{DSAT} ensures sufficient headroom to support a maximum single-ended output swing of 150mV with a 1V supply. Simulations show a minimum gain of 42dB

and a tunable negative resistance increases the overall output resistance enabling a maximum gain of 63dB. Furthermore, the reduced MDAC gain in this ADC and corresponding increase in feedback factor to 1/3 means that an open-loop unity gain frequency of 7.5GHz is sufficient for 1GS/s operation. The op-amp employs switched capacitor common-mode feedback (CMFB) and the feedback correction is applied to the tail transistor.

3.4.2   Sub-ADC Comparators

The 1st stage sub-ADC comparators, which achieve a 75ps decision time, are based on [46] but adapted to use floating-body FETs which have a speed, power and area advantage over body-contacted devices. SOI memory effects are eliminated by resetting the comparator inputs to a common mode voltage and resetting all internal nodes to either the supply or ground prior to the comparison phase. Furthermore, a comparator random offset of 8 ADC-LSBs and a comparator redundancy of two guarantees with 90% probability that 1st stage sub-ADC decision errors and a 1st stage clock skew of up to ±8.5ps does not degrade ADC SNDR by more than 3dB (Figure 3-11).

The 2nd stage sub-ADC noise requirement is relaxed by the 1st stage MDAC gain of two and enables sub-micron device widths, beneficial for power and speed, to be employed in the comparator design. The comparator, also based on [46], consists of floating-body FETs and exhibits large offset suited for redundancy and reassignment. SOI memory effects are eliminated by resetting the comparator inputs to a common mode voltage via V_{RESET} in Figure 3-8 and resetting all internal nodes to either the supply or ground prior to the comparison phase. Deliberate offsets are introduced by asymmetric loading of the drain nodes of the differential pair with a floating body MOS capacitor as

shown in Figure 3-17. This method, unlike asymmetric sizing of the input pair [32], does not tradeoff comparator input capacitance for deliberate offset and results in a comparator input capacitance less than 1fF (extracted).
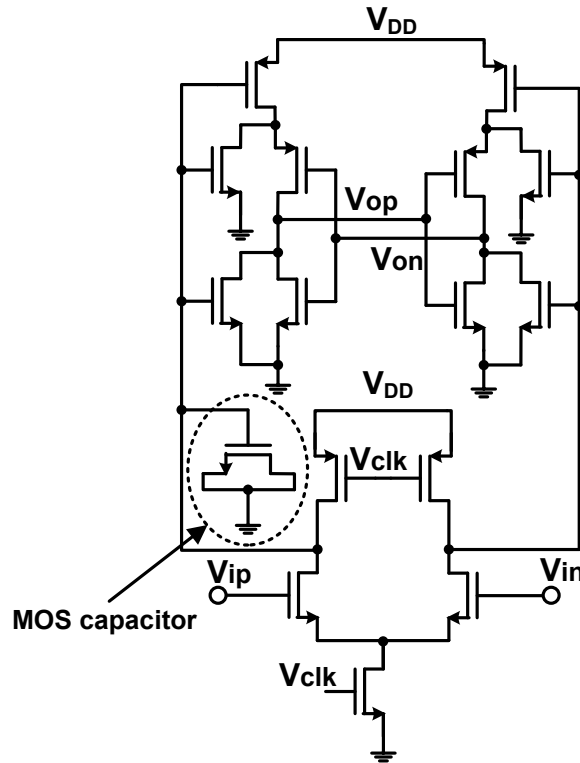
Figure 3-17 2nd stage sub-ADC comparator with MOS-capacitor for deliberate offset.

Spectre transient noise simulations show that thermal noise from the input pair is the most dominant and its input-referred noise equivalent is given by [47],

$$\overline{\delta V_{in}^2} = \frac{4kT\gamma V_{dsat}}{C_L V_{DD}} \qquad 3.12$$

where γ is the MOS noise factor, V_{DD} is the supply voltage, V_{dsat} is the overdrive voltage of the input pair and C_L is the load capacitance at their drain nodes. The V_{DD} term in

Equation 3.12 stems from delay $t_d = V_{DD}/(2I_D)$ which dictates the time one of the drain nodes in the source coupled pair discharges to $V_{DD}/2$ at which point the latch in Figure 3-17 begins to regenerate. Any circuit noise referred to the input during regeneration is negligible. Equation 3.12 shows that increasing the capacitance C_L or reducing V_{dsat} by increasing the input pair widths or decreasing the input common mode voltage reduces noise. In this design, a combination of the latter two approaches is leveraged and yields a simulated 0.4 ADC-LSBs of circuit noise (Figure 3-18a). Furthermore, Spectre Monte-Carlo simulations indicate s a 1σ comparator random offset of 17 ADC-LSBs (Figure 3-18b).
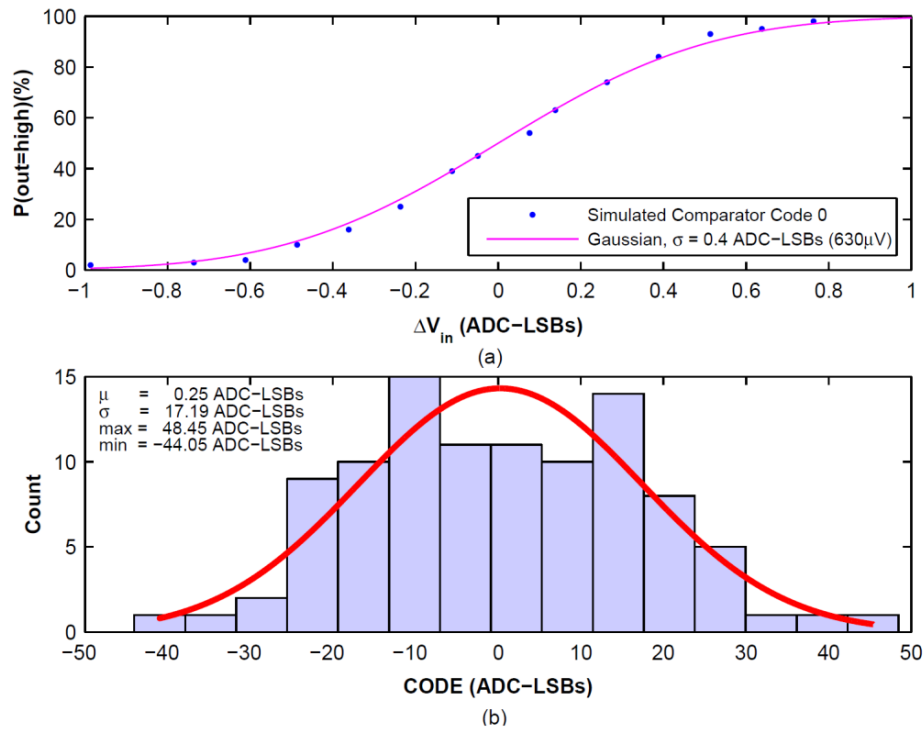
Figure 3-18 Simulation data on 2nd stage sub-ADC comparator (a) cumulative noise distribution and Gaussian fit and (b) random offset.

Figure 3-19 illustrates the deliberate and random offset scheme used for setting the 2nd stage sub-ADC input range. Twelve variants of a floating-body MOS capacitor enable a 2nd stage sub-ADC input range from -50mV to 150mV in 12.5mV increments which translates to one deliberate offset for every four codes. Furthermore, the 3σ comparator offset is 24LSBs where the LSB is the resolution of the 2nd stage sub-ADC. Exploiting an offset of this magnitude with a comparator redundancy of four-per-code provides sufficient granularity in between deliberate offsets to ensure an overall ADC ENOB greater than 8.5bits with 90% yield.
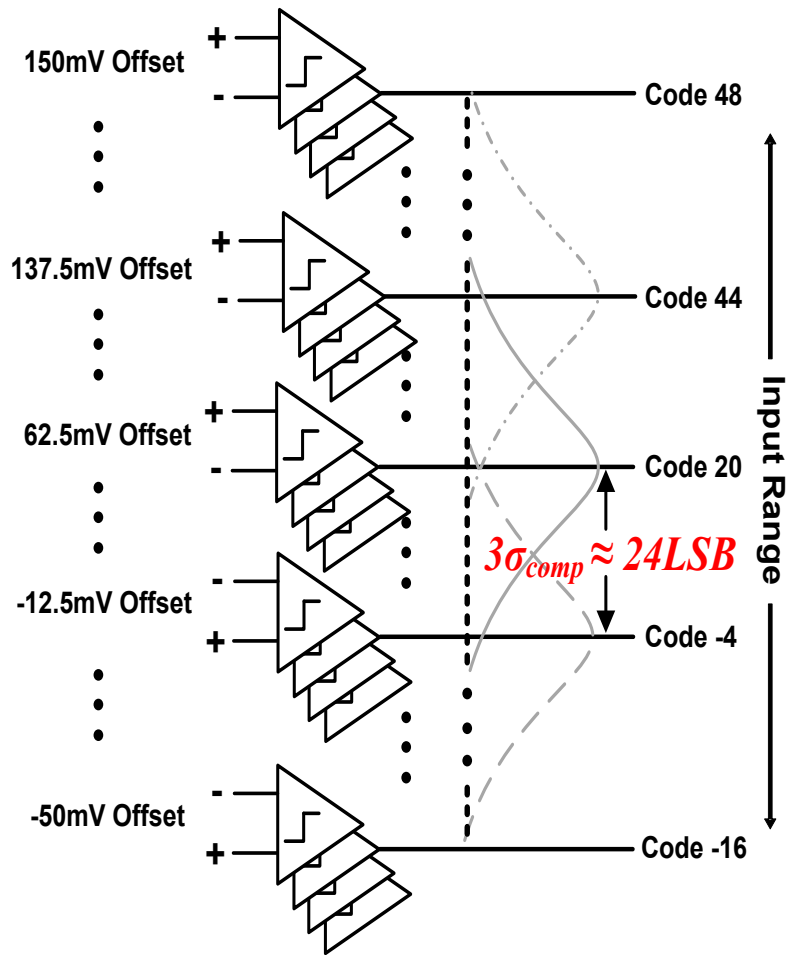
Figure 3-19 Deliberate and Random offset scheme for setting 2nd stage sub-ADC input range.

3.5 Measurement Results

The prototype, fabricated in a 45nm SOI-CMOS process, occupies a core area of 0.125mm^2. A die micrograph is shown in Figure 3-20. The prototype ADC has a differential input signal range of 800mVpp and input capacitance of 500fF.

Figure 3-21 shows experimental data for determining the 2nd stage comparator random offset. Each comparator's measured offset is subtracted from its simulated (extracted) offset so that all comparators in the comparator bank can be used in the sample set for calculating the standard deviation. Experimental measurements yield a 1σ random offset of 14.4 ADC-LSBs. Linearity plots (Figure 3-22) for the 2nd stage sub-ADC show a maximum DNL/INL of 0.75 and 1.07LSB. This translates to an ENOB of 5.6[19] for the sub-ADC and shows that a comparator redundancy of four-per-code is sufficient for limiting SNR degradation from non-uniform quantization noise to 2.4dB. The maximum measured ADC DNL/INL values are 0.75/1.17LSB (Figure 3-23).

Figure 3-24 shows the output spectrum for a 500.5MHz input signal sampled at 1GS/s, with and without clock skew correction. The output data is decimated by 16X for reliable transmission off-chip. Figure 3-25 shows measured data of 1st and 2nd stage sub-ADC output codes during conversion of a 750MHz input signal sampled at 1GHz. The dashed lines indicate the 2nd stage correction range and the top and bottom plots correspond to an ADC conversion without and with 1st stage clock skew correction respectively. The data shows that sampling mismatch between the 1st stage sub-ADC and MDAC cause the majority of the correction range to be consumed at high frequencies.

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[19] A Matlab model of a 6bit flash ADC incorporating the measured DNL data of Figure 16 yields an ENOB of 5.6.

However, the bottom plot in Figure 3-25 shows that digital trimming of the delay circuit (Figure 3-12) in each of the 1st stage clock paths mitigates clock skew and the remaining correction range that is consumed is due to the 1st stage comparator offsets. Figure 3-26 shows the measured SNDR and SFDR versus input frequency at 1GS/s with and without clock skew correction. A 3.5dB improvement in SNDR is observed for Nyquist-rate and 750MHz input signals.

The prototype ADC achieves an ENOB and SFDR of 7.8bits and 61.6dB, respectively, at low frequency and 7.4 bits and 52.7 dB at Nyquist. The ADC consumes a total of 27mW from a 1V/1V analog/digital supply and achieves an FOM of 160fJ/conversion-step. TABLE VI shows the performance summary of the prototype ADC.

TABLE VI ADC PERFORMANCE SUMMARY

Technology	45nm SOI-CMOS
Supply	1.0V
Resolution	9bit
Input Range (Differential)	800mV$_{PP}$
Sampling Rate	1GS/s
Power Consumption	27mW
DNL/INL	0.75/1.17LSB
SFDR @ Nyquist	52.7dB
SNDR @ Nyquist	46.3dB
ENOB @ Nyquist	7.4
FOM	160fJ/Conv-step
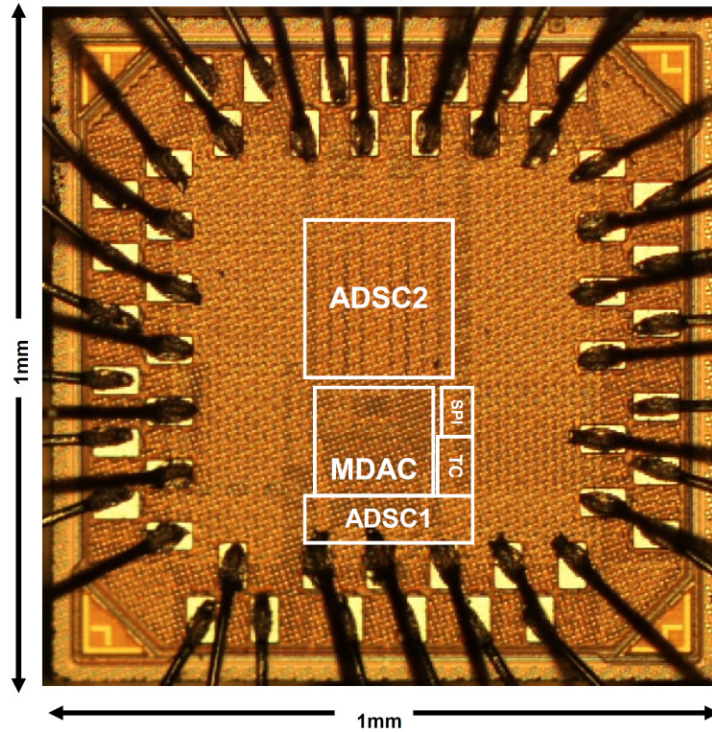
Figure 3-20 45nm CMOS-SOI prototype ADC die microphotograph.
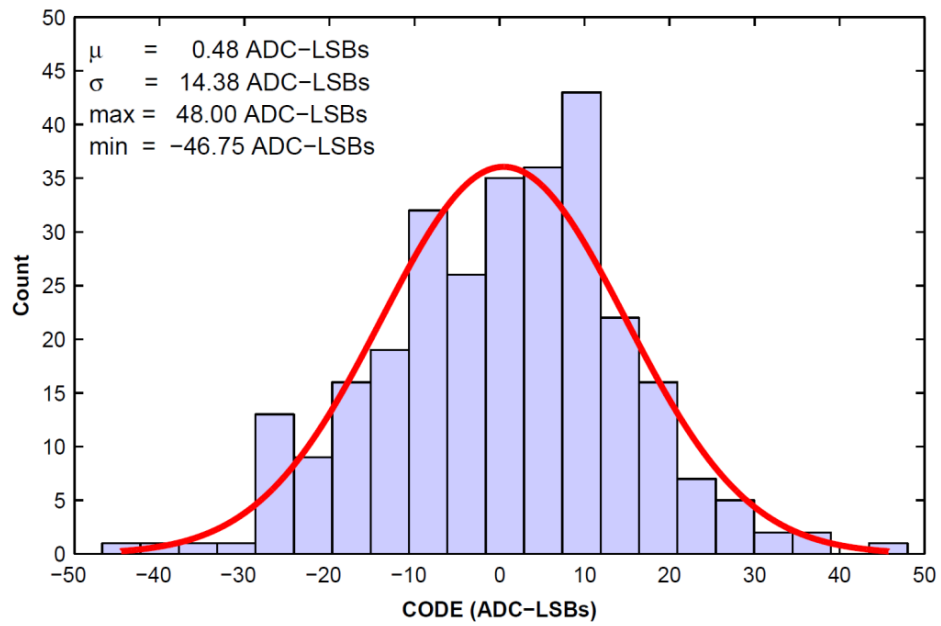
Figure 3-21 Measurement data of 2nd stage sub-ADC comparator random offset.
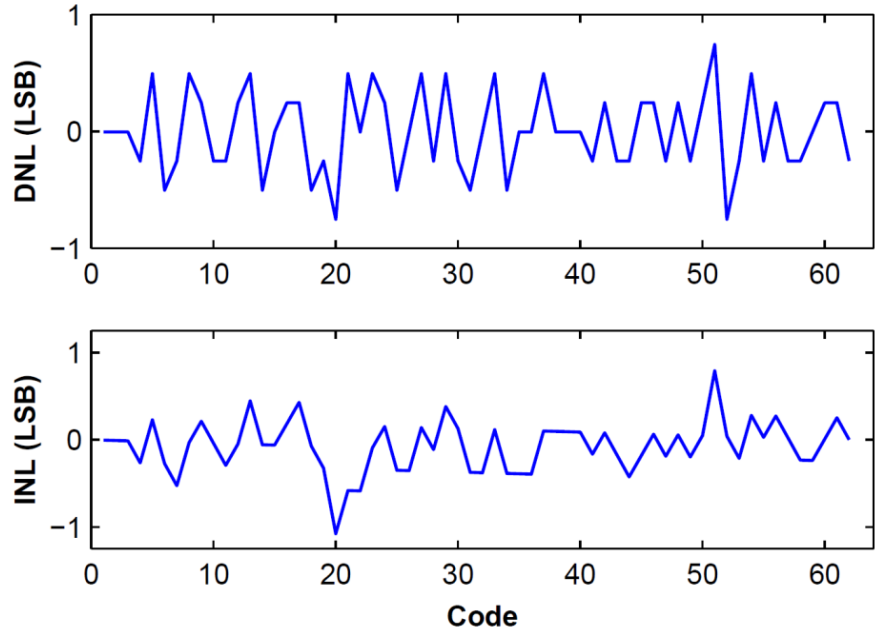
Figure 3-22 Measured 2nd stage sub-ADC DNL and INL.
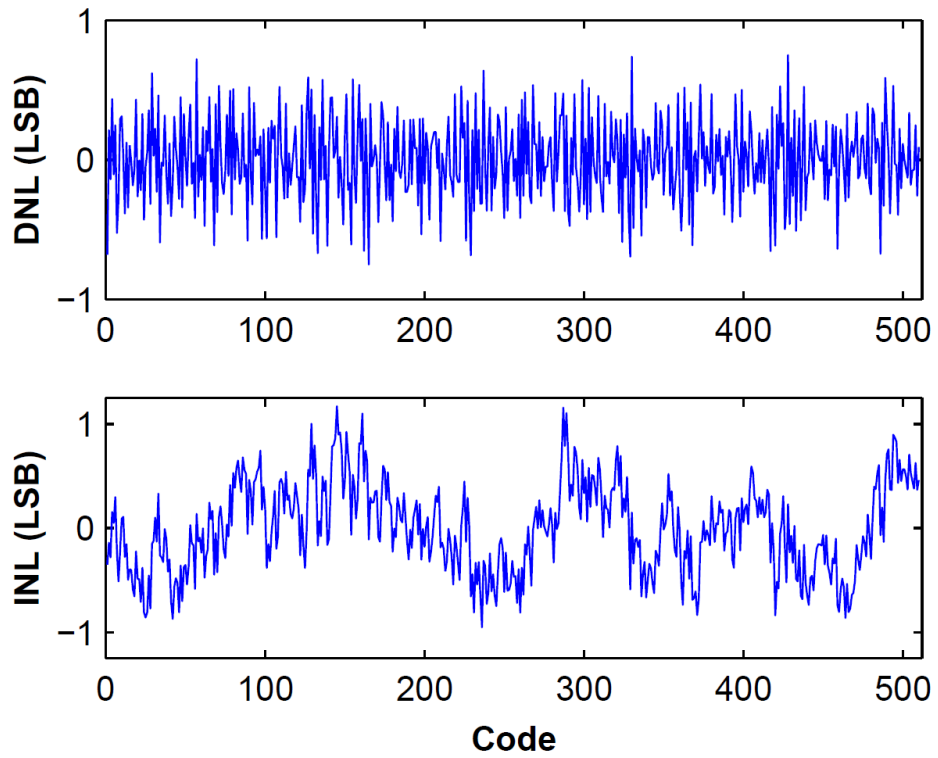
Figure 3-23 Measured ADC DNL and INL.
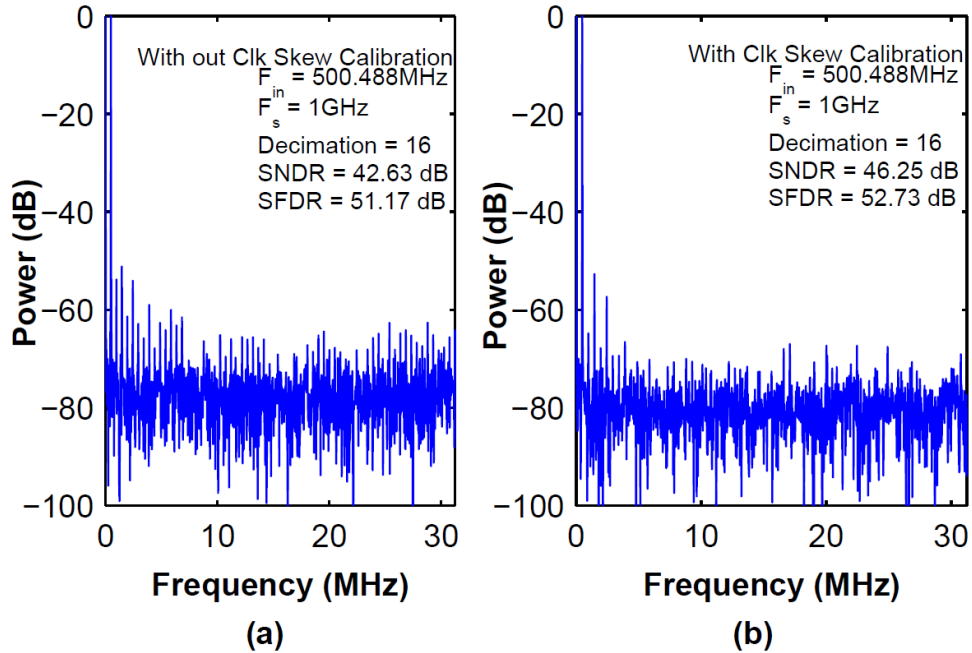
Figure 3-24 Output spectrums for a 500.49MHz input and 16X decimation without and with (b) clock skew correction.
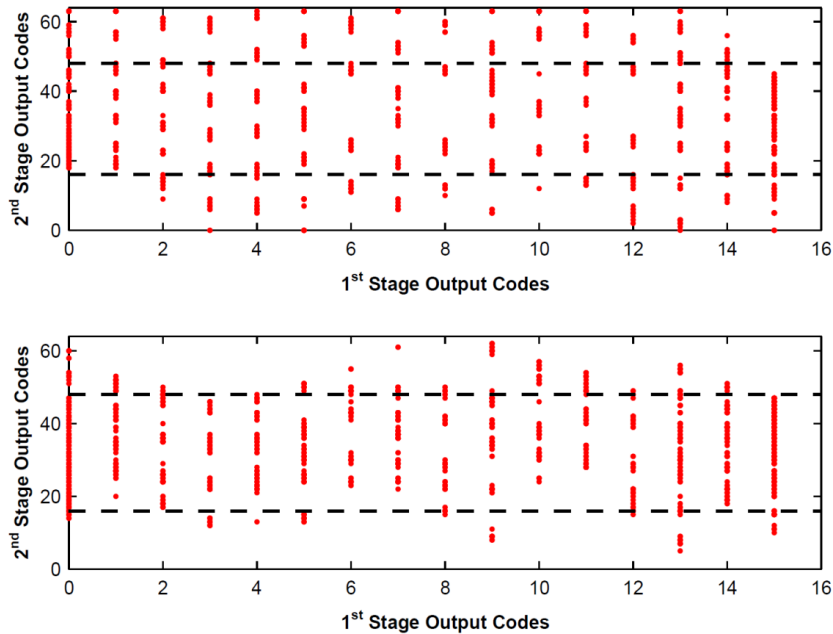
Figure 3-25 Measured data of 1st and 2nd stage sub-ADC output codes during conversion of a 750MHz input signal sampled at 1GHz without (top) and with (bottom) 1st stage clock skew correction. The dashed lines indicate the 2nd stage correction range.
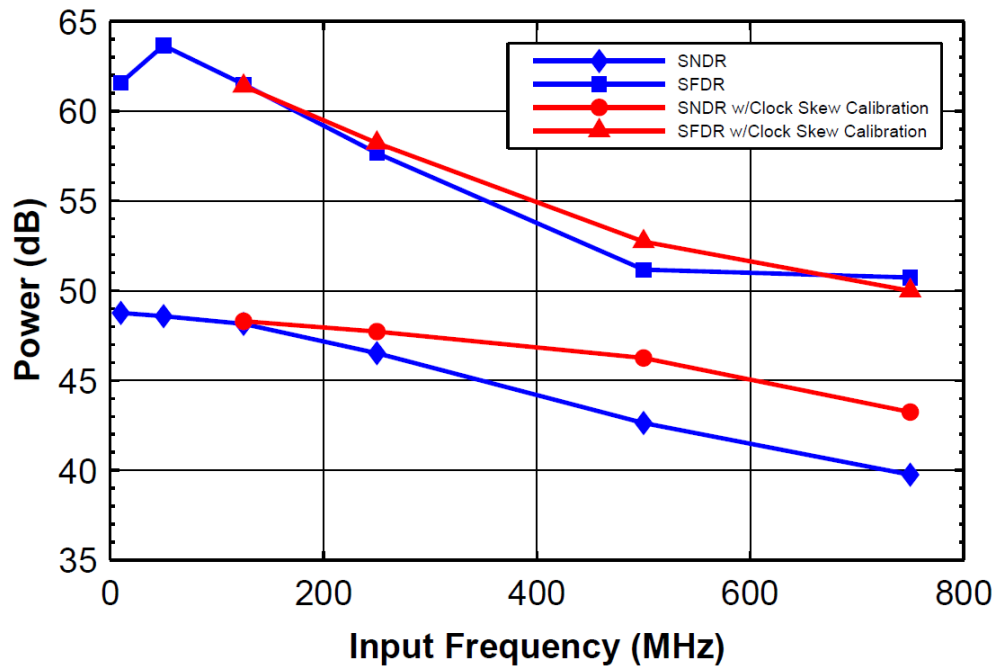
Figure 3-26 Measured SNDR & SFDR vs. Fin (Fs = 1.0GS/s) with and without clock skew correction.

CHAPTER 4 A Technique for sub-ADC Sharing in Time-Interleaved ADCs

4.1   Introduction

This chapter introduces a new 2-times interleaved ADC architecture that leverages the two-stage pipeline ADC in [33] and also incorporates a combination of op-amp and sub-ADC sharing to double the bandwidth and at the same time reduce power and area. In this design, the 2nd stage sub-ADC is shared between two time-interleaved 1st stage MDACs and effectively decouples 2nd stage speed from 1st stage accuracy requirements. This enables a 2nd stage redundancy-based flash sub-ADC to utilize the speed of the 45nm process and at the same time reduce active area. Furthermore, op-amp sharing between the two time-interleaved MDACs is employed for power and area reduction. A simple clock-skew correction circuit reduces timing mismatch between the two channels. The 9bit, 2GS/s 45nm SOI-CMOS prototype achieves a peak ENOB of 7.6b, no missing codes at 9b resolution and consumes only 45mW at 2GS/s from a 1V supply. This 2X-interleaved 9bit ADC occupies only 0.215mm^2 and achieves a figure of merit (FOM) of 167fJ/conversion-step at Nyquist.

Since the proposed architecture leverages directly from [33], only aspects unique to the proposed 2X-interleaved design are described here. The paper is organized as follows. Section 4.2 describes the new ADC architecture in detail and discusses its advantages over conventional approaches. Section 4.3 presents the measured results of the prototype ADC.

4.2   Proposed ADC Architecture
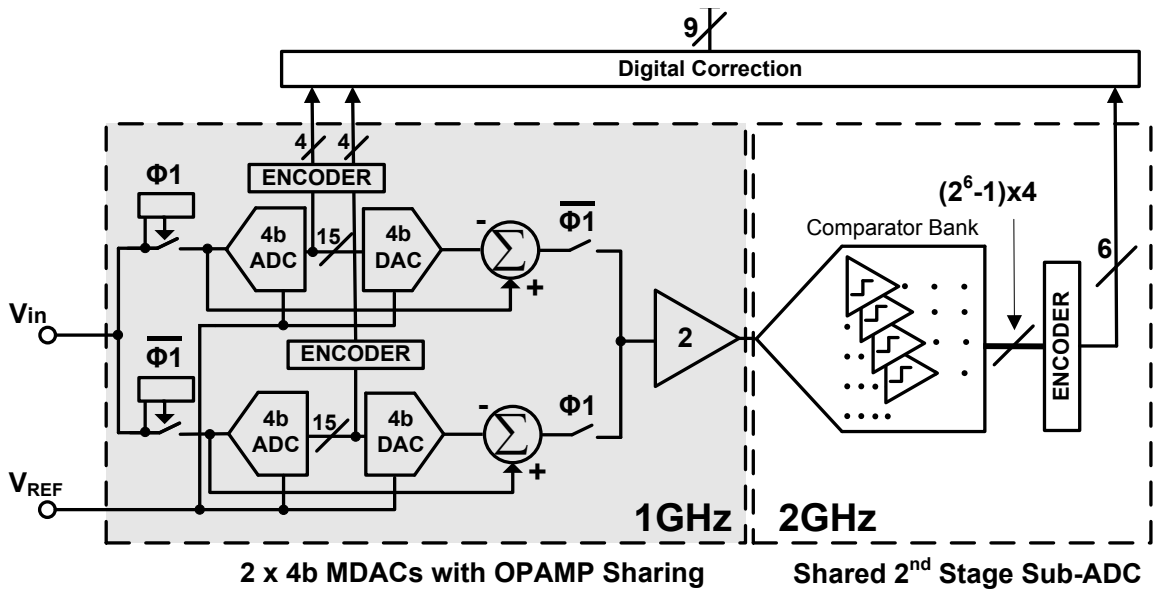
Figure 4-1 Simplified single-ended representation of proposed ADC architecture.

Figure 4-1 shows a block diagram of the proposed 2X interleaved architecture. Two interleaved track-and-hold circuits sample a differential input signal (single-ended shown) at opposite phases of a 1GHz clock. The sampled signals are subsequently processed by two 4b MDACs that incorporate op-amp sharing for power efficiency and area reduction. The residues are then digitized in alternating order by a single 2nd stage 6b flash ADC sub-converter operating at twice the frequency of the two interleaved MDACs. The time-interleaved 4b MDACs leverage a high feedback factor of 1/3 to relax the op-amp gain and bandwidth requirements by 5.7X and also enable a single-stage op-amp design. The shared 2nd stage 6b flash sub-ADC employs comparator redundancy and re-assignment and deliberate and random mismatch set the desired trip-points. These techniques enable a low 2nd stage FOM of 205fJ/conversion-step. A 1b over-range in the

2nd stage compensates for 1st stage comparator offsets. A simple clock skew correction block reduces timing mismatch between the two time-interleaved 4b MDACs and eliminates the need for a power-hungry conventional front-end sample and hold (SAH). This section analyzes the individual sub-blocks and their advantages in detail.

4.2.1 2X-Interleaved 1st stage 4b MDACs
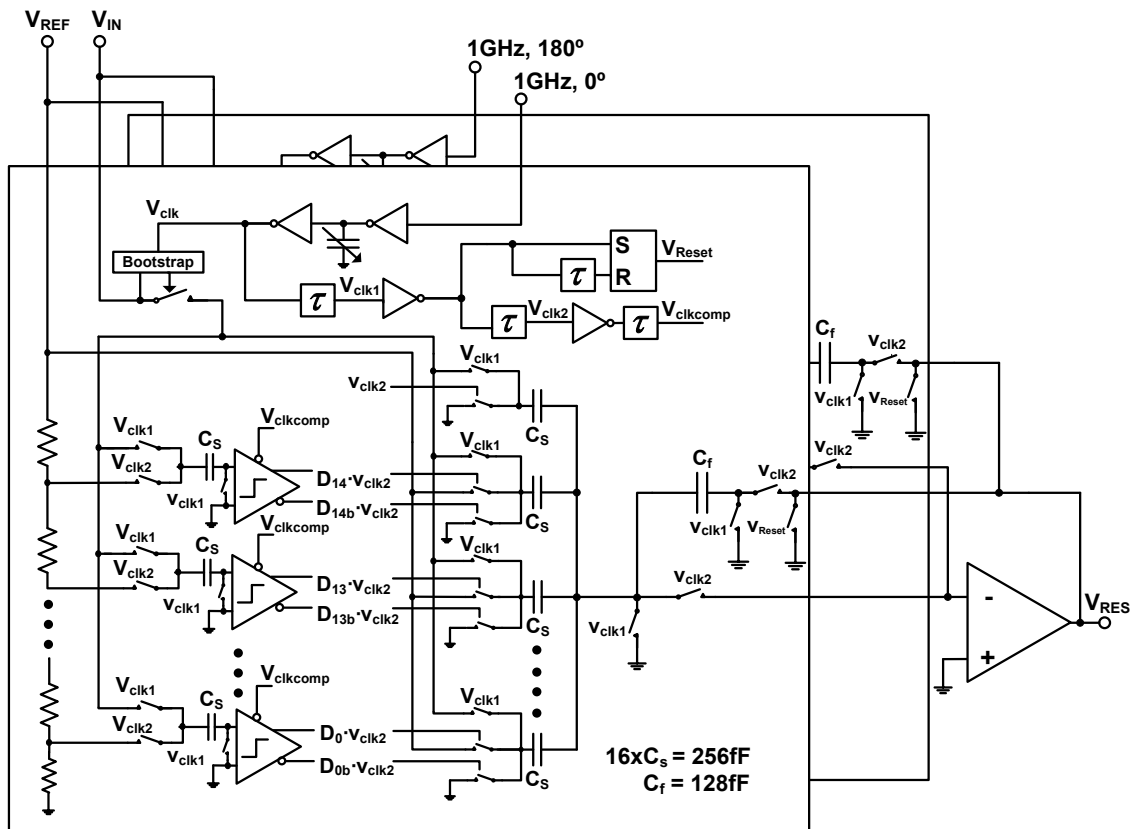
Figure 4-2. Simplified single-ended representation of two time interleaved 4-bit MDACs with op-amp sharing.

Figure 4-2 shows a simplified schematic of two time-interleaved 1st stage MDACs and their sub-ADCs. Each channel is similar to the architecture in [33] which is presented

in chapter 3. Similar to [33], an array of thermometer-encoded unit capacitor C_S serve as the input sampling capacitor array for the 4b MDAC. A second array of capacitors C_S serves as the input sampling capacitors for the comparators that make up the 4b flash sub-ADC. A resistor reference ladder sets the 1st stage comparator thresholds. The front-end switch in each channel is bootstrapped for improved linearity and mitigates the series switch resistances between the ADC input and sampling capacitors. For power efficiency and area reduction, the 2X-interleaved architecture employs an op-amp sharing technique between MDACs and each channel is clocked at opposite phases of a 1GHz clock. The timing waveforms for a single channel are shown in Figure 4-3.
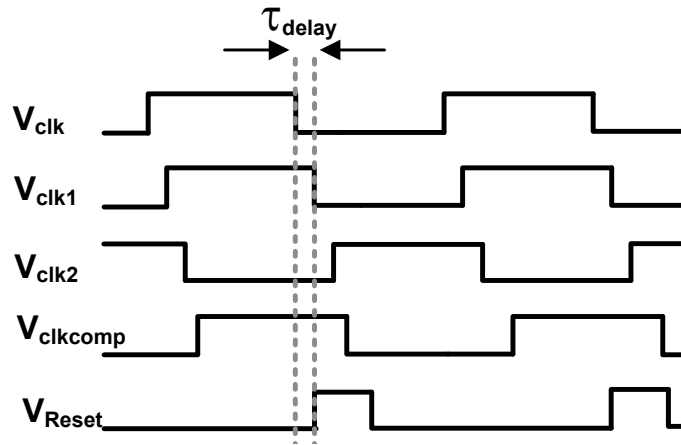
Figure 4-3 Timing waveforms for one of two time-interleaved 1st stage 4-bit MDACs in Figure 4-2.

When V_{clk1} is high, the sampling capacitors C_S in both the sub-ADC and MDAC track the input via their respective input sampling switches. The track-to-hold instant occurs at the falling edge of V_{clk1}. A delay (τ_{delay} delay in Figure 4-3) between the falling edges of

V_{clk} and V_{clk1} ensures that the MDAC and its sub-ADC sample a near-DC signal. This reduces the jitter requirements of the 1st stage sampling clocks and mitigates the effects of clock skew between the 1st stage MDAC and its sub-ADC.

The rising edge of V_{clk2} couples the flash sub-ADC reference voltages onto each of the comparator's sampling capacitors. The difference between the comparator reference voltages and sampled input signal are then coupled to the sub-ADC comparator inputs. A short delay between the rising edge of V_{clk2} and the falling edge of V_{clk_comp} allows adequate settling of the resistor ladder prior to the sub-ADC comparison. The sub-ADC comparator outputs then drive the MDAC reference switches to produce the residue V_{RES} at the output.

The time prior to the sub-ADC decision is used to reset the MDAC output for a period determined by pulse V_{Reset} as shown in Figure 4-3 and offers the same advantages as in [33]: reduced SOI memory effect, mitigated slewing at the op-amp output and mitigates signal dependent settling errors. However, in this design V_{Reset} serves two additional purposes. First, it reduces crosses talk between the two interleaved MDACs. Second, since the op-amp is shared between two MDACs, the op-amp is continuously active and therefore cannot employ a switched-capacitor common-mode feedback (CMFB) during the MDAC track phases. However, by utilizing the 1st stage sub-ADC decision time that begins at the rising edge of V_{clk2}, a pulse defined by V_{Reset} is sufficient for driving the op-amp switch-capacitor CMFB circuit. This approach eliminates the need for continuous time CMFB which would be challenging to implement with conventional op-amp techniques in 45nm CMOS with only 1V supply voltage.

To correct for timing mismatch between channels, simple digital trimming of a pair of tunable delay circuits [22] in the sampling paths is implemented. 5b control and 200fs delay increments provide sufficient granularity within a 1.5ps window to limit SNR degradation to ~3dB for a 1GHz input signal. Furthermore a 180° phase shift between channels ensures that only a single channel loads the ADC input during tracking. Finally sharing the op-amp between two interleaved MDACs eliminates channel mismatch due to gain and offsets that arise when employing separate op-amps in each interleaved channel. Therefore complex calibration schemes to mitigate gain and offset mismatch between channels is not required.

4.2.2   Shared 2nd Stage sub-ADC

Figure 4-4 shows a simplified single-ended block diagram of the shared 2nd stage sub-ADC and its timing waveforms. The residues from the 2X-interleaved 1st stage MDACs are processed in alternating order at the falling edge of V_{COMP} as shown in Figure 4-4. Since the 2nd stage flash sub-ADC is no longer constrained by the settling time requirements of the 1st stage MDACs, it can operate at twice the speed (i.e. 2GHz) and offers a simple and area efficient alternative to time-interleaving two stand-alone pipeline ADCs. Furthermore, sharing the 2nd stage sub-ADC eliminates channel mismatch due to offsets that arise when employing separate 2nd stage sub-ADCs in each interleaved channel. Therefore complex offset calibration schemes to mitigate this effect are not required.
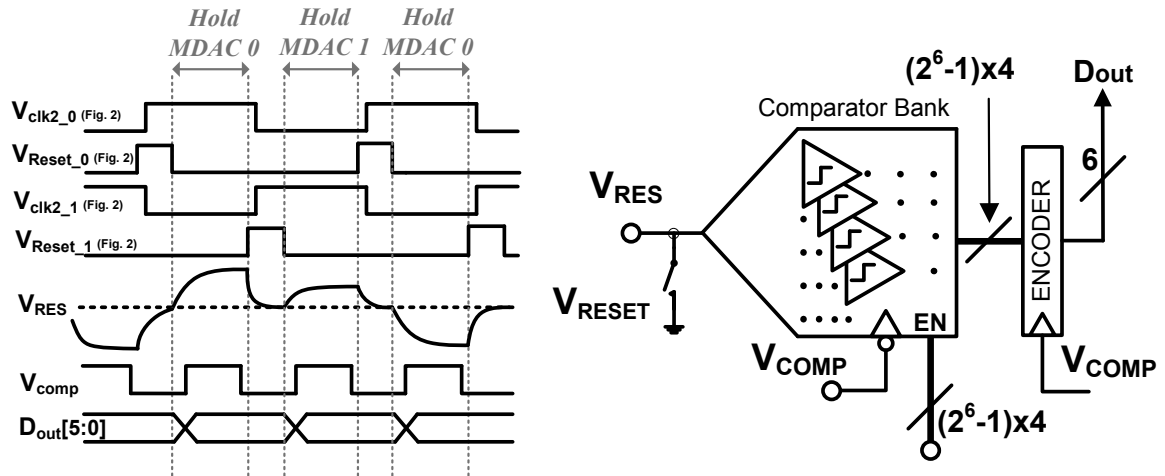
Figure 4-4 Simplified single-ended representation and timing waveforms for the shared 2nd stage 6b sub-ADC with redundancy of four comparators per code.

The sub-ADC incorporates redundancy and reassignment to correct DNL errors [17]. Furthermore, a combination of random and deliberate offset set the comparators trip-points and eliminates the need for a high-precision, low-impedance resistor reference ladder [32]. An encoder block, comprised of full adders, resolves the comparator outputs to the 6-bit sub-ADC output code. Finally, a startup calibration routine finds the comparators closest to the desired trip-points.

4.3 Measurement Results

The prototype, fabricated in a 45nm SOI-CMOS process, occupies a core area of 0.215mm^2. A die micrograph is shown in Figure 4-5. The prototype ADC has a differential input signal range of 900mVpp and input capacitance of 500fF.

The measured DNL and INL for each channel is within -0.85/+1.3LSB and -1.75/+1.58LSB respectively and is shown in Figure 4-6. Due to averaging, the overall DNL and INL improve to -0.69/+1.11 and -1.58/+1.37 respectively.

Figure 4-7 shows the output spectrum for a 1000.98MHz input signal sampled at 2GS/s. The output data is decimated by 9X for reliable transmission off-chip. Figure 4-8 shows the measured SNDR and SFDR versus input frequency at 2GS/s.

The prototype ADC achieves an ENOB and SFDR of 7.6 bits and 65.57dB, respectively, at low frequency and 7.07 bits and 56.04dB at Nyquist. The ADC consumes a total of 45mW from a 1V/1V analog/digital supply and achieves an FOM of 167fJ/conversion-step. Table VII shows the performance summary of the prototype ADC.

Table VII ADC PERFORMANCE SUMMARY

Technology	45nm SOI-CMOS
Supply	1.0V
Resolution	9bit
Input Range (Differential)	900mV$_{PP}$
Sampling Rate	2GS/s
Power Consumption	45mW
DNL/INL	1.11/-1.58LSB
SFDR @ Nyquist	56.0dB
SNDR @ Nyquist	44.3dB
ENOB @ Nyquist	7.07
FOM	167fJ/Conv-step
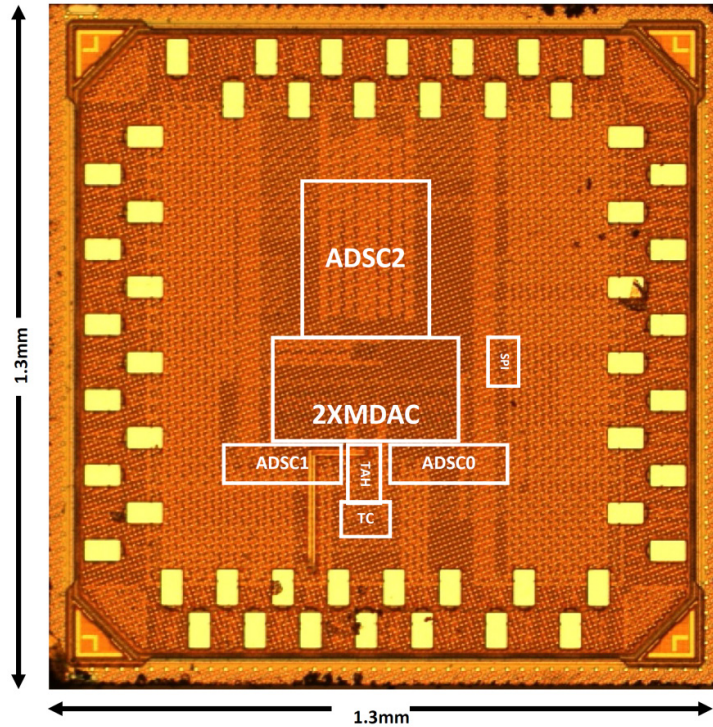
Figure 4-5 45nm CMOS-SOI prototype ADC die microphotograph.
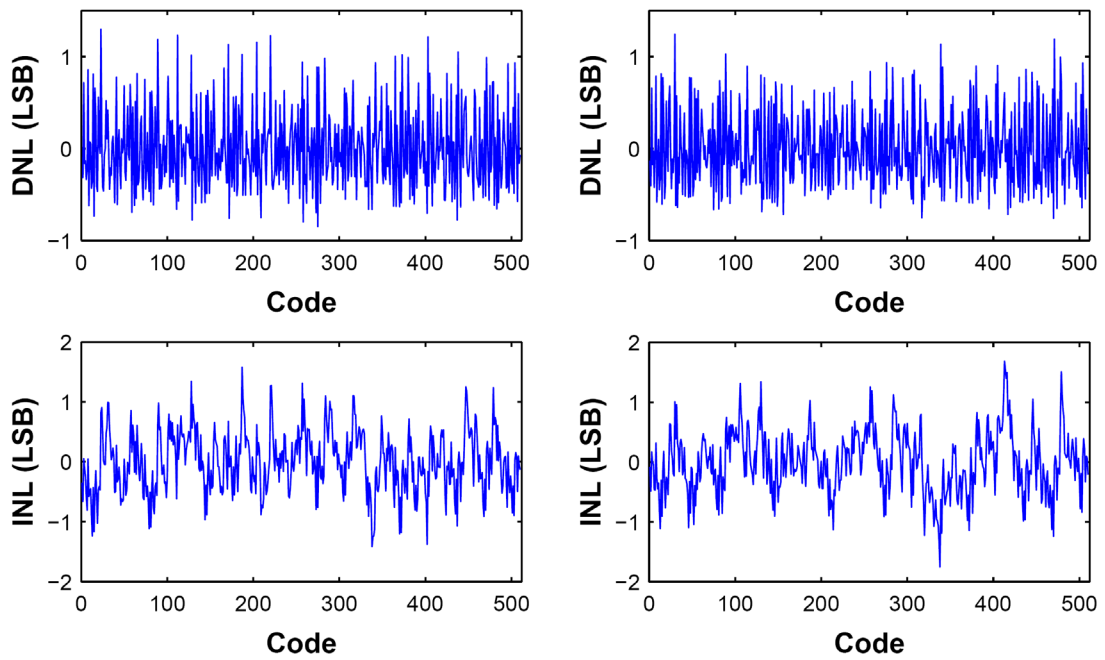
Figure 4-6 DNL (top) and INL (bottom) of channel 1 (right) and channel 2 (left).
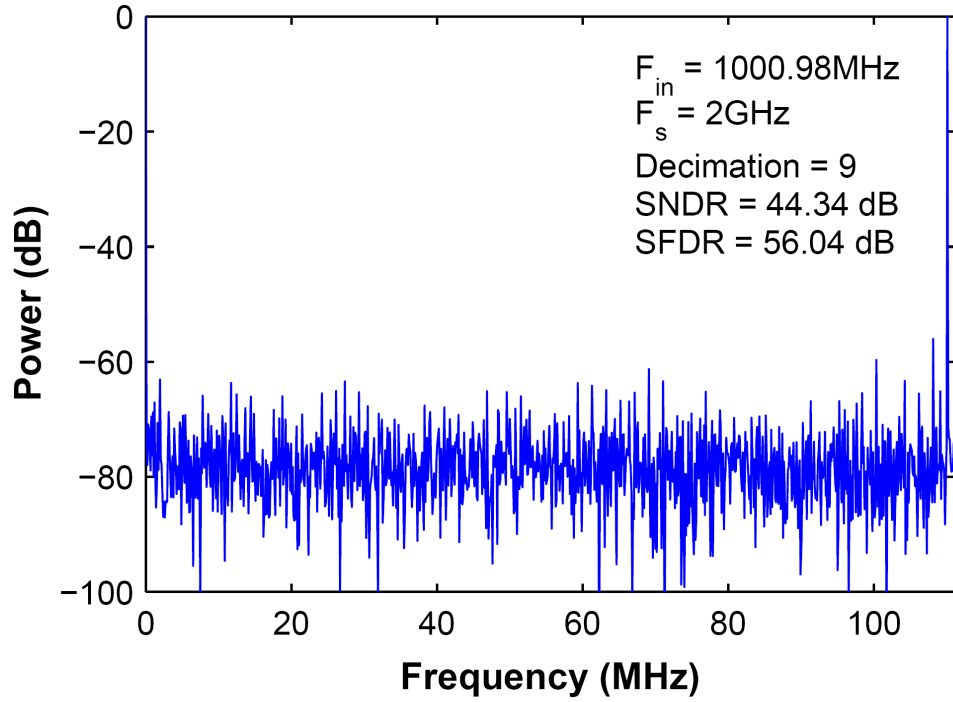
Figure 4-7 Output spectrums for a 1000.98MHz input and 9X decimation.
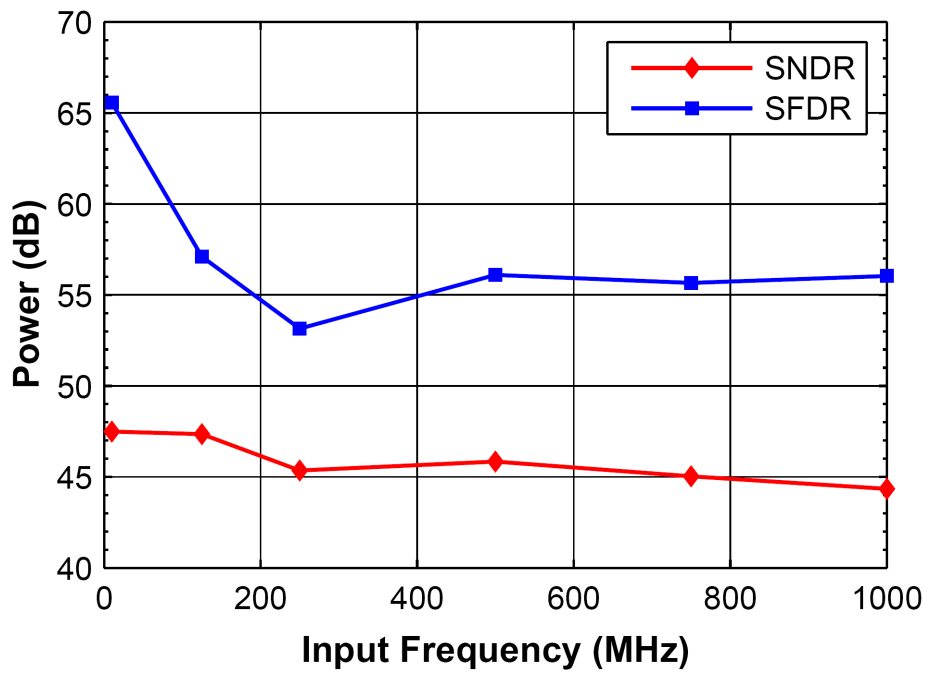
Figure 4-8 Measured SNDR & SFDR vs. Fin (Fs = 2.0GS/s).

CHAPTER 5 Conclusion

5.1   Summary

Significant improvements in area and energy efficiency are demonstrated with three generations of moderate resolution, GS/s+ prototype ADC chips. The first proof-of-concept chip showed that the speed and accuracy requirements of a high performance ADC can be decoupled, allowing the ADC to be small and fast, and enabling it to take advantage of state-of-the-art nanometer CMOS technology. This architecture is leveraged in a 2nd prototype chip which incorporates digitally-assisted analog techniques to benefit even more from advanced CMOS technology. Experimental results show greater than 10X improvement in energy efficiency and area compared to the best commercially available ADCs of similar performance. A 3rd prototype chip that incorporates time-interleaving for increased throughput achieves a 2X improvement in speed with similar energy efficiency.

5.2   Contributions

Chapter 2 presents a 7b 1.5GS/s flash ADC with comparator trip-points set purely by random and deliberate mismatch. The proposed technique eliminates the need for a low impedance, high precision resistor reference ladder. Furthermore, comparator bandwidth and accuracy requirements are decoupled so that small and fast dynamic comparators, amenable to digital scaling, can be used. A calibration algorithm at power on sweeps a $600mV_{PP}$ differential input to select the most suitable subset of a bank of redundant

comparators. Unselected comparators are powered off. Power consumption is dominated by the power consumption of the encoding and clock network which consume 77% of the 204mW total power. The conservative value of comparator redundancy in the first prototype doubles the complexity of both the clock wiring and encoder. Extensive pipelining in the encoder to achieve very low measured BER, also increases power consumption. However, this architecture scales with CMOS technology and benefits from the power and speed advantages associated with each new process node. The prototype ADC has the highest ENOB and highest sampling frequency of any reported flash ADC utilizing redundancy.

Chapter 3 presented a SAH-less 9b two-stage pipeline ADC architecture that incorporates a new combination of redundancy and pipelining to enable GS/s sampling at moderate resolutions. The trip-points of the 2nd stage comparators are set purely by random and deliberate offsets to decouple ADC performance from matching requirements. Only twelve deliberate offsets and a 1σ comparator random offset of 17 ADC-LSBs with a redundancy of only four gives sufficient granularity to limit SNR degradation to less than 3dB with 90% yield. Reducing the gain from 16 to 2 in the 4b MDAC increases the feedback factor (β) from 1/17 to 1/3 which substantially relaxes the op-amp gain and bandwidth requirements by a factor of 5.7. Furthermore, the reduced op-amp output swing enables extensive cascoding with only a 1V power supply. Finally, the front-end sample and hold is substituted with digital trimming of a delay chain that matches the sampling paths of the 1st stage MDAC and its sub-ADC. The 1GS/s 9bit prototype ADC achieves a Nyquist FOM of 160fJ/conversion-step and has one of the best energy efficiencies among reported 1GS/s+ ADCs with ENOB > 7b.

Chapter 4 presents a 9b 2-times interleaved 2GS/s ADC that incorporates a new combination of op-amp and sub-ADC sharing to achieve a 1GHz input bandwidth and at the same time reduce power and area. The architecture interleaves two 9b two-stage pipeline ADCs and employs op-amp sharing and 2nd stage sub-ADC sharing between two time-interleaved 1st stage MDACs. This technique effectively decouples 2nd stage speed from 1st stage accuracy requirement to enable an efficient redundancy-based 6b flash sub-ADC to utilize the speed of the 45nm process and at the same time reduce active area. Furthermore, op-amp and 2nd stage sub-ADC sharing between two 1st stage MDACs eliminates the need for complex calibration schemes to correct for gain and offset mismatch between channels. Digital trimming corrects for timing mismatch between channels. The 2GS/s 9bit prototype ADC achieves a Nyquist FOM of 167fJ/conversion-step and has one of the best energy efficiencies among reported 1GS/s+ ADCs with ENOB > 7b.

5.3   Comparison with State of the Art

Figure 5-1 shows a plot of energy vs. SNDR of the three prototype ADCs (i.e. GEN1-3) presented in this work and other state of the art GS/s+ ADCs [48]. The plot shows that the energy[20] of the 2nd and 3rd generation prototype ADCs are in-line with current (i.e. VLSI 2012) state of the art GS/s+ ADCs with ≥ 8b resolution.

Figure 5-2 shows a plot of bandwidth vs. SNDR of the three prototype ADCs (i.e. GEN1-3) presented in this work and other state of the art GS/s+ ADCs [48]. The plot shows that the 2nd and 3rd generation prototype ADCs achieve both a speed and ENOB that are in-line with current (i.e. VLSI 2012) and previous (i.e. VLSI 1997-2011 &

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[20] In pico-Joules and defined as ADC power divided by ADC sample rate.

ISSCC 1997-2011) state of the art GS/s+ ADCs with ≥ 8b resolution. However, the power dissipation of each of the previous state of the art ADCs within this region are in the hundreds of milli-watts and is not reflected in Figure 5-2. TABLE VIII below compares key performance metrics of the 2nd and 3rd generation prototype ADCs with all other state of the art GS/s+ ADCs with ≥ 7b resolution. The 2nd and 3rd prototype ADCs achieve a Nyquist FOM[21] of 160fJ/conv-step and 167fJ/conv-step respectively and consume an active area of 0.125mm^2 and 0.215mm^2 respectively. They have one the best energy efficiencies and have one of the smallest areas among reported 1GS/s+ ADCs with ENOB > 7b.

TABLE VIII COMPARABLE GS/S+ ADCS WITH ≥ 7b RESOLUTION

YEAR	ARCHITECTURE	TECH	RES	Fs (GHz)	PWR (mW)	AREA (mm^2)	Nyquist ENOB	BW (MHz)	FOM (fJ/conv)	REF
2006	Pipe, TI	0.130	11	1	250	3.5	8.34	500	772	[23]
2007	SAR, TI	0.130	10	1.35	175	1.6	7	675	1013	[26]
2007	Pipe, TI	0.090	7	1.1	46	0.19	5.7	550	804	[49]
2008	Pipe, TI	0.065	8	0.8	30	0.12	7.05	400	283	[50]
2011	Pipe	0.040	12	3	500	0.4	8.1	1500	607	[15]
2011	Pipe, Folding	0.045	7	1.3	22	0.023	5.2	650	460	[28]
2011	Subranging	0.055	8	1	16	0.2	6.23	500	213	[21]
2011	Single Slope, TI	0.130	7	1	26.5	0.55	6.16	500	371	[51]
2011	SAR, TI	0.065	10	2.6	480	5.1	7.76	1300	852	[31]
2011	Pipe, TI	0.040	12	0.8	105	0.88	9.5	400	181	[27]
2012	Pipe	0.065	11	1	33	0.225	8.41	500	97	[52]
2012	SAR, TI	0.065	11	2.8	45	0.18	7.71	1400	76	[53]
2012	SAR, TI	0.065	8	1	4	0.013	6.81	500	34	[54]
2012	Pipe	0.045	9	1	27	0.125	7.4	500	160	GEN2, [33]
2013	Pipe, TI	0.045	9	2	45	0.215	7.07	1000	167	GEN3, [34]

A closer comparison of this work with current state of the art GS/s+ ADCs with ENOB > 7b also show an advantage in simplicity in both architecture and digital calibration methods for correcting ADC non-idealities.

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[21] FOM= PWR/(2$^{Nyquist\_ENOB}$*2*BW)

In [52], a SAH-less nine-stage 1GS/s 11b pipeline ADC employs a complex calibration algorithm, that leverages from the Karanicolas method [55], to determine correction coefficients that correct for capacitor mismatch in its 4b 1st stage and ADC errors from finite op-amp gain and offset in the first five stages. On the other hand, in [33] a SAH-less two-stage 1GS/s 9b pipeline ADC employs comparator redundancy in its 2nd stage to correct DNL errors and a simple code search calibration algorithm selects comparators closest to the desired trip points. Calibrating the 2nd stage through the ADC input inherently corrects ADC errors from finite op-amp gain and offset and no calibration is required to correct for capacitor mismatch in the 1st stage MDAC. Furthermore, simple digital trimming of a pair of delay chains matches the sampling paths between the 1st stage MDAC and its sub-ADC.

In [53], an 11b 2.8GS/s, 24-way interleaved SAR ADC employs a complex least-mean-square (LMS) calibration algorithm to determine the digital weight coefficients and offsets to correct for timing, gain and offset mismatch between channels. On the other hand, in [34] a 9b 2GS/s, 2-way interleaved, two-stage pipeline ADC employs 1st stage op-amp and 2nd stage sub-ADC sharing between two 1st stage MDACs which inherently eliminates the need for correcting gain and offset mismatch between channels. Like in [33], comparator redundancy in the shared 2nd stage corrects DNL errors and a simple code search calibration algorithm selects comparators closest to the desired trip points. Furthermore, simple digital trimming of pair of tunable delay circuits in the sampling paths corrects for timing mismatch between channels.
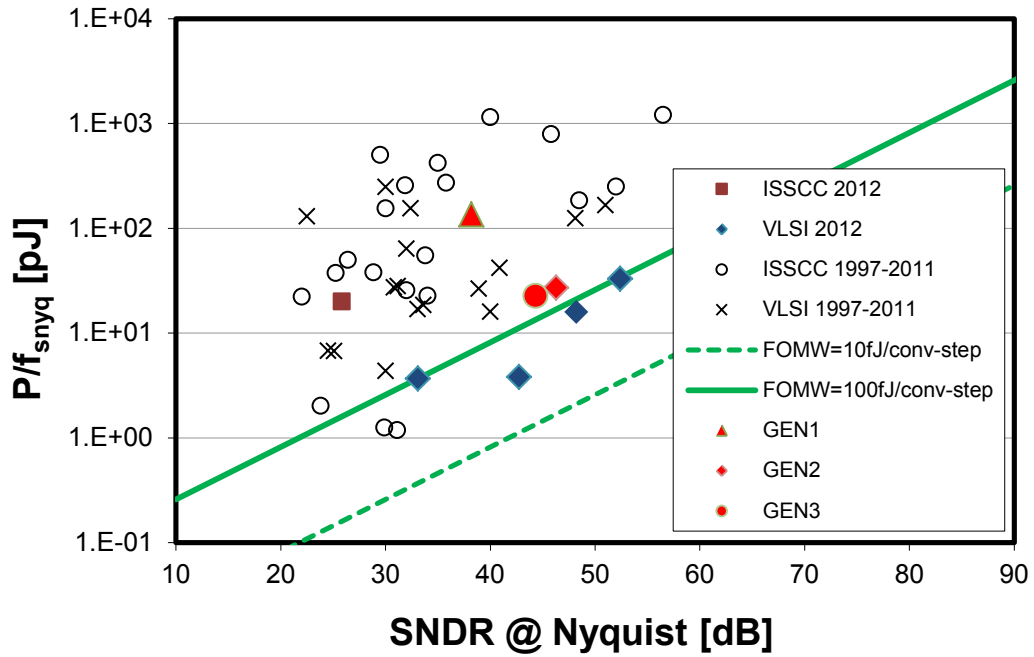
Figure 5-1 Energy vs. SNDR for comparing this work (i.e. GEN1-3) with other state of the art GS/s+ ADCs.
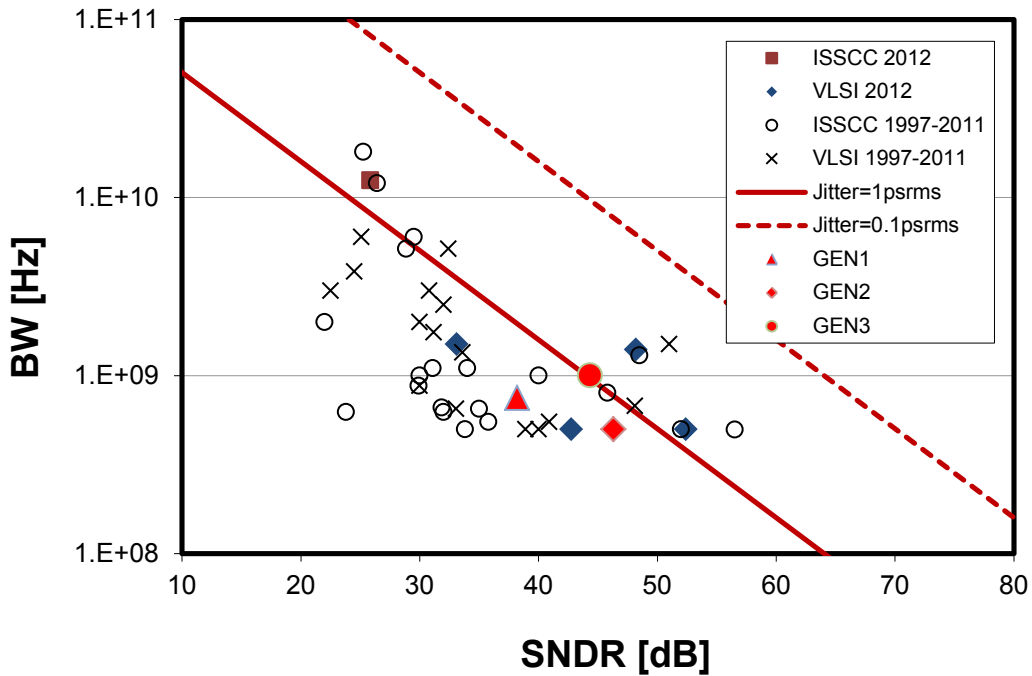
Figure 5-2 Bandwidth vs. SNDR for comparing this work (i.e. GEN1-3) with other state of the art GS/s+ ADCs.

5.4   Future Research Directions

5.4.1   A 10b 1GS/s 2X-Interleaved Pipeline ADC
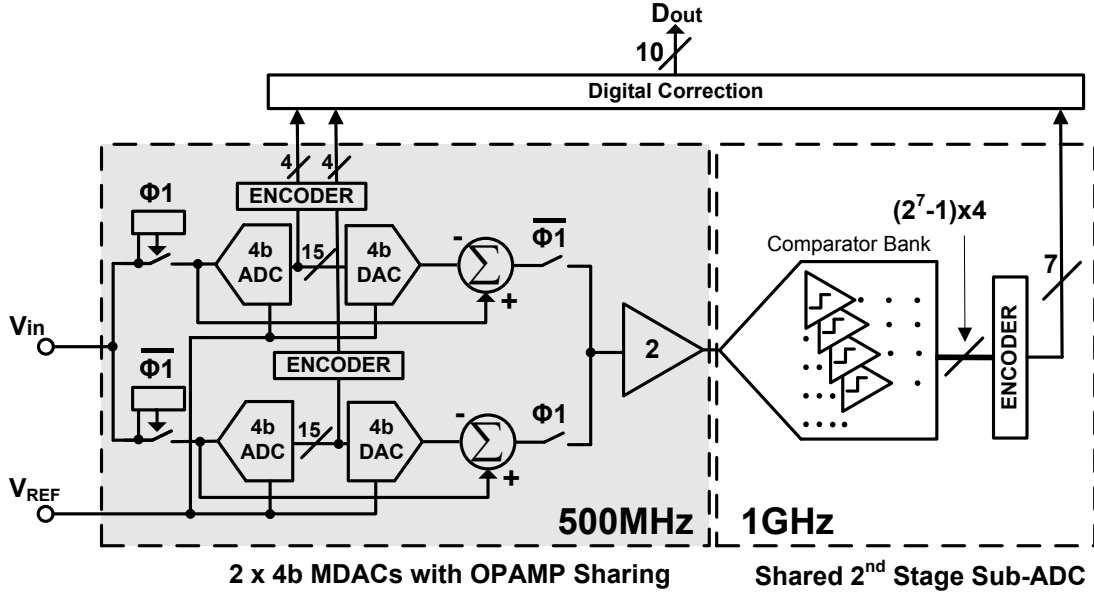
Figure 5-3 Proposed 10b 1GS/s ADC architecture.

Figure 3-19 of chapter 3 illustrates the deliberate and random offset scheme for setting a 2nd stage sub-ADC input range from -50mV to 150mV in both the 1GS/s and 2GS/s 9b ADC prototypes. A simple modification in the switching scheme in the MDAC followed by an increase in the ADC input range from 800mV$_{PP}$ to 1.2V$_{PP}$ yields an improved 2nd stage sub-ADC input range of ±150mV$_{PP}$. This modification can be followed by an increase in 2nd stage resolution to 7bits by doubling the number of comparators to yield a 10b two-stage pipeline ADC implementation. Furthermore, 0.4 ADC-LSBs of 2nd stage comparator noise[22] relative to the 9b ADC prototypes translates

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[22] Based on extracted noise simulations of 2nd stage sub-ADC comparators.

to 0.533 ADC-LSBs[23] of 2nd stage comparator noise relative to a 10b ADC with a 1.2V_{PP} input range. This is sufficiently attenuated by a 1st stage MDAC gain of two and yields an ADC SNR of 59.25dB[24]. However, a 1bit increase in 2nd stage resolution roughly doubles the sub-ADC input capacitance and halves the op-amp bandwidth. Therefore, for same settling accuracy (i.e. 5bits) the sample rate can be reduced by 1/2 and the remaining 1LSB of settling error is inherently corrected when calibrating the 2nd stage sub-ADC through the ADC input. Furthermore, the op-amp used in the 9b ADC prototypes incorporates a tunable negative resistance that can be used to enhance the gain to meet the increased open-loop gain requirement of 46dB. Leveraging the 2X-interleaved two-stage pipeline ADC architecture presented in chapter 4 is therefore a feasible approach for achieving 10bit resolution with a 500MHz Nyquist bandwidth with little overhead in terms of design time and complexity. Figure 5-3 shows the proposed ADC architecture. The estimated power is 40mW. Finally, this architecture would achieve the highest resolution with the least amount of interleaving and pipelining of any reported time-interleaved pipeline ADC or single-channel pipeline ADC of similar performance.

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[23] Increasing the resolution by 1bit for the same ADC input range doubles the input referred noise in LSB terms. However, increasing the ADC input range from 0.8 to 1.2 reduces noise by 0.8/1.2. Therefore, 0.533 = 0.4·2·0.8/1.2

[24] Quantization noise for an N bit ADC is 0.288LSB. For a 10b ADC, 0.533/2 LSB of input referred thermal noise equates to an $SNR = 20 \log \left(\frac{1024 LSB/2\sqrt{2}}{\sqrt{(0.288 LSB)^2 + (0.27 LSB)^2}} \right) = 59.25 dB$ (i.e. 9.5bits).

5.4.2   A 12b 2GS/s 2X-Interleaved Pipeline ADC
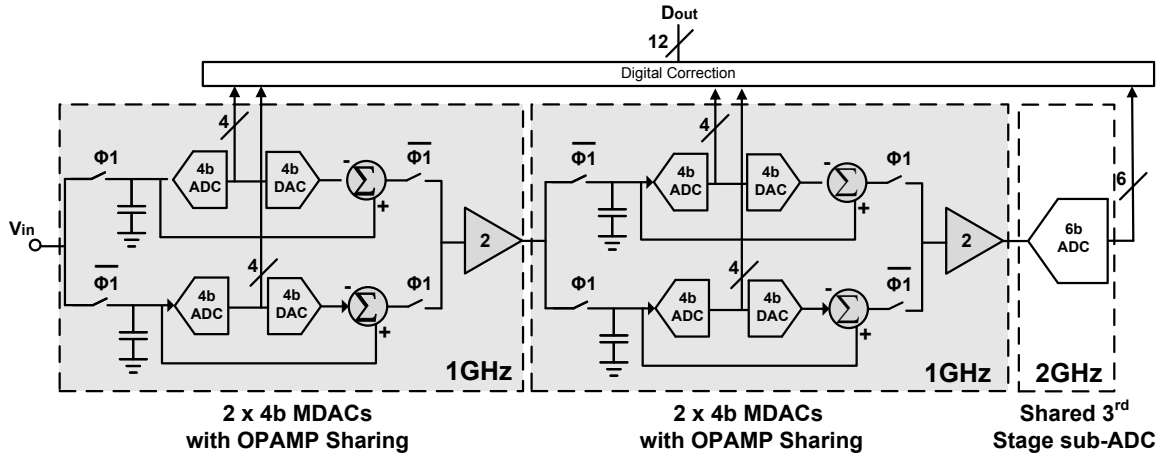
Figure 5-4 Proposed 12b 2GS/s ADC Architecture.

The time-interleaved architecture presented in chapter 4 can also be leveraged to implement in a 12b 2GS/s 2-times interleaved pipeline ADC. Figure 5-4 shows the proposed ADC architecture. Similar to the architecture presented in chapter 4, two 1st stage 4b MDACs are time-interleaved and a last stage 6b redundancy-based flash sub-ADC is shared between the two channels. However, by adding an additional 4b flash-based MDAC stage after the 1st stage MDAC in each channel, an additional 3bits is resolved for a total ADC resolution of 12 bits[25] . Furthermore, similar to the time-interleaved 1st stage MDACs, the 2nd stage MDACs are implemented with a gain of 2 instead of 16 and also incorporate op-amp sharing for power and area reduction. Furthermore, the op-amp used in the 9b ADC prototypes incorporates a tunable negative resistance that can be used to enhance the gain to meet the increased 1st stage op-amp open-loop gain requirement of 58dB. Sharing op-amps between two MDACs that reside

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[25] 1bit over-range in the 2nd and 3rd stage sub-ADCs compensate for 1st and 2nd stage comparator offsets.

in adjacent channels, and sharing the 3rd stage sub-ADC between the two-interleaved channels, eliminates channel mismatch due to gain and offset mismatch that arise when employing separate op-amps and sub-ADCs in each channel. Therefore complex calibration schemes to mitigate gain and offset mismatch between channels is not required. ADC errors due to finite op-amp gain, offset, non-linearity and incomplete settling can be corrected by calibrating the 3rd stage sub-ADC through the ADC input as shown in section 3.3.5 of chapter 3. Tunable delays in the front end sampling path mitigate clock skew between channels and 200fs granularity is sufficient for limiting degradation in ADC SNDR to less than 3dB for a 1GHz input signal. The estimated power consumption is 125mW. Finally, this architecture would achieve the highest sampling rate and resolution with the least amount of interleaving and pipelining of any reported time-interleaved pipeline ADC of similar performance.

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