Low Power Continuous-time Bandpass Delta-Sigma Modulators

by

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To Dad, Mom, my brother, and friends...

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ADC	Analog-to-digital converter
BPDSM	Bandpass delta-sigma modulator
BPF	Bandpass filter
CTBPDSM	Continuous-time bandpass delta-sigma modulator
CTDSM	Continuous-time delta-sigma modulator
CTLPDSM	Continuous-time lowpass delta-sigma modulator
DAC	Digital-to-analog converter
DEM	Dynamic element matching
DSM	Delta-sigma modulator
DSP	Digital signal process
DTBPDSM	Discrete-time bandpass delta-sigma modulator
DTDSM	Discrete-time delta-sigma modulator
FOM	Figure of merit
HPF	Highpass filter
HZ	Half-clock-delayed return-to-zero
LPF	Lowpass filter

LVDS	Low voltage differential swing
NRZ	None-return-to-zero
NTF	Noise transfer function
RZ	Return-to-zero
SDR	Software defined radio
SNDR	Signal to noise and distortion ratio
SNR	Signal to noise ratio
STF	Signal transfer function

Abstract

Low power techniques for continuous-time bandpass delta-sigma modulators (CTBPDSMs) are introduced. First, a 800MS/s low power 4^{th}-order CTBPDSM with 24MHz bandwidth at 200MHz IF is presented. A novel power-efficient resonator with a single amplifier is used in the loopfilter. A single op-amp resonator makes use of positive feedback to increase the quality factor. Also, a new 4^{th}-order architecture is introduced for system simplicity and low power. Low power consumption and a simple modulator structure are achieved by reducing the number of feedback DACs. This modulator achieves 58dB SNDR, and the total power consumption is 12mW.

Second, a 6^{th}-order CTBPDSM with duty cycle controlled DACs is presented. This prototype introduces new architecture for low power consumption and other important features. Duty cycle control enables the use of a single DAC per resonator without degrading the signal transfer function (STF), and helps to lower power consumption, low area, and thermal noise. This ADC provides input signal filtering, and increases the dynamic range by reducing the peaking in the STF. Furthermore, the center frequency is tunable so that the CTBPDSM is more useful in the receiver. The prototype second modulator achieves 69dB SNDR, and consumes 35mW, demonstrating the best FoM of 320fJ/conv.-step for CTBPDSMs using active resonators.

The techniques introduced in this research help CTBPDSMs have good power efficiency compared with the other kinds of ADCs, and make the implement of a software-defined radio

architecture easier which is appropriate for the future multiple standard radio receivers without a power penalty.

Chapter 1. Introduction

1.1 Software Defined Radio (SDR)

Our daily lives depend on the mobile devices such as cellphones and tablets more than ever as these devices are absorbing the features of other individual wireless devices. This means that mobile devices need to utilize several RF transceiver chips with different RF frequencies and bandwidths. Having more ICs on the board tends to increase the power consumption of mobile devices, and hence also increases the battery size. Therefore, a single receiver that supports multiple standards is very attractive for wireless communication since low power and small size are essential for handheld devices. The RF front-end not only has to be reconfigurable but also has to have wide bandwidth. However, most current wireless receivers rely on several inflexible analog blocks and at most support only a few standards.

One of the most popular receiver architectures is the super-heterodyne architecture, shown in Figure 1. This architecture is very good for frequency selectivity and sensitivity in an environment with strong interferers[1]. However, this architecture suffers from the complexity of receiver chain and the lack of reconfigurability. It also requires several stages of filtering,

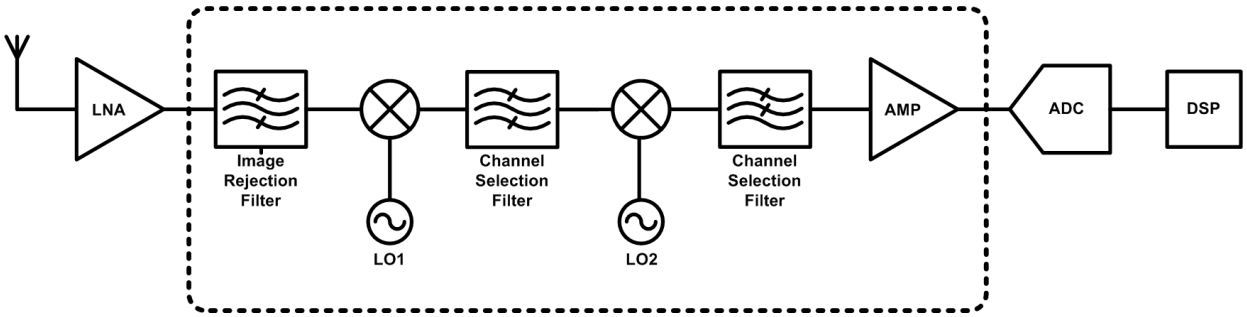


Figure 1. Super-heterodyne Receiver Architecture

mixing and amplification, which leads to a large area and high cost. In addition, the power consumption increases as more blocks are needed in the receiver. Furthermore some of the blocks such as SAW filters are off-chip, and this increases a board area needed.

A software-defined radio (SDR) is a good choice for future receivers. SDR is not a new concept, and was introduced in the 1980s[2]. However, SDR is currently used mainly for military applications which require flexible wireless communication for to a variety of protocols. Also, SDR can help enable cognitive radio, where the receiver is configured depending on the current usage of the channels to utilize the limited bandwidth efficiently[3].

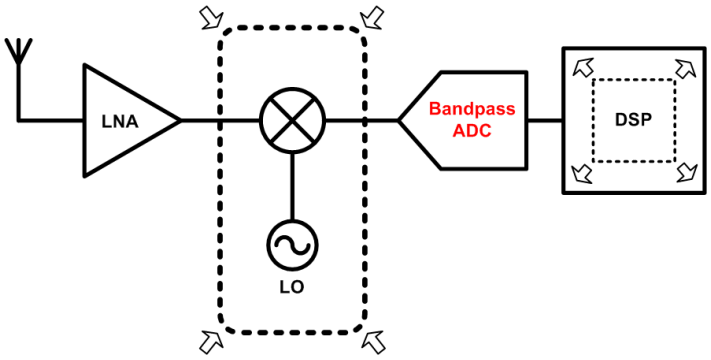


Figure 2. Software-defined radio

Currently, SDR is not practical due to the difficulties of implementation and the large power consumption[4]. Thanks to recent improvements in analog-to-digital converters (ADCs) and to the scaling of technology, SDR is again being strongly considered. As in Figure 2, an SDR omits many blocks in the super-heterodyne architecture by digitizing a wide band signal without down-converting to the baseband. Once the ADC passes the digitized signal to the digital signal processor (DSP), the DSP takes care of filtering, channel selection and mixing in the digital domain[5][6]. In most cases, digital processing costs less in terms of area and power because it is

not affected by thermal noise and mismatch, and therefore if the performance of the ADC can be addressed then SDR architecture is attractive for future mobile devices.

1.2 ΔΣ Modulators (DSM)

1.2.1 Oversampling ADC

ADCs convert analog inputs to digital signals based on sampling. Microprocessors are designed to process digital signals but every real signal exists in the analog domain[7]. Therefore, it is necessary to convert analog signals into the digital equivalents to make use of computing systems and to process data effectively. The quality of A-D conversion is very important in order not to lose the original information during the conversion, and it is mostly related with the resolution of the ADC. Due to the truncation, quantization noise is added to the original signal. This truncation error or quantization noise usually behaves like white noise. The quantization noise decreases the quality of the original signal by decreasing the signal-to-noise ratio (SNR). It is known that the fundamental limit of SNR in dB when one sample has 2^N possible levels which are evenly spaced is :

$$SNR = 6.02N + 1.76 \text{ [dB]}$$

This assumes that the quantization noise is uniformly distributed between the levels[8][9]. The quantization noise is summed up between DC and $F_s/2$ which is the highest frequency in discrete-time domain. $F_s/2$ is called Nyquist-rate. Nyquist-rate ADCs convert signals with frequencies up to Nyquist-rate and the quantization noise floor is flat in terms of the output power spectral density.

However, Nyquist-rate ADCs have shown limitations as technology develops and struggle to meet the requirements of high speed and high resolution for many applications. For Nyquist-rate ADCs, it is difficult to have both high speed and high resolution due to analog component imperfections[10][11]. For example, the mismatch between the passive components such as capacitors in SAR ADCs causes harmonics and distorts the signal. As CMOS technology scales, it gets more difficult to have good matching between components and the maximum resolution is becoming saturated[12].

Instead, an oversampling ADC improves resolution by increasing the sampling rate instead of increasing the number of sampled levels[13]. The higher sampling rate can cause more power consumption, but oversampling easily achieves high resolution. Thanks to the scaling of CMOS technology, high speed sampling is more feasible and oversampling ADCs are becoming attractive in many applications.

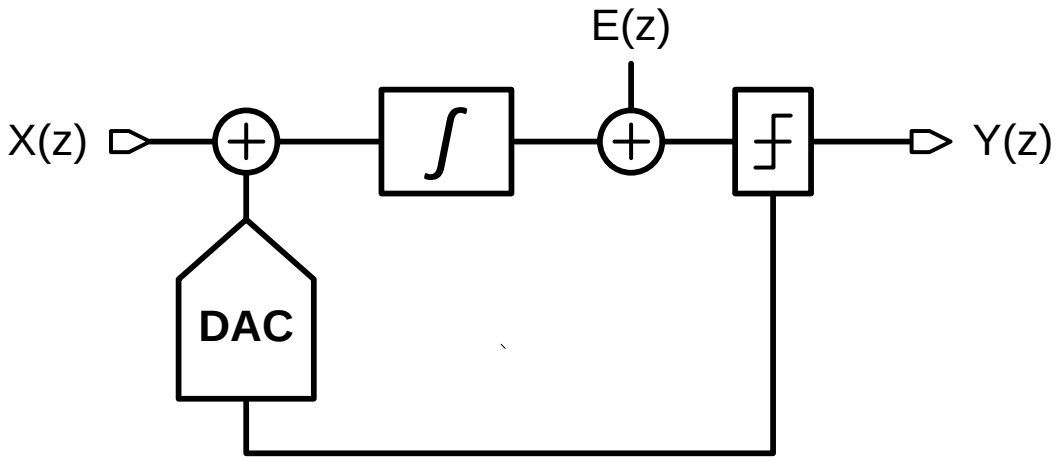


Figure 3. ΔΣ ADC

A ΔΣ modulator is commonly used in oversampling ADCs, and it cancels out the error coming from the analog component imperfections with the help of excessive sampling and

feedback loops[14]. The basic configuration is a feedback loop with filters, a local low-resolution ADC and feedback digital-to-analog converter (DAC) as shown in Figure 3. The transfer function from the input *X* to the output *Y* is called signal transfer function (STF), and the transfer function from the quantization noise *E* to the output *Y* is noise transfer function (NTF). Both STF and NTF are determined by the loop transfer function, but they differ since the summing nodes are different. Through the feedback loop, the quantization noise *e(n)* is reduced by *e(n-1)*, which is the quantization noise from the previous sample. This makes the NTF highpass, and causes the quantization noise distribution over frequency to be non-uniform. In other words, the feedback loop generates a notch at DC in the NTF and shapes the quantization noise, decreasing the in-band noise floor level as in Figure 4. The STF is not affected by this noise shaping since STF and NTF are different as mentioned and STF can be flat in-band with appropriate loop configurations. A high SNR can be achieved by considering the signal and the noise only in a specific frequency range where the noise floor level is lowered through noise shaping.

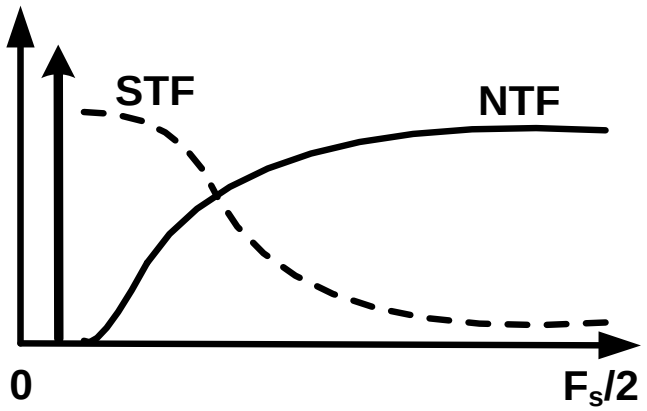


Figure 4. STF and NTF of ΔΣ modulators

The advantage of ΔΣ modulators is their immunity to the analog component imperfections which is a problem even in modern CMOS technology[15]. For example, a coarse ADC can be used because the imperfections of the coarse ADC are also frequency-shaped by the same feedback loop as the quantization noise, and therefore do not affect the SNR. Also, the input offset of the filters are dithered out by a large amount of sampling and averaging. Recent development in ΔΣ modulators has lead to high resolution, wide bandwidth and good power efficiency, so ΔΣ modulators are becoming more important in wireless systems[16]-[20].

1.2.2 Discrete-time ΔΣ Modulator

The first time ΔΣ modulators were implemented in the discrete-time domain by using switched-capacitor circuits in standard CMOS technology[21]. The system is represented in z-domain, so the analysis of pole-zero in the STF and NTF is apparent as in the example in Figure 5. Therefore, fine tuning is possible even in a higher order modulator since every block can be expressed with linear model.

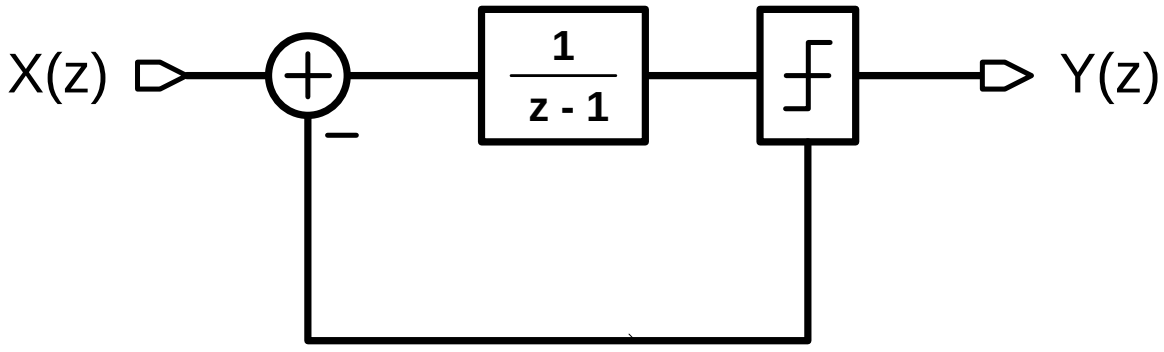


Figure 5. 1st-order discrete-time ΔΣ modulator

While a discrete-time ΔΣ modulator (DTDSM) is suited to optimization[22], the circuit implementation brings up some problems. Although the use of switched-capacitors can easily

map the transfer functions to circuits, switched-capacitors are very slow due to the required settling time[23]. The settling error at the frontend of the modulator causes nonlinearity and decreases SNDR (signal-to-noise and distortion ratio)[24]. Also, switched-capacitor circuits have issues such as charge injection and clock feed-through and require a very accurate sample-and-hold circuit at the front. Therefore, although they provide high resolution, DTDSMs are not appropriate for high speed applications.

1.2.3 Continuous-time ΔΣ Modulator

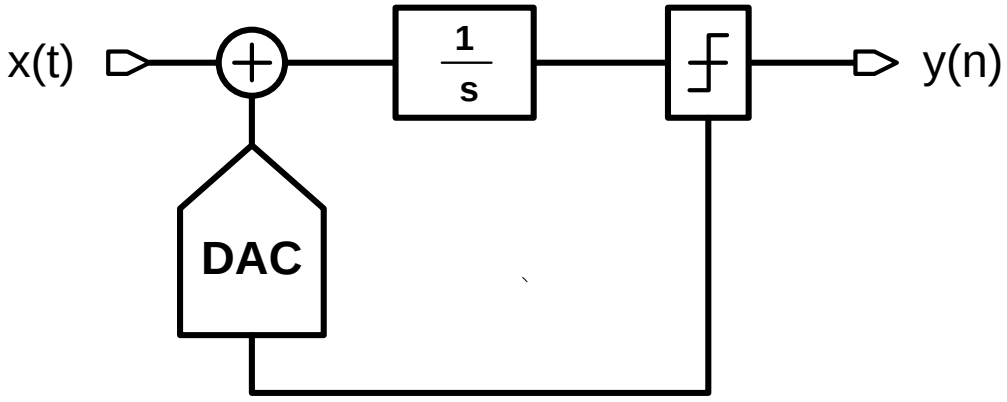


Figure 6. 1st-order continuous-time ΔΣ modulator

A continuous-time ΔΣ modulator (CTDSM) uses continuous-time analog filters instead of switched capacitors as in Figure 6. For example, an active RC integrator can be used in the place of the discrete-time integrator which is based on the feedback with a delay. The sampling occurs only at the local ADC, and the sampling error is not critical as mentioned in 1.2.1. The use of continuous-time analog filters allows the modulator to operate at higher frequency and have a wider bandwidth since the filter does not need to settle within the clock period[25]. Also, the power consumption is lower[26] compared to discrete-time counterparts, since the switching circuitry requires a lot of power. Another important advantage is the intrinsic anti-alias filtering,

which is important because it makes the anti-alias filter at the input of the ADC unnecessary, saving power and area[27].

However, the CTDSM architecture has two critical drawbacks, namely, excess loop delay[28] and high clock jitter sensitivity[29]-[31]. The excess loop delay is the delay from the quantizer output to the output of DACs, and causes the loop to be instable. The problem is that it is impossible to totally remove the excess loop delay in a continuous-time system. And clock jitter varies the charge amount from the DAC to the filter. The change in the charge amount appears as input noise, and decreases SNR. The effect of clock jitter becomes severe as the sampling frequency goes higher. However, these problems are becoming easier to tackle with scaling and the use of new CTDSM architectures[32][33]. Therefore, CTDSMs are becoming more attractive than DTDSMs for mobile environment because of the high speed and good power efficiency.

1.2.4 Bandpass ΔΣ Modulator

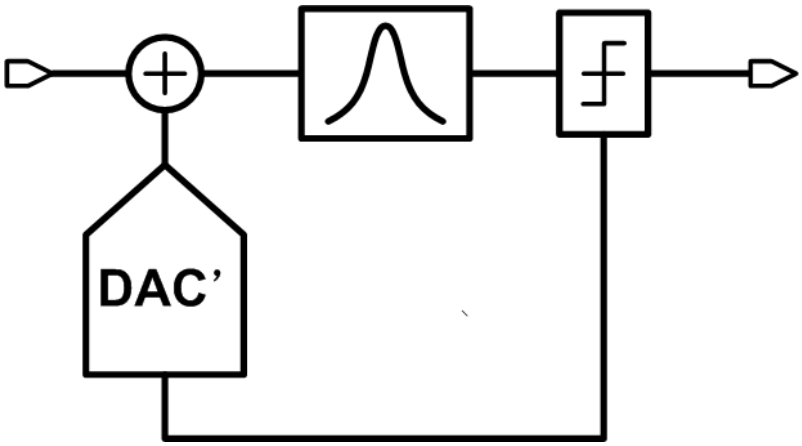


Figure 7. Bandpass ΔΣ modulator

The DSMs explained previously are lowpass modulators which use integrators in the loopfilter. Lowpass modulators have notches around DC in the NTF, thus the signal band is located at low frequency as in Figure 4. By using another kind of filters in the loopfilter, it is

possible to modify the STF and NTF to provide different noise shaping to that of lowpass modulator. The use of a resonator in the loopfilter leads to the bandpass ΔΣ modulator (BPDSM) in Figure 7, which has notches in the NTF at a mid or high frequency region[34][35]. This means that the noise shaping lowers the noise floor level at RF or IF as shown in Figure 8. Accordingly, the signal band can be at RF or IF, and in this way it becomes possible to digitize the signal directly without down-converting when the signals are transmitted with modulation[36].

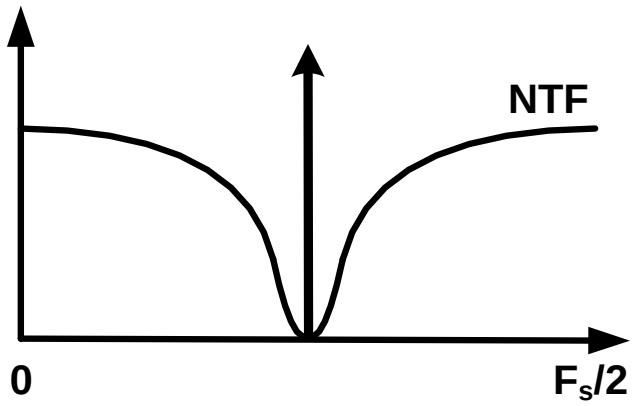


Figure 8. NTF of bandpass ΔΣ modulator

We can easily get the transfer function for discrete-time bandpass ΔΣ modulators (DTBPDSMs) by replacing z with $-z^2$ in the discrete-time transfer function of LPDSMs[37], as in Figure 9. The discrete-time resonator consists of two-delay block in the feedback path. The continuous-time resonator can be an LC resonator or a bi-quadratic resonator, but the feedback DAC topology requires some modification since the continuous-time resonator is not mapped to the discrete-time transfer function correctly[38]-[40].

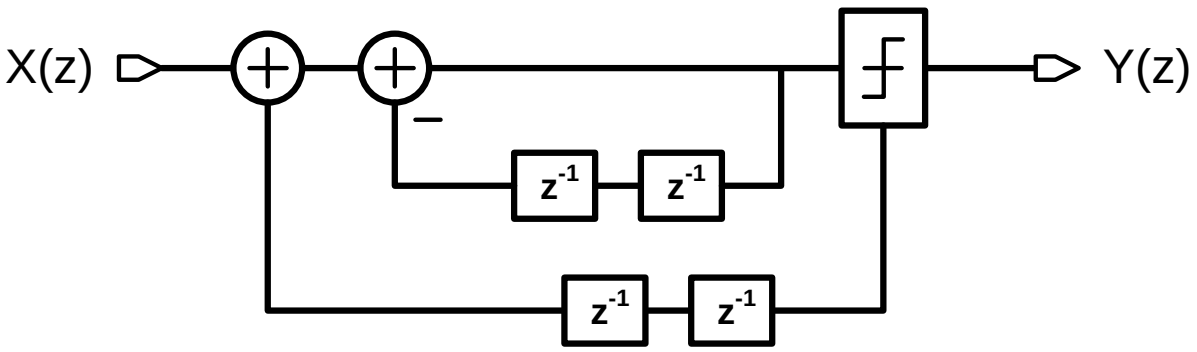


Figure 9. Discrete-time bandpass ΔΣ modulator

1.3 Continuous-time Bandpass ΔΣ Modulator (CTBPDSM)

1.3.1 CTBPDSM in SDR

The bottleneck in the realization of SDR is the design of an ADC with wide bandwidth, high resolution, and reasonable power consumption[4]. The use of Nyquist-rate ADCs is not a good solution, since it is difficult to achieve a very high sampling rate at high resolution because of component mismatches and power consumption[41]. Furthermore there is no channel selectivity with a Nyquist ADC since it digitizes the entire spectrum below the Nyquist frequency. A continuous-time lowpass ΔΣ modulator (CTLPDSM) is better in terms of power efficiency, but its lowpass nature is not appropriate for SDR. On the other hand a CTBPDSM has features that make it very attractive for SDR. A CTBPDSM digitizes RF or IF signals directly, and the frequency band can be tuned in some architectures [42].

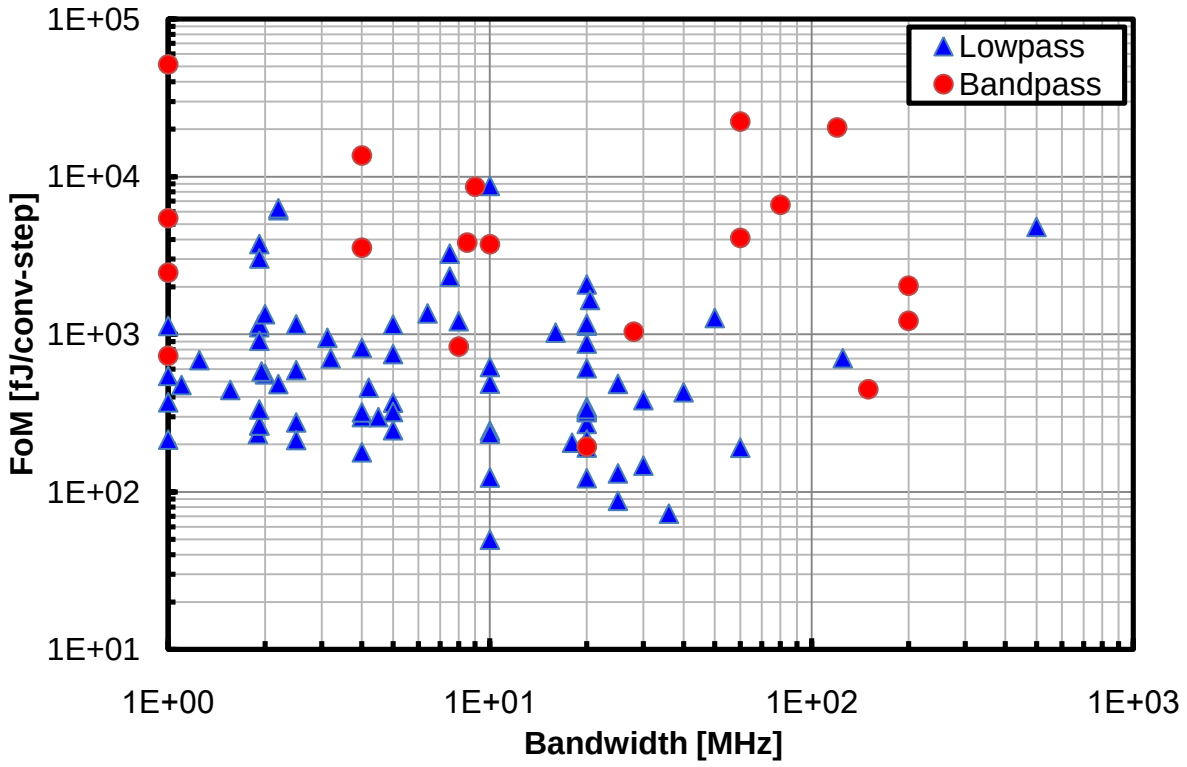


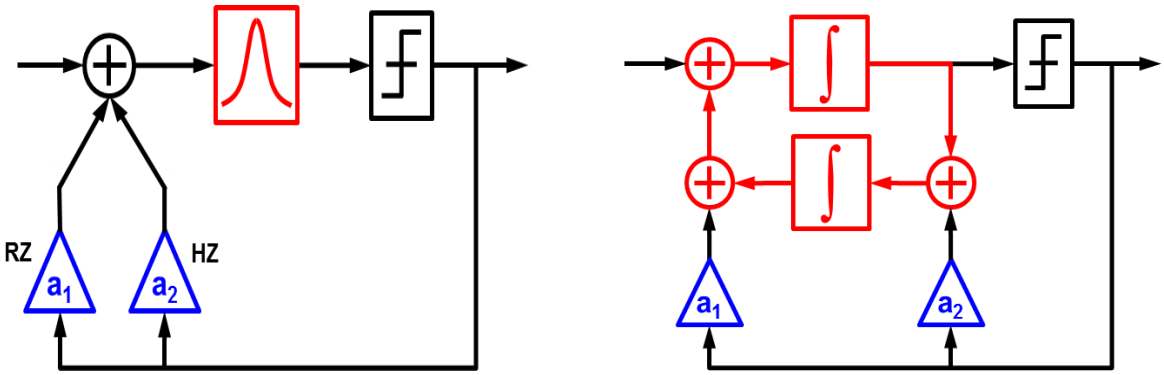
Figure 10. Power efficiency of CTLPDSMs vs. CTBPDSMs

Although noise shaping enables high resolution, CTBPDSMs still consume a lot of power. Continuous-time operation helps achieve good power efficiency, however state-of-the-art CTBPDSMs show worse energy efficiency compared to other kinds of ADCs. The poor energy efficiency of CTBPDSMs limits their use in receivers.

CTLPDSMs are dominant in many applications due to their performance and simplicity as well as power efficiency. Figure 10 compares the power efficiency of recently published lowpass and bandpass ΔΣ modulators[43]-[56]. There is a big difference between the best figure-of-merit (FoM) for CTLPDSMs and CTBPDSMs. While the CTLPDSM architecture is not suitable for SDR because it cannot digitize signals at RF or IF, it is very power-efficient and is an attractive ADC architecture for the complex super-heterodyne architecture. However, CTBPDSMs still

have enormous potential considering that the SDR architecture is more desirable for the future wireless communication systems.

1.3.2 Conventional CTBPDSM Architectures



(a) Passive Resonator **(b) Active Resonator**

Figure 11. Conventional CTBPDSM architectures

An LC tank resonator can be used as the filter in a CTBPDSM[57]. Figure 11(a) shows the conventional CTBPDSM architecture using an LC tank resonator[58]. It requires two DACs per resonator. These DACs are a return-to-zero (RZ) DAC and a half-clock-delayed return-to-zero (HZ) DAC. Two kinds of DACs with different phases are used in the feedback loop to map the discrete-time transfer function to the continuous-time transfer function correctly regardless of the reduced number of summing nodes.

For example, in second-order modulation, the discrete-time loop transfer function of the modulator is :

$$\frac{z^{-2}}{1+z^{-2}} \tag{1}$$

The transfer function of a continuous-time resonator is expressed as :

$$\frac{s\omega}{s^2+\omega^2} \tag{2}$$

and the impulse response of the resonator is :

$$h(n) = \begin{cases} 0 & n = 0,1 \\ cos\left(\frac{(n-2)\pi}{2}\right) & n = 2,3,\dots \end{cases} \quad (3)$$

An RZ DAC has a transfer function in the continuous-time domain of :

$$\frac{1 - e^{-sT_s/2}}{s} \quad (4)$$

Then, the loop transfer function coming from the resonator and the RZ DAC can be transformed into a discrete-time form by sampling the impulse response with F_s.

$$T_{res} \times T_{RZ} = \frac{z^{-1}((1 - 1/\sqrt{2}) - 1/\sqrt{2}\, z^{-1})}{1 + z^{-2}} \quad (5)$$

$$T_{res} \times T_{HZ} = \frac{z^{-1}(1/\sqrt{2} - (1 - 1/\sqrt{2})z^{-1})}{1 + z^{-2}} \quad (6)$$

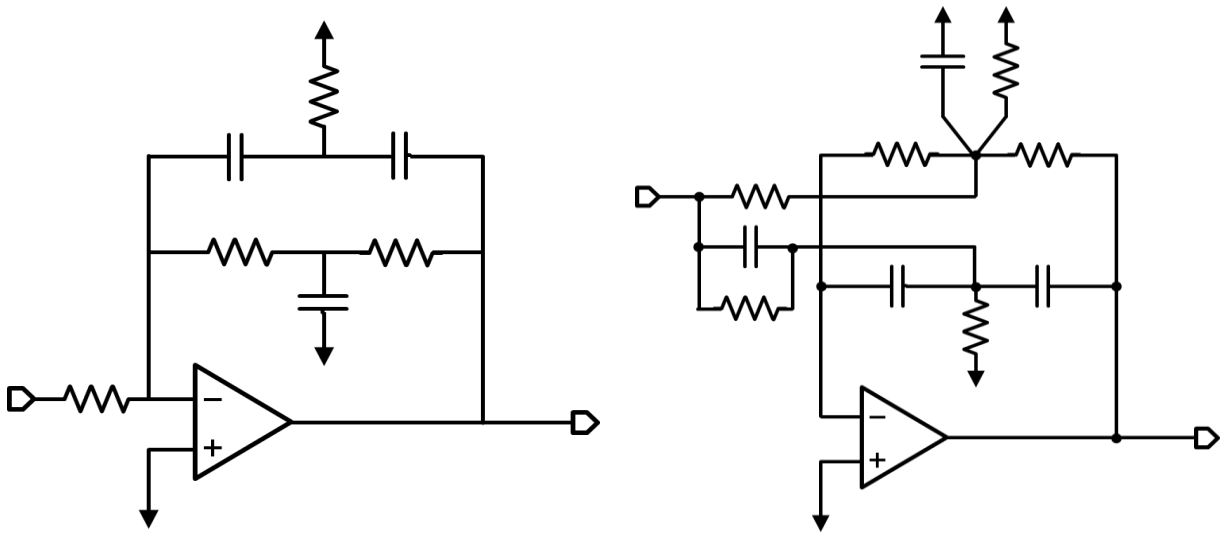
(5) and (6) are the sampled loop transfer function using RZ DAC and HZ DAC, respectively. The goal is to get (1), and this can be achieved by a linear combination of (5) and (6). Therefore, the perfect mapping from the discrete-time domain to the continuous-time domain is possible thanks to the use of two DACs with different phases.

The main advantages of this architecture are low power, low noise and the high quality factor of the resonator. However, this approach requires two feedback DACs per resonator, and this increases both the silicon area and the overall power consumption. In contrast there is one feedback DAC per integrator in a CTLPDSM. Also, the chip is large due to the size of the inductors and the inductors do not get smaller as the technology scales.

A bi-quadratic resonator can be used instead of LC tank resonators[59][60]. A bi-quadratic resonator consists of two integrators in a loop. A bi-quadratic resonator provides two summing

nodes, which allows a different CTBPDSM architecture as shown in Figure 11(b). This architecture is from the direct mapping from a discrete-time transfer function to a continuous-time transfer function since both need two integrators to implement a resonator. Two feedback DACs are connected to each summing node, and these are both non-return-to-zero (NRZ) DACs. The use of an active resonator avoids large inductors, but each integrator uses an op-amp which is power hungry and contributes thermal noise to the modulator.

1.4 Single Op-amp Resonator



(a) Twin-T filter **(b) Modified Twin-T filter**

Figure 12. Single op-amp resonators

A single op-amp resonator can replace conventional resonators in CTBPDSMs, and achieve both low power consumption and small silicon area. In this way, only one op-amp generates thermal noise into the loop, so that the total noise is lower. This means lower power consumption

for a given noise requirement. Also, the use of a single op-amp makes the chip design easier due to the reduced number of components and reduced silicon area.

Several single op-amp resonators have been reported[61][62]. The twin-T filter in Figure 12(a) has two feedbacks which cause resonance, but this filter is not suitable for CTBPDSMs because the transfer function is different to that of an ideal resonator. It resonates at a certain frequency, but it does not filter the low frequency perfectly. The modified twin-T filter in Figure 12(b) is based on the twin-T filter, and the transfer function is improved and also flexible. However, the input stage is not purely resistive, and it is difficult to be integrated with current-mode DACs because the summing nodes for the two feedback DACs see a different transfer function to the inputs. Also, this resonator has many passive components that contribute to the total thermal noise. Therefore, a new single op-amp resonator with an appropriate transfer function and summing nodes, as well as fewer passive components, is the key for low power CTBPDSMs.

1.5 Application Specifications

The target of this research is to design a CTBPDSM modulator which can cover the following standards:

- UMTS (US) : 5MHz @ 2100MHz with 12b
- CDMA2000 (Europe) : 1.25MHz @ 2100MHz with 13b
- 802.11b/g : 22MHz @ 2400MHz with 6b

The carrier frequencies of these three standards are close to each other, and a receiver with a tunable CTBPDSM can be reconfigured for them without standard-specific analog components.

The prototype does not include the LNA and mixer, and the modulator converts input signals at 200MHz with 24MHz bandwidth and 10bit (1st prototype) or 12bit (2nd prototype) resolution. This modulator specification is enough for the standards above, and it can also support more standards between 2GHz-2.4GHz.

1.6 Research Contributions

A single op-amp resonator with positive feedback is used for lower power consumption and area. This new single op-amp resonator can replace the existing resonators which have either large area or high power consumption.

Also, new CTBPDSM architectures are presented; one reduces the number of feedback DACs and achieves good power efficiency, while the other uses duty-cycle-controlled DACs for low power consumption and other features. The duty cycle control enables the modulator to have frequency tuning and to bandpass-filter input signal. And the redesign of op-amps and DACs provides the latter architecture 11dB more SNDR in the test compared with the first one by reducing the noise from the circuits.

1.7 Research Overview

By improving the power efficiency of CTBPDSMs to that of CTLPDSMs, SDR can be made practical receiver architecture for mobile platforms. The goal of this research is to reduce the power consumption of CTBPDSMs by adopting a new architecture and a new single op-amp resonator. In Chapter 2, a new CTBPDSM architecture, which minimizes the number of

components in the feedback loop, is introduced. This architecture lowers the total power consumption and the silicon area. Also, the circuitry for each block, including the new single op-amp resonator, is explained. Chapter 2 also presents the evaluation results of the CTBPDSM prototype. Chapter 3 introduces an improved prototype with a higher-order CTBPDSM architecture and better performance. This chapter also describes new blocks that improve the noise and linearity performance of the modulator, and presents measurement results. Chapter 4 suggests future work and Chapter 5 summarizes the research contributions.

Chapter 2. CTBPDSM with a Reduced Number of DACs and Single Op-amp Resonators

2.1 System Architecture

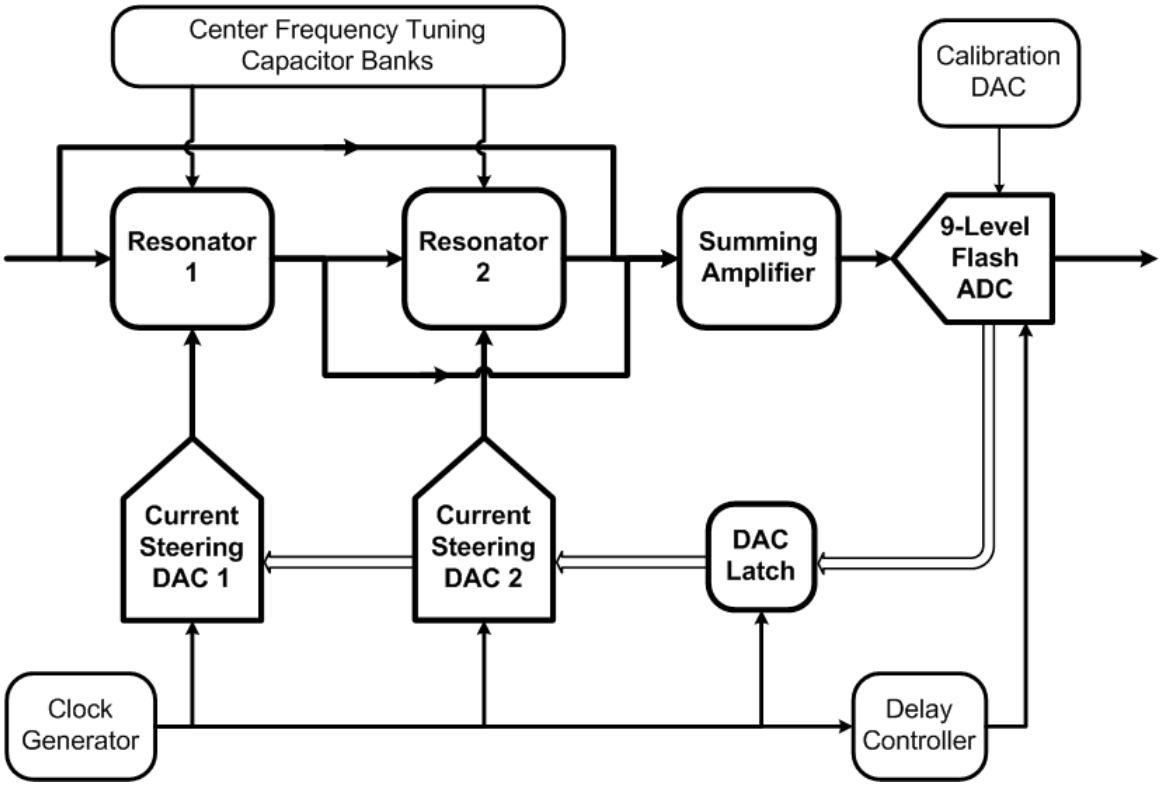


Figure 13. System block diagram

2.1.1 Overview

The modulator performance mostly depends on the modulator architecture. There are many factors for the architecture such as the modulation order, the quantizer bit number, and the feedback or feedforward topology. Therefore, the architecture design is important to achieve the required performance with the best power efficiency. This new CTBPDSM has a 4^{th}-order architecture with 3bit quantization as shown in Figure 13. Two resonators and two DACs are

used to achieve 4th-order bandpass noise shaping. Both resonators are single op-amp resonators and capacitor banks tune both the resonant frequencies and the quality factor. As discussed in the next section (2.1.2), the modulator has two DACs instead of four DACs. The DACs are both current-steering DACs. *DAC1* connected to *Resonator 1* is a half-clock-delayed return-to-zero (HZ) DAC while *DAC2* connected to *Resonator 2* is a return-to-zero (RZ) DAC. *Resonator1* and *DAC1* are more critical in regards to noise performance. The summing amplifier sums the output of *Resonator2* and the feedforward paths (which are the modulator input) and the *Resonator1* output. A 9-level flash ADC quantizes the output of the summing amplifier. An auxiliary current DAC, dedicated to the flash ADC, calibrates the offset of the comparators. The clock generator receives a sine wave from off-chip and generates a square clock waveform appropriate for this modulator. To compensate for the clock timing difference between the DACs and the flash ADC, a clock delay controller is used to clock the flash ADC.

2.1.2 Reduction of the number of current-mode DACs

As discussed in 2.2.1, we use a single op-amp resonator as the resonator in this CTBPDSM. This single-opamp resonator has only one summing node for the feedback loop paths. As with LC resonators in other CTBPDSMs, which similarly present only one summing node, this motivates the use of a multi-path feedback design for the modulator shown in Figure 14(a), which perfectly transforms a DTBPDSM into a CTBPDSM with LC resonators. However, the use of multiple feedback paths per resonator increases static power and adds more noise to the first resonator. Adding feedforward paths can replace the feedback DACs since it leads to the same loop transfer function as when only feedback paths exist[63]. Therefore, a feedforward path from the first resonator output to the quantizer removes two feedback DACs in a 4th-order

CTBPDSM, but even with a feedforward path, the two DACs at the front of the modulator remain the same and still add noise to the first resonator input which is critical to the total modulator input referred noise. In this work, a different analysis of a multi-path feedback design leads to noise reduction as well as power consumption reduction by using only one feedback DAC per resonator along with signal feedforward paths around the resonators.

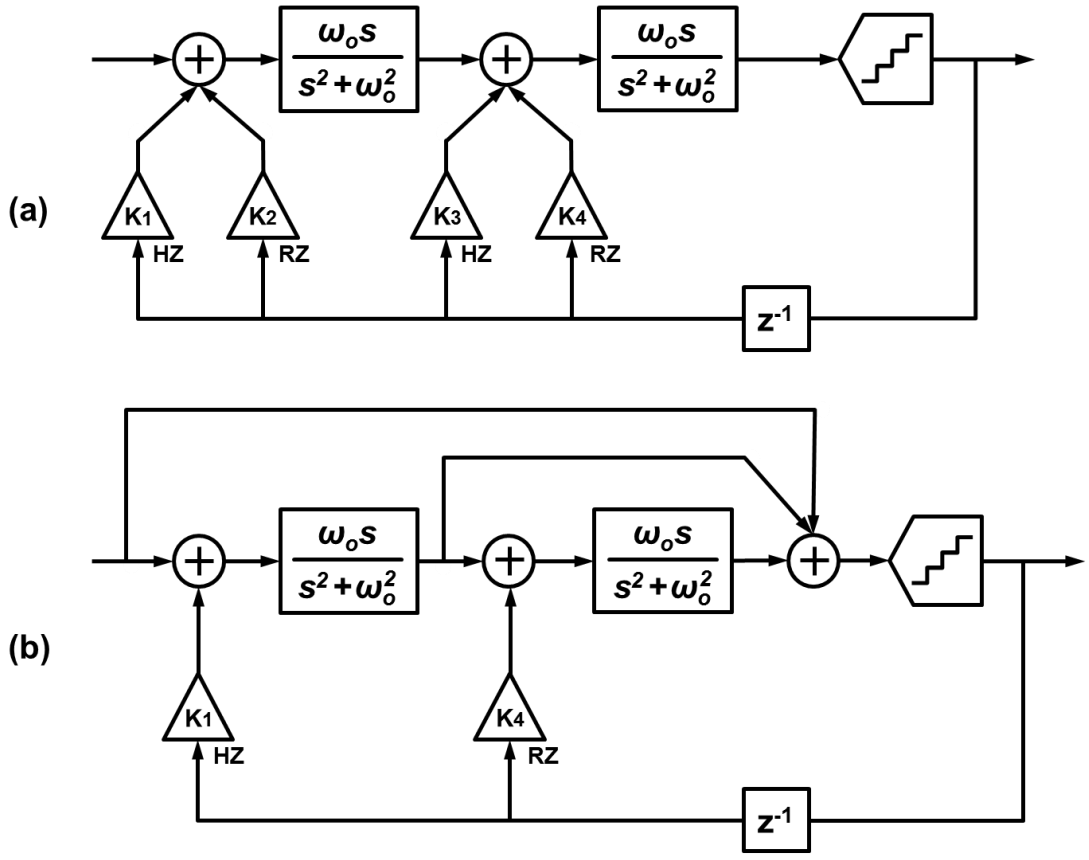


Figure 14. 4th-order CTBPDSM architecture (a) conventional (b) simplified

Due to the delay block and the excess loop delay a classic discrete-time to continuous-time pole-zero mapping to synthesize a continuous-time transfer function from a discrete-time transfer function is not easy and the final pole-zero needs to be tweaked after the transformation[64]. Also, imperfections of system blocks, including the finite quality factor of the resonators, make

the tweaking necessary. Therefore the use of ideal modulator coefficients might not lead to optimal performance in a real system. However, this characteristic also provides the possibility for the modulator coefficients to be flexible to some degree. Even though one of the feedback coefficients varies slightly due to any analog imperfections, a small change of the other coefficients can compensate for this to keep the stability and the performance. With the original coefficients of the two DACs connected to the first resonator (Figure 14(a)), K_2 is much smaller than K_1 when the coefficients are calculated as in [58] and optimized for 3bit quantization. And the result of the removal of K_2 does not lead to instability, but it causes peaking in the NTF and degrades the SNDR. However, the original value of K_2 is small, and K_1, $K_{3\text{-}4}$ can be tuned to compensate for the nulling of K_2. Suitable tuning of K_1, $K_{3\text{-}4}$ removes the NTF peaking and provides essentially the same noise shaping as with a non-zero K_2. The only difference is the symmetry of the overall power spectral density centered at the quarter of the sampling frequency: zeroing K_2 makes the slopes of the NTF on the left and right side of the center frequency slightly different, as shown in Figure 15. However this asymmetry does not affect the noise shaping within the passband and the performance in the in-band, including the maximum SNDR, is the same. The key point is that $K_2 < K_1$ allows removal of K_2. On the other hand, removing K_1 instead of K_2 is difficult since in this case coefficients' sensitivity introduces instability and performance degradation.

Similarly, K_3 or K_4 cannot be nulled once K_2 is zeroed or two other coefficients, instead of three, have to be tuned to compensate, and this leads to a large variation in the coefficients and ultimately to a significant performance degradation. Thus a feedforward path is used to remove another feedback DAC, K_3. The feedforward path from the first resonator output to the quantizer

provides the same feedback loop represented by one HZ DAC, K_3 and the second resonator because the loop consisting of the first resonator and the feedforward path also contains one HZ DAC and one resonator. Figure 14(b) shows the architecture after the modifications.

Next we show that by using a half-width DAC[66] instead of a NRZ DAC, the NTF in the passband does not change for the architecture introduced here.

Traditionally, an NRZ DAC is represented by a constant coefficient in a z-domain representation of the modulator. But in a continuous-time system, an NRZ pulse with a sampling period of T_s has a transfer function of

$$(1 - exp(-sT_s))/s \tag{7}$$

At lower frequencies, the exponential term can be approximated as :

$$exp(-sT_s) \approx 1 - sT_s \tag{8}$$

This is because, for a high oversampling ratio, sT_s is very small in the frequency range of interest. Hence (7) is close to T_s, leading to a constant value as required. On the other hand, this approximation is not accurate for the passband (e.g. at $F_s/4$) of a bandpass modulator.

Instead, a half-width RZ or HZ pulse represented by

$$(1 - exp(-sT_s/2))/s \tag{9}$$

can be approximated by the exponential term $exp(-sT_s)$ giving a much better approximation to a constant value within the passband of a bandpass system thanks to the halved exponential term.

$$NTF(s) = \frac{(s^2 + \omega_o^2)^2}{s^4 - c_2\omega_o s^3 + (2 - c_1)\omega_o^2 s^2 - c_2\omega_o^3 s + \omega_o^4} \tag{10}$$

$$\text{where } c_1 = (k_1 + k_2),\ c_2 = (k_3 + k_4) \tag{11}$$

Equation (10) is the NTF of the 4th-order multi-path feedback design in Figure 14(a), and we get the NTF around the center frequency by assuming that the DAC coefficients are constants.

$$NTF(s) = \frac{(s^2 + w_o^2)^2}{s^4 - (k_1 + k_4)w_o s^3 + (2 - k_1)w_o^2 s^2 - (k_1 + k_4)w_o^3 s + w_o^4} \quad (12)$$

And (12) is the NTF of the new architecture in Figure 14(b) with the same assumption on the DAC coefficients. A key observation about the two NTFs is that they can have the same noise shaping around the center frequency if the coefficients are properly chosen. This is why this new architecture can keep the same SNDR as the conventional CTBPDSMs even though the number of DACs is reduced.

The feedforward path from the input to the quantizer decreases signal swing through the analog signal path[67][68], which is helpful for low power consumption and for the linearity of resonators. As a result, this modulator architecture is advantageous in terms of power, complexity, and silicon area compared to existing architectures.

2.1.3 Noise Transfer Function (NTF)

The sampling frequency of the prototype modulator is 800MHz, and the center frequency is 200MHz. The required bandwidth is 24MHz as specified in the previous chapter, so the OSR is 16.7. Based on a target SNDR of 70dB and this OSR, at least a 4th-order architecture with 3bit quantization or a 6th-order one with 2bit quantization is required[10]. A 2nd-order architecture or an 8th-order one is not suitable due to higher power consumption and instability[69]. The 4th-order architecture is adopted for this modulator because it is more stable even with analog component mismatches but the total power requirement is similar to the 6th-order one.

The two notches generated by the two resonators are located at the same frequency as in Figure 15 and the simulation of this modulator shows 70dB SNDR when the input is a 200MHz tone. The STF is flat because the feedforward paths are used in this architecture[67], but there is still attenuation at higher frequency region for anti-aliasing.

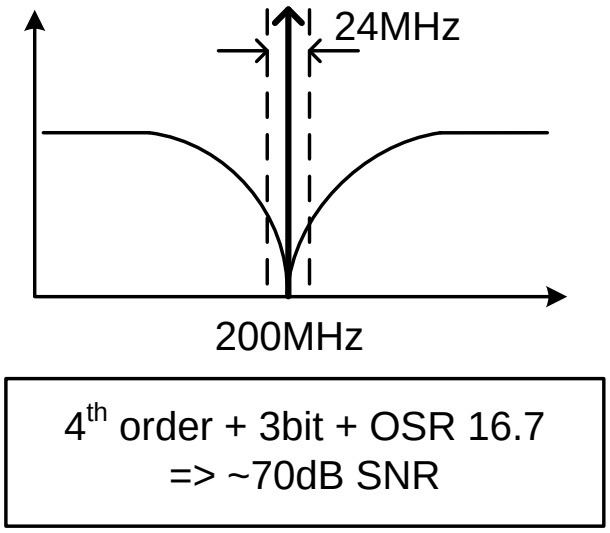


Figure 15. Noise transfer function of the modulator

2.2 Circuit Blocks

2.2.1 Single Op-Amp Resonator

2.2.1.1 Positive Feedback

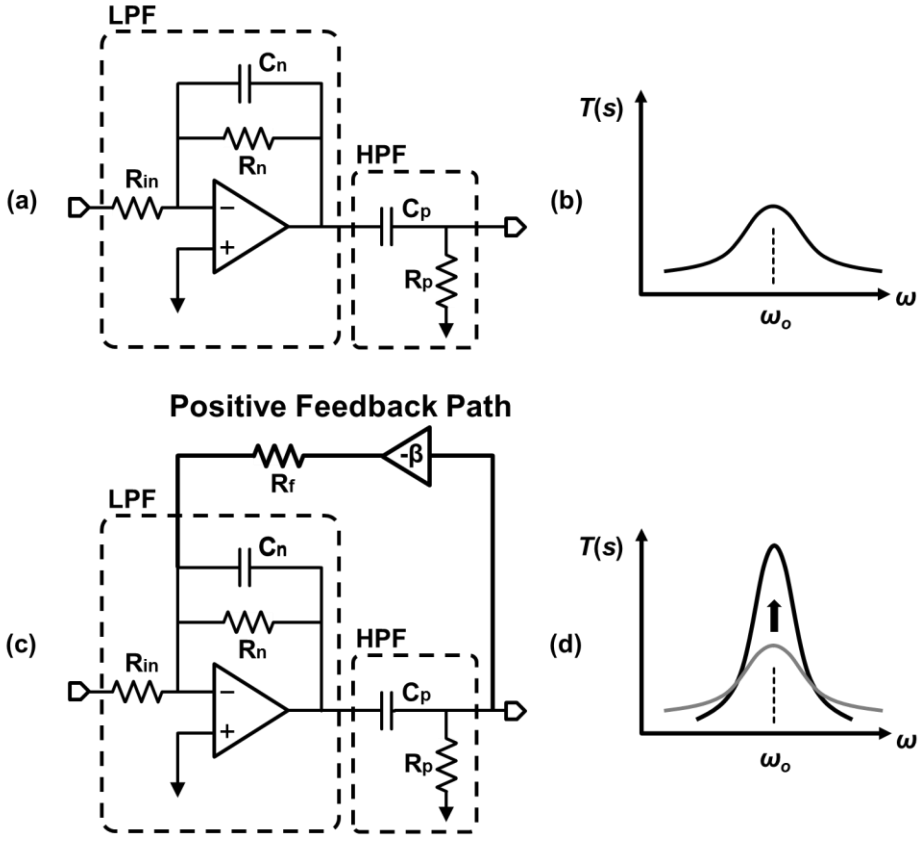


Figure 16. Quality factor enhancement by positive feedback

In this work, by applying positive feedback[70] to a conventional active filter, a high quality-factor resonator is realized with a single amplifier, replacing the LC or bi-quadratic resonators in a conventional CTBPSDM. We begin with the low-quality-factor single-amplifier bandpass filter (BPF) consisting of a lowpass filter (LPF) and a passive highpass filter (HPF) in series shown in Figure 16(a). The transfer function of this BPF is expressed as:

$$T(s) = k_o \frac{\omega_o s}{s^2 + 2\omega_o s + \omega_o} \tag{13}$$

$$\text{where} \quad \omega_o = 1/R_p C_p R_n C_n \tag{14}$$

The first-order term in the denominator decides the quality factor, which is very low for this BPF as in Figure 16(b). To enhance the quality factor we add a positive feedback path (Figure 16(c)) to the BPF. The positive feedback path boosts the low quality-factor BPF output, therefore it resonates around the resonant frequency ω_o while suppressing the out-of-band signals. The positive feedback path results in the transfer function:

$$T(s) = k_o \frac{\omega_o s}{s^2 + 2 \cdot (1 - \beta) \cdot \omega_o s + \omega_o} \tag{15}$$

The quality factor of this filter can be increased to the level required for this modulator depending on the feedback gain β. As β approaches 1, the first-order term in the denominator approaches zero and the quality factor goes to infinity making this filter have the same transfer function as that of an ideal 2nd-order resonator. However, this requires the positive feedback of -1 (=β) and another resistor R_f. The HPF outputs are directly fed back to inputs not to add these components. The gain of -1 can be easily realized in the differential mode, and R_p can replace R_f. R_p is located between the resonator output and the ground while R_p is between the resonator output and the virtual ground node. This similarity enables the replacement and prevents the use of additional resources for the resonator implementation.

A differential mode circuit implementation of the resonator is shown in Figure 17. The feedback gain is fixed to -1, and the resonance condition and quality factor now depend only on passive component values. The transfer function of this circuit is expressed as :

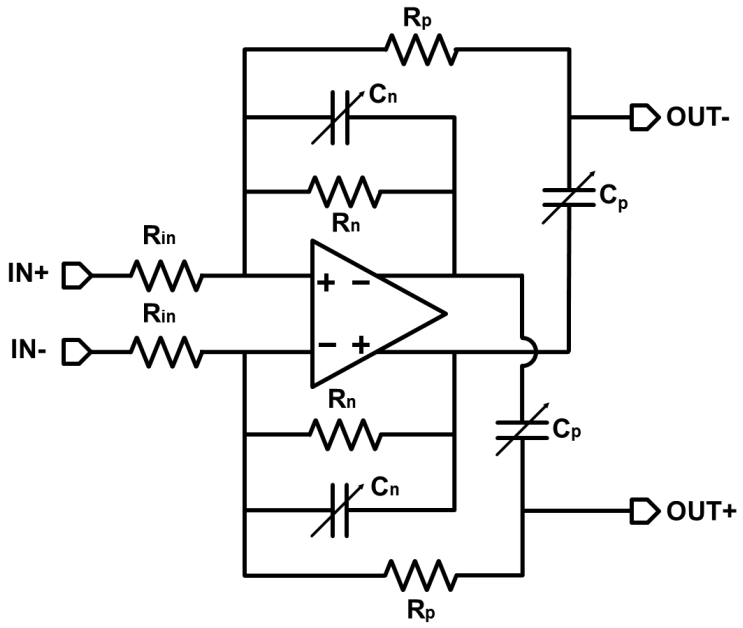


Figure 17. Differential-mode implementation of single op-amp resonator

$$T(s) = k_o \, ' \frac{\omega_o s}{s^2 + 2 \cdot k \cdot \omega_o s + \omega_o} \tag{16}$$

$$\text{where } k = R_n C_n + R_p C_p - R_n C_p \tag{17}$$

$$\omega_o = 1/R_n C_n = 1/R_p C_p \tag{18}$$

The resonance condition of the differential circuit is $k=0$ from (16). There are innumerable solutions for $k=0$, and a solution of $C_p=2C_n$, $R_n=2R_p$ is chosen so that the filter has the best noise performance and the smallest passive area since this solution minimizes the resistors and the capacitors while the resonant frequency is fixed.

The main advantage of this resonator in CTBPDSMs is that it consumes 40% less power compared to the traditional bi-quadratic resonator, which has two amplifiers while keeping the same noise performance. The power and area savings are significant, especially in higher order modulators. The block linearity of this type of resonator may be inferior to a more traditional circuit with negative feedback, but this is significantly mitigated when the resonator is used in a

modulator with a feedforward architecture since the latter reduces the swing where the nonlinearity occurs. That is the case of the modulator presented here.

2.2.1.2 Op-Amp

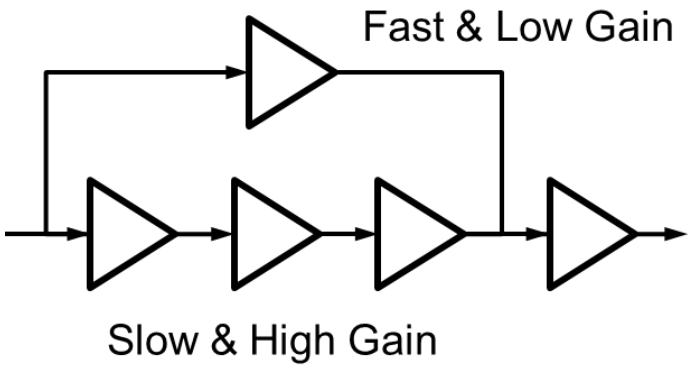


Figure 18. Multi-path amplifier

A high-gain op-amp is required for the resonator to get good linearity and a small error in the resonant frequency. However, it is difficult to use a cascode structure to achieve the required high gain because the supply voltage has become low in advanced CMOS process nodes[71]. A multi-stage amplifier is a good alternative for a continuous-time modulators[72]-[75]. Cascading of individual low gain amplifiers can provide high overall gain and also achieve a sufficient voltage swing even with a low supply voltage. As shown in Figure 18, there are two paths in parallel; one is a high-gain narrow-bandwidth amplification path with four amplifying stages (slow path) while the other is a low-gain high-bandwidth one consisting of a single stage (fast path). The fast path provides the wide bandwidth of the op-amp. At high frequencies, the gain of the fast path, which has a much higher bandwidth than the slow path, dominates because the gain of the slow path falls off at lower frequency. Furthermore, the fast path also helps the stability

compensation. The phase of the fast path dominates the total phase response at high frequency and more phase margin is achieved because this path does not have a cascode structure.

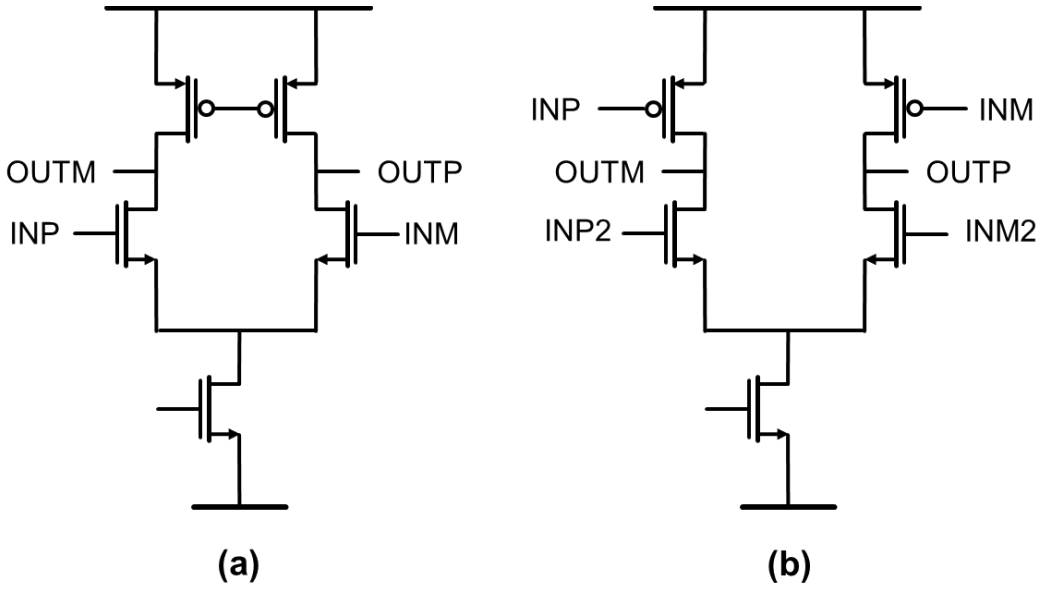


Figure 19. Stage units of the amplifier (a) w/o summing (b) w/ summing

In the multi-stage amplifier described here, each stage is a single common-source amplifier with a current source as the load (Figure 19(a)). Even when the circuit is implemented in a differential manner, there is still a signal headroom of more than half the supply voltage, for a 1.25V supply. The amplifier on the fast path is a single common-source amplifier for fast operation. The technology used in this work is 65nm CMOS, and considering the balance between the speed and the gain, the optimal gain for each stage is estimated to be 15-20dB in simulation. In total, four stages are used to provide enough gain, and the fourth amplifier stage uses a different scheme to sum the fast path and the slow path. As in Figure 19(b), a push-pull structure enables the summing of two paths and each PMOS or NMOS common-source amplifier sees the other as the load. To get a 60 degree phase margin, nested Miller-compensation is used[76]. The total gain and phase margin response of this amplifier is shown in Figure 20. The

DC gain is 73dB and the phase margin is 65 degrees. The gain at 200MHz is 30dB. The total power consumption is 2mW, and half of the power is consumed by the last stage. The first stage consumes one quarter of the total power to achieve a low thermal noise. In addition the input devices are very large for good matching and low input referred noise.

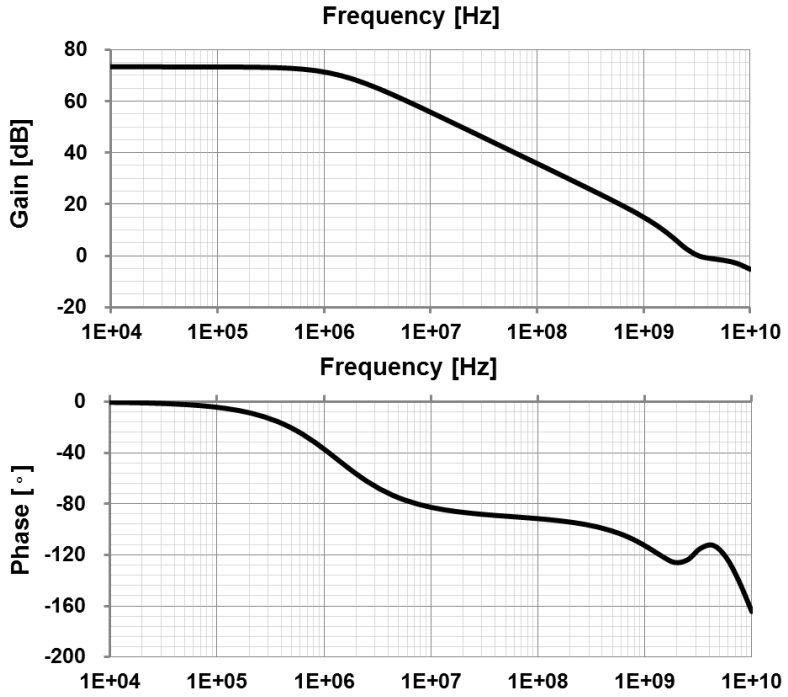


Figure 20. Gain and phase response of the amplifier

2.2.1.3 Center Frequency and Quality Factor Tuning

Both the mismatch of the passive components and process variation change the resonant frequency. The resonant frequency of the resonators decides the center frequency of the CTBPDSM, so calibration is required for the passive components to get the exact center frequency. Calibration of the capacitors R_p and R_n in the positive and negative feedbacks in Figure 17 enables the calibration of both the center frequency and quality factor. Calibrating only capacitors is enough to correctly set the center frequency. Digitally controlled capacitor

banks[65] are placed in parallel with the main capacitors in Figure 21. The quality factor of this resonator is also related to the capacitances since they decides the first order coefficient in the numerator, therefore fine tuning of the capacitance is required to have a good control on the quality factor. 4bit capacitor banks are used for each capacitor. It is clear that the capacitances are inversely proportional to the center frequency ω_o in (18). And from (17), C_p is proportional to the quality factor while C_n is the opposite. So the change of each capacitor affects both the center frequency and the quality factor as in Figure 22.

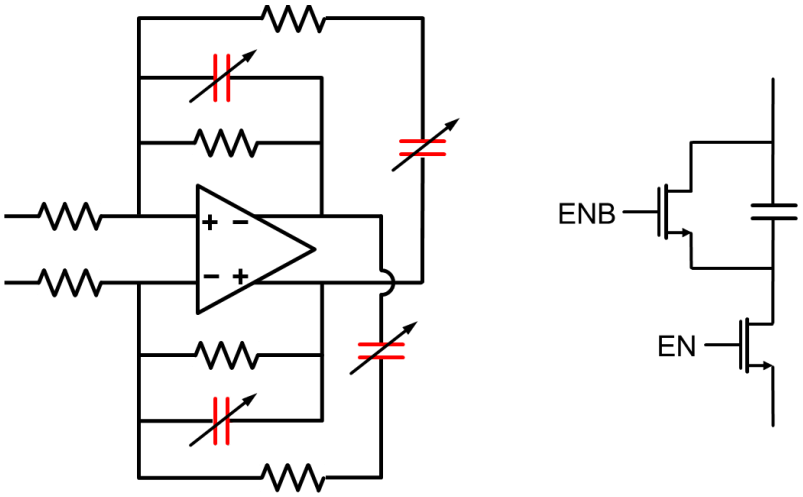


Figure 21. Resonator RC tuning with capacitor banks

The center frequency has to be accurate while the quality factor just needs to be above a certain threshold. So the center frequency is calibrated first, and then the quality factor is adjusted by the two capacitors keeping the same center frequency. A quality factor of 20 is sufficient for the target modulator performance and is used in test, even though a higher Q can be achieved.

And due to the mismatch and process variation or depending on the calibration activity, (17) can have a negative value. This means that the resonator becomes unstable, but this does not lead

to the instability of the modulator because the feedback loop of the delta-sigma modulator cancels out the resonating signal. Therefore, this resonator is robust in the delta-sigma modulator regardless of the calibration accuracy of the quality factor, but has to have a sophisticated calibration method in other systems without the feedback loop.

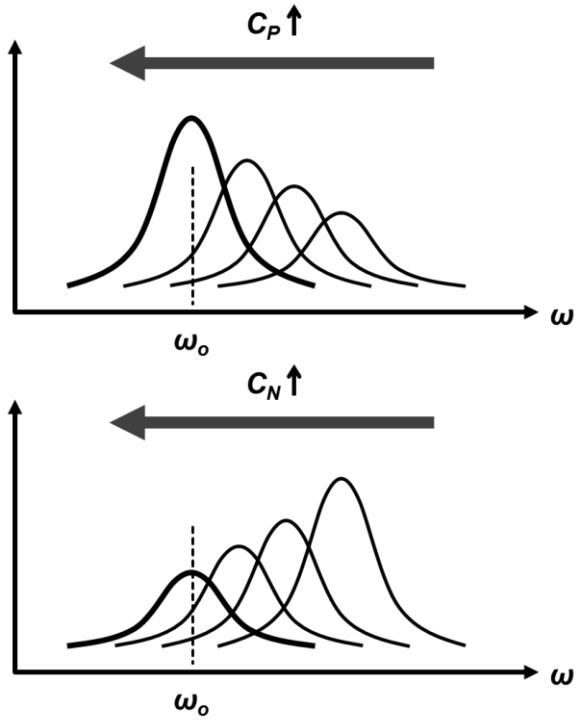


Figure 22. Quality factor and center frequency tuning

2.2.1.4 Resonator Outputs

Although the original resonator outputs are *OUT+'* and *OUT-'* in Figure 17 an alternative configuration gives more flexibility and reduces kickback. When this resonator feeds a block with resistive inputs, the time constant of the feedback paths changes and this also changes the resonant frequency and the quality factor. In Figure 23 the amplifier outputs *OUT+* and *OUT-* directly feed the next block through another RC HPF formed by R_p' and C_p'. This HPF does not

affect the feedback around the amplifier and enables the connection with any other blocks with resistive inputs in CTBPDSMs.

The time constant of this HPF is the same as R_pC_p. This helps reduce kickback and improve flexibility. Kickback from other blocks can be injected to the inputs through the resistor in the original configuration, but the new configuration suppresses it with the help of the HPF. An advantage is that here, R_p' which is bigger than R_p is used to reduce the amplifier's load without affecting the total noise performance. Furthermore, these capacitors are not calibrated since they barely change the resonance characteristic of the feedback loops.

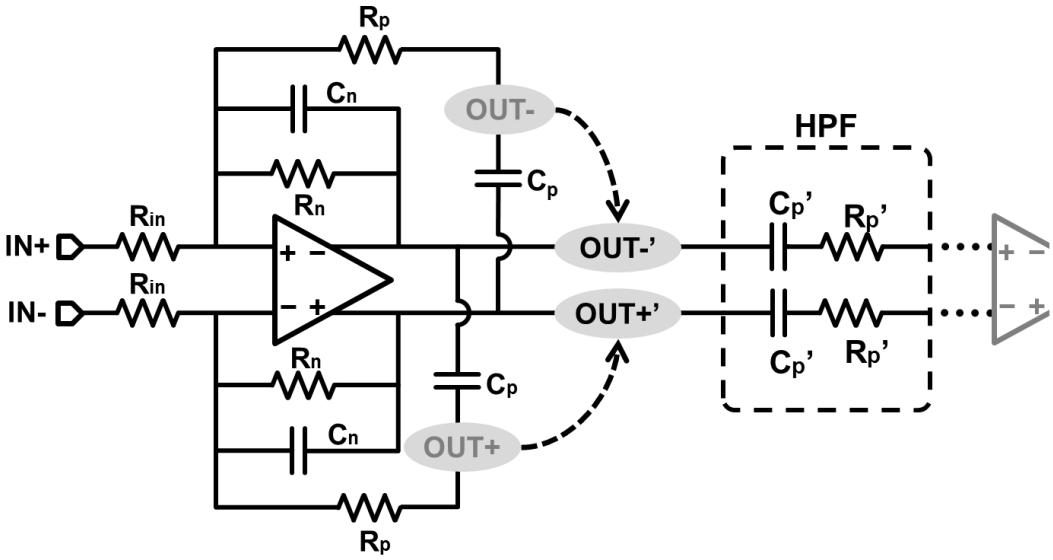


Figure 23. Output node change

2.2.2 Current-steering DAC

2.2.2.1 Current Sources

The current-steering DAC is connected to the virtual ground nodes of the resonator, so the output impedance of the DAC has to be very high for good linearity[77]. The triple cascode

structure in Figure 24 provides high output impedance and isolates the current source at the bottom from the switches. Without this isolation, the current source is affected by switching noise and generates a data dependent current output instead of constant one, which causes nonlinearity.

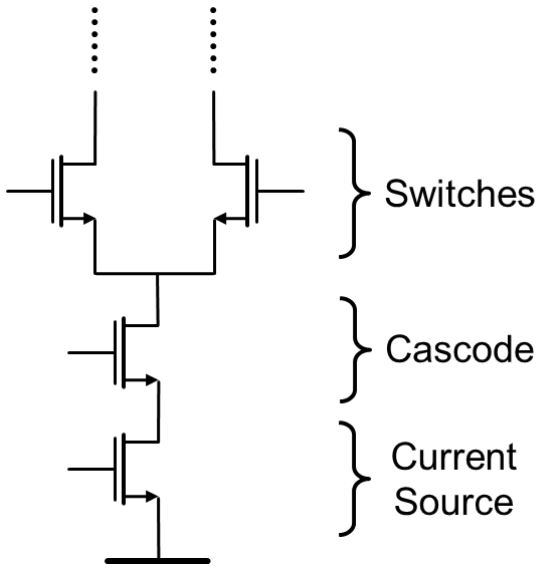


Figure 24. Triple cascode structure for DAC

The thermal noise from the current source is directly injected to the resonator. Due to the switching, the differential mode implementation does not cancel the thermal noise. The thermal noise from the current source in *DAC1* significantly contributes to the total noise[78], thus it has to be minimized so as not to limit the maximum SNDR. On the other hand, flicker noise is filtered by the resonator, so can be ignored. By increasing the overdrive voltage of the current source, the thermal noise can be reduced. However, the headroom for the triple cascode structure is not enough for strong overdrive with a 1.25V supply voltage, and so a certain amount of noise being fed into the modulator is inevitable. In this work, the total voltage headroom for the triple cascode is 750mV and 400mV out of this is assigned to the current source.

The device size is also important for the linearity. Mismatch between the current sources can modulate the output current and introduce nonlinearity, regardless of the resonator performance[79][80]. Dynamic element matching (DEM) can cancel this nonlinearity by shuffling the mismatch, but DEM is complex and increases the power consumption. Here, the target SNDR is met by increasing the device sizes and achieving sufficient matching by design. By using very large devices for the current sources while maintaining the *W/L* ratio, the mismatch is minimized. Monte-Carlo simulations indicate a 0.2% mismatch, which is sufficient for the target performance.

The current source of *DAC2* does not need to be as large as that of *DAC1*. Any nonlinearity caused after the *Resonator1* barely appears at the output. The same is true for the thermal noise, and a large overdrive is not necessary in *DAC2*.

2.2.2.2 DAC Switches

The switching devices change the current direction to the resonator, so they are sized as small as possible for fast switching. This is also helpful in reducing the clock injection to the resonator by decreasing the parasitic capacitance. Also, small switch size reduces the parasitic capacitance at the interface with the resonator, which can affect the feedback gain of the amplifier. The voltage headroom is slightly larger than V_{DSAT} to give more overdrive to the current source while keeping the switching devices in saturation. With a gate voltage of 900mV, the switching device is turned on and fully saturated, which gives the maximum output impedance. The two switching devices are completely symmetric in the layout since any mismatch can cause nonlinearity[82]. The cascode device is also sized small for fast operation.

2.2.2.3 DAC Latch

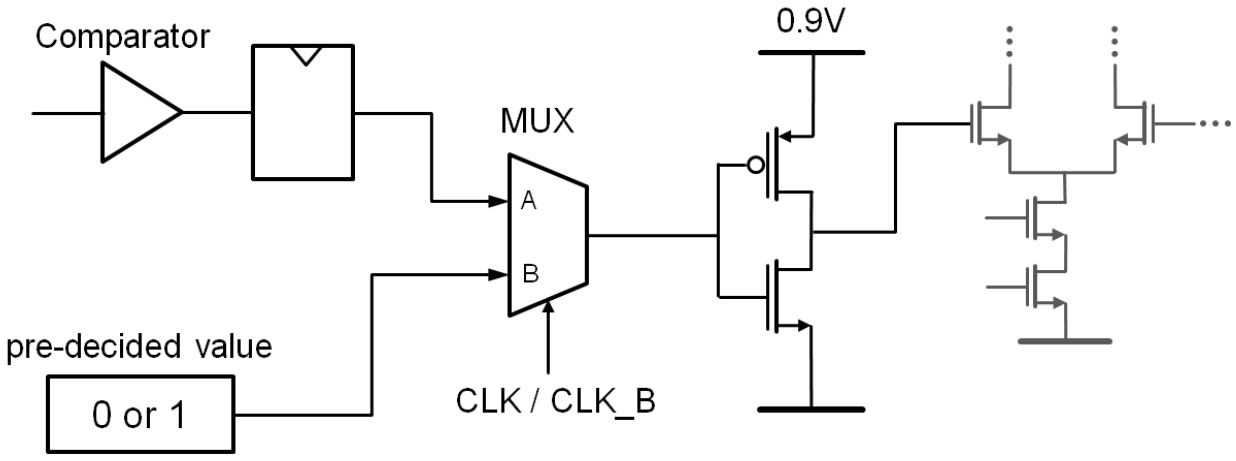


Figure 25. Return-to-zero pulse DAC latch

Both the RZ DAC and HZ DAC require a return-to-zero pulse, and both the outputs are zero for half of the clock period. We use an even number of current sources to implement this pulse. The differential-mode current output of the DAC is zero when the same amount of current flows on both sides of the output. There are total eight current sources, and four current sources are directed to each of the differential outputs when the overall differential output returns to zero. Figure 25 shows the bitwise implementation, which is one side of the differential implementation. The mux has two inputs; the comparator output from the quantizer and the pre-decided value *'0'* or *'1'* that refers the current direction since *'1'* turns on the switch and *'0'* turns off the switch. Four of the eight DAC latches have a pre-decided value of *'0'*, and the others have *'1'*. The clock controls the mux output, and therefore the mux passes the comparator output for half a clock period and passes the pre-decided value for the other half clock period. While the mux outputs are at the pre-decided values, the current flow on both sides of the DAC output is equal, and this becomes the return-to-zero phase. The mux output drives an inverter which controls the switching devices coming after the inverter. The inverter is supplied with 900mV. The switches

are intended to be in saturation and go into the linear region if the gate voltage goes higher than 900mV. The use of the dedicated supply voltage also helps to set the exact switching timing. If the supply rail becomes noisy because of other digital blocks, the transition timing changes and this is considered as a kind of clock jitter noise[83].

2.2.3 Quantizer

2.2.3.1 Comparator

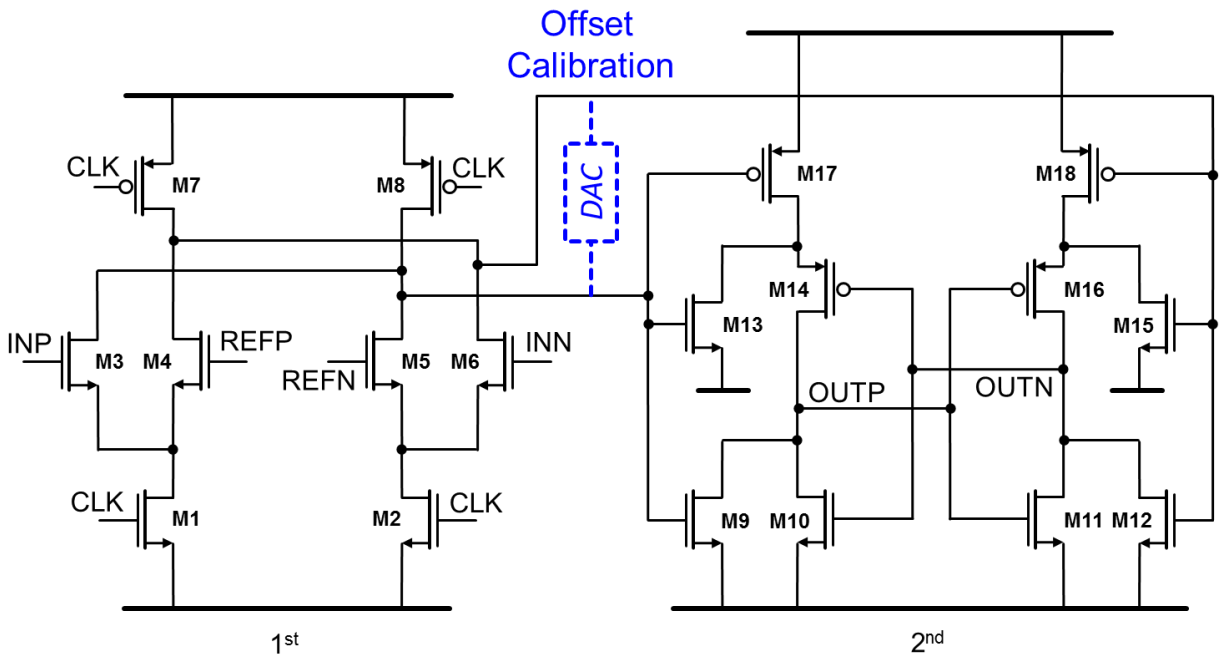


Figure 26. Comparator of the flash ADC

The quantizer is a flash ADC with 8 comparators and generates a 9-level digital output. The comparator is shown in Figure 26, and consists of two stages[81]. When the clock is low, *M1-2* are off and *M7-8* reset the first stage outputs to high. These first stage outputs also reset the nodes in the second stage, and the comparator outputs go low. When the clock goes high, *M7-8* are turned off and *M1-2* discharge the first stage output nodes. The discharge speed differs for

both sides depending on the input and reference voltages, and this makes the output voltage different. As both of the first stage outputs go low with a small voltage difference between them, *M17-18* are turned on and *M9*, *M12* are turned off. This makes the second stage a back-to-back latch, and the small voltage difference from the first stage is regenerated by this latch. The comparator outputs are valid only for half a clock period, so there is an SR latch after the comparator to hold the value for the rest half clock period.

2.2.3.2 Input Offset Calibration

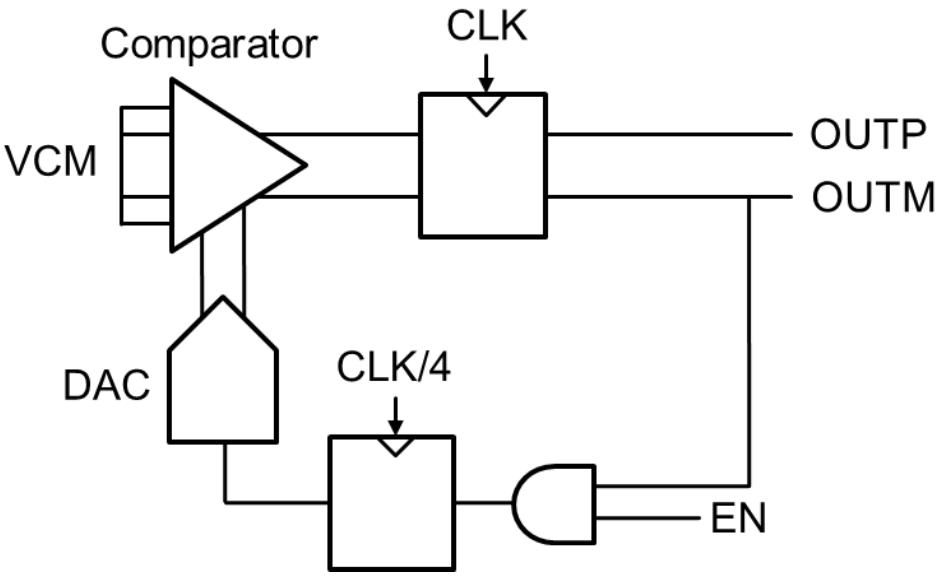


Figure 27. Comparator input offset calibration

M3 and *M6* in Figure 26 are sized minimum to reduce the load of the summing amplifier which drives this quantizer. Large input devices are good for matching and reduce the input offset of the comparator[84], but the summing amplifier has to drive 8 comparators. A big load causes a pole at the output of the summing amplifier and this limits the bandwidth[85]. For this reason, minimum size input devices are used for fast operation, but this causes a large input offset, even with careful layout. An auxiliary current-mode DAC[65] is assigned to each

comparator to calibrate the input offset. This 4bit DAC is between the first stage outputs, and sinks a different amount of current from both sides. Figure 27 shows how this DAC cancels the input offset. During the startup, all inputs and references are tied together and the digital logic slowly varies the DAC current and finds the current value which flips the comparator output. The input offset is compensated by keeping this auxiliary DAC current fixed at this value during normal operation.

2.2.3.3 Clock Delay Controller

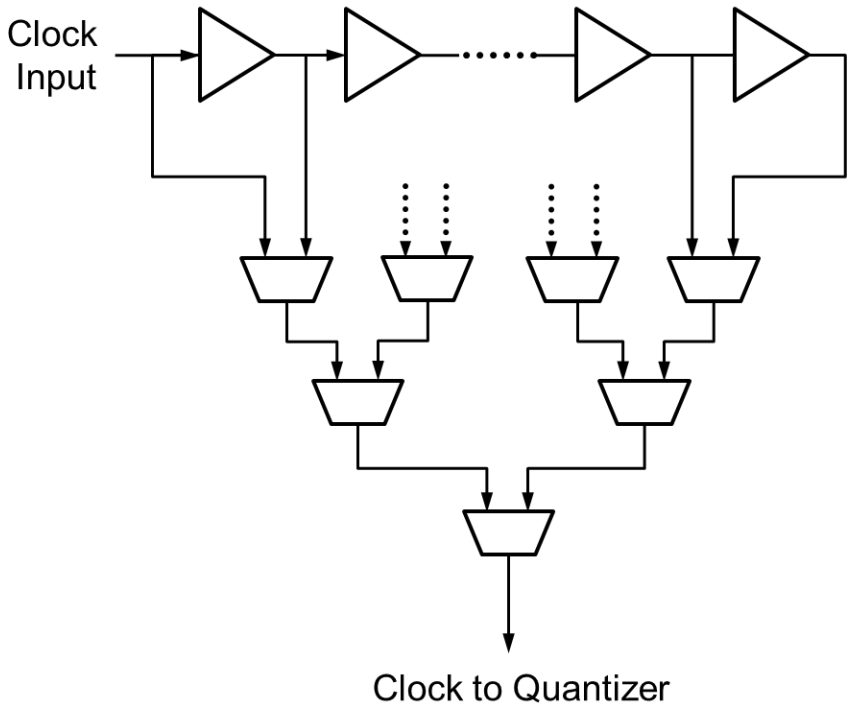


Figure 28. Clock delay controller

The clock generator has to feed the DACs as well as the quantizer. However, there is a clock path mismatch between these blocks, and more timing difference is caused because the clock receiving devices have different sizes. Also, the summing amplifier is not ideal and causes a slight delay. A clock delay controller compensates all of these mismatches and aligns the

sampling and the current triggering. The clock delay controller in Figure 28 is placed between the clock generator and the quantizer, and consists of a series of buffers and muxes. Each buffer is two inverters in series, and makes a delay of approximately 30ps. The mux selects one of the delayed clocks and sends it to the quantizer. The total tuning range is 210ps with 7 buffers. This block is controlled manually from off-chip. Tuning is based on the measured power spectral density of this modulator. The difference in the clock timing shows up as a noise peak in the power spectral density as in Figure 29.

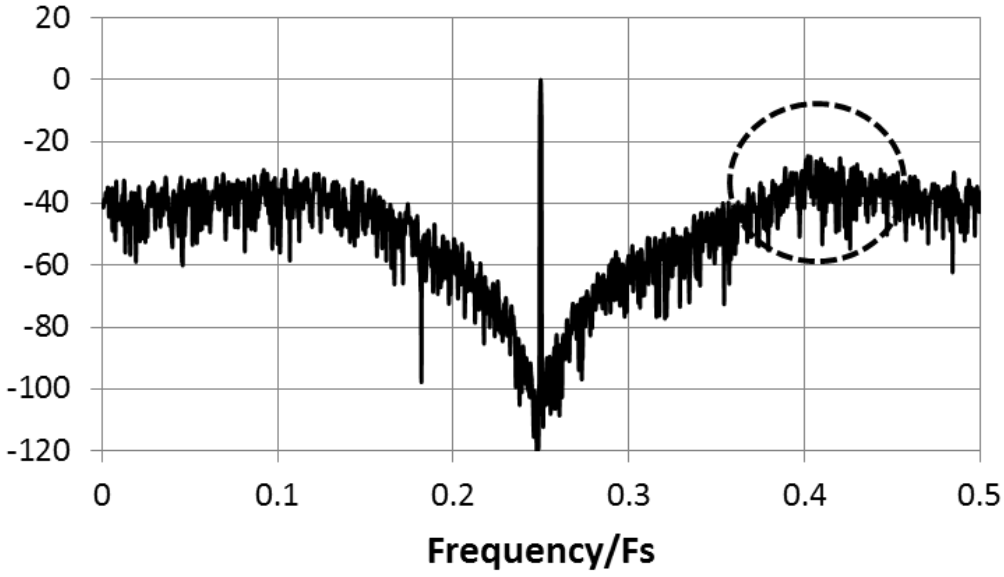


Figure 29. Effect of clock path mismatch

2.2.4 Summing Amplifier

A summing amplifier is necessary before the quantizer to sum the second resonator output and the feedforward paths. Nonlinearity or thermal noise added at this position hardly affects the modulator performance, so the op-amp can have very simple design. A multi-stage amplifier is also used, but without a feedforward path. The amplifier has three stages and no feedforward

path, and Miller-compensation is used. Miller-compensation is sufficient for this three-stage amplifier because the third stage is low gain high swing stage. The open-loop gain of this amplifier is 120, and the phase margin is 50 degree. Resistive feedback is applied to achieve a gain of 1, and the HPF at the output of the resonator is connected to the virtual ground nodes. Large resistors are used for low power consumption, since the thermal noise from these resistors is not significant.

2.2.5 System Implementation

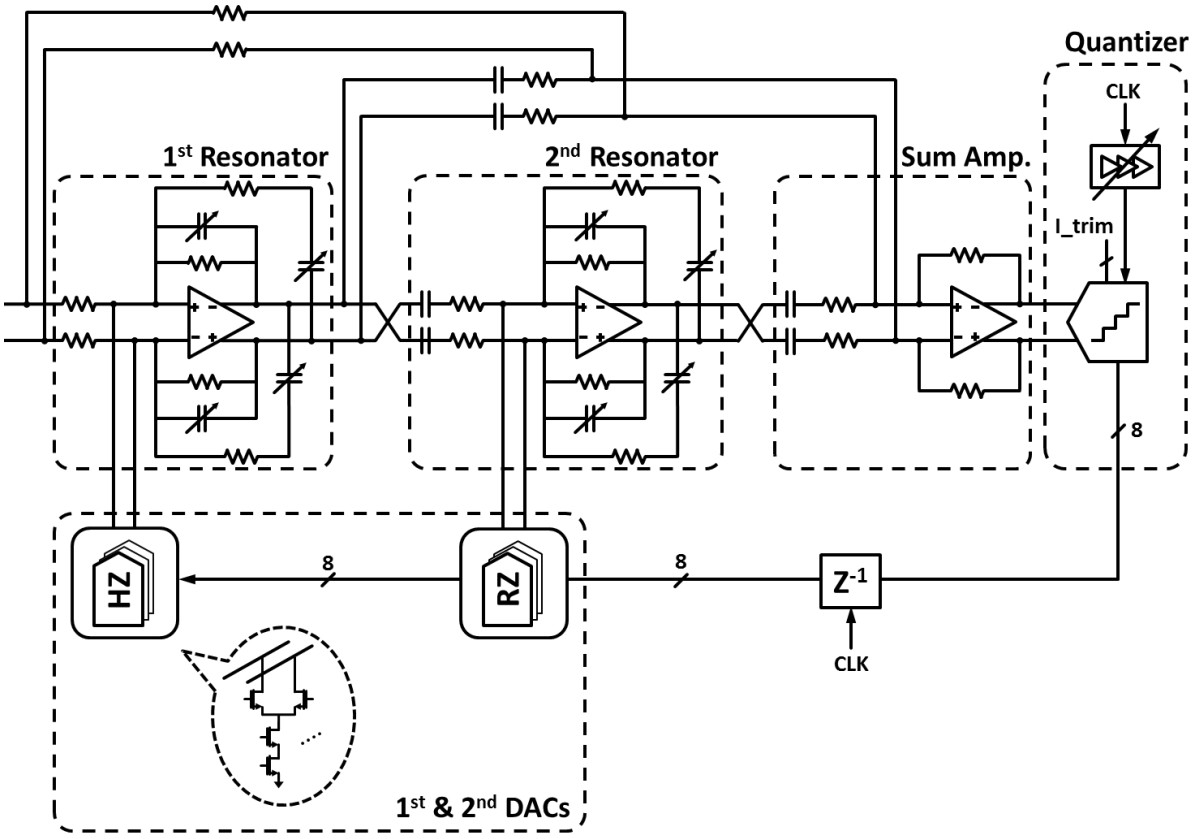


Figure 30. System implementation

Figure 30 shows the circuit implementation of the core loop. The first resonator drives the second resonator through an HPF, and the second resonator drives the summing amplifier in the

same way. There are two feedforward paths, and they also consist of HPFs due to the characteristic of the resonator. The current-mode DAC outputs are connected to the virtual ground nodes of the amplifiers. The extra delay coming from the resonators and the summing amplifier is also compensated by the clock delay controller connected to the quantizer.

2.3 Prototype Test Results

The prototype[86] is fabricated in 65nm CMOS with 9 metal layers and the active die area is $0.2mm^2$. Figure 31 shows the die micrograph. The two resonators take the most of the area due to the passive components. The first DAC occupies most of the DAC block area since the current sources are very large. A 48-pin QFN package is used for this test.

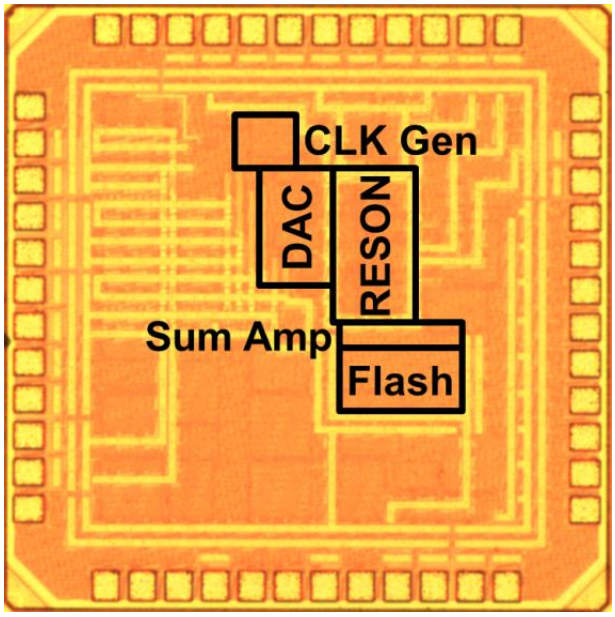


Figure 31. Die micrograph of the prototype

2.3.1 Power Spectral Density

Figure 32 shows the measured power spectral density of this modulator output. The top-left graph shows the entire spectrum from DC to $F_s/2$. And the main graph is in-band spectrum over a 24MHz bandwidth. A 200MHz tone with -3.9dBFS amplitude is used as an input, and the measured SNDR of 58dB while operating with 1.25V supply. The third harmonic is next to the fundamental tone because it is folded down from higher frequency. The third harmonic is mainly caused by the amplifier and the DAC nonlinearity, but it is comparable to the in-band noise and does not reduce the SNDR.

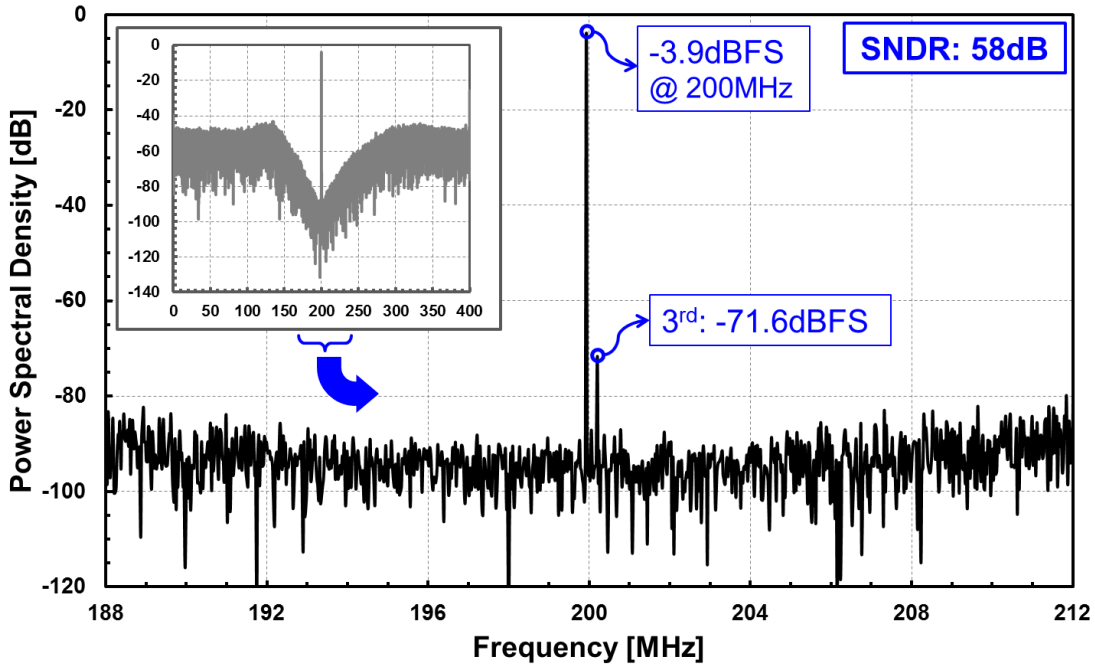


Figure 32. Power spectral density

2.3.2 Dynamic Range

The dynamic range is also tested with a 200MHz tone, and the minimum detectable signal amplitude is -63.9dBFS. The input amplitude showing the maximum SNDR is -3.9dBFS, and the

dynamic range of this modulator is 60dB as in Figure 33. The dynamic range is limited by the thermal noise from the first resonator and the first DAC.

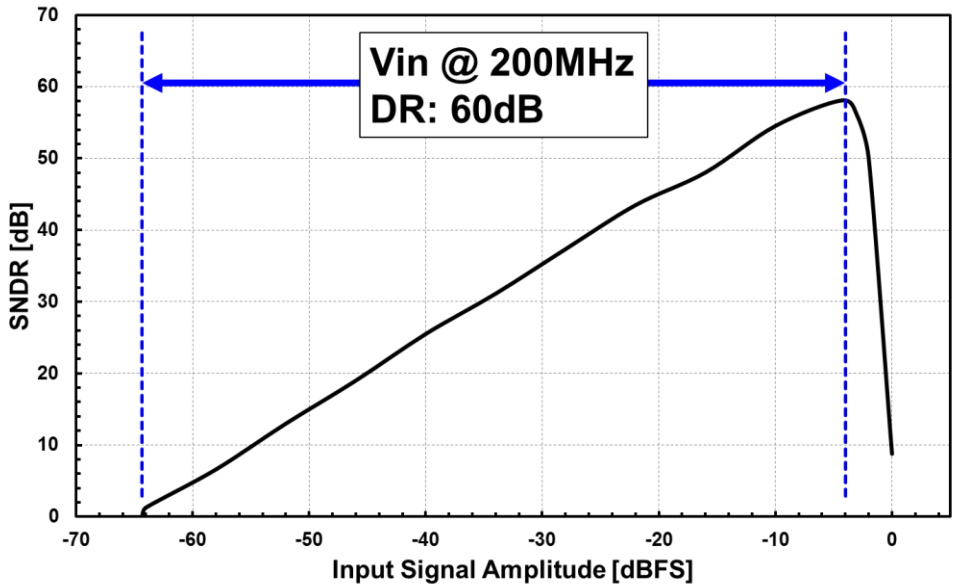


Figure 33. Dynamic range

2.3.3 Two-tone Test

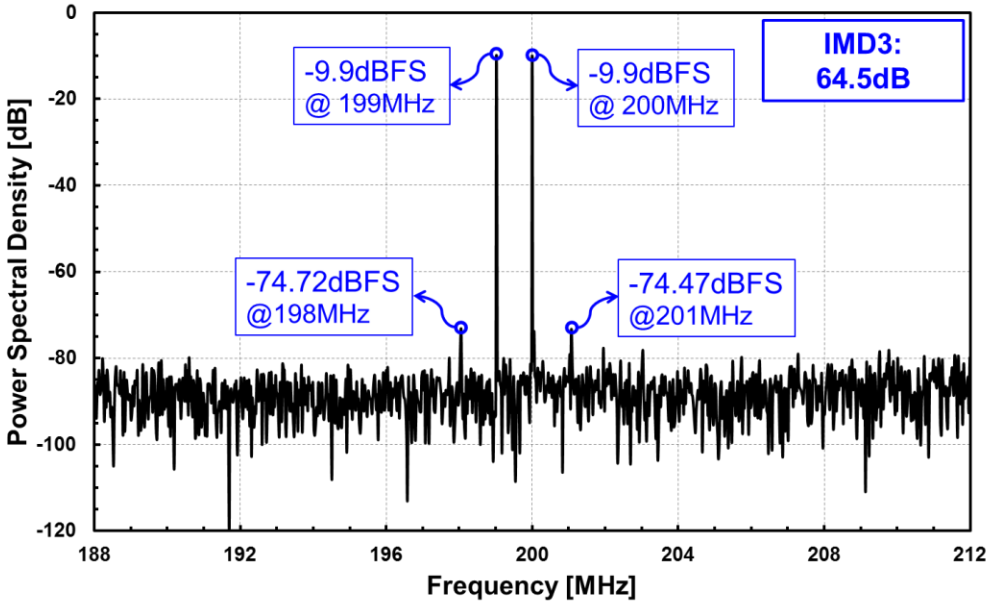


Figure 34. Power spectral density with two-tone inputs

A two-tone test is done with two tones 1MHz apart, and amplitudes are -9.9dBFS. In Figure 34, the inter-modulated tones are -74.72dBFS and -74.47dBFS, and this indicates a modulator IM3 of 65dB.

2.3.4 Power Consumption

Table 1. Supply voltage and power consumption by blocks

Analog	1.25V	5mW
Digital	1V	4mW
Clock Gen	1V	2mW
DAC Driver	0.9V	1mW
Total		**12mW**

The total power consumption including that of the clock generator is 12mW. Table 1 shows the power consumption of each block. The analog part, including the resonators, the DAC current sources and the summing amplifier, consumes 5mW. A 1.25V supply voltage is used to ensure headroom for the triple cascode structure of the DAC current source. The first resonator consumes 2mW, and the second resonator consumes 1.5mW. The two DACs consume 1mW, and the summing amplifier consumes 0.5mW. The digital part consists of the quantizer and the DAC latch. The DAC latch consumes most of the digital power due to the switching, and the calibration circuits do not consume any power during normal operation. The DAC driver uses 0.9V supply voltage, and consumes 1mW. The clock generator includes the clock delay controller, and consumes 2mW. Figure 35 compares the power consumption of the different blocks in a pie graph.

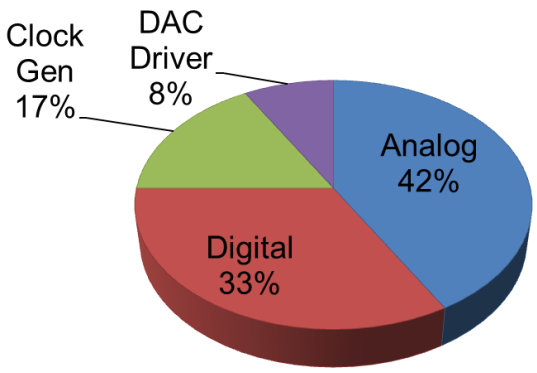


Figure 35. Power consumption details

2.3.5 Performance Summary and State of the Arts

Table 2 shows a performance summary of this prototype. The sampling rate is 800MHz, and the center frequency is 200MHz, which is the quarter of the sampling frequency. The FoM is 385fJ/conversion which to our knowledge is the best for CTBPDSMs using active resonators.

Table 3 compares this work with the state-of-the-art.

Table 2. Performance summary

Sampling Rate	800MHz
Center Frequency	200MHz
BW	24MHz
Power	12mW
SNDR	58dB
DR	60dB
IMD3	64.5dB
Area	0.2mm^2
FoM	385fJ/conv

Table 3. State of the arts

Author	Schreier	Thandri	Chalvatzis	Ryckaert	Lu	This work
Publication	JSSC 2006	JSSC 2007	JSSC 2007	JSSC 2009	JSSC 2010	
Order	4^{th}	4^{th}	4^{th}	6^{th}	6^{th}	4^{th}
Resonator	active-RC	LC	LC	LC	active-RC	new RC
DR [dB]	90	65	53		70	60
F_s [MHz]	264	3800	40000	3000	800	800
F_c [MHz]	44	950	2000	2400	200	200
BW [MHz]	8.5	0.2/1	60/120	60	10	24
SNDR [dB]			55/52	40	68.4	58
SNR [dB]	77	63/59				
Power [mW]	375	75	1600	40	160	12
Area [mm^2]	2.5	1.08	2.4	0.8	2.5	0.2
Process	0.18 CMOS	0.25 BiCMOS	0.13 BiCMOS	0.09 CMOS	0.18 CMOS	0.065 CMOS
FoM [pJ/step]	3.81	162/51	29/20	4.08	3.72	0.385

* $FoM = Power/(2 \cdot BW \cdot 2^{ENOB})$, $ENOB = (SNDR - 1.76)/6.02$

Chapter 3. CTBPDSM with DAC Duty Cycle Control

The first prototype achieves good power efficiency, but the SNDR and dynamic range are not enough for practical SDR. Considering that a higher resolution and a wide bandwidth, such as 12bit resolution at 24MHz, is required in mobile environments[91], the first prototype can achieve 2 more bits by increasing the modulation order or the quantizer resolution. Also, the first resonator and the first DAC need to have lower in-band thermal noise to reduce the noise floor and improve SNDR.

Bandpass filtering of the input signal also makes CTBPDSMs more suitable for SDR since this filtering suppresses interferers and prevents saturation of the modulator [92]-[95]. Furthermore, filtering helps to increase the dynamic range. The STF of the first prototype is almost flat due to the feedforward paths, and a modification of this architecture adds a bandpass characteristic to the STF. To keep the power consumption low, another new technique reduces the number of feedback DACs.

We introduce a 6^{th}-order CTBPDSM architecture with 4bit quantization in this chapter. This device has better resolution than the first prototype and also provides bandpass filtering of the input signal. This new architecture has total two DACs thanks to DAC duty cycle control. With the help of a new duty-cycle-controlled feedback DAC scheme, we can make an architecture that is both simple and reconfigurable. A single, duty-cycle-controlled DAC replaces the conventional combination of RZ and HZ DACs that usually feed each resonator. This new scheme does not rely on feedforward paths to eliminate feedback DACs, and importantly this enables input signal filtering without peaking in the STF. Also, the duty-cycle controlled DAC enables the center frequency to be easily reconfigurable.

Table 4. Target spec of the new prototype

Sampling Rate	800MHz
Center Frequency	200MHz
BW	24MHz
Power	40mW
SNDR	75dB
DR	80dB

Table 4 shows the new target specifications. The target SNDR and dynamic range are 75dB and 80dB, respectively. The amplifiers and the DAC current sources are newly designed for lower thermal noise and the better linearity to achieve the target performance. Other peripheral circuits are also modified appropriately. Although it introduces reconfigurability and STF filtering, the prototype achieves the best energy efficiency of any CTBPDSM using active resonators.

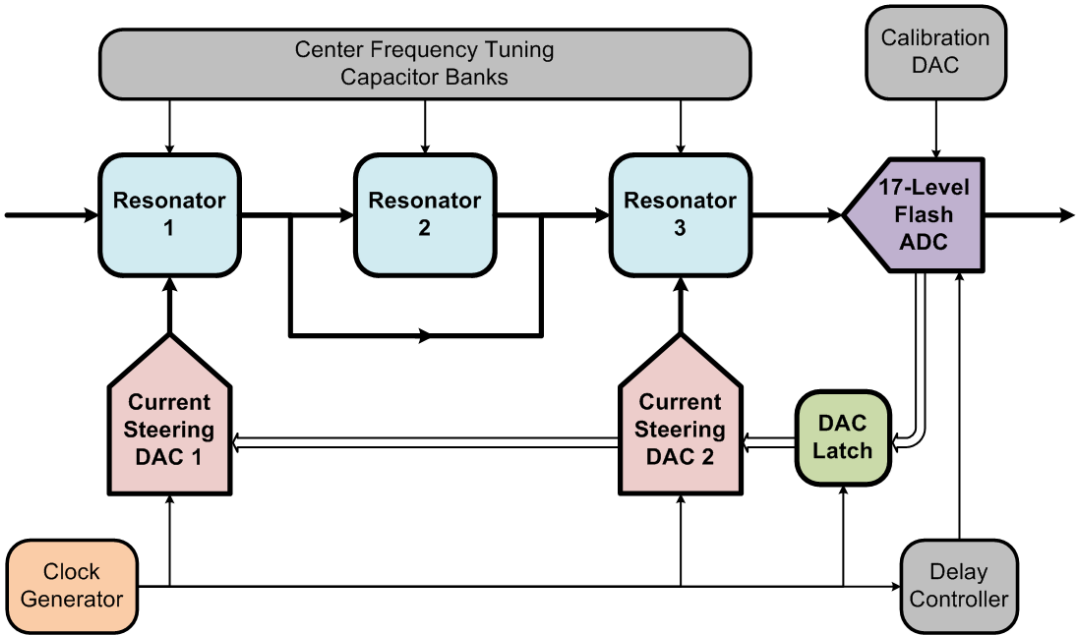


Figure 36. System block diagram

3.1 New Architecture

The 6th-order CTBPDSM architecture in Figure 36 has three resonators, and there is no summing amplifier. Single-opamp resonators are used for low power consumption. The two DACs are connected to *Resonator1* and *Resonator3*, and one feedforward path exists between the *Resonator1* output and the *Resonator3* input for low power. The quantizer is expanded to a 17-level flash ADC, and this, together with the 6th-order modulation, increases the SNDR. The feedforward path from the input is removed, and *Resonator3* drives the quantizer directly. The absence of the feedforward path in front of the quantizer helps the bandpass filtering.

The two DACs are not RZ DACs, but change the current direction depending on the preset duty cycle. This makes one DAC look like two DACs, and this helps to further reduce the total number of DACs in this modulator.

The simulation results with this architecture show 75dB SNDR with the STF peaking minimized. The maximum SNDR with 6th-order modulation and 4bit quantization is higher than this, but it causes STF peaking when there is a feedforward path in the modulator. The degrade in the SNDR can lead to the STF with the minimum peaking, and this still satisfies the original target SNDR.

3.2 Frequency Tuning

A flexible modulator center frequency[96] requires adjustment of both the feedback and/or feedforward coefficients, as well as modification of the resonant frequency of resonators. [58] transforms a DTBPDSM to a CTBPDSM with RZ and HZ DACs. This transformation is not

limited to the condition that the center frequency F_c is $F_s/4$, and can be used for the transformation of DTBPDSMs with any F_c between DC and $F_s/2$. If the resonator is tunable then from analysis of the loop impulse response, the modulator can operate with any F_c by changing the amplitudes of the RZ and HZ pulses (Figure 37). Different combinations of RZ and HZ DAC amplitudes (a_1,b_1) and (a_2,b_2) enable different center frequencies, F_{c1} and F_{c2} since they lead to the appropriate sampled loop impulse response required for different values of F_c.

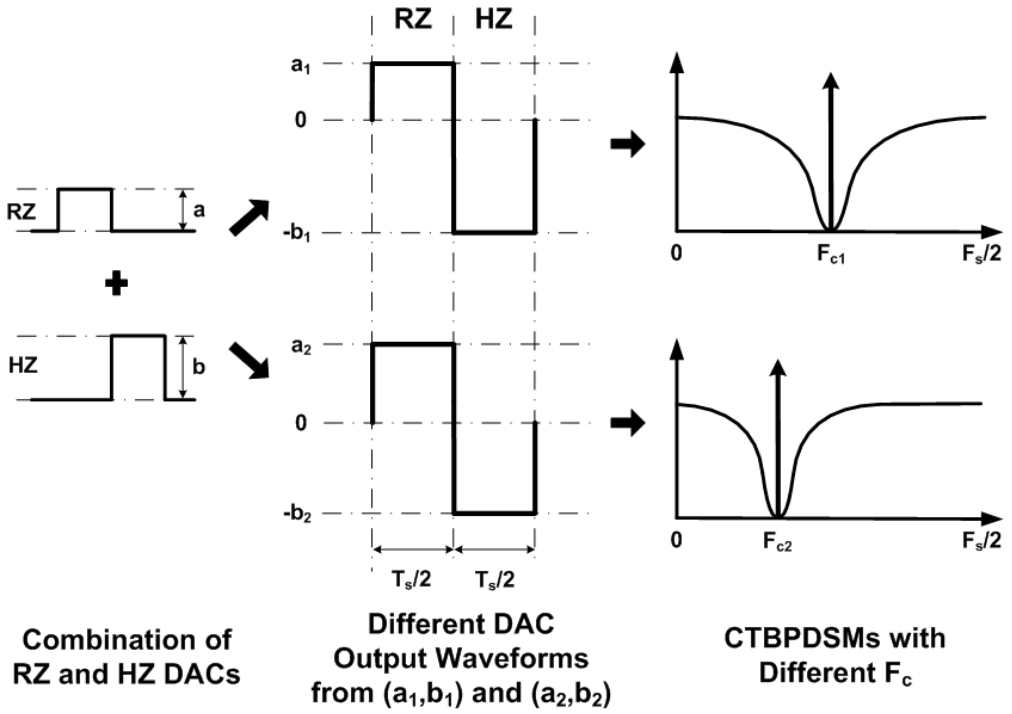


Figure 37. Center frequency tuning with RZ and HZ DACs

The general expression for the 2nd-order loop transfer function of a DTBPDSM is

$$\frac{-2\cos\theta z^{-1} + z^{-2}}{1 - 2\cos\theta z^{-1} + z^{-2}} \tag{19}$$

θ is the center frequency location with regard to the sampling frequency ($360°$) and when $\theta = 90°$, the center frequency is at the quarter of the sampling frequency and the loop transfer function becomes:

$$\frac{z^{-2}}{1+z^{-2}} \tag{20}$$

A CTBPDSM can be designed by making the loop transfer function of the CTBPDSM, sampled at every T_s the same as that of the DTBPDSM as in [58]. And this method can be applied generally regardless of the center frequency location.

The transfer function of a resonator is expressed as:

$$\frac{\omega_c s}{s^2+\omega_c^2} \tag{21}$$

$$\omega_c = 2\pi f_c = 2\pi/T_c \tag{22}$$

The RZ DAC and the HZ DAC have the transfer functions of:

$$\frac{1-e^{-sT_s/2}}{s} \tag{23}$$

$$\frac{e^{-sT_s/2}\,(1-e^{-sT_s/2})}{s} \tag{24}$$

The loop transfer function is the product of the transfer functions of the resonator and the DAC. The two loop transfer functions with the two kinds of DACs are expressed as:

$$\frac{\omega_c(1-e^{-sT_s/2})}{s^2+\omega_c^2} \tag{25}$$

$$\frac{\omega_c e^{-sT_s/2}\,(1-e^{-sT_s/2})}{s^2+\omega_c^2} \tag{26}$$

The loop impulse response for the case with the RZ DAC is

$$sin(\omega_c t) + sin(\omega_c(t - T_s/2))u(t - T_s/2) \tag{27}$$

where *u(t)* is a unit step function.

By sampling this impulse response with the sampling period of T_s, we get

$$sin(\omega_c n T_s) - sin\left(\omega_c\left(nT_s - \frac{T_s}{2}\right)\right)u\left(nT_s - \frac{T_s}{2}\right), n = 0, 1, 2, \ldots \tag{28}$$

The z-transform with this discrete-time impulse response gives

$$\frac{(sin(\omega_c T_s) - sin\,(\omega_c T_s/2))\,z^{-1} - sin(\omega_c T_s/2)\,z^{-2}}{1 - 2\,cos(\omega_c T_s)\,z^{-1} + z^{-2}} \tag{29}$$

Another loop impulse response with the HZ DAC can be written in the same method and it is

$$\frac{sin(\omega_c T_s/2)z^{-1} + (sin\,(\omega_c T_s/2) - sin\,(\omega_c T_s))\,z^{-2}}{1 - 2\,cos(\omega_c T_s)\,z^{-1} + z^{-2}} \tag{30}$$

A linear combination of the two discrete-time transfer functions, (29) and (30) can result in (19), and this completes the transformation of the DTBPDSM to the CTBPDSM with an arbitrary center frequency. The only variables here are the amplitudes of the two kinds of DACs, and the resonator frequency should be changed as well.

Therefore, reconfiguration of F_c is achieved by adjusting the RZ and HZ DAC currents but conventionally this requires both RZ and HZ DACs.

3.3 Duty Cycle Control

A problem with the conventional approach to frequency reconfiguration in 3.2 is that it requires both an RZ and an HZ feedback DAC for each resonator. This prevents the use of the new architecture in 2.1.2 that halves the number of feedback DACs. That architecture requires

only one feedback DAC per resonator thereby significantly reducing power consumption, thermal noise and silicon area. However, the scheme in 2.1.2 requires a feedforward path to remove one DAC and this has the disadvantage of causing STF peaking. Furthermore, reconfiguration of F_c is not possible because the approximation made to remove another feedback DAC is only valid for $F_c = F_s/4$.

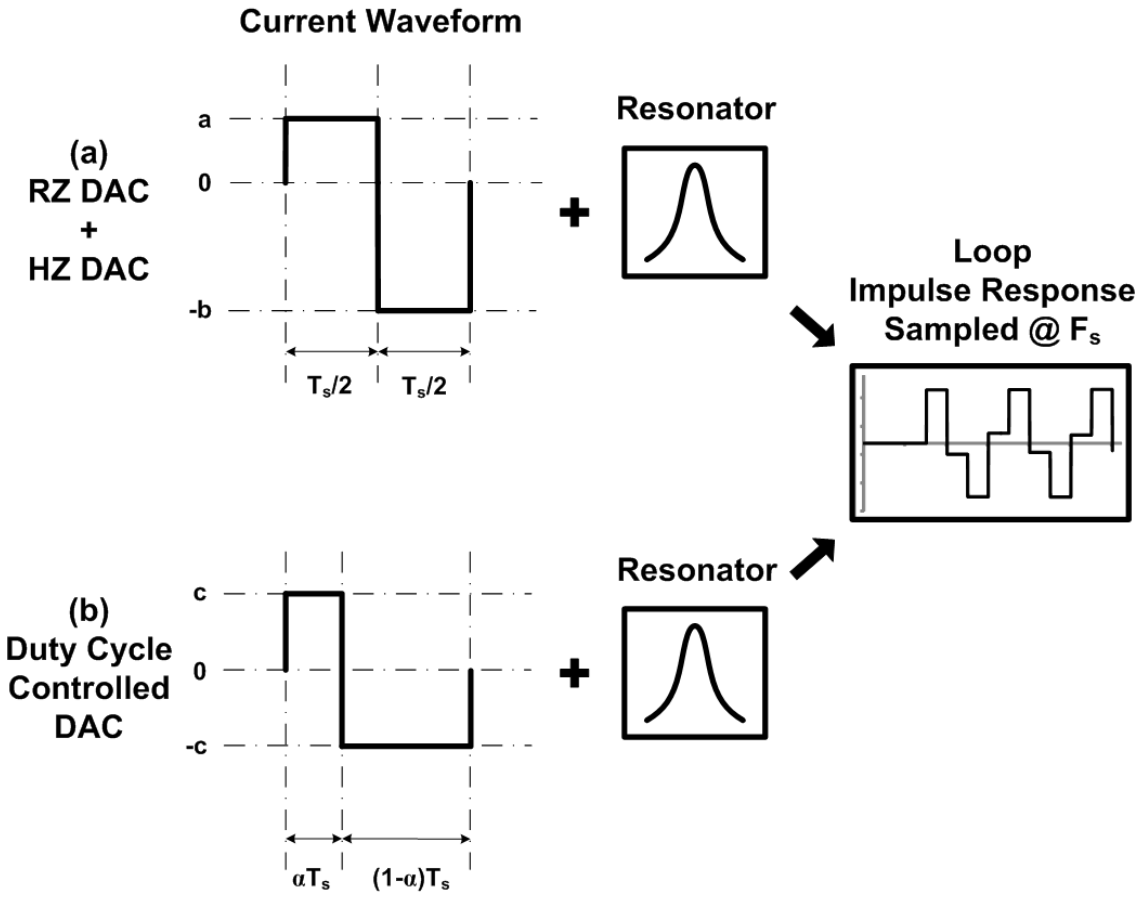


Figure 38. Replacement of two DACs with one duty-cycle-controlled DAC

Instead, without affecting the STF, we introduce a single, variable-duty-cycle NRZ DAC to replace the combination of the RZ and HZ DACs. Here adjustment of the duty cycle allows one single DAC to operate as two DACs (i.e. RZ and HZ) in a CTBPDSM, since both the pulse width and pulse amplitude convey information. Figure 38(a) shows the waveform resulting from

the combination of RZ and HZ pulses with RZ and HZ DAC amplitudes of 'a' and 'b'. The duty-cycle controlled DAC waveform in Figure 38(b) is NRZ and has constant amplitude 'c', and the duty cycle is no longer 50%. Thanks to the variable duty cycle, the waveform has information in the amplitude 'c' and the duty cycle 'α', while the conventional combination of RZ and HZ DACs only has the information of the amplitudes of the two pulses. Therefore, the duty-cycle controlled DAC waveform of Figure 38(b) is made equivalent to that of Figure 38(a) in one clock period of a CTBPDSM by choosing 'c' and 'α'. It can be easily shown that the sampled loop impulse response of this duty-cycle-controlled DAC, plus resonator, in a CTBPDSM is exactly the same as that for the two DAC systems. Similarly by adjusting the duty cycle, this new DAC facilitates a CTBPDSM with $F_c \neq F_s/4$.

An NRZ current waveform with the duty cycle of α ($0 < \alpha < 1$) and a constant amplitude is expressed as:

$$\frac{1 - e^{-s\alpha T_s}}{s} - \frac{e^{-s\alpha T_s}\,(1 - e^{-s(1-\alpha)T_s})}{s} = \frac{1 - 2e^{-s\alpha T_s} + e^{-sTs}}{s} \tag{31}$$

Next, the loop transfer function when combined with a resonator in the 2nd–order CTBPDSM is

$$\frac{\omega_c(1 - 2e^{-s\alpha T_s} + e^{-sTs})}{s^2 + \omega_c^2} \tag{32}$$

The impulse response of this transfer function is:

$$sin(\omega_c t) + sin\big(\omega_c(t - T_s)\big)\,u(t - T_s) - 2sin\,(\omega_c(t - \alpha T_s))u(t - \alpha T_s) \tag{33}$$

And the z-transform of this impulse response gives

$$\frac{sin(\omega_c T_s)z^{-1} + sin(\omega_c T_s)\, z^{-2} - 2(sin\,(\omega_c(1-\alpha)T_s)z^{-1} - sin\,(\omega_c \alpha T_s)\, z^{-2})}{1 - 2\,cos(\omega_c T_s)\, z^{-1} + z^{-2}} \quad (34)$$

$$= \frac{(sin(\omega_c T_s) - 2sin\,(\omega_c(1-\alpha)T_s))z^{-1} + (sin(\omega_c T_s) - 2sin\,(\omega_c \alpha T_s))\, z^{-2}}{1 - 2\,cos(\omega_c T_s)\, z^{-1} + z^{-2}}$$

The goal is to make (34) and (19) the same, and the variables are α, ω_c. The center frequency is related to ω_c, θ (in (19)). So even though the center frequency varies, the equivalence can be kept by changing α. For example, when the center frequency is at $F_s/4$, $\omega_c T_s = \theta = \pi/2$. This makes (19) become (20), and in (34) we can figure out that

$$sin(\omega_c T_s) - 2\,sin(\omega_c(1-\alpha)T_s) = 0 \quad (35)$$

since there should not be the term for z^{-1} in the numerator. We can get $\alpha = 2/3$ easily from this, and the same method can be used for any other center frequency location.

The advantage of the duty-cycle-controlled DAC scheme is that it has constant amplitude and can be implemented with one DAC. This reduces the power consumption and thermal noise of the DACs, and simplifies the modulator architecture. The new DAC scheme halves the total number of DACs without any detrimental modification of the architecture (such as additional feedforward paths), and therefore the CTBPDSM can have at most one DAC per resonator in any combination of feedback and feedforward paths.

3.4 Input Signal Filtering

The feedback-only architecture is the best for the bandpass filtering of the input signal, but this increases the number of DACs and also has large signal swings through the signal path.

Therefore it consumes a lot of power, and this is one of the reasons why many CTDSMs combine the feedback and feedforward paths[10].

In this architecture, the feedforward paths to the quantizer are all removed because these prevent filtering of out-of-band signals and make the STF flat. However, the feedforward path from *Resonator1* to *Resonator3* in Figure 36 barely affects the STF if the gain of *Resonator2* is adjusted, and so it can be used to reduce the output swing of *Resonator1*, which is the most power hungry block in the modulator. This feedforward path also allows the removal of the DAC for *Resonator2*. Any peaking in the STF due to this path is minimized with little penalty in SNDR by reducing the gain of *Resonator2*. This method relaxes the power and linearity requirements. Furthermore, it does not require a summing amplifier before the quantizer, which can take a large portion of the total power consumption. At the same time, we minimize STF peaking to below 1dB and achieve a bandpass STF.

Even though this architecture is not able to filter the input signal as well as a resonator since it has a wide bandwidth, it definitely helps suppress interferers that are far away, and prevents the modulator from being saturated by them.

3.5 Circuit Blocks

3.5.1 Op-amp

For better noise performance, the resonator has to have smaller input resistors since the input resistors mainly decide the input referred noise of the modulator. Accordingly, all the resistor sizes in the RC network are decreased and the capacitor sizes are increased in order to keep the

same resonator gain and resonant frequency. The thermal noise caused by the amplifier itself also has to be reduced below the thermal noise of the input resistors. This makes increased power consumption inevitable. The increased linearity requirement also leads to an increase in power consumption. The amplifier has a larger load, so the output stage has to drive more current to prevent slewing. The increase in current leads to large device sizes, which limit the bandwidth of the amplifier.

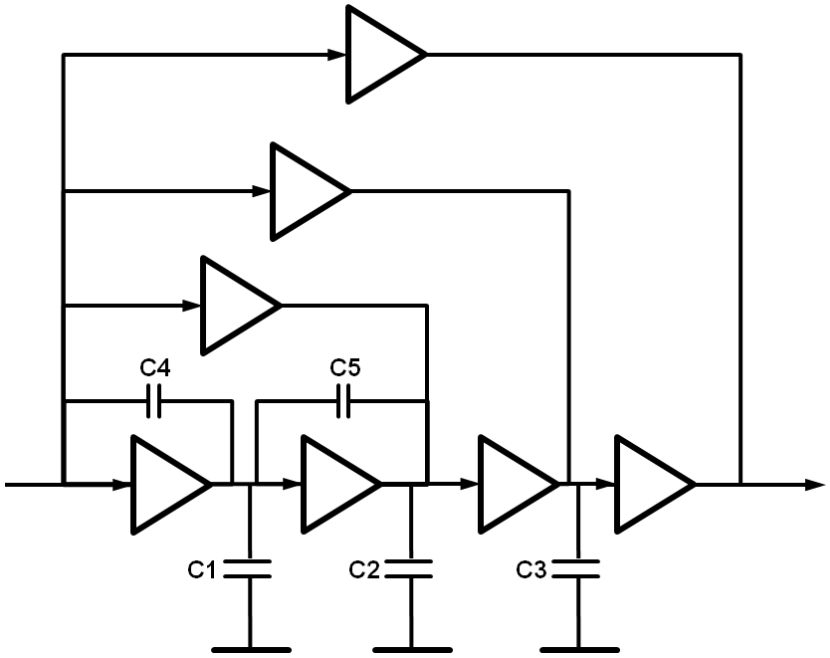


Figure 39. Multi-stage amplifier with gm-C compensation

The amplifier structure is modified to ensure large bandwidth as well as high gain. The new amplifier uses a multi-stage scheme like the first prototype, but has g_m-*C* compensation instead of nested Miller-compensation[97]. Figure 39 shows the amplifier structure. The gain gradually decreases as the frequency goes up due to the capacitor *C1-3* after each stage. These capacitors limit the bandwidth of each path, and let the fastest path with a single stage keep the phase shift low at higher frequency and guarantee a good phase margin. The longest path with four stages

has the highest gain but the narrowest bandwidth. The next longest path has three stages, and the gain is lower but the bandwidth is wider compared to the longest path. Therefore, this path gets dominant over the longest path above a certain frequency, and the same thing happens to the other paths. By using feedforward paths to the internal nodes, the stages are shared by several paths and the total power consumption as well as the total number of stages are reduced[92]. The total of four paths give wider bandwidth and higher gain compared to the amplifier used in the first prototype.

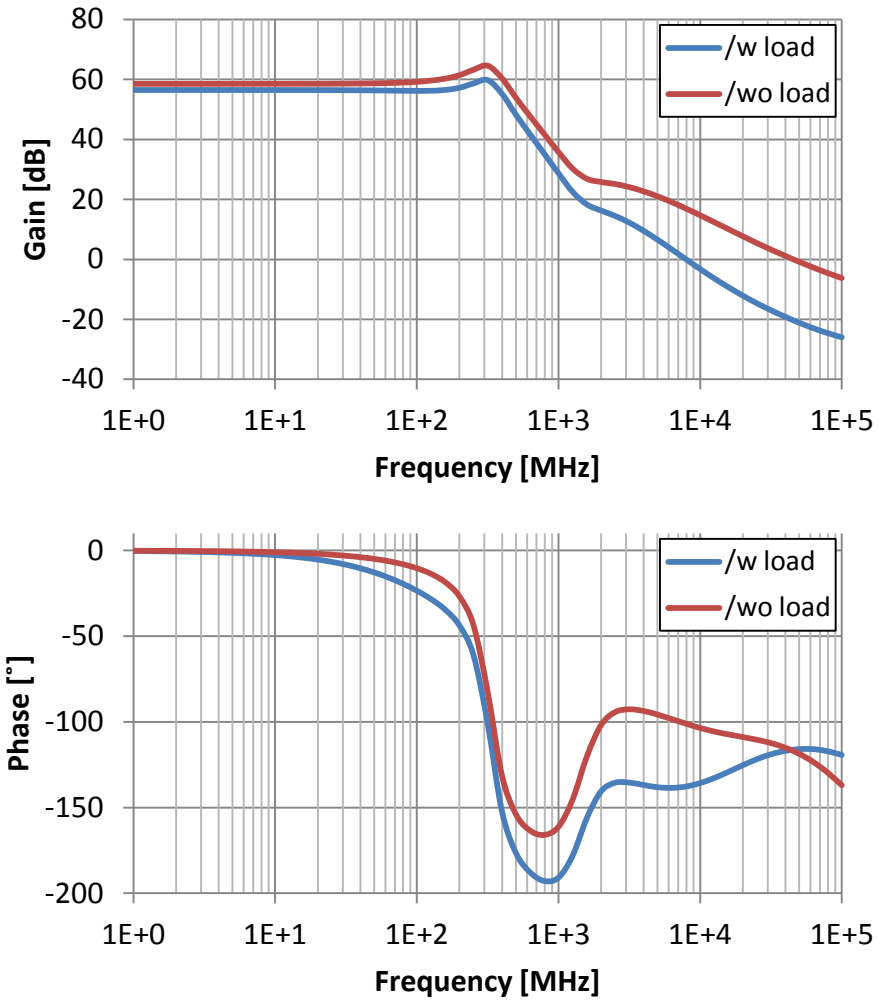


Figure 40. Gain and phase response of the amplifier

Introducing capacitors *C4-5* from the input and output of the first two stages (between the same polarity) generates left-plane zeros[98]. These effectively reduce the bandwidth of each stage and can reduce the capacitor size *C1-2* between the stages due to Miller-effect. Since these cause slight peaking in the open-loop gain response of the amplifier, it is possible to get more gain around the edge of the bandwidth and thus wider total open-loop bandwidth of the amplifier. The left-plane zero due to *C4-5* prevents the gain attenuation at high frequency, but it also recovers the phase response close to 0 degree and does not decrease the total phase margin. The simulation result in Figure 40 compares the gain and phase response of the amplifier for the first resonator with or without the load which are the passive components in the feedback network. The amplifier has a 450MHz 3dB bandwidth with 57dB DC gain even with a load. The phase margin is around 50 degree.

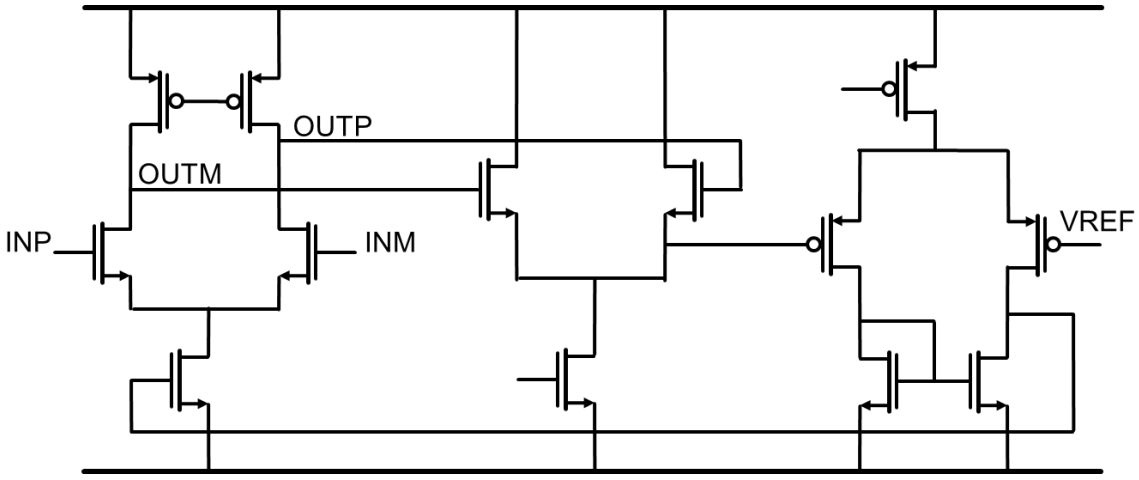


Figure 41. First stage of the amplifier with CMFB

Figure 41 shows the first stage of the amplifier in the longest path, and includes the common mode feedback circuit. The thermal noise from this stage is critical for the input referred noise, so the output common mode voltage sensing is done through source followers since the direct use of resistors at the output for sensing adds thermal noise to the amplifier output. The other

stages are less critical for the thermal noise, and use resistive common mode feedback circuits. The width of the input devices is sized large to decrease the input referred noise. The noise voltage at the output is proportional to $\sqrt{g_m}$ while the gain is proportional to g_m, which means that increasing g_m by adopting large (*W/L*) helps reduce the input referred noise.

For a large voltage headroom in the last stage of the amplifier, a separate high supply voltage of 1.7V is used only for the last stage, while the other stages run from 1.2V supply. Larger voltage swing at the output helps reduce the input referred noise because it allows the resonator to have more gain. The power consumption of the first resonator is 7.5mW, and the other two resonators consume a total of 9mW.

3.5.2 DAC

The regular supply voltage is not enough to suppress the thermal noise of the current source when a triple cascode structure is used. So I/O devices and a 2.5V supply voltage are used to get a very large gate overdrive of the current sources[92] since this helps lower the g_m of the current source and reduce the thermal noise. The virtual ground node voltage of the resonator is 1V, so PMOS devices are used for the current source as in Figure 42. The voltage headroom is 1.5V now, and 1V is assigned to the current source. The remainder of the headroom is assigned equally to the cascode device and the switching devices. This reduces the thermal noise significantly, and the input referred noise of this modulator also decreases to the required level.

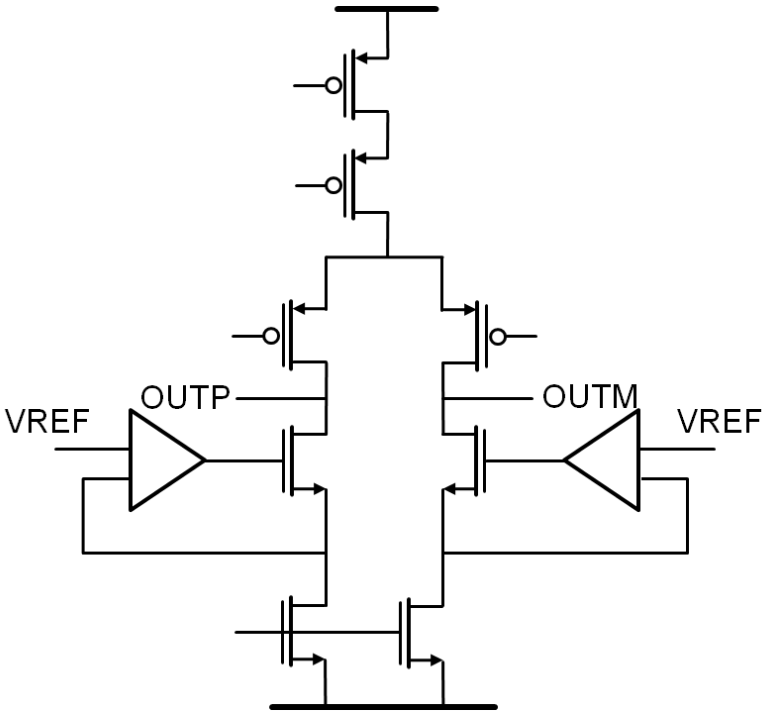


Figure 42. Triple-cascode PMOS DAC and counterpart NMOS current source

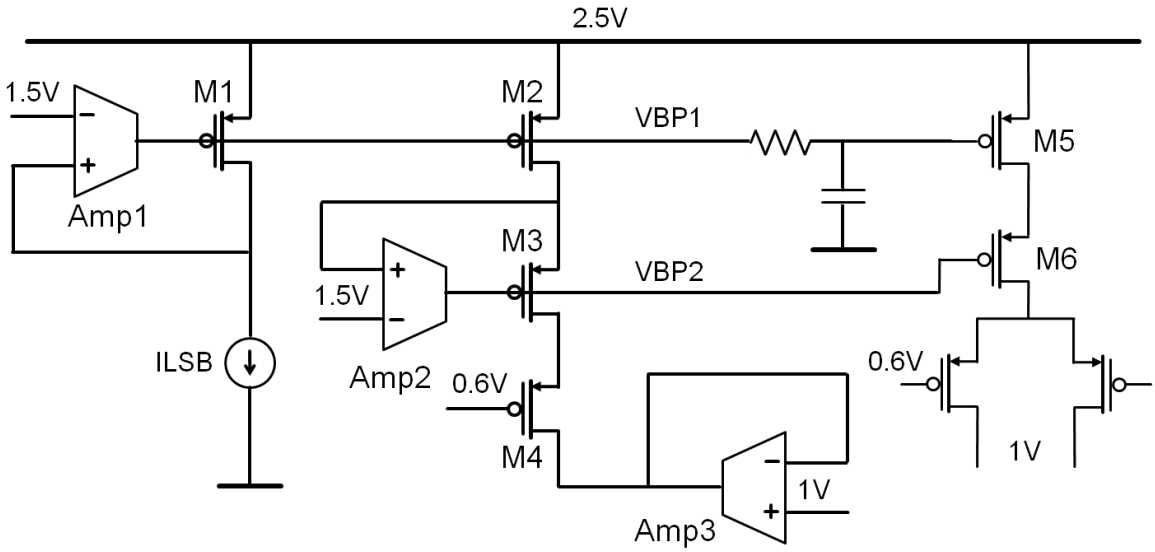


Figure 43. DAC bias circuit

The biasing circuit in Figure 43 is used to generate a bias voltage to maintain the source-to-drain voltage, V_{DS}, assigned to each transistor. The first step is to generate the gate voltage of the PMOS current source *M1* with the bias current set to current 1 LSB of the current DAC and the drain voltage is set to 1.5V by a feedback loop with *Amp1*. The gate bias voltage of *M1* is applied to another current source device *M2* with the same size, and then the cascode device *M3* is biased by another feedback loop with *Amp2*. A PMOS transistor *M4* with the same size as the switching device is connected to the drain of *M3*. The other side of *M4* is fixed at 1V to get the exact same condition as the triple cascode structure in the DAC. For this, a unity gain buffer with *Amp3* provides the 1V bias based on a 1V reference generated by a resistor ladder connected between the supply rails. The generated bias voltage *VBP1* goes through an LPF comprised of a resistor and a capacitor to suppress thermal noise injection through the gate of the current source *M5*. There is no filtering for *VBP2* to *M6* since this is not critical for thermal noise.

The counterpart NMOS current source to sink the current from the PMOS current source has an active cascode structure as shown in the lower part in Figure 42. This keeps the output impedance high, and also gives enough headroom to overdrive the NMOS current source to reduce thermal noise. Similarly with the biasing of the triple cascode structure, the V_{DS} of the NMOS current source device is assigned to 750mV, and the active cascode structure generates the gate voltage of the cascode devices to set the drain voltage of the current source to 750mV. And another feedback loop not shown in the figure generates the gate voltage of the NMOS current sources to get 1V at the DAC outputs, which makes the NMOS bias current the same as the PMOS bias current.

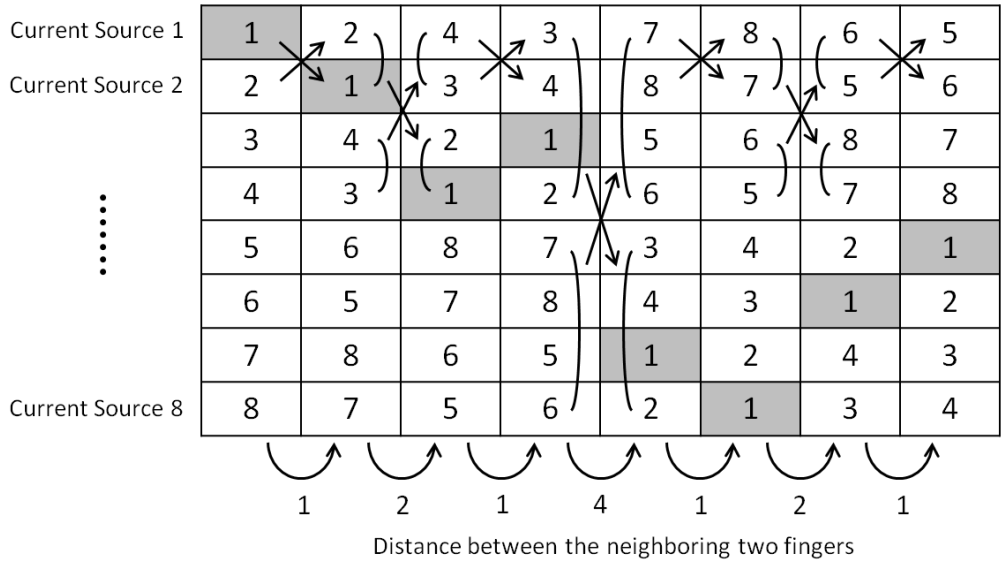


Figure 44. Layout of the DAC current sources

Matching between the current sources is very important to suppress harmonics at the modulator output. So as not to use DEM circuits which consume more power, the size of the PMOS current sources is made very large for good matching. For even better matching between the current sources, the devices are split into several fingers and the fingers are mixed as common-centroid layout to avoid local mismatch. Figure 44 shows how the current sources are configured. There are eight current sources in the example shown here, and each device has eight fingers (total 64 transistors). None of the fingers for the same current source exist in the same row, but every row has one finger from each current source. Even though the fingers are distributed evenly over the layout, the mismatch in the connection length can contribute to nonlinearity. Each current source is connected to the cascode device on either left or right side of the whole layout. The connection length of eight fingers from the same current source has to be the same for every current source. To solve this, each finger in a column is connected to the finger in the next column with the same distance for every current source. From the first column

to the second column, every finger is switched with the neighbor in pair, which fixes the connection length between two fingers in the two columns from the same current source to 1. From the second to the third column, two fingers are grouped and the groups are switched, and this fixes the distance to 2. In this way, the whole connection length of eight fingers from the same current source can be the same for all current sources. The local mismatch between the current sources is reduced substantially since the device size is large.

3.5.3 DAC Latch

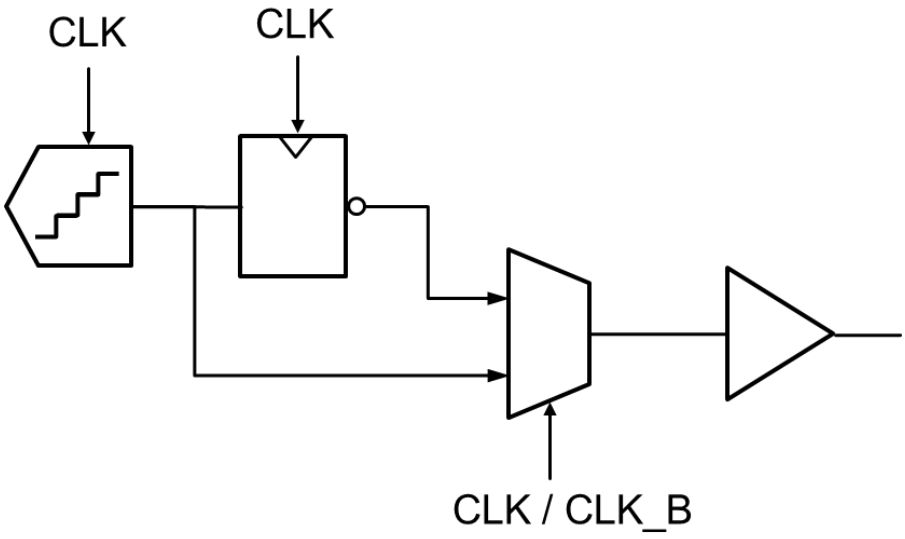


Figure 45. DAC latch with duty cycle control

To generate a DAC output signal with variable duty cycle, the DAC latch has to combine the quantizer output with the clock. The DAC latch consists of a flip-flop and a mux, and is shown in Figure 45. The flip-flop holds the comparator output since the comparator output is valid only for the first half clock period. The output of the flip-flop is inverted, and the clock switches the mux output between the comparator output and the inverted one. This generates the required output

signal with the duty cycle same as the clock. The mux and the following inverter chain use large (*W/L*) to reduce the jitter noise.

3.5.4 Level Shifter

The output common mode voltage of the DAC is 1V, so the switching devices of DACs become saturated at 0.6V and totally turn off at 1.4V. The digital output from the DAC latch swings between the supply rails of 0V and 1.2V, and therefore a level shifter is required to generate the switching signal that goes between 0.6V and 1.4V. Separate supply domains are necessary to isolate the DAC driver from other supplies since supply noise can be considered as clock jitter noise and reduces SNDR.

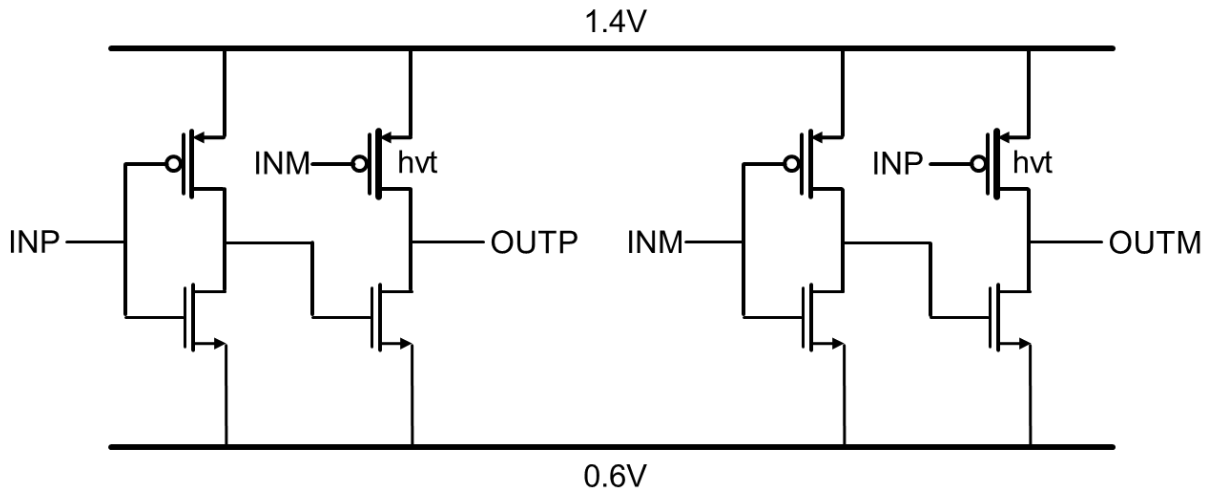


Figure 46. Level shifter

The level shifter has to operate fast enough to suppress the transient noise, and the differential output signals should cross with each other at lower voltage (close to 0.6V) to prevent both PMOS switches from being turned off at the same time[99]. Figure 46 shows the level shifter implementation. On the left side, the first inverter works faster when the input *INP* goes down

since the ground is tied to 0.6V and V_{GS} of the NMOS decreases fast. Therefore, the inverter output increases quickly to 1.4V and the output *OUTP* drops down quickly to 0.6V. Due to the supply domain change from 0V and 1.2V to 0.6V and 1.4V, a low cross-over voltage of the differential output signals is inherently achieved, but the first inverter output goes down too slowly when *INP* goes up. If another inverter is used for the second stage, both the outputs stay low for a while since it takes time to turn on the PMOS of the second inverter. Instead, *INM* is directly connected to the PMOS gate instead of the inverter output. This makes pulling up *OUTP* faster, and prevents both the signals from being low together for a long time. To guarantee the low crossing of the signals at the same time, a high threshold voltage (hvt) device is used for the PMOS.

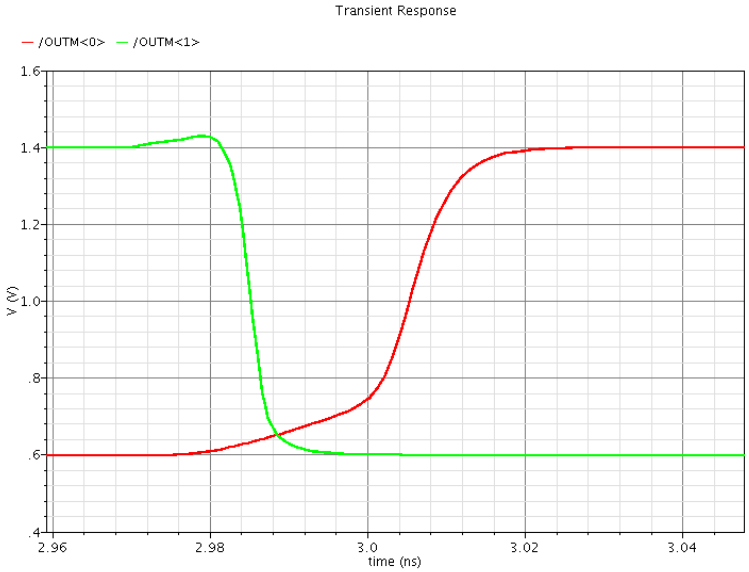


Figure 47. Level shifter output waveform

Figure 47 shows the differential outputs of the level shifter. The two signals cross close to 0.6V, and the rising signal rises right after the crossing with the help of a hvt device.

3.5.5 Clock Generator

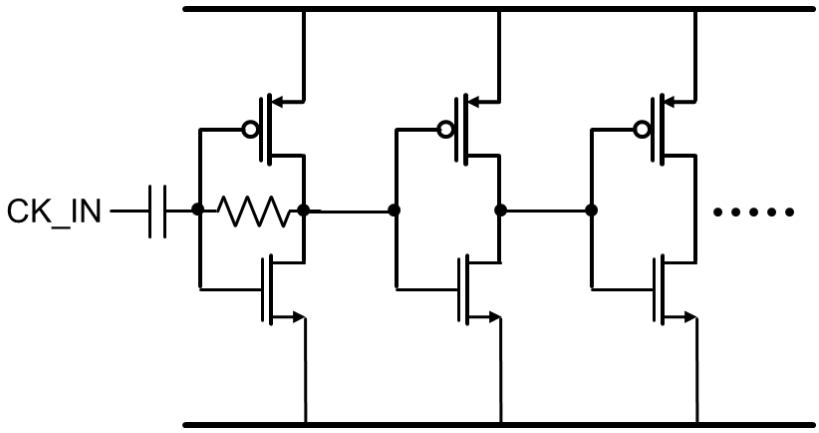
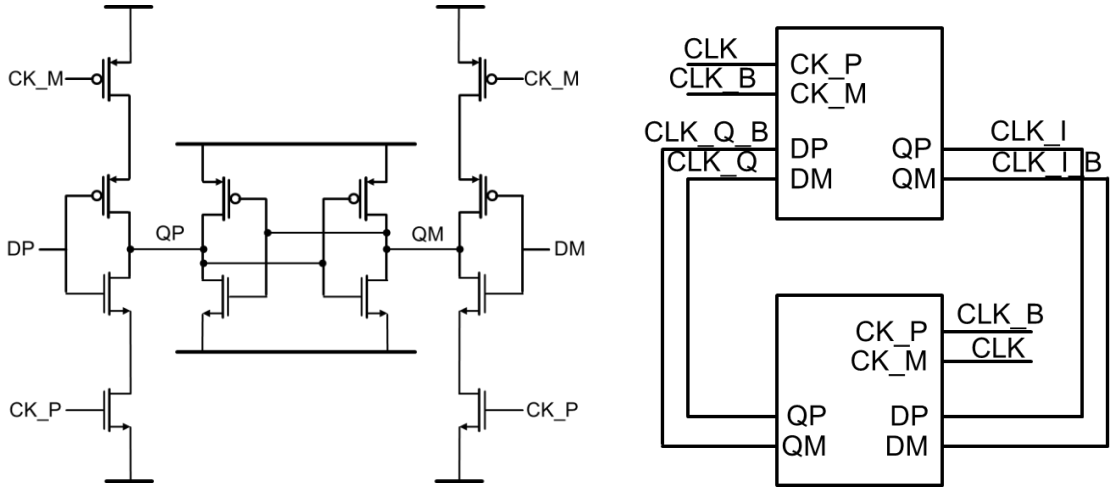


Figure 48. Clock receiver



(a) Latch **(b) Divider with two latches**

Figure 49. Clock divider

The clock input twice faster than the sampling frequency is used to generate 25% duty cycle with minimum clock jitter. The 25% duty cycle is generated by 'AND' operation on the two divided clocks with different phases. The clock receiver in Figure 48 gets the clock input from off-chip, and generates a square waveform from the sine waveform input. It uses resistive

feedback to self-bias the amplifier and ac-couple the clock input. To generate I and Q phases from this clock signal, the clock divider in Figure 49 is used. This latch and the clock divider provide balanced clock and its complement as well as two phases.

The default duty cycle for this modulator is 25%, but a different duty cycle is required for the frequency tuning as mentioned in 3.3. To adjust the clock duty cycle, a separate bias voltage is used for the clock receiver as in Figure 50. The voltage at node *X* is generated by another inverter with resistive feedback. This additional circuit changes only the bias voltage and keeps the original clock receiver transistor sizes, which are determined by the clock jitter noise. The bias generator inverter has smaller transistors to reduce power consumption, and the noise from this circuit barely gets into the main clock path because the gate noise at node *X* of the bias generator is very small. There are several PMOS transistors in parallel, and can be turned on and off depending on a digital control signal. This changes the voltage at node *X*, and also changes the duty cycle of the clock receiver output since it changes the midpoint of the sinusoidal input.

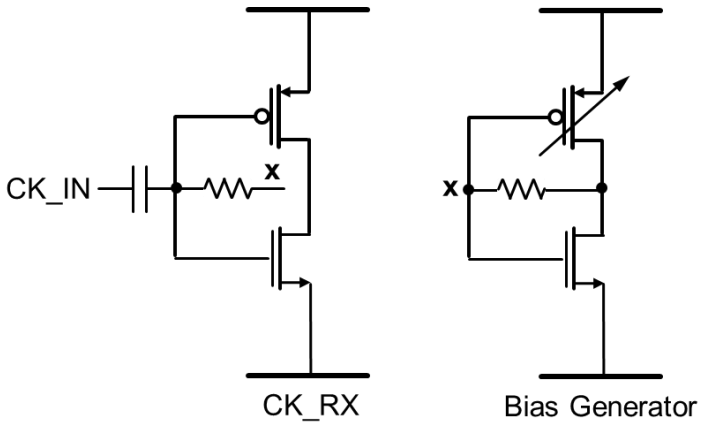


Figure 50. Clock receiver bias circuit

Clock jitter noise is important since it increases the noise around the NTF notch in a manner similar to the thermal noise caused by other blocks. Inverter chains with a large (*W/L*) ratio are

used from the clock receiver to reduce the clock jitter. The clock jitter requirement for this modulator is 500fs[100] to achieve around 80dB SNDR, but the inverters are sized to have the clock jitter of 250fs for margin, in case of inaccuracy of the simulator. The clock generation and distribution circuits run from a separate clean supply in order to have better jitter performance.

3.5.6 Quantizer

A 17-level flash ADC is used as the quantizer, and the comparator is the same as that used in the first prototype. The input swing to the quantizer is doubled compared to that of the first prototype to keep the LSB size the same. This enables the re-use of the comparator and the offset calibration circuits.

3.5.7 Global Bias Circuit

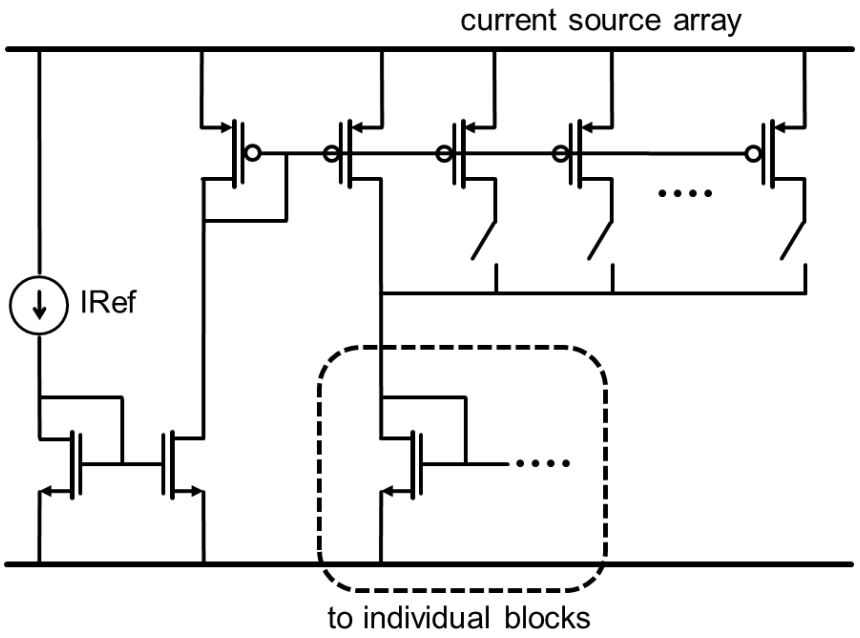


Figure 51. Global bias circuit

This modulator gets only one bias current from off-chip, and generates bias currents for every block from this current. The global bias generation circuit is shown in Figure 51. The bias current for each block is generated by a current mirror DAC and the magnitude is digitally controlled by the scan chain. The PMOS transistors with switches in parallel with the main transistor are turned on and off depending on the digital code to change the bias current to the individual blocks. For fine adjustment of the bias current to each block, the bias currents to three resonators and the second DAC are controlled to 5 bit resolution and the bias current to the first DAC is set to 6bit value. The bias current for the flash ADC calibration is a 4bit value since it does not need to be very accurate. While all the bias currents to the blocks are below 40uA, a 100uA current is used as the off-chip reference bias current '*IRef*' for more accuracy.

3.5.8 System Implementation

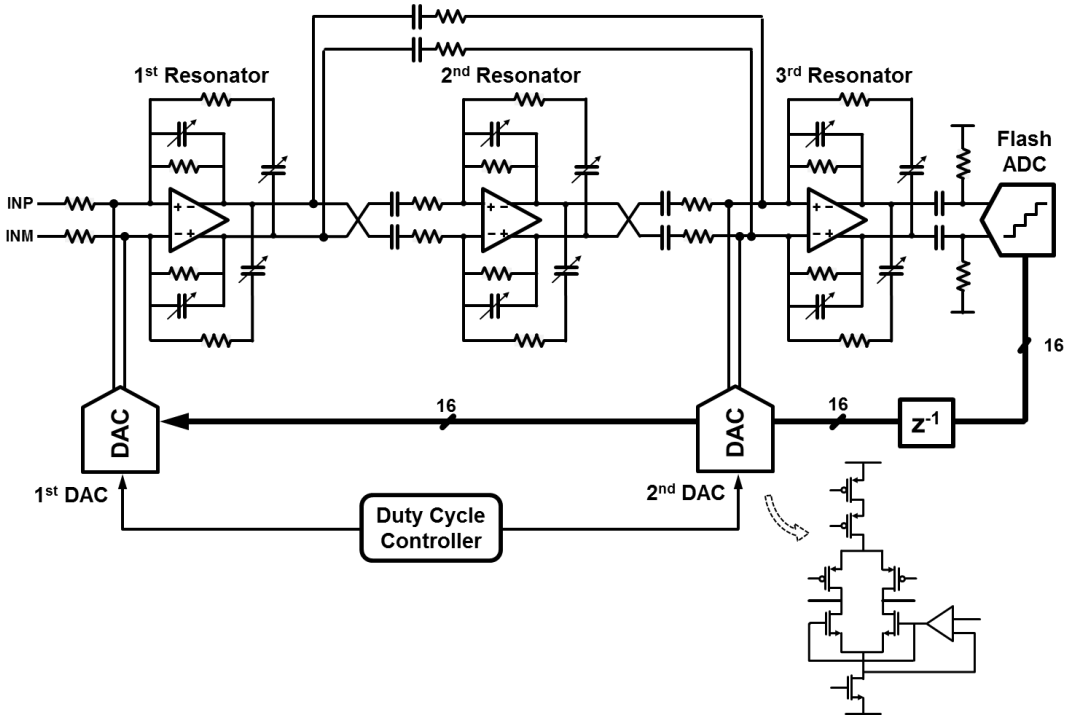


Figure 52. System implementation

Figure 52 shows the system implementation. Passive HPFs are used to connect resonators and to make a feedforward path. The output of the flash ADC is delayed by one clock. To implement a 6^{th}–order CTBPDSM, three op-amps and two current-mode DACs are used with the help of duty cycle control, and this enable large savings in terms of power and area.

There are also calibration circuits for resonator RC tuning, DAC biasing, flash ADC offset cancellation, clock duty cycle control, and clock path mismatch compensation. Several test point nodes are multiplexed to pads in order to facilitate the calibration.

3.5.9 Output Buffer

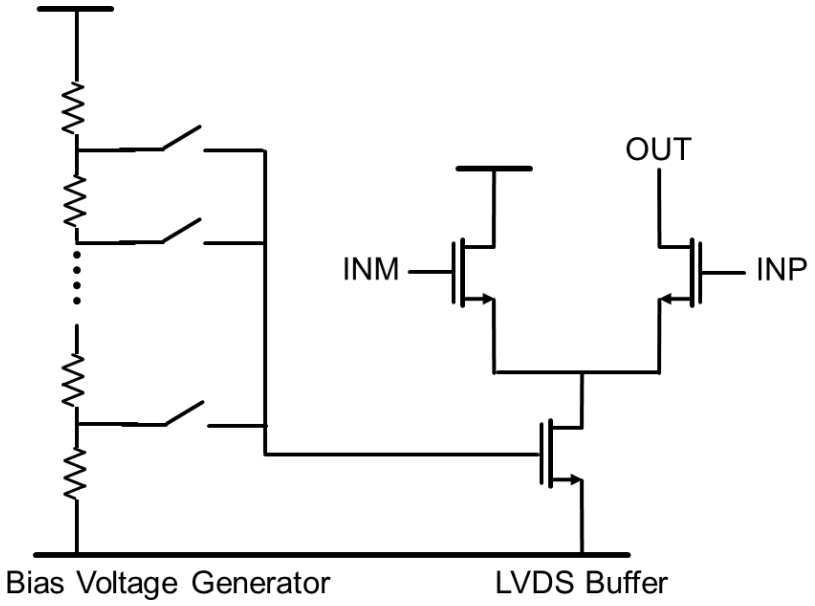


Figure 53. LVDS buffer for output

This modulator operates with a sampling rate of 800MHz, however it is difficult to get the 800MHz digital signal off the chip even with decent equipment. Therefore, the digital output of the flash ADC is interleaved by 2, and the digital output runs at 400MHz. More interleaving is not possible due to the limited number of I/O pads. However, 400MHz is still fast and inverters

are not suitable to drive the output pads because the outputs drive a large amount of current for high speed but it makes the supply rails too noisy. This can affect the other supply domains and cause harmonics at the modulator output. To avoid this, low-voltage differential signaling (LVDS) buffers drive the digital outputs[101]. Figure 53 shows the buffer structure. The differential output steers the current direction between the supply and the output pad. Only one side is connected to the output pad in order to reduce the number of output pads, and this is not critical since the current through the ground pad is still the same. The power pad for the LVDS buffers is isolated with other supply rails. The gate bias voltage of the current source of the LVDS driver does not need to be accurate, so a resistor ladder with switches is used for flexible biasing. The current output can vary from 1mA to 12mA per buffer, which provides a large dynamic range for the detection of the logic signal off-chip.

3.6 Measurement

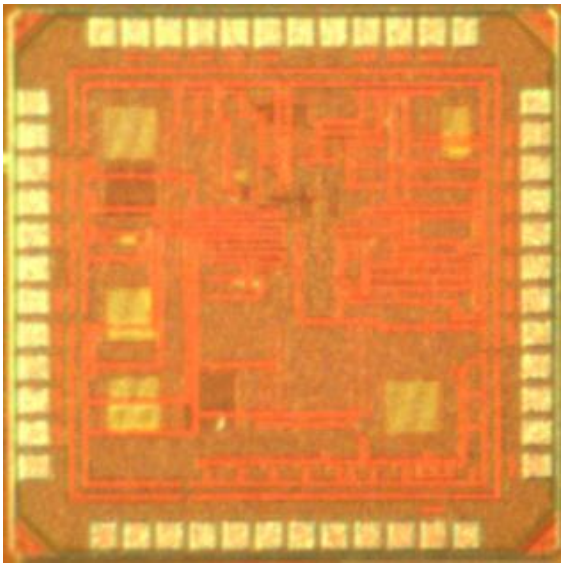


Figure 54. Die micrograph

The prototype is fabricated in 65nm CMOS, and the active area of the die, which includes resonators, DACs, DAC latches, a clock generator, and a quantizer is total 0.25mm^2. 9 metal layers are used, and Figure 54 shows the die micrograph. The biasing of the circuits is done on the chip, so most pads are assigned for power, ground, and digital I/O.

Calibration of the resonators is performed before evaluating the normal operation of the modulator. The quality factor is measured by observing the test point from the resonator output with a spectrum analyzer. The calibration circuit is able to feed the input signal to each resonator directly while bypassing and disabling the other circuits. This makes it easier to calibrate individual resonators independently.

The digital signals are read by a logic analyzer which can support up to 500MHz, and the interleaved signal is recovered by software. The LVDS output signal swing is around 300mV.

3.6.1 SNDR

Measurements show 69dB SNDR over a 24MHz bandwidth with a 800MHz sampling rate when F_c is set to 200MHz as in Figure 55. Thanks to the 6th-order modulation with more anti-alias filtering and better design of the blocks, the third harmonic is suppressed enough not to affect the SNDR. The use of the duty-cycle-controlled DAC perfectly replaces the two DACs with RZ and HZ phases, and it does not cause any asymmetry in the measured power spectral density. The measured noise shaping slope is between 40dB/dec. and 60dB/dec. since the gain of the second resonator is reduced to suppress the peaking in the STF.

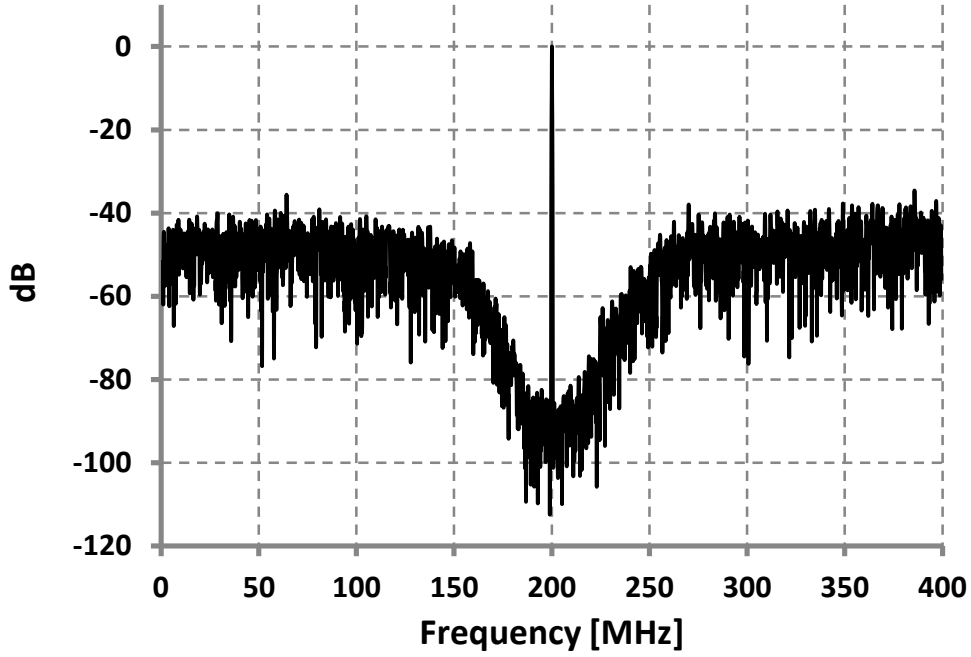


Figure 55. Power spectral density

3.6.2 STF

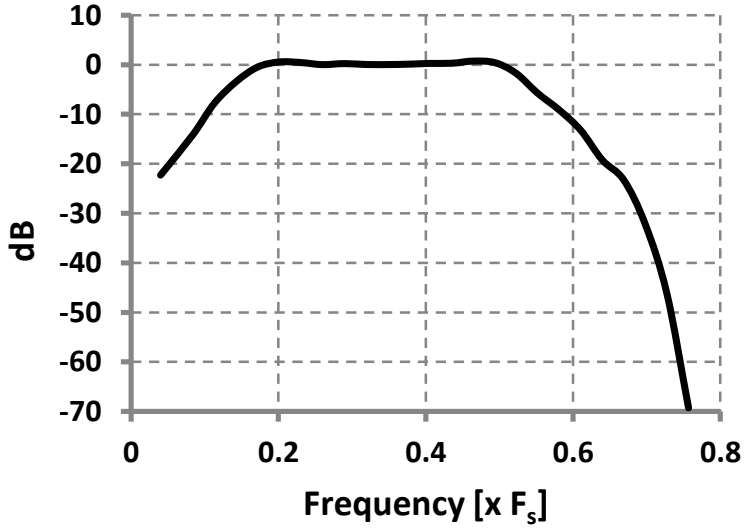


Figure 56. Measured signal transfer function

The STF is measured by feeding two tones to the modulator input. One has the same frequency as the center frequency, and the other tone varies from DC to higher frequency. The

difference between the two output magnitudes implies the input filtering characteristic of this modulator. The measured STF is shown in Figure 56. The maximum peaking is less than 1dB and the 3dB bandwidth is 300MHz.

3.6.3 IM3

Figure 57 shows the measured power spectral density with a two-tone input. The tones are 1MHz apart from each other, and are located around the edge of the bandwidth since it shows how the signals are intermodulated to in-band IM3 product. The measured IM3 is 73dB, and the intermodulated signals are close to the noise floor.

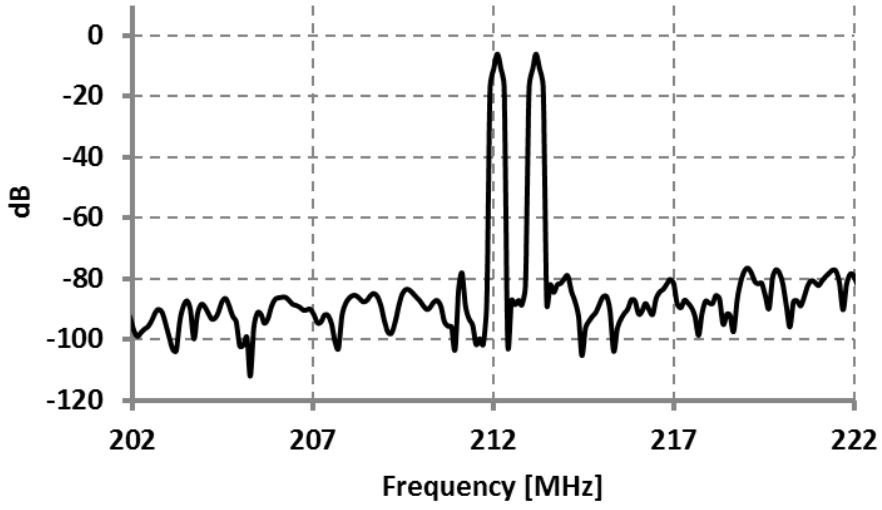


Figure 57. Power spectral density with a two-tone input

3.6.4 Frequency Tuning

Figure 58 shows the operation of the prototype at other center frequencies. The resonator and the clock duty cycle have +-10% tuning range, and the center frequency of the prototype can be tuned from 180MHz to 220MHz. Figure 58(a) and Figure 58(b) show the measured power

spectrum density at each corner, and indicate an SNDR of 66dB and 67dB for the low and high F_c corners, respectively.

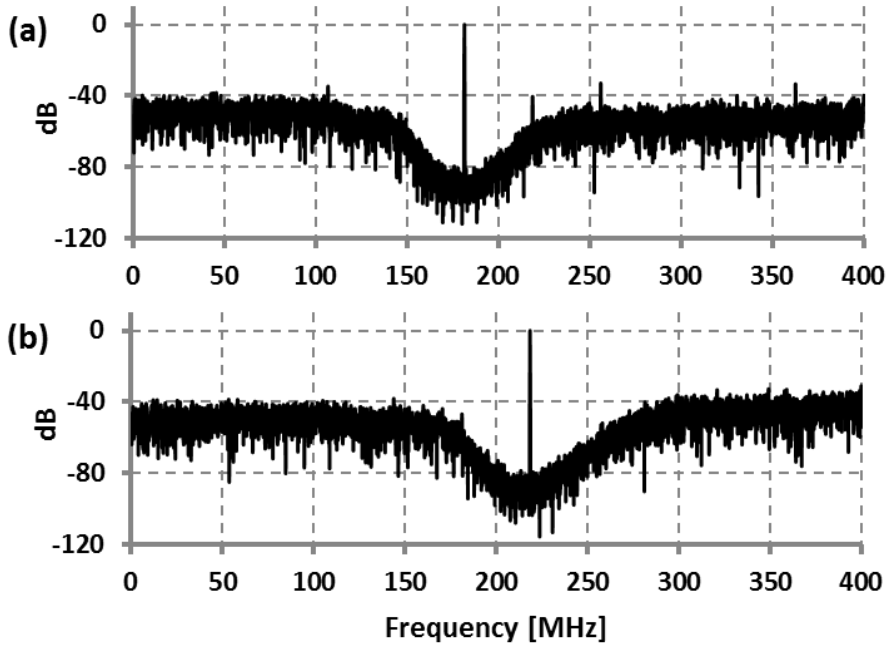


Figure 58. Different center frequency (a) 180MHz (b) 220MHz

3.6.5 Power Consumption

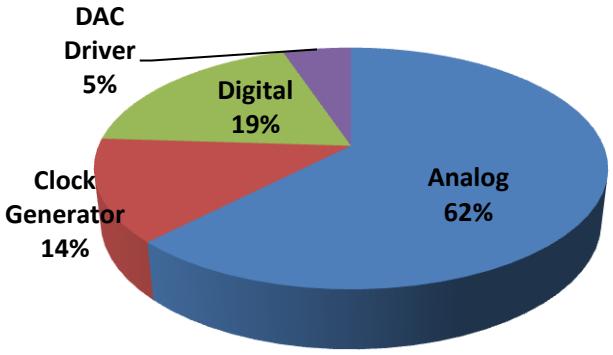


Figure 59. Power consumption details

The total power consumption including that of the clocking and bias generator is 35mW, and this corresponds to an FoM of 317fJ/conv-step. Table 5 shows the power consumption and the supply voltage details for each block. The resonators use dual supplies and the DACs run from a 2.5V supply in order to get better noise and linearity performance, while digital blocks use regular 1.2V supply. These blocks consume more than half of the total power as shown in Figure 59.

Table 5. Supply voltage and power consumption by blocks

Analog		
Resonators	1.2V+1.7V	16.5mW
DAC	2.5V	4.3mW
Bias	1.2V	1mW
Digital	1.2V	6.6mW
Clock Gen	1.2V	4.8mW
DAC Driver	0.6V+1.4V	1.8mW
Total		**35mW**

3.6.6 Performance Summary and State of the Arts

Table 6 summarizes the performance of this prototype. The sampling rate, the center frequency, and the bandwidth are the same as those of the first prototype, but there is huge improvement in performance. The 69dB SNDR corresponds to two more bits of resolution, and the dynamic range is 10dB higher. However, the power increases by less than a factor of 3 and this makes the FoM even better than that of the first prototype.

Table 6. Performance summary

Sampling Rate	800MHz
Center Frequency	200MHz
BW	24MHz
Power	35mW
SNDR	69dB
DR	70dB
Area	0.25mm^2
FoM	320fJ/conv.

Table 7 compares this work with state-of-the-art CTBPDSMs. Even with the reconfigurability, to our knowledge this work demonstrates the best energy efficiency for CTBPDSMs using active resonators.

Table 7. State of the arts

Author	Schreier	Ryckaert	Lu	Harrison	Shibata	1st Work	2nd Work
Publication	JSSC 2006	JSSC 2009	JSSC 2010	ISSCC 2012	ISSCC 2012	ISSCC 2012	
Order	4th	6th	6th	6th	6th	4th	6th
DR [dB]	90		70		74	60	70
F_s [MHz]	264	3000	800	3200	4000	800	800
F_c [MHz]	44	2400	200	7-800	450	200	200
BW [MHz]	8.5	60	10	20	150	24	24
SNDR [dB]		40	68.4	70		58	69
SNR [dB]	77				69		
Power [mW]	375	40	160	20	550	12	35
Area [mm^2]	2.5	0.8	2.5	0.4	5.5	0.2	0.25
Process	0.18um CMOS	90nm CMOS	0.18um CMOS	40nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
FoM	3.81	4.08	3.72	0.19	3.72	**0.38**	**0.32**

Chapter 4. Future Work

The prototypes show excellent performance and occupy very little die area. This makes the CTBPDSM suitable for mobile applications, however the current prototype requires complex testing environment. The difficulty in the calibration and test causes additional cost, and cannot be ignored in practice in large scale production.

Many pads are saved by generating most of the bias current on-chip, but still the prototype requires several supply domains for different blocks. The second prototype uses three different supply voltages, 1.2V, 1.7V, and 2.5V, for the analog circuits. The main reason for this is to reduce the noise and enhance the linearity. In the future work, the number of power domains can be reduced by using other methods to improve noise and the linearity, or by generating the supply voltages on-chip. A bandgap reference is also necessary for the modulator to be robust to the temperature variation, and remove the on-board bias circuit.

Next, the output signal needs a lot of I/O pads due to the interleaving. To avoid the waste of the I/O pads, a decimation circuit [103] could be integrated on-chip. Alternatively an SRAM could be used to store digital output of the modulator and then a serializer could be used to flush the data from the SRAM to off-chip. This would reduce the number of I/O pads and also slow down the output signal speed and simplify the data reading process.

Also, most calibration is done manually through the scan chain, and takes a long time. Automated calibration is necessary for practical designs, and therefore it is important to design the automated calibration method especially for the resonators. It is possible to measure the center frequency and quality factor by examining the resonator output swing variation. Therefore, a digital controller and comparators can support an automated calibration process.

By adding the listed characteristics to the current prototype, it can work as an independent system which requires only a single power supply, and can be easily used with other front-end blocks in the receiver.

Finally, a major change in the architecture can give a big advantage to CTBPDSMs. The second modulator provides only the wide bandpass filtering of the input, but a narrowband bandpass filtering is necessary considering the unexpected interferes and the reduction of the number of filters in the receiver. A different combination of the feedback and feedforward paths and the use of the filters in the modulator can achieve a narrowband bandpass filtering.

Also, another type of a resonator has to be exploited for the digitization of higher frequency signals. The current active resonator cannot cover the GHz frequency due to the finite gain-bandwidth product of the amplifier. It is related with the scale of CMOS technology, and a new method to maximize the operating range of the resonator is necessary for the modulator flexibility in the receiver.

By enhancing the input signal filtering capability and increasing the center frequency of the modulator, the software-defined radio can be more robust to the interferers with only a few analog blocks and be more easily reconfigurable for multiple standards.

Chapter 5. Conclusions

CTBPDSMs are very useful in the implementation of a software-defined radio due to their bandpass characteristic and the reconfigurability. And to solve the power efficiency problems, several methods to reduce the power consumption of CTBPDSMs are introduced in this research.

Here are the key contributions.

- A power-efficient single op-amp resonator can replace the LC tank resonator to achieve both low power and low area. The use of the positive feedback enables the implementation of the single op-amp resonator with only a few passive components.
- A simple 4^{th}-order architecture with low power consumption is also introduced. This architecture minimizes the number of DACs and there are one feedback DAC per resonator similarly to CTLPDSMs. And this reduces the power consumption and thermal noise of the DACS, and requires a small silicon area.
- The use of a new resonator and a new architecture reduces the number of the critical components in the CTBPDSM by half compared to the conventional ones.

The first prototype based on these techniques achieves 58dB SNDR and 60dB DR, and consumes 12mW including the power of the clock generator. And it has the better power efficiency compared to the state-of-the-art. The power efficiency approaches the efficiency of CTLPDSMs, and makes CTBPDSMs practical in the receiver.

The second prototype introduces other methods to reduce the power consumption.

- The use of duty-cycle-controlled DACs enables the use of a single DAC per resonator without affecting the STF. This replacement helps low power consumption, low area, and low thermal noise.
- The new architecture provides input signal filtering capability, and increases the dynamic range by reducing the peaking in the STF. This feature makes CTBPDSMs more robust in the software defined radio when interferers exist by reducing the chance for the modulator to be saturated.

  The center frequency becomes tunable with the help of duty-cycle-controlled DACs. This makes the mixer unnecessary in the receiver, and provides more flexibility making this CTBPDSM very useful in the receiver.

The measurement results of the second prototype show 11dB more SNDR, which is 2 more bit resolution, than the first prototype. And the DR is 70dB which gives 10dB more than the first one. The total power consumption is 35mW, and there is a 15% improvement in the figure-of-merit achieving even better power efficiency of the CTBPDSM.

The excellent power efficiency achieved with the techniques introduced here makes it easier to build an SDR without a power penalty compared to super-heterodyne receivers. Also, the flexibility and the filtering capability make CTBPDSMs more attractive for the front end of the receiver.

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