Efficient Si Nanowire Array Transfer via Bi-Layer Structure Formation Through Metal-Assisted Chemical Etching

*Taeho Moon, Lin Chen, Shinhyun Choi, Chunjoong Kim, and Wei Lu**

Nanowires (NWs) have shown great potential for applications in flexible and transparent electronics. The main challenges lie in improving the transfer yield and reducing the cost of NW fabrication. Here, it is shown that a bilayer SiNW structure can spontaneously form during metal-assisted chemical etching (MaCE). The bilayer structure formation is in turn accompanied by horizontal weak point formation that facilitates efficient nanowire transfer to diverse substrates. A mass-transport model is developed to explain the bilayer structure and horizontal crack formation effects. Significantly, these results allow repeated SiNW etch/transfer from the same Si wafer, thus potentially greatly reducing the fabrication cost of NW-based electronics. SiNW array-based transistors fabricated from two sequential etch/transfer processes using a single wafer are successfully demonstrated on Si and plastic substrates.

1. Introduction

Nanowires (NWs) have been extensively studied for their potential applications in electronics, optics and sensing applications.[1–3] In particular, the ability to transfer single-crystalline NWs from the growth substrate to another receiving substrate allows the fabrication of high-performance flexible and/or transparent electronics that can potentially outperform alternative approaches based on polymers or organics.[4,5] Key challenges for nanowire-based flexible electronics are improving the transfer efficiency and reducing the fabrication cost. Instead of growing NWs using a catalyst-mediated chemical-vapor deposition (CVD) method, metal-assisted chemical etching (MaCE) has recently received strong interest as a low-cost, large-scale fabrication alternative.[6–11] In particular, by using anodized aluminum oxide (AAO) membranes as templates, well-ordered and uniformly aligned SiNWs with sub-10 nm diameter can be obtained, which compares favorably to other template methods using nanosphere, block copolymer, interference lithography, and so forth.[12–16] However, controlled transfer of NWs onto other substrates such as glass or plastic is essential and still remains a major challenge. Additionally, the use of single-crystalline Si wafers as the starting material still brings up cost concerns. The direct transfer technique, based on contact printing by applying mechanical shear force to break and anchor NWs to produce NW arrays with an aligned form, appears most attractive due to merits such as process easiness and scalability for the integrated circuitry.[17,18] However, contact printing of the SiNWs formed by MaCE is difficult because of the lack of uniform weak points during NW-fabrication, which results in non-uniform NW breakage and low transfer yield. A few recent studies have tried to address this problem by creating intentional crack formation at the middle of SiNWs during MaCE, by using water soaking at high temperature or periodic pulsing of anodic bias in order to facilitate NW breakage at desired positions.[19,20] However, these processes requre additional steps or electrochemical setups, which can bring up cost and reliability concerns.

Herein, we show that horizontal cracks parallel to the Si substrate can be formed spontaneously during MaCE, leading to the formation of a bi-layer structure with well defined weak points for subsequent NW transfer. A phenomenological model based on mass transport was developed to explain the spontaneous bi-layer structure formation mechanism. Remarkably improved NW transfer to foreign substrates has been demonstrated. Significantly, we demonstrate repeated MaCE and transfer processes using the same Si substrate, illustrating the potential for low cost and large scale production of advanced SiNW electronics on plastic and transparent substrates.

2. Results and Discussion

The repeated transfer protocol of single crystalline SiNWs using a single Si wafer is schematically illustrated in **Figure 1**a. Aligned SiNWs with controlled diameters are produced through MaCE using AAO templates, followed by contact printing to produce aligned SiNW arrays on another device substrates (e.g., Kapton for flexible electronics applications), the Si wafer is then planarized, and the MaCE and transfer processes are repeated using the same Si wafer so that large scale SiNW-based electronics can be produced with high-quality Si nanowires at low cost.

The Au-mesh used for MaCE was produced by magnetron sputtering on an AAO membrane, and solution-transferred

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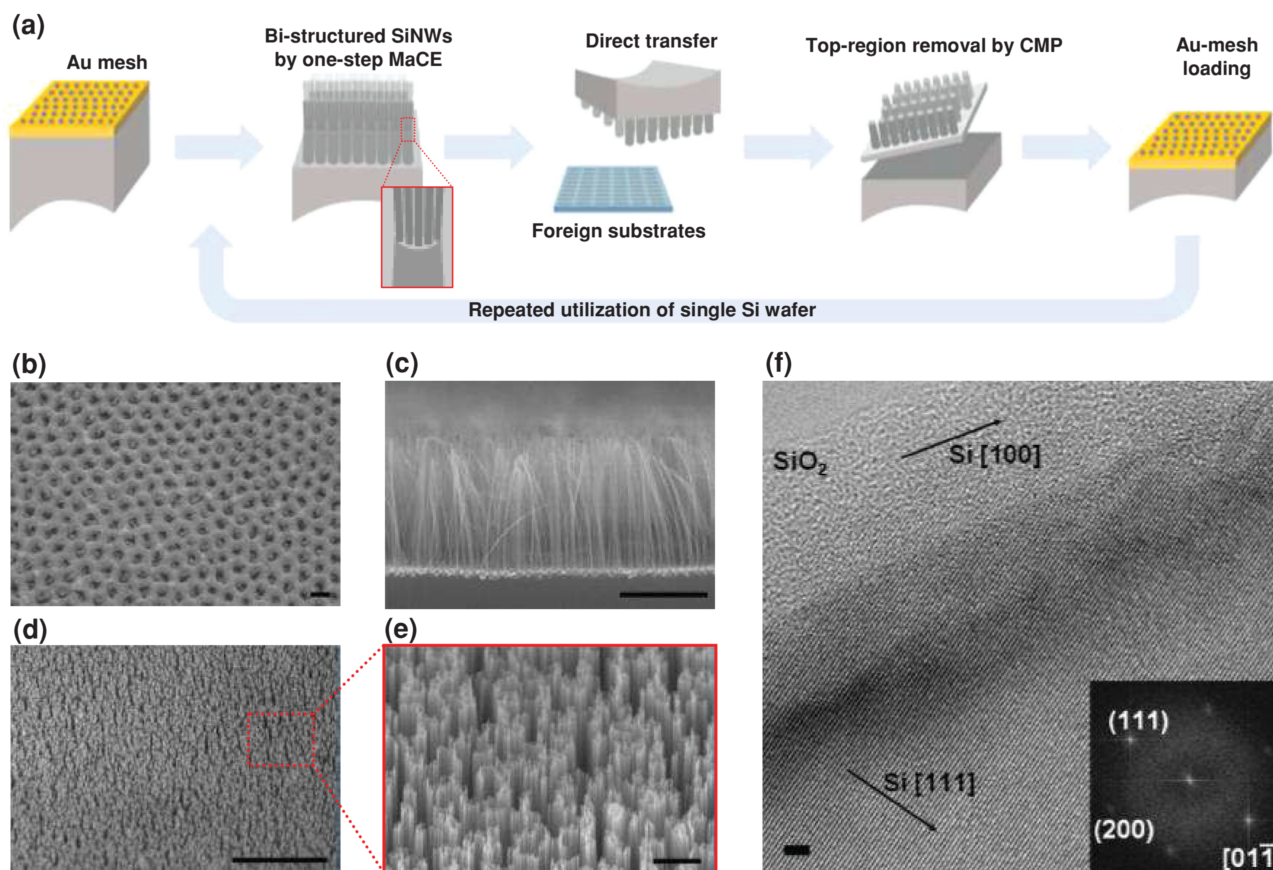

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Figure 1. Continuous massive fabrication of single crystalline SiNWs, using a single Si wafer. a) Schematic illustration showing the protocol of using a single Si wafer for massive SiNW fabrication, via Au-mesh loading, MaCE for bi-structured SiNW formation, NW transfer onto foreign substrates, and CMP. b–c) SEM images of the Au-mesh-loaded Si wafer etched for 10 min. b) Plane-view image. Scale bar: 100 nm. c) Cross-sectional view image. Scale bar: 1 µm. d) SEM image of the Si nanowires (etched for 30 min), after Au removal. Scale bar: 10 µm. e) Magnified image of (d). Scale bars: 1 µm. f) High resolution TEM image of the Si nanowire. Scale bar: 2 nm. Inset: Corresponding Fourier-transformed diffraction pattern.

onto (100)-oriented *p*-type Si wafers (B-doped, 1–5 Ω cm^{-1}). Two types of AAO membranes having pore periodicities (diameters) of 107 nm (35 nm) and 251 nm (80 nm) were used as templates for the fabrication of the Au meshes.[21,22] Figure 1b,c shows the top and side view SEM images of the Au-mesh-loaded Si wafer etched for 10 min, confirming vertical etching through the well-ordered hexagonal Au-nanohole array. The average diameter of the obtained SiNWs was estimated to ≈20 nm and ≈50 nm from SEM imaging, for AAO-pore diameters of 35 nm and 80 nm, respectively. The smaller diameters of the SiNWs compared to those of the AAO template pore sizes can be explained by side-wall deposition during Au sputtering on the AAO membranes.[12] Figure 1d shows a zoomed-out SEM image of another device after etching for 30 min and after Au removal, verifying the formation of large scale, vertically aligned SiNWs (Figure 1e). High resolution TEM studies further verify the single crystalline nature of the SiNWs produced by this method (Figure 1f). The SiNWs are found to be along the [100] direction with surface roughness of ≈3 nm. The formation of high-density single-crystalline SiNWs and the successful transfer of the SiNWs onto device substrates will be the key enabling factor for NW-based flexible/transparent electronics. Below we discuss how a bi-layer structure can be formed in the SiNWs during MaCE which in turn leads to horizontal cracks in parallel to the Si-wafer surface and facilitates the efficient transfer of the SiNWs at the top layer on diverse substrates. Significantly, this process can be repeated on the same starting Si wafer after planarization, further enabling the fabrication of low-cost and high-performance NW-based flexible and/or transparent electronics.

The bilayer structure formation and SiNW morphology evolution during MaCE were investigated systematically at different etching times, using a metal-mesh-pore periodicity of 107 nm (**Figure 2**). At a short etching time of 30 min, regular, well-aligned vertical SiNWs are clearly observed (Figure 2a). When the etching time is increased to 60 min, however, a bilayer structure starts to appear, with a well-defined NW top layer and a microstructure bottom layer, and a clear, uniform interface parallel to the Si wafer throughout the device (Figure 2b). Further increasing the etching time to 90 min simply resulted in the increase of the bottom-layer thickness while the top SiNW layer thickness remain unchanged at ≈18 µm (Figure 2c).

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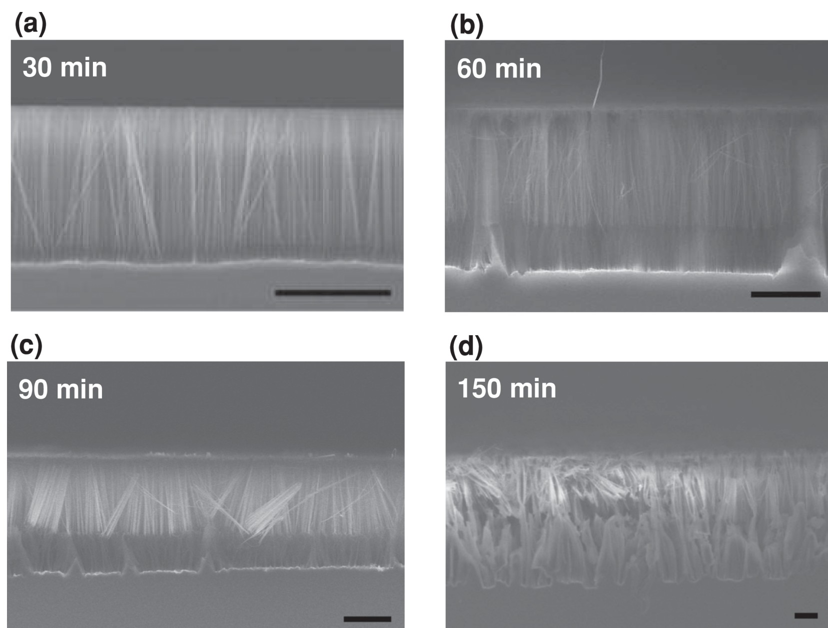

Figure 2. Etching-morphology evolution of the Si wafers during MaCE at different etch times, for Au-mesh-pore periodicity of 107 nm. a) 30 min. b) 60 min. c) 90 min. d) 150 min.

measurements over 50 NWs in each case, respectively. This observation also correlates well with the behavior that the top SiNW layer thickness remains unchanged when etching time was increased. Control experiments on samples dried naturally without critical point drying further suggested the bilayer structure provides natural weak points and crack formation for SiNW breakage and dramatically improve the transfer yield (see Supporting Information, Figure S1).

The SiNW morphology evolution was investigated further using a different metal-mesh-pore periodicity of 251 nm (**Figure 4**). At 30 min etch time, single layer vertical SiNWs are again observed (Figure 4a). However, unlike the result with the smaller 107 nm periodicity in Figure 2c, a 90 min etch time only results in the onset of bilayer structure formation, as shown in (Figure 4b), and well-defined bilayer structures did not appear until the etch time is further increased (e.g., 105 min, Figure 4c), which clearly indicates the retardation of bilayer structure formation with larger pores. When the etching time was further increased to 120 min (Figure 4d), the increase of the bottom-layer thickness was observed, along with clear horizontal etching at different locations in the bottom layer. The

Finally, when the etching time is increased to 150 min, the SiNWs are found to collapse into each other and a very irregular morphology is formed at the bottom layer (Figure 2d).

The spontaneous formation of the bilayer structure was found to significantly improve the SiNW transfer quality, as shown in **Figure 3**. A SiO_2/Si wafer was used as the receiver substrate in this study. In the case of 30-min-etching with a single layer of SiNWs, after transfer only few NW fragments were observed (Figure 3a). By comparison, in the case of 60-min-etching that started to produce the bi-layer structure, long SiNWs can be observed after transfer, but the NW density is still low and NW clusters are observed (Figure 3b). Optimal transfer results were obtained for 90 min etching with well-defined bilayer structures, showing well aligned SiNW arrays with high density and yield (Figure 3c). Finally, when the etching time was increased to 150 min, NW clusters was again observed after transfer with very few individual NWs (Figure 3d).

The correlation between the different etching morphologies and the transfer results clearly suggests that the bilayer structure facilitates the breakage and transfer of individual, well-aligned SiNWs. Analysis of the transferred NW lengths further reveals that they are independent of the etch time. For the samples with etching times of 90 min and 150 min, similar lengths of 6.9 ± 2.8 μm and 6.5 ± 2.7 μm were obtained from

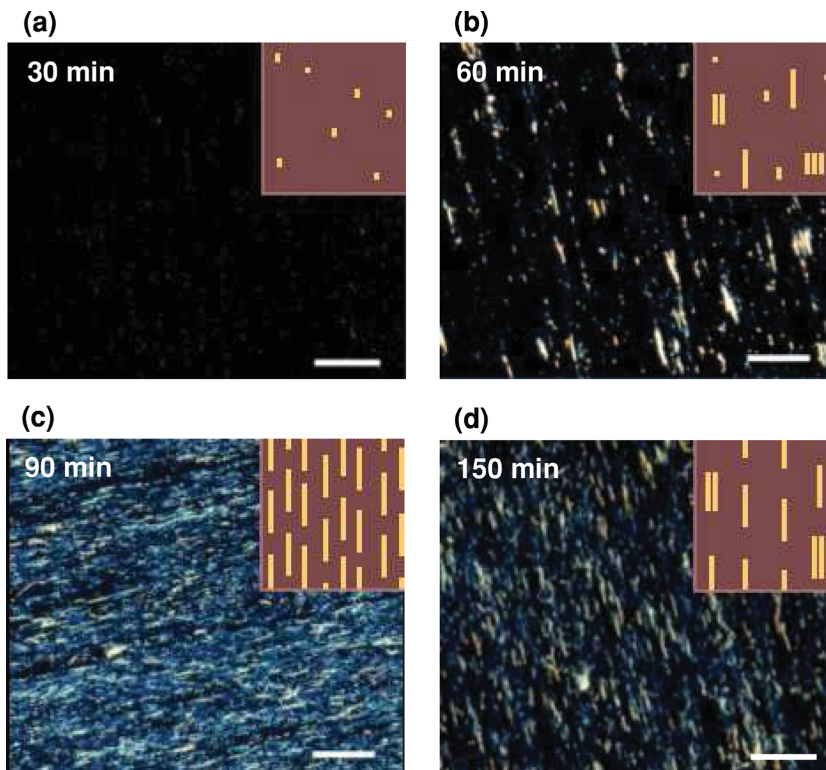

Figure 3. Transfer characteristic of the SiNWs. Dark field optical images of the SiNWs transferred onto SiO_2/Si wafers, for etch time of a) 30 min, b) 60 min, c) 90 min, and d) 150 min. Scale bars: 50 μm. The schematics in each panel illustrate the transfer results.

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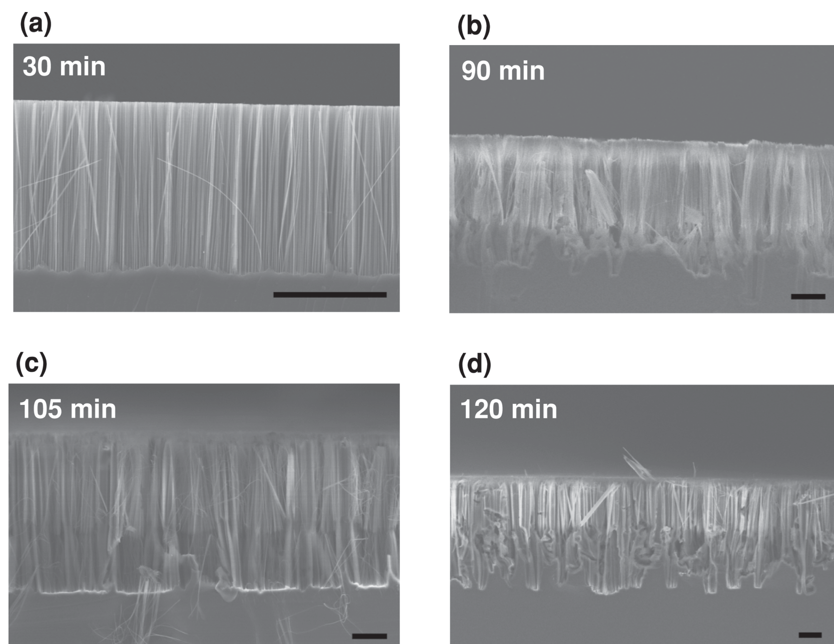
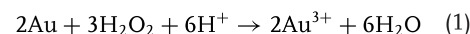


Figure 4. Etching-morphology evolution of the Si wafers during MaCE at different etch times, for Au-mesh-pore periodicity of 251 nm. a) 30 min. b) 90 min. c) 105 min. d) 120 min.

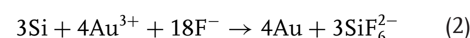
geometry dependence of the etching morphology was summarized in Supporting Information (Figures S2,S3), and suggests that mass transport plays a key role in the bilayer structure formation, as diffusion becomes easier with the increase of Au-mesh pore size.

Based on these results, we hypothesize the bi-structure formation mechanism as follows : 1) diffusion plays a key role in bilayer structure formation; 2) the aspect ratio is the limiting factor for the diffusion; 3) the bilayer structure formation involves horizontal crack formation near the bilayer interface. A phenomenological model based on these assumptions is schematically shown in **Figure 5**.

The Au-catalyzed Si etching can be expressed by two reactions:



$$2Au + 3H_2O_2 + 6H^+ \rightarrow 2Au^{3+} + 6H_2O \quad (1)$$



$$3Si + 4Au^{3+} + 18F^- \rightarrow 4Au + 3SiF_6^{2-} \quad (2)$$

H_2O_2 is reduced with Au oxidation producing Au^{3+} ions in solution (Equation 1; meanwhile Si is oxidized/dissolved by HF, and Au^{3+} ions are reduced back and deposited at Au surface as preferred positions (Equation 2. Following the model of Geyer et al. [23] MaCE using a continuous metal film as catalyst involves first creating a thin porous layer in the Si substrate underneath the metal film; followed by the diffusion of the etching reagents and the byproducts through the

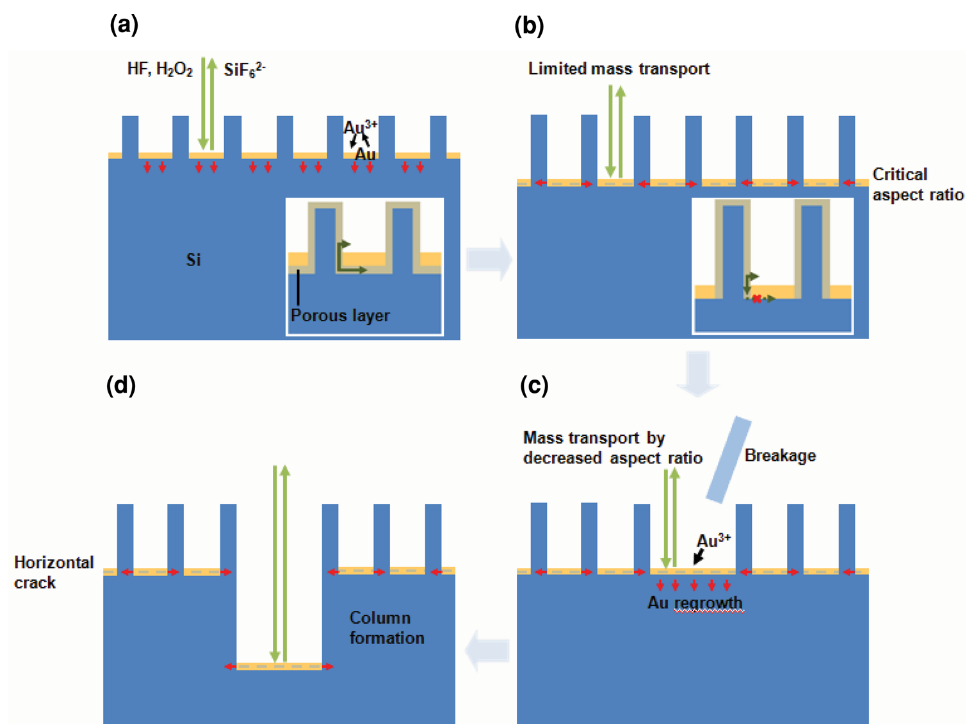


Figure 5. Bilayer structure formation mechanism. Schematic illustrations of the phenomenological model for MaCE, showing a) continuous vertical etching, b) lateral etching due to limited mass transport at critical depth, c) horizontal crack formation by lateral etching, and d) bilayer structure with column formation.

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porous layer towards the openings of the film (i.e., the edge of the Au dots, Figure 5a). If sufficient electrolyte can continue to reach the vertical interface between Au and Si and the reaction byproducts can be effectively removed, Si can be effectively removed and thereby the Au film can sink into the Si substrate leading to continuous vertical etching (Figure 5a).[23] However, as the trench becomes deeper, it becomes harder for fresh reactants to reach underneath the Au film, and lateral etching via breakaway Au particles generated from reaction process (2) will take place at the opening (the edge) of the Au dots (Figure 5b). The critical depth for the electrolyte to reach the vertical Au/Si interface efficiently thus depends on the starting pore size during MaCE (Figure S2, Supporting Information). The lateral etching at the Si sidewalls will create horizontal cracks, and eventually lead to the detachment of SiNWs and the formation of effectively larger Au dots at the detached site (Figure 5c). This process leads to reduced aspect ratio and vertical Au etching can resume again to create thick vertical columns, as schematically illustrated in Figure 5d.

Since the formation of the bilayer structures is accompanied with horizontal crack formation, it should facilitate efficient transfer of SiNWs onto diverse substrates where the breakage of SiNWs from the original substrate is a necessary step. To demonstrate the potential of this approach, SiNW FETs were fabricated on SiO_2/Si or plastic substrates from well-aligned SiNW arrays obtained from contact printing using the Si wafers optimally etched for 90 min (**Figure 6**). The transfer quality on plastics in general was somewhat worse compared to that on SiO_2/Si wafers, possibly due to substrate characteristics such as surface roughness or stickiness, which may be improved by lubricant or surface functionalization.[18] Prior to the characterization of the SiNW-array FETs, performance of single-NW FETs (prepared by the usual drop casting method on SiO_2/Si wafers) were investigated. The SiNW FETs showed p-type transistor behavior with on/off ratio of ≈10^7, subthreshold swing of 607 ± 54 mV dec^{-1}, threshold voltage of −3.8 ± 0.3 V, and transconductance of 20.8 ± 5.0 nS, resulting in a measured electrical mobility of 6.9 ± 2.6 cm^2 V^{-1} s^{-1} (estimated by using the cylinder-on-plane model), as shown in Figure S4, Supporting Information.[24] It is believed that the relatively low mobility and the negative shift of threshold voltage are mainly due to the surface roughness compared to the NW diameter, which can be controlled by optimization of etching system or post etching techniques after NW formation such as surface oxidation and removal.[10,25] Using the transferred SiNW arrays, back-gated SiNW-array FETs were fabricated on SiO_2/Si wafers, and the representative SiNW-array FET showed similar p-type transistor characteristics with threshold voltage of −5.1 V and the transconductance of 267.6 nS, corresponding to ≈13 NWs in each SiNW-array FET (Figures 6a,b), assuming that nanowires are identical and single NW capacitance is maintained.[24] For NWs transferred on to plastic substrates, top-gated SiNW-array FETs were successfully fabricated with similar transistor performances to those on Si wafers (Figures 6c,d), demonstrating the capability of transferring aligned SiNW arrays on diverse substrates using this approach.

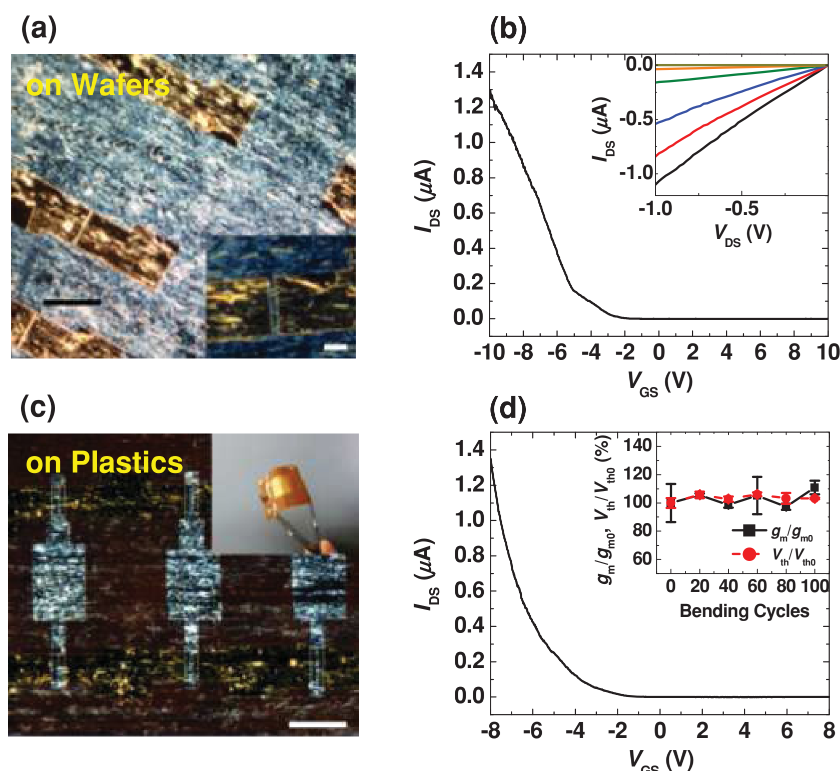

Figure 6. SiNW FETs fabricated on Si or plastic substrates. a,c) Dark field optical images of the SiNW FETs fabricated on a) a SiO_2/Si wafer or c) plastic substrate. Scale bars: 100 μm. Inset of (a): magnified image showing the nanowire array between electrodes. Scale bar: 20 μm. Inset of (c): photograph of the device fabricated on plastic. b,d) Transistor characteristics of the SiNW FETs fabricated on b) Si or d) plastic. V_{DS} = −1 V. Inset of (b): V_{DS}–I_{DS} family curves. V_{GS} = −10 to 0 V in 2 V steps from bottom to top. Inset of (d): transistor performance as a function of bending cycles.

The flexibility of the SiNW-array FETs fabricated on plastic was further tested by monitoring the transistor characteristics with respect to bending cycles. As shown in the inset of Figure 6d, the transistor performance (i.e., transconductance) was maintained for up to 100 cycles, verifying the bending durability of the SiNW-array FETs on plastic and their potential in flexible electronics applications.

Most importantly, we show the MaCE and transfer processes can be repeated using the same starting Si wafer, thus greatly reducing the fabrication cost, which has been a main concern for SiNW based devices versus other approaches based on polymers or organic materials. This capability is demonstrated in **Figure 7**. After the initial MaCE etching (Figure 7a) and SiNW transfer, the top region of the consumed Si wafer was removed and planarized by chemical mechanical polishing (CMP). The SEM image of Figure 7b shows the clean surface of the polished Si wafer, and the overall Si wafer thickness is decreased to ≈50 μm. Subsequently, Au-mesh transfer and MaCE were performed again using the

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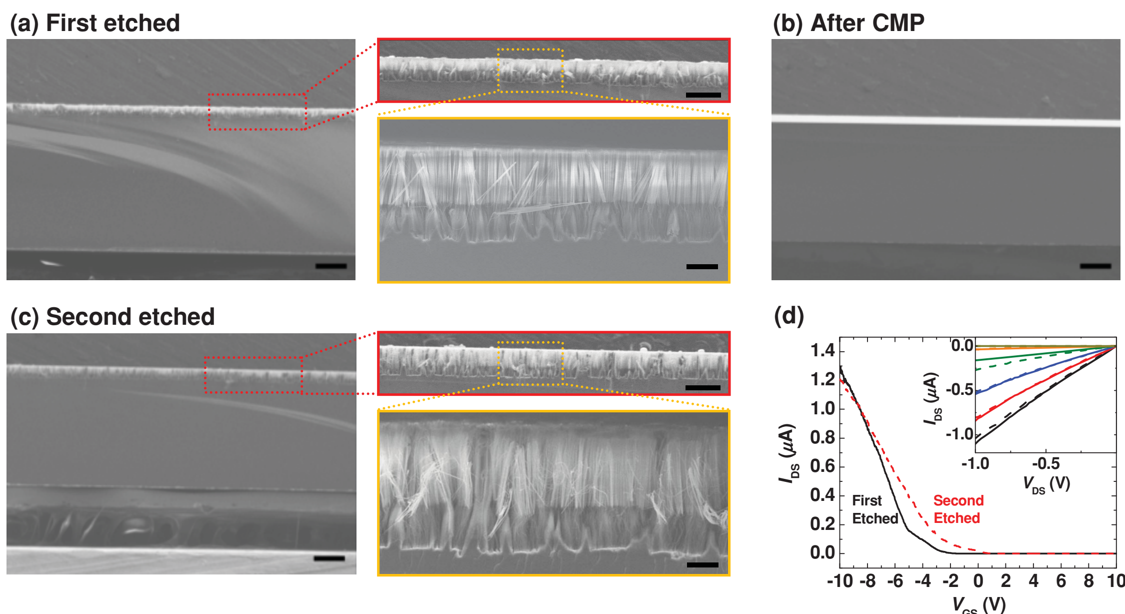

Figure 7. Repeated SiNW fabrication using a single Si wafer. a) SEM images showing first etched SiNWs. Scale bars: 100 μm (left), 50 μm (upper right), and 10 μm (lower right). b) SEM image of the Si wafer cleaned by CMP. Scale bar: 100 μm. c) SEM images showing SiNWs from the second etch. Scale bars: 100 μm (left), 50 μm (upper right), and 10 μm (lower right). d) Comparison of the transistor characteristics for the SiNW FETs prepared in the two etching and transfer processes. $V_{DS} = -1$ V (solid: first etched SiNWs, dash: second etched SiNWs). Inset: V_{DS}–I_{DS} family curves. $V_{GS} = -10$ to 0 V in 2 V steps from bottom to top.

polished Si wafer. The SEM images of Figure 7c show that uniform bilayer-structured SiNWs can still be obtained with similar properties in the recycled Si wafer. Figure 7d shows the transfer curve and *I–V* family curves of the SiNW-array FETs obtained from using the first etched/transferred SiNWs and the second etched/transferred SiNWs from the same Si wafer. Similar transistor characteristics are clearly observed and confirm that SiNW quality is well maintained through the repeated etch/transfer processes.

3. Conclusions

We showed that sub-100 nm single crystalline SiNWs can be mass fabricated by MaCE using Au meshes with controlled pore diameter and periodicity prepared with AAO membranes as templates. The SiNW etching morphology was carefully investigated as functions of etching time and template geometry, and it was found that well-defined bilayer structures can appear spontaneously above critical etching conditions. The bilayer structure formation was closely related with horizontal crack formation running parallel to the Si substrate, and facilitates NW breakage that allows the efficient transfer of aligned NW arrays on diverse substrates. Based on these findings, a protocol was developed and demonstrated that allowed repeated SiNW etch/transfer from the same Si wafer, thus potentially dramatically reducing the cost associated with SiNW based flexible/transparent electronics. Our study broadens strategy spectrum for large scale fabrication and assembly of SiNWs on desired substrates and provides the insight toward the low cost mass production of advanced SiNW electronics.

4. Experimental Section

SiNW Fabrication: (100)-oriented *p*-Si wafers (B-doped, 1–5 Ω cm^{-1}) were used for SiNW fabrication by MaCE. As templates for Au-mesh fabrications, two kinds of AAO membranes (purchased from Synkera Technologies) having the pore periodicities (diameters) of 107 nm (35 nm) and 251 nm (80 nm) were used, with the thickness of 50 μm. 25-nm-thick Au thin films were sputter-deposited onto AAO membranes, and the Au-coated membranes were floated on 3 M KOH solutions to remove the membranes. After rinsing with DI water, the bottom sides were briefly etched by floating the Au meshes on diluted aqua regia solutions ($HCl:HNO_3:H_2O$ = 3:1:40 in volume ratio) in order to remove loosely connected Au particles. After rinsing with DI water, the Au meshes were transferred onto the Si wafers, and the Au-mesh-loaded Si wafers were dried at 100 °C to remove residual water between the Au meshes and the Si wafers. MaCE was performed by using the etching solution of 4.4 M HF and 0.36 M H_2O_2. The etched Si wafers were immersed in aqua regia solutions for Au removal, and subsequently the Si wafers were rinsed with methanol or DI water and dried using a critical point dryer (Automegasamdri 915B, tousimis) or naturally. For the multiple fabrications of SiNWs using single Si wafer, after NW transfer, the top region of the used Si wafer, was briefly removed by a mechanical polisher first, and subsequently smoothened by a chemical mechanical polisher (CMP: IPEC-472, SpeedFam).

SiNW-FET Fabrication: For back-gated FETs, SiO_2/Si wafers (B-doped, 0.001–0.005 Ω cm^{-1}) with 50-nm-thick thermal SiO_2 were used as substrates. The SiNWs were prepared on the wafers, by either direct transfer or drop casting of NW solutions (immersed in an isopropyl alcohol through ultrasonication). As source and drain, 100-nm-thick Au was deposited by evaporation and patterned by conventional photo lithography and lift-off methods. For top-gated FETs, the SiNW arrays were prepared by direct transfer on plastic substrates (Kapton 75H, Dupont). 100-nm-thick Au as source and drain and 100-nm-thick Al as gate were evaporated and patterned. As gate oxide, 25-nm-thick Al_2O_3 was deposited at 150 °C by atomic layer deposition (ALD: OpAL, Oxford).

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Characterizations: Electrical measurements were carried out with a probe station (TTP-4, Desert Cryogenics), using either a customer-built setup or a semiconductor-characterization system (4200-SCS, Keithley). In the bending test, the device size was 2 cm × 2 cm and the bending radius was fixed at 0.8 cm. The direction of bending was parallel to that of the SiNW arrays, and 1-bending cycle means that the device is returned to the flat state after bending with a fixed curvature. The etching morphology of Si wafers were examined using a scanning electron microscopy (SEM: SU8000, Hitachi). The crystallinity and surface roughness of the SiNWs were investigated by a transmission electron microscopy (TEM: JEM-2100F, JEOL). For the TEM-sample preparation, the etched Si wafer was ultrasonicated in methanol and the nanowire suspension was dropped on a carbon-coated Cu grid, and followed by overnight drying of the sample in a vacuum oven.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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