# Thermoelectric Properties of

# Nanostructured Silicon Films

by

## Xiao Guo

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Materials Science and Engineering)
in the University of Michigan
2014

Doctoral Committee:

Assistant Professor Akram I. Boukai, Chair

Assistant Professor Pramod S. Reddy

Professor Dennis Sylvester

Assistant Professor Anish Tuteja

# Acknowledgements

# Table of Contents

# List of Figures

xiii

xviii

# List of Tables

# Abstract

Thermoelectric Properties of Nanostructured Silicon Films

by

Xiao Guo

Chair: Professor Akram I. Boukai

Based on the Seebeck effect, thermoelectric materials can convert temperature heat into electrical energy. Alternatively, based on the Peltier effect, thermoelectric cooling can be achieved by supplying current through thermoelectric materials. Since the best thermoelectric materials are heavily doped semiconductors, and silicon is the most abundant semiconductor on earth, investigation of the thermoelectric properties of strained silicon and ~100 nm thick silicon thin films, and the thermoelectric cooling application of the ~100 nm thick silicon thin film become the focus of this dissertation.

In the Seebeck effect, charge carriers thermally diffuse from a high temperature to low temperature, creating an open circuit voltage potential across the thermoelectric material. However, the application of such technology is mainly limited due to its poor efficiency when competing with the traditional engines; the efficiency depends on the temperature difference and a dimensionless figure of merit, $ZT$. It has been determined

that $ZT=S^2\sigma T/\kappa$, in which $S^2\sigma$ is the power factor, S is the Seebeck coefficient, $\sigma$ is the electrical conductivity, $\kappa$ is the thermal conductivity, and T is the average temperature. The interdependence of S, $\sigma$ and $\kappa$ makes it difficult to improve *ZT* because optimizing one parameter adversely affects another. *ZT* is the key parameter to determine the thermoelectric performance not only in thermoelectric power generation application based on Seebeck effect, but also in thermoelectric cooling application based on Peltier effect. A higher *ZT* results in better thermoelectric performance. It has been proved that silicon nanomesh materials result in a reduced thermal conductivity due to the increased phonon-boundary scattering. This work focuses on using novel nanostructured silicon thin films fabricated by block copolymer lithography to study thermoelectric properties of silicon, and to use these results to estimate the thermoelectric performance of two types of silicon thin films with nanomesh structures.

In the past, improvements of *ZT* in silicon and other semiconductors were made by alloying or nanostructure engineering to reduce the thermal conductivity, while maintaining the power factor ($S^2\sigma$). To improve *ZT* further, we propose to use n-type tensile strained silicon to *enhance the power factor* and to maintain a low thermal conductivity by using a nanomesh structure. It is known that tensile strained silicon exhibits splitting of the six-fold degenerate conduction bands, which leads to decreased inter-valley scattering and increased electron mobility. Thus, its electrical conductivity could be potentially increased. The first part of this dissertation investigates the electrical conductivity and thermopower of 5 nm thick strained silicon and 10 nm thick unstrained silicon thin films with a nanomesh structure over the temperature range of 230-380 K from the $S^2\sigma$ device set. At 300 K, the electrical conductivity of strained silicon with

nanomesh and its power factor were increased by ~400% and ~100%, respectively, compared with those measured in unstrained silicon with nanomesh. The measurements were conducted on a $S^2\sigma$ (power factor) device set consisting of two bulk devices to measure $\sigma$ and S, respectively.

The second part of the dissertation investigates the *ZT* of ~100 nm thick boron-doped silicon nanomesh thin film from a *ZT* device set to study the thermoelectric cooling application of this material. Higher *ZT* results in higher cooling efficiency based on the Peltier effect. Three micro-sized devices were fabricated on the same sample chip to measure the thermopower (S), electrical resistivity ($\rho = 1/\sigma$), and thermal conductivity ($\kappa$), respectively. The thermopower was measured from a 2-thermometer device over a 500 X 500 $\mu m^2$ size nanomesh thin film; the electrical resistivity was measured using the Van der Pauw method with a Greek cross structure; and the thermal conductivity was measured by a $2\omega$ method from a suspended micro-device. The measurement results of the three parameters at 303 K were 435.99 $\mu V/K$, 23.2 $m\Omega\bullet cm$, and 8.51 $W/m\bullet K$, respectively. Thus, *ZT* was determined to be approximately 0.03 at 303 K. Due to the high resistivity of this silicon nanomesh sample, thermal treatments were investigated to reduce the damage-induced degradation of the electrical conductivity, possibly caused by the Schottky barrier at the metal-silicon nanomesh interface or the surface states of the silicon nanomesh. Furthermore, a thermoelectric cooling device composed of equally doped phosphorus and boron nanomesh legs was fabricated using the same material conditions as the one used in the *ZT* device set. It is predicted that the maximum temperature difference this device can generate under vacuum is 3.4 K when the hot side

temperature is kept at 303 K, and that the electrical current required to obtain such cooling effect is 51.3 μA, flowing from the n-type leg towards the p-type leg.

The efforts in the studies of $S^2\sigma$ device set and *ZT* device set both use block copolymer lithography to fabricate nanomesh structures in 5 nm thick strained silicon and ~100 nm thick silicon thin films. The thermoelectric properties of S, σ or ρ ($\rho = 1/\sigma$) are measured in both studies from bulk samples and micro-devices, respectively. Both studies also benefit from the reduction of thermal conductivity due to nanomesh structure in each material, so that the *ZT* is increased. Therefore, better thermoelectric performance in thermoelectric power generation or thermoelectric cooling applications are expected from strained silicon and ~100 nm thick silicon thin films with nanomesh compared with bulk silicon.

# Chapter 1

# Introduction

## 1.1 Thermoelectric energy conversion

Thermoelectric effects can convert heat to electricity and vice versa. The sources of heat can be solar radiation or waste heat from a running automobile engine. In automobile engines, such thermal loss is up to 60-70% of the output energy in the vehicle and it is almost always wasted. Among all the thermoelectric effects, the Seebeck effect associates the power generation from a temperzature gradient on a conductor to an electrical field. [1-2] Classically, in a conductor, charge carriers (electrons or holes) diffuse from the high temperature side to low temperature side, creating an internal electrical field to counteract further charge carrier diffusion until a steady state is reached. A new temperature gradient is required to break the balance and resume the diffusion. This conversion process is environmental friendly without any secondary waste but its applications are mainly limited by low efficiency, which is determined by a dimensionless figure of merit $ZT$ (Equation 1.1).

$$ZT = \frac{S^2\sigma}{\kappa}T$$

<div align="right">(1.1)</div>

*ZT* is a function of Seebeck coefficient or thermopower (S), electrical conductivity (σ), thermal conductivity (κ), and temperature (T). [3] For a given temperature T, the major challenge to maximize *ZT* is that the three parameters S, σ, and κ are interdependent and adversely affect each other. [4] For example, increasing electrical conductivity reduces thermopower due to the negative impact on charge carrier concentration and effective mass; but it increases the electronic part of the thermal conductivity due to the Wiedemann-Franz law. [5-6]

Taking the above three parameters into consideration, the most efficient thermoelectric materials have been heavily doped semiconductors. [4] A thermoelectric module for power generation typically consists of both n-type and p-type semiconductors. They are connected electrically in series and thermally in parallel (Figure 1.1). When a temperature gradient is applied across the module from top down, electrons and holes diffuse in the same direction and generate a current. The ratio of output electrical energy to input thermal energy gives the power generation efficiency. It has been shown that when *ZT*>3 the thermoelectric efficiency is competitive with the ones from traditional heat engines. [7] Numerous studies to improve the efficiency have been performed in the past 50 years. Most endeavors were devoted to reducing thermal conductivity in various semiconductor materials via two major approaches: alloying (section 1.3) and nanostructures (section 1.4). In order to understand how thermal conductivity can be reduced by both methods, detailed background on thermal transport in semiconductors is provided, with an emphasis on silicon (section 1.2).

Later on, with this understanding, two studies were conducted using a nanomesh structure to investigate thermoelectric properties of two types of thin films. The first study was the power factor enhancement in ~5 nm thick strained silicon thin film with nanomesh (section 1.5), and the second study was the *ZT* result of ~100 nm thick boron doped silicon nanomesh thin film, followed by an extended discussion of its potential in thermoelectric cooling application (section 1.6).
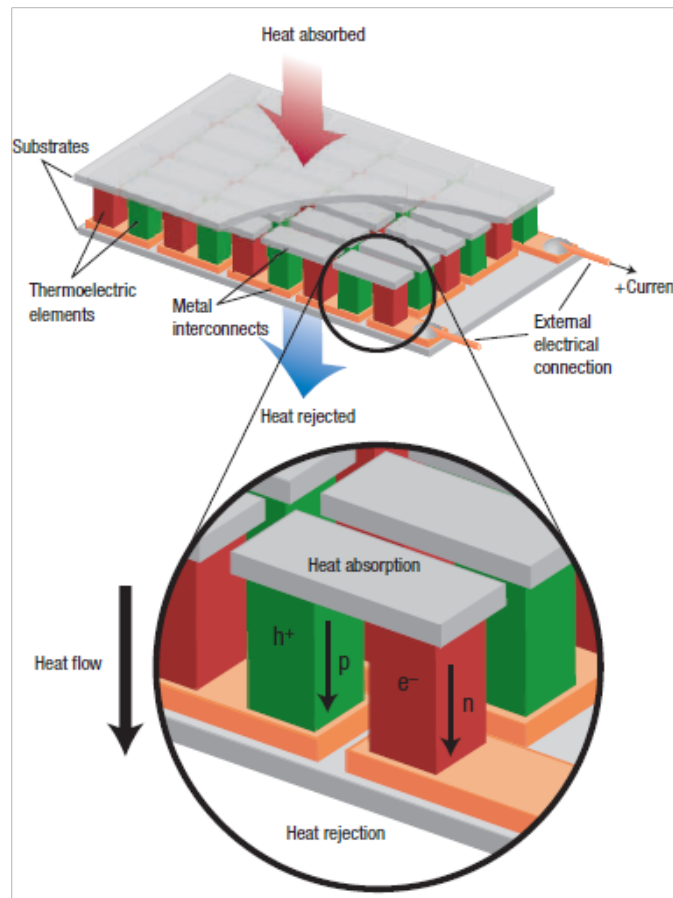


**Figure 1.1 Thermoelectric module functions as power generator or cooler.** [5] **P and n legs are connected electrically in series and thermally in parallel.**

## 1.2 Thermal transport in silicon

Reduction in thermal conductivity has been the most convenient approach to increase thermoelectric efficiency. Comprehensive understanding of thermal conductivity has been developed through extensive studies of heat transfer in various materials. Two carriers are considered responsible for the thermal transport in electrical conductors: charge carriers and phonons (crystalline lattice vibration modes), while only phonons dominate the thermal transport in semiconductors such as silicon.

## 1.2.1 Phonons: classical lattice vibration

Silicon atoms, which are bonded by covalent bonding, vibrate about their mean positions due to thermal fluctuations. Simple vibrations along a one-dimensional atomic lattice have been studied to understand the dispersion relation between phonon wavevectors and frequency (Figure 1.2). [8]
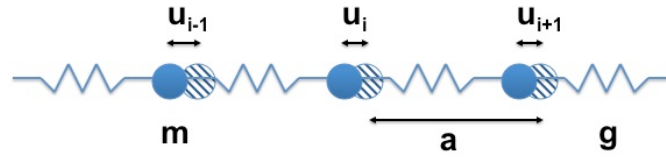


**Figure 1.2 Linear lattice of atoms: cross-hatched spheres represent the silicon atoms at their mean positions.**

The force equation for the $i_{th}$ atom during vibration can be expressed based on the motions of the adjacent $(i+1)_{th}$ and $(i-1)_{th}$ atoms (Equation 1.2).

$$m\frac{d^2u_i}{dt^2} = g(u_{i+1} + u_{i-1} - 2u_i)$$ (1.2)

(m is the mass of the atom; g is the spring constant between atoms; and a is the lattice constant)

A solution to Equation 1.2 can take a general form (Equation 1.3) where k is the wavevector, $k=2\pi/\lambda$, n is an integer, $\omega$ is the angular frequency of lattice wave, and t is the time.

$$u_i = ue^{i(nka-\omega t)} \tag{1.3}$$

Using this ansatz in Equation 1.2, the dispersion relation between wavevector and angular frequency can be derived with a sine function (Equation 1.4, Figure 1.3)

$$\omega = \sqrt{\frac{2g}{m}} \left| \sin\frac{ka}{2} \right| \tag{1.4}$$
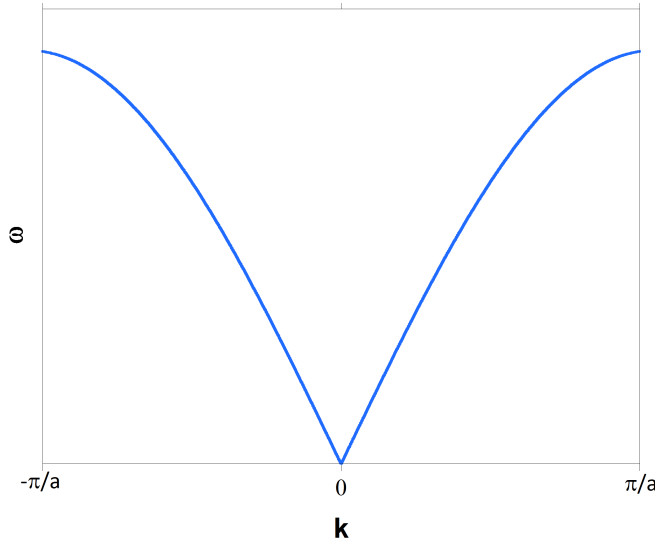


**Figure 1.3 Linear dispersion relation of phonons in silicon. The region $-\pi/a<k<\pi/a$ is the first Brillouin zone. [8]**

In this dispersion relation, the region $-\pi/a<k<\pi/a$ is the first Brillouin zone of silicon in reciprocal space; $-\pi/a$ and $\pi/a$ are the boundaries of the first Brillouin zone. Due to the classical limit of $\lambda_{min}=2a$, the maximum wavevector is $k_{max}= \pi/a$. Any wavevector outside of the first Brillouin zone, however, can be transformed to a wavevector within the first Brillouin zone by subtracting a reciprocal lattice vector G, resulting in the same solution to the elastic wave equation.

5

This analysis can be extended to a 3-D crystal structure. Each silicon atom can be considered as a harmonic oscillator participating in different lattice vibrational modes or phonons in three dimensions. The discrete energies of phonons are given from quantum mechanics (Equation 1.5). [9]

$$E_n = (n + \frac{1}{2})\hbar\omega \qquad (1.5)$$

(n is an integer and ℏ is Planck's constant)

At each quantized energy level there are a certain number of phonon modes available. The total vibrational energy is thus a sum of phonons of all wavevectors and branches in a crystal system. Phonons have acoustic and optical branches based on frequency; for simplicity, Figure 1.3 shows only the acoustic branch. The total energy can be expressed using the number of phonon modes (Equation 1.6) per unit frequency range, i.e. the phonon density of states ($D(\omega)$, Equation 1.7).

$$N = \frac{\frac{4}{3}\pi k^3}{\left(\frac{2\pi}{L}\right)^3} = \frac{k^3 V}{6\pi^2} \qquad (1.6)$$

(L is the 3-D cubic crystal side length; $V=L^3$ is the volume of the crystal)

$$D(\omega) = \frac{dN}{d\omega} = \frac{dN}{dk}\frac{dk}{d\omega} = \frac{Vk^2}{2\pi^2}\frac{dk}{d\omega} \qquad (1.7)$$

The number of modes (N) is defined as the volume of reciprocal space $\frac{4}{3}\pi k^3$ divided by the volume occupied by each phonon mode $\left(\frac{2\pi}{L}\right)^3$. $D(\omega)$ is directly related to the phonon dispersion relation, $\frac{dk}{d\omega}$. A linear Debye approximation (explained in next

section) sufficiently simplifies the dispersion relation for lower energy modes at lower temperature with the exception of some acoustic modes at the first Brillouin zone edge. For a large crystal, the discretization in the wave-vector space is very dense, so the sum of total vibrational energy, $E = \sum_{k,p} (n + \frac{1}{2}) \hbar \omega_{k,p}$, can be converted to an integral over $\omega$ using $D(\omega)$ (eq 1.8).

$$E = \sum_p \int (n + \frac{1}{2}) \hbar \omega_{k,p} D(\omega) d\omega \qquad (1.8)$$

The total energy is the key to understanding the heat capacity ($C_v$) and the thermal conductivity ($\kappa$), and it can be simplified by using the Debye approximation for the dispersion relation, $\dfrac{dk}{d\omega}$.

## 1.2.2 Debye approximation

Two classic models are widely accepted for estimating the heat capacity (or specific heat) in solids: the Einstein model and the Debye model. Unlike the Einstein model that assumes that all the atoms vibrate at the same frequency independently, the Debye model treats thermal vibrations as collective modes of all the atoms confined in a box. The Debye model matches well with experimental results at low temperatures (4-50 K), in which the dependence of heat capacity on temperature T is proportional to $T^3$. The Debye model starts with a linear dispersion relation assumption (Equation 1.9), in which the phonon modes propagate at the group velocity ($v_g$) closely estimated by the speed of sound ($v_s$) in silicon. [10] It also provides a cut-off frequency ($\omega_D$, Equation 1.10) based on

Equations 1.6 and 1.9. [8] The heat capacity ($C_v$) can be derived from the total thermal energy with a simplified density of states $D(\omega)$ (Equations 1.11-1.12).

$$\omega = v_s k \tag{1.9}$$

$$\omega_D = v_s^3 \sqrt[3]{\frac{6\pi N}{V}} \tag{1.10}$$

$$D(\omega) = \frac{V\omega^2}{2\pi^2 v_s^3} \tag{1.11}$$

$$C_v = \frac{\partial E}{\partial T} = \frac{9Nk_B}{V}\left(\frac{T}{\theta_D}\right)^3 \int_0^{\frac{\theta_D}{T}} \frac{x^4}{\left(e^x - 1\right)^2} dx \tag{1.12}$$

($\theta_D = \frac{\hbar v_s}{k_B} \sqrt[3]{\frac{6\pi^2 N}{V}}$ is the Debye temperature derived from $\theta_D k_B = \hbar \omega_D$, $k_B$ is Boltzmann constant and $\hbar$ is Planck's constant)

The Debye temperature can be interpreted as the temperature at which all the phonon modes are activated. The Debye temperature of silicon is reported to be 645 K. [4] When $T<<\theta_D$, $C_v \approx 233Nk_B(T/\theta_D)^3$ for 3-D crystals; when $T>>\theta_D$, $C_v=3Nk_B/V$ is the Dulong-Petit limit (Figure 1.4). [11] The volumetric heat capacity ($C_v$) is an essential parameter in calculating thermal conductivity based on the kinetic theory of gases.

8
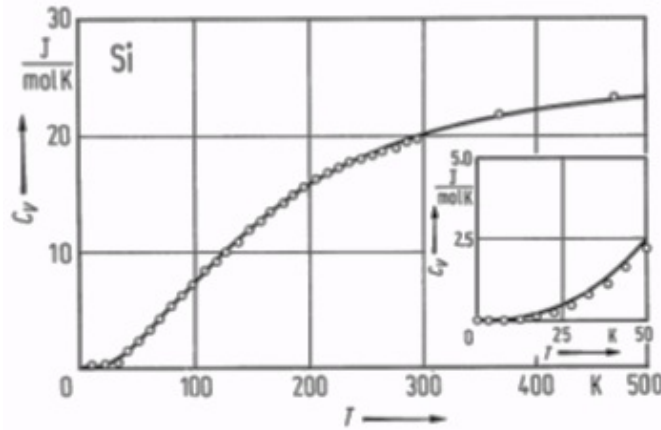
**Figure 1.4 The volumetric heat capacity of crystalline silicon. At low temperatures (T<50 K) heat capacity varies as T³; and at high temperatures (T~500 K), it approaches the Dulong-Petit limit. [11]**

## 1.2.3 Thermal conductivity

Phonons are essentially wave-like lattice vibrations but they can also be treated as particles in order to approximate how heat is transferred in solids. The same kinetic theory used to model a large number of small gas particles traveling in random fashion is applied to heat-carrying phonons moving in a solid under a temperature gradient. Phonons interact with boundaries, imperfections (defects, impurities, etc), and other phonons, to transfer energy. The theory assumes that all the interactions among phonons are in the form of collisions (i.e. phonon-phonon scattering) and that all collisions are elastic and conserve energy. The phonons can also interact with other defects or imperfections in the crystal, as well as the crystal's boundaries (i.e. phonon-imperfection scattering and phonon-boundary scattering). The average time that phonons travel between interactions is defined as the mean free time ($\tau$), and the average distance that phonons travel between interactions is defined as the mean free path (MFP, $\ell$). The

9

thermal conductivity can be estimated based on heat capacity, the speed of sound, and the

phonon mean free path (Equation 1.13).

$$\kappa = \frac{1}{3} C_v v_s \ell \tag{1.13}$$

Essentially, the thermal conductivity is determined by energy-dependent

parameters such as the dispersion relation $\frac{dk}{d\omega}$, which defines density of states $D(\omega)$; the

average group velocity of all phonons $v_g \approx v_s$, and the average phonon mean free time

$\tau = \ell / v_g$. Here, the group velocity is considered to be the same for all phonons; in

reality, short wavelength phonons (with higher energy) travel slower than long

wavelength ones (with lower energy). The phonon mean free time depends on the

scattering mechanisms as expressed by Matthiessen's rule (Equation 1.14). The strongest

scattering determines the limit for thermal conductivity. The phonon scatterings are

highly dependent on material, phonon frequency, and temperature. They will be

discussed in detail below with a focus on silicon; however, the same mechanisms apply

in general to all semiconductors.

$$\frac{1}{\tau} = \frac{1}{\tau_{phonon-phonon}} + \frac{1}{\tau_{phonon-imperfection}} + \frac{1}{\tau_{phonon-boundary}} \tag{1.14}$$

## 1.2.3.1 Phonon-phonon scattering

To simplify the discussion only the scenario of two phonons interacting to form a

third phonon is considered. This interaction leads to two results: a normal process and an

Umklapp process (Figure 1.5). [8]
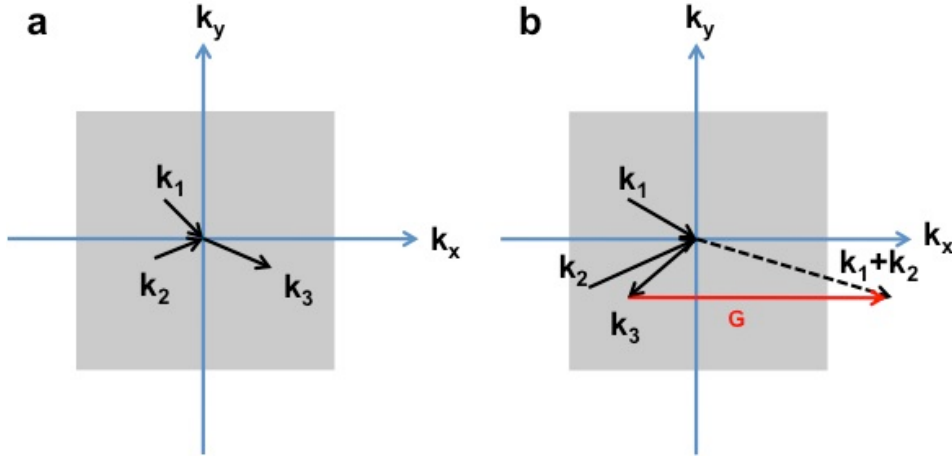
**Figure 1.5 Phonon-phonon interactions in a 2-D lattice plane. (a) Normal process; (b) Umklapp process.**

In a normal process, the wavevector of the third phonon is within the first Brillouin zone so that both energy and phonon momentum (ℏk) are conserved. The interactions following a normal process do not create thermal resistance in silicon; therefore, they do not contribute to heat transfer. In an Umklapp process, the interaction results in a third phonon with a wavevector ($k_1+k_2$) that would extend beyond the first Brillouin zone. But that is physically impossible because the minimum wavelength of a phonon is 2a so the maximum wavevector is limited by $\pi/a$. The third phonon with $\left| k_1 + k_2 \right| > \pi/a$ is brought back to the first Brillouin zone by subtracting a reciprocal vector G. The phonon interaction in an Umklapp process creates thermal resistance due to the lack of momentum conservation and is mainly responsible for the phonon-phonon scattering that affects lattice thermal conductivity at high temperatures where more phonons with larger wavevectors and higher frequencies are activated. The phonon-phonon scattering mean free time is found to relate to phonon angular frequency as

$$1/\tau_{phonon-phonon} \propto \omega^2_{phonon} .$$

## 1.2.3.2 Phonon-imperfection scattering

Imperfections in a crystal such as silicon can be the absence of atoms or the presence of foreign atoms; such imperfections create changes in mass and local strain field that alter the vibrational characteristics of the crystal. Phonons are treated as lattice vibrational waves here. A travelling lattice wave is scattered by imperfections resulting in thermal resistance to heat transfer.

Based on the kinetic theory from Vincenti, the phonon-imperfection scattering mean free time is related to the scattering cross section and velocity of phonons (Equation 1.15). [12]

$$\frac{1}{\tau_{phonon-imperfection}} = \alpha \varphi \eta \upsilon_g \qquad (1.15)$$

($\alpha$ is a constant on the order of unity; $\varphi$ is the scattering cross section; $\eta$ is the number of scattering sites per unit volume or the imperfection density; and $\upsilon_g$ is the phonon group velocity, $\upsilon_g \approx \upsilon_s$)

The scattering cross section $\varphi$ is related to the incident phonon frequency and the imperfection size. If the phonon wavelength ($\lambda$) is larger than imperfection size ($\pi R^2$, R is imperfection radius), the relation approaches the Rayleigh limit, [13] $\varphi \propto \lambda^{-4}$; if $\lambda << \pi R^2$, the scattering cross section is $\varphi = \pi R^2$, independent of $\lambda$. [14] Majumdar proposed a relation between $\varphi$ and $\lambda$ to link these two limits (Equation 1.16). [15]

$$\varphi = \pi R^2 \left( \frac{\chi^4}{\chi^4 + 1} \right) \qquad (1.16)$$

($\chi$ is the size parameter, $\chi = \dfrac{2\pi R}{\lambda}$)

At very low temperatures, most of the excited phonons have low frequency and long wavelength. The phonon-imperfection scattering cross section φ appears very small to the incident phonons, according to the Rayleigh limit; consequently, the mean free time of this type of scattering ($\tau_{phonon-imperfection}$) is long. Therefore, phonon-imperfection scatterings do not dominate at very low temperatures. However, with large amount of imperfections such as dopants or alloying atoms, the imperfection density η can increase and lead to a smaller scattering mean free time to reduce thermal conductivity over a wide temperature range according to Equations 1.13 and 1.15. Otherwise the phonon-impurity scattering starts to dominate thermal conductivity when the temperature increases and more short-wavelength phonons are activated with λ comparable to the imperfection size $\pi R^2$.

### 1.2.3.3 Phonon-boundary scattering

Casimir proved that during phonon-boundary scattering, a boundary wall is not a perfect mirror surface that simply reflects phonons without energy loss; in fact, a boundary wall is a rough surface where phonons are first absorbed then re-radiated based on the local temperature in a diffusive fashion. [16] Diffusive scattering introduces thermal resistance into the crystal and affects the phonon mean free path (MFP). The phonon mean free path (MFP) in this scattering mechanism has a fixed value in an infinite crystal such as bulk silicon. [17] For most of the finite structures such as thin films, the MFP ($\ell$) is determined by the film thickness (L) according to Sondheimer's work (Equations 1.17-1.18). [18]

$$\frac{\ell}{L} = \frac{3}{4}\left(\frac{2-d}{d}\right)\ln\left(\frac{\ell_b}{L}\right) \text{ for } \ell_b \gg L \qquad (1.17)$$

$$\frac{\ell}{L} = \frac{1}{L/\ell_b + 3d/8} \text{ for } \ell_b \ll L \qquad (1.18)$$

(d is the probability of diffuse phonon scattering at boundaries, in perfect diffusive scattering d=1; $\ell_b$ is the MFP in a bulk medium. It is reported that in bulk silicon, $\ell_b$ ~300 nm. [19])

When the film thickness is much smaller than the mean free path of the bulk material, $L \ll \ell_b$, the MFP is on the order of film thickness, $\ell \sim L$. [15] Thermal conductivity is mainly limited by phonon-boundary scattering at low temperature (T<20 K in bulk silicon) since most short wavelength phonons are still not activated and phonon-imperfection scattering is not dominant.

The above described three major scattering mechanisms that explain how the thermal resistance in bulk silicon is produced and how the thermal conductivity is determined. At very low temperatures (T<20 K), phonon-boundary scattering dominates. Thermal conductivity has a $T^3$ temperature dependence based on the Debye approximation. As temperature increases, phonons with wavelengths close to the imperfection size determine the mean free path (MFP). At high temperatures, more phonons with larger wavevectors and shorter wavelengths scatter to increase thermal resistance and thus reduce thermal conductivity.

Unlike the situation in bulk silicon, nanostructures can further tailor the thermal conductivity based on phonon-boundary scattering over a wide temperature range. This behavior can also be explained from the dependence of the cumulative thermal conductivity on the MFP distribution. Boundary roughness can also be important.

## 1.2.3.4 Thermal conductivity from lattice dynamics

Dames and Chen [20-21] treated phonons as lattice waves and derived the contribution from each phonon mean free path (MFP) to the total thermal conductivity in bulk silicon (Equations 1.19-1.20). The MFP is a function of wavelength, $\lambda$.

$$d\kappa\left(\ell_{k\lambda}\right) = \frac{1}{3}C_{V,k\lambda}\nu_{g,k\lambda}\ell_{k\lambda} \tag{1.19}$$

$$\kappa\left(\ell\right) = \frac{1}{N}\sum_{k\lambda}^{\ell_{k\lambda}<\ell}d\kappa\left(\ell_{k\lambda}\right) \tag{1.20}$$

($C_{v,k\lambda}$, $\nu_{g,k\lambda}$ and $\iota_{k\lambda}$ are the heat capacity, group velocity, and MFP associated with the phonon mode $k\lambda$)

From the above differential and cumulative thermal conductivity analysis, phonons with thermal wavelength $\lambda < 6$ nm carry all the heat at 277 K in bulk silicon, and its thermal conductivity is ~150 W/m•K. The MFPs in silicon range from 1 nm to 10 μm, with more than 67% of MFPs above 100 nm. It has significant meaning for nanostructures in silicon; as the critical dimension ($\ell_c$, the smallest in-plane size in silicon) is lowered, more MFPs are reduced by phonon-boundary scattering since the MFPs approaches $\ell_c$; in turn, phonon-boundary scattering limits the thermal conductivity over the temperature range 100-500 K, in agreement with experimental results. [21]

15
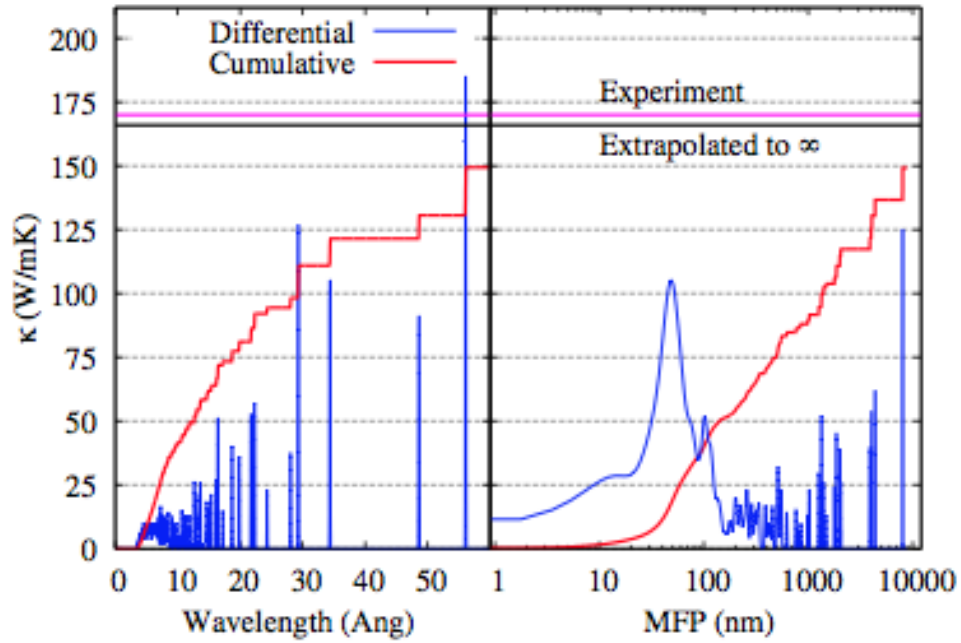
**Figure 1.6 Differential and cumulative contributions of phonons to the thermal conductivity at 277 K. The left plot shows the dependence on wavelength; the right plot shows the dependence on MFP. The differential and cumulative thermal conductivities are shown in blue and red, respectively. [21]**

Thermal conductivity in silicon has been reduced in the past decades based on engineering principles to increase phonon-imperfection scattering and phonon-boundary scattering. Different approaches employed to reduce thermal conductivity in order to increase the figure of merit *ZT* are discussed below.

## 1.3 Thermal conductivity reduction through alloying

Before the 1990s, the major focus in thermoelectric research was to search for bulk material systems that exhibited high *ZT* within a wide temperature regime. Such systems as $Bi_2Te_3$, PbTe, $Si_{1-y}Ge_y$ and $Zn_4Sb_3$ were widely investigated, especially in the high temperature range (>600 °C). Alloying was the first attempt to tailor the thermal conductivity in those materials to increase *ZT*. By adding atoms with heavier atomic

mass, the lattice thermal conductivity (phonon contribution) was lowered due to anharmonic phonon scattering. Specifically, the imperfection density η (alloying atom density) can increase and lead to a smaller phonon-imperfection scattering mean free time to reduce thermal conductivity (see section 1.2.3.2). Studies have shown $Bi_2Te_3$ based alloys (($Bi_{1-x}Sb_x)_2(Te_{1-x}Se_x)_3$) with *ZT* near 1 at room temperature [22-23] (Figure 1.7). Historically, *ZT*~1 was referred to as the 'alloy limit' [24] for the past 30 years, though there was no theoretical prediction that it should be the upper limit of thermoelectric performance. [25] Later on, nanostructure engineering has been found to be a promising approach to improve *ZT*.
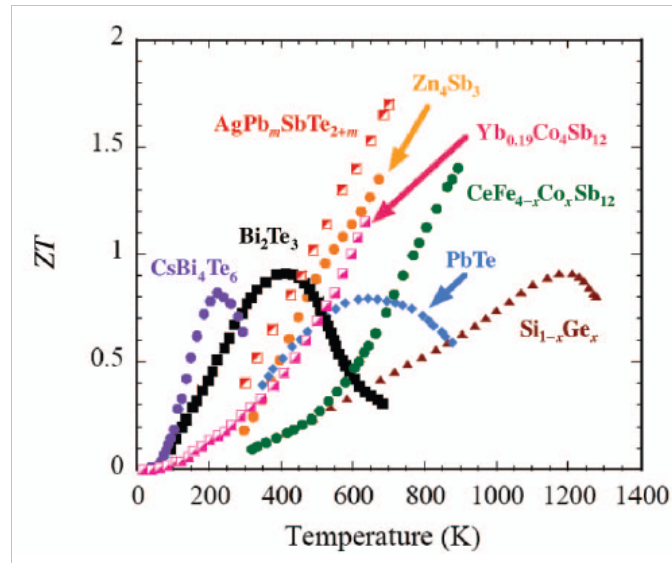


**Figure 1.7 Temperature dependence of figure of merit *ZT* for several bulk thermoelectric material systems. [25]**

## 1.4 Thermal conductivity reduction through nanostructures

Experiments starting in the 1990s using 'phonon-glass electron-crystal' engineering on traditional thermoelectric materials have improved thermoelectric performance. The idea is to suppress thermal conductivity by reducing the dimensions of

17

materials in structures such as superlattices, thin films, or quantum wires, while retaining bulk-like electrical conductivity. The minimum limit of thermal conductivity in bulk semiconductors was considered to be ~1 W/m•K found in amorphous $SiO_x$ since its heat transfer was considered as a random walk. [5] Nanostructures have made it possible to reach such a limit in single crystal materials without the need to make an amorphous material.

This nanostructure-engineering was proposed to describe the ideal thermoelectric material, one that scatters phonons but not charge carriers. One method to accomplish this is to exploit the difference between the electron and phonon mean free paths (MFPs). For example, the electron mean free path (MFP) in highly doped bulk silicon at room temperature is 5-10 nm, [3, 26] but 67% of its phonon MFPs are above 100 nm (see section 1.2.3.4). [21] Therefore, silicon with nanostructures approaching a critical dimension of ~10nm should reduce thermal conductivity by increasing phonon-boundary scattering without significantly affecting electrical conductivity, leading to an increase in *ZT*. This idea was first examined on the earliest and most investigated materials.

L.D. Hicks [6, 27] showed theoretically that *ZT* of $Bi_2Te_3$ could be increased dramatically from bulk material by using quantum well or quantum wires. Experimentally, it was shown that *ZT* was increased from 0.5 in bulk $Bi_2Te_3$ with Sb, Se alloys to approximately 2.4 in a $Bi_2Te_3/Se_2Te_3$ superlattice at room temperature. [28] T.C. Harman [29] also discovered that by growing a PbTe/Te superlattice, *ZT* of PbTe was improved by approximately 40.5% (Figure 1.8). Past efforts in nanostructure-engineering have been focused on rare semiconductors. Few investigations on earth abundant elements such as silicon have been performed.
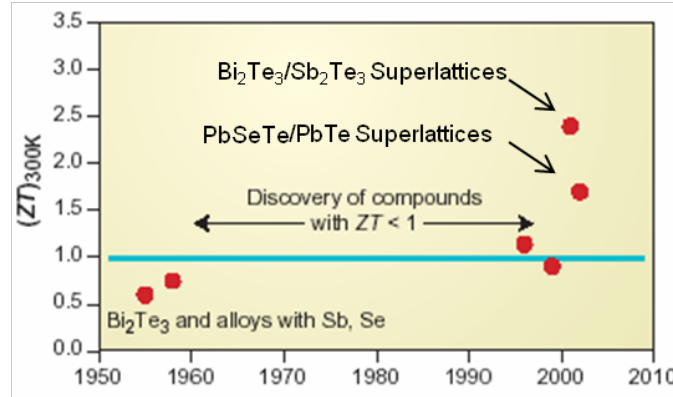
**Figure 1.8 Temperature dependence of figure of merit *ZT* for superlattice systems. [28]**

Recent research has shown that nanostructure-engineering in both silicon nanowires and nanomesh structures exhibited extremely low thermal conductivities, about two orders of magnitude lower than that of bulk silicon. Such drastic reduction in thermal conductivity made a positive impact on silicon's *ZT* value. Bulk silicon has *ZT*~0.01 at 300 K due to a high thermal conductivity (~150 W/m·K). A. I. Boukai showed *ZT*~1 at 200 K in 20 nm wide silicon nanowires made by the superlattice nanowire pattern transfer (SNAP) method; [4] SNAP reduced the thermal conductivity by a factor of 75 (Figure 1.9).
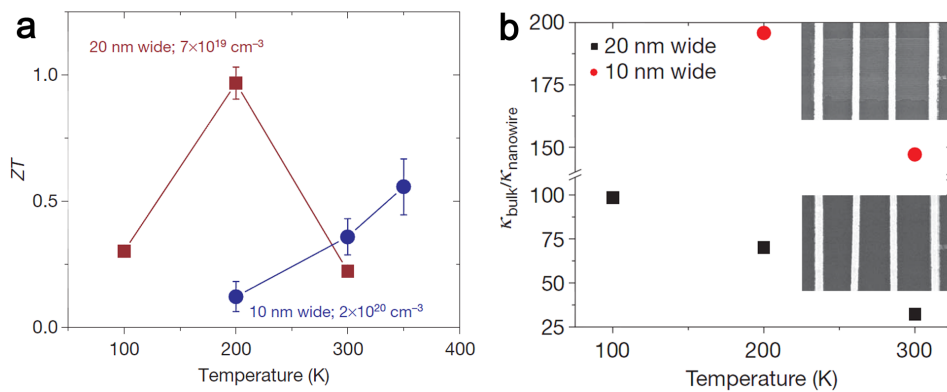


**Figure 1.9 10 nm and 20 nm wide silicon nanowire fabricated by SNAP method. (a) *ZT* of heavily doped nanowires as a function of temperature; (b) The ratio of thermal conductivity in bulk silicon to thermal conductivity in silicon nanowires as a function of temperature. [4]**

J.Y. Tang et al [22] studied holey silicon nanostructures fabricated by nanosphere lithography (NSL) or block copolymer lithography (BCP) in 100nm thick silicon films. Reduction in hole pitch to 55 nm further reduced the thermal conductivity to ~2 W/m·K. The *ZT* measured in this holey structure was 0.4 at 300 K. J.K. Yu et al [23] demonstrated similar nanomesh structures (Figure 1.10, a, b, e) fabricated by e-beam lithography (EBM) and superlattice nanowire pattern transfer (SNAP). The nanomesh silicon and holey silicon are essentially two terminologies for the same structure. The lowest thermal conductivity obtained was 1.9 W/m·K (Figure 1.10, d) for nanomesh structures by SNAP, while the electrical conductivity was preserved close to that of bulk silicon at a similar doping level (Figure 1.10, c).



| | T (nm) | W (nm) | D (nm) | P (nm) | Surface/Volume (nm$^{-1}$) |
|---|---|---|---|---|---|
| TF | 25 | – | – | – | 0.08 |
| EBM | 22 | 115 | 270 | 385 | 0.07 |
| NWA | 20 | 28 | – | – | 0.17 |
| NM 1 | 22 | 23 | 11 | 34 | 0.12 |
| NM 2 | 22 | 18 | 16 | 34 | 0.14 |
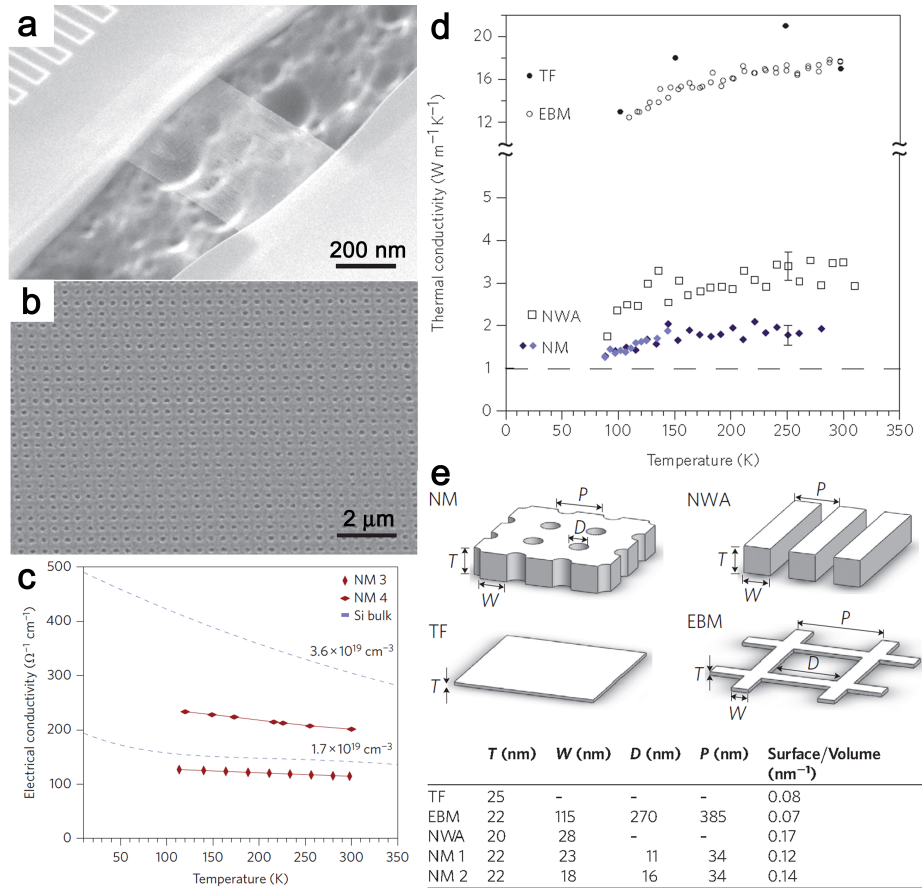
**Figure 1.10 Characterization and thermal conductivity results of different nanomesh structures. (a) SEM image of fully suspended thermal microdevice; (b) SEM image of long-**

**range ordered nanomesh film; (c) Electrical conductivity of two boron doped nanomesh films compared with boron doped bulk silicon film with similar doping level (2x10$^{19}$ atoms/cm$^3$); (d) Thermal conductivity of different nanostructures as a function of temperature. TF (thin film) and EBM (large mesh fabricated by e-beam lithography) show similar high conductivity; NWA (nanowire arrays) show smaller thermal conductivity due to the size effect in two dimensions and a large surface to volume ratio; NM1 and NM2 (nanomeshes) have the lowest thermal conductivity resulting from their three dimensional heat impedance. [23]**

These results indicated that phonon propagation was significantly reduced in nanostructure-engineered materials, while the electrical conductivity ($\sigma$) or even the power factor ($S^2\sigma$) was comparable to that of the bulk silicon. The impedance in heat transfer was found to be the main reason for enhancement of *ZT*. The next step is to further enhance *ZT* by increasing the power factor, while retaining low thermal conductivity by using nanostructures such as nanomesh. The work in this thesis describes efforts to enhance the power factor of tensile strained silicon to uncover its potential in improving *ZT* and to perform a cooling measurement on silicon nanomesh devices for the first time.

## 1.5 Power factor enhancement through strained silicon with nanomesh

Tensile strained silicon has been used in n-channel MOSFETs (NMOS) to increase electron mobility through the channel. This idea was first used in Intel's 90 nm process to increase device performance by more than 10% in 2000. [30-32] This improvement in electron mobility also leads to increased electrical conductivity. Therefore strain-engineered silicon can be a solution to increase the power factor. One of the objectives in this dissertation is to employ tensile strained silicon with nanomesh to maximize *ZT* both by enhancing the power factor and reducing the thermal conductivity. This is also the first time that tensile strained silicon is studied for its thermoelectric

properties. In the following, the method of tensile strained silicon thin film fabrication is introduced then the strain effects on silicon's bandstructure are studied in detail.

## 1.5.1 Tensile strained silicon fabrication

There are mainly two ways to introduce tensile strain in silicon. The conventional technique in CMOS devices is to deposit a tensile strained film such as $SiN_x$ on top of a silicon film to elongate silicon's lattice constant; another method is to obtain strained silicon from a $Si/Si_{1-x}Ge_x$ bilayer, then transfer the strained silicon film to an oxide ($SiO_x$) on silicon wafer, which can be further processed for various applications. In this study, we used strained silicon films obtained from the second method.

$Si_{1-x}Ge_x$ has an identical crystal structure (diamond) with silicon, but a slightly larger lattice constant. Its lattice constant varies as a function of Ge atomic content (Equation 1.21, Figure 1.11). [33] When silicon atoms are epitaxially deposited layer by layer on top of a relaxed $Si_{1-x}Ge_x$ substrate, the film goes through a pseudomorphic growth up to a critical thickness $h_c$ (Equation 1.22). [34] The bonds between silicon atoms stretch to match the $Si_{1-x}Ge_x$'s lattice constant, building tensile strain in the film.

$$c(Si_{1-x}Ge_x)=0.002733x^2+0.01992x+0.5431(nm) \tag{1.21}$$

(x stands for the percentage of germanium in the composition; $c(Si_{1-x}Ge_x)$ is lattice constant of $Si_{1-x}Ge_x$)

$$h_c = \frac{b}{8\pi f} \frac{\left(1-\nu\cos^2\theta\right)}{(1+\nu)\cos\lambda}\left(\ln\frac{h_c}{b}+1\right) \tag{1.22}$$

22

($h_c$ is the film critical thickness; $\theta$ is the angle between the dislocation line and its Burgers vector; $\lambda$ is the angle between the slip direction and the direction in the film plane which is perpendicular to the line of intersection of the slip plane and the interface)
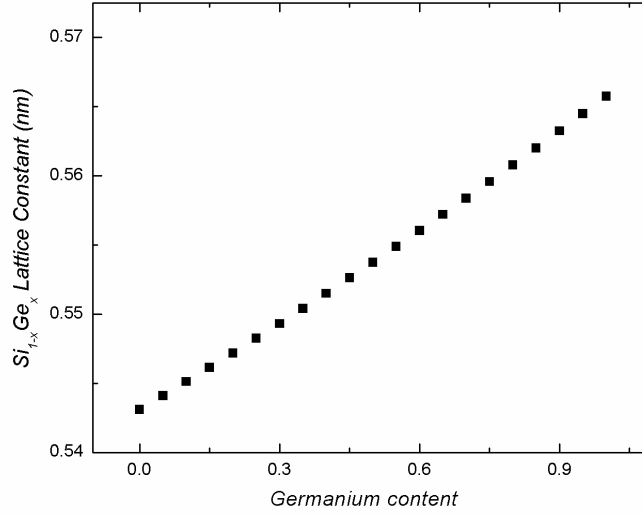


**Figure 1.11 Lattice constant of $Si_{1-x}Ge_x$ as a function of germanium content.**

A $Si/Si_{1-x}Ge_x$ bilayer is difficult to process. It is also critical to preserve tensile strain in the silicon film for future micromachining while removing the $Si_{1-x}Ge_x$ layer. J. L. Hoyt developed a bond and etch back technology to fabricate ultra-thin strained silicon on insulator in 2003. [35] First, ultra-high vacuum chemical vapor deposition (UHVCVD) was employed to deposit a $Si_{1-x}Ge_x$ layer, with Ge content graded at 10% per μm and a final content of 29%, on an 8 in <100> silicon wafer. One μm of relaxed $Si_{0.71}Ge_{0.29}$ remained on top of the SiGe graded layer. Then a stack of layers were deposited epitaxially as follows: strained silicon layer (10 nm) as etch-stop, relaxed $Si_{0.71}Ge_{0.29}$ layer to induce strain, and the final strained silicon layer (13-14 nm) (Figure 1.12, a).

To transfer and retain the strained silicon layer, another thermal oxide on an 8 in <100> silicon wafer was bonded with the top strained silicon layer from the first wafer at

room temperature and then annealed at high temperature to strengthen the bonding (Figure 1.12, b). Chemical mechanical polishing (CMP) and various chemical etching methods were used to remove the silicon handle and the rest of the stacked layers from the first wafer to stop at the last strained silicon film (Figure 1.12, c). [36-37] The final structure had an 13-14 nm strained silicon on thermal oxide on silicon wafer (SSOI, Figure 1.12, d). The thickness uniformity standard deviation of the strained silicon thin film was around 3.6% (Figure 1.13). The presence of tensile strain can affect the electrical properties in silicon.
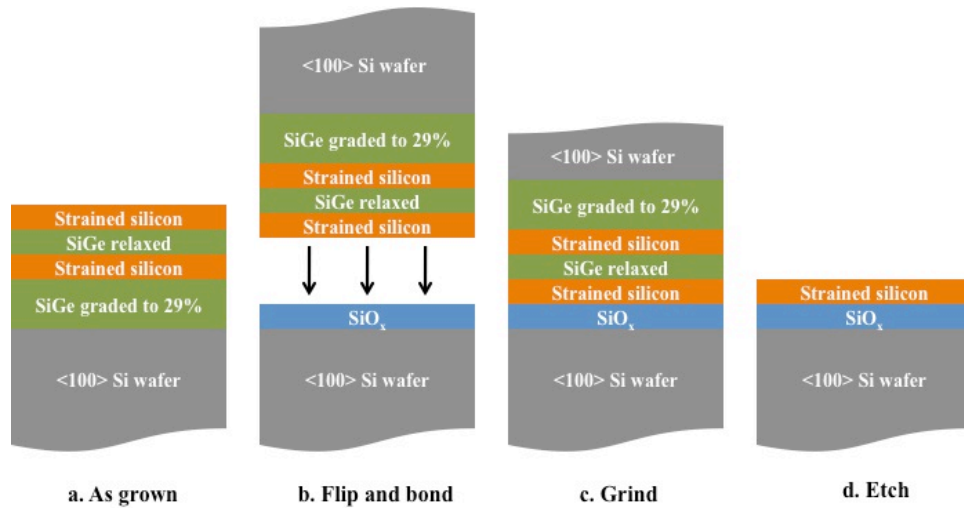


**Figure 1.12 Bond and etch back technology to obtain ultra-thin strained silicon thin film. The plot is modified from reference [35].**
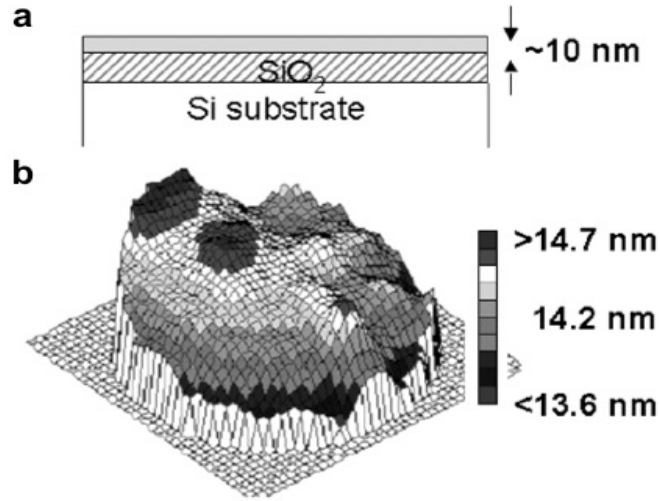
**Figure 1.13 Strained silicon on insulator. (a) The final structure after etch stop at the strained silicon thin film; (b) Surface roughness of the top strained silicon thin film.** [35]

## 1.5.2 Effects of tensile strain on silicon bandstructure

Tensile strain affects silicon's bandstructure. As an indirect semiconductor (Figure 1.14), its conduction band minima are located along {100} directions with six-fold degeneracy near the X point. The valence band minima consist of a heavy-hole band (HH), a light hole band (LH) and a spin-orbit-split hole band (SO) at the $\Gamma$ point. The HH and LH bands are degenerate at K=0 in unstrained silicon, separated from the SO band by 44 meV. [38]

Figure 1.14 Silicon bandstructure. [39]

The tensile strain introduces two major effects for silicon's electrical properties. First, the conduction band minima are split into two groups. Two of the degenerate bands ($\Delta_2$) are lowered from original energy level ($E_c$), and apart from the rest of the bands ($\Delta_4$) by roughly 180 meV. This band offset is much larger than silicon's room temperature thermal energy ($k_BT$=25.6 meV) so electron inter-valley scattering is greatly reduced thus increasing electron mobility. While in the valence band, the light hole band (LH) stays above the heavy-hole band (HH) at the Γ point, with a heavy-hole like effective mass (Figure 1.15). Such arrangement reduces hole mobility.

Second, tensile strain also causes conduction band curvature to increase. As a result, electron effective mass is reduced (Equation 1.23), electron mobility is enhanced (Equation 1.24), and electrical conductivity is enhanced (Equation 1.25). Overall the tensile strain favors electron conduction. [35-36]

$$m^* = \hbar^2 \left( \frac{d^2E}{dK_z^2} \right)^{-1} \tag{1.23}$$

(m* is electron effective mass; ℏ is Planck's constant, $6.63 \times 10^{-34}$ J•s)

26

$$\mu = \frac{e}{m^*}\tau \; \text{[40]} \qquad (1.24)$$

($\mu$ is the electron mobility; $\tau$ is the electron average scattering time associated with various scattering mechanisms)

$$\sigma = ne\mu \; \text{[5]} \qquad (1.25)$$

($\sigma$ is electrical conductivity; n is electron concentration)
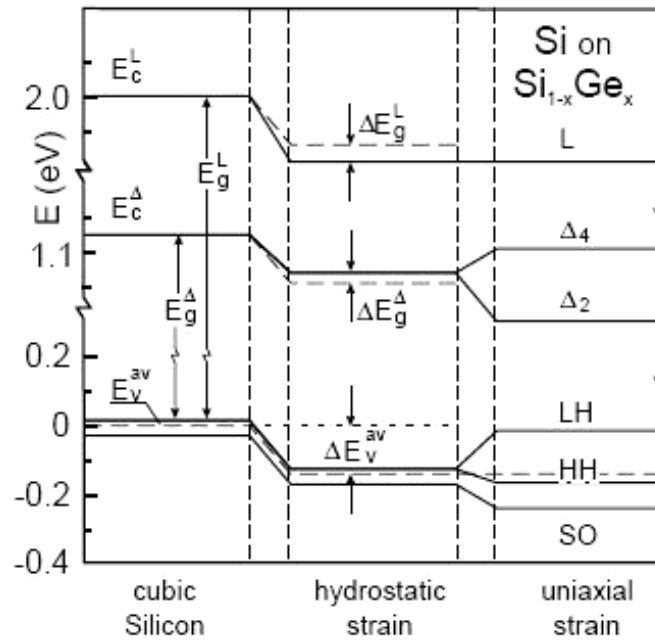


**Figure 1.15 Effect of hydrostatic and uniaxial strain on silicon conduction band and valence band by pseudomorphicly growing Si on $Si_{0.7}Ge_{0.3}$ substrate. [40]**

Both effects on bandstructure favor electron conduction in tensile strained silicon. Ismail et al proved that electron mobility was increased by 200% in uniaxially strained silicon compared with unstrained silicon at 295 K (Figure 1.16). [41]
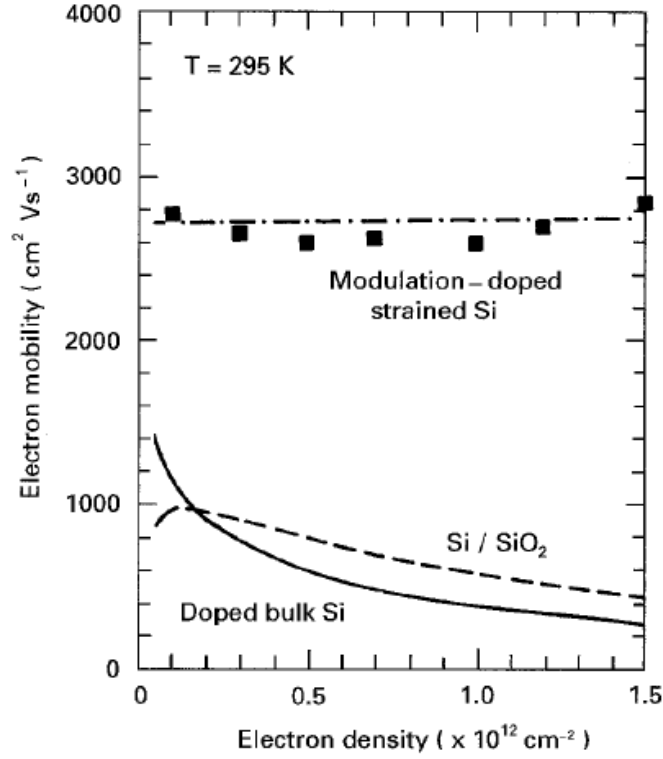
**Figure 1.16 The electron mobility dependence on electron density of modulation-doped strained silicon, doped bulk silicon and Si / SiO₂ inversion layer. [41]**

In order to study the power factor of tensile strained silicon thin film with nanomesh, two devices are fabricated to measure electrical conductivity and thermopower, respectively. These two devices are referred as "$S^2\sigma$ device set" in the future chapters 2, 3, and 5.

## 1.6 Thermoelectric cooling study with silicon nanomesh thin film

Thermoelectrics generally have two major applications: power generation and thermoelectric cooling. The determination of *ZT* of a specific material is the key to understanding the performance of the material in either of the applications.

This work also includes an investigation of *ZT* of an ~100 nm thick silicon nanomesh thin film. Three devices were fabricated to measure thermopower, electrical resistivity, and thermal conductivity from the same chip. These three devices are referred to below as a "*ZT* device set". This silicon thin film with nanomesh was then investigated for thermoelectric cooling applications.

## 1.6.1 Introduction to thermoelectric cooling (TEC)

Thermolelectric cooling employs the Peltier effect, and it is the reverse of the Seebeck effect. It differs from the conventional cooling methods, such as the one used in refrigerators, in the following ways: it uses solid-state devices without any moving parts; it does not release ozone-depleting chlorofluorocarbons (CFCs), so that it is more environmental friendly; and it can achieve very precise temperature control ($\Delta T < \pm 0.1$ °C). Since its efficiency is low compared to that of the conventional cooling methods, TEC mostly operates in conditions where the conventional refrigeration fails to function, such as counteracting unevenly distributed thermal radiation on satellites and spacecrafts, reducing the thermal noise on astronomical telescopes and high-end digital cameras, and maintaining stable functions on electronic components.

The Peltier effect describes how a current through a semiconductor material can generate a temperature gradient across its ends. When a voltage potential is applied to a metal-semiconductor-metal component from left to right, the current is flowing in the same direction (Figure 1.17). In an n-type semiconductor, such as phosphorus doped silicon, electrons in the metal need to overcome an energy barrier ($E_C$-$E_F$) to flow into the conduction band of the semiconductor from its right end (Figure 1.17, a). The electrons

with highest energy can travel through such barrier and flow effortlessly (no energy barrier) into the metal on the left end. Heat is conducted from the right end to the left by an electrical current accompanied by a thermal current. Similarly, in a p-type semiconductor, such as boron-doped silicon, holes need to overcome an energy barrier ($E_F$-$E_V$) to travel from left to right from the metal to semiconductor (Figure 1.17, b). Holes with the highest energy are depleted from the left end and accumulated on the right end. [42]
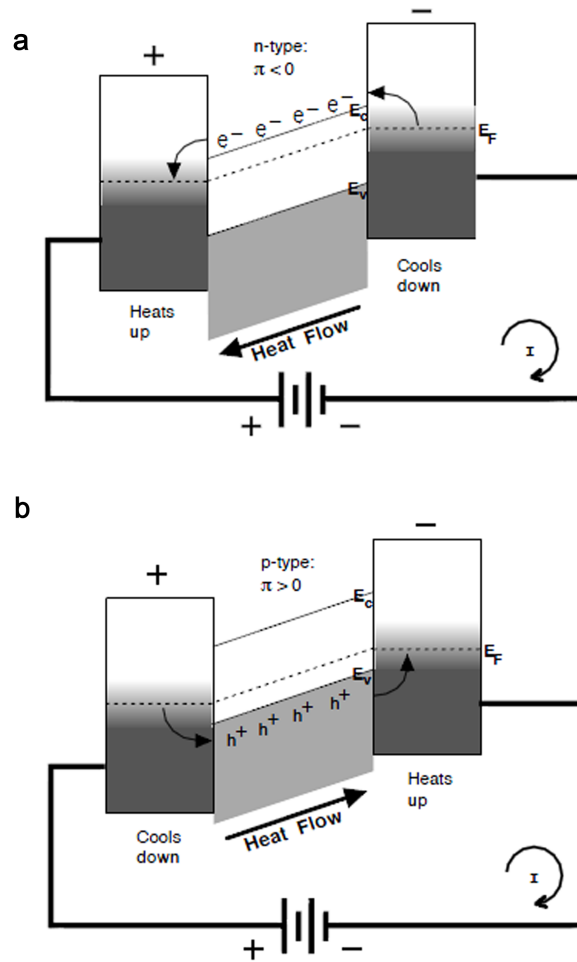


**Figure 1.17 Illustrations of Peltier effect on a metal-semiconductor-metal component. (a) Electrons with the highest energy overcome the energy barrier at the right end, and deplete the region while removing the heat from the left end to the right end; (b) Holes with the highest energy flow in the opposite direction, carrying heat from the left end to the right end. [42]**

The magnitude of the Peltier effect is expressed by the Peltier coefficient, $Q = \Pi \cdot I$, where Q is thermal power, and I is the electrical current. $\Pi$ is essentially a measure of the ratio of the thermal current to the electrical current in a material, and is related to the thermopower (S) by the 2nd Thompson relation: $\Pi = S \cdot T$, where T is the absolute temperature.

The best Peltier cooling effect can be achieved by using a two-leg structure, where one leg is n-type and the other is p-type semiconductor with an optimized device figure of merit $Z_d T$ (Equation 1.26), [43-44] considering the semiconductors, and all parasitic effects to their junction and the device.

$$Z_d T = \frac{S_d^2 T}{R_d K_d} \tag{1.26}$$

($S_d$ is the sum of the absolute thermopower from both the n-type and p-type semiconductors; $R_d$ is the device total electrical resistance including the resistance of both semiconductors and the contact resistance; $K_d$ is the total thermal conductance including the thermal conductance for both semiconductors, the contact thermal conductance, the thermocouple or bonding wire thermal conductance, and the thermal radiation)

The temperature decreases at the p-n junction, and increases on the other end when the current is flowing from the n leg to the p leg, as shown in Figure 1.18. The temperature difference created within this device is $\Delta T = T_h - T_c$ ($T_h$ and $T_c$ are temperatures for the hot and cold ends, respectively), and it is an important criterion regarding the cooling device's performance of the cooling device.
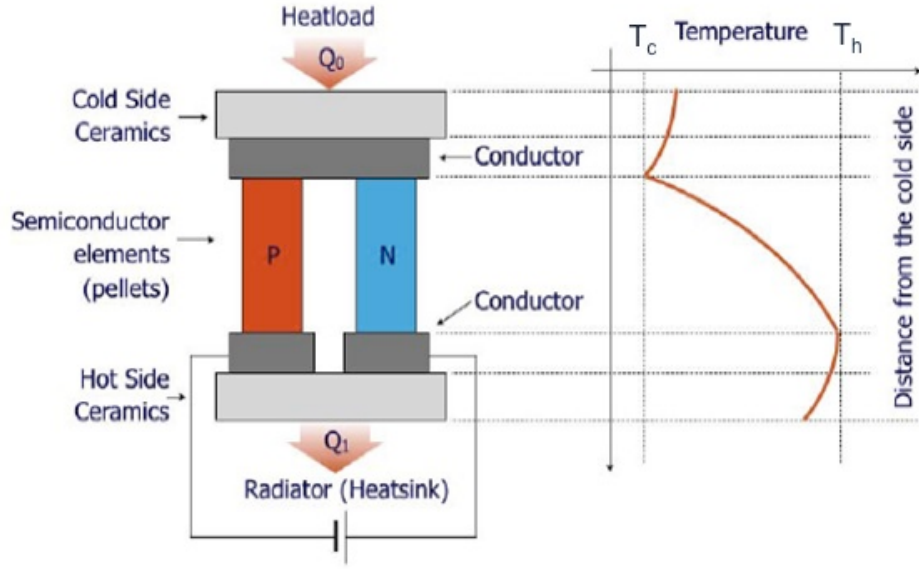
**Figure 1.18 Thermoelectric cooling module and temperature profile.** [43]

With good metal-semiconductor contacts and proper device design and temperature control, the parasitic effects can be negligible; then, $R_d$ and $K_d$ are determined by only the n- and p- type semiconductors, i.e. $R_d=R_p+R_n$, and $K_d=K_p+K_n$.

The optimization of *ZT* is the key to maximize the thermoelectric cooling efficiency $\phi$ (Figure 1.19) and $\Delta T$ generated by the Peltier effect in the device. [42] It can be achieved by minimizing the product of $R_d$ and $K_d$, which can be satisfied by adjusting the device geometry, and electrical and thermal properties (Equation 1.27), essentially to obtain $R_nK_p=R_pK_n$.

$$\rho_p\kappa_n\frac{\ell_p A_n}{\ell_n A_p}=\rho_n\kappa_p\frac{\ell_n A_p}{\ell_p A_n} \tag{1.27}$$

($\rho$ is the electrical resistivity; $\kappa$ is the thermal conductivity; $\ell$ is the length; and A is the cross-sectional area of the semiconductor)
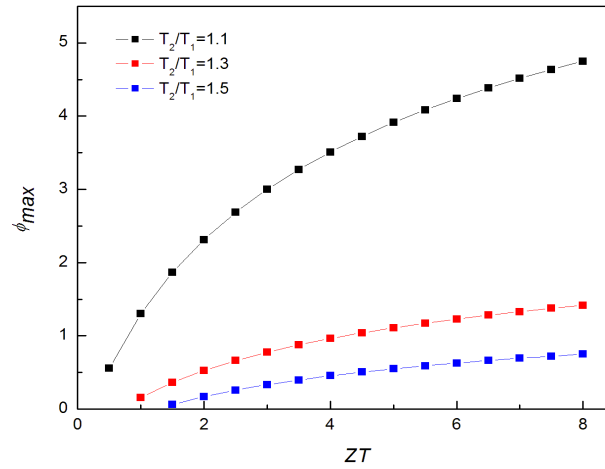
**Figure 1.19 The dependence of the thermoelectric cooling efficiency $\phi_{max}$ on the figure of merit *ZT* for different values of the hot (T$_2$)/cold (T$_1$) temperature ratio in the device.**

## 1.6.2 Thermoelectric cooling devices

Typically, $Bi_2Te_3$-alloys are one of the most common materials used in commercial thermoelectric coolers. These devices are composed of n and p-type semiconductor legs, which are connected electrically in series and thermally in parallel (Figure 1.20). The legs are sandwiched between two thermally conductive plates. [43]
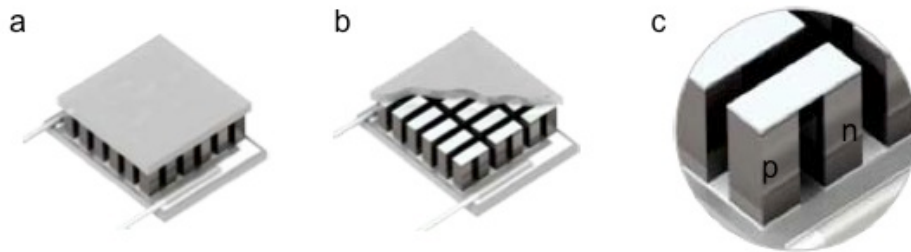


**Figure 1.20 A commercial thermoelectric cooler. (a) Perspective view of an assembled single-stage thermoelectric cooler; (b) Partially cut-away view showing the arrangement of the n- and p- type semiconductor legs sandwiched between two thermally conductive plates; (c) Close-up view of the legs that are electrically connected by copper thin films. [43]**

The maximum temperature difference ($\Delta$T) these devices can achieve is ~70 K, at 300 K ambient temperature in a vacuum. [43] Even better cooling effect can be achieved

by stacking multiple stages where the heat can be delivered to the bottom of the device when current is supplied in a way that heat is absorbed on the top.

In addition to studies on commercial thermoelectric coolers, the cooling properties can also be investigated by fabricating novel micro devices, such as a suspended device with ~100 nm thick n and p-type silicon nanomesh thin films in this study (Figure 1.21).
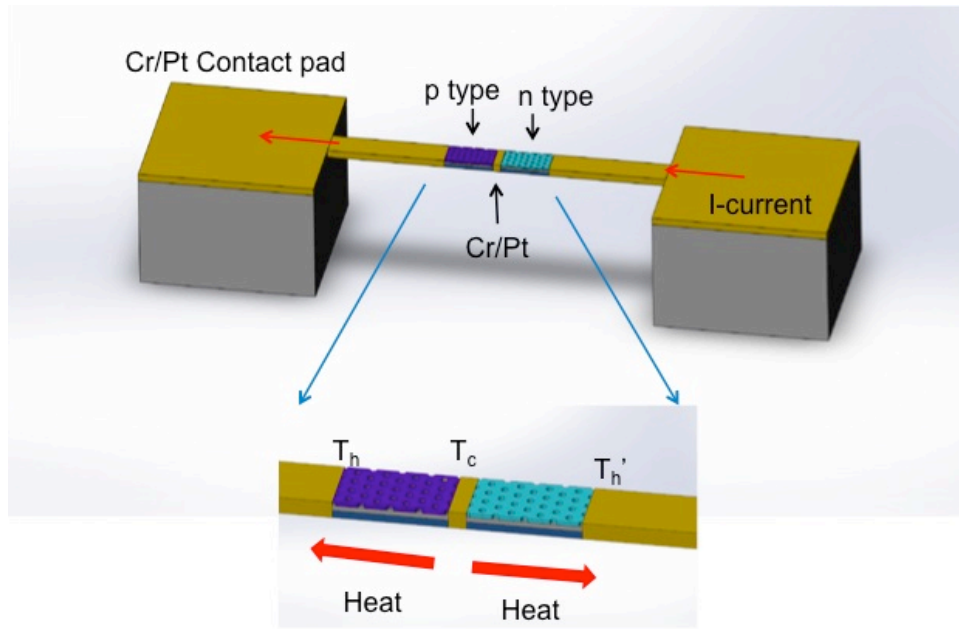


**Figure 1.21 Sketch of thermoelectric cooling of a suspended device with silicon nanomesh thin films.**

When the current goes from right to left in Figure 1.21, heat is transported away from the center of the p-n junction by electrons and holes. The silicon legs are fully suspended from a SOI sample to avoid parasitic thermal leakage. This study focuses first on measuring the figure of merit *ZT* from the doped silicon nanomesh thin film, then on investigating the cooling properties using this material in the device shown in Figure 1.21. The maximum temperature difference this device can create is the main interest.

## 1.6.3 Thermoelectric cooling measurements in a silicon nanomesh device

In order to achieve the better cooling, n and p-type silicon nanomesh thin films used in this device have the same geometry (length, width, and thickness), the same doping level with boron and phosphorus, respectively, to yield very similar electrical resistivity, and the same nanostructure to obtain comparable thermal conductivity.

The rate of cooling ($q_c$) from the heat source, or the cold side, is determined by the thermoelectric properties of this two-leg device, such as S, R and K (Equation 1.28). [42, 44]

$$q_c = (S_p + |S_n|)IT_c - K_d(T_h - T_c) - \frac{1}{2}I^2R_d \tag{1.28}$$

($S_p$ is the thermopower of the p-type silicon nanomesh and it satisfies the condition $S_p > 0$; $S_n$ is the thermopower of the n-type silicon nanomesh and it satisfies the condition $S_n < 0$; I is the current sent through the heat source; $T_c$ is the cold temperature in the middle of the p-n junction; and $T_h$ is the hot temperature at the contact pads on the bulk substrate)

The temperature difference ($\Delta T$) between the center of the p-n junction and the contact pads reaches its maximum ($\Delta T_{max}$, Equation 1.29) when the experimental conditions are adjusted so that $q_c \approx 0$. The corresponding current required for this optimization is $I^*$ (Equation 1.30). [42, 44]

$$\Delta T_{max} = \frac{(S_p + |S_n|)^2}{2K_dR_d}T_c^2 = \frac{1}{2}Z_dT_c^2 \tag{1.29}$$

$$I^* = \frac{S_p + |S_n|}{R_d}T_c \tag{1.30}$$

The thermoelectric cooling properties of silicon nanomesh thin films, such as $\Delta T_{max}$ and $I^*$, are studied in this work based on the *ZT* device set measurement results from a boron doped silicon nanomesh thin film sample.

## 1.7 Summary and organization of this thesis

In this chapter, we discussed the importance of thermoelectrics and the recent development in improving their efficiencies. Research to improve *ZT* has progressed from (a) investigating various semiconductor systems over a wide temperature range to (b) alloying in bulk materials and then to (c) nanostructure-engineering. Recent investigations in nanostructure-engineering (nanomesh and nanowires) have already revealed the reduction of thermal conductivity in silicon thin films. In this thesis, we first propose to use strain engineering to further increase electrical conductivity. As a result, power factor is enhanced for better thermoelectric performance potentially in thermoelectric power generation or cooling applications. Then the value of *ZT* is measured from an ~100 nm thick silicon nanomesh thin film, and the potential of silicon nanomesh thin films in thermoelectric cooling applications is discussed. The organization of the thesis is as follows.

In chapter 2, we describe the fabrication processes for (a) a device set for measuring the power factor of strained silicon with nanomesh and (b) a device set for measuring the *ZT* of the silicon nanomesh. These device sets are referred to below as the $S^2\sigma$ (power factor) device set and the *ZT* device set, respectively. First, the nanomesh fabrication method, including block copolymer lithography, is described in detail for both device sets, with different nanomesh transfer techniques due to the difference in the film

thickness. Second, fabrication of the $S^2\sigma$ device set is described. The $S^2\sigma$ device set consists of two devices to measure electrical conductivity and thermopower on a bulk sample, respectively; these two parameters are used to determine the power factor of the strained silicon with nanomesh. Third, fabrication of the *ZT* device set is described. The *ZT* device set consists of three devices on a single SOI chip to measure the thermopower, electrical resistivity, and thermal conductivity, respectively; these three parameters are used to determine the *ZT* value of the ~100 nm thick silicon nanomesh thin film around 303 K.

In chapter 3, the characterization techniques and metrology are described for the $S^2\sigma$ and *ZT* device sets. We report measurements of the nanomesh morphologies in both device sets; the tensile strain level in the top silicon film in the $S^2\sigma$ device set; the film thickness and silicon nanomesh porosity of the *ZT* device set; and the boron doping profile in the ~100 nm thick silicon thin film in the *ZT* device set. We then describe different measurement methods used in both devices and provide preliminary analysis.

In chapter 4, we present the measurement results of electrical conductivity and thermopower of strained silicon thin film with nanomesh from the $S^2\sigma$ device set and discuss the results: the electrical conductivity of strained silicon with nanomesh (SSNM) is five times as large as that of the unstrained silicon with nanomesh (USNM), while its thermopower is reduced by 36.5%; however, the power factor of SSNM is enhanced by ~100% compared to USNM around room temperature.

In the final chapter, we present the results of the three thermoelectric properties (S, $\rho$, and $\kappa$) and the figure of merit *ZT* of the ~100 nm thick boron doped silicon nanomesh thin film at 303 K. We also discuss two thermal treatments to improve the

electrical conductivity of the nanomesh thin film after it has been damaged by the etching related processing. In the end, the thermoelectric cooling application of this film is investigated by calculating the maximum temperature difference (3.4 K) and the current required to achieve it (51.3 μA) from a suspended device with a p-n junction composed of ~100 nm thick boron and phosphorus doped silicon nanomesh thin films.

## 1.8 Reference

[1] D.K.C. MacDonald, *Thermoelectricity: An Introduction to the Principles,* New York, Wiley, 1962.

[2] G. Mahan, B. Sales & J. Sharp, *Physics Today* **50** 42–47 (1997).

[3] K. Hippalgaonkar, B.L. Huang, R.K. Chen, K. Sawyer, P. Ercius and A. Majumdar, *Nano Letters* **10** 4341-4348 (2010).

[4] A.I. Boukai, Y. Bunimovich, J.T. Kheli, J.K. Yu, W.A. Goddard III & J.R. Heath, *Nature* **451** 168-171 (2008).

[5] G.J. Snyder and E.S. Toberer, *Nature Materials* **7** 105-114 (2008).

[6] L.D. Hicks and M.S. Dresselhaus, *Physical Review B* **47** 16631-16634 (1993).

[7] C.B. Vining, *Nature Materials* **8** 83-85 (2009).

[8] C. Kittel, *Introduction to solid state physics*. John Wiley & Sons, Inc., 1996.

[9] D. Bohm, *Quantum Theory*. Englewood Cliffs, N.J.: Prentice-Hall, 1951.

[10] J. Callaway, *Physical Review* **113** 1046–1051 (1959).

[11] H.M. Kagaya and T. Soma, *Phys. Stat. Sol. (b)* **127** 5–7 (1985).

[12] W.G. Vincenti and C.H. Kruger, *Introduction to Physical GasDynamics,* Robert Krieger Publ., New York, 1977.

[13] Rayleigh, Lord, *Theory of Sound,* Macmillan and Co., London, 1896.

[14] D. Walton,  and E. J. Lee, *Physical Review* **157** 724-729 (1967).

[15] A. Majumdar, *Journal of Heat Transfer* **115** 7–16 (1993).

[16] H. Casimir, *Physica V* **6** 495–500 (1938).

[17] Y.S. Touloukian, *Thermal Physical Properties of Matter, Vol 2: Thermal Conductivity-Nonmentallic Solids*. New York: Plenum Press, 1970.

[18] E.H. Sondheimer, *Advances in Physics* **1** 1-42 (1952).

[19] Y.S. Ju and K.E. Goodson, *Applied Physics Letters* **74** 3005-3007 (1999).

[20] C. Dames and G. Chen, *Thermoelectrics Handbook: Macro to Nano-Structured Materials*, D. Rowe, Ed, 2005.

[21] K. Esfarjani, G. Chen, and H. Stokes, *Physical Review B* **84** 1–11(2011).

[22] J.Y, Tang, H.T. Wang, D.H. Lee, M. Fardy, Z.Y. Huo, T.P. Russell, and P.D. Yang, *Nano Letters* **10** 4279-4283 (2010).

[23] J.K. Yu, S. Mitrovic, D. Tham, J. Varghese and J.R. Heath, *Nature Nanotechnology* **5** 718 -721 (2010).

[24] W. Kim, J. Zide, A. Gossard, D. Klenov, S. Stemmer, A. Shakouri, and A. Majumdar, *Physical Review Letters* **96** 045901-1 (2006).

[25] T.M. Tritt and M.A. Subramanian, *MRS Bulletin* **31** 188-198 (2006).

[26] A.I. Hochbaum, R. Chen, R.D. Delgado, W. Liang, E.C. Garnett, M. Najarian, A. Majumdar and P. Yang, *Nature* **451** 163-167 (2008).

[27] L.D. Hicks and M.S. Dresselhaus, *Physical Review B* **47** 12727–12731(1993).

[28] A. Majumdar, *Science* **303** 777-778 (2004).

[29] T.C. Harman, D.L. Spears, and M.P. Walsh, *Journal of Electronic Materials* **28** L1–L4 (1999).

[30] S. Thompson, et al., *International Electron Devices Meeting Technical Digest*, 61-64 (2002).

[31] T. Ghani, et al., *International Electron Devices Meeting Technical Digest*, 978-980 (2003).

[32] K. Mistry, et al., *Symposium on VLSI Technology Digest of Technical Papers*, 50-51 (2004).

[33] J.P. Dismukes, L. Ekstrom, and R.J. Paff, *Journal of Physical Chemistry* **68** 3021-3027 (1964).

[34] J.W. Matthews and A.E. Blakeslee, *Journal of Crystal Growth* **27** 118-125 (1974).

[35] T.S. Drake, C. NÍ Chleirigh, M.L. Lee, A.J. Pitera, E.A. Fitzgerald, D.A. Antoniadis, D.H. Anjum, J. Li, R. Hull, N. Klymko, and J.L. Hoyt, *Journal of Electronic Materials* **32** 972-975 (2003).

[36] G.E. Pikus and G.L. Bir, *Symmetry and Strain-Induced Effects in Semiconductors,* New York, Wiley, 1974.

[37] T.K. Carns, M.O. Tanner, and K.L. Wang, *Journal of Electrochemical Society* **142** 1260-1266 (1995).

[38] L. Börnstein, *Physics of Group IV Elements and III-V Compounds*, Berlin, Springer, 1982.

[39] S. Krishnamurti, A. Sher and A. Chen, *Applied Physics Letters* **47** 160-162 (1985).

[40] F. Schäffler**,** *Semiconductor Science and Technology* **12** 1515–1549 (1997).

[41] K. ISMAIL, B.S. MEYERSON, *Journal of Materials Science: Materials in Electronics* **6** 306-310 (1995).

[42] E.J. Winder and A.B. Ellis, *Journal of Chemical Education* **73** 940-946 (1996).

[43] Thermoelectric Cooler Basics, TEC Microsystems GmbH, Schwarzschildstrasse 3, 12489 Berlin, Germany.

[44] T.C. Harman, P.J. Taylor, M.P. Walsh and B.E. LaForge, Science **297** 2229-2232 (2002)

# Chapter 2

# Fabrication of S²σ and *ZT* device sets

In this chapter, we describe the fabrication processes for the S²σ device set (for the power factor measurement of strained silicon with nanomesh) and the *ZT* device set (for the *ZT* measurement of ~100 nm thick silicon nanomesh). First, the common technology used to fabricate nanomesh, block copolymer lithography (BCP), is described here with an introduction to block copolymer self-assembly, the procedures used to apply the technique, and the nanoscale pattern transfer details. Then, the device fabrication processes are provided for the S²σ and *ZT* device sets, respectively. The most commonly used fabrication techniques are photolithography, metal deposition, and plasma etching such as reactive ion etching (RIE) and deep reactive ion etching (DRIE).

## 2.1 Block copolymer lithography (BCP)

The BCP process has mainly two steps: (a) nanomesh patterns are generated via block copolymer self-assembly on the samples and (b) nanomesh patterns are transferred to the underlying silicon thin films via RIE or DRIE. The nanomesh pattern used in the S²σ device set for the strained silicon thin film has 18 nm diameter and 36 nm pitch, but

in *ZT* device set it has 40 nm diameter and 80 nm pitch. Therefore, different block copolymers solutions are used for each device set. Before describing the BCP process, its self-assembly mechanism is first introduced below.

### 2.1.1 Block copolymer self-assembly

Block copolymers are made up of distinct blocks or subunits. Each block is composed of the same chemical species, and all blocks are covalently bonded into a single unit. Block copolymers are known for their ability to self-assemble into various periodic structures. Linear diblock, PS-b-PMMA (PS-polystyrene; PMMA-poly(methyl methacrylate)), was used in this study. Its structural motifs after self-assembly can be spherical micelles, cylindrical micelles, tubular micelles and lamellae (Figure 2.1). [1-2] Each nanostructure can be obtained by controlling the relative volume fraction of PS and PMMA.
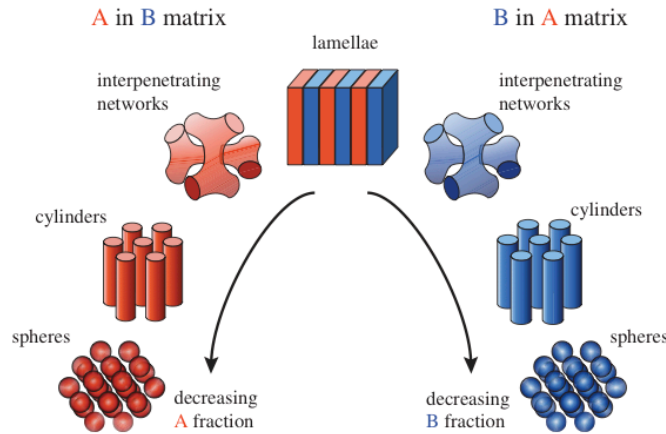


**Figure 2.1 Morphologies after linear diblock copolymer self-assembly. The motifs gradually change based on block A and B's volume fraction.** [1]

The phase diagram demonstrates the mechanism of self-assembly from block A and B (Figure 2.2) in an A-b-B block copolymer. [1, 3-4] The y-axis represents the product

of the degree of polymerization (N) and the Florry-Huggins interaction parameter ($\chi$); the x-axis represents the volume fraction ($f$) of block A in the total melt. The y-axis value indicates whether the self-assembly is disordered or ordered, since $\chi$ represents the immiscibility of adjacent A and B type polymers. If $\chi$ is low in the melt, there is less repulsion between unlike species; consequently, diblock copolymers turn into a disordered state. On the other hand, if $\chi$ is high in the melt, unlike species strongly repel each other to form periodically ordered phases such as a hexagonal lattice of cylindrical micelles, hexagonally-close packed or face-centered spherical micelles, and gyroid or lamellar layers. The value of $f$ from the x-axis determines the specific structural motif as a result of minimized free energy.
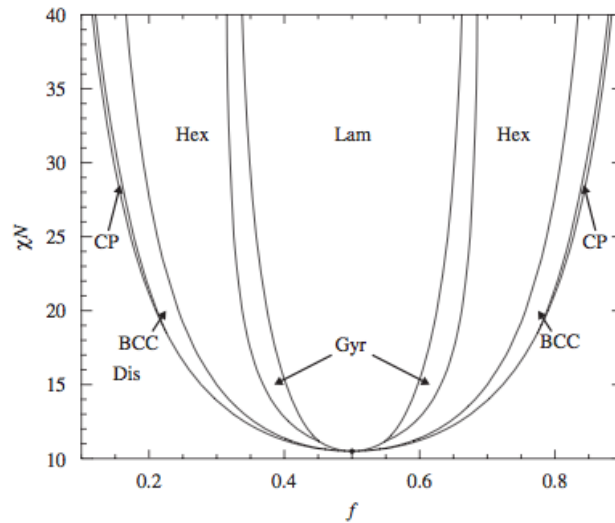


**Figure 2.2 Phase diagram of linear diblock copolymer. Ordered phases are labeled as close-packed (CP) and body-centered cubic (BCC) spherical micelles; hexagonal cylindrical micelles (Hex); lamellae (Lam); gyroid (Gyr). [1,3-4]**

These nanostructured patterns can be used as templates to engineer electronic devices. [5-7] Here a cylindrical pattern was used to introduce a nanomesh into underlying silicon thin films. Striking progress has been made by researchers to solve the challenges

of long-range order and pattern transfer [8-15]. After selectively removing cylinder fillings, in this case the PMMA, RIE was performed to transfer nanomesh patterns using a copolymer matrix as a template (details described below).  In order to obtain a suitable nanomesh pattern, it was important to first clean and hydroxylate the silicon surface and then perform a necessary brush treatment to ensure the proper vertical alignment during the copolymer self-assembly.

## 2.1.2 Pre-BCP brush treatment

The starting materials in the $S^2\sigma$ device sets were strained silicon on insulator substrates (SSOI) with an ~14 nm thick tensile strained silicon layer and a 150 nm thick buried $SiO_x$ layer (Soitec USA, Inc.).  The starting material in the *ZT* device sets was a SOI substrate with an ~100 nm thick silicon layer and a 200 nm thick buried $SiO_x$ layer (Soitec USA, Inc.).  Both type of substrates had 680 μm thick silicon handles.

A brush treatment was performed on both materals with a 1 wt% random block copolymer solution of poly(styrene-co-methyl methacrylate) (Polymer Source, Inc.) in toluene. Details of the process flow are provided here (Figure 2.3).
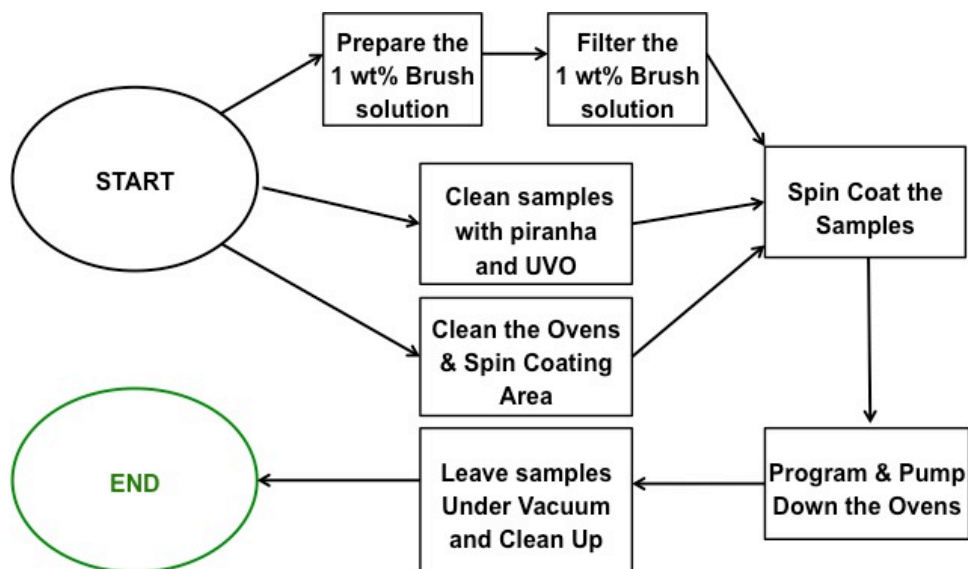
**Figure 2.3 Brush treatment process flow.**

## 2.1.2.1 Preparation of the 1 wt% brush solution

Cleanliness is key to a successful brush treatment: dust can contaminate the sample surface and disrupt the surface neutralization. A 20 ml glass vial, its cap, and a spatula were rinsed with acetone and isopropanol (IPA) and then blown with dry nitrogen ($N_2$) to remove all the dust. First, 0.1000 g (± 0.0010 g) of 62 mol% PS-r-PMMA copolymer (P7343-SMMAranOHT) and 0.1000 g (± 0.0010 g) of 71.2 mol% PS-r-PMMA copolymer (P3448-SMMAranOHT) were added into the vial. Then, 19.8000 g (± 0.0100 g) of toluene was mixed with the random copolymers. The glass vial was then placed in the sonicator (Fisher Scientific FS110H) for a 30 min sonication until all solid particles were dissolved.

## 2.1.2.2 Filtering of the 1 wt% brush solution

After sonication, the brush solution was filtered three times before use. The solution was first drawn from the glass vial into a 20 ml syringe outfitted with a hypodermic needle. The hypodermic needle was then removed from the syringe and replaced by a 0.2 μm filter. Meanwhile, the glass vial and hypodermic needle were cleaned thoroughly with toluene and IPA three times and blown dry with $N_2$. The solution was then filtered back into the cleaned glass vial. The filtering was repeated for two more times with new filters to obtain a homogeneous clean solution. The brush solution was then ready for use.

## 2.1.2.3 Sample cleaning

After the brush solution had been prepared, SOI samples went through a two-step cleaning process before being coated with a brush layer. In the first step, samples were subjected to a standard piranha cleaning, which consisted of immersing the samples in a solution of $H_2SO_4/H_2O_2$ (1:1 v/v) at 120 °C for 20 min to remove surface organic contaminants and hydroxylate the silicon surface. The samples were then thoroughly rinsed with deionized water (DIW) and dried with dry $N_2$. In the second step, the SOI samples were placed in a UV-ozone (254 nm UV light, Jelight Company, Inc.) machine for 20 min (Figure 2.4). They were then ready for spin coating.

**Figure 2.4 UV-ozone machine used for the organic cleaning of the pre-brush samples.**

## 2.1.2.4 Spin coating of the brush layer

The brush solution was applied to the SOI sample with a cleaned spin coater. Each clean SOI sample was centered on the coater chuck and blown with $N_2$ before coating to remove any dust. A pipette was cleaned with toluene and IPA before extracting 2-3 ml of brush solution. The solution was then deposited on the sample surface; the solution was applied carefully to ensure that no air bubbles were trapped in the coating. The spin coater's hood sash was closed to prevent dust contamination before the spinner ran at 1000 rpm for 60 s, with a 2 s ramp-up time.

## 2.1.2.5 Brush layer annealing in a vacuum oven

A vacuum oven was used to anneal the random copolymer brush layer to avoid oxidation. The cleaned oven was programmed to anneal coated samples for 6 hr at 225

°C at a pressure of 0.5-0.7 in. of Hg. Before annealing, the oven was slowly pumped down to avoid samples flipping over inside due to the flow. The vacuum valve was slowly opened to ensure that the pressure decreased no faster than 0.1 in Hg per second. Once the pressure was below 7.0 in Hg, the vacuum valve was opened all the way. During the thermal annealing, the random copolymer chemically bonded with the –OH groups on the samples to neutralize the surface. After annealing, the samples stayed inside the vacuum oven for at least 4 hr until it completely cooled down to avoid thermal shock to the samples.

## 2.1.2.6 Sample cleaning after annealing

After the thermal annealing, samples were cleaned by one-step cleaning before being coated with a block copolymer layer. Samples were placed into hot toluene at 110 °C for 30 min (± 1 min).  The toluene was warmed up on a hot plate for at least 5 min before use.  After 30 min, the samples were rinsed with room temperature toluene and dried with dry $N_2$ to remove dust. The purpose of soaking with hot toluene was to remove any excess random copolymer that was not bonded to the sample surface after the previous thermal annealing:  only one atomic layer of the bonded brush layer would be sufficient to neutralize the surface. Finally, a contact angle measurement can be conducted on this brush layer to characterize the surface neutralization before applying the block copolymer layer.

## 2.1.2.7 Contact angle measurement on the brush layer

One way to determine the quality of a brush layer is to characterize the surface energy based on Young's equation (Equation 2.1, Figure 2.5).

$$\Upsilon^{sv} = \Upsilon^{sl} + \Upsilon^{lv}\cos\theta \qquad\qquad (2.1)$$

($\theta$ is the contact angle; $\Upsilon^{sv}$ is the solid surface free energy; $\Upsilon^{sl}$ is the solid/liquid interfacial free energy; $\Upsilon^{lv}$ is the liquid surface free energy.)
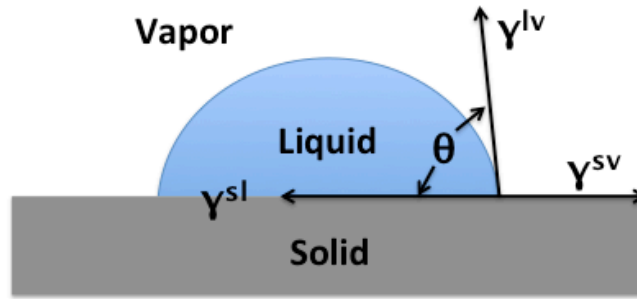


**Figure 2.5 Contact angle of a droplet on a solid surface.**

The contact angle measurement on the brush layer was performed with a contact angle goniometer (Model 190, Rame-Hart Instrument Co., Figure 2.6). A contact angle of 75 °-80 ° is a good indication of successful treatment based on the brush layer's roughness. There are mainly three types of contact angles: static angle, advancing angle, and receding angle. Static angle is measured by dropping only one droplet of water (1 ml) onto the sample surface after brush treatment (79 °, Figure 2.7, a); advancing angle is measured when dropping a second water droplet onto the first one (81 °, Figure 2.7, b); receding angle is measured when removing half of the first water droplet (76 °, Figure 2.7, c). All three angles should be the same if the surface is uniformly smooth. They vary when there is roughness. For the advancing angle measurement, the second water droplet prefers to mix with the first one instead of spreading on the film surface, so the angle gets bigger when the droplets grow rounder. For the receding angle measurement, the

remaining half water droplet tends to shrink but surface roughness hinders its movement, so the contact angle decreases. Typically, advancing angle > static angle > receding angle. In this study, the brush layer's contact angle measurements confirmed effective surface treatment. Samples were then ready for spin coating with block copolymer solutions.
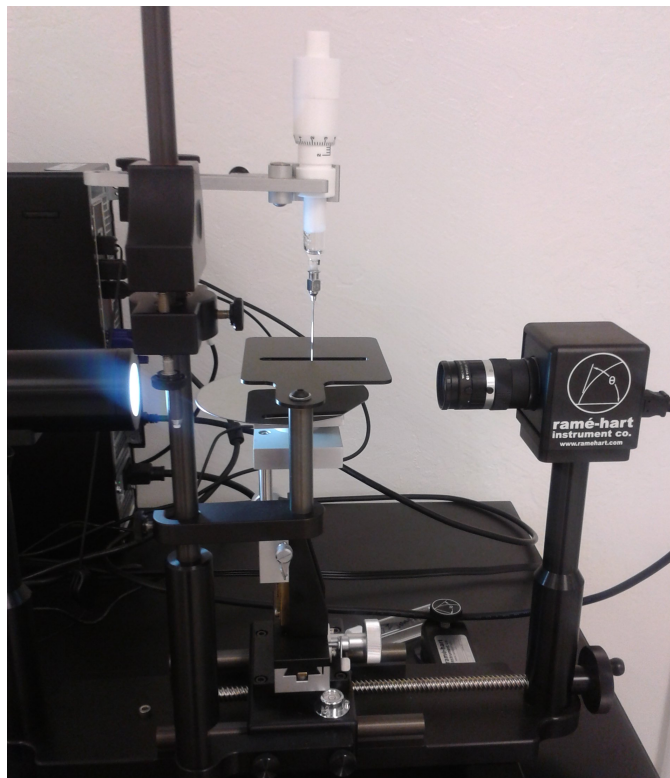


**Figure 2.6 Contact angle goniometer.**
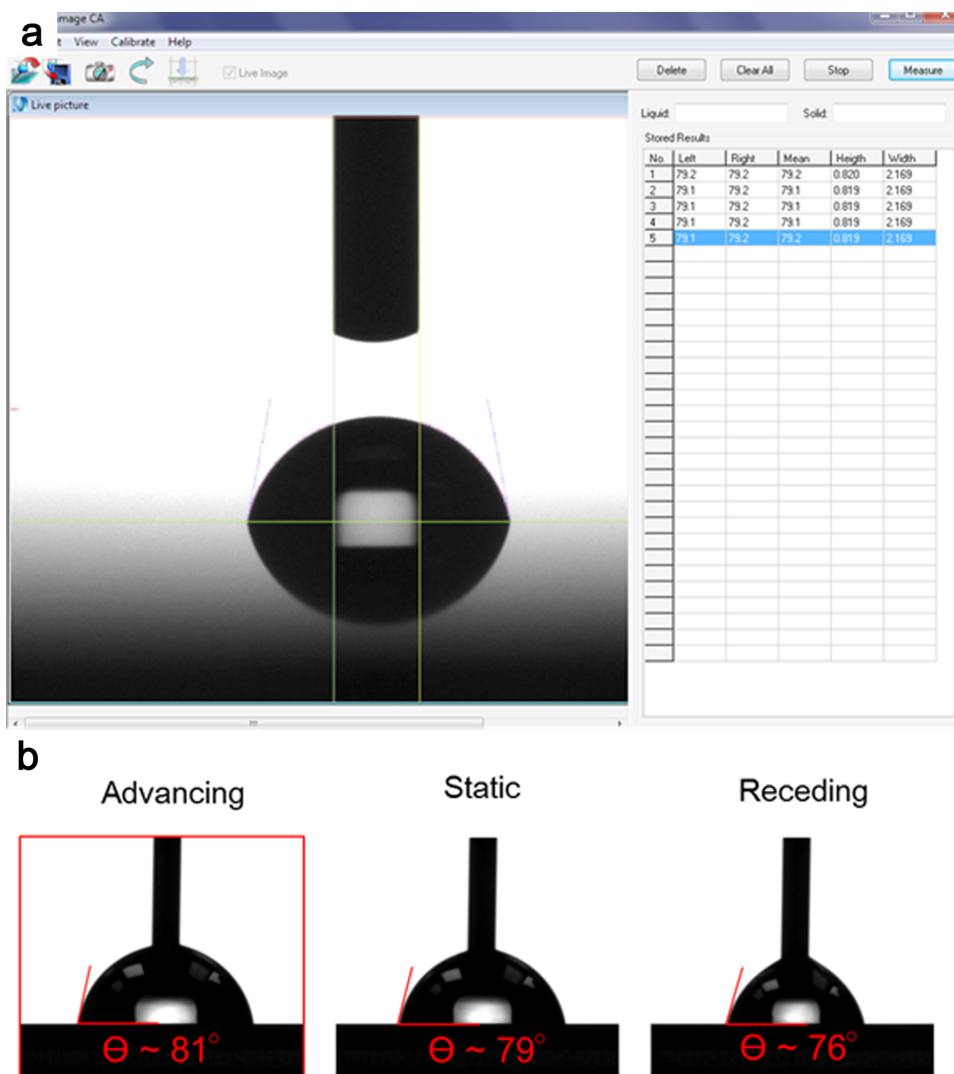
**Figure 2.7 Contact angle measurements. (a) Static measurement of brush layer with a contact angle goniometer; (b) Comparison of advancing, static, and receding contact angles on brush layer.**

Next, block copolymer solutions were prepared and coated on top of the brush layer to form vertical cylindrical domains (details described below).

## 2.1.3 Block copolymer self-assembly (BCSA)

The process chart (Figure 2.8) summarizes the main steps for block copolymer self-assembly (BCSA). The same level of cleanliness was required for this process as for

the brush treatment procedure described above. Samples also went through similar thermal annealing, except they were coated with poly(styrene-methyl methacrylate) solutions of different compositions from the brush layer.
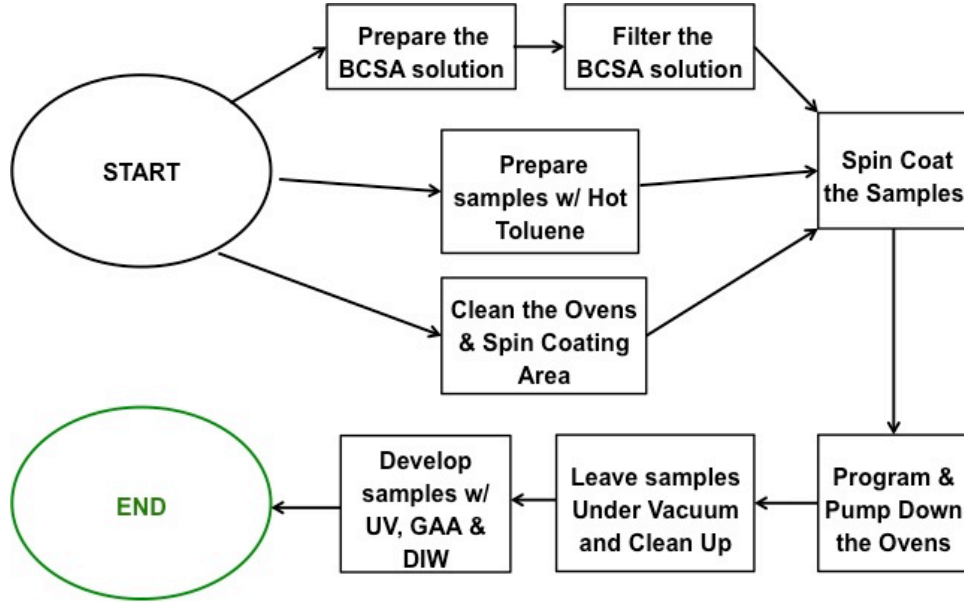


**Figure 2.8 Block copolymer self-assembly process flow.**

## 2.1.3.1 Preparation of the block copolymer solutions

As mentioned before, materials used in the $S^2\sigma$ and *ZT* device sets required different block copolymer solutions to form two nanoscale templates. The first template used on the strained silicon thin film in the $S^2\sigma$ device set was formed by using 2 wt% of 46 k - 21 k PS-b-PMMA (Polymer Source, Inc.) in toluene. The second template used on ~100 nm thick silicon thin film in the *ZT* device set was formed by using 1.5 wt% of 140 k – 65 k PS-b-PMMA in toluene. Both solutions had a small amount of 5 k – 5 k PS-b-PMMA to serve as a lubricant during the following thermal annealing step. The weighing and mixing procedures of these solutions are the same as the ones used in the brush solution in section 2.1.2.1.

## 2.1.3.2 Filtering of the block copolymer solutions

The block copolymer solutions were filtered using the same procedure as described above for filtering the brush solution in section 2.1.2.2.

## 2.1.3.3 Spin coating block copolymer solutions

Each clean sample was coated with block copolymer solutions following procedures similar to those described above for coating samples with a brush solution. For block copolymer solutions, the spinner ran at 2000 rpm for 60 s, with 2 s ramp-up time.

## 2.1.3.4 Block copolymer thermal annealing in a vacuum oven

The coated samples were annealed in a vacuum oven following procedures similar to those described above for annealing the brush layer. The vacuum oven was programmed to anneal coated samples for 6 hr at 225 °C. The temperature ramp-up took 15-30 min. During the thermal annealing, the block copolymer achieved self-assembly and formed desired cylindrical domains. After annealing, the vacuum oven was pumped open and cooled down following the procedures described in section 2.1.2.5. After the samples had been removed from the cooled oven, they were ready to be developed to form nanomesh structures.

## 2.1.3.5 Block copolymer developing after thermal annealing

After thermal annealing, a successful template would have PS and PMMA self-assembled into cylindrical domains with PMMA filled inside the cylinders and PS filled in the rest of area and formed into a nanomesh matrix. The self-assembled structure was further strengthened by 254 nm UV exposure. The UV lamp was first warmed up for at least 5 min before the samples were exposed for 10 min. The purpose of the UV exposure was to breakdown the PMMA cylinders and crosslink the PS matrix.

Afterwards, the samples were soaked in glacial acetic acid (GAA) for 30 min (± 1 min). This development step removed the degraded PMMA cylindrical fillings and left the PS matrix intact. The samples were then immediately soaked in DIW for another 30 min, and then dried with dry $N_2$. The nanomesh structures within block copolymer layers were obtained and sent for SEM analysis.

## 2.1.3.6 SEM image of nanomesh structure

The top surface of samples in each template was imaged with SEM (JEOL 3100, Figure 2.9). Different block copolymer compositions in BCSA solutions were carefully chosen to produce the desired patterns. The first template was formed by using 46 k – 21 k PS-b-PMMA to generate nanomesh with 18 nm diameter and an 36 nm pitch for the $S^2\sigma$ device set (Figure 2.9, a). The second template used 140 k – 65 k PS-b-PMMA for a nanomesh structure with 40 nm diameter and an 80 nm pitch for the *ZT* device set (Figure 2.9, b). The resulting PS thickness was determined to be ~100 nm for both templates, as determined by SEM.
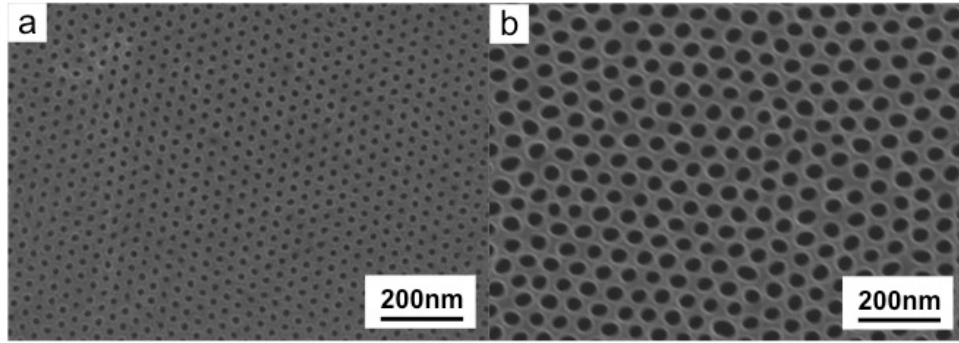
**Figure 2.9 SEM images of nanomesh structures after developing thermally annealed block copolymer. (a) The first nanomesh template for the S²σ device set where the nanomesh had 18 nm diameter and an 36 nm pitch; (b) The second nanomesh template for the *ZT* device set where the nanomesh had 40 nm diameter and an 80 nm pitch.**

## 2.1.4 Nanomesh transfer from block copolymer to silicon

Traditionally, photolithography and electron beam lithography use UV or electron sensitive resists to create patterns (or templates) after UV or electron exposure. The patterns are generated either with photo masks or programmed writing. A pattern is then transferred onto the underlay film by metal deposition or etching. BCP, however, forms templates by block copolymer self-assembly. After developing, templates are ready for further processing. In this study, we transferred the two templates for the S²σ and *ZT* device sets by RIE and DRIE to etch through 5 nm thick strained silicon thin film and ~100 nm thick silicon thin film, respectively.

### 2.1.4.1 First nanomesh template transfer by RIE

To transfer the nanomesh template from the PS matrix to the top strained silicon film, a two-step RIE was performed. First, oxygen plasma was used to clear out the remaining PMMA residue in the holes; the following process conditions were used: $O_2$ flow rate = 20 sccm, power = 50 W, and pressure = 20 mtorr. Then $CF_4$ plasma was used

to etch the strained silicon thin film with the PS matrix as an etch mask (Figure 2.10). PS

residue was removed afterwards by $O_2$ plasma descum (Plasmatherm 790, Plasma-

Therm, LLC).
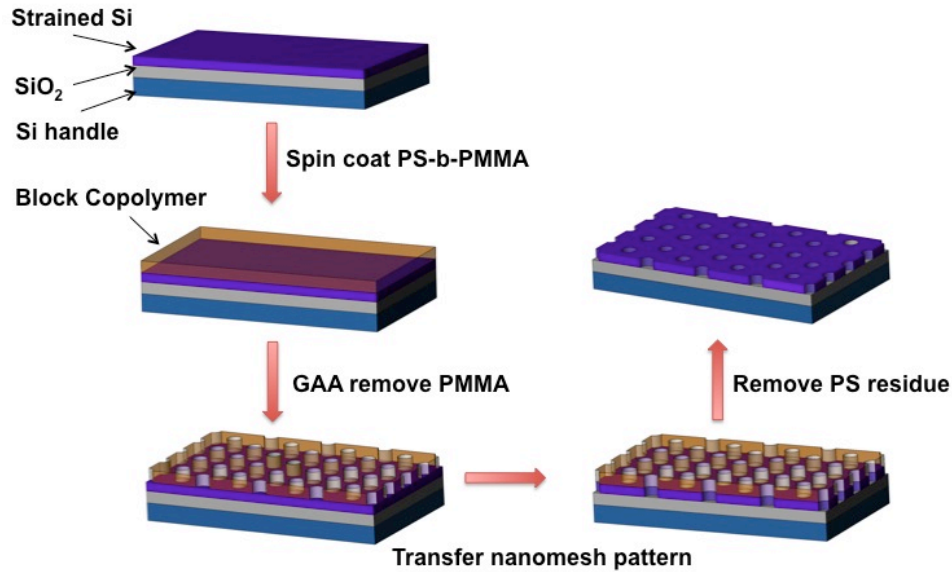


**Figure 2.10 Fabrication procedure for strained silicon nanomesh. (a) Starting sample is an ~5 nm thick SSOI substrate; (b) Apply PS-b-PMMA coating and thermallly treat PS-b-PMMA block copolymer; (c) Remove PMMA by UV exposure and acetic acid; (d) RIE etch strained silicon thin film with PS as etch mask; (e) Remove PS residue by oxygen plasma descum.**

## 2.1.4.2 Second nanomesh template transfer by DRIE

The second template transfer requires higher ratio of etch rates in silicon and PS

(selectivity) due to their similar film thickness. DRIE can perform with a high selectivity

and more vertically anisotropic etching to avoid too much undercut (lateral etching). Here

the nanomesh template was transferred to an underlay silicon thin film by a two-step

etching process. First, oxygen plasma was used to clear out the remaining PMMA residue

within holes; the following process conditions were used: $O_2$ flow rate = 20 sccm, power

= 50 W, and pressure = 20 mtorr (Plasmatherm 790, Plasma-Therm, LLC). Then, the nanomesh pattern transfer was achieved by DRIE (Pegasus STS, SPTS Technologies).

It is crucial that the silicon between two holes (neck) is preserved with the least undercut after DRIE and that the entire silicon film is thoroughly etched through. A poor DRIE process would result in lateral over-etching that destroys the nanomesh structure (Figure 2.11, a); the resulting silicon film exhibits very poor electrical conductivity. A good DRIE process successfully transfers the nanomesh structure from the block copolymer layer to the silicon film with essentially a vertical etching profile (Figure 2.11, b); the resulting silicon film exhibits good electrical conductivity.
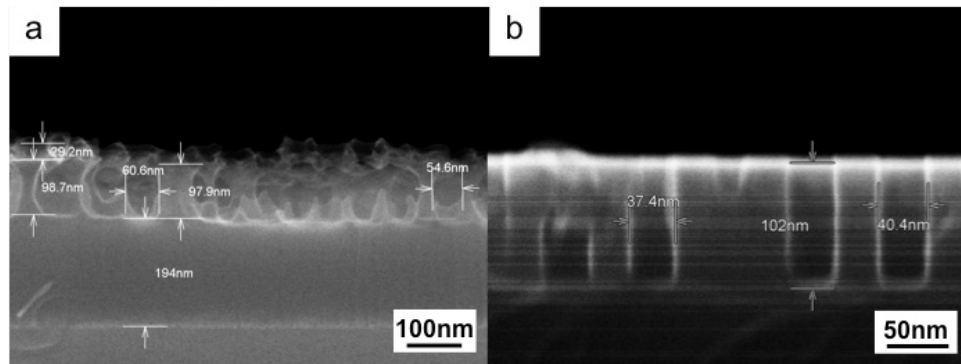


**Figure 2.11 Cross-sectional SEM images for SOI with ~100 nm thick silicon and 200 nm thick silicon oxide after DRIE. (a) Poor DRIE with excess lateral etching; (b) Good DRIE with vertical etching.**

The DRIE process employed in this study is essentially a Bosch process. It consists of two steps to achieve anisotropic etching; i.e., to reduce lateral etching and enhance vertical etching. In this process, a plasma is generated with a 13.56 MHz coil at 600 W. A $SF_6$ plasma is used to etch silicon, and a directional bias power of 80 W generated from a 380 kHz platen drives the plasma downwards. A chemically inert passivation substance (similar to Teflon) yielded from $C_4F_8$ plasma is deposited in a

58

conformal manner on the sample surface and the etched sidewalls of holes. $SF_6$ and $C_4F_8$ plasmas are switched alternatively and generated for 1.2 s and 1.0 s, respectively, per cycle (Figure 2.12). There are 20 etch cycles in total. The $SF_6$ flow rate is kept at 120 sccm for all etching cycles, while the $C_4F_8$ flow rate is decreased from 150 sccm to 100 sccm gradually from the beginning to the end of 20 cycles so the etching becomes more aggressive at the bottom of the holes. The deposited substance at the bottom of each hole is removed much faster than the coating on the sidewalls, resulting in net etching into the hole. The higher $C_4F_8$ flow rate gives better protection to the sidewalls but also reduces vertical etch rate. The reduced vertical etch rate can be compensated for by increasing the bias power to achieve more directional etching. Additionally, chilling the sample platen to 0 °C during etching reduces plasma volatility and facilitates etching.
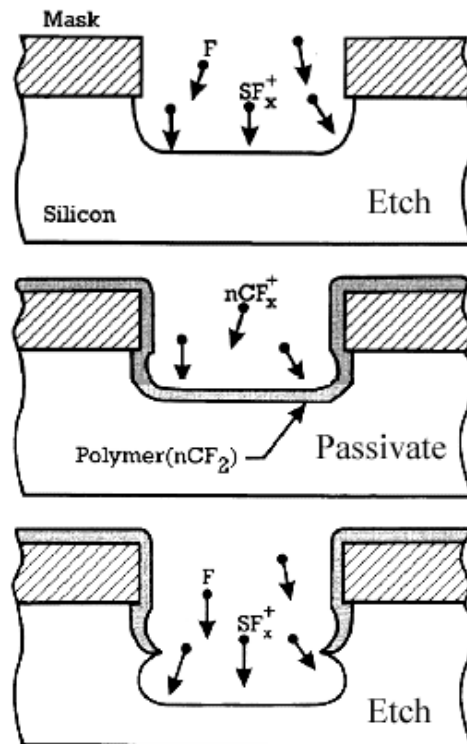


**Figure 2.12 Bosch etching with $SF_6$ and $C_4F_8$ plasma alternatively switched to etch vertically into the trench.**

After DRIE, the remaining PS matrix residue was in a hardened state and difficult to remove with only a piranha clean. Therefore, an $O_2$ descum process was first performed to soften the hardened PS layer; then, the samples were subjected to a standard piranha clean ($H_2SO_4/H_2O_2$, 1:1 v/v, 120 °C, 20 min). The $O_2$ descum was conducted in Drytek4 (figure 6-12) with $O_2$ flow rate = 20 sccm, pressure = 150 mtorr, power = 50 W, and process time = 5 min. After the two-step cleaning, the SOI sample with nanomesh was ready for *ZT* device set fabrication.

Overall, this BCP process of the *ZT* device set essentially follows the same steps used in the one of the $S^2\sigma$ device set, as previously described in Figure 2.10 (section 2.1.4.1).

## 2.2 $S^2\sigma$ device set fabrication

For the $S^2\sigma$ device set, both strained silicon thin films (SSOI) and unstrained silicon thin films (SOI) with similar film thickness were prepared. The SOI samples were control samples to exam the strain effects in the strained silicon. Both SSOI and SOI samples were also prepared with nanomesh and without nanomesh to study the effects of nanomesh on electrical conductivity and thermopower. For brevity, the device fabrication process is mainly illustrated with a SSOI sample with nanomesh.

The SSOI sample was doped with a diffusion doping method using a solid source and rapid thermal processing (RTP). After doping, BCP was employed to fabricate the first nanomesh template and reactive ion etching (RIE) was used to transfer the pattern into the strained silicon thin film, as described in section 2.1. For electrical conductivity and thermopower devices, metal contacts (titanium and platinum) were deposited in an

electron beam evaporator (Enerjet, OEM Company) onto samples covered with a photoresist mask patterned by photolithography (MA/BA-6, Karl Suss). The unstrained silicon thin film from a SOI sample was also prepared using the same processes as the control sample with similar film thickness for comparison. For brevity the device fabrication process is mainly illustrated with a SSOI sample.

## 2.2.1 Solid-state diffusion with phosphorus dopants

The starting thin film was a SSOI sample (Soitec USA) composed of a 14 nm thick, <100>-oriented, intrinsic tensile-strained silicon layer on top of a 150 nm thick buried thermal oxide layer on top of a bulk silicon handle.

## 2.2.1.1 Pre-doping clean

Before diffusion doping, the SSOI sample was subjected to a two-step cleaning and etching process: a first cleaning step in piranha solution of sulfuric acid and hydrogen peroxide ($H_2SO_4$:$H_2O_2$=1:1, v/v, 120C, 20min) followed by a second etching step in buffered hydrofluoric acid BHF (NH4F:HF=10:1, v/v, 20 C, 5 s). The first step removed organic contaminants from the SSOI surface. The second step removed native silicon oxide, which acts as a barrier against diffusion doping. Samples were then rinsed in DIW for 5min, dried with dry $N_2$, and immediately transferred into a rapid thermal annealing furnace (RTA, Jetfirst 150, JIPELEC).

## 2.2.1.2 Solid-state diffusion doping

A solid diffusion wafer with phosphorus dopants embedded in a silicon carbide substrate (Saint Gobain Ceramic Materials, Inc, Figure 2.13) was positioned on top of a SSOI substrate. Dummy silicon pieces were position between them at their edges to avoid direct contact so that contamination is kept at a minimum. The RTA furnace was programmed with a sequence to ramp up the temperature from 20° C to 900° C within 2 min, hold the temperature at 900° C for 2 min, and then ramp the temperature back down to 20° C. An ambient flow of argon gas at 1000 sccm was supplied throughout the run to ensure an inert atmosphere so as to prevent silicon oxidation.
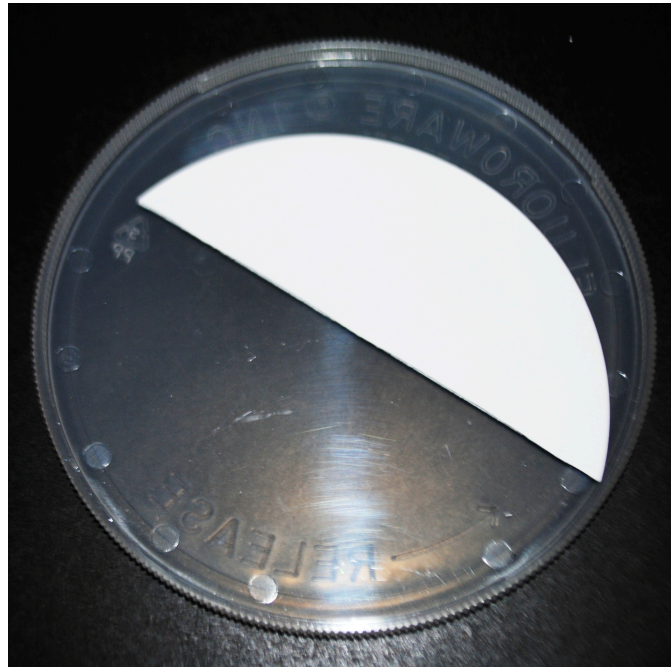


**Figure 2.13 Phosphorus dopants embedded solid diffusion wafer on a 4 in wafer carrier.**

At 900° C, phosphorus dopants diffuse into silicon, where they concentrate close to the silicon surface. The phosphorus diffusion profile from can be calculated based on Fick's second law (Equation 2.2).

$$\frac{\partial C}{\partial t} = -D \frac{\partial^2 C}{\partial x^2}$$ (2.2)

(C is the dopant concentration under the silicon surface; D is the dopant diffusion coefficient as a function of temperature; t is the time of diffusion; x is the distance into silicon from the silicon surface, where x=0 at the surface)

Under the conditions of semi-infinite slab diffusion with constant or infinite supply of dopants, the solution to Equation 2.2 is given below (Equation 2.3). [16]

$$N(x,t) = N_0 \mathrm{erfc}(\frac{x}{2\sqrt{Dt}}) \tag{2.3}$$

(N(x,t) is the dopant concentration at depth x after time t; $N_0$ is the dopant concentration at the silicon surface; D is the phosphorus diffusion coefficient, $1.48 \times 10^{-15}$ $cm^2$/s)

For t = 120 s, the dopant concentration profile is plotted (Figure 2-14).
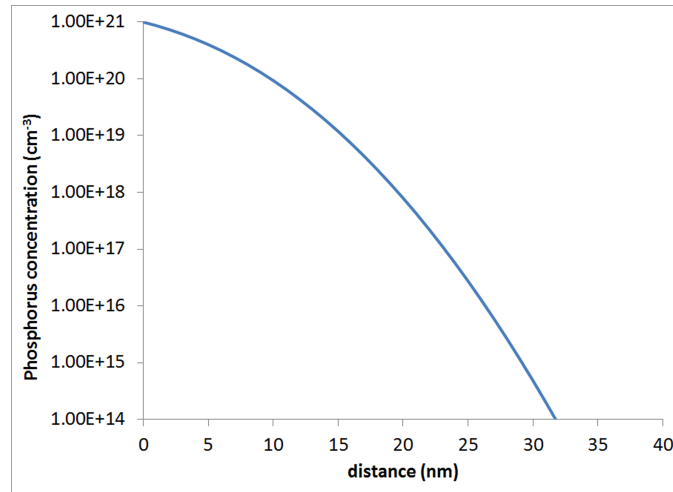


**Figure 2.14 Diffusion dopant concentration profile for phosphorus with arbitrary surface dopant concentration, $N_0 = 10^{21} cm^{-3}$.**

After diffusion doping, samples were dipped into BHF for 30 s to remove any undesirable surface compound consisting of phosphorus oxide. The film thickness of strained silicon was measured 5 nm due to oxidation consumption, while the film thickness of unstrained silicon was measured to be 10 nm by atomic force microscopy (AFM, Veeco Nanoman, Veeco Instruments Inc.). The sheet resistance of both SSOI and

SOI (for comparison) samples were measured with a four-point probe station (Lucas Labs) paired with a sourcemeter (Keithley 2400). Samples were positioned face-up on the station. Four pins were lowered to contact with the silicon surface. The sourcemeter's 4-wire function was used to measure sheet resistance. Resistivity can be determined from sheet resistance (Equation 2.4).

$$\rho = R_s t \hspace{4cm} (2.4)$$

($\rho$ is resistivity; $R_s$ is thin film sheet resistance, and t is thin film thickness)

After applying BCP with the first template on SSOI and its SOI control sample as described in section 2.1, the sheet resistance increased in both samples due to the presence of nanomesh. A table is provided below for the comparison of sheet resistance of both samples, without nanomesh and with nanomesh (Table 2.1).

**Table 2.1 Sheet resistance of SSOI and SOI samples without and with nanomesh after diffusion doping at 900° C, measured with four-point probe station at room temperature in air.**

| Sample | SSOI without nanomesh | SSOI with nanomesh | SOI without nanomesh | SOI with nanomesh |
|---|---|---|---|---|
| Sheet resistance ($\Omega$) | 13286 | 39427 | 35908 | 95866 |

## 2.2.2 Metallic contacts

Metallic contacts for the electrical conductivity measurement device were fabricated by depositing metal films through a photoresist mask on the surface of SSOI and SOI samples. A photolithography mask (Figure 2.15) was first designed with L-edit software. The green boxes (150 μm X 150 μm squares) represent transparent windows on the mask and also the metal contacts after deposition. The masked samples were first dipped into BHF for 3 s to remove surface native oxide and then transferred into an electron beam evaporator. A 10 nm thick titanium film and a 100 nm thick platinum film

were deposited under a pressure of $2E^{-6}$ mtorr. After metal deposition, the photoresist mask was stripped off in acetone. The sample was then annealed in a rapid thermal annealing furnace (RTA Jetfirst-100, JIPELEC) at 350 °C with forming gas (95% $N_2$, 5% $H_2$) for 5 min to drive out moisture and oxygen from the deposited metal films. Good bonding was formed between the silicon surface and the metallic contacts.
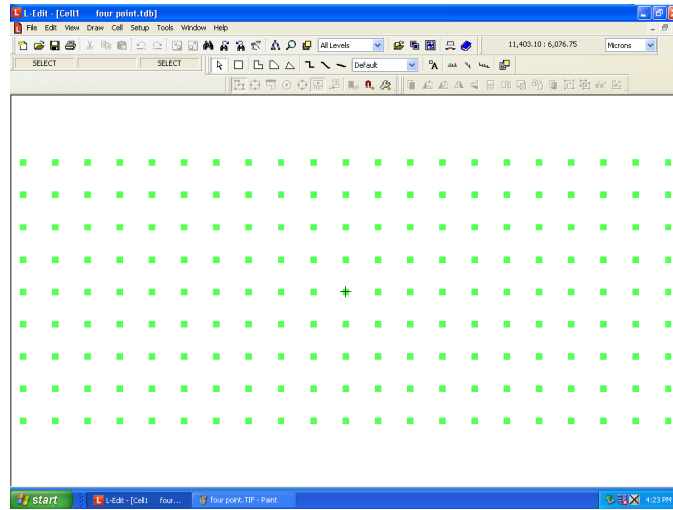


**Figure 2.15 Mask design (using L-edit) of metallic contact pads for electrical conductivity measurement on SSOI and SOI samples.**

The two metallic contacts for the thermopower measurement device were patterned by photolithography and deposited in an electron beam evaporator, approximately 1 cm apart, using the same procedures described above for contacts of the electrical conductivity measurement device. The two contacts were also annealed in the same way to enhance the bonding between metals and silicon.

## 2.3 *ZT* device set fabrication

Since *ZT* is calculated from the formula $ZT = S^2 T/(\rho\kappa)$, three parameters [thermopower (S), electrical resistivity ($\rho$), and thermal conductivity ($\kappa$)] need to be

determined at a given temperature T. In our studies, each parameter was determined from a measurement on an individual device. All three devices of the *ZT* device set were fabricated on a single chip; together, three measurements allow us to determine the figure of merit *ZT*. In particular, the thermopower (S) was measured from a first device using the 2-thermometer method (Figure 2.16, a); the electrical resistivity ($\rho$) was measured from a second device using a Greek cross structure with the Van der Pauw method (Figure 2.16, b); and the thermal conductivity ($\kappa$) was measured from a third (suspended) device using the 2$\omega$ method (Figure 2.16, c). Details of device fabrication for the three devices are provided in this section.

Block copolymer was first used to make the second nanomesh template; then, deep reactive ion etching (DRIE) was used to transfer the nanomesh pattern from the PS mask to the ~100 nm thick silicon layer as described in section 2.1.4.2. Ellipsometry was used to determine the structural thickness and nanomesh porosity of the SOI nanomesh sample after DRIE, and the results are shown in chapter 3. Ion implantation and after-implant activation were then used to dope the silicon nanomesh thin film with boron.

After doping, the three devices were fabricated as follows. First, silicon nanomesh (abbreviated as NM) was patterned and etched by DRIE. Second, thermopower thermometers and Van der Pauw contact pads were fabricated using photolithography and metal deposition. Third, thermopower heaters, 2$\omega$ electrodes, and contact pads were fabricated using photolithography and metal deposition. Finally, the area of the 2$\omega$ electrodes was suspended from the backside of the SOI sample.
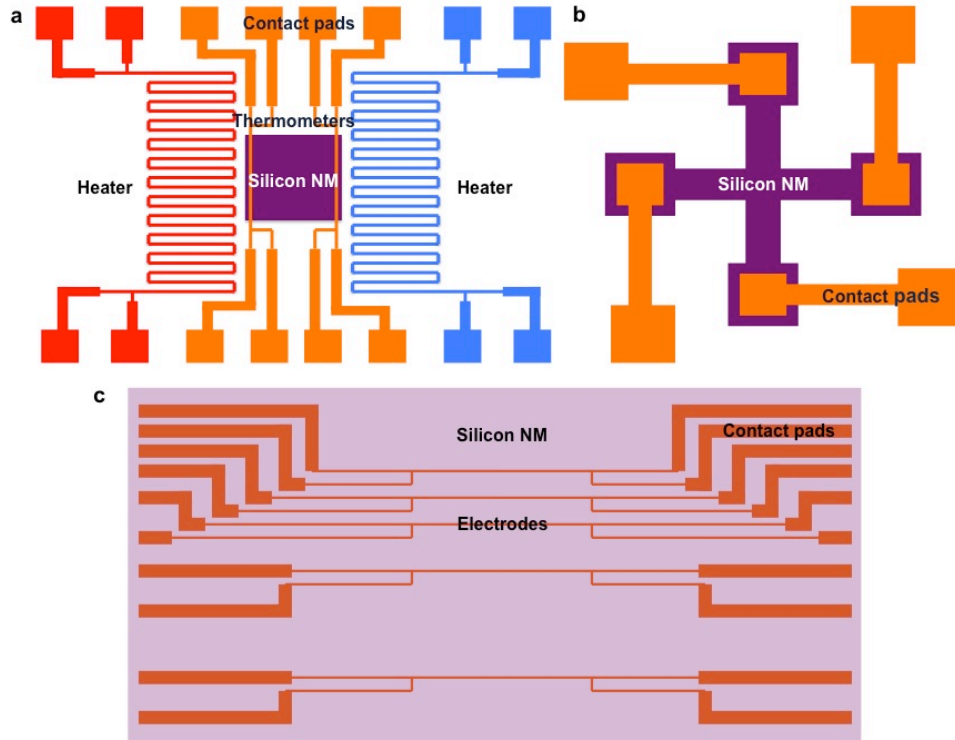
**Figure 2.16 Illustrations of three devices fabricated on the same chip. (a) The first device is used to measure thermopower (S) with a 2-thermometer method; (b) The second device is used to measure electrical resistivity (ρ) with a Van der Pauw method; (c) The third (suspended) device is used to measure thermal conductivity (κ) with the 2ω method.**

## 2.3.1 Silicon nanomesh doped by ion implantation

In order to study thermopower and electrical conductivity in silicon nanomesh, the ~100 nm thick silicon thin film was doped into p-type with boron after BCP process in this study. Ion implantation was chosen for the following advantages: controllable process and uniform doping profile. A three-step process was conducted to obtain p-doped silicon nanomesh: pre-implant cleaning, ion implantation, and after-implant thermal annealing. After doping, samples were characterized for their doping level and electrical resistivity at room temperature.

## 2.3.1.1 Pre-implant cleaning

SOI nanomesh samples were subjected to a standard piranha cleaning consisting of $H_2SO_4/H_2O_2$ (1:1 v/v) at 120 °C for 20 min. The purpose of piranha cleaning was to remove surface organic contaminants. After 20 min, the samples were then thoroughly rinsed with DIW and dried with dry $N_2$.

In order to monitor the ion implantation, the SOI nanomesh sample had a corresponding SOI monitor piece (without a nanomesh structure) cleaned and implanted at the same time. The SOI monitor piece also had the same thickness and composition of silicon/buried oxide/silicon handle as the SOI nanomesh sample. Both the SOI nanomesh sample and the SOI monitor piece were taped onto a 4 in silicon carrier wafer with Kapton tape prior to ion implantation. After doping, secondary ion mass spectroscopy (SIMS) was conducted on the SOI monitor piece to obtain the doping profile for the ion implantation procedure since it requires complicated calibrations to conduct accurate SIMS measurement on a SOI nanomesh sample. The SIMS result of a SOI monitor is shown in chapter 3.

## 2.3.1.2 Ion implantation

<100>-oriented silicon nanomesh samples and SOI monitor pieces were exposed to a boron ion source during ion implantation (Axcelis GSD 200, Innovion Corporation, San Jose, CA). B(11)+ ions were implanted at 12.5 keV with a dose of $2X10^{14}$ $cm^{-2}$ to the top silicon nanomesh layer. Based on the implant energy and dose, boron ions penetrated ~20 nm below the silicon surface. The implant was conducted with an off-

axis angle of 7 ° to minimize ion channeling along the <110> direction in silicon during ion implantation; minimizing the ion channeling leads to the most reproducible results.

## 2.3.1.3 After-implant thermal annealing

After ion implantation, the samples need a thermal annealing step to activate the dopants. To avoid any organic or inorganic contamination, the samples were annealed face down on a carrier wafer at 1050 °C for 4 min in a rapid thermal processing (RTP) system (All-Win 610, Allwin21 Corporation). Throughout the annealing process, the furnace was purged with nitrogen gas at a flow rate of 7 slpm. The temperature was ramped up from 20 °C to 1050 °C within 30 s, stabilized at 1050 °C for 240 s, and then ramped back down to 20 °C within 90 s. After annealing, the samples were kept in the furnace for 5 min to cool down.

After RTP, the boron dopants were activated and distributed within the ~100 nm thick silicon nanomesh thin film. A four-point probe station was used to estimate the electrical resistivity of the nanomesh sample at room temperature in air.

## 2.3.1.4 Electrical resistivity result from four-point probe station

The silicon nanomesh sample after boron implantation and activation was measured with a four-point probe station to estimate its electrical resistivity at room temperature. The four-point probe station was connected to a sourcemeter (Keithley 2400) set at auto measurement. The resistance measured was ~600 $\Omega$. If the thickness of the silicon nanomesh thin film was 100 nm, the electrical resistivity was then determined to be ~27 m$\Omega$•cm (Equation 2.5).

$$\rho = 4.53tR \qquad\qquad (2.5)$$

($\rho$ is the resistivity; t is the film thickness, and R is the resistance read from the sourcemeter configured for a 4-wire function)

A more accurate resistivity measurement was conducted on the silicon nanomesh with the Van der Pauw method from the second device; a custom-designed vacuum setup was used. The accurate resistivity result is presented in chapter 3. After this four-point measurement, the SOI nanomesh sample was ready for the photolithographic and metallurgical steps of device fabrication.

## 2.3.2 Device fabrication after doping

The device fabrication after doping consisted of four main steps as described previously. In each of the first three steps, chips were patterned by a photomask with photolithography then processed mainly by RIE or metal deposition. At the last step, the third device was suspended for $2\omega$ thermal conductivity measurement.

## 2.3.2.1 First step-silicon nanomesh patterning

In the first step, the silicon nanomesh sample was coated with photoresist. Photolithography was used to create patterns on the photoresist for fabrication of all three devices; the patterns included alignment marks as reference for further photolithography steps.

First, the sample was dehydrated at 150 ℃ and primed by HMDS (Hexamethyldisilazane) vapor (YES oven, Yield Engineering Systems, Inc.) to provide better coverage and adhesion between oxides (native silicon oxide in this case) and

photoresists. Positive photoresist SPR 3612 (Shipley Europe Ltd.) was chosen to coat the SOI sample. The photoresist was applied on a spinner (Headway Research, Inc.) at 5000 rpm for 1 min, followed by a 1 min soft bake at 90 °C. The resist thickness should be ~1 μm. The sample was then exposed under 365 nm UV light for 1.6 s, with the first photomask defining desired silicon nanomesh patterns and alignment marks; a MA/BA mask aligner (Karl Süss, Süss MicroTec AG) was used.

The sample was then developed in MF-26A developer (Shipley Europe Ltd.) for 45 s to remove the exposed photoresist. To clear the photoresist residue after developing, 30 s of $O_2$ plasma descum was performed under 150 mtorr pressure with 100 sccm $O_2$ flow rate and 500 W power in a Drytek2. The sample was then etched by RIE in the Drytek2 to transfer the photo-patterns; the RIE stopped at the buried oxide layer. The plasma used was a mixture of sulfur hexafluoride ($SF_6$) and $ChClF_2$ (Freon 22) under 150 mtorr pressure with 400 W RF power; the flow rates of $SF_6$ and $ChClF_2$ were 117 sccm and 51 sccm, respectively.

After RIE, the buried oxide thickness was measured to be 198 nm by ellipsometry with a NanoSpec 6100 (Nanometrics, Inc.). The oxide was over-etched by 1%. Later, the remaining photoresist was removed by dipping samples into a piranha solution consisting of $H_2SO_4/H_2O_2$ (1:1 v/v) at 120 °C for 20 min. The SOI sample was considered clean when no more bubbles appeared.

## 2.3.2.2 Second step - metallization

In the second step, the sample was coated with photoresist, which was then patterned with the second photomask. The patterned photoresist, after further processing,

served as a mask for deposition of metals to fabricate resistive thermometers and contact pads for the thermopower and electrical resistivity devices.

First, the sample surface was primed with HMDS vapor, as in step one. The sample surface was then coated with two layers of photoresist as follows. First, LOR5A resist was coated on the samples to serve as an undercut layer in bi-layer lift-off processing. The LOR5A resist was applied with a spinner at 5000 rpm for 60 s and baked at 170 °C for 5 min. The second layer photoresist was SPR3612, with the same coating and baking conditions as in section 2.3.2.1. The bi-layer thickness should be ~1 μm.

The samples were then exposed to 365 nm UV light for 1.8 s on a mask aligner with the second photomask to form the patterns for metal deposition. After exposure, the sample was developed for 45 s, and double lines of the exposed features were imaged under an optical microscope (Figure 2.17). In this image, the outer line was from LOR5A, and the inner line was from SPR3612. The double line feature ensures good metal lift-off since LOR 5A dissolves faster than SPR3612 in the developer solution.
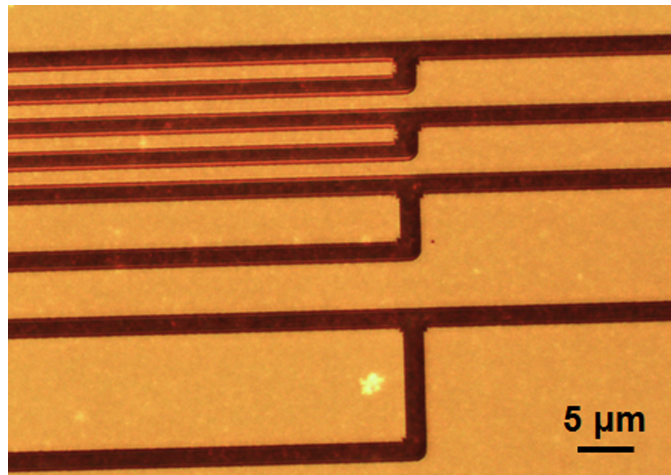


**Figure 2.17 Optical microscopy image of LOR5A and SPR3612 double line feature after UV exposure and photoresist developing.**

After development, the sample was subjected to $O_2$ descum for 30 s and dipped in buffered oxide etchant (6:1 BOE, 34%vol $NH_4F$, 7%vol HF, and 59%vol water, Transene Company, Inc.) for 5 s to remove native silicon oxide. The sample was then transferred immediately for metal deposition in an electron beam evaporator (Innotec ES26C; Innotec, Corp.). A 100 Å thick Cr film and a 1400 Å thick Pt film were deposited. Metal lift-off was conducted in a remover PG solution (Microchem, Corp.) for 20 min at 120 °C. The sample was then cleaned with IPA and dried with dry $N_2$, ready for the third step.

## 2.3.2.3 Third step - metallization

The third step was mainly dedicated to fabricating 10 μm wide heaters in the thermopower device and the contact pads and 2 μm wide thermometers in the thermal conductivity device. In order to obtain uniform temperature on each thermometer for thermal conductivity measurement, a 200 Å thick $SiN_x$ layer was deposited on top of the chip by PECVD at 350 °C (PlasmaTherm Shuttlelock SLR-730; Plasma-Therm, LLC.). This film had ~220 Mpa tensile stress and served as an isothermal medium for the thermometers. After $SiN_x$ deposition, the third photolithography was conducted with the same procedure as in the second step in section 2.3.2.2, but with a different photomask. The sample was developed and descumed as before. A 50 Å thick Ti film and a 500 Å thick Au film were then deposited in the electron beam evaporator. After metal lift-off, the sample was ready for the last step, thermal conductivity device suspension.

## 2.3.2.4 Last step- thermal conductivity device suspension

The sample was first coated with photoresist on the top silicon layer side to prevent silicon etching. It was then taped (with Kapton tape) face down onto a sample carrier to expose an ~1 X 1 mm square of silicon on the SOI handle side, centered over the thermometers in the thermal conductivity device. The silicon etching was conducted in a Xactix gas-phase etcher (Xactix, Inc.) with $XeF_2$ gas at 3 torr pressure for 100 cycles with 30 s per cycle. The etching was completed when the chip looked semi-transparent through the exposed square (Figure 2.18). Meanwhile, the buried silicon oxide from the SOI served as an etch stop due to a very low $XeF_2$ etch rate on $SiO_x$. After suspension, the top side of the chip was gently etched by $O_2$ plasma to remove the protective photoresist. This descum was conducted with 20 sccm $O_2$ flow rate under 150 mtorr pressure and 100 W RF power for 5 min.
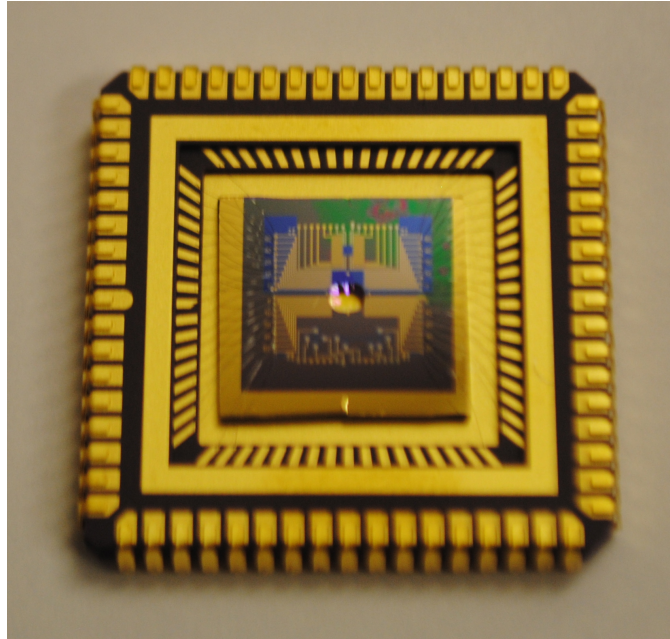


**Figure 2.18 The SOI sample was etched from the backside until the membrane looked semi-transparent.**

After the device fabrication, the chip was bonded to a chip carrier on a wirebonder (West Bond 7476E Wedge-Wedge Wire Bonder, West Bond, Inc.) with aluminum wire at room temperature under these settings: 260 mN bond force and 30 μs bond time. The sample is then ready for thermopower, electrical conductivity, and thermal conductivity measurements to determine *ZT*. The metrology for all three measurements is provided in chapter 3. Details of data collection and analysis are discussed in chapter 5.

## 2.4 Summary

## 2.4.1 Summary of fabrication of S$^2$σ device set

We described the fabrication process of the S$^2$σ device set on SSOI and its SOI control sample in section 2.2. Solid-state diffusion doping was first employed to drive phosphorus dopants into silicon. After doping, samples were thermally treated with a brush layer to assist a formation of a vertically aligned cylindrical micelle structure. Then BCSA was performed to obtain the desired nanomesh diameter and pitch. RIE ensured the successful transfer of the structure from the PS matrix layer to the underlying strained silicon thin film. Two devices were fabricated using photolithography and metal deposition to measure electrical conductivity and thermopower. Metallic contacts of titanium/platinum were chosen to minimize contact resistance at the metal-semiconductor junction. Forming gas annealing helped strengthen the metallic bonding and reduce defects from deposition.

## 2.4.2 Summary of fabrication of *ZT* device set

In section 2.3, details of sample preparation and the *ZT* device set fabrication were provided. PS-b-PMMA block copolymer was employed for BCSA, and DRIE transferred the nanomesh pattern into the top silicon layer in the ~100 nm thick SOI sample. Ion implantation was used to dope silicon nanomesh thin film with boron at the level of $2 \times 10^{19}$ atoms/cm$^3$. Then device fabrication consisted of four steps using techniques such as photolithography, RIE, metal deposition, PECVD SiN$_x$ deposition, XeF$_2$ etching, etc. This process was designed to fabricate three different devices on one chip for the purpose of thermopower, electrical resistivity, and thermal conductivity measurements. First, desired silicon nanomesh regions were patterned and preserved after plasma etching. Then, contact pads, heaters, and thermometers for the three devices were patterned and fabricated with separate photomasks at different steps. After the third step, all three devices on the chip were finished. The last step was to suspend the thermometers from the thermal conductivity device to reduce thermal leakage.

## 2.5 Reference

[1] G.M. Grason, *Physics Reports* **433** 1-64 (2006).

[2] I.W. Hamley, *The Physics of Block Copolymers*, Oxford University Press, Oxford, 1998.

[3] M.W. Matsen, M. Schick, *Physics Review Letter* **72** 2660 (1994).

[4] M.W. Matsen, F.S. Bates, *Macromolecules* **29** 1091 (1996).

[5] J.Y. Cheng, C.A.Ross, H.I. Smith, and E.L. Thomas, *Advanced Materials* **18** 2505-2521 (2006).

[6] K.W. Guarini, C.T. Black, Y. Zhang, H. Kim, E.M. Sikorski, and I.V. Babich, *Journal of Vacuum Science and Technology B* **20** 2788-2792 (2002).

[7] C.T. Black, K.W. Guarini, Y.Zhang, H. Kim, J. Benedict, E. Sikorski, I.V. Babich, and K.R. Milkove, *IEEE Electron Device Letters* **9** 622-624 (2004).

[8] S.B. Darling, *Progress in Polymer Science* **32** 1152-1204 (2007).

[9] Y.H.Ting, S.M. Park, C.C. Liu, X.S. Liu, F.J. Himpsel, P.F. Nealey, and A.E. Wendt, *Journal of Vacuum Science and Technology B* **26** 1684-1689 (2008).

[10] C.J. Hawker, and T.P. Russell, *MRS Bulletin* **30** 952-966 (2005).

[11] M.F. Zhang, L. Yang, S. Yurt, M.J. Misner, J.T. Chen, E.B. Coughlin, D. Venkataraman and T.P. Russell, *Advanced Materials* **19** 1571-1576 (2007).

[12] D. Zschech, D.H. Kim, A.P. Milenin, R. Scholz, R. Hillebrand, C.J. Hawker, T.P. Russell, M. Steinhart, U. Gosele, *Nano Letters* **7** 1516-1520 (2007).

[13] R. Ramanathan, M. Nettleton, S.B. Darling, *Thin Solid Films* **517** 4474-4478 (2009).

[14] J.Y. Cheng, A.M. Mayes and C.A. Ross, *Nature Materials* **3** 823-828 (2004).

[15] Y.S. Jung and C.A. Ross, *Nano Letters* **7** 2046-2050 (2007).

[16] R.F. Pierret, *Semiconductor Device Fundamentals*, Addison Wesley, 1996.

# Chapter 3

# Characterization Techniques and Metrology for S2σ and *ZT* Device Sets

In this chapter, we perform characterizations and describe measurement methods (metrology) for both the $S^2\sigma$ and *ZT* device sets. For the $S^2\sigma$ device set, we first characterize the nanomesh feature with scanning electron microscopy (SEM) and the strain level in SSOI with Raman spectroscopy. Then we describe the measurement methods for electrical conductivity and thermopower from two devices to determine the power factor of strained and unstrained silicon thin films with nanomesh; two measurement setups in a temperature-controlled vacuum cryostat are used. Electrical conductivity was normalized for nanomesh samples with a correction factor obtained from COMSOL simulation.

For the *ZT* device set, we first characterize the nanomesh features in the ~100 nm thick silicon thin film with scanning electron microscopy (SEM) and ellipsometry, and characterize the boron doping concentration with secondary ion mass spectroscopy (SIMS). We then describe the measurement methods for thermopower, electrical

resistivity, and thermal conductivity to obtain *ZT* from one chip around room temperature in a custom-designed vacuum setup.

## 3.1 S²σ device set characterization techniques and metrology

## 3.1.1 S²σ device set characterization techniques

Here we conduct scanning electron microscopy (SEM) for nanomesh morphology and confocal Raman spectroscopy to characterize the partial strain relaxation in the strained silicon nanomesh thin film.

## 3.1.1.1 Scanning electron microscopy

Nanomesh structures in strained silicon thin films were characterized with SEM (Hitachi SU8000). The plan-view image (Figure 3.1, a) showed a homogeneously arrayed nanomesh feature. This hexagonally arranged structure (Figure 3.1, a inset) has holes with ~18 nm diameter and ~36 nm pitch. It extended throughout the whole sample except for occasional defects such as merging holes. The cross-sectional SEM image (Figure 3.1, b) also confirmed that RIE etched through the strained silicon thin film and stopped at the buried oxide layer. The thin film thickness was 5 nm, as measured by atomic force microscopy (AFM, NanoMan). A similar structure reported by Peidong Yang's group, with 55 nm pitch and 100 nm film thickness, showed a thermal conductivity of 1.14-2.03 W/m·K at 300 K. [1]  An even lower value could be achieved by the nanomesh structure described in this chapter. After the nanomesh feature had been confirmed, Raman

spectroscopy was used to examine the strain level in SSOI before and after nanomesh formation.
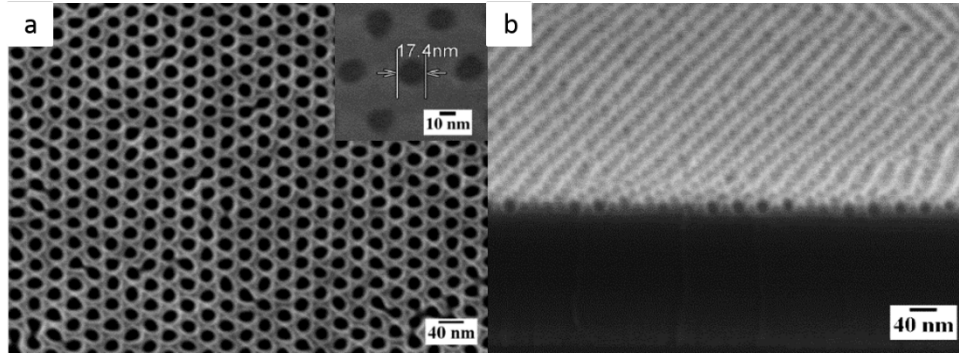


**Figure 3.1 SEM image of a nanomesh patterned strained silicon layer. (a) Top view (inset, hexagonally arranged nanomesh pattern with diameter of 17.4 nm); (b) Cross-sectional view.**

## 3.1.1.2 Confocal Raman spectroscopy

Raman spectroscopy is a spectroscopic technique that characterizes chemical bonds and molecular vibrational and rotational modes in a system. It is commonly used to study crystal structures. The strained silicon thin films before and after being engineered with a nanomesh were examined with confocal Raman microscope (inVia, Renishaw Inc) to confirm the tensile strain level. The amount of strain in silicon thin films can be detected with this technique from the peak shift of Raman scatterings between Si-Si and Si-SS (strained silicon) modes.

Confocal Raman microscopy was conducted on the following samples: a bulk silicon substrate, an intrinsic SSOI sample, an SSOI sample stripped of the strained silicon layer, and n-doped SSOIs with 5 nm thick tensile strained silicon thin films before and after nanomesh formation. A 514 nm laser source was used to excite Raman

scattering peaks, and a 100X Leica microscopic lens was employed to capture the scattered light.

The bulk silicon sample, with a resistivity of 10-20 ohms·cm, showed a Si-Si peak at 521 cm$^{-1}$ (Figure 3.2). It is consistent with data collected from relaxed silicon. The SSOI sample without a top strained silicon layer (removed by XeF$_2$ etching in Xactix) also exhibited the same peak coming from the silicon substrate beneath a 150 nm thick buried oxide layer in SSOI. Both intrinsic and n-doped SSOI samples without nanomesh had a distinctive red-shifted Si-SS peak at 515.9 cm$^{-1}$. It indicated a Raman shift of 5.1 cm$^{-1}$ (Equation 3.1) and a strain level of 0.7% (Equation 3.2). [2] The n-doped SSOI with nanomesh showed a slight strain relaxation due to the voids in the thin film. It confirmed that the tensile strain was still retained after nanomesh engineering. Also, all SSOI samples demonstrated the same bulk silicon peak at 521 cm$^{-1}$ from the silicon handle.

$$\Delta\omega = \omega_{Si(Bulk)} - \omega_{Si(Strained)} \tag{3.1}$$

$$\varepsilon = 1.38 \times 10^{-3} \Delta\omega \tag{3.2}$$

($\Delta\omega$ is the wavenumber shift or Raman shift; $\omega_{Si(Bulk)}$ is the wavenumber of bulk silicon peak; $\omega_{Si(Strained)}$ is the wavenumber of the strained silicon peak, and $\varepsilon$ is the strain in the silicon.)
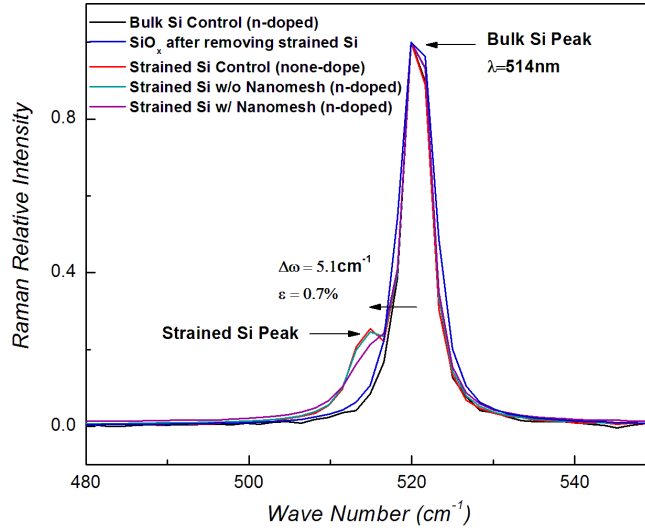
**Figure 3.2 Confocal Raman microscopy spectra with relaxed and strained silicon peaks at 521 cm $^{-1}$ and 515.91 cm $^{-1}$, respectively, with 514 nm laser excitation. A set of samples were measured to verify the source of the redshift: black curve - a relaxed silicon control sample, slightly n-type doped; purple curve - SiO$_x$ layer from SSOI after removing the strained silicon film with XeF$_2$ etching; blue curve - undoped strained silicon film on SSOI; orange curve - heavily n-doped strained silicon film on SSOI without nanomesh; green curve-heavily doped strained silicon film on SSOI with 18 nm-diameter nanomesh.**

## 3.1.2 S$^2$σ device set metrology

After the device characterization described above, the SSOI samples and the SOI control samples were patterned by photolithography, and metallic contact pads were deposited on the electrical conductivity and thermopower devices. For convenience, the metrology of the device set is described using the SSOI sample, while the SOI control samples were measured with the same metrology. Data was collected under controlled temperature and vacuum conditions.

### 3.1.2.1 Cryostat system

A cryostat (Janis VPF500) provided vacuum and temperature control during measurements. A turbo vacuum pump (HiPace 80, Pfeiffer Vacuum GmbH) was used to

pump the cryostat chamber down to $10^{-6}$ mtorr. A temperature controller (LakeShore 335, Lake Shore Cryotronics, Inc) balanced heating from an embedded heater in the sample stage and cooling from liquid nitrogen. The cryostat was connected to nanovoltmeters (Keithley 2400) for electrical conductivity and thermopower measurements (Figure 3.3).
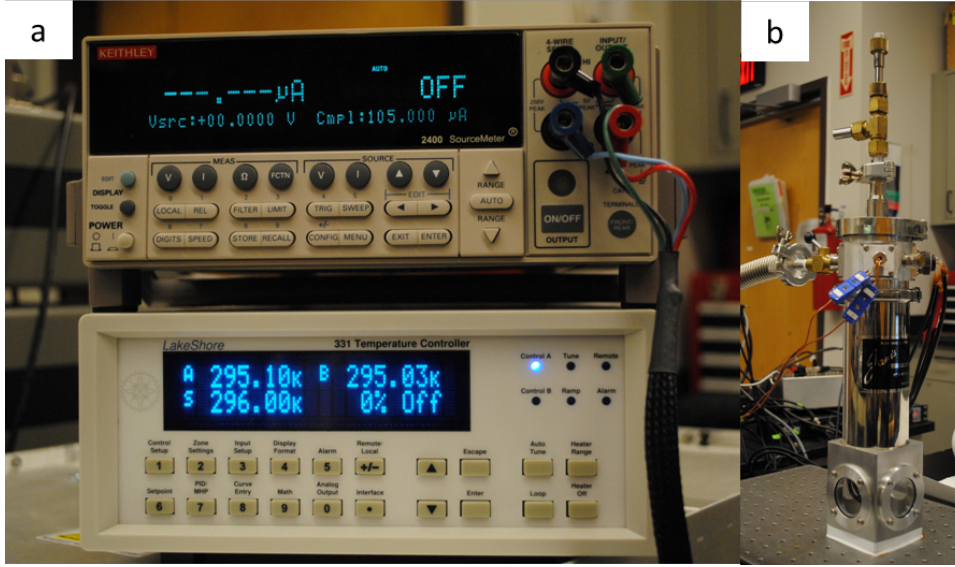


**Figure 3.3  Cryostat measurement setup.  (a) Measurement instruments: sourcemeter and temperature controller; (b) Cryostat.**

A SSOI sample was mounted to a chip carrier sitting in the cryostat sample stage (Figure 3.4, a). For electrical conductivity measurements, each pin of the chip carrier was connected from behind the sample stage to an electrical feedthrough (Figure 3.4, b). For thermopower measurements, two twisted pairs of Ph-Br wires (Cu (94.8%), Sn (5%), Ph (.2%); .005 in OD, polyimide insulation) were used for voltage measurement to lower the noise level (through a second electrical feedthrough not shown here). Also, type T (copper–constantan) thermocouples used for temperature measurement were installed through the temperature feedthrough (Figure 3.4, b).
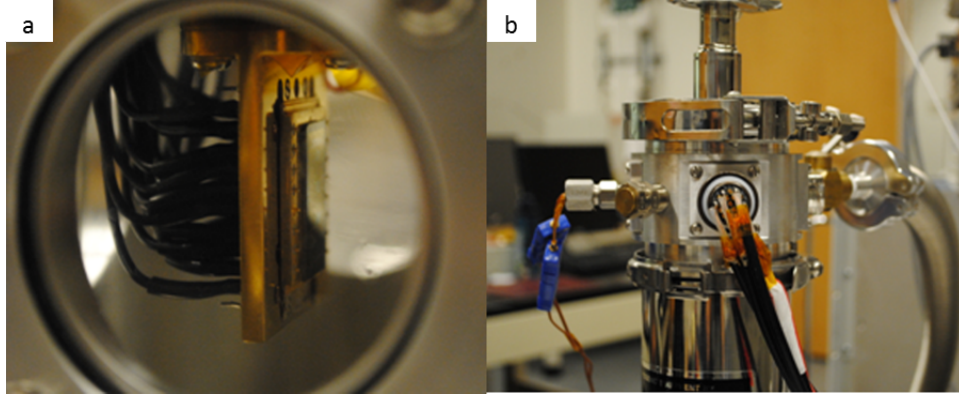
**Figure 3.4 Electrical conductivity and thermopower measurements conducted in cryostat with temperature and vacuum controls. (a) SSOI mounted on a chip carrier sitting in a cryostat sample stage. Pins on the chip carrier were connected to an electrical feedthrough; (b) Electrical and thermocouple feedthroughs on the cryostat shell.**

## 3.1.2.2 Electrical conductivity measurement

The electrical conductivity was measured from a SSOI sample with a modified four-point probe method in the above described cryostat system. A COMSOL simulation was conducted to compensate for the presence of nanomesh in strained silicon thin film.

- **Modified four point probe method**

The electrical conductivity measurements were based on the traditional four-point probe method. [3] The approach was to obtain the sheet resistance $R_s$ of the semiconductor thin film and then convert it to electrical conductivity (Equations 2.4, 3.3).

$$\sigma = \frac{1}{\rho} \qquad (3.3)$$

($\rho$ is the electrical resistivity; $\sigma$ is the electrical conductivity, reciprocal to the electrical resistivity.)

Classically, the four-point probe measurement is conducted on a probe station by bringing four probes in contact with the surface of the semiconductor thin film, supplying

current between the outer two probes, and measuring the voltage drop across the inner two probes. The four probes are evenly distributed, and the probe spacing should be much larger than the thickness of the thin film (i.e., s>>t, where s is the probe spacing). To measure the electrical conductivity as a function of temperature (200 K-380 K) in this study, the method in which probes contacted a thin film was modified. First, rows of metallic contact pads (150 μm X 150 μm) were deposited with equal spacing (1000 um) on strained silicon thin films, parallel to the sample edges. The SSOI sample was attached to a chip carrier with silver paste (silver paste plus, SPI Supplies/Structure Probe, Inc.). Then, four adjacent contact pads in a row were wirebonded to the chip carrier (Figure 3.5, a). The chip carrier was subsequently mounted to the sample stage of the cryostat. Four contact pads were connected to a sourcemeter (Keithley 2400) via the electrical feedthrough of the cryostat (Figure 3.5, b). The 4-wire function of the sourcemeter measured and displayed the sheet resistance directly. Ten data points were averaged per temperature point, and the temperature was ramped from 200 K to 380 K in 10 K increments.
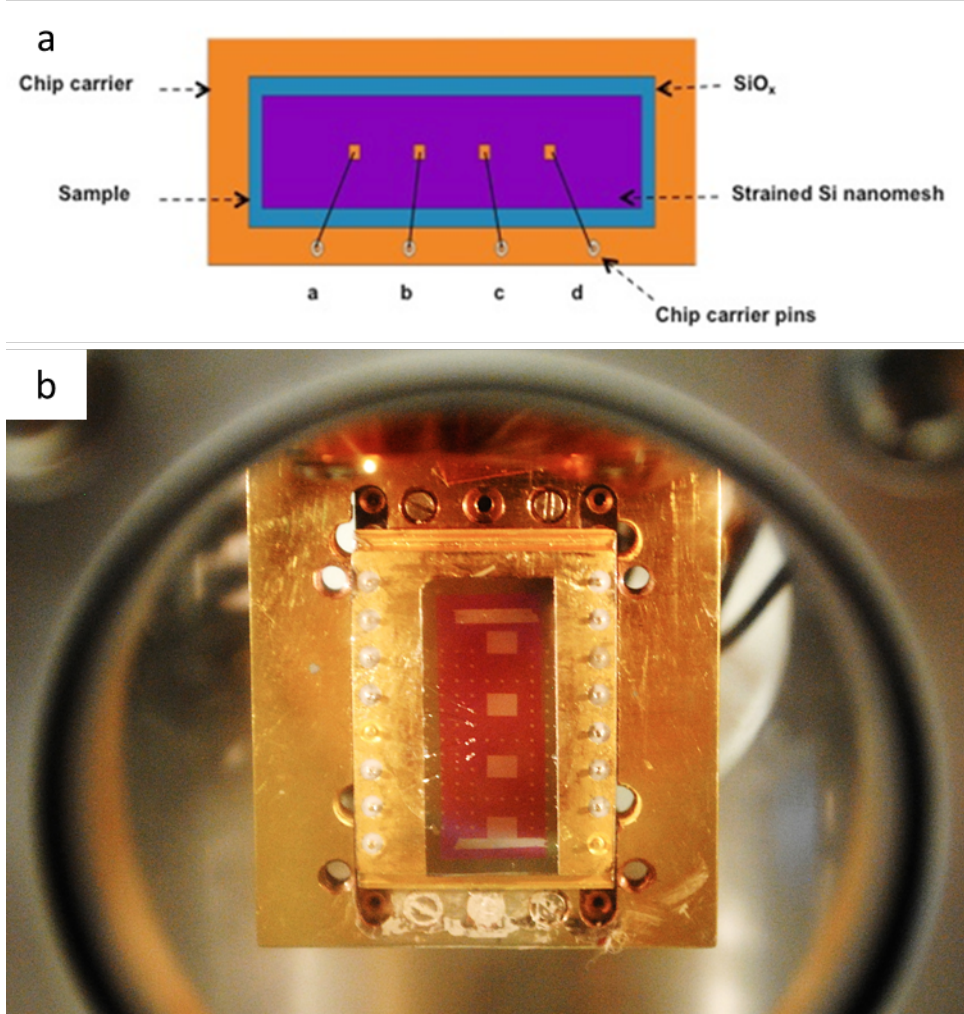
**Figure 3.5 Electrical conductivity devices. (a) SSOI sample with four contact pads wirebonded to the chip carrier; (b) Chip carrier mounted to cryostat's sample stage with four contact pads wirebonded to chip carrier pins.**

The sheet resistance of the strained silicon thin film was calculated from the four-point probe measurements (Equation 3.4) and plotted as a function of temperature (Figure 3.6). The sheet resistance of both strained silicon and unstrained silicon with and without nanomesh was collected and converted into electrical conductivity.

$$R_s = \frac{\pi}{\ln 2} \frac{V}{I} \approx 4.53 \times \frac{V}{I} \qquad (3.4)$$

(I is the current passing through the two outer probes; V is the voltage across the two inner probes)
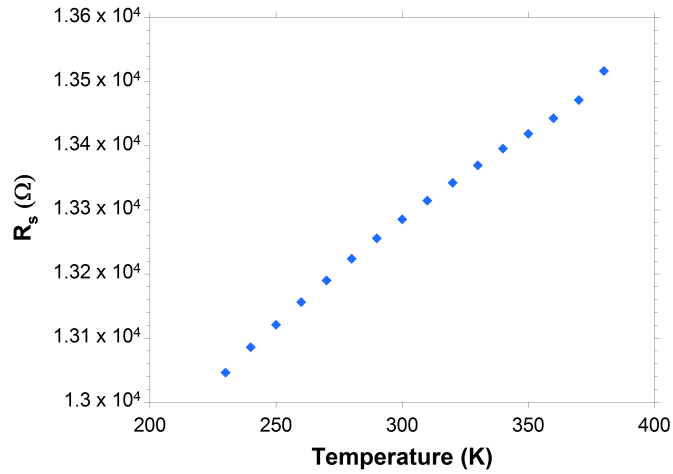


**Figure 3.6 Temperature dependence of sheet resistance in strained silicon thin film without nanomesh.**

The advantage of using the four-point probe method is to eliminate probe resistance, probe contact resistance, and spreading resistance from the measurement results (Figure 3.7). [3] In this study, the probe spacing (1000 μm) was much larger than the thickness of the strained silicon thin film (5 nm). Probes were also sufficiently far away from the sample edges to avoid measurement artifacts. To avoid any leakage, the edges of the strained silicon thin film were etched away by $XeF_2$ (Xactix, Xactix Inc.), and the exposed $SiO_x$ provided good insulation between the strained silicon layer and the bulk silicon handle (Figure 3.5, a)
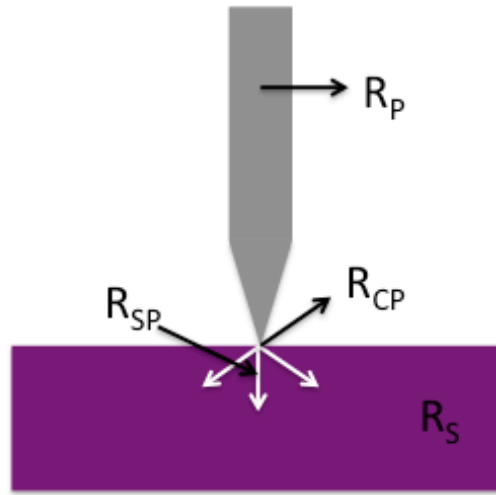
**Figure 3.7 Four-point probe measurement of silicon thin film sheet resistance ($R_P$: probe resistance; $R_{CP}$: probe contact resistance; $R_{SP}$: probe spreading resistance; $R_S$: silicon thin film sheet resistance).**

The presence of nanomesh structures introduced inhomogeneity in strained silicon thin films. A COMSOL simulation was conducted to introduce a correction factor to account for the porosity. This normalization was directly related to the measured sheet resistance.

- **COMSOL simulation**

Classically, a homogeneous film is required in the four-point probe method for thin film resistivity measurement. A correction factor is included in this work due to the presence of a nanomesh structure. In the COMSOL simulation, the resistance of a plain block without nanomesh was measured as the norm. Models 1 to 4 gradually added the variables such as nanomesh diameter, neck between holes (the length of silicon between two holes), and hole arrangements (Table 3.1). It was found that the resistance of thin films with nanomesh structures was larger than the norm. The geometrical factor should be considered while using the four-point probe method. Model 4 closely described the

hexagonally packed nanomesh structure employed in this study. A voltage of 0.5 V was applied on the films (Figure 3.8). The current density was integrated to determine current. The resistance of this thin film was then determined from Ohm's law:  it is 1.5 times the one from plain block (Table 3.1).  Consequently, in this study, a correction factor of 1.5 was used to compensate for the geometrical effect on the four-point probe measurements.

**Table 3.1 COMSOL simulation results of thin film resistance.**

| Model # | # of holes | Hole radius (nm) | Neck between holes (nm) | Normalized resistance |
|---|---|---|---|---|
| Plain block | 0 | n/a | n/a | 1 |
| 1 Base model | 64 | 9 | 18 | 1.49 |
| 2 Increased radius | 64 | 11 | 18 | 1.63 |
| 3 Increase spacing between holes | 64 | 9 | 20 | 1.44 |
| 4 Hexagonal lattice | 64 | 9 | 18 | 1.5 |
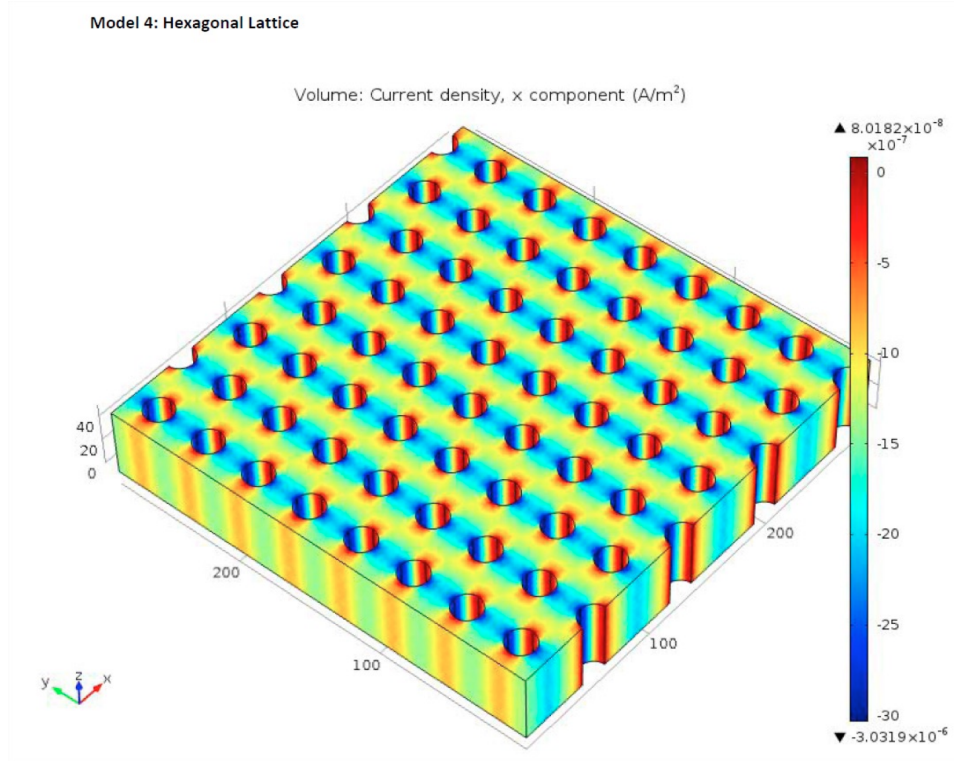
**Figure 3.8 COMSOL simulation of thin film current density in model 4, nanomesh with hexagonal lattice and 18nm diameter.**

## 3.1.2.3 Thermopower measurement

For the thermopower measurement, a temperature gradient was created across the sample (or device), while temperature and voltage drops were measured simultaneously by two nanovoltmeters. A Labview program was created to record and collect data. Here, a strained silicon without nanomesh sample was used as an example to describe the metrology. The temperature dependence of thermopower from this sample was provided, as well as error analysis.

- **Measurement setup**

The bottom left side of a SSOI sample was attached to the sample stage of the cryostat, and the bottom right side of the SSOI sample was attached to a Kapton heater (Figure 3.9); silver paste was used for attachment. When the Kapton heater was turned

on, a temperature gradient was generated from left to right. The Kapton heater served as a heat source while the temperature controlled sample stage served as a heat sink. On the SSOI sample, two metallic contact pads had been previously deposited, approximately 1 cm apart. Both temperature and voltage data were measured from these pads simultaneously by two nanovoltmeters (Keithley 2182A). Two pairs of twisted Ph-Br wires were used for voltage measurement to lower the noise level. Two type T (copper–constantan) thermocouples were soldered with indium onto two contact pads to measure a temperature difference. Good electrical and thermal contacts were required to ensure the accuracy of measurement, as well as a vacuum and cryogenic environment to avoid noise and contamination from the surroundings.
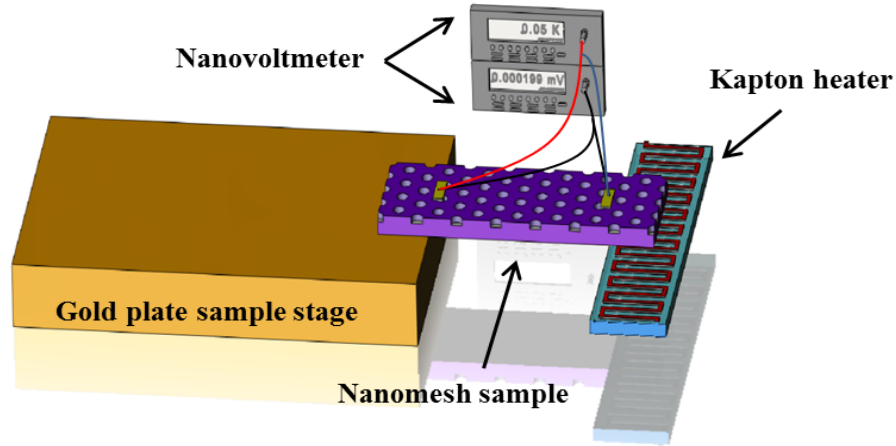


**Figure 3.9 Thermopower measurement setup in cryostat simultaneously collecting voltage and temperature data.**

- **Labview program**

For thermopower measurements, a Labview program was designed to activate and record signals (Figure 3.10, a). The current through the Kapton heater started from zero ($I_0$) then increased by five steps as $I_{i+1} = \sqrt{i+1}I_i$ to obtain a similar step-size in voltage

91

and temperature drop ($\Delta V$, $\Delta T$) across the sample; here, i is an integer index from 1 to 4, $I_{i+1}$ is the heater current at the (i+1)-th step, and $I_1$ = 100 mA. At each step, 800 datapoints were recorded, and a steady-state plateau was always established before the heater current was increased. In order to verify that the measured voltage drop $\Delta V$ was indeed a result of the temperature gradient, the current polarity of the Kapton heater was reversed after the third step. The measured voltage was the same as the value before the reversal (Figure 3.10, b). At each step, the last 50-100 datapoints for $\Delta V$ and $\Delta T$ were averaged. The linear slope from $\Delta V$- $\Delta T$ was then taken as the Seebeck coefficient or thermopower. As a result, we obtain the dependence of thermopower on temperature (Figure 3.11); the inset shows typical error bars, calculated as standard deviation from fitting of thermopower with six data sets at each measured temperature, with a magnitude of approximately 0.3 $\mu V/K$.

The unstrained silicon samples (or devices) with nanomesh and without nanomesh were also mounted and measured following the same procedures described above. The results are used for comparison with the strained silicon samples with nanomesh and without nanomesh in chapter 4.
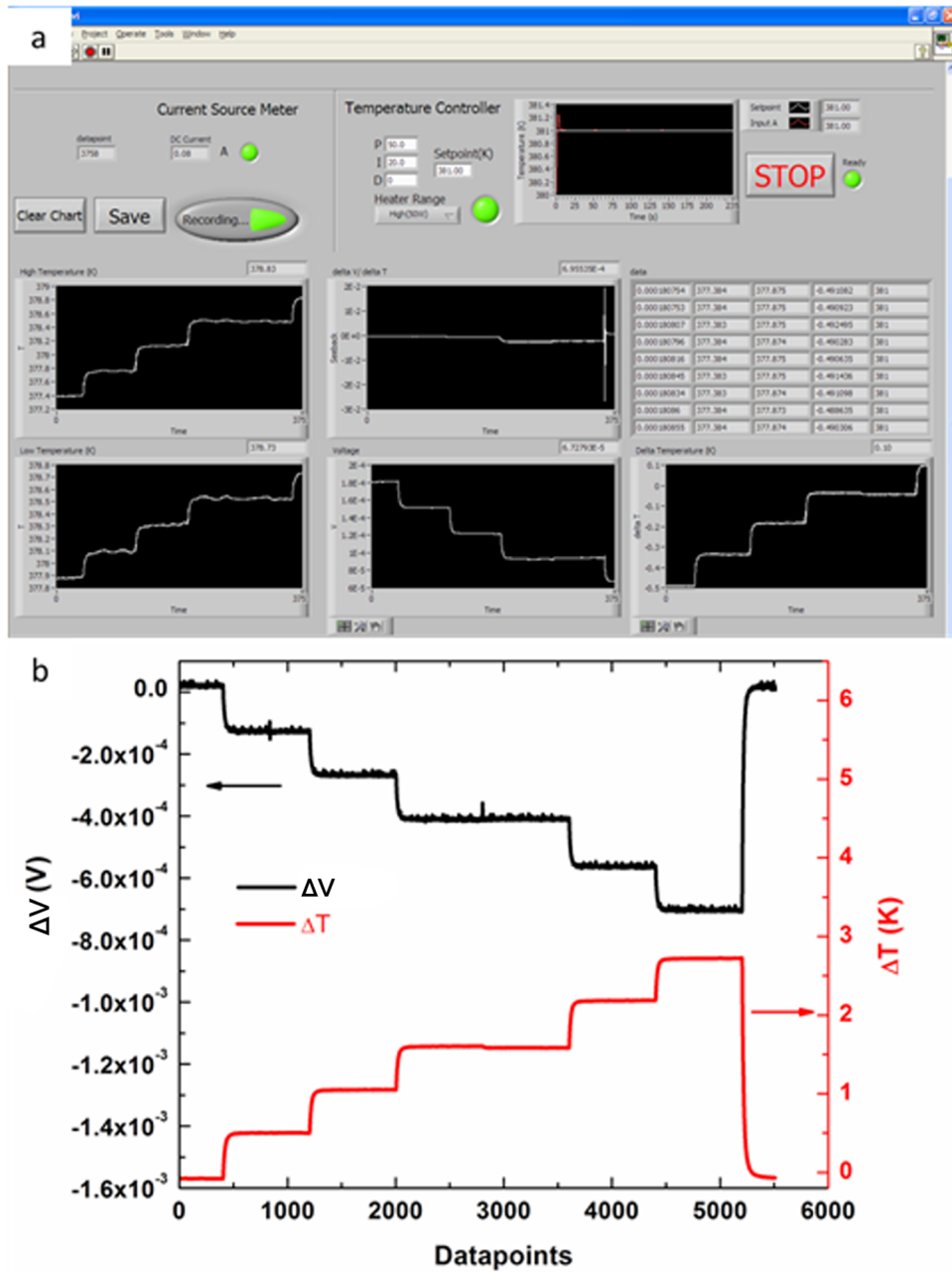
**Figure 3.10 Labview program used to activate and record voltage and temperature drops from a SSOI sample. (a) The program interface showing the Kapton heater current, voltage and temperature drops from SSOI sample, and sample stage temperature; (b) The recorded data for ΔV and ΔT, with five plateaus triggered by the increase in Kapton heater current.**
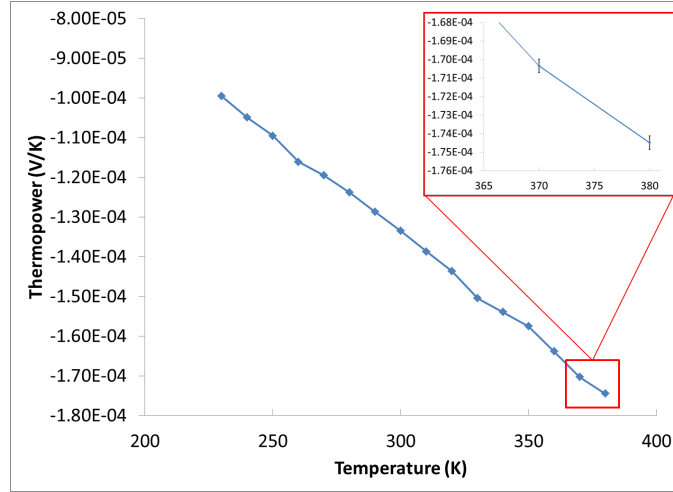
**Figure 3.11 Temperature dependence of the thermopower of strained silicon without nanomesh.**

## 3.2 *ZT* device set characterization techniques and metrology

### 3.2.1 *ZT* device set characterization techniques

The characterization techniques such as SEM, ellipsometry and SIMS were applied to the ~100 nm thick silicon nanomesh thin film. The results are shown below.

### 3.2.1.1 Scanning electron microscopy

The nanomesh structure in the ~100 nm thick silicon thin film was imaged by SEM (JEOL 3011, JEOL USA, Inc.). The plan-view (Figure 3.12, a) showed a homogeneous, hexagonally arrayed nanomesh pattern. The cross-sectional view (Figure 3.12, b) showed silicon thin film fully etched through with straight sidewalls, and the plasma etching stopped at the buried oxide layer. Occasionally, defects such as unpatterned areas and grain boundaries were observed due to irregularities in the block copolymer self-assembly. Based on the SEM images, the nanomesh diameter was

measured to be ~53 nm after etching. The porosity of nanomesh (the ratio of the area of holes to the total surface area) was approximately 40%. Next, an ellipsometry technique was used to measure the film thickness of the silicon and buried oxide. The porosity of the silicon nanomesh was also measured by ellipsometry; the value of porosity measured by ellipsometry was then compared to the value measured by SEM.
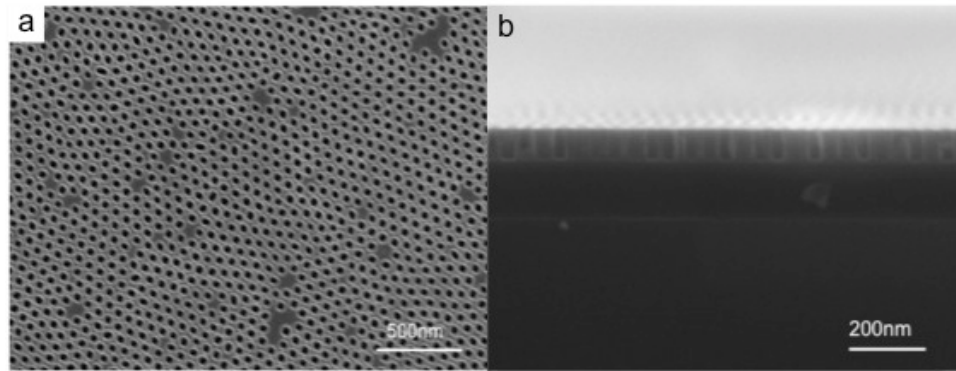


**Figure 3.12 SEM images of nanomesh patterned silicon thin film. (a) Top view of nanomesh pattern; (b) Cross-sectional view of thoroughly etched silicon thin film.**

## 3.2.1.2 Ellipsometry result

The ellipsometer (Woollam M2000, J.A. WOOLLAM CO. Inc.) was used to estimate the film thickness of both the top silicon and buried oxide layers in the SOI sample and the nanomesh porosity in the silicon layer by measuring the amplitude and phase changes between the reflected light and the incident light. The top silicon nanomesh and buried oxide layers were measured to be 912.13 Å thick and 1989.48 Å thick, respectively; the nanomesh porosity was measured to be 41.5%. Both the thickness and porosity results fall into a reasonable range compared with the SOI substrate specifications on film thickness and the porosity calculated from the previous SEM images.

### 3.2.1.3 Secondary ion mass spectroscopy result

SIMS was conducted on a monitor SOI sample without a nanomesh pattern to characterize the doping level of boron after ion implantation (Figure 3.13). The result showed that the level of boron was ~$2 \times 10^{19}$ atoms/cm$^3$, and the ions were uniformly distributed within the silicon film. This analysis also detected low-level concentrations of phosphorus (P), antimony (Sb), and arsenic (As) atoms, which are common contaminants from the rapid thermal annealing furnace during implant activation; however, the amount of these impurities ($10^{16}$ - $10^{17}$ atoms/cm$^3$) should not affect this study.
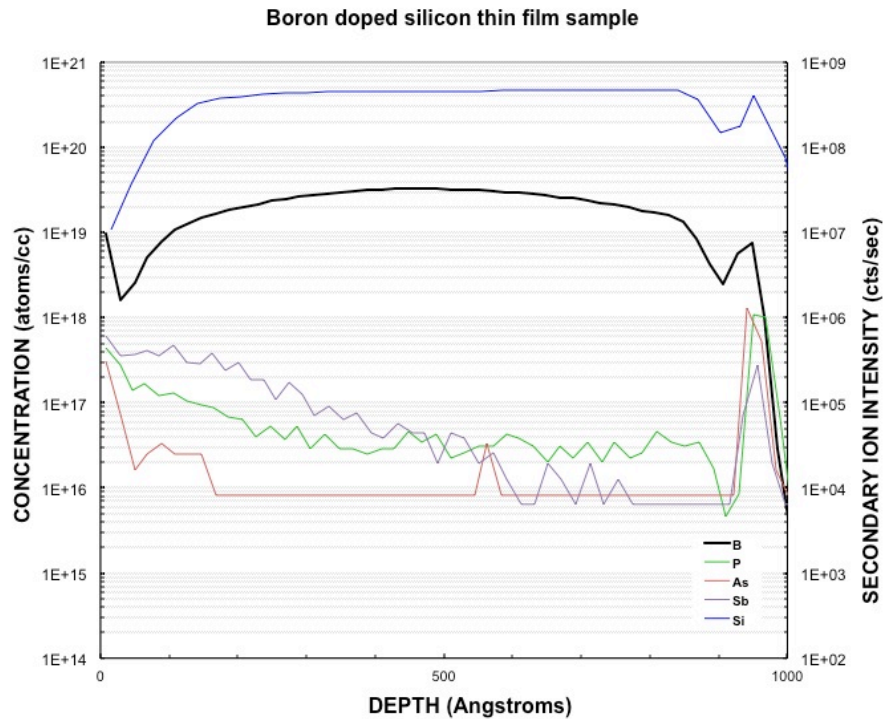


**Figure 3.13 Secondary ion mass spectroscopy (SIMS) result on monitor SOI after boron implantation and activation.**

### 3.2.2 *ZT* device set metrology

After sample characterization, three devices were fabricated on the same chip for thermopower, electrical resistivity, and thermal conductivity measurements to obtain *ZT*.

96

Data was collected from a custom-designed apparatus with sample temperature control under desired vacuum to avoid thermal convection between the sample and air (Figure 3.14).
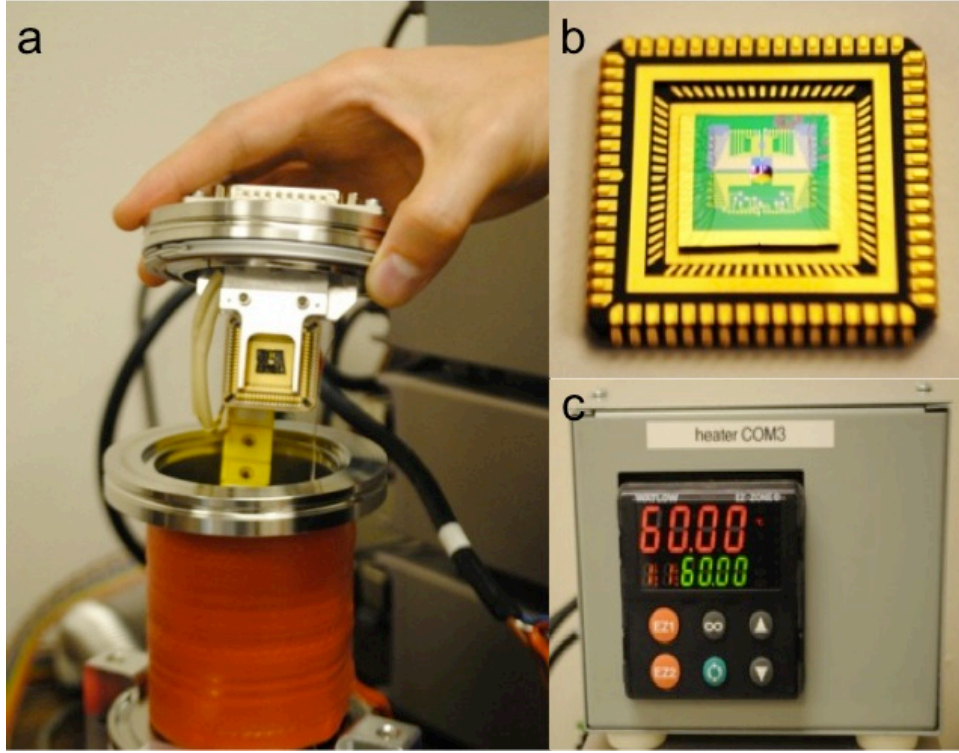


**Figure 3.14 *ZT* device set measurement setup pictures. (a) A custom-designed apparatus sealed by vacuum; (b) *ZT* measurement sample wirebonded to a chip carrier. The chip carrier was fixed on the cryostat stage in (a); (c) A PID global temperature controller.**

## 3.2.2.1 The thermopower measurement

The thermopower (S) was measured by a linear fit of voltage and temperature differences across the nanomesh sample using two resistive thermometers, $S=-\Delta V/\Delta T$, where $\Delta V$ is the voltage difference and $\Delta T$ is the temperature difference. As described below, the temperature difference was measured with two spaced-apart resistive thermometers, and the voltage drop across the two thermometers was also measured. First, a 500 μm X 500 μm silicon nanomesh pad was patterned and sectioned using

photolithography and RIE (Figure 3.15). Two 10 μm-wide platinum heating coils (the right one was a backup heater) were deposited, after photolithography patterning on both sides of the nanomesh pad. The length of the heaters was ~1500 μm, three times as long as the nanomesh pad. A temperature gradient across the nanomesh pad was generated when a DC current was supplied to the left heater. The heater was considered to provide a one-dimensional heating profile, and the healing length $L_H$ of the sample is calculated below. Two resistive thermometers were located on two edges of the nanomesh pad. Each thermometer was designed for a four-point resistance measurement to eliminate the effect of the contact resistance between the bonding wires and the metal contact pads, and to eliminate the effect of the dependence of resistance on temperature in the bonding wires.
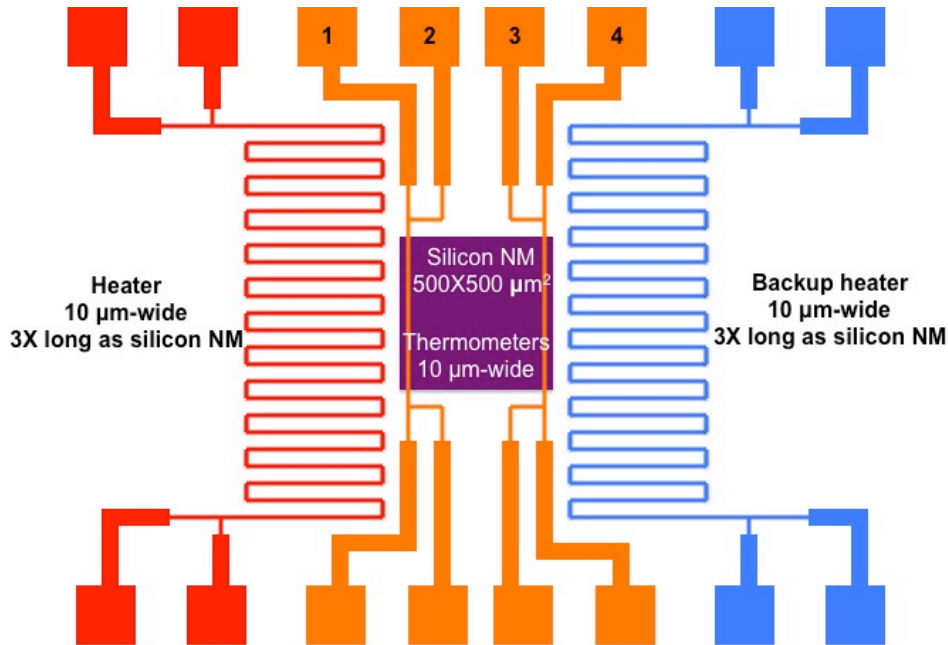


**Figure 3.15 Illustration of thermopower measurement by using one heater and two thermometers. Both voltage and temperature difference between two thermometers under a temperature gradient generated by the left heater were measured, and the linear fit of ΔV and ΔT gives the thermopower.**

- **The healing length**

The healing length is a length scale at which the heat loss in the sample is dominated by the thermal radiation, and the temperature of the material is not affected by thermal disturbance from the heater so that it is equal to the environment temperature. It can be used to characterize how far the thermometer's heater can create a temperature change in the sample in a steady state. A detailed derivation of the healing length is provided later in section 3.2.2.3, and it is given below (Equation 3.5).

$$L_H = \sqrt{\frac{\kappa d}{2h}} \qquad (3.5)$$

($L_H$ is the healing length; $\kappa$ is the thermal conductivity; d is the thickness of the sample; and h is the heat transfer coefficient, where h=10 W/m$^2$•K for air)

In this study, the thermopower was measured from a stack structure of silicon nitride (~29 nm thick), silicon nanomesh (~91 nm thick), silicon oxide (~196 nm thick) and bulk silicon handle (~680 μm thick) (Figure 3.16). Due to the large contact area between the metal heater and the substrate and the presence of the bulk silicon (which has a thermal conductivity of 150 W/m•K), it is believed that the heat conduction downwards through the stack of layers ($q_1$) is faster than the lateral heat conduction ($q_2$) in the sample. The lateral heat conduction corresponds to the heat conduction from the left heater to the right in Figure 3.15.
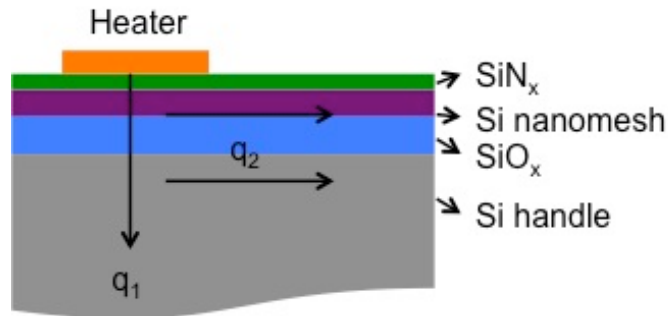
**Figure 3.16 The stack structure of silicon nitride (SiN$_x$), silicon nanomesh, silicon oxide (SiO$_x$) and bulk silicon handle with two directions of heat conduction: heat conduction downwards through the stack of layers (q$_1$), and heat conduction in the sample from the left to right (q$_2$).**

The thermal conductivity of this lateral conduction (q$_2$) can be estimated (Equation 3.6) based on the conservation of thermal conductance, $K = \sum_{i=1}^{4} \kappa_i \frac{A_i}{\ell}$, where K is the thermal conductance of the four-layer stack; i = 1 − 4 is the index of a layer; $\kappa_i$ is the thermal conductivity of the layer i; A$_i$ is the cross-sectional area of thermal conduction of the layer i, where A$_i$ is calculated from the product of the length of the heater (~1500 μm) and d$_i$ (the thickness of the layer i); and $\ell$ is the length of the conduction, which is the same for all layers. Based on equation 2, $\kappa d \cong \kappa_{Si\,handle} d_{Si\,handle}$ due to the dominant thermal conductivity and film thickness in the silicon handle.

$$\kappa d = \kappa_{SiNx} d_{SiNx} + \kappa_{Si} d_{Si} + \kappa_{SiOx} d_{SiOx} + \kappa_{Si\,handle} d_{Si\,handle} \tag{3.6}$$

Also, the heat transfer coefficient h satisfies the relation h < 10 W/m$^2$•K for the sample measured in a vacuum setup. Therefore, the estimate of $\kappa$d in Equation 3.5 along with an upper bound of h give the lower bound of the healing length to be approximately 71500 μm when the steady state is established, much larger than the width of the silicon nanomesh pad, 500 μm. The entire nanomesh pad was under the influence of heat conduction from the left heater, and the left thermometer had a larger temperature change than the right one.

- **Thermometer calibration**

The resistive thermometers were used to measure the local temperature, and yield ΔT across the nanomesh pad. The temperature measurement is based on the linear

dependence of the resistance of the thermometer on temperature, dR/dT, where R is resistance of the thermometer and T is the temperature. The resistances of the two thermometers were measured when the temperature was controlled by a PID temperature controller for the entire chip with a feedback thermocouple mounted on the chip. Seven reference temperature values (at equilibrium) were chosen within 303-336 K while an AC current of 0.1 mA (the AC peak current) was sent to each resistive thermometer from a DC and AC current sourcemeter (6221 DC and AC current source, Keithley, Inc.) and the corresponding AC voltage was measured with a lock-in amplifier (Stanford Research SR830, SRS, Inc.) at every reference temperature to obtain the resistance of the thermometer. The linear relationship of thermometer resistance and the temperature was obtained for calibration, and the slope of the linear fit provided dR/dT (Figure 3.17). The calibration yielded 0.1603 $\Omega$/K and 0.1595 $\Omega$/K for the left and right thermometer based on Figure 3.15, respectively.



| | slope ($\Omega$/K) | $R^2$ |
|---|---|---|
| left thermometer | 0.1603 | 0.9998 |
| right thermometer | 0.1595 | 0.9999 |
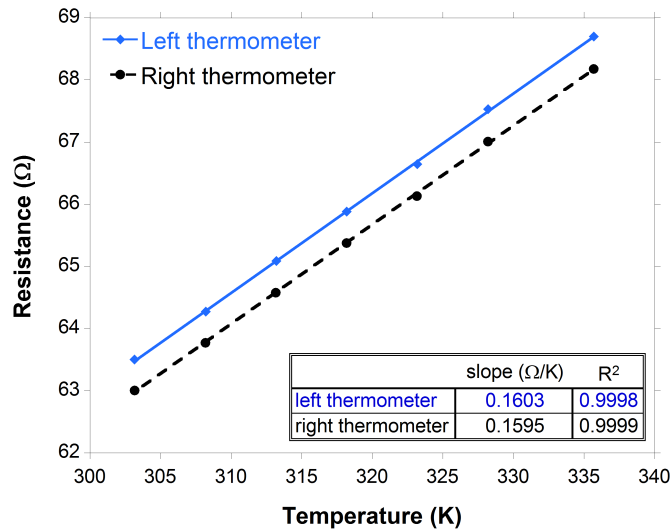
**Figure 3.17 The plot of the resistance of both thermometers as a function of sample temperature.**

- **ΔT measurement**

101

The temperature difference between the two thermometers was measured by ramping the heater current in 1 mA increments while simultaneously measuring the resistance of each thermometer. First, a DC current was supplied to the left heater in Figure 3.15 to create a temperature gradient across the nanomesh pad. Then, the DC and AC current sourcemeters and lock-in amplifiers were paired up again to obtain the resistance of each thermometer. The temperature of each thermometer was elevated by less than 0.5 K above 303 K when the maximum heater current was 2 mA. Such temperature change was related to its individual resistance change using dR/dT (Equations 3.6-3.7).

$$\Delta T_{left} = \frac{R_{left} - R_{0,left}}{[dR/dT]_{left}} \tag{3.6}$$

$$\Delta T_{right} = \frac{R_{right} - R_{0,right}}{[dR/dT]_{right}} \tag{3.7}$$

($R_{0,\,left}$ and $R_{0,\,right}$ are the resistance of the left thermometer and the resistance of the right thermometer, respectively, at 303 K; $R_{left}$ and $R_{right}$ are the resistance of the left thermometer and the resistance of the right thermometer, respectively)

After equilibrium was established at 303 K, the resistance of each thermometer ($R_{left}$ and $R_{right}$) was averaged from 100 datapoints. The corresponding temperature change in each thermometer was related to the heater current in a parabolic relationship considering that the heat transferred through each thermometer was part of the Joule heating from the left heater ($Q = I_{heater}^2 R_{heater}$, where $I_{heat}$ is the heater current, and $R_{heat}$ is the heater resistance) (Figure 3.18). This result verified that the heat transfer mechanism on the silicon nanomesh was dominated by thermal conduction in vacuum, and thermal radiation and convection were negligible.
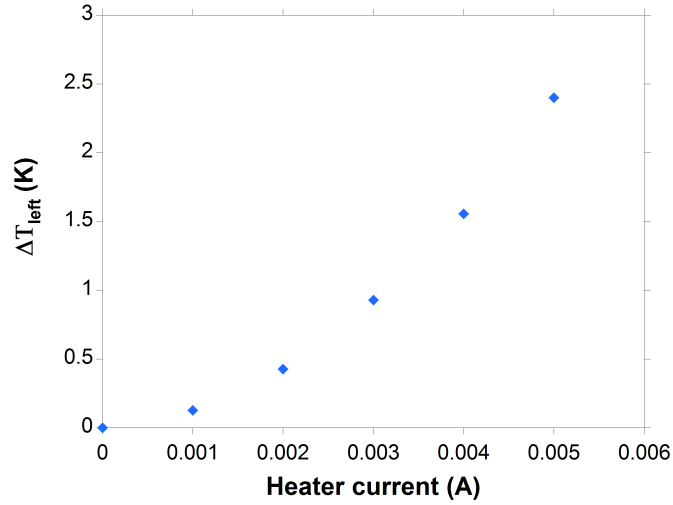
**Figure 3.18 The parabolic relationship between the temperature change of the left thermometer and the left heater current as a result of thermal conduction.**

Both thermometers showed the parabolic relationship indicated in Figure 3.18, while the left thermometer had a larger temperature change compared to the right one because it was in closer proximity to the left heater. Therefore, $\Delta T$ can be determined by subtracting $\Delta T_{right}$ from $\Delta T_{left}$ (Equation 3.8).

$$\Delta T = \Delta T_{left} - \Delta T_{right} \tag{3.8}$$

Next, the voltage difference between the two thermometers was also measured in order to obtain the linear fit for the thermopower.

- **ΔV measurement**

The thermoelectric voltage difference ($\Delta V$) between the two thermometers was measured by a nanovoltmeter (Keithley 2182A, Keithley Instruments, Inc.) in the presence of the temperature gradient along the nanomesh pad created by a DC current in the left heater (Joule heating). In order to verify the accuracy of the measurement, the current polarity in the left heater was reversed, and it did not affect the magnitude and

103

polarity of ∆V. Also the two thermometers extended to eight electrodes and contact pads based on the device design in Figure 3.15. Four combinations (electrodes 1-3, 2-4, 1-4, and 2-3) were chosen to measure the voltage difference between each pair of electrodes induced by heater current with increments of 1 mA. Meanwhile, ∆T was measured with the same heater current variation (Table 3.2).

**Table 3.2 The thermoelectric voltage and temperature difference measured from thermometer electrodes as the heater current was increased in 1 mA increments.**

|  | Heater current=0 mA | Heater current=1 mA | Heater current=2 mA |
|---|---|---|---|
| ∆V 1 (V) | $1.40 \times 10^{-6}$ | $3.76 \times 10^{-6}$ | $1.12 \times 10^{-5}$ |
| ∆V 2 (V) | $1.46 \times 10^{-6}$ | $4.04 \times 10^{-6}$ | $1.16 \times 10^{-5}$ |
| ∆V 3 (V) | $3.95 \times 10^{-6}$ | $6.46 \times 10^{-6}$ | $1.40 \times 10^{-5}$ |
| ∆V 4 (V) | $2.79 \times 10^{-6}$ | $5.30 \times 10^{-6}$ | $1.27 \times 10^{-5}$ |
| ∆T (K) | 0 | $4.05 \times 10^{-3}$ | $2.23 \times 10^{-2}$ |

The thermoelectric voltage measured when the heater current I = 0 mA was the base noise level from the nanovoltmeter. The slope of a linear fit from the ∆V versus ∆T plot provided the value of the thermopower. The fitting process was repeated for all four thermoelectric voltages in Table 3.2. The thermopower at 303 K was averaged based on the four results, and its value is given in chapter 5.

### 3.2.2.2 Electrical resistivity measurement

The electrical resistivity was also measured at 303 K by using a Greek cross structure based on the Van der Pauw method. The Van der Pauw method was initially used to measure the electrical resistivity of an arbitrarily shaped flat sample, without

knowing the current pattern, by making four negligible small contacts along the sample periphery (Figure 3.19). [3]
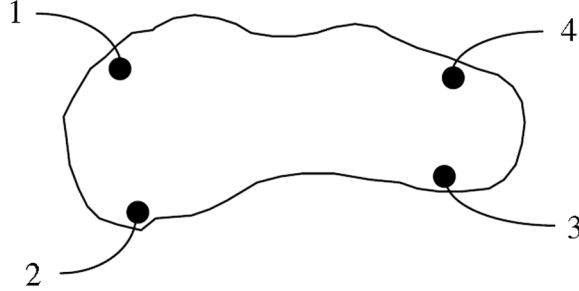


**Figure 3.19 Arbitrary shaped sample measured by the Van der Pauw method with four contacts. [3]**

The resistance of the sample is measured from four contacts 1, 2, 3, and 4 as indicated in Figure 3.19. For instance, $R_{12, 34}$ is obtained by a voltage measurement between contacts 3 and 4, when a current enters contact 1 and leaves contact 2 (Equation 3.9). $R_{23, 41}$ is also measured in a similar way. Both $R_{12, 34}$ and $R_{23, 41}$ are averaged to determine the electrical resistivity ($\rho$) of the sample (Equation 3.10).

$$R_{12,34} = \frac{V_{34}}{I_{12}} \tag{3.9}$$

$$\rho = \frac{\pi t}{\ln 2} \frac{R_{12,34} + R_{23,41}}{2} F \tag{3.10}$$

(t is the thickness of the sample; F is a function of resistance ratio $R_r = R_{12, 34} / R_{23, 41}$)

Also, F and $R_r$ are found to satisfy the following relation (Equation 3.11).

$$\frac{R_r - 1}{R_r + 1} = \frac{F}{\ln 2} \operatorname{arccos} h(\frac{\exp(\ln 2 / F)}{2}) \tag{3.11}$$

If the sample is a symmetrical circle or square (Figure 3-20), Equation 3.10 can be simplified due to $R_r = F = 1$ (Equation 3.12).

105

$$\rho = 4.532tR_{12,34} \tag{3.12}$$
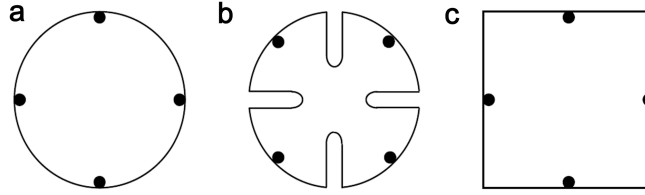


**Figure 3.20 Symmetrical sample shapes for Van der Pauw method. (a) Circular; (b) Cloverleaf; and (c) Square sample configurations. [3]**

The Van der Pauw method is very popular in integrated circuit technology because it requires a smaller metal contact size compared to the sample size. Compared to a cloverleaf (Figure 3.20, b), the circular and square configurations are easier to pattern using lithography. For a square, the placement of the contacts at the midpoints of the sides is better than at the corners, and it can be easily achieved (Figure 3.20, c). Thus, the required sample configuration evolves into a Greek cross structure where the contact size can be big compared with the sample size and it does not affect the measurement since only the shaded area is measured (Figure 3.21). This Greek cross structure was used in silicon nanomesh resistivity measurement at 303 K. After the sheet resistance has been measured, the electrical resistivity of the silicon nanomesh thin film is determined based on Equation 3.12.
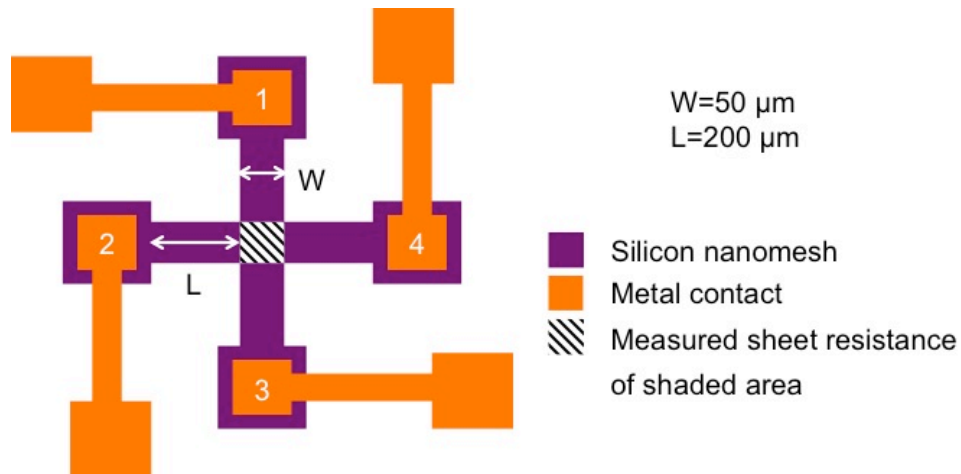
**Figure 3.21 Greek cross structure used in Van der Pauw method for silicon nanomesh resistivity measurement.**

## 3.2.2.3 Thermal conductivity measurement

The thermal conductivity was measured by a 2ω method, which is based on the well-known 3ω method, but using a second harmonic in a voltage signal instead of the third harmonic. Both methods are simple, quick and accurate in measuring the thermal conductivities in low-κ materials, such as dielectrics, porous materials and carbon nanotubes, [4-7] using frequency dependent temperature oscillations; a small sample size is used to reduce black body radiation. Both techniques are developed from the analysis of the heat conduction in a thin rod of small cross-section, as given by Carslaw and Jaeger. [8]

- **3ω technique**

The 3ω technique was first developed by Cahill [4] as a method to reduce the measurement errors arising from black body radiation from the surface of the sample in low-κ materials above 50 K. Before this, the thermal conductivities in solids were measured by a temperature gradient produced by a one-dimensional heat flow. [9-10] The

3ω technique uses a deposited metal line with width 2b on the sample to act as both a heater and a thermometer (Figure 3.22).
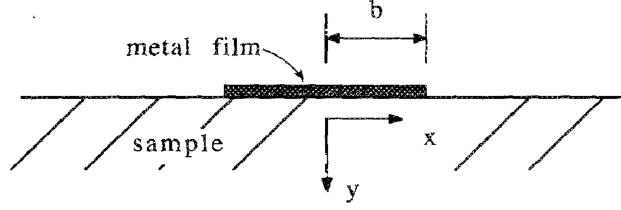


**Figure 3.22 Side view of the heater and sample geometry for the 3ω method.** [4]

When an AC current at an angular frequency ω is sent to the metal line, the heat power generated from it oscillates at a frequency 2ω because the Joule heating is related to the current by a quadratic function. The temperature at a distance r from the heater inside the sample, $r = \sqrt{x^2 + y^2}$ , also oscillates at 2ω frequency (Equation 3.13). [4]

$$\Delta T(r) = \frac{Q}{\ell \pi \kappa} K_0(qr) \tag{3.13}$$

(ΔT(r) is the difference between the temperature at r and the temperature at r=0; Q is the heater power, $\ell$ is the length of the metal line, κ is the thermal conductivity, $K_0$ is the zeroth-order modified Bessel function, and q is given by $q = \left(\frac{i2\omega}{D}\right)^{\frac{1}{2}}$, where D is the thermal diffusivity)

Since the resistance of the metal line varies linearly with the temperature, the resistance also oscillates at the frequency 2ω. The resulting voltage signal on the metal line shows a relation to the third harmonic, 3ω. The thermal conductivity can be determined directly from the out-of-phase voltage (the imaginary part) or indirectly from the in-phase voltage (the real part). [4]

- **2ω technique**

In contrast to the 3ω technique, the 2ω method uses two metal lines to act as heater and thermometer (sensor), separately. The AC current in the heater also has an angular frequency of ω, and the temperature oscillation around the heater source is also dependent on the frequency 2ω; however, the voltage is measured from the thermometer with a DC current to produce a second harmonic signal, hence the name 2ω method.

In this work, the silicon nanomesh thin film was suspended to avoid thermal leakage from the handle substrate. The measured thermal conductivity is considered as one-dimensional $\kappa_X$, compared with the average result of thermal conductivity from $\kappa_X$ and $\kappa_Z$ in the 3ω method (Figure 3.23). Therefore, the 3ω method can be used in bulk materials, while the 2ω method gives more accurate results for thin films. A table is provided below to summarize the similarities and difference for both methods (Table 3.3).
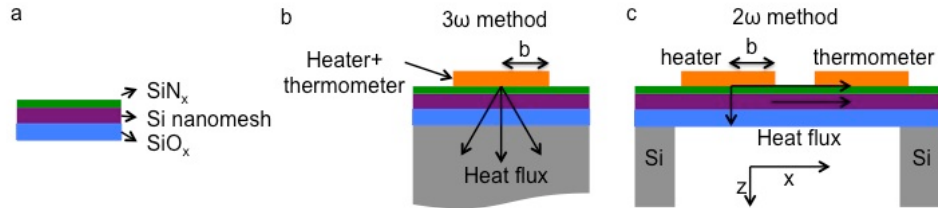


**Figure 3.23 The illustrations of sample structures in the 3ω and the 2ω methods. (a) The stack of layers for thermal conductivity measurement; (b) The sample structure in the 3ω method where the heater also acts as the thermometer, and the thermal conductivity is an averaged result from $\kappa_X$ and $\kappa_Z$; (c) The sample structure in the 2ω method where the heater and the thermometer are separate, and the thermal conductivity is $\kappa_X$ due to the suspension of the film.**

**Table 3.3 Table of comparison between the 3ω and the 2ω methods.**

| | 3ω | 2ω |
|---|---|---|
| Device layout | Single metal line as heater and thermometer | Separate heater and thermometer(s) |
| Measurement | Temperature oscillation on the metal line | Temperature oscillation on the thermometer |
| Current in heater | $I_{AC}(\omega)$ | $I_{AC}(\omega)$ |
| Temperature oscillation from heater source | $\Delta T(2\omega)$ | $\Delta T(2\omega)$ |
| Current in thermometer | $I_{AC}(\omega)$ | $I_{DC}$ |
| Voltage on thermometer | $V(3\omega)$ | $V(2\omega)$ |
| Thermal conductivity | Averaged $\kappa_X$ and $\kappa_Z$ (the bulk sample) | In plane $\kappa_X$ (the suspended film) |
| Interfacial thermal impedance (between sample and metal / thermometer) | Sensitive | Not sensitive |

In order to understand the 2ω method for obtaining the thermal conductivity of the silicon nanomesh thin film, detailed calculations are provided below based on the model from Carslaw and Jaeger. [8] Two scenarios are considered: steady state temperature distribution from the heater, and periodically varying temperature oscillation from the heater. The investigation of the steady state using a semi-infinite rod in Carslaw and Jaeger's model is essential because it sets the foundation for the study of the temperature oscillation at a frequency 2ω in this work.

- **The steady state analysis**

Carslaw and Jaeger [8] investigated a semi-infinite thin rod with the end of the rod (x=0) fixed at a temperature $T_0$. The temperature distribution due to this heat flow inside the rod is specified by the time t and the distance x (Figure 3.24, a). They also assumed that the surface of the rod lost heat through thermal radiation, not thermal convection. This model can also be employed for the silicon nanomesh thin film where the heat source inside the film is the Joule heating of the metal line. Only the heat flow in the direction of the heater to the thermometer is considered in this work, so it also uses the semi-infinite assumption (Figure 3.24, b).
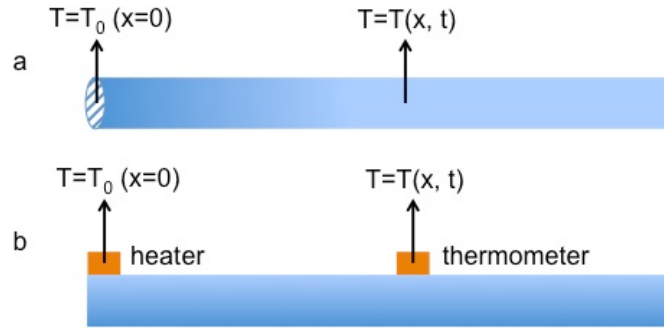


**Figure 3.24 Illustrations of one-dimensional heat flow. (a) The heat flow and boundary conditions in a semi-infinite thin rod; (b) The heat flow and boundary conditions in silicon nanomesh thin film using a metal heater as a heat source.**

*a. The temperature distribution equation*

Suppose that the thin rod is lying in the x direction, and the temperature gradient within the thin rod can be expressed as $\Delta T = -\dfrac{\partial T}{\partial x} \Delta x$, and the negative temperature gradient $\dfrac{\partial T}{\partial x}$ indicates that the heat flows from higher to lower temperature. The rate of

heat flow ($Q/\Delta t$) across the face of the thin rod at a distance x can be expressed by the Fourier's law (Equation 3.14).

$$\frac{Q}{\Delta t} = -\kappa A \frac{\partial T}{\partial x}$$  (3.14)

(Q is the total amount of heat flow across the face at distance x; t is the time; $\kappa$ is the thermal conductivity; and A is the cross-sectional area)

Similarly, the rate of heat flow across the face at a distance x+$\Delta$x can be expressed below (Equation 3.15).

$$\frac{Q'}{\Delta t} = -\kappa A \frac{\partial T}{\partial x} - \kappa A \frac{\partial^2 T}{\partial x^2} dx - ......$$  (3.15)

($Q'$ is the total amount of heat flow across the face at distance x+$\Delta$x)

Without an additional heat source or sink, the element at the interval [x, x+$\Delta$x] gains heat by subtracting the heat flow in Equation 12 from the heat flow in equation 11 (Equation 3.16).

$$\frac{\Delta Q}{\Delta t} = \kappa A \frac{\partial^2 T}{\partial x^2} dx$$  (3.16)

Additionally, the thermal radiation at the suface of the thin rod is also taken into consideration: $hp(T - T_{env})dx$, where h is the heat transfer coefficient, p is the perimeter of the rod, and $T_{env}$ is the environment temperature. Therefore, the rate of total heat gain (q) is obtained by subtracting the thermal loss through surface radiation from the heat gain by heat flowing through the element (Equation 3.17).

$$q = \kappa A \frac{\partial^2 T}{\partial x^2} dx - hp(T - T_{env})dx$$  (3.17)

Meanwhile, an alternative expression for the rate of heat gain (q) in this element can be expressed by using the heat capacity, C (Equation 3.18).

$$q = \frac{Cm\Delta T}{\Delta t}$$ (3.18)

(m is the mass of the element and it can be replaced by m=ρ•A•Δx (ρ is the density); and

ΔT can be expressed by the rate of temperature change, $\Delta T = \frac{\partial T}{\partial t}\Delta t$ )

Therefore, Equation 3.18 can also be expressed as: $C\rho A \frac{\partial T}{\partial t}dx$ . Equations 3.17 and 3.18 yield the temperature differential equation (Equation 3.19).

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} - v(T - T_{env})$$ (3.19)

(α is the thermal diffusivity, $\frac{\kappa}{C\rho}$ ; and v is equal to $\frac{hp}{C\rho A}$ )

If one assumes that the environment temperature is zero ($T_{env}$=0), Equation 3.19 can be simplified (Equation 3.20), and reduced to a one-dimensional heat equation (Equation 3.21) with the substitution of $T = u(x)e^{-vt}$ .

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} - vT$$ (3.20)

$$\frac{\partial u}{\partial t} = \alpha \frac{\partial^2 u}{\partial x^2}$$ (3.21)

The Equation 3.21 can be solved by knowing the boundary conditions at t=0, such as T=$V_0$ ($V_0$=$T_0$-$T_{env}$=$T_0$ when considering $T_{env}$=0) at x=0, and T=$T_{env}$=0 at x>0. Therefore, the solution for t>0 is solved and expressed with an error function (Equation 3.22).

$$T = \frac{1}{2}V_0 e^{-x\sqrt{v/\alpha}}\mathrm{erfc}\left[\frac{x}{2\sqrt{\alpha t}} - \sqrt{vt}\right] + \frac{1}{2}V_0 e^{x\sqrt{v/\alpha}}\mathrm{erfc}\left[\frac{x}{2\sqrt{\alpha t}} + \sqrt{vt}\right] \qquad (3.22)$$

### b. The conservation of heat flux and fitting for thermal conductivity

At the steady state, Equation 3.21 gives the temperature at a distance x as $T = V_0 e^{-x\sqrt{v/\alpha}}$ when $t \to \infty$. The above discussions are also valid for the temperature distribution in the silicon nanomesh thin film as indicated in Figure 3.24. Thus, in the case of a thin film with a deposited metal heater, the heat flux (F, the heat rate per unit area) at the heat source (output heat flux) can be expressed based on the temperature distribution equation (Equation 3.23), $F = -\kappa\left[\frac{\partial T}{\partial x}\right]_{x=0}$, and it also equals to half of the heat flux generated by the resistive metal heater (input heat flux) due to the nature of the semi-infinite configuration (Equation 3.24).

$$F = \kappa V_0 \sqrt{v/\alpha} \qquad (3.23)$$

$$F = \frac{I^2 R}{2\ell d} \qquad (3.24)$$

(I is the root mean square of the AC current; R is the resistance of the metal heater; $\ell$ is the length of the heater; and d is the thickness of the heater)

The conservation of heat flux Equations 3.23 and 3.24 can be solved for the temperature of the metal heater (x=0) in the steady state ($t \to \infty$) when considering $T_{env}$=0: $V_0 = \frac{I^2 R}{2\ell d\kappa\sqrt{v/\alpha}}$. Eventually, the environment temperature is included in the temperature distribution equation T(x) (Equation 3.25), where $T_0$ is the real temperature

114

of the metal heater, and $L_H$ is the healing length, $L_H = \sqrt{\dfrac{\kappa d}{2h}}$. The healing length is a

length scale at which the heat loss in the material is dominated by thermal radiation, and

the temperature of the material is not sensitive to thermal disturbance from the heater so

that it is equal to the environment temperature. The healing length, $L_H = \sqrt{\dfrac{\kappa d}{2h}}$, is a

unique thermal characteristic in the steady state, and it gives the thermal conductivity, $\kappa$.

$$T(x) - T_{env} = (T_0 - T_{env}) e^{-x/L_H}$$

(3.25)

Therefore, the thermal conductivity of the silicon nanomesh thin film or the semi-

infinite thin rod can be measured based on the data fitting of the temperature distribution

Equation 3.25. Overall, the key to solving the one-dimensional heat transfer problem is to

determine the temperature differential equation, such as Equation 3.20 in the steady state

analysis, and then establish the conservation of heat flux between Equations 3.23 and

3.24. In this work, a periodically varying AC current at the frequency $\omega$ is sent to the

heater instead of a DC current, which results in a temperature oscillation at an angular

frequency $2\omega$. The solution to this new condition requires very similar methodology as

used in the steady state analysis.

- **$2\omega$ analysis**

Similarly to the steady state analysis, for the semi-infinite thin rod or the silicon

nanomesh thin film in this study, the rate of heat gain in the $2\omega$ analysis is also equivalent

between Equations 3.17 and 3.18, with the consideration of the thermal radiation from the

sample surface. The environment temperature is also assumed zero ($T_{env}$=0) for the sake

of simplicity. So far, the 2ω analysis obtains the same temperature differential Equation

3.20, $\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} - \nu T$, as in the steady state analysis.

However, in the 2ω analysis, one end of the thin rod or the metal heater on the nanomesh thin film is subjected to a periodic variation in the temperature due to a AC current, which causes the heat waves to travel in the material with the same frequency (2ω). The thermal conductivity is calculated from data fittings to these waves. [8]

### a. The temperature oscillation equation

If the AC current in the metal heater takes the form of $I = I_0 \sin(\omega t)$, the Equation 3.20 can be reduced to the one-dimensional heat equation (Equation 3.26) with the substitution of $T = u(x)e^{i(2n\omega t)}$.

$$\frac{\partial^2 u}{\partial x^2} - \frac{i(2n\omega + \nu)}{\alpha} u = 0 \tag{3.26}$$

(n is an integer; α is the thermal diffusivity, $\frac{\kappa}{C\rho}$; ω is the angular frequency of the AC current in the metal heater; and ν is equal to $\frac{hp}{C\rho A}$)

There are two solutions to Equation 3.26: $u(x) = u_0 e^{\pm(a_n + ib_n)x}$, where $a_n$ and $b_n$ are frequency dependent parameters, but only $u(x) = u_0 e^{-(a_n + ib_n)x}$ satisfies the physical condition that the temperature further away from the heater in the material should remain unaffected by the temperature oscillation at x=0, so that it satisfies T(x=∞)=0 due to the

116

zero environment temperature assumption ($T_{env}$=0). Only this solution is then substituted back into Equation 3.26 to define the parameters $a_n$ and $b_n$ (Equations 3.27-3.30).

$$a_n + ib_n = \sqrt{\frac{\nu + i(2n\omega)}{\alpha}} \qquad (3.27)$$

$$a_n = \sqrt{\frac{\nu + \sqrt{\nu^2 + 4n^2\omega^2}}{2\alpha}} \qquad (3.28)$$

$$b_n = \sqrt{\frac{-\nu + \sqrt{\nu^2 + 4n^2\omega^2}}{2\alpha}}$$

(3.29)

$$a_n b_n = \frac{n\omega}{\alpha} \qquad (3.30)$$

According to Carslaw and Jaeger, [8] a general periodic temperature solution of $u(x) = u_0 e^{-(a_n + ib_n)x}$ oscillates with a period $\pi/\omega$ (Equation 3.31).

$$T = \sum_{n=0}^{\infty} A_n e^{-a_n x} \cos(2n\omega t - b_n x + \varepsilon_n) \qquad (3.31)$$

If only the second harmonic in the temperature oscillation at the heater is considered at x=0, the temperature at the heater should be expressed with the first two terms of Equation 3.31 to satisfy the $2\omega$ analysis: $T(x = 0) = A_0 \cos\varepsilon_0 + A_1 \cos(2\omega t + \varepsilon_1)$. Then the temperature oscillation at a distance x and a time t in the material can also be expressed by the first two terms (Equation 3.32) from Equation 3.31.

$$T = A_0 e^{-a_0 x} \cos\varepsilon_0 + A_1 e^{-a_1 x} \cos(2\omega t - b_1 x + \varepsilon_1) \qquad (3.32)$$

*b. The conservation of heat flux and fitting for thermal conductivity*

Now, similar to the steady state analysis, the heat flux at the heater source ($x=0$) can be expressed below (Equation 3.33) based on Equation 3.32.

$$F = -\kappa \left[ \frac{\partial T}{\partial x} \right]_{x=0} = \kappa A_0^* a_0 + \kappa A_1 a_1 \cos(2\omega t + \varepsilon_1) - \kappa A_1 b_1 \sin(2\omega t + \varepsilon_1)$$

$$= \kappa A_0^* a_0 - \kappa A_1 \left\{ \sqrt{\frac{\sqrt{v^2 + 4\omega^2}}{\alpha}} \cos \left[ 2\omega t + \varepsilon_1 + \frac{\pi}{2} - \arcsin \sqrt{\frac{v}{2\sqrt{v^2 + 4\omega^2}} + \frac{1}{2}} \right] \right\}$$

$$(3.33)$$

($A_0^*$ is the product of $A_0$ and $\cos\varepsilon_0$)

Again according to the conservation of heat flux, the output heat flux based on thermal conduction and radiation is equal to half of the input heat flux generated by the resistive metal heater (Equation 3.34) due to the nature of the semi-infinite configuration.

$$F = \frac{I_0^2 R \sin^2(\omega t)}{2\ell d} = \frac{I_0^2 R}{4\ell d} \left[ 1 - \cos(2\omega t) \right] \tag{3.34}$$

($I_0$ is the amplitude of the AC current; and $I = I_0 \sin(\omega t)$)

This thermal energy conservation results in two equations (Equations 3.35, 3.36) from the constant part and the cosine function part of Equations 3.33 and 3.34.

$$\kappa A_0^* a_0 = \frac{I_0^2 R}{4\ell d} \tag{3.35}$$

$$\kappa A_1 \left\{ \sqrt{\frac{\sqrt{v^2 + 4\omega^2}}{\alpha}} \cos \left[ 2\omega t + \varepsilon_1 + \frac{\pi}{2} - \arcsin \sqrt{\frac{v}{2\sqrt{v^2 + 4\omega^2}} + \frac{1}{2}} \right] \right\} = \frac{I_0^2 R}{4\ell d} \cos(2\omega t)$$

$$(3.36)$$

The above equations can help solve for three unknown parameters, $A_0^*$, $A_1$, and $\varepsilon_1$ (Equations 3.37-3.39). Then the temperature oscillation Equation can be clearly established when these three parameters are substituted into Equation 3.32.

$$A_0^* = A_0 \varepsilon_0 = \frac{I_0^2 R}{4\ell d\kappa\sqrt{\nu/\alpha}} \tag{3.37}$$

$$A_1 = \frac{I_0^2 R}{4\ell d\kappa\sqrt{\dfrac{\sqrt{\nu^2 + 4\omega^2}}{\alpha}}} \tag{3.38}$$

$$\varepsilon_1 = -\frac{\pi}{2} + \arcsin\sqrt{\frac{\nu}{2\sqrt{\nu^2 + 4\omega^2}} + \frac{1}{2}} \tag{3.39}$$

Equation 3.39 can be further simplified in a special case where $\nu \ll 2\omega$ to obtain $\varepsilon_1 = -\pi/4$. In this work, the frequency $\omega$ is 1004.8 Hz ($\omega = 2\pi f$, and f=160 Hz), so that the approximation condition is satisfied. Therefore, the temperature oscillation equation 3.32 can be specifically expressed by a cosine function (Equation 3.40) with amplitude A (Equation 3.41), phase shift $\Delta\phi$ (Equation 3.42), and a constant part. Very similar results are also derived independently by Grigoropoulos. [11]

$$T \cong \frac{I_0^2 R}{4\ell d\kappa\sqrt{\nu/\alpha}}e^{-x\sqrt{\nu/\alpha}} + \frac{I_0^2 R}{4\ell d\kappa\sqrt{2\omega/\alpha}}e^{-x\sqrt{\omega/\alpha}}\cos(2\omega t - x\sqrt{\omega/\alpha} - \frac{\pi}{4})$$

$$\tag{3.40}$$

$$A = \frac{I_0^2 R}{4\ell d\kappa\sqrt{2\omega/\alpha}}e^{-x\sqrt{\omega/\alpha}}$$

$$\tag{3.41}$$

$$\Delta\phi = -x\sqrt{\omega/\alpha} - \frac{\pi}{4} \tag{3.42}$$

If the environment temperature is taken into consideration, Equation 3.40 is essentially the solution to the temperature change measured from the thermometer in the $2\omega$ method as a function of time. This temperature change is related to the voltage in the thermometer through the relation below (Equation 3.43):

$$V = I_{DC}R = I_{DC}\frac{dR}{dT}\Delta T \tag{3.43}$$

(V is the DC voltage measured from the thermometer; $I_{DC}$ is the DC current supplied to the thermometer; dR/dT is the dependence of the resistance of the thermometer on temperature; and $\Delta T$ is determined from Equation 3.40 at a fixed distance from the heater)

One lock-in amplifier was used to measure the amplitude and the phase change in the voltage of the thermometer. The thermal diffusivity α was first obtained by fitting the phase change data to Equation 3.42. Later, the thermal conductivity κ was determined by the fitting on the voltage amplitude data to Equation 3.44 below, using the thermal diffusivity value previously obtained.

$$[A]_V = \frac{I_{DC}I_0^2R[dR/dT]}{4\ell d\kappa\sqrt{2\omega/\alpha}}e^{-x\sqrt{\omega/\alpha}} \tag{3.44}$$

- **The thermal conductivity measurement from the 2ω device**

To implement the 2ω method, a series of electrodes, 2 μm wide, were deposited and annealed on top of the silicon nanomesh (Figure 3.25). The first one was the heater and the rest were thermometers with the spacing of 10 μm, 20 μm, and 40 μm, respectively. An estimation of the healing length gives $L_H$>127 μm for the steady state part of the heat oscillation based on Equation 3.5, so that all the thermometers should undergo a temperature increase compared with the global temperature. The sample was also suspended beneath the heater and thermometers to avoid parasitic heat leakage.

120
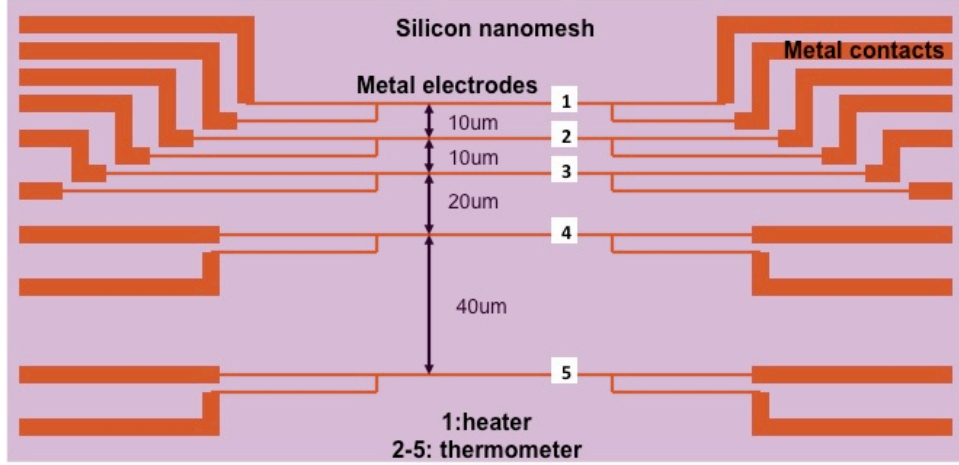
**Figure 3.25 The thermal conductivity device layout for the 2ω measurement. The electrode 1 is the heater, and electrodes 2-5 are thermometers.**

A 29 nm thick $SiN_x$ layer was deposited on top of the sample to ensure that each electrode is isothermal so that the temperature across the cross-section is considered to be uniform. Due to the presence of $SiN_x$ and the buried $SiO_x$ layer from the SOI sample, the thermal conductivity of the silicon nanomesh thin film was obtained by a two-step measurement sequence. First, the measurement was conducted on a stack of layers: silicon nitride, silicon nanomesh, and silicon oxide to obtain a thermal conductivity of the stack, $\kappa_{stack}$. Then, it was repeated on a two-layer structure ($SiN_x$ and the buried $SiO_x$ layers) after etching away the silicon nanomesh thin film to obtain $\kappa_{SiOx+SiNx}$. Finally, the thermal conductivity of the silicon nanomesh, $\kappa_{Si}$, is calculated based on the conservation of thermal conductance (Equation 3.45), similar to Equation 3.6.

$$\kappa_{Si}d_{Si} + \kappa_{SiOx+SiNx}(d_{SiOx} + d_{SiNx}) = \kappa_{stack}d_{stack} \tag{3.45}$$

($d_i$ is the thickness of each layer; i=Si, $SiN_x$, or $SiO_x$; $d_{stack}$ is the thickness of all three layers)

Besides thermal conductivity, this 2ω measurement also yields the heat capacity and thermal diffusivity of the two-layer structure composed of $SiN_x$ and $SiO_x$. The results are presented in chapter 5.

## 3.3 Summary

### 3.3.1 Summary of characterizations and metrology of the $S^2\sigma$ device set

In the section 3.1, we characterized the cylindrical structure of a nanomesh (from top and cross-sectional views) and the actual strain level in strained silicon thin films before and after introducing a nanomesh. The characterization showed the following. The nanomesh was patterned hexagonally with a uniform and long-range order; this nanostructure was etched through a strained silicon thin film. The strain level in strained silicon thin film without a nanomesh was 0.7%, as measured by Raman spectroscopy; the engineering of the nanomesh did not totally relax the tensile strain in silicon thin films.

The measurement setup and metrology for electrical conductivity and thermopower of the $S^2\sigma$ device set were also described. For electrical conductivity, the sheet resistance from a SSOI sample was measured in a modified four-point probe method; the sheet resistance was then converted to thin film resistivity. A correction factor of 1.5 is required to compensate for the addition of a geometrical factor.

For thermopower measurements, a Labview program was used to trigger and record both voltage and temperature drops simultaneously across strained silicon films. Data was collected and analyzed for measurement error. Thermopower was determined based on a linear fit from ΔV-ΔT plots.  The temperature dependence of thermopower

from strained and unstrained silicon thin films, with and without nanomesh, was studied and the results are shown in chapter 4.

## 3.3.2 Summary of characterizations and metrology of *ZT* device set

In the section 3.2, various characterization techniques were used to characterize the ~100 nm thick silicon nanomesh: the nanomesh morphology by SEM, the silicon nanomesh thickness and porosity by ellipsometry, and the silicon nanomesh doping level by SIMS. After the characterizations, three sets of devices were fabricated on the same chip (the *ZT* device set) for the measurements of thermopower, electrical resistivity, and thermal conductivity at around 303 K to determine *ZT*. First, the thermopower measurement used a resistive metal heater to create a one-dimensional heating profile across the silicon nanomesh pad; the voltage and temperature difference across the pad were measured by two resistive thermometers; the linear fit of $\Delta V$-$\Delta T$ resulted in the thermopower, S. Second, the electrical resistivity was determined on a Greek cross structure using the Van der Pauw method; the sheet resistance of the nanomesh was measured and converted to resistivity using an equation also used in the four-point probe method. Last, the thermal conductivity was measured by a novel $2\omega$ method by fitting the voltage signal from the thermometer to the amplitude and phase change in a derived equation; the final thermal conductivity of the silicon nanomesh was obtained by subtracting the thermal conductivity of $SiN_x$ and the buried $SiO_x$ double layers from the thermal conductivity of the stack of layers. The measurement results are shown in chapter 5.

## 3.4 Reference

[1] J.Y. Tang, H.T. Wang, D.H. Lee, M. Fardy, Z.Y. Huo, T.P. Russell, and P.D. Yang, *Nano Letters* **10** 4279-4283 (2010).

[2] T.S. Drake, C. NÍ Chleirigh, M.L. Lee, A.J. Pitera, E.A. Fitzgerald, D.A. Antoniadis, D.H. Anjum, J. Li, R. Hull, N. Klymko, and J.L. Hoyt, *Journal of Electronic Materials* **32** 972-975 (2003).

[3] D.K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, 2006.

[4] D.G. Cahill, *Review of Scientific Instruments* **61** 802-808 (1990).

[5] D.G. Cahill and R. O. Pohl, *Physical Review B* **35** 4067 (1987).

[6] X.J. Hu, A.A. Padilla, J. Xu, T.S. Fisher and K.E. Goodson, *Journal of Heat Transfer* **128** 1109-1113 (2006).

[7] S.M. Lee and D. G. Cahill, *Journal of Applied Physics* **81** 2590-2595 (1997).

[8] H.S. Carslaw and J.C. Jaeger, *Conduction of Heat in Solids* London, Oxford University Press, 1959.

[9] G.K. White, *Thermal Conductivity, Vol. I*, 69 (1969).

[10] R. Berman, Pmc. R. Soc. (London) A **208** 90 (1951)

[11] X. Zhang and C.P. Grigoropoulos, *Review of Scientific Instruments* **66** 1115-1120 (1995).

# Chapter 4

# Strained Silicon Power Factor Results and Discussion

The thermoelectric figure of merit *ZT* determines the efficiency of power generation. *ZT* is expressed as $ZT = \dfrac{S^2\sigma}{\kappa}T$, a function of the power factor ($S^2\sigma$) and thermal conductivity ($\kappa$). Studies showed that *ZT* of silicon was improved by ~40X compared to that of bulk silicon, by reducing the thermal conductivity using nanomesh or holey structure, and keeping the power factor comparable to that of the bulk silicon. In this study, we propose to further enhance *ZT* by increasing the power factor, while retaining low thermal conductivity by using nanostructures such as nanomesh.

Here we present the measurement results of electrical conductivity and thermopower from strained silicon thin films, with nanomesh and without nanomesh, and from unstrained silicon thin films, with nanomesh and without nanomesh. Data was collected from SSOI and SOI bulk samples (or devices) measured in a cryostat with temperature and vacuum controls. For the first time in thermoelectric studies, we also discuss the enhancement in power factor from strained silicon with nanomesh compared with that from unstrained silicon thin films with nanomesh.

## 4.1 Electrical conductivity measurement results

Both SOI and SSOI samples were measured over the temperature range of 230 K-380 K. The resistivity of both samples without nanomesh showed distinctive behaviors. For strained silicon, the resistivity increased slightly as the temperature increased, consistent with metallic behavior. Unstrained silicon, however, behaved like a semiconductor; i.e., the resistivity decreased as the temperature increased (Figure 4.1, a). The strained silicon and unstrained silicon thin films were doped under the same conditions with diffusion doping to achieve the same doping level. Based on Figure 4.1 (a), the strained silicon without nanomesh film showed slight metallic behavior due to the strain effect on the silicon bandstructure; the measured resistivity was equivalent to a phosphorus concentration of $8X10^{18}$ atoms/cm$^3$ in an unstrained silicon film. However, the unstrained silicon without nanomesh film showed an equivalent phosphorus concentration of $4.4X10^{17}$ atoms/cm$^3$ after the same diffusion doping process, as measured by the four-point probe station. For comparison, n-type degenerate or highly doped silicon (doping concentration higher than $1.6 \times 10^{18}$ atoms/cm$^3$) begins to show metallic behavior in electrical conductivity. [1]
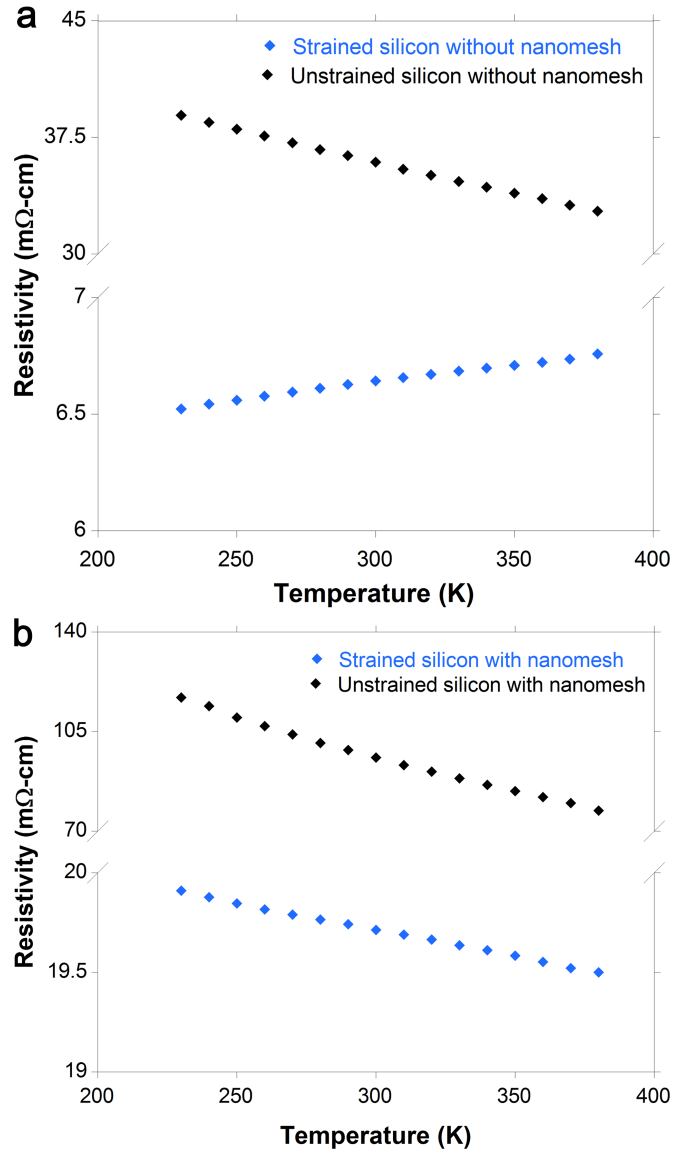
**Figure 4.1 Electrical resistivity from strained silicon and unstrained silicon thin films. (a) Before nanomesh, strained silicon showed metallic behavior while unstrained silicon showed semiconductor behavior; (b) After nanomesh, both strained and unstrained silicon showed semiconductor behavior.**

After a nanomesh had been fabricated on SSOI and SOI samples, however, both samples exhibited semiconductor behavior, since the nanomesh hindered electrical conduction in both samples (Figure 4.1, b). It has been reported that when a silicon thin film was highly doped with a concentration of $5 \times 10^{19}$ atoms/cm$^3$ of boron before

fabricating a nanomesh, its resistivity after fabricating the nanomesh still showed metallic

behavior due to high degeneracy (Figure 4.2).
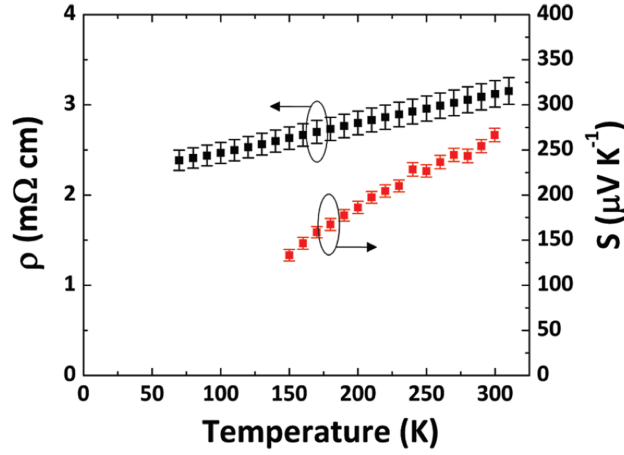


**Figure 4.2 Temperature-dependent electrical resistivity (ρ) and thermopower (S) of boron doped 55 nm pitch holey silicon ribbon.**

It is also shown in Figure 4.1 that, with or without a nanomesh, strained silicon

has a lower electrical resistivity compared with that of unstrained silicon. Electrical

resistivity is reciprocal to electrical conductivity. Experimentally we corroborate that

strain can increase the electrical conductivity of silicon by changing its bandstructure.

Direct measurement data showed that the resistivity of both SSOI and SOI

samples was increased by roughly 200% after a nanomesh had been fabricated. Previous

COMSOL simulation demonstrated that 50% of the increase was due to the geometrical

factor effect on the measurement method (Table 4.1). The rest of the enhancement in

resistivity (50%) was attributed to increased electron scattering resulting from the

nanomesh.

**Table 4.1 Electrical resistivity comparison of strained silicon thin film from SSOI and unstrained silicon thin film from SOI before and after fabrication of a nanomesh.**

| Sample | SSOI | | SOI | |
|---|---|---|---|---|
| Nanomesh | No | Yes | No | Yes |
| Electrical resistivity ($\Omega \cdot$cm) | 0.00664 | 0.01971 | 0.03591 | 0.096 |

After taking into account the correction factor of 1.5 for the four-point probe method, the conductivity at 300 K of strained silicon thin film with a nanomesh was approximately five times that of unstrained silicon thin film with a nanomesh (Figure 4.3). As the temperature was lowered, the ratio of the conductivities increased further. It is shown in this study that strained silicon is a good candidate for thermoelectrics as it can potentially increase the figure of merit *ZT* for higher thermoelectric efficiency compared with unstrained silicon.
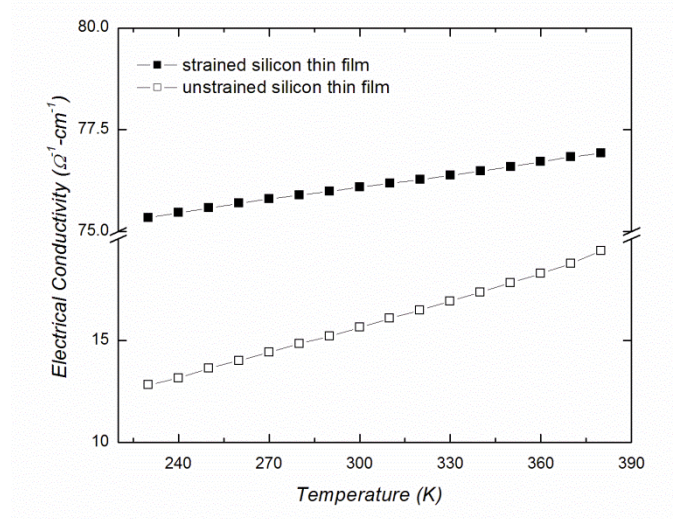


**Figure 4.3 Corrected electrical conductivity of strained and unstrained silicon thin films with nanomesh.**

## 4.2 Thermopower measurement results

Phosphorus doped silicon (n-type) shows negative thermopower. Classically, there are two contributions to thermopower: charge carrier diffusion and phonon-drag. For charge carrier diffusion, the driving force results from a temperature gradient across the silicon structure. A larger temperature gradient results in higher kinetic energy for hot electrons in the high-temperature end to diffuse towards the low-temperature end and creates a larger electrical potential across the silicon structure. The contribution of charge carrier diffusion to thermopower is linearly dependent on temperature.

Phonon-drag occurs when electrons moving through a silicon lattice significantly distort or polarize the silicon lattice. The electron-phonon interaction results in an increased electron effective mass (m*), which leads to a reduced electron mobility (μ). The reduced electron mobility then leads to an increased phonon-drag contribution to the thermopower ($S_{ph}$) (Equations 2.1-2.2). [2-4]

$$\mu \propto \frac{1}{m^*} \quad [2] \tag{2.1}$$

$$S_{ph} \propto \frac{\tau_{ph}}{\mu T} \quad [3\text{-}4] \tag{2.2}$$

($\tau_{ph}$ is the phonon lifetime; T is the temperature)

Phonon-drag has been observed at T<200 K in one-dimensional 20 nm-wide silicon nanowires. [5]

In this study, there was no appreciable phonon-drag phenomenon near 200 K, possibly due to an even further reduced nanostructure size in the nanomesh, in which the phonon mean free path is smaller, and phonon-electron scattering is reduced (Figure 4.4). The dominant phonon scattering mechanism in the nanomeshes in this study is phonon-boundary scattering.

A similar study on a 100 nm thick, 55 nm pitch, boron doped nanomesh silicon thin film also showed higher thermopower at higher temperatures due to charge carrier diffusion, without any appreciable phonon-drag contribution to thermopower (Figure 4.2, thermopower S). [6] It is known that a higher doping level leads to a lower thermopower [7]. This boron doped nanomesh sample had an impurity concentration of $5X10^{19}$ atoms/cm$^3$, but it showed a higher thermopower than the phosphorus doped unstrained nanomesh sample with an impurity concentration of $4.4X10^{17}$ atoms/cm$^3$ in this study. This result can be explained by the difference in nanomesh thickness. In this study, the unstrained silicon thin film was only 10 nm thick, 10% of the thickness of the boron doped nanomesh sample. Electron diffusion is further hindered by extra electron-boundary scatterings since the electron mean free path is on the order of 1-10 nm. [6]

In our study, the thermopower increased by approximately 17% at 300 K after fabricating a nanomesh in an unstrained silicon thin film (Figure 4.4). The same tendency was also observed in strained silicon samples.
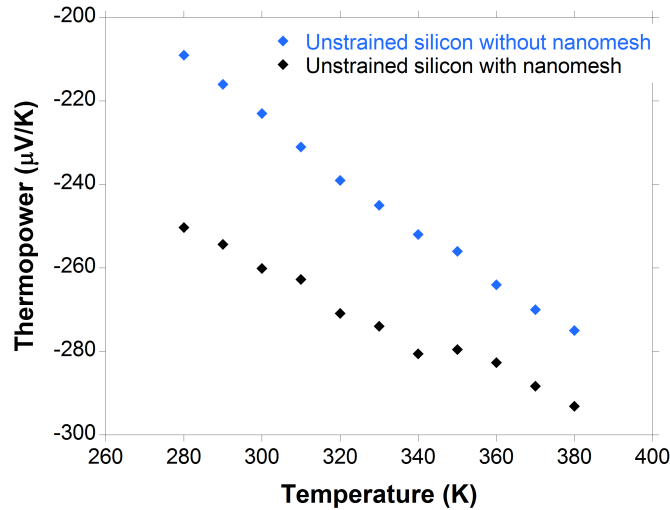


**Figure 4.4 Dependence of thermopower on temperature for unstrained silicon with and without nanomesh.**

131

There was a 36.5% reduction in strained silicon thin film with nanomesh compared with unstrained silicon with nanomesh at 300 K (Figure 4.5). This difference can be explained by the charge carrier diffusion contribution (electronic contribution) to the thermopower ($S_e$), which can be estimated from the Mott's formula (Equations 2.3-2.4). [8-9]

$$S_e = -\frac{\pi^2}{3}\left(\frac{k_B^2 T}{e}\right)\frac{\sigma^*}{\sigma} \tag{2.3}$$

$$\sigma^* = \frac{\partial\sigma(\varepsilon)}{\partial\varepsilon}\bigg|_{\varepsilon=\varepsilon_F} \tag{2.4}$$

($\sigma$ is the electrical conductivity; $k_B$ is the Boltzmann constant, $1.38 \times 10^{-23}$ J/K; T is the temperature; $\varepsilon$ is the energy dispersion; $\varepsilon_F$ is the Fermi energy.)

In strained silicon with nanomesh, both $\sigma^*$ and $\sigma$ increase because the electron effective mass, bandgap, and density of states change due to the strain effect on the silicon bandstructure. It is estimated that $\sigma^*/\sigma$ is reduced in strained silicon; hence its thermopower is lower than that of unstrained silicon with nanomesh.
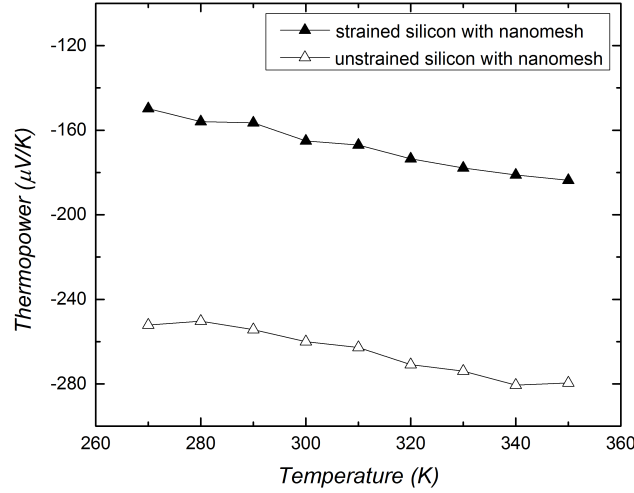
**Figure 4.5 Dependence of thermopower on temperature of strained and unstrained silicon thin films with nanomesh.**

## 4.3 Power factor results

The power factor $S^2\sigma$ is an important parameter to determine the thermoelectric figure of merit $ZT$ of a material; this figure of merit characterizes its thermoelectric efficiency. A change in thermopower (S) has more effect on $ZT$ than does a change in electrical conductivity ($\sigma$). The advantage of using nanomesh in silicon thin films arises primarily from two considerations. First, the thermal conductivity at 300 K in a nanomesh sample is reduced by 34 times compared with a plain thin film without nanomesh and by 85 times compared with bulk silicon (Figure 4.6, a). The thermal conductivity of bulk silicon is 150 W/m•K. Second, the power factor of a nanomesh thin film is not degraded compared with thin film without nanomesh, resulting in a net increase in $ZT$ mainly due to a suppression of thermal conductivity (Figure 4.6, a). A previous holey silicon ribbon study has shown that $ZT$ can be increased by ~ 40 times compared with that of bulk silicon ($ZT_{bulk}$=0.01) at room temperature by using nanomesh structure (Figure 4.6, b). [6]

133
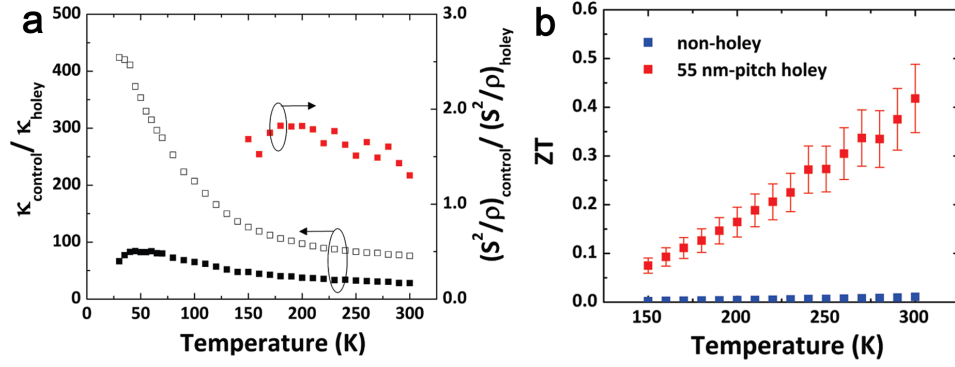
**Figure 4.6 Thermoelectric properties and *ZT* comparisons for 55 nm-pitch nanomesh (holey) and non-nanomesh (non-holey) 100 nm thick silicon ribbons.** (a) Thermal conductivity comparison of nanomesh ribbon (red squares, $5\times10^{19}$ atoms/cm$^3$, boron doped) with non-nanomesh ribbon (black squares, $5\times10^{19}$ atom/cm$^3$, boron doped) and bulk silicon (open squares, $1.7\times10^{19}$ atoms/cm$^3$ As-doped); power factor comparison of nanomesh ribbon and non-nanomesh ribbon; (b) *ZT* comparison of nanomesh ribbon (red squares) and non-nanomesh ribbon (blue squares). *ZT* is increased by ~40 times with nanomesh at room temperature. [6]

Based on the previous investigation, *ZT* in silicon nanomesh was increased due to a reduction in thermal conductivity; and the power factor in silicon nanomesh was equivalent to that in plain silicon thin films. In this study, we compared the power factor from strained silicon with nanomesh and unstrained silicon with nanomesh and showed a 100% increase in power factor from that of strained silicon at 300 K (Figure 4.7). Also, the thickness of the silicon thin films in this study ranged from 5-10 nm. Their thermal conductivity was estimated to be ~ 1.9 W/m•K, based on similar silicon nanomesh (Figure 1.10). [10] The *ZT* is estimated to increase by a factor of 18 in strained silicon with nanomesh thin film compared with a plain unstrained silicon thin film.
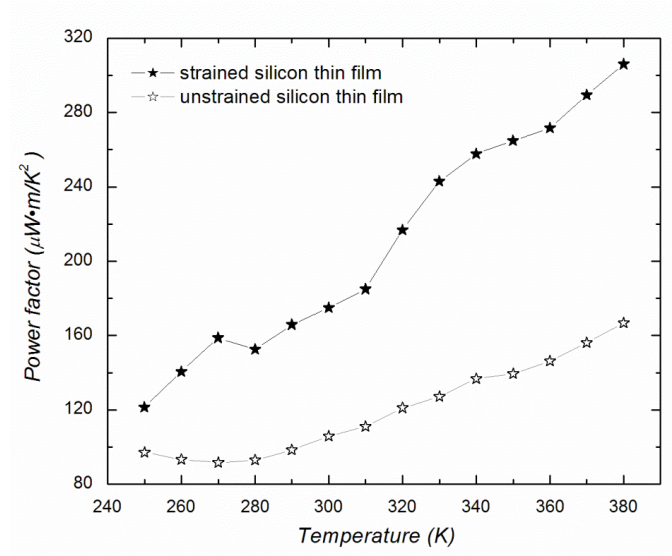
**Figure 4.7 Power factor of strained and unstrained silicon thin film with nanomesh.**

Strained silicon has shown great potential in getting better thermoelectric efficiency. Such advantage is more beneficial at higher temperature. This study showed this tendency over the 250 K-380 K temperature range based on power factor. This is also the first time that strained silicon has been investigated for its thermoelectric applications.

Samples in this study have a carrier concentration of $4.4 \times 10^{17}$ atom/cm$^3$. The best *ZT* or thermoelectric efficiency in strained silicon can be achieved by increasing the carrier concentration to be between $10^{19}$ - $10^{21}$ atoms/cm$^3$. The power factor ($S^2\sigma$) reaches a maximum at a higher carrier concentration than *ZT* (Figure 4.8). Therefore, strained silicon can be an excellent thermoelectric material if an even higher doping level can be achieved.
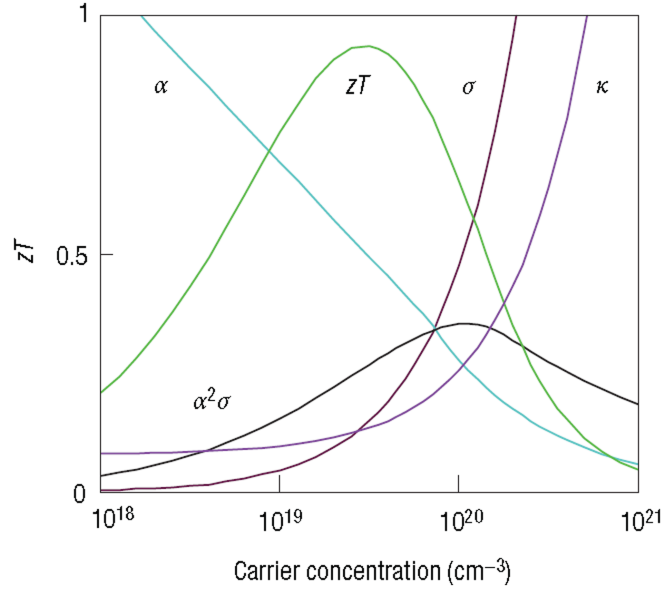
**Figure 4.8 Maximizing the efficiency (*ZT*) of a thermoelectric involves a compromise of thermal conductivity (κ; plotted on the y axis from 0 to 10 W/m•K) and Seebeck coefficient (α; 0 to 500 µV/K) with electrical conductivity (σ; 0 to 5000 $\Omega^{-1}cm^{-1}$). [7]**

## 4.4 Summary

In this chapter, we have presented measurement results of electrical conductivity and thermopower from both strained and unstrained silicon thin films, with and without nanomesh. At low carrier concentration, only strained silicon without nanomesh showed metallic behavior in electrical resistivity. Also, the resistivity in both strained silicon and unstrained silicon thin films increased by 3X after nanomesh was transferred by RIE. Overall, the electrical conductivity of strained silicon with nanomesh compared to the electrical conductivity of unstrained silicon with nanomesh was increased by a factor of five. Strained silicon with nanomesh showed a lower thermopower than unstrained silicon with nanomesh due to changes of parameters such as electron effective mass and density of states arising from changes in the silicon bandstructure. As a result of the combined effects of electrical conductivity and thermopower, the power factor of strained

silicon with nanomesh was 100% higher than that of unstrained silicon with nanomesh. This is the first time that thermoelectric properties of tensile-strained silicon have been reported. Based on the results from this chapter, the *ZT* in strained silicon thin film with nanomesh structures is 18 times as that of a plain unstrained silicon thin film. This result can be further improved by increasing the carrier concentration to be between $10^{19}$ - $10^{21}$ atoms/cm$^3$ in the future.

## 4.5 References

[1] R.F. Pierret, *Semiconductor Device Fundamentals*, Addison Wesley, 1996.

[2] F. Schäffler**, *Semiconductor Science and Technology* **12** 1515–1549 (1997).

[3] C. Herring, *Physical Review* **96** 1163–1187 (1954).

[4] L. Gurevich, *Zhurnal Eksperimentalnoi I Teoreticheskoi Fiziki* **16** 193–228 (1946).

[5] A.I. Boukai, Y. Bunimovich, J.T. Kheli, J.K. Yu, W.A. Goddard III & J.R. Heath, *Nature* **451** 168-171 (2008).

[6] J.Y, Tang, H.T. Wang, D.H. Lee, M. Fardy, Z.Y. Huo, T.P. Russell, and P.D. Yang, *Nano Letters* **10** 4279-4283 (2010).

[7] G.J. Snyder and E.S. Toberer, *Nature Materials* **7** 105-114 (2008).

[8] M. Jonson and G.D. Mahan, *Physical Review B*   21 4223-4229 (1980).

[9] N.W. Ashcroft and N.D. Mermin, Solid State Physics, *Cengage Learning 1st edition* 255-256 (1976).

[10] J.K. Yu, S. Mitrovic, D. Tham, J. Varghese and J.R. Heath, *Nature Nanotechnology* **5** 718 -721 (2010).

# Chapter 5

# *ZT* Measurement Results and Discussion

Here we present the measurement results around room temperature of thermopower, electrical resistivity, and thermal conductivity from the *ZT* device set. Detailed discussions are provided on the high electrical resistivity in the silicon nanomesh thin film after DRIE and the thermal conductivity of silicon nanomesh based on the two-step measurement. Finally, the *ZT* is obtained on this sample, and a prediction on the thermoelectric cooling effect is given based on the *ZT* result.

## 5.1 Thermopower measurement result

The metrology of this measurement was provided in chapter 3 with a list of measurement results of ΔV and ΔT from the two thermometers in Table 3.2. The linear fit of ΔV1-ΔT plot gave the first thermopower, 431.53 µV/K, with the goodness of fit $R^2$=0.996 at 303 K (Figure 5.1).
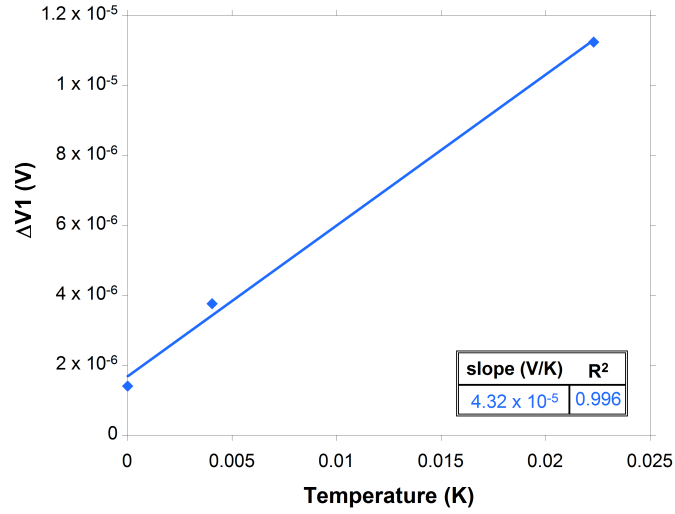
**Figure 5.1 The linear fit on ΔV1-ΔT plot with the goodness of fit of 0.996 for the first thermopower result.**

Three other linear fits were conducted on the remaining ΔV values (ΔV2-ΔV4) measured from the two thermometers based on the choice of electrode combination vs. ΔT, and all the thermopower results are listed below (Table 5.1). The average thermopower is 435.99 µV/K with an error of 4.47 µV/K, calculated from the standard deviation of the four fittings.

**Table 5.1 The thermopower fitting results from four plots of ΔV-ΔT with the average thermopower and its error at 303 K.**

|  | ΔV1-ΔT | ΔV2-ΔT | ΔV3-ΔT | ΔV4-ΔT |
|---|---|---|---|---|
| S (µV/K) | 431.53 | 442.89 | 436.96 | 432.59 |
| $\bar{S}$ [a] (µV/K) | 435.99 | | | |
| ΔS[b] (µV/K) | 4.47 | | | |

[a] : theaverage of thermopower measurements
[b] : the standard deviation calculated from four slope-fittings of ΔV-ΔT

In this study, the thermopower is measured from a 91.2 nm thick silicon thin film with a nanomesh of 80 nm pitch, 27 nm wide neck (the shortest distance between the two edges of holes), and ~41.5% porosity (the ratio of area of holes to the entire surface area).

Similarly, P.D. Yang [1] measured a thermopower of ~250 μV/K from a 100 nm thick holey silicon ribbon with 55 nm pitch, ~20 nm wide neck, and ~35% porosity. The boron concentrations in these two studies are ~2X10$^{19}$ atoms/cm$^3$ and 5X10$^{19}$ atoms/cm$^3$, respectively. Therefore, the difference in the thermopower could be due to the difference in the density of states resulted from the doping and nanomesh related parameters according to Equation 2.3 in chapter 4.

Next, the electrical resistivity result is obtained by the Van der Pauw method using a Greek cross structure. Upon obtaining an unexpectedly high resistivity value from the nanomesh sample, two thermal treatments were conducted to investigate possible methods to repair damage causing the poor electrical properties, likely due to Schottky barrier and carrier depletion by surface states.

## 5.2 Electrical resistivity measurement result and discussion

Similar to the four-point probe method, the Van der Pauw method also relates resistivity ($\rho$) to sheet resistance by the same relation: $\rho = \rho_s \bullet t$, where the sheet resistance is determined from: $\rho_s=4.53R_{12, 34}$, and t is the thickness. When the temperature on the chip was controlled at 303 K, the sheet resistance was measured as 2541 $\Omega/m^2$. Based on previous ellipsometry measurement (section 3.2.1.2), the silicon nanomesh thin film thickness was 91.2 nm. The electrical resistivity was then calculated to be 23.2 mΩ•cm.

The previous monitor sample measured by SIMS (section 3.2.1.3) showed a boron doping level at ~2X10$^{19}$ atoms/cm$^3$, which was equivalent to an electrical resistivity of 5.11 mΩ•cm from a ~100 nm thick silicon thin film without nanomesh. The resistivity

with a nanomesh appeared to be increased by ~350%. This result was contradictory to

that reported in a previously cited holey silicon study (Table 5.2). [1]

**Table 5.2 A comparison between the holey silicon study and this study regarding nanohole (nanomesh) pitch, silicon film thickness (t), and electrical resistivity before and after making nanoholes; measurements were taken around room temperature.**

|  | Pitch (nm) | t (nm) | Porosity | $\rho_{before}$ (m$\Omega$•cm) | $\rho_{after}$ (m$\Omega$•cm) |
|---|---|---|---|---|---|
| Holey silicon study | 55 | 100 | ~35% | 2.34 | ~3 |
| This study | 80 | 91.2 | ~41.5% | 5.11 | 23.2 |

This table has shown that the resistivity in the holey silicon study was increased

by only 28.2%, while the nanomesh sample in this work became highly resistive. It is

very likely that either the measured sample forms an Schottky contact at the metal-

semiconductor junction under the current doping condition, or the surface states

(electronic states on the surface) on the silicon nanomesh shield the semiconductor from

the metal. The holey silicon study [1] also proposed that the increase in electrical

resistivity with the holey structure was possibly due to the carrier depletion by surface

states, which was preliminarily verified by the enhanced electrical conductivity when a

surface passivation layer of $Al_2O_3$ was deposited on the holey silicon sample by atomic

layer deposition (ALD). To justify the hypotheses about the Schottky contact and surface

states in this work, a discussion of two types of metal-semiconductor junctions is

provided below.

## 5.2.1 Metal-semiconductor junction

In solid-state physics, a metal-semiconductor junction is formed when a metal and

a semiconductor, such as p type silicon, are brought into contact (Figure 5.2, a). Electrons

flow from the metal to the silicon until their chemical potentials, or Fermi levels $E_F$, reach equilibrium (Figure 5.2, b).
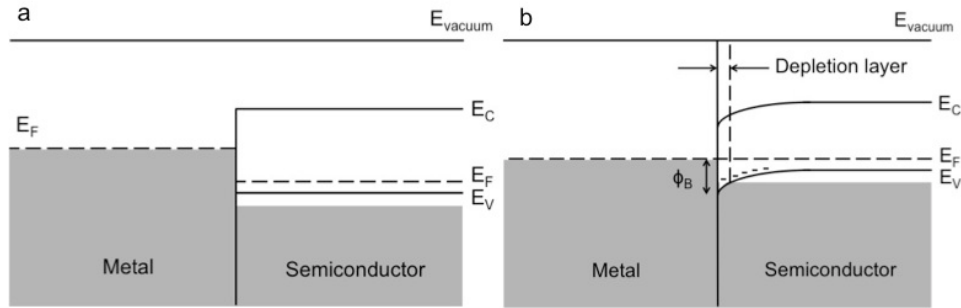


**Figure 5.2 Illustrations of the band diagrams of a metal and a p type semiconductor in contact. (a) Before Fermi levels have been equallized on both sides; (b) After Fermi levels have been equalized on both sides.**

This equilibrium results in a curvature of the valence bands upwards (band bending), a depleted region of holes (depletion layer), and a potential barrier where an excess energy is required for holes to overcome before recombining with electrons from the metal, i.e. the Schottky barrier. The Schottky barrier height ($\phi_B$) is almost completely insensitive to the work function of the metal (based on the Fermi level pinning phenomenon), where $\phi_B$ is almost half of the semiconductor's bandgap $E_g$ (Equation 5.1).

$$\phi_B \approx \frac{1}{2} E_g \qquad (5.1)$$

## 5.2.2 High resistivity due to Schottky contact

The difference between a Schottky contact and an ohmic contact lies in $\phi_B$. An ohmic contact has a linear current - voltage (I-V) curve following Ohm's law. It allows current to flow easily in both directions between the metal and semiconductor without rectification. It is easier to form an ohmic contact if the semiconductor is heavily doped at

142

the surface so that the charge carriers can be transported through the Schottky barrier by tunneling (Figure 5.3).
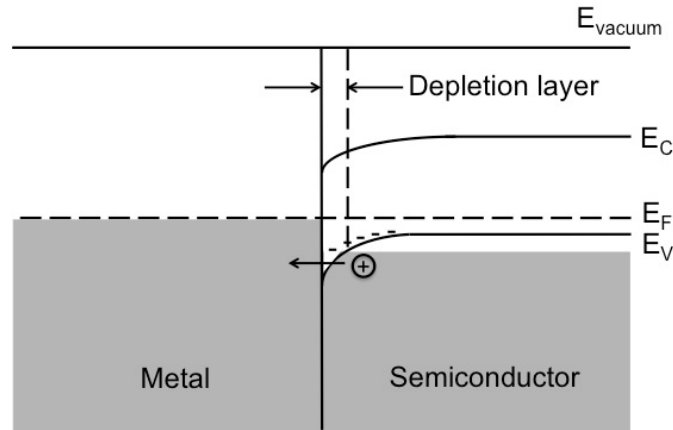


**Figure 5.3 Holes from the semiconductor transport through the Schottky barrier by tunneling if the metal-semiconductor junction is an ohmic contact.**

The nanomesh measured in this work was doped by ion implantation. A uniform dopant distribution within the ~100 nm thick silicon thin film was characterized by SIMS. The lack of excess dopants at the silicon nanomesh surface could be one of the reasons for the high resistivity. Therefore, the diffusional doping method by gas or solid diffusion wafer is recommended for future work.

## 5.2.3 High resistivity due to surface states

Besides the space charge due to the holes depletion at the metal-semiconductor junction, resulting in a region of high resistivity, [1] there can be localized states on the surface of the semiconductor with energies lying within the bandgap. The surface states can either rise in the sharp transition from the material to vacuum or the extension of metal electron states into the semiconductor bandgap due to the match of Fermi levels, and they lead to a change in the electron potential and bandstructure solely at the very

143

surface of the crystal. [2] If there is relatively high density of surface states in the case of a nanomesh with a high surface to volume ratio, a large amount of electrons can be absorbed from the metal at the moment of contact. These surface states are pinned to the Fermi level almost regardless of the metal used. [1, 3] Due to this Fermi level pinning effect, the potential barrier at the metal-semiconductor junction can be difficult to overcome in a silicon nanomesh. However, it is possible to add an intermediate insulator layer to unpin the bands.

An investigation was conducted on various samples to seek solutions to improve the resistivity after DRIE. It also shed light on ways to repair the damage, which likely resulted from the Schottky barrier and surface states, using thermal annealing and oxidation for future study.

## 5.2.4 Thermal treatments to repair damaged silicon nanomesh

It was observed that samples became very resistive after using DRIE to transfer a nanomesh pattern into silicon thin films. It appears that the etching process has damaged the thin film in a way that the hole mobility is reduced, possibly due to the lack of excess dopants at the Schottky barrier or possibly due to the presence of surface states, while the dopant concentration in the nanomesh film should remain the same as it is before DRIE, since DRIE is a physical etching process. Two approaches are attempted to improve the resistivity: rapid thermal annealing (RTA) in inert gas and rapid thermal oxidation (RTO) in oxygen.

## 5.2.4.1 RTA approach to improve resistivity

It has been observed that nanomesh samples after RTA have much lower resistivity. First, Test A was conducted to verify the correlation between electrical resistivity and nanomesh porosity from nanomesh samples etched with a 40 nm-diameter and 80 nm-pitch copolymer mask (Table 5.3). The porosity varies with etching parameters, such as flow rate, etch time per cycle, and number of cycles. The higher porosity indicates less remaining dopants in nanomesh samples and is expected to result in higher resistivity. Although the sourcemeter used in the four-point resistance measurements of all three samples directly after DRIE showed "overflow" (i.e. resistance of samples was unmeasureable, or beyond measurement range ~2 GΩ), the lowest porosity sample (SOI A-2) was improved the most in resistivity after a RTA treatment at 1050 °C in nitrogen gas for 2 min. Test A concludes that lower porosity (or more directional etching to reduce the size of nanomesh) and thermal annealing in nitrogen gas after DRIE are favorable for lower resistivity in silicon nanomesh. Next, Test B was designed to uncover a better treatment to further repair the damage resulting in degradation of the electrical properties of nanomesh by reducing the contamination on the sample surface before RTA.

**Table 5.3 Test A for resistivity comparison from ~100 nm thick pre-boron doped silicon nanomesh samples with various porosities and a RTA treatment.**

| Sample | t (nm) [a] | $\rho$ before DRIE (mΩ•cm) | $\rho$ after DRIE (mΩ•cm) | Porosity [b] | $\rho$ after DRIE +RTA (mΩ•cm) |
|--------|------------|---------------------------|--------------------------|--------------|-------------------------------|
| SOI A-1 | 100 | 14.7 | -- [c] | 45.8% | 310 |
| SOI A-2 | 100 | 14.7 | -- | 39.4% | 97.41 |
| SOI A-3 | 100 | 14.7 | -- | 54.7% | -- |

[a]: the silicon nanomesh thin film thickness.

[b]: measured from ellipsometry.

[c]: stands for "unmeasureable".

Test B was conducted on three ~145 nm thick silicon nanomesh samples etched with a 40 nm-diameter and 80 nm-pitch copolymer mask, with additional cleaning and capping procedures before RTA (1050 °C, $N_2$, 2 min) to significantly reduce contamination from the thermal annealing chamber (Table 5.4). A modified RCA pre-oxidation cleaning and silicon oxide deposition were selectively performed on the samples during this test. The modified RCA cleaning consisted of sequentially cleaning the samples in three different solutions. In the first step, the piranha cleaning [$H_2SO_4$: $H_2O_2$ (3:1 v/v) at 90 °C for 10 min] is used to remove organic contaminants on the surface. The standard SC-1 cleaning normally used in RCA cleaning is replaced by piranha cleaning here to avoid uncontrollable silicon etching. The second step is standard SC-2 cleaning [$H_2O$: HCl: $H_2O_2$ (6:1:1 v/v) at 80 °C for 10 min] to remove ionic contamination and protect the surface with a thin passivation layer to avoid subsequent contamination. The third step [HF: $H_2O$ (1:50 v/v) for 15 s) removes the oxide from previous cleanings. The third step is performed on some samples ("with HF" condition in Table 5.4) to compare with those that skip this step ("No HF" condition in Table 5.4) to verify if the HF step is crucial for surface cleaning during RTA.

After the modified RCA cleaning, a 77 nm thick silicon oxide layer was deposited on the samples by PECVD using a capacitive coupled plasma (CCP) configuration at 350 °C (PlasmaTherm Shuttlelock SLR-730-PECVD, Plasma-Therm, LLC.), and it is named CCP oxide for brevity. This oxide layer provides higher quality surface passivation to protect the sample from contamination in the annealing furnace, and it can be removed after RTA by dipping samples into HF: $H_2O$ (1:50 v/v, 7.5 min). If no CCP oxide is

deposited before RTA, the sample is dipped into HF: H$_2$O (1:50 v/v, 30 s) after the rapid

thermal annealing.

**Table 5.4 Test B for resistivity comparison from ~145 nm thick pre-boron doped silicon nanomesh samples with different oxide passivation procedures and a RTA treatment.**

| Sample | t (nm)$^*$ | $\rho_{before\ DRIE}$ (mΩ•cm) | $\rho_{after\ DRIE}$ (mΩ•cm) | RCA before CCP | $\rho_{after}$ CCP+RTA+50:1HF (mΩ•cm) | $\rho_{before\ RTA}$ / $\rho_{after\ RTA}$ |
|---|---|---|---|---|---|---|
| SOI B-1 | 145 | 6.8 | 328 | No RCA No CCP | 22.6 | 14.5 |
| SOI B-2 | 145 | 6.8 | 328 | No HF | 21.8 | 15.0 |
| SOI B-3 | 145 | 6.8 | 328 | with HF | 24.6 | 13.3 |

$^*$: the silicon nanomesh thin film thickness.

The three samples in Test B were etched with an improved DRIE process to yield

a smaller porosity of 30.4% with 58 nm thick silicon remaining after the etching. The

"bulk" layer of silicon under nanomesh contributed to a lower resistivity. From the

comparison in Table 5.4, the sample (SOI B-2) cleaned by RCA without removing the

resultant oxide and also deposited with CCP oxide is shown to yield the best result in

electrical resistivity as it was improved by 15 times after RTP. This conclusion was

verified by repeating the different cleaning procedures on two more samples for each

procedure. It appears that the oxide passivation can help avoid certain contamination, but

the major contribution for lowering resistivity comes from RTP treatment.

Therefore, the rapid thermal annealing procedure is crucial in improving the

electrical resistivity of the silicon nanomesh by relieving damage resulting from DRIE. It

is also possible that the dopants segregated near the surface after RTA treatment and the

local charge carrier concentration is possibly increased. A dopant distribution similar to

that of diffusion doping may be achieved here. The excess dopants at the surface could

have compensated for the Schottky barrier at the metal-semiconductor junction and some holes may be able to tunnel through the barrier. There is a necessity for a precise spectroscopy analysis, such as advanced SIMS with consideration of thin film porosity, to verify the possibility of dopant segregation.

## 5.2.4.2 RTO approach to improve resistivity

A thin layer of silicon at the nanomesh surface was oxidized in an attempt to tune and pin the silicon valence band. Test C was conducted on nanomesh samples etched with a 30 nm - diameter and 60 nm - pitch copolymer mask (Table 5.5). The RTO process grows a higher quality surface passivation layer than native or deposited oxides, and it includes three steps: a rapid thermal oxidation ($O_2$, 1000 °C, 45 s), a post-oxidation annealing (Ar, 1000 °C, 2 min), and a forming gas annealing (95% $N_2$, 5% $H_2$, 350 °C, 8 min). This process grows an ~5 nm thick silicon oxide layer, as verified by ellipsometry.

**Table 5.5 Test C for resistivity comparison from ~100 nm thick pre-boron doped silicon nanomesh samples before and after RTO process.**

| Sample | t (nm) [a] | $\rho_{before\ DRIE}$ (mΩ•cm) | $\rho_{after\ DRIE}$ (mΩ•cm) | $\rho_{after\ DRIE\ +RTO}$ (mΩ•cm) |
|--------|-----------|-------------------------------|------------------------------|-----------------------------------|
| SOI C-1 | 100 | 6.0 | -- [b] | 88.8 |
| SOI C-2 | 100 | 6.0 | 171.9 | 85.0 |

[a]: the silicon nanomesh thin film thickness.

[b]: stands for "unmeasureable".

The surface passivation by RTO is proven effective in improving the silicon nanomesh resistivity at least by a factor of two based on Table 5.5. It is very likely that the thermal oxide layer partially reduces the surface state density. It is possible that a

thicker oxide layer may result in a better passivation, while it is not desirable to lose more silicon nanomesh thickness to oxidation.

## 5.2.5 Summary of electrical resistivity result and discussion

Overall, the silicon nanomesh sample showed high resistivity, 23.2 m$\Omega$•cm, at 303 K possibly due to two reasons: Schottky barrier and surface states. Test samples were treated with RTA and RTO in attempts to repair the damage caused by DRIE. This etching process not only reduced the total amount of dopants in the silicon thin film, but also created a larger surface to volume structure, nanomesh, that increased the surface state density. After RTA treatment with optional surface cleaning and oxide capping processes, the resistivity was greatly improved by more than 10 times. It also appears that the rapid thermal annealing is more crucial to the damage repair compared with surface cleaning and passivation. On the other hand, RTO treatment was also found effective in possibly reducing the surface state density to unpin the valence band. Further studies are required on both approaches to gain confidence in the mechanisms behind these thermal treatments.

Next, the thermal conductivity measurement result on the silicon nanomesh thin film is presented. The 2$\omega$ method also yields the heat capacity and thermal diffusivity of the SiN$_x$ and SiO$_x$ double layers.

## 5.3 Thermal conductivity measurement result

In order to obtain the thermal conductivity of the silicon nanomesh thin film, a two-step measurement sequence was conducted. The first measurement was conducted

on a stack of $SiN_x$, Si nanomesh, and $SiO_x$ layers; the second measurement was conducted on the $SiN_x$, $SiO_x$ double layers. Details of each step are provided below.

## 5.3.1 Measurement results of the stack layers

According to the thermal conductivity metrology in chapter 3, the amplitude and phase change of the voltage of the thermometer were measured by a lock-in amplifier. First, the phase change data was fitted to Equation 3.42 in chapter 3, $\Delta\phi = -x\sqrt{\omega/\alpha} - \dfrac{\pi}{4}$. The first thermometer on the device layout in Figure 3.25 was used here, so x=10 μm. Also, the angular frequency $\omega$ was 1004.8 Hz ($\omega=2\pi f$, and f=160 Hz). Therefore, the thermal diffusivity of the stack layers, $\alpha$, was obtained over the temperature range of 310-350 K (Figure 5.4). Since the thermal diffusivity of silicon ($8.8 \times 10^{-5}$ $m^2$/s) [4] is 1-2 orders of magnitude larger than the thermal diffusivities of $SiN_x$ ($9.1 \times 10^{-6}$ $m^2$/s) [5] and $SiO_x$ ($8.3 \times 10^{-7}$ $m^2$/s) [4] at room temperature, the thermal diffusivity measurement result of the stack layers reflects the temperature dependence of thermal diffusivity in silicon. Figure 5.4 showed a reduced thermal diffusivity when temperature increased, which matched the measurement results of silicon by Shanks, et al (Figure 5.5). [6]

**Figure 5.4 The thermal diffusivity of the stack layers measured by the 2ω method over the temperature range of 310-350 K.**
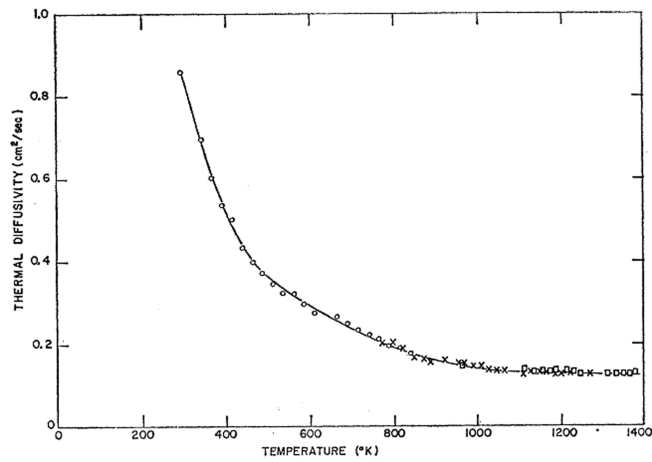


**Figure 5.5 Thermal diffusivity of silicon from 300 to 1400 K.** [6]

The thermal conductivity of the stack layers can be obtained by fitting the voltage

amplitude measurements to Equation 3.44 in chapter 3, $[A]_V = \dfrac{I_{DC}I_0^2R[dR/dT]}{4\ell d\kappa\sqrt{2\omega/\alpha}}e^{-x\sqrt{\omega/\alpha}}$ ,

and by substituting the previously determined thermal diffusivity into this equation

(Figure 5-6). The thermal conductivity of the stack layers showed a slight linear reduction

when temperature increased. A clearer temperature dependence of thermal conductivity

of silicon nanomesh alone in section 5.3.3 is provided and analyzed later since the dominance of silicon nanomesh in this set of data is not clear.
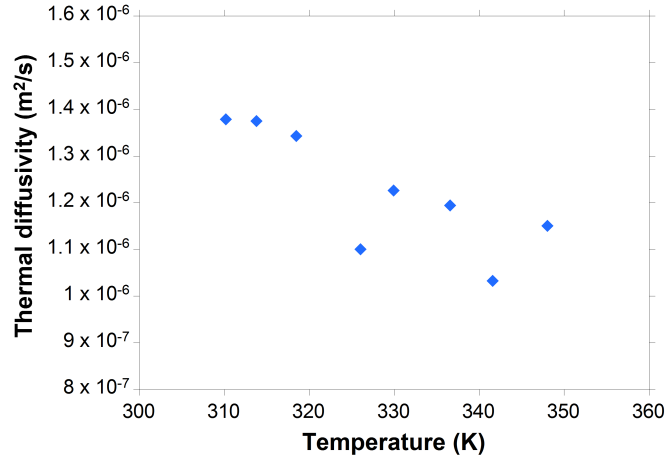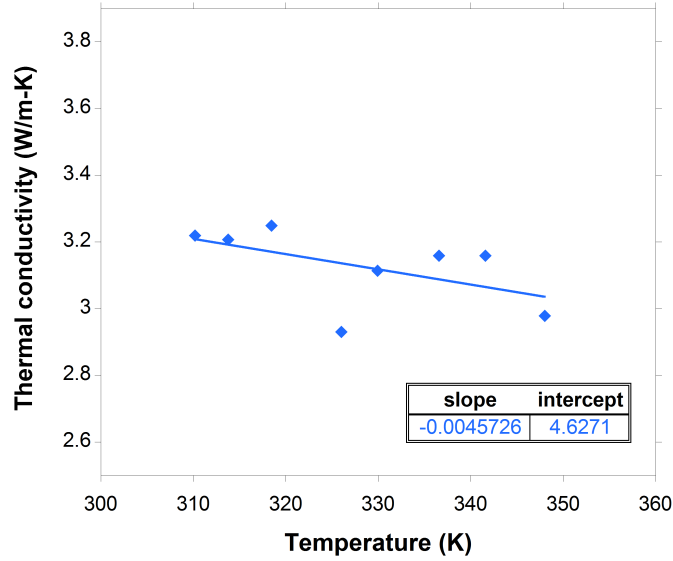


**Figure 5.6 The thermal conductivity of the stack layers measured by the 2ω method over the temperature range of 310-350 K.**

Additionally, the volume-specific heat capacity of the stack layers is the product of the density and the specific heat, ρ•C, and it can be calculated from the thermal diffusivity and thermal conductivity of the material: ρ•C=α•κ (Figure 5.7). According to Figure 1.4, the heat capacity of silicon follows the Debye approximation at low temperature $(T<0.1\theta_D)$, $C_v \approx 233 Nk_B (T/\theta_D)^3$; it approaches the Dulong-Petit limit, $C_v = 3Nk_B/V$, at high temperature $(T >> \theta_D)$; and it increases when temperature increases between the two temperature regimes. The measured heat capacity from the stack layers in Figure 5.7 showed this temperature dependence. It is very likely that the thicker silicon nanomesh layer dominates the heat capacity in the stack layers even though $SiN_x$, Si, and $SiO_x$ have very similar heat capacity of ~700 J/Kg•K at 300 K.
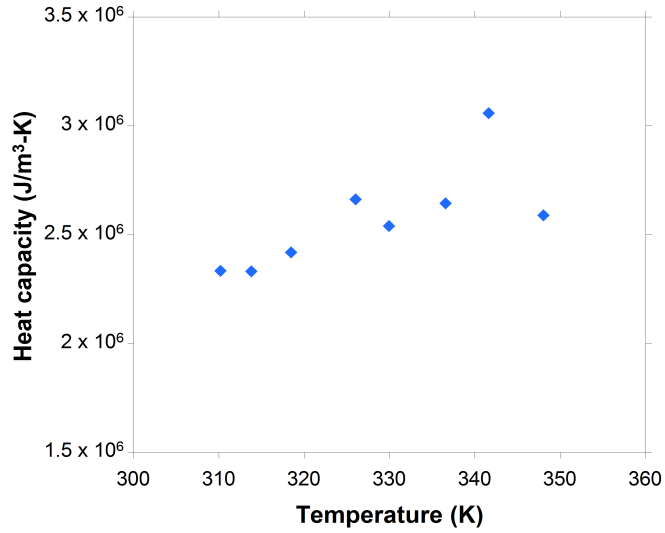
**Figure 5.7 The volume-specific heat capacity of the stack layers measured by the 2ω method over the temperature range of 310-350 K.**

## 5.3.2 Measurement results of the double layers

The same 2ω measurement was conducted on the $SiN_x$ and $SiO_x$ double layers after etching the silicon nanomesh layer away by RIE. The corresponding thermal diffusivity (Figure 5.8, a), thermal conductivity (Figure 5.8, b), and volume specific heat capacity (Figure 5.8, c) of the double layers were obtained based on the new voltage measurements from the thermometer over the temperature range of 310-350 K. The thermal conductivity for the silicon nanomesh thin film was then determined based on the conductivities measured from the stack layers and the double layers.
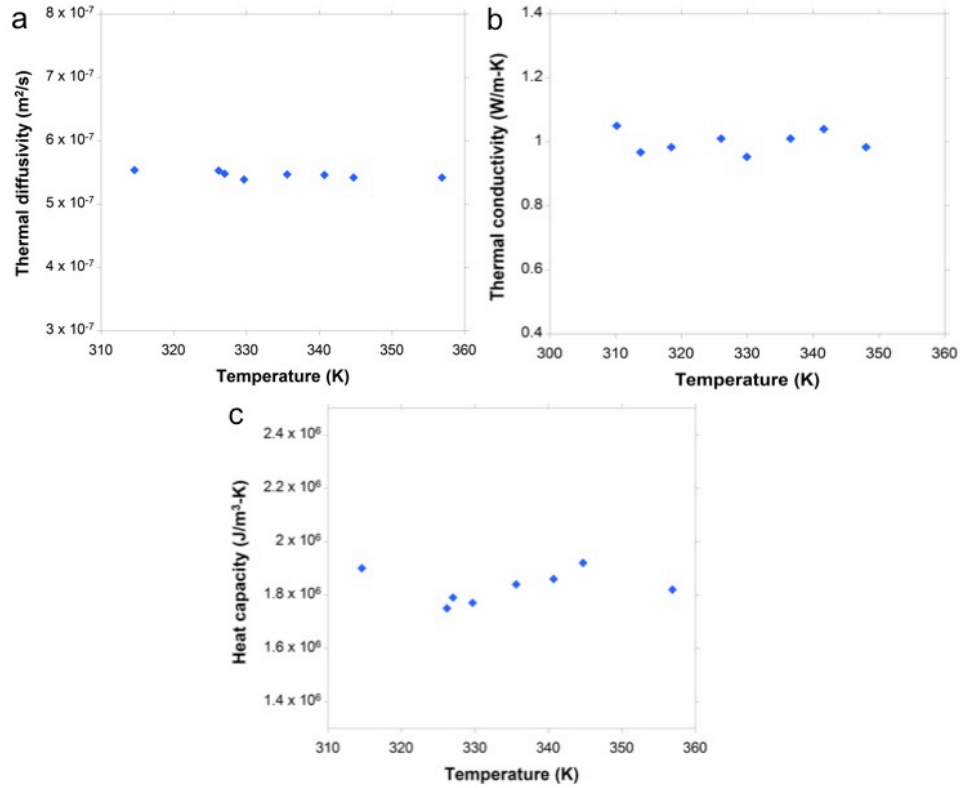
**Figure 5.8 The thermal properties measured from the SiN$_x$ and SiO$_x$ double layers by the 2ω method over the temperature range of 310-350 K. (a) Thermal diffusivity; (b) Thermal conductivity; (c) Volume specific heat capacity.**

## 5.3.3 Thermal conductivity of silicon nanomesh

The thermal conductivity of ~100 nm thick silicon nanomesh was calculated based on the conservation of thermal conductance from the three layers: SiN$_x$ (~29 nm thick), silicon nanomesh (~91 nm thick), and SiO$_x$ (~196 nm thick), according to Equation 3.45 in chapter 3, $\kappa_{Si}d_{Si} + \kappa_{SiOx+SiNx}(d_{SiOx} + d_{SiNx}) = \kappa_{stack}d_{stack}$, where d is the film thickness. The thermal conductivities of the stack layers and double layers were substituted into this equation, along with the film thicknesses, to give $\kappa_{Si}$ (Figure 5.9).
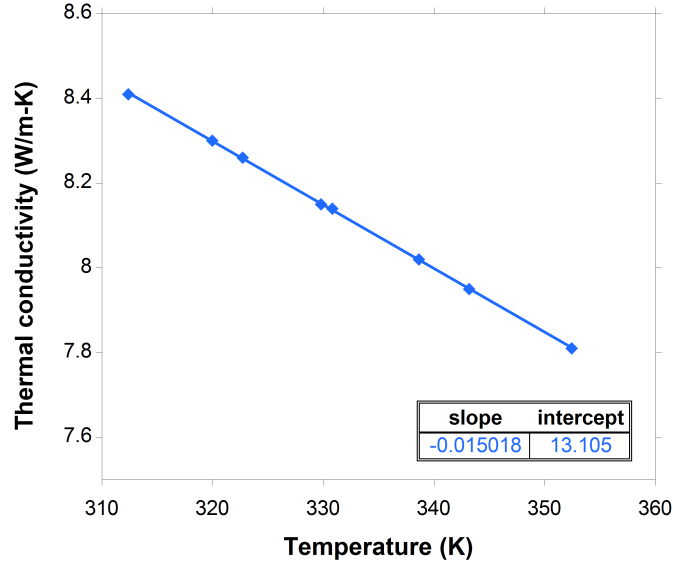
**Figure 5.9 The thermal conductivity of the silicon nanomesh thin film measured by the 2ω method over the temperature range of 310-350 K.**

Previously, P.D. Yang, et al have demonstrated that the peak of the thermal conductivity versus temperature curve (Umklapp peak, $T_{peak}$) has shifted from $T_{peak}$~130 K in bulk silicon, to $T_{peak}$~200 K in 350 nm pitch holey silicon film (100 nm thick), and to $T_{peak}$>300 K in 140 nm and 55 nm pitch holey silicon film (100 nm thick). [1] It was shown that the reduction of thermal conductivity contributed by phonon-phonon scattering was postponed to room temperature or higher when the dimension of the nanomesh or holey structure was decreased. In this study, it is likely that the Umklapp peak is below 310 K but near 300 K in the ~100 nm thick silicon nanomesh thin film with 80 nm pitch. Figure 5.9 showed the temperature dependence of thermal conductivity after approaching the peak value.

If one can assume that this thermal conductivity is linearly related to temperature over a small interval (310-320 K), $\kappa_{Si}$ at 303 K can be obtained based on an extrapolation on the first three data points in Figure 5.8, $\kappa_{Si}$ (303 K) ≈ 8.51 W/m•K. This result is

similar to the thermal conductivity of 140 nm pitch holey silicon, 6.96±0.34 W/m•K, measured by P.D. Yang, et al. [1]

## 5.4 *ZT* of silicon nanomesh

So far, the thermopower (435.99 µV/K), electrical resistivity (23.2 mΩ•cm), and thermal conductivity (8.51 W/m•K) of silicon nanomesh have been measured from three devices on the same chip at 303 K. The figure of merit *ZT* can be calculated as $ZT=S^2T/(\rho\kappa) \approx 0.03$. *ZT* is expected to be ~4 times higher than this result if the electrical resistivity of silicon nanomesh on this chip could be recovered by thermal treatments.

Next, a thermoelectric cooling device was fabricated with the same nanomesh structure and the same silicon film thickness, and the prediction on the expected cooling effect was calculated based on the same *ZT* result measured from the *ZT* on chip sample.

## 5.5 The thermoelectric cooling device and the cooling effect prediction

The purpose of conducting measurements from this nanomesh sample is to study thermoelectric cooling effects. The *ZT* obtained from the previous work is used to predict the maximum cooling an equivalent device can create. A thermoelectric device was also prepared in an attempt to directly measure this temperature difference.

### 5.5.1 The thermoelectric cooling device

A thermoelectric cooling device was fabricated using the same sample conditions as in the *ZT* measurement. In order to achieve a cooling effect, a p-n junction was made by doping two nanomesh legs (200 µm X 200 µm) with boron and phosphorus,

156

respectively, both at the concentration of ~$2 \times 10^{19}$ atoms/cm$^3$ by ion implantation. The device was completely suspended by etching away the bulk silicon handle with XeF$_2$, while the buried SiO$_x$ remained. A resistive thermometer was fabricated in the middle of the p-n junction to measure the cooling temperature. Chromium (Cr) and plantinum (Pt) films were deposited for the thermometer and metallic contacts with a thickness of 100 Å and 140 Å, respectively. The geometric parameters of the doped silicon nanomesh films and the thermometer were chosen to ensure that the thermal conductance through the silicon nanomesh films ($2.1 \times 10^{-6}$ W/K) was at least one order of magnitude higher than the thermal conductance of the thermometer, composed of Cr, Pt, and buried SiO$_x$ layers, ($5.6 \times 10^{-8}$ W/K) to obtain valid cooling measurements.

SEM images were taken of the thermoelectric device. An overview showed the layout of the suspended device (Figure 5.10, a); the cooling and environment temperatures were to be measured from the suspended thermometer, and from one of the two heater coils next to the contact pads overlapped with silicon nanomesh films. A close-up image on the p-n junction (Figure 5.10, b) showed that both the thin films and the thermometer were completely suspended. The nanomesh next to the thermometer was imaged (Figure 5.10, c) directly from the in-situ suspended device. The cross-sectional view of the nanomesh (Figure 5.10, d) confirmed a successful pattern transfer by DRIE; the etching stopped at the buried oxide layer.
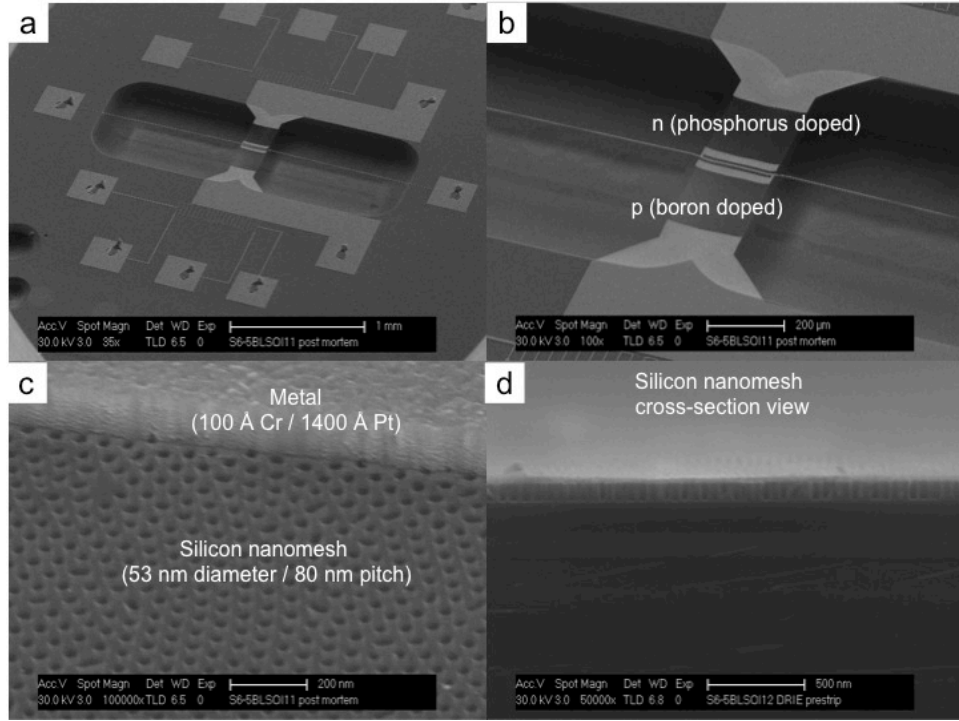
**Figure 5.10 SEM images of the suspended thermoelectric cooling device. (a) A perspective view of the device; (b) A close-up view of the p type and n type nanomesh islands and the resistive thermometer at the p-n junction; (c) The inferface of a metallic contact and the silicon nanomesh; (d) A tilted cross-sectional view of ~100 nm thick silicon nanomesh.**

The previously discussed issue with the nanomesh films being highly resistive posed a difficulty in measuring the thermoelectric cooling effect from this cooling device. However, the fabrication process was fully understood; the device proved to be a solid architecture after the suspension; and all the metallic contacts on the heater coils and the thermometer on the p-n junction were functional, with their measured resistance closely matching theoretical calculations.

Therefore, in order to understand the cooling effect in this device, mathematical calculations were performed to predict the best cooling and the current required for this optimization in the device.

## 5.5.2 The thermoelectric cooling predictions

Based on the measurement results from boron doped silicon nanomesh and the geometrical design of the cooling device, the cooling properties can be predicted under the following approximations: (a) both n and p-type legs would have the same or very similar thermopower, and (b) the electrical resistivity and thermal conductivity of both legs are also similar. The buried $SiO_x$ (200 nm thick, and $\kappa_{SiOx}\approx1$) under the silicon nanomesh is also taken into consideration.

First, when the hot side temperature, i.e. the contact pads temperature, is fixed at 303 K, the lowest temperature ($T_c*$) at the center of p-n junction can be estimated from the $\Delta T_{max}$ equation, $T_c*$=299.6 K (Equation 5.2).

$$T_h - T_c^* = \frac{(S_p + |S_n|)^2}{2K_d R_d}(T_c^*)^2 \tag{5.2}$$

($T_h$=303 K, $S_p$=-$S_n$=435.99 μV/K, $K_d$=1.95X10$^{-6}$ W/K, $R_d$=5.09 kΩ)

Then, the maximum temperature difference is $\Delta T_{max}$= $T_h$- $T_c*$=3.4 K, which is achieved when the current sent through the device is $I^*$=51.3 μA, based on

$$I^* = \frac{S_p + |S_n|}{R_d}T_c.$$

## 5.6 Summary

Three measurements were conducted on a boron doped silicon nanomesh thin film sample to obtain its thermopower (435.99 μV/K), electrical resistivity (23.2 mΩ•cm), and thermal conductivity (8.51 W/m•K) at 303 K. These results were used to calculate the cooling properties of a suspended thermoelectric cooling device composed

of equally doped phosphorus and boron nanomesh legs. The maximum temperature difference this device can generate under vacuum is 3.4 K when the hot side temperature is kept at 303 K. The electrical current required to achieve such cooling effect is 51.3 μA, flowing from the n-type leg towards the p-type leg.

## 5.7 References

[1] J. Bardeen, *Physical Review* **71** 717 (1947).

[2] S.G. Davison and M. Steslicka, *Basic Theory of Surface States*, Clarendon Press, 1992.

[3] V. Heine, *Physical Review* **138** 1689 (1965).

[4] M. Brown, *Introduction to Heat Transfer* (3rd edition), McGraw-Hill, 1958.

[5] O. Koszor, A. Lindemann, F. Davin and C. Balázsi, *Key Engineering Materials* **409** 354-357 (2009).

[6] H.R Shanks, P.H. Sidles, P.D. Maycock and G.C. Danielson, *Physical Review* **130** 1743 -1748 (1963).

# Chapter 6

# Conclusion and outlook

## 6.1 Contributions

The thermoelectric effect plays a significant role in the field of energy conversion. It can achieve direct conversion of a temperature difference to electricity and vice versa. The figure of merit $ZT$ ($ZT=S^2\sigma T/\kappa$) is a key parameter to determine the efficiencies of electric power generation and thermoelectric cooling. Higher $ZT$ results in higher efficiencies. Thermoelectric materials can be used to harvest heat from solar radiation or industrial waste heat; traditional methods for harvesting heat from such sources have been difficult to implement. Thermoelectric materials can also be used in thermoelectric cooling devices, which mostly operate in conditions where conventional refrigeration fails to function.

This study is motivated by the fact that the $ZT$ of nanostructured silicon is improved mainly by reducing its thermal conductivity ($\kappa$). Meanwhile, its power factor ($S^2\sigma$) maintains equivalent value as that in silicon without nanostructures. The significant contributions of this study are summarized below.

- Investigation of the n-type tensile strained silicon thin film with nanomesh structure for the proof of power factor enhancement. The tensile strained silicon is predicted to show higher electrical conductivity compared with unstrained silicon thin film. Studies have shown that the electron mobility at 295 K was increased by 200% in uniaxially strained silicon compared with unstrained silicon. However, the impact of strained silicon on thermoelectrics has not been studied until now. Measurements were conducted on the $S^2\sigma$ device set consisting of an electrical conductivity device and a thermopower device for each sample. The modified four-point method allowed us to measure $\sigma$ from a wire-bonded device in a temperature-controlled cryostat. The measurement results showed that, at 300 K, the electrical conductivity of the 5 nm thick phosphorus doped strained silicon thin film with nanomesh is five times as much as that of the 10 nm thick phosphorus doped unstrained silicon thin film with nanomesh. This finding is in accordance with the previously studied prediction of the strain effects on silicon. This study is also the first to discover that the power factor of strained silicon with nanomesh is enhanced by ~100% compared with that of unstrained silicon with nanomesh.

- Measurements of thermopower (S), electrical resistivity (ρ), and thermal conductivity (κ) from an ~100 nm thick silicon nanomesh sample to determine *ZT* at 303 K from the *ZT* device set. The *ZT* device set consisted of three micro-sized devices: the 2-thermometer device yielded a thermopower of 435.99 µV/K; the Greek cross structured device measured an electrical resistivity of 23.2 mΩ•cm, using the Van der Pauw method; and the 2ω device measured a thermal conductivity of 8.51 W/m•K, using a novel 2ω method. The methodology was described in detail for all three devices. In

particular, the silicon nanomesh thin film in this work was suspended to avoid thermal leakage from the handle substrate. Thus, the measured thermal conductivity is considered as an in-plane value $\kappa_X$, compared with the average result of thermal conductivity from $\kappa_X$ and $\kappa_Z$ ($\kappa_Z$ is in the direction perpendicular to the film) in the popular 3ω method. Therefore, the 2ω method gives more accurate results for thin films. Overall, *ZT* of ~100 nm thick silicon nanomesh was determined to be ~0.03 at 303 K. Due to the unexpected high resistivity of this sample, thermal treatments were investigated to reduce the damage-induced degradation of the electrical conductivity, possibly caused by the Schottky barrier at the metal-silicon nanomesh interface or the surface states of the silicon nanomesh.

- Fabrication of a thermoelectric cooling device with a suspended p-n junction doped by boron and phosphorus using the same sample conditions as in the *ZT* device set measurement. Although the highly resistive silicon nanomesh thin film posed a difficulty in measuring the thermoelectric cooling effect from this cooling device, it has allowed us to predict the cooling properties of this silicon nanomesh thin film based on the previously measured *ZT*. The maximum temperature difference this device can generate under vacuum is 3.4 K when the hot side temperature is kept at 303 K. The electrical current required to achieve such cooling effect is 51.3 μA. We have also fully understoodd the fabrication process of this device. The device also proved to be a solid architecture after the suspension. Also, the device fabrication process was fully understood, and the device proved to have a solid architecture after the suspension.

Overall, we have studied the thermoelectric properties of silicon thin films with nanomesh structures in regard to the potential of tensile strained silicon for improving *ZT*

through an enhanced power factor and in regard to the thermoelectric cooling application of silicon nanomesh thin film. We contributed valuable knowledge of the strained silicon and nanomesh structure in advancing the future study of thermoelectrics.

## 6.2 Future work

Further studies of the strained silicon will provide innovative solutions to improve *ZT* of silicon when the thermal conductivity is reduced to its minimum limit with nanoscale structures. The charge carrier concentration in this work can be further increased to between $10^{19}$ - $10^{21}$ atoms/cm$^3$ for the tensile strained silicon thin film to achieve a higher power factor or *ZT*. The compressive strained silicon should also present superior electrical conductivity if doped with p-type dopants such as boron. In this case, the strain effects occur at the valence band instead of the conduction band. The enhancement in the hole mobility in compressive strained silicon has also been proved by Intel in CMOS devices in 1990s.

For the ~100 nm thick silicon nanomesh thin film, a change of doping method from ion implantation to diffusion doping is proposed to avoid high resistivity after transferring nanomesh features to the thin film so that the thermoelectric cooling effect can be studied directly. Future studies should also examine the exact cause of the reduced electrical conductivity.