

# **Power Management Circuits for Miniature Sensor Systems**

by

**In Hee Lee**

A dissertation submitted in partial fulfillment  
of the requirements for the degree of  
Doctor of Philosophy  
(Electrical Engineering)  
in The University of Michigan  
2014

Doctoral Committee:

Professor David Blaauw, Chair  
Professor Michael Flynn  
Assistant Professor Jeffrey T. Scruggs  
Professor Dennis Michael Sylvester

*To my wife Haehyun  
and my children Sichan and Siwoo  
and my parents*

# TABLE OF CONTENTS

<b>DEDICATION</b> . . . . .	ii
<b>LIST OF FIGURES</b> . . . . .	v
<b>LIST OF TABLES</b> . . . . .	viii
<b>CHAPTER</b>	
1 Introduction . . . . .	1
1.1 Motivation . . . . .	1
1.2 Contribution of This Work and Organization . . . . .	7
2 A Constant Energy-per-Cycle Ring Oscillator over Wide Frequency Range . . . . .	11
2.1 Motivation . . . . .	11
2.2 Conventional Current-Starved Ring Oscillator (CSRO) . . . . .	13
2.3 Proposed Energy-Efficient Oscillators . . . . .	16
2.3.1 Leakage-Based Ring Oscillator for Fixed Clock Frequency . . . . .	16
2.3.2 Proposed Constant Energy-per-Cycle Oscillator (CEpCRO) . . . . .	19
2.3.3 Proposed Hybrid Ring Oscillator (HRO) . . . . .	23
2.3.4 Bias Voltage Generator . . . . .	25
2.4 Measurement Results . . . . .	26
2.5 Application Example . . . . .	30
2.6 Summary . . . . .	38
3 A Ripple Voltage Sensing MPPT Circuit . . . . .	39
3.1 Introduction . . . . .	39
3.2 Ripple Voltage Sensing . . . . .	40
3.3 Energy Harvester Using Ripple Voltage Sensing MPPT . . . . .	44
3.4 Measurement Results . . . . .	46
3.5 Summary . . . . .	49
4 A Low Power Battery Supervisory Circuit . . . . .	50
4.1 Introduction . . . . .	50
4.2 Battery Supervisory Circuit . . . . .	52
4.3 Circuit Implementation . . . . .	55

4.3.1	Diode-Stack Voltage Divider . . . . .	56
4.3.2	Voltage Reference . . . . .	59
4.3.3	Comparator and Clock Generator . . . . .	63
4.3.4	Other Blocks . . . . .	66
4.4	Reset Propagation Strategy . . . . .	68
4.4.1	Reset Propagation Strategy in mm-scale Multi-layer System . . . . .	68
4.4.2	Secondary Reset Detector . . . . .	72
4.5	Experimental Results . . . . .	74
4.6	Summary . . . . .	80
5	A Low Power Battery Supervisory Circuit with Adaptive Battery Health Monitor . . . . .	83
5.1	Introduction . . . . .	83
5.2	Proposed BSC . . . . .	86
5.3	Measurement Results . . . . .	89
5.4	Summary . . . . .	94
6	Conclusion . . . . .	95
	<b>BIBLIOGRAPHY . . . . .</b>	<b>98</b>



## LIST OF FIGURES

### Figure

1.1	Miniaturization of implantable pacemakers. . . . .	2
1.2	Examples of recent miniature sensing systems. . . . .	2
1.3	Batteries. . . . .	3
1.4	Average power budget for desired lifetime with different batteries. . . . .	4
1.5	Michigan Micro-Mote: a mm-scale sensing platform [2]. . . . .	5
1.6	mm-scale temperature sensing system [12]. . . . .	6
1.7	Implantable pressure monitor [13]. . . . .	6
2.1	Capacitive step-down converter in a wireless sensor node with a lithium battery. . .	11
2.2	Current-starved ring oscillator (a) oscillator circuit diagram (b) simplified model (c) internal node waveforms (d) circuit status of the first stage delay cell. . . . .	14
2.3	Simulated power consumption of a 7-stage conventional current-starved ring oscillator with an inverter output buffer over frequency. . . . .	16
2.4	Fixed-frequency leakage-based oscillator (a) oscillator circuit diagram (b) simplified model (c) internal node waveforms (d) circuit status of the first stage delay cell. . . . .	17
2.5	Simulated $I_{DS}$ versus $V_{DS}$ (minimum-size transistor). . . . .	18
2.6	Proposed constant energy-per-cycle ring oscillator (a) oscillator delay cell (b) simplified model (c) circuit status of a delay cell (d) internal node waveforms from oscillators with different speed. . . . .	20
2.7	Simulated power consumption of a 7-stage proposed CEpCRO with an inverter output buffer over frequency. . . . .	21
2.8	Simulated power consumption of CSRO, CEpCRO, and HRO over frequency. . . .	23
2.9	Proposed hybrid ring oscillator (HRO) (a) circuit diagram of a delay cell (b) CEpCRO mode (c) CSRO mode. . . . .	24
2.10	Bias voltage generator (a) voltage-divider-based circuit followed by analog mux (b) current-mirror-based circuit. . . . .	26
2.11	Test chip for oscillators (a) die photograph (b) test structure. . . . .	27
2.12	Measured power and energy-per-cycle of CSRO and CEpCRO (a) power (b) energy-per-cycle. . . . .	29
2.13	Measured bias voltage profile of CEpCRO over frequency. . . . .	30

2.14	Measured frequency range of CEpCRO over supply voltage (a) $f_{MAX}$ and $f_{MIN}$ (b) $f_{MAX}/f_{MIN}$ . . . . .	31
2.15	Measured performance of HRO over frequency (a) power (b) energy-per-cycle. . .	32
2.16	Measured energy-per-cycle of CSRO, CEpCRO, and HRO . . . . .	33
2.17	Test chip for a capacitive step-down converter (a) die photograph (b) converter diagram . . . . .	34
2.18	Measured converter over load power (a) input power and converter efficiency (b) operating frequency. . . . .	36
2.19	Measured power consumption of oscillators at oscillator supply voltage in the converter. . . . .	37
2.20	Efficiency of converters using CSRO and CEpCRO. . . . .	37
3.1	Conventional harvested energy monitor for maximum power point tracking (MPPT). . . . .	40
3.2	Proposed ripple voltage sensing harvested energy monitor. . . . .	41
3.3	Waveform of ripple voltage sensing harvested energy monitor. . . . .	42
3.4	Block diagram of the designed energy harvesting unit. . . . .	44
3.5	Reconfigurable switched capacitor boot converter. . . . .	45
3.6	Tracking efficiency over light intensity. . . . .	46
3.7	MPPT overhead over light intensity. . . . .	47
3.8	Examples of MPPT operation with conversion ratio. . . . .	47
3.9	Examples of MPPT operation with switch size update. . . . .	48
3.10	Die Photo. . . . .	48
4.1	Varying battery voltage and required functions of battery supervisory circuit (BSC). . . . .	51
4.2	Quiescent current over power-on-reset (POR) delay of commercial POR/BOD circuits. . . . .	51
4.3	Conventional BSC structure. . . . .	52
4.4	Proposed BSC structure. . . . .	53
4.5	Conceptual BSC operation according to battery voltage ( $V_{BAT}$ ). . . . .	54
4.6	Circuit implementation of proposed BSC. . . . .	55
4.7	Problem from small $V_{HYSTERESIS}$ in a system with high battery internal resistance. . . . .	57
4.8	Impact of process variation and mismatch on reset threshold voltages (a) $V_{TRIGGER}$ and $V_{RELEASE}$ (b) $V_{HYSTERESIS}(=V_{RELEASE}-V_{TRIGGER})$ . . . . .	58
4.9	Simulated power consumption and speed of voltage divider. . . . .	59
4.10	Problems from using conventional low-power voltage reference (a) false reset release using decoupling capacitor to ground (b) suppressed reset trigger by using decoupling capacitor to supply. . . . .	60
4.11	Simulated conventional and proposed voltage reference (a) line sensitivity (b) power supply rejection ratio (PSRR). . . . .	62
4.12	Comparator transistor diagram. . . . .	64
4.13	Simulated power consumption of preamplifier over temperature. . . . .	64
4.14	Leakage-based oscillator (a) delay cell (b) its half circuit (c) waveform (d) half circuits for each phase of operation. . . . .	65
4.15	Power consumption versus operating frequency. . . . .	67

4.16	<i>RESET</i> control. . . . .	67
4.17	1 mm <sup>3</sup> -sensor system where proposed BSC is integrated. . . . .	69
4.18	Reset propagation in 1 mm <sup>3</sup> -sensor system. . . . .	70
4.19	Conventional level converter. . . . .	71
4.20	Secondary reset detector (a) proposed reset detector (b) waveform. . . . .	73
4.21	Measured operation of BSC and secondary reset detector in the complete sensor system. . . . .	74
4.22	Measured $V_{REF}$ , $DIVVBAT$ , and ' $V_{RET}-V_{BIAS}$ ' (a) temperature dependency (b) battery voltage dependency. . . . .	75
4.23	Measured operating frequency of oscillator over temperature and battery voltage. . . . .	76
4.24	Measured parameters of BSC (a) $V_{TH,LBVRST}$ over temperature from different battery voltage transition speed (0.25 mV/s and 0.8 MV/s) (b) $V_{TRIGGER}$ , $V_{RELEASE}$ , and $V_{HYSTERESIS}$ over temperature from different battery voltage transition speed (0.25 mV/s and 0.8 MV/s) (c) POR delay over temperature and battery voltage. . . . .	78
4.25	Power consumption of BSC (a) Average power consumption from 15 chips over temperature and battery voltage (b) Power breakdown at 25 °C and 3.6 V. . . . .	79
4.26	Die photograph. . . . .	81
5.1	Battery supervisory circuit (BSC) for a wireless sensor node (Red: Proposed only). . . . .	84
5.2	Operation of conventional BSC with fixed-threshold voltages. . . . .	85
5.3	Operation of proposed BSC with adaptive-threshold voltage ( $V_{ENABLE}$ ). . . . .	86
5.4	Circuit diagram of proposed BSC with $R_{BAT}$ monitor. . . . .	87
5.5	Circuit diagram and operation of proposed $R_{BAT}$ monitor. . . . .	88
5.6	Clock and control signal generation for $R_{BAT}$ monitor. . . . .	89
5.7	Measured oscilloscope waveforms. . . . .	90
5.8	Measured $dout$ & $V_{ENABLE}$ over $R_{BAT}$ & $V_{BAT}$ . . . . .	90
5.9	Measured $R_{BAT}$ over discharge cycles & $V_{HYST}$ tracking error. . . . .	91
5.10	Measured standby power & power-on-reset delay. . . . .	92
5.11	Die photo. . . . .	93

## LIST OF TABLES

### Table

2.1	Performance summary of the proposed oscillator and comparison to other prior works . . . . .	33
3.1	Performance summary of the proposed MPPT circuit and comparison to other prior works. . . . .	49
4.1	Measured reset threshold voltages from 15 chips at 25 °C with different battery voltage transition speed. . . . .	77
4.2	Performance summary of the proposed BSC and comparison to other prior works. .	80
5.1	Performance summary of the proposed adaptive BSC and comparison to other prior works. . . . .	93

# CHAPTER 1

## Introduction

### 1.1 Motivation

Miniature sensor nodes have recently enabled new application spaces in VLSI. In the continuation of Bell's Law [1], the size of computing systems have been shrunk down to cubic-millimeter scale (e.g. Michigan micro-mote) [2]. Especially, since the term "Smart Dust" was coined [3], rapid advances in low-power wireless sensor nodes have been driving the realization of Internet of Things [4]. With a unique feature set such as wireless communication, energy harvesting, the small form-factor, thus enabling non-invasive and secure placement, the sensor nodes have been developed for a number of applications such as medical, infrastructure, and surveillance [5–8].

For example, biomedical sensors have significantly increased the quality of medical care through miniaturization. Fig. 1.1 shows how the implantable cardiac pacemakers have changed in size. Their size has been reduced by 35 times over the last 54 years. There are the reasons for creating smaller biomedical devices: 1) with a smaller device, implantation can be done through a minimally invasive surgery or even a syringe; 2) small devices have better bio-compatibility and reduce foreign body rejection; 3) the small size allows devices to be placed in new locations where the space is very limited, like eyes, which enables more efficient treatments for a disease, such as glaucoma [9].

There has been active research on miniaturization of the sensing systems [5,6,9,10]. As shown in Fig. 1.2, the size of the bare die is often 1 ~ 2 mm. However, the associated systems, which are shown in the bottom of Fig. 1.2, are typically much larger than the bare die, resulting in

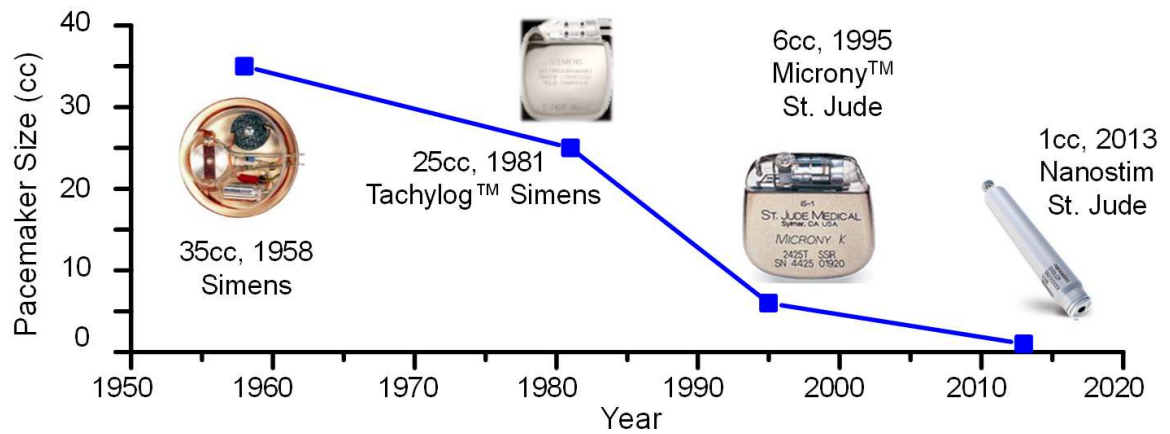


Figure 1.1: Miniaturization of implantable pacemakers.

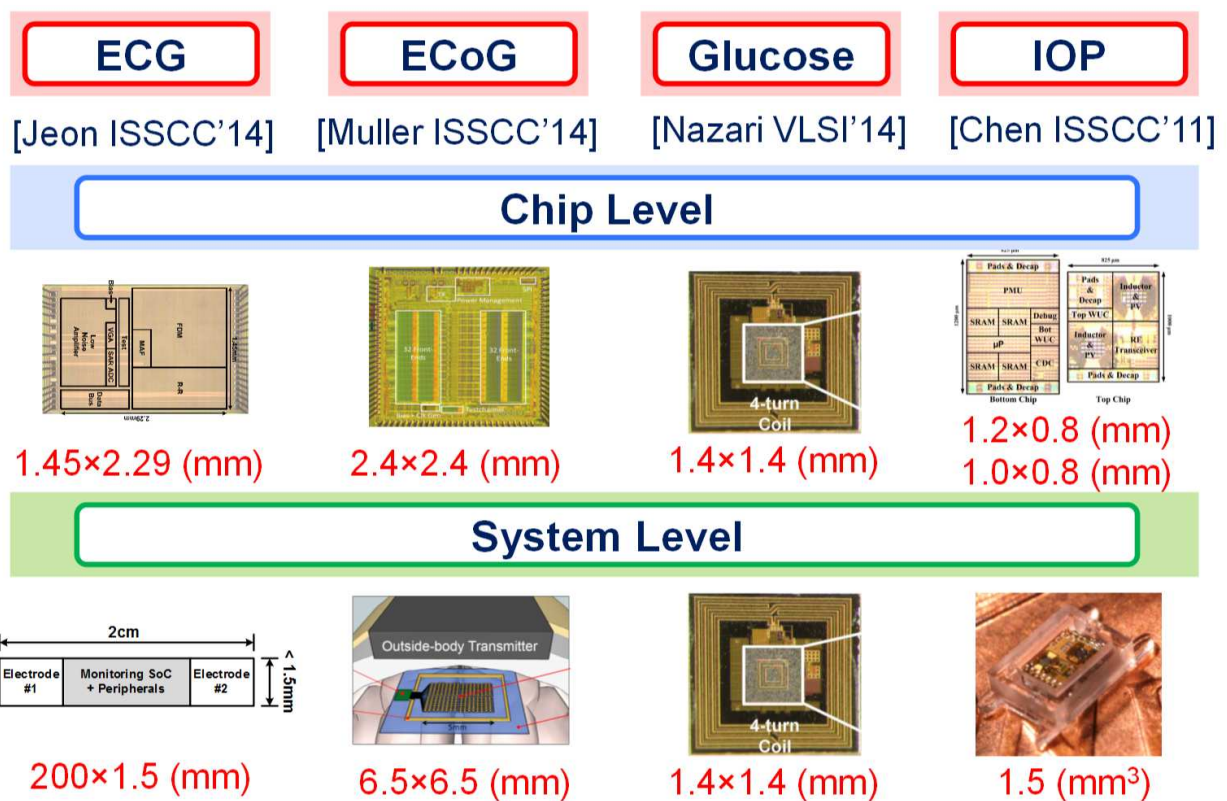


Figure 1.2: Examples of recent miniature sensing systems.

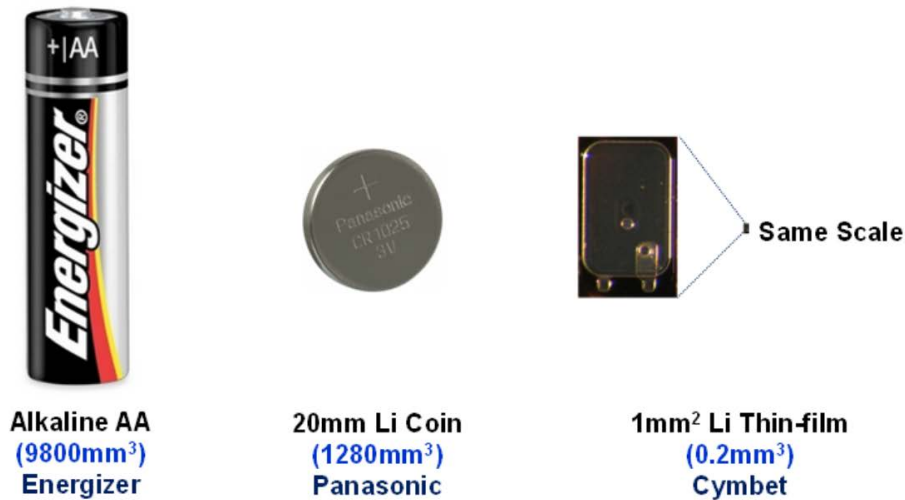


Figure 1.3: Batteries.

the size up to centimeters, due to included peripherals such as electrodes, batteries, and casings. This leads to the first design challenge for electronics of the miniaturized systems; the maximum physical battery size is severely limited, so is the battery storage capacity. This issue becomes more important in implantable biomedical sensing systems, where the battery cannot be easily replaced, since it requires a surgery which would be difficult and expensive. As a result, low-power circuit design and energy harvesting techniques need to be investigated to allow the system operation within a very small power budget. Another important issue is that discrete components cannot be used due to the size constraint. This limits use of off-chip components such as a high-density capacitor, a high q-factor inductor, and a precise crystal oscillator. Thus, it requires design of high quality on-chip references, DC-DC converters, and RF frequency synthesizers. Of course, there are other challenges as well (e.g. packaging). However, in this dissertation, we will focus on the low power circuit and energy harvesting techniques.

Fig. 1.3 shows alkaline and lithium coin batteries, which are used widely in everyday life. From these two large batteries, Fig. 1.4 shows available average power budget for desired lifetime [11]. With 10  $\mu$ W average power, a system can be sustained for over a decade. However, these large-size batteries cannot be used for a miniature sensor node. Fig. 1.3 also shows a mm-scale lithium thin-film battery, which is designed for the miniature systems. As the battery size is reduced, its battery storage capacity is also limited as shown in the blue line in Fig. 1.4. With 2 nW to 200 nW average power consumption, a system can survive several days (up to a month). This lifetime

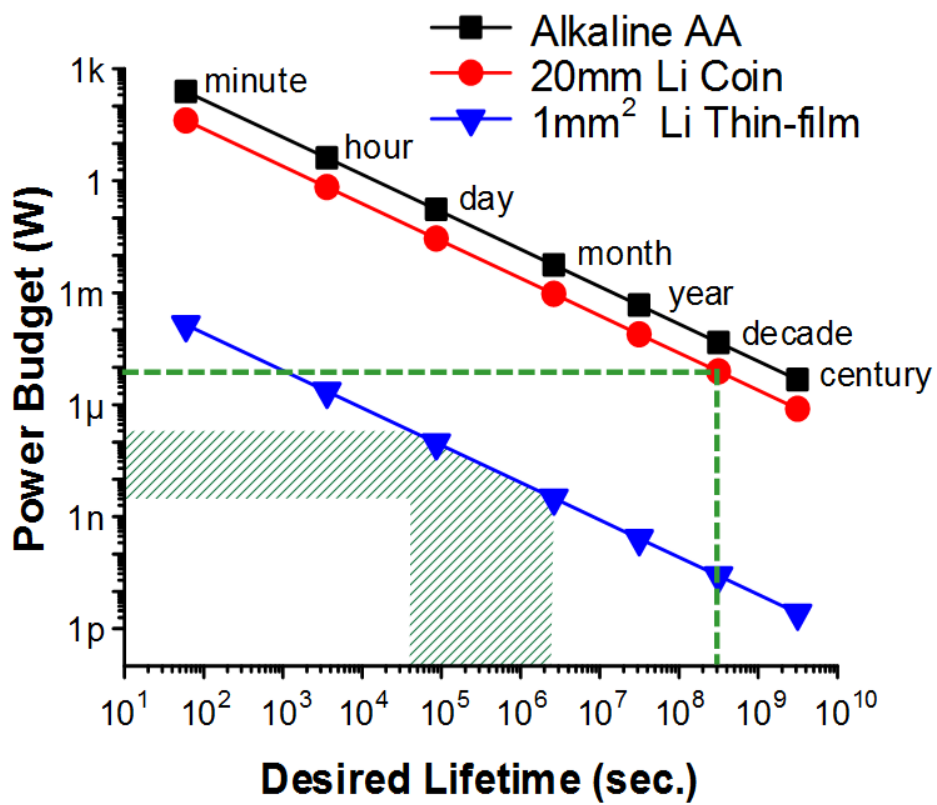
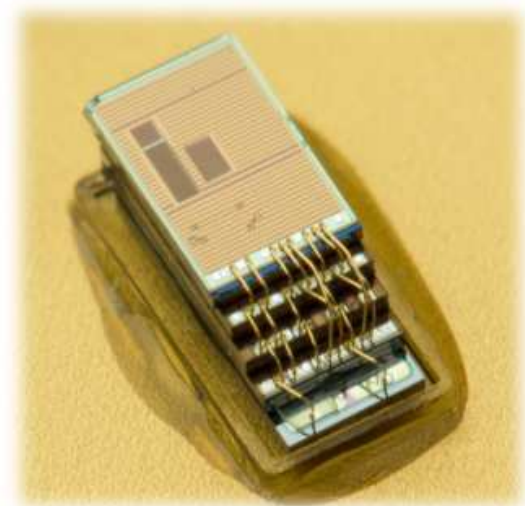
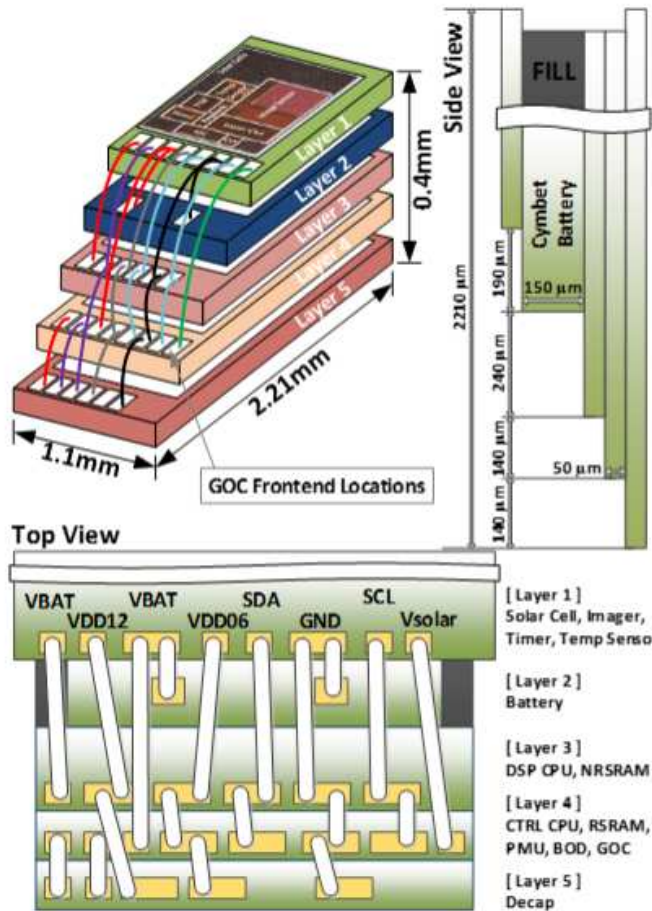


Figure 1.4: Average power budget for desired lifetime with different batteries.



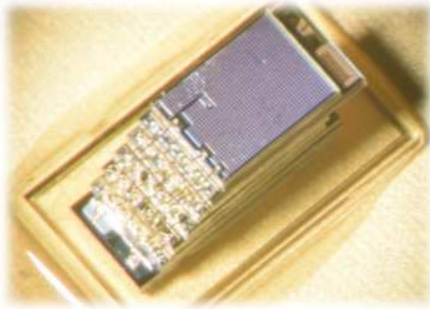


- Size: 1.1 × 2.2 × 0.4 (mm)
- Modular die-stacked structure
- Enables diverse technology
- Swappable layers
- 12.3mm<sup>2</sup> in 2.5mm<sup>3</sup>

Figure 1.5: Michigan Micro-Mote: a mm-scale sensing platform [2].

can then be extended with the help of an energy harvester. If the harvested power is larger than the average power of the system, the lifetime becomes no longer limited by the battery capacity but by the battery endurance, i.e., the number of charging cycles till the battery becomes worn out.

With this energy limitation, a mm-scale sensing platform, called Michigan micro-mote, has been developed [2]. In order to optimize circuit performance, the system is constructed from die fabricated in different technologies which are then stacked and wire-bonded together. Fig. 1.5 shows the wire bonding scheme for electrical connectivity. The stacked structure increases silicon area per unit volume and also makes it easy to swap layers in and out for flexibility in system configuration. To create a sensor system for new applications, end users can design an application-specific layer in a preferred technology, which complies with the given system power and communication interface. Fig. 1.6 shows a mm-scale temperature sensing system based on the platform [12]. Its size is 1.1mm × 2.2mm × 1mm and consists of an energy harvester, a recharge-



- Size: 1.1 × 2.2 × 1.0 (mm)
- 2nA standby power
- Self-starting harvester
- Able to sustain in room light (400lux)

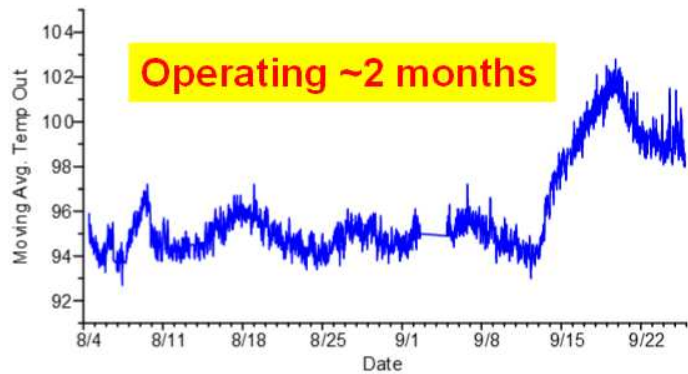
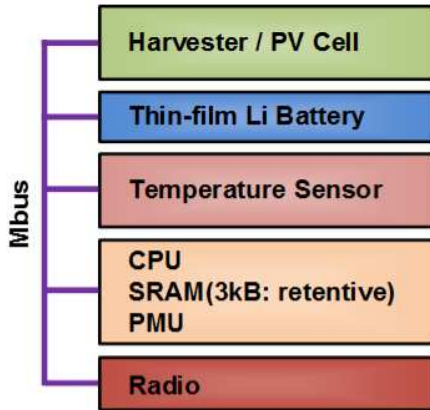
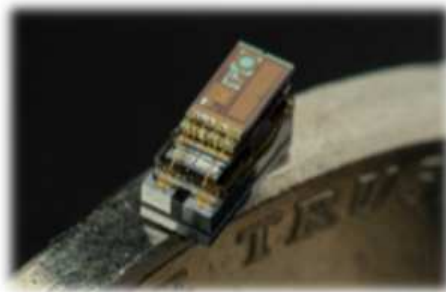
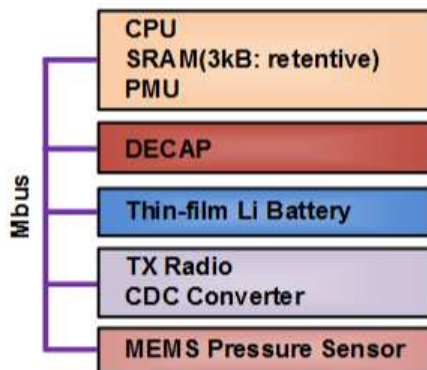


Figure 1.6: mm-scale temperature sensing system [12].



- On the size of a US 5 cent coin
- MEMS pressure sensor
- Capacitive-to-Digital conversion
- RF transmission



**[Pressure Readout from mouse]**

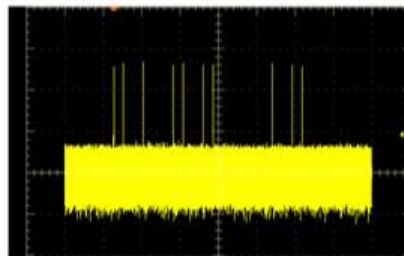


Figure 1.7: Implantable pressure monitor [13].

able thin-film lithium battery, a temperature sensor, an ARM processor, a 3kB retentive SRAM, power management circuits, and a near-field radio transmitter. For inter-layer communications, a low-power serial protocol, called Mbus, is used. This temperature sensing system has 8 nW standby power. With self-starting harvesting, it can sustain indefinitely in the room light condition, which is about 400 lux. In this condition, the system has survived a long-term test (over 1 month of operation), which is also shown in Fig. 1.6. Fig. 1.7 shows another miniature system, which is an implantable pressure monitor [13]. The system is small enough to be placed on the side of a nickel. This pressure monitor includes a MEMS pressure sensor and a capacitive-to-digital converter. The system was implanted in a mouse and radio signals were received from the in-vivo sensor.

In these miniature sensing systems, there are four different energy flows: 1) energy harvester from a source (e.g., solar cells) to the battery; 2) power delivery circuits (e.g., Power Management Unit); 3) always-on circuits; 4) duty-cycled circuits. Available energy from the source of the harvester changes depending on the environmental condition, and the load current also changes considerably due to the duty-cycled operation. In such a dynamic system, an optimization of the energy harvester and the power converter is a key issue. In order to minimize the average power consumption to achieve a longer lifetime, always-on circuits should be designed to meet the extremely low standby power requirement of the system. Also, duty-cycled circuits need to be power-gated to keep the low standby power.

In this dissertation, new circuit techniques developed to satisfy these requirements will be discussed, which include a constant energy-per-cycle ring-oscillator designed for wide frequency range and a low power maximum-power-point-tracking circuit. A low power battery supervisory circuit and a battery health monitoring circuit will be also covered.

## **1.2 Contribution of This Work and Organization**

In Chapter 2, two energy-efficient oscillators that can be used for power converters are discussed. They are based on a leakage-based oscillator where the intermediate voltage region that causes a short-circuit current is quickly restored to the full-rail voltage, and the amount of the cell delay is determined by charging/discharging the internal nodes through the leakage. Also, the oscillators provide wide frequency range without a loss in energy efficiency thanks to a current

feeding scheme with gate voltage control. A test chip is fabricated in 0.18  $\mu\text{m}$  CMOS process, and the measurements show that the first proposed oscillator, Constant Energy-per-Cycle Ring-Oscillator (CEpCRO), achieves the constant energy-per-cycle of 0.8 J/cycle in 21 Hz  $\sim$  60 MHz, which is more energy-efficient than a conventional Current-Starved Ring-Oscillator (CSRO) if operating below 300 kHz at 1.8 V supply voltage. CEpCRO is implemented in a capacitive step-down converter, and compared to a converter using CSRO, it shows 56 % higher converter efficiency for 583 pW load power. The second proposed oscillator, Hybrid Ring-Oscillator (HRO), improves energy efficiency by 56 % for  $>80$  kHz operations, compared to CEpCRO, by utilizing different modes to reduce switching capacitance.

In Chapter 3, Maximum-Power-Point-Tracking (MPPT) circuit is described which measures ripple voltages in a switched capacitor energy harvester. Miniature-scale systems are typically equipped with a harvesting unit (solar, thermal, etc.) to recharge their battery. The small form factor of these sensors has led designers to use integrated switched capacitor boost converters (SCBCs) with a total capacitance in the range of 0.5 to 1.5 nF. Furthermore, the efficient energy extraction from the energy source, as well as the voltage up-conversion, has a major priority due to the limited size of the harvesting unit. However, there are various types of energy sources, and their operating point can significantly vary. A highly flexible SCBC is therefore needed that effectively performs maximum power point tracking (MPPT), allowing it to automatically search for and track the optimum configuration that delivers the maximum power to the battery. The proposed design demonstrates an MPPT circuit that takes advantage of the unique structure of SCBC - it has a small sampling capacitor in parallel with the flying or decoupling cap in the SCBC that “eavesdrops” on the voltage transfer that occurs in the voltage converter. The power delivered to the battery can be determined by integrating the small voltage fluctuations using correlated double sampling (CDS). Since the sampling capacitor is  $64.8\times$  smaller in size than the flying cap, the impact on the conversion efficiency is negligible. By directly tracking the power delivered to the battery, all parameters of the SCBC can be optimized, including the switching frequency, the switch size, and the conversion ratio. In general, MPPT involves simultaneous measurements of both voltage and current delivered to the battery, which are multiplied and fed into a search algorithm. Given the small power budget of micro-sensors, the voltage/current measurements and the search algorithm must be performed with minimum power overhead. Conventional comprehensive MPPT methods

where the battery inflow current is measured have the advantage of directly measuring energy delivered to the battery, but they incur a voltage drop over the current mirror transistors, resulting in significant energy loss. Furthermore, they also require a high bandwidth amplifier to track the dynamic current influx. Compared to the conventional current-mirror type MPPT circuits, the proposed design incurs no voltage drop and does not require high bandwidth amplifiers. Using correlated double sampling, the measured results in 180 nm CMOS show that high accuracy is achieved with only 5 % overhead in the power consumption even at low harvested current of 1.4  $\mu\text{A}$ .

In Chapter 4, a low-power battery supervisory circuit (BSC) is discussed. It provides power-on reset, brown-out detection, and recovery detection to prevent system malfunction and battery damage. In general, mm-scale systems are equipped with a harvesting unit (e.g., solar cells) to recharge their battery. They therefore require a battery supervisory system to perform three critical functions: 1) Power-On Reset (POR) detects power-on when the battery is initially connected and properly resets the sensor electronics; 2) Brown-Out Detection (BOD) detects dangerously low battery voltages and disconnects the battery from the system because, otherwise, it could damage the battery or cause unpredictable circuit operation; 3) Recovery Detection (RCD) determines whether a sufficient voltage level is restored through harvesting to re-activate the normal system operation. A BSC is one of the few always-on components in a sensor node. Given the total average power limit of a few nW for typical mm-scale systems, BSC current draw is therefore limited to  $\sim 1$  nA to prevent it from dominating the overall power budget. While commercial POR/BODs are widely available, their typical power consumption is in the order of 0.1-to-10  $\mu\text{A}$  range, motivating the work on ultra-low power BSC designs to enable the emerging class of ultra-small sensor nodes. Ultra-low power is achieved using a 57 pA, fast stabilizing two-stage voltage reference, an 81 pA leakage-based oscillator, and a clocked comparator. The BSC was fabricated in 180 nm CMOS and consumes 635 pW at 3.6 V supply voltage, which is a  $213\times$  reduction over the best prior work. Integrated with a complete 1 mm<sup>3</sup> sensor system, the BSC controls the reset functionality of electronics on its own die as well as orchestrates the reset sequence in other chip layers by modulating power supply voltages that are monitored by secondary reset detectors on those dies.

In Chapter 5, an adaptive battery supervisory system with a battery quality monitor is described. It automatically adapts to the battery health, which can be estimated from its internal resistance



( $R_{BAT}$ ), and establishes a constant effective threshold voltage. Compared to a conventional fixed-threshold BSC, the new design avoids oscillation and widens the usable range of battery voltages, independent of  $R_{BAT}$ .  $R_{BAT}$  is measured by inducing a test current using decap and measuring the resulting RC response time. Miniature wireless sensor nodes are unique in that they employ very small batteries with high  $R_{BAT}$  leading to large IR drops. Battery health degrades with discharge cycles, increasing  $R_{BAT}$ , and it is also dependent on environment conditions. As a result, the current BSC approach requires a large  $V_{HYST}$  to accommodate the worst-case  $R_{BAT}$  over its lifetime, which delays system turn-on time and reduces the usable range of battery voltages ( $V_{USE}$ ) over which the system can operate. When tested with a  $2 \mu\text{Ah}$  battery and  $11 \mu\text{A}$  sensor system, the BSC improves the required hysteresis from  $656 \text{ mV}$  to  $77 \text{ mV}$ , increasing the usable battery voltage range by  $2.7\times$ .

All presented works are summarized and concluded in Chapter 6.

## CHAPTER 2

# A Constant Energy-per-Cycle Ring Oscillator over Wide Frequency Range

### 2.1 Motivation

Recent trend in miniature sensor nodes is designing energy-efficient systems to realize energy autonomy using an energy harvester [14, 15]. For this goal, WSNs adaptively optimize themselves according to energy harvesting, load power, and battery voltage condition in circuits such as power converters, dynamic frequency scaled circuits, and adaptive analog/RF circuits [15–20]. One of the adaptive techniques is changing operation speed by switching clock frequency for higher efficiency [18–20].

As an examples, Fig. 2.1 shows a capacitive step-down converter in a WSN with a lithium

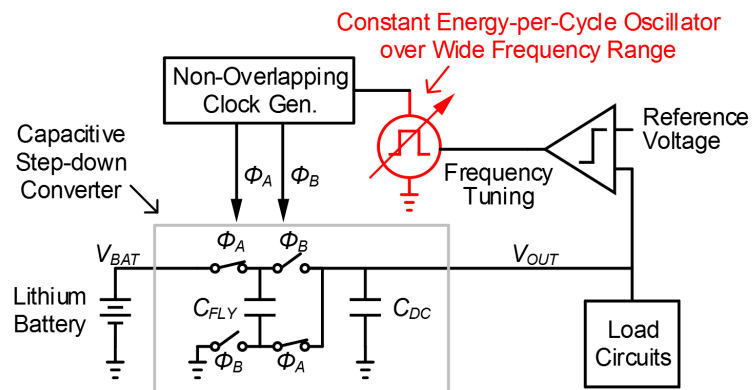


Figure 2.1: Capacitive step-down converter in a wireless sensor node with a lithium battery.

battery. It delivers power from high battery voltage to a level where load circuits efficiently operate (e.g., 0.6 V [2] and 0.45 V [21] for microprocessors and SRAM). Its energy efficiency mainly depends on switching and conduction losses [22]. Switching loss comes from energy spent to charge/discharge parasitic capacitance and drive power switches. Conduction loss results from on-resistance of power switches by Joule effect. As operating frequency becomes faster, switching loss increases by  $C \times V_{DD}^2 \times f$  whereas conduction loss decreases in slowing-switching limit (SSL) and saturated in fast-switching limit (FSL) [23]. The optimal operating point for the highest efficiency exists at frequency where the sum of those losses is minimized. However, the point varies according to load power condition. For instance, the converter in [2] changes switching frequency to 340 Hz for 1-to-10 nW load power in standby mode to save energy while it uses 335 kHz for 1-to-10  $\mu$ W in active mode for high performance operation.

An oscillator in the WSN requires not only to cover wide frequency range, but also to consume less power with lower frequency not to dominate overall power at slow speed. For this requirement, a ring oscillator is a good candidate due to wide tuning range, small silicon area, and compact design. However, in previous ring oscillators, power scalability to frequency is not considered as an important factor although it covers 10s of Hz to 100s of MHz [24–30]. A ring oscillator in [31] scales its power consumption from 1.75 kHz to 10 MHz in simulation by using signals from earlier delay stage to reduce short-circuit current, but it is not verified on silicon.

In this section, we propose two energy efficient oscillators over a wide range of frequency to maintain energy efficiency for circuits in WSNs. They are based on a leakage-based oscillator topology that charges/discharges capacitance without short-circuit current [32]. The first oscillator employs current feeding scheme with gate voltage control in a leakage-based oscillator to efficiently control output frequency. Due to rapid escape from short-circuit current region, its power consumption scales with frequency over wide frequency range. The second oscillator combines benefits of a current-starved ring oscillator and the first proposed oscillator. It improves its efficiency by switching mode to reduce switching capacitance.

The prototype oscillators are implemented in a standard 0.18  $\mu$ m CMOS process. The first proposed oscillator achieves constant 0.8 J/cycle over 21 Hz  $\sim$  60 MHz at 1.8 V power supply, which is higher efficiency than a current-starved ring oscillator (CSRO) below 300 KHz. The second one improves its energy efficiency by 56 % than the first one above 80 kHz.



## 2.2 Conventional Current-Starved Ring Oscillator (CSRO)

Fig. 2.2 (a) shows CSRO. Its delay stage consists of a delay generator ( $M_{X2}$  and  $M_{X3}$ ) and a current starving circuit ( $M_{X1}$  and  $M_{X4}$ ). Charging/discharging current depends on source-to-drain resistance of the current starving circuit, which is controlled by their gate voltage ( $V_{BIASP}$  and  $V_{BIASN}$ ). The gate voltage control enables the oscillator to tune output clock frequency with low energy efficiency penalty. An internal signal ( $N_1$ ) is connected to a logic inverter ( $M_{B1}$  and  $M_{B2}$ ) to buffer the output.

To simplify, transistors are modeled as shown in Fig. 2.2 (b). The current starving transistors are represented by current sources of  $I(V_{BIASP})$  and  $I(V_{BIASN})$ , and the delay generator is modeled by ideal switches with leakage current sources of  $I_{LEAKP}$  and  $I_{LEAKN}$ .  $C_L$  is the sum of parasitic capacitance charged or discharged. For the first stage,

$$C_L = C_{db,M11} + C_{sn,M12} + C_{db,M12} + C_{db,M13} + C_{sb,M13} + C_{db,M14} + C_{gs,M22} + C_{gs,M23}. \quad (2.1)$$

The inverter buffer is similarly modeled except for switch internal resistance ( $R_1$  and  $R_2$ ).

Based on this model, Fig. 2.2 (c) shows the waveform of internal nodes ( $N_1$ ,  $N_2$ , and  $N_3$ ) in steady state. Fig. 2.2 (d) displays circuit status of the first stage delay cell where input is  $N_1$  and output is  $N_2$ .  $V_{THN}$  and  $V_{THP}$  are threshold voltages for NMOS and PMOS, respectively. Here, it is assumed that  $I(V_{BIASP})$  or  $I(V_{BIASN}) \gg I_{LEAKP}$  or  $I_{LEAKN}$  and current starving transistors are in saturation region, and thus their dependency on  $V_{DS}$  is negligible. In phase A and C, the delay cell charges or discharges  $C_L$  according to  $I(V_{BIASP})$  and  $I(V_{BIASN})$ .  $I_{LEAKP}$  and  $I_{LEAKN}$  disturb the charging/discharging operation.

For slow clock generation, the input signals slowly pass voltage range between  $V_{THP}$  and  $V_{THN}$  with low  $I(V_{BIASP})$  and  $I(V_{BIASN})$ . In this region (phase B), short circuit current flows in the delay cells and inverter buffer by connecting both top and bottom switches together. It results in energy loss since it does not contribute to generate a clock pulse but only waste energy.

From the simplified model, overall period for the N-stage oscillator and time for each phase

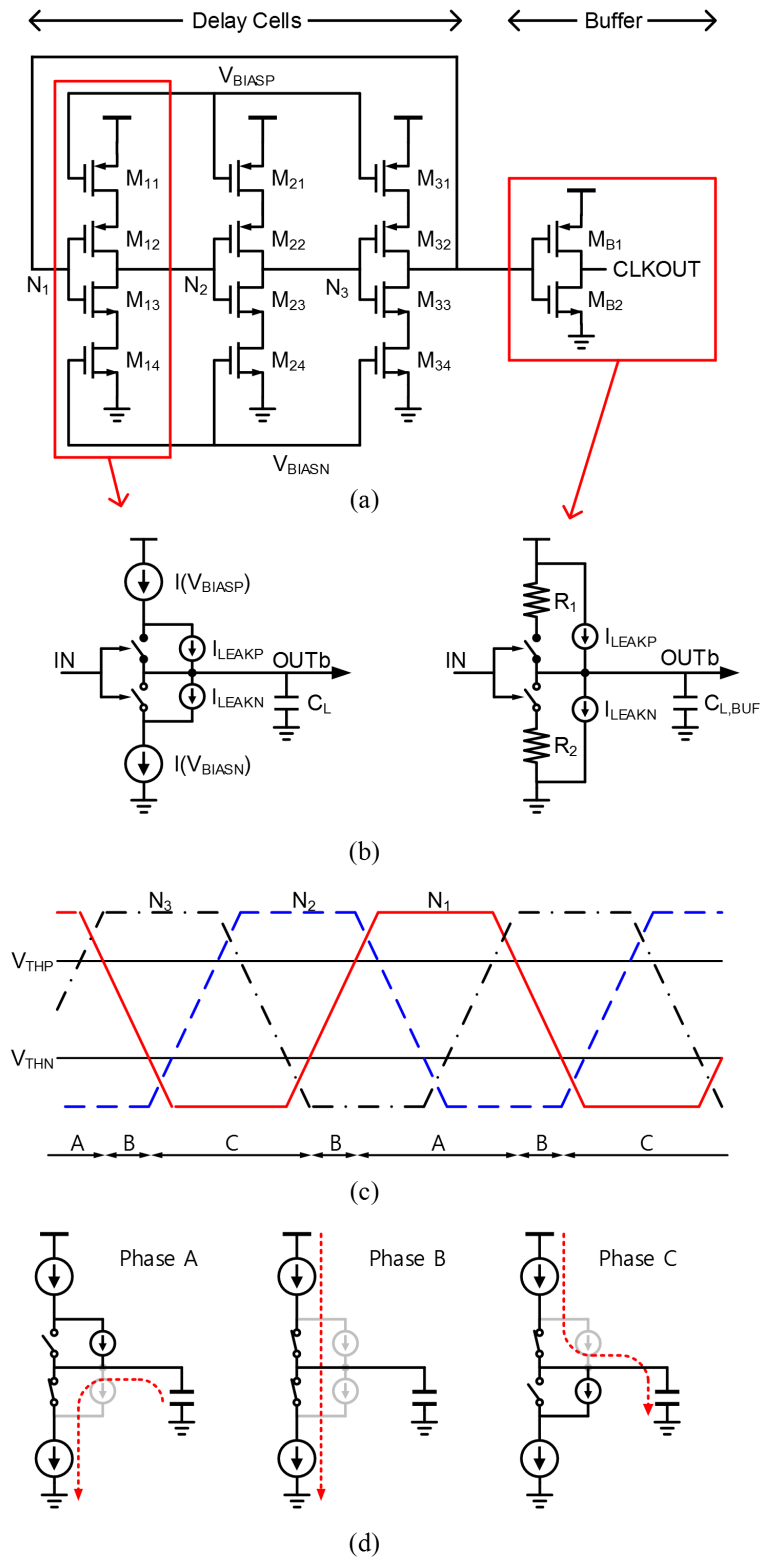


Figure 2.2: Current-starved ring oscillator (a) oscillator circuit diagram (b) simplified model (c) internal node waveforms (d) circuit status of the first stage delay cell.

can be calculated as follows:

$$T_{Period} = 2NC_L(V_{DD} - V_{TH})/I_{BIAS}, \quad (2.2)$$

$$T_A = T_C = C_L((N - 1)V_{DD} - (N - 2)V_{TH})/I_{BIAS}, \quad (2.3)$$

$$T_B = C_L(V_{DD} - 2V_{TH})/I_{BIAS}, \quad (2.4)$$

where  $V_{TH} = V_{THN} = V_{THP}$ , and  $I_{BIAS} = I(V_{BIASN}) = I(V_{BIASN})$ .

Energy-per-cycle (EpC) is required energy for one clock cycle, which is as a commonly used figure-of-merit for energy-efficient oscillators [33, 34]. From equation 2.2 and 2.4, EpC of this oscillator can be obtained as:

$$\begin{aligned} EpC &= E_{charging} + E_{leakage} + E_{sc,delaycell} + E_{sc,buf} \\ &= (NC_L + C_{BUF})V_{DD}^2 + 2(N + 1)I_{LEAK}V_{DD}T_A + 2NI_{BIAS}V_{DD}T_B + 2I_{BUF}V_{DD}T_B, \end{aligned} \quad (2.5)$$

where  $I_{LEAK} = I_{LEAKN} = I_{LEAKP}$ ,  $I_{BUF} = V_{DD} / (R_1 + R_2)$ , and  $C_{BUF} = C_{gs,MB1} + C_{gs,MB2} + C_{db,MB1} + C_{db,MB2}$ . By equation 2.2 and 2.3, the terms from short-circuit current can be expresses as:

$$E_{sc,delaycell} = 2NC_LV_{DD}(V_{DD} - 2V_{TH}), \quad (2.6)$$

$$E_{sc,buf} = I_{BUF}V_{DD}(V_{DD} - 2V_{TH})/2fN(V_{DD} - V_{TH}), \quad (2.7)$$

where  $f = 1 / T_{Period}$ . Although short-circuit current in delay cells increases dynamic power of the oscillator, it results in constant energy-per-cycle, and its power is proportional to frequency. However, due to short-circuit current, the inverter buffer consumes constant power with slow frequency, increasing energy-per-cycle.

Fig. 2.3 shows the power consumption of CSRO over frequency. The delay cells have power proportional to frequency. However, the output buffer suffers from short-circuit current and its power is limited to 130 nW below  $\sim 1$  MHz. Thus, circuits using this oscillator cannot maintain energy-per-cycle below that frequency.

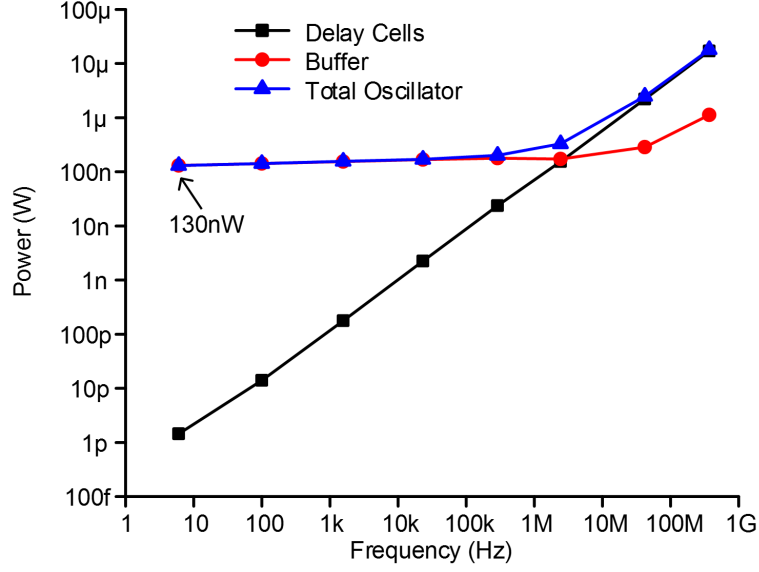


Figure 2.3: Simulated power consumption of a 7-stage conventional current-starved ring oscillator with an inverter output buffer over frequency.

## 2.3 Proposed Energy-Efficient Oscillators

### 2.3.1 Leakage-Based Ring Oscillator for Fixed Clock Frequency

A leakage-based oscillator introduced in [32] is shown in Fig. 2.4 (a) as a conceptual 3-stage ring oscillator. It efficiently generates slow frequency clock with low power (e.g. 100 Hz with 10 pW) by rapidly escaping voltage region that causes short circuit current. The delay cell includes input transistors ( $M_{X1A}$ ,  $M_{X1B}$ ,  $M_{X4A}$ , and  $M_{X4B}$ ) and back-to-back inverters ( $M_{X2A}$ ,  $M_{X2B}$ ,  $M_{X3A}$ , and  $M_{X3B}$ ). Input and output consist of differential configuration. The back-to-back inverters accelerate changing output status to reduce short circuit current. Two inverters are added as buffers for balanced output.

Fig. 2.4 (b) shows a simplified model for a delay cell of the leakage-based oscillator. The output buffer can be modeled as CSRO. Fig. 2.4 (c) and (d) shows oscillator internal signals in steady state and circuit status of the first stage delay cell (input:  $N_{1X}$  & output:  $N_{2X}$ ), respectively. For simplification, only a left half circuit is displayed.

In phase A,  $N_{2A}$  (OUTb) is initially supply voltage while  $N_{1A}$  (IN) just becomes supply voltage. Since  $N_{2B}$  is ground,  $S_2$  and  $S_4$  are connected whereas  $S_1$  and  $S_3$  are disconnected. There are two leakage paths. One comes from  $I_{LEAK3}$  and  $S_4$ , and the other does from  $I_{LEAK1}$  and  $S_2$ . Since  $V_{DS}$

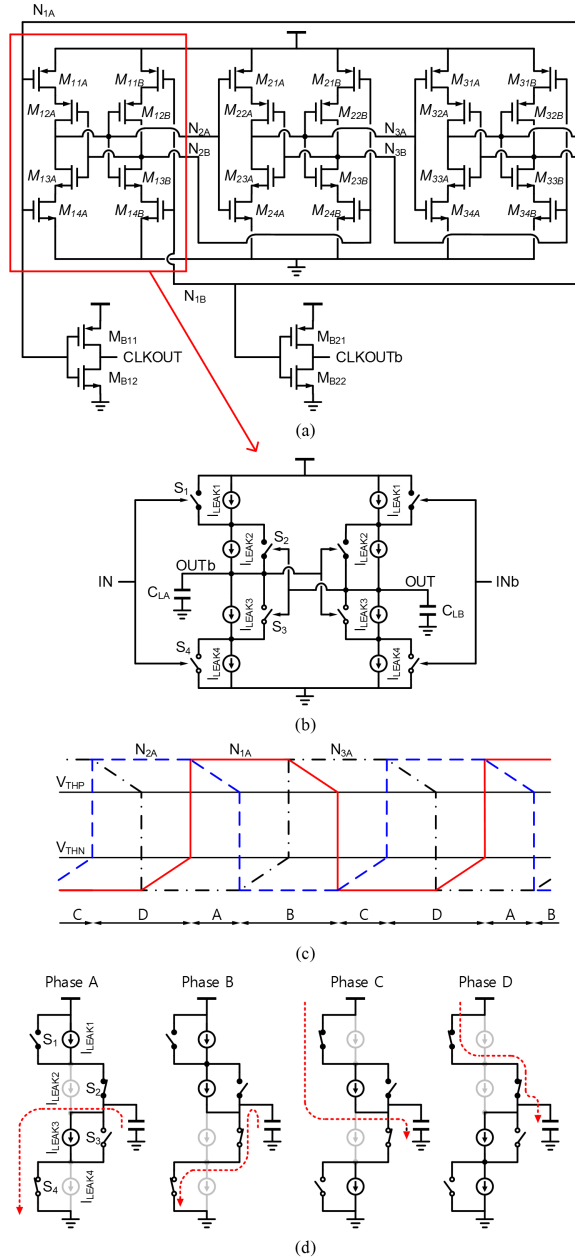


Figure 2.4: Fixed-frequency leakage-based oscillator (a) oscillator circuit diagram (b) simplified model (c) internal node waveforms (d) circuit status of the first stage delay cell.

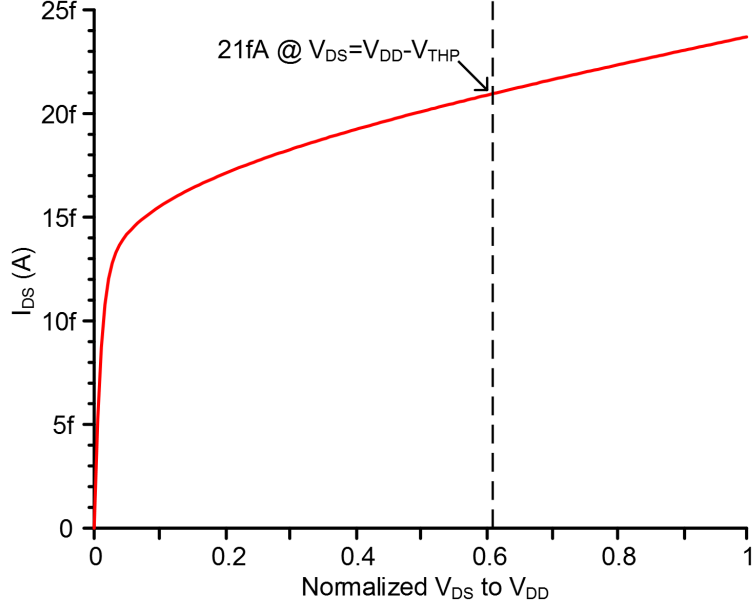


Figure 2.5: Simulated  $I_{DS}$  versus  $V_{DS}$  (minimum-size transistor).

of  $M_{13A}$  is larger than  $V_{SD}$  of  $M_{11A}$  due to high  $N_{2A}$ , the leakage path to ground dominates. Fig. 2.5 shows drain current of a minimum-size NMOS transistor.  $I_{DS} = 0$  A at  $V_{DS} = 0$  V while  $I_{DS} = 21$  fA at  $V_{DS} = V_{DD} - V_{THP}$ . The dependency of  $I_{DS}$  on  $V_{DS}$  can be found in subthreshold current equation ( $V_{GS} = 0$  V) expressed as:

$$I_{DS} = \mu C_{OX} \frac{W}{L} (m-1) V_T^2 e^{-\frac{V_{TH}}{mV_T}} (1 - e^{-\frac{V_{DS}}{V_T}}). \quad (2.8)$$

where  $\mu$  is mobility,  $C_{OX}$  is oxide capacitance,  $W$  is transistor width,  $L$  is transistor length,  $m$  is subthreshold slope factor ( $m = 1 + C_d/C_{OX}$  where  $C_d$  is depletion capacitance), and  $V_T$  is thermal voltage ( $kT/q$ ). Also, the current can be more increased by short-channel effect such as drain-induced barrier lowering (DIBL) and gate-induced drain leakage (GIDL) in advanced technology. The small discharging current sets a period of this oscillator with phase C, which is complementary phase of A.

Phase B begins when  $N_{2A}$  becomes lower than  $V_{THP}$  while  $N_{2B}$  does higher than  $V_{THN}$ . Since  $N_{1A}$  is still higher than  $V_{THP}$ ,  $S_3$  and  $S_4$  are connected whereas  $S_1$  and  $S_2$  are disconnected. It immediately discharge  $C_{LA}$  and charge  $C_{LB}$ . This rapid voltage transition allows to avoid short-circuit current in the oscillator itself and buffers by quickly escaping voltage range between  $V_{THN}$  and

$V_{THP}$ . Note that the short-circuit current in a buffer degrades energy efficiency in the conventional CSRO.

The delay cell enters phase C as  $N_{1A}$  becomes lower than  $V_{THP}$ . Here,  $C_{LA}$  is charged by  $S_1$  and  $I_{LEAK1}$ . In contrast to phase A, charging leakage is larger than discharging one since  $N_{2A}$  is ground and  $V_{SD}$  of  $M_{11A}$  is larger than  $V_{DS}$  of  $M_{14A}$ .

Phase D starts with  $N_{2A}$  increased above  $V_{THN}$ .  $N_{1A}$  stays as ground, and  $S_1$  and  $S_2$  are connected whereas the others are disconnected.  $C_{LA}$  is instantly charged, and  $N_{2A}$  jumps to voltage higher than  $V_{THP}$ . As complementary phase of B, it helps to prevent short-circuit current.

Since the voltage transition time in phase B and D is negligible, the clock period of this oscillator is decided by the sum of charging time between ground to  $V_{THN}$  during phase A and discharging time between  $V_{THP}$  to supply voltage during phase C. Due to small leakage current, this leakage-based oscillator offers a clock with long period. It can generate a slow clock with higher energy efficiency than CSRO since short-circuit current issue is resolved by fast voltage transition between  $V_{THN}$  to  $V_{THP}$  in phase B and D.

### 2.3.2 Proposed Constant Energy-per-Cycle Oscillator (CEpCRO)

Using the leakage-based oscillator topology, we propose a constant energy-per-cycle ring oscillator (CEpCRO) of which power scales with frequency. In order to adjust output clock speed, gate voltage control scheme is employed as shown in Fig. 2.6 (a). It includes the same input transistors and back-to-back inverters as the leakage-based oscillator. In addition, current control transistors ( $M_{CPA}$ ,  $M_{CPB}$ ,  $M_{CNA}$ , and  $M_{CNB}$ ) are added to adjust charging and discharging current.

In contrast to CSRO, CEpCRO changes output clock frequency by the opposite concept. CSRO changes its output frequency by limiting current while the proposed one inject more current for frequency change. When current control transistors are disabled, the proposed oscillator operates as the leakage-based oscillator generating the slowest frequency. For higher clock frequency, more charging/discharging currents,  $I(V_{BIASN})$  and  $I(V_{BIASN})$ , are added by current control transistors as shown in Fig. 2.6 (b). Oscillator frequency can be modified with different load capacitance and transistor size, but gate voltage control scheme is selected to minimize overhead from additional capacitance as CSRO.

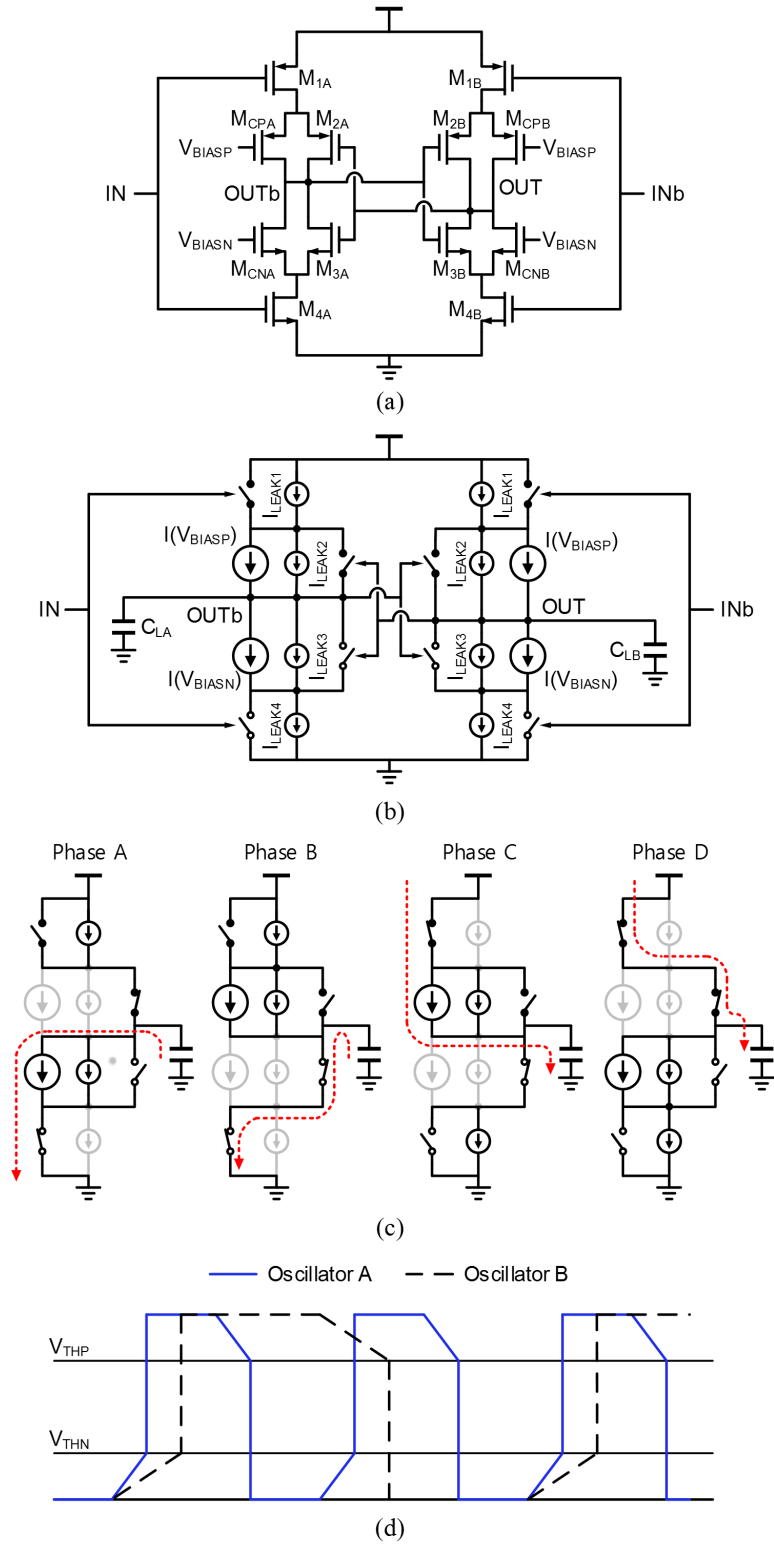


Figure 2.6: Proposed constant energy-per-cycle ring oscillator (a) oscillator delay cell (b) simplified model (c) circuit status of a delay cell (d) internal node waveforms from oscillators with different speed.



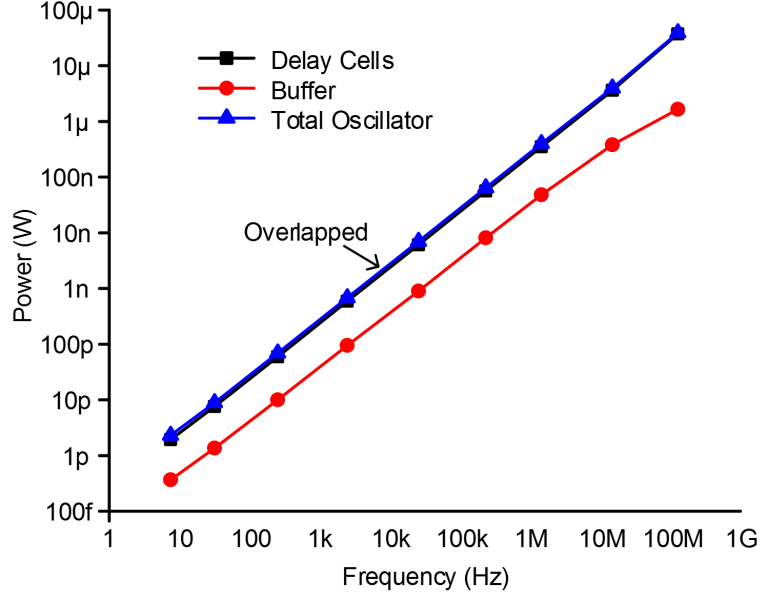


Figure 2.7: Simulated power consumption of a 7-stage proposed CEpCRO with an inverter output buffer over frequency.

Due to injected or ejected current, originally slow voltage transition is accelerated according to control voltage such as  $V_{BIASP}$  and  $V_{BIASN}$ . Fig. 2.6 (c) shows circuit status of each phase that corresponds to one of the leakage-based oscillator (Fig. 2.4 (d)). Supplemented current paths through additional transistors increase discharging current in phase A and charging current in phase C. They are changed from  $I_{LEAK3}$  and  $I_{LEAK2}$  to  $I_{LEAK3}+I(V_{BIASN})$  and  $I_{LEAK2}+I(V_{BIASP})$ , respectively. In phase B and D, outputs are shorted to ground or supply voltage by switches as in the leakage-based oscillator, and the oscillator swiftly escapes energy-inefficient voltage range which is above  $V_{THN}$  and below  $V_{THP}$ . Thus, this proposed oscillator still holds an important advantage of the leakage-based oscillator. Fig. 2.7 shows simulated power consumption of the proposed CEpCRO over frequency, which demonstrates its power scalability to frequency.

As an example, Fig. 2.6 (d) shows two oscillators with  $2\times$  frequency difference. Their charging/discharging slope of internal voltage is different due to leakage plus voltage-controlled current in voltage range below  $V_{THN}$  or above  $V_{THP}$ .

From the simplified model, overall period for the N-stage oscillator and time for each phase

can be calculated as follows:

$$T_{Period} = 2NC_L V_{TH} / (I_{LEAK} + I_{BIAS}), \quad (2.9)$$

$$T_A = T_C = C_L V_{TH} / (I_{LEAK} + I_{BIAS}), \quad (2.10)$$

$$T_B = T_D = (N - 1)C_L V_{TH} / (I_{LEAK} + I_{BIAS}), \quad (2.11)$$

where  $V_{TH} = V_{THN} = V_{THP}$ ,  $I_{BIAS} = I(V_{BIASN}) = I(V_{BIASP})$ ,  $I_{LEAK} = I_{LEAK2} = I_{LEAK3}$  &  $I_{LEAK1} = I_{LEAK4} = 0$  in phase A & C, and

$$\begin{aligned} C_L = & C_{db,M1A} + C_{gs,M1A} + C_{db,MCPA} + C_{sb,MCPA} + C_{sb,M2A} + C_{db,M2A} + C_{gs,M2B} \\ & + C_{sb,M3A} + C_{db,M3A} + C_{gs,M3B} + C_{db,MCNA} + C_{sb,MCNA} + C_{db,M4A} + C_{gs,M4A}, \end{aligned} \quad (2.12)$$

where it is assumed that parasitic capacitance in delay cells are symmetrical. Including an inverter buffer, energy-per-cycle for this oscillator can be expressed as:

$$E_{pC} = 2(NC_L + C_{BUF})V_{DD}^2 + (N + 1)I_{LEAK}V_{DD}T_{Period}, \quad (2.13)$$

where  $I_{LEAK} = I_{LEAK3}$ (phase A) =  $I_{LEAK1}$ (phase B) =  $I_{LEAK2}$ (phase C) =  $I_{LEAK4}$ (phase D). Here, it is assumed that power consumption due to short-circuit current is negligible since internal signals of the oscillator rapidly moves between short-circuit-current-free voltage region. Therefore, circuits using this oscillator are able to maintain energy-per-cycle.

Since  $V_{DS} \gg V_T$ ,  $I_{LEAK}$  in phase A and C can be expressed as:

$$I_{LEAK} = \mu C_{OX} \frac{W}{L} (m - 1) V_T^2 e^{-\frac{V_{TH}}{mV_T}}. \quad (2.14)$$

The current control transistors obtain required  $I_{BIAS}$  by adjusting  $V_{BIASN}$  or  $V_{BIASP}$ , which enables output clock to cover wide frequency range. By assuming the transistors operating in saturation region, the maximum and minimum of  $I_{BIAS}$  can be expressed as:

$$Max.I_{BIAS} = \frac{1}{2} \mu C_{OX} \frac{W}{L} (V_{DD} - V_{TH})^2. \quad (2.15)$$

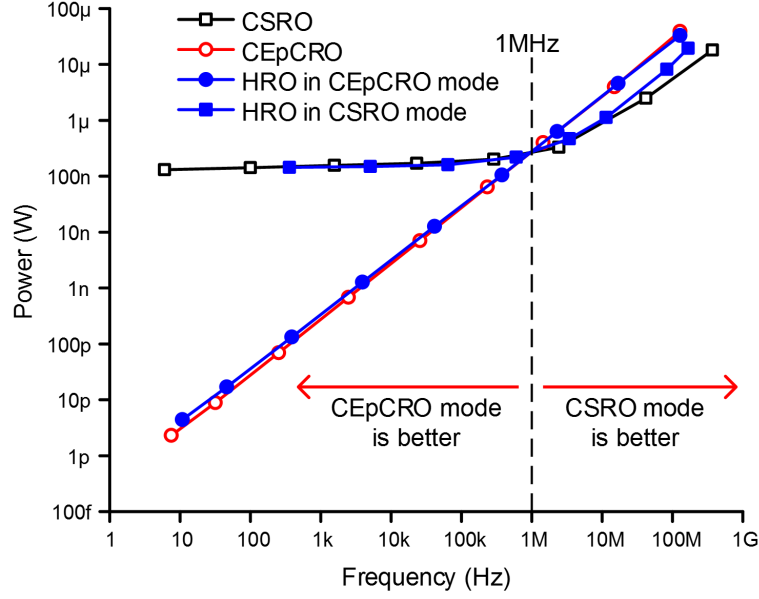


Figure 2.8: Simulated power consumption of CSRO, CEpCRO, and HRO over frequency.

$$\text{Min. } I_{BIAS} = I_{LEAK}. \quad (2.16)$$

From equation (16) and (17), the maximum and minimum frequency can be obtained as:

$$f_{MAX} = \frac{\mu C_{OX} \frac{W}{L} (V_{DD} - V_{TH})^2}{4NC_L V_{TH}} \quad (2.17)$$

$$f_{MIN} = \frac{\mu C_{OX} \frac{W}{L} (m-1) V_T^2 e^{-\frac{V_{TH}}{mV_T}}}{NC_L V_{TH}} \quad (2.18)$$

Here,  $\text{Max. } I_{BIAS} \gg I_{LEAK}$ .

### 2.3.3 Proposed Hybrid Ring Oscillator (HRO)

CEpCRO achieves power consumption which scales with frequency. As shown in equation 2.1 and 2.13, however, load capacitance is increased with additional transistors. Fig. 2.8 shows simulated power consumptions of oscillators. Power of CEpCRO is higher than CSRO above 1 MHz where dynamic power is larger than constant power at a buffer due to short-circuit current.

To combine the advantages from both oscillators, we also propose a hybrid oscillator (HRO) that becomes one of the two oscillator topology by changing switch configuration. Fig. 2.9 (a)

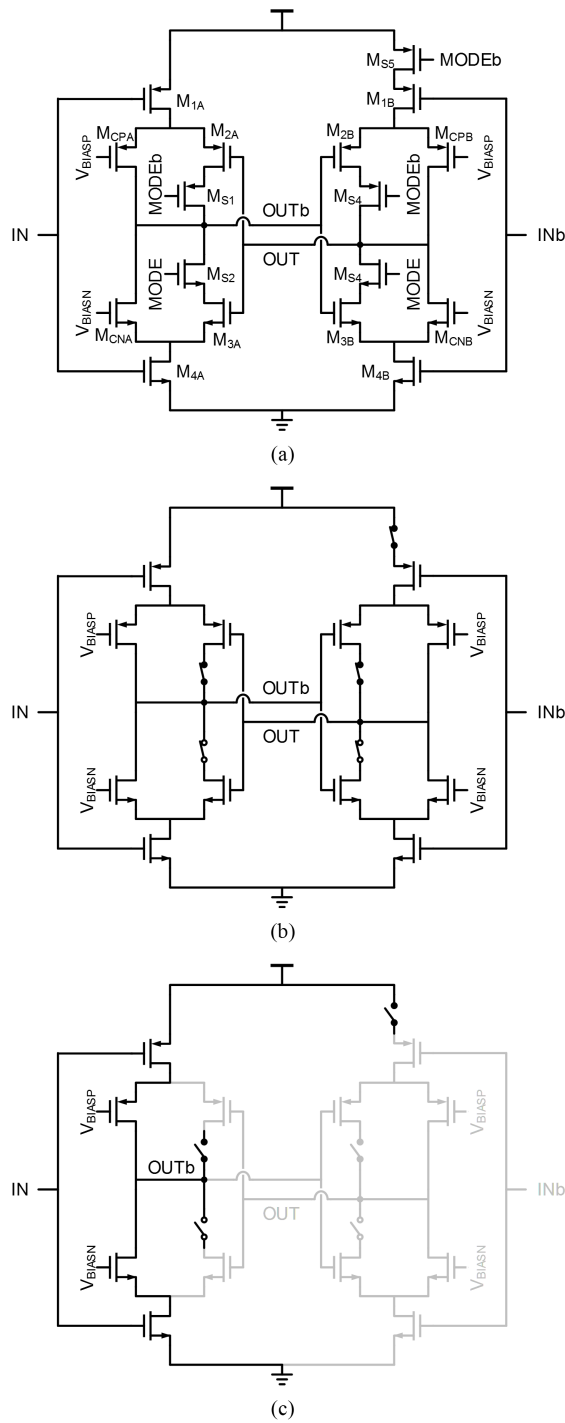


Figure 2.9: Proposed hybrid ring oscillator (HRO) (a) circuit diagram of a delay cell (b) CEpCRO mode (c) CSRO mode.

shows a delay cell for HRO. Five more transistors ( $M_{S1} \sim M_{S5}$ ) are added to CEpCRO. By connecting all the switches in CEpCRO mode (Fig. 2.9 (b)), this oscillator becomes the same as CEpCRO. In contrast, by disconnecting switches in CSRO mode (Fig. 2.9 (c)), the circuit operates like CSRO. Half a delay cell is disabled by power gating switch ( $M_{S5}$ ), and back-to-back inverters are disassembled by disconnecting  $M_{S1}$  and  $M_{S2}$ . Remained active part is input and current control transistors just as CSRO.

Load capacitance  $C_L$  in each mode is as follows: In CSRO mode,

$$\begin{aligned}
C_{L,CSRO_{MODE}} = & C_{db,M1A} + C_{gs,M1A} + C_{db,MCPA} + C_{sb,MCPA} + C_{sb,M2A} \\
& + C_{gs,M2B} + C_{db,MS1} + C_{sb,MS1} + C_{db,MS2} + C_{sb,MS2} \\
& + C_{sb,M3A} + C_{gs,M3B} + C_{db,MCNA} + C_{sb,MCNA} + C_{db,M4A} + C_{gs,M4A}.
\end{aligned} \tag{2.19}$$

In CEpCRO mode,

$$C_{L,CEpCRO_{MODE}} = C_{L,CSRO_{MODE}} + C_{db,M2A} + C_{sb,MS1} + C_{sb,MS2} + C_{db,M3A}. \tag{2.20}$$

CEpCRO needs to switch two  $C_L$  in equation (12) in a delay cell for differential configuration, but HRO requires to charge/discharge only one  $C_{L,CSRO_{MODE}}$  (equation ??) in CSRO mode for single-ended scheme. Due to less switching capacitance from disabled transistors, as shown in Fig. 2.8, HRO in CSRO mode is more efficient than CEpCRO above 1 MHz where the impact of short-circuit current is not significant.

Above 1 MHz, HRO has higher efficiency in CSRO mode than CEpCRO mode. By switching mode at 1 MHz, HRO modify its circuit for better efficiency between CSRO and CEpCRO over wide frequency range. HRO can be used in the application where pre-characterization is allowed, which tells the best frequency to change mode.

### 2.3.4 Bias Voltage Generator

In the proposed oscillators, bias voltage needs to be given in order to control voltage-controlled current. Fig. 2.10 shows two bias voltage generators such as voltage-divider-based and current-mirror-based circuits. To obtain power consumption proportional to frequency even at slow fre-

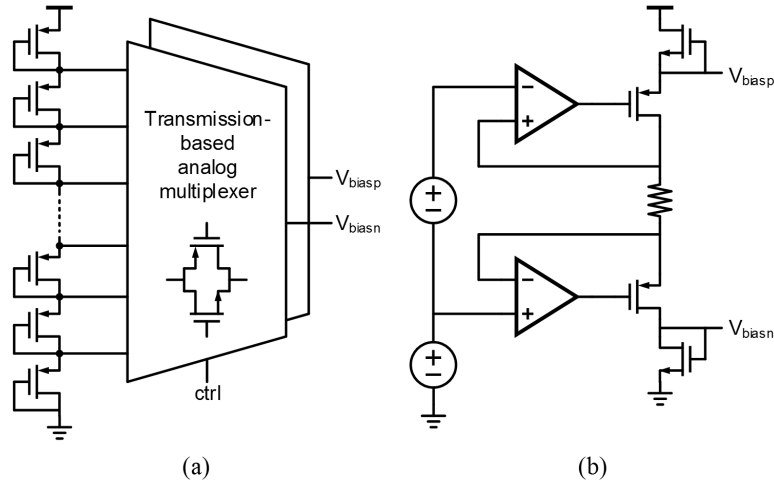


Figure 2.10: Bias voltage generator (a) voltage-divider-based circuit followed by analog mux (b) current-mirror-based circuit.

quency, the bias voltage generator should also be designed as low power as the oscillator itself.

As shown in Fig. 2.10 (a), stacked diode-connected transistors offer different voltages. One of taps is connected to gates of the current control transistors through a transmission-gate-based multiplexer. Fine voltage steps are required under threshold voltage of a transistor since current and frequency significantly change in subthreshold region.

The bias voltage can also be set using a current source and a current mirror as shown in Fig. 2.10 (b). It provides with robust bias voltage against process variation since current from the current source directly decide charging/discharging current. A current source in [12] consumes 5 nW. It forces 10 mV to an on-chip 2.5 M $\Omega$  resistor to generate 4 nA current. Bias voltage can be adjusted with copy ratio of the current mirror and resistance value in the current source. Power-scalable oscillator can be designed with this circuit to tune output frequency where the 4 nA current source does not dominate oscillator power consumption.

## 2.4 Measurement Results

The prototype oscillators were fabricated in a 0.18  $\mu\text{m}$  CMOS technology, including 7-stage conventional (CSRO) and proposed ring oscillators (CEpCRO and HRO) with inverter buffers for comparison as shown in Fig. 2.11. A diode stack with PMOS transistors and a 64-input analog multiplexer using transmission gates are implemented to provide with bias voltages for oscillators.

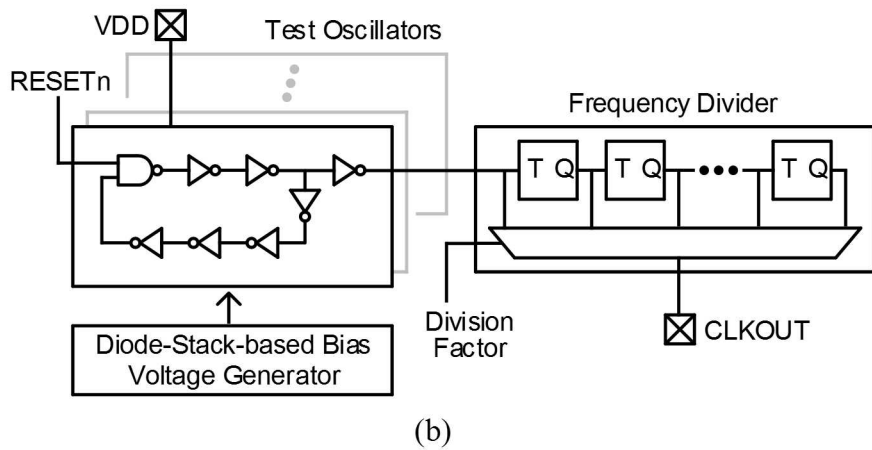
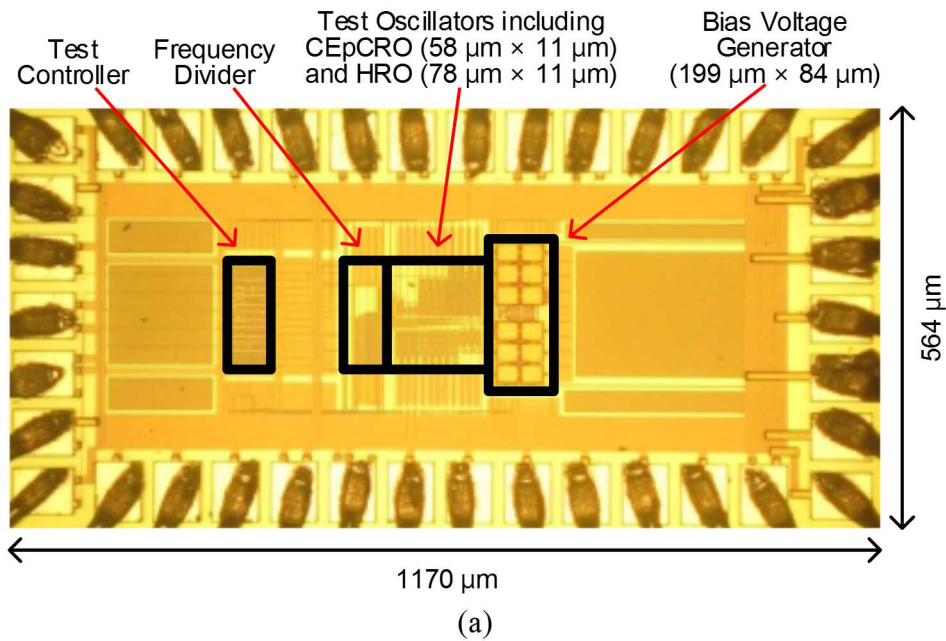


Figure 2.11: Test chip for oscillators (a) die photograph (b) test structure.

Outputs of the oscillators are connected to a frequency divider. With its division factor, oscillator frequency is controlled to be observed through a pad.

Fig. 2.12 shows measured power and energy-per-cycle of CSRO and CEpCRO. In Fig. 2.12 (a), CEpCRO shows linearly scaled power consumption from 1.2 Hz to 60 MHz ( $f_{MAX}/f_{MIN} = 5 \times 10^7$ ). However, power consumption of CSRO is limited to 144 nW due to short-circuit current through a buffer. It results in worse energy-per-cycle for lower frequency as shown in Fig. 2.12 (b). Instead, CEpCRO has constant energy-per-cycle of 8 pJ/cycle from 21 Hz to 60 MHz, which is enabled by rapid escape from voltage region triggering short-circuit current. Below 300 kHz, CEpCRO requires less energy-per-cycle than CSRO since large short-circuit current in CSRO becomes a dominant factor compared to dynamic energy.

Fig. 2.13 shows measured bias voltage profile of CEpCRO for wide frequency generation. Most of frequency range is covered under threshold voltage (0.7 V) of transistors controlling charging/discharging current. High drain current sensitivity on gate voltage in subthreshold region results in  $(1.14 \times 10^5) \times \text{Hz/V}$  of frequency sensitivity on gate voltage from 21 Hz to 1.2 MHz. Thus, this range should be well covered with fine steps in bias voltage generator.

Fig. 2.14 shows measured maximum and minimum oscillator frequency over supply voltage. CEpCRO operates down to 0.3 V while the maximum supply voltage is limited by process. The maximum frequency less sensitive than the minimum frequency since transistors work in strong-inversion region for supply voltage higher than  $V_{TH}$ . Frequency range increases from  $101.5 \times$  to  $107.8 \times$  over 0.3 V  $\sim$  1.8 V, and it is saturated with supply voltage higher than 1.8 V.

Fig. 2.15 shows measured power and energy-per-cycle of HRO with different mode. Similar to CEpCRO, HRO in CEpCRO mode has maintained energy-per-cycle (1.2  $\sim$  7.1 pJ/cycle) over 35 Hz  $\sim$  51 MHz. In CSRO mode, although power is limited to 131 nW below 53 kHz as CSRO, HRO has more efficient than CEpCRO mode above 200 kHz. Hence, mode in HRO is switched at 200 kHz as optimized control to achieve lower energy-per-cycle.

Fig. 2.16 shows energy-per-cycle of CSRO, CEpCRO, and optimized HRO. Below 80 kHz, HRO has higher energy-per-cycle than CEpCRO up to 38 % (180 Hz). It came from increased switching capacitance from additional transistors for mode change. Above 80 kHz, HRO achieves lower energy-per-cycle up to 56 % (7 MHz) than CEpCRO. It is enabled by disabling more than a half of circuits in delay cells to reducing switching capacitance. However, although HRO sim-



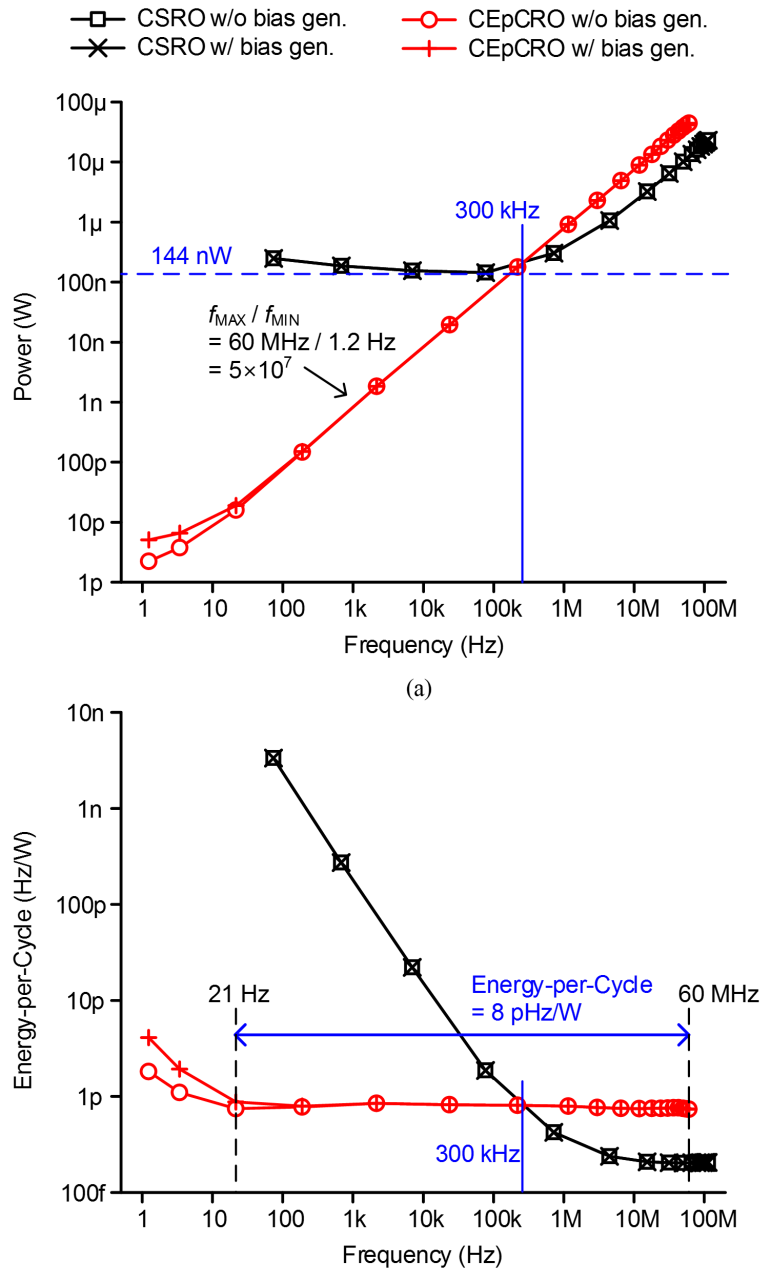


Figure 2.12: Measured power and energy-per-cycle of CSRO and CEpCRO (a) power (b) energy-per-cycle.

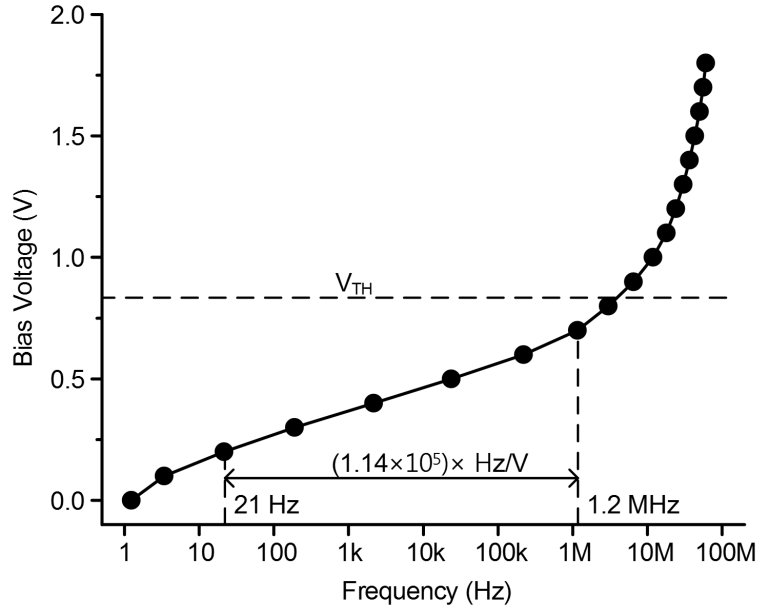


Figure 2.13: Measured bias voltage profile of CEpCRO over frequency.

ilarly operates as CSRO, it is still less efficient than CSRO at the high frequency since HRO has additional capacitance to change mode.

Table 2.1 shows performance summary of the proposed oscillators and prior wide-range-frequency ring oscillators. CEpCRO shows the widest range of frequency with [24], but power at slowest frequency is not reported. Although [30] and [31] show good performance on energy-per-cycle, their frequency range is not wide as much as CEpCRO and HRO in this work, and also their work are not verified in silicon. CEpCRO and HRO demonstrate good energy-per-cycle over wide frequency range, which allows circuits in a wireless sensor node to operate with higher efficiency. An example will be shown in the following section.

## 2.5 Application Example

The proposed CEpCRO was implemented to operate a capacitive step-down converter and were fabricated in a  $0.18 \mu\text{m}$  CMOS technology as shown in Fig. 2.17 (a). A 6:1 step-down converter is designed to deliver power from a Li thin-film battery ( $\sim 3.8 \text{ V}$ ) to digital system such as a processor and a memory ( $0.6 \text{ V}$ ) for a low-power wireless sensor node.

Fig. 2.17 (b) shows the block diagram of a converter including CEpCRO. Multiple-size switches

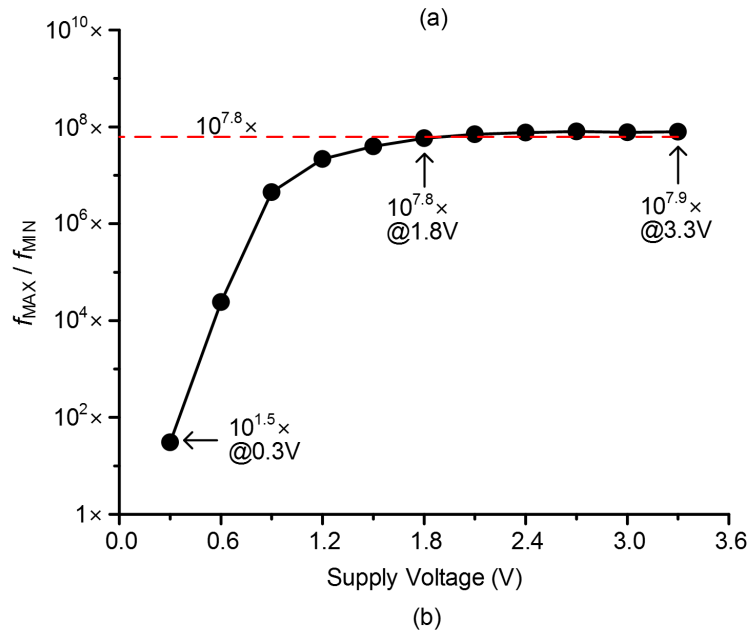
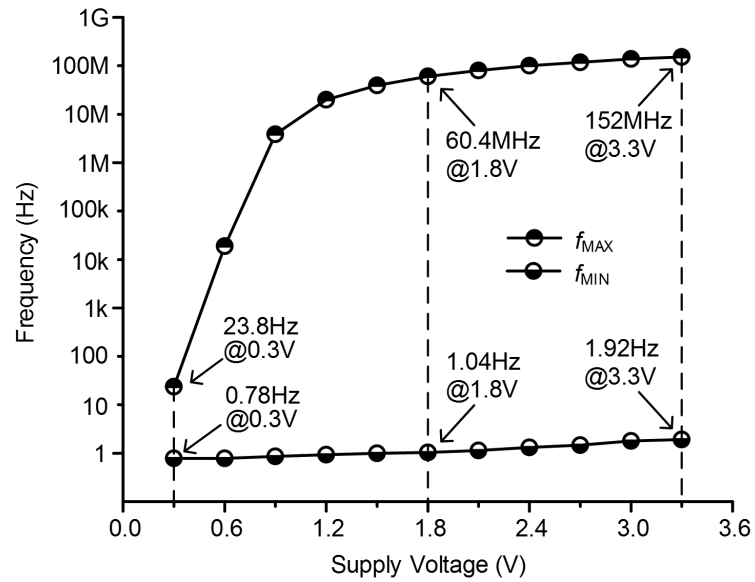
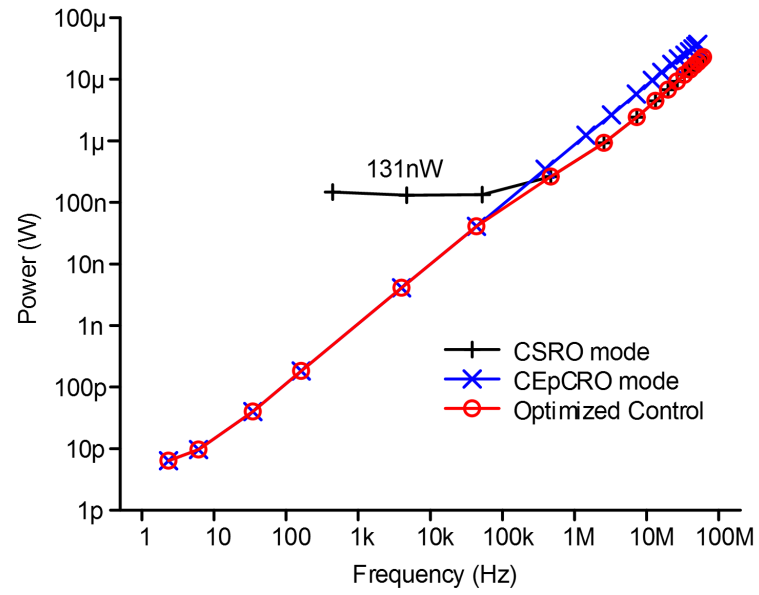


Figure 2.14: Measured frequency range of CEpCRO over supply voltage (a)  $f_{MAX}$  and  $f_{MIN}$  (b)  $f_{MAX}/f_{MIN}$ .



(a)

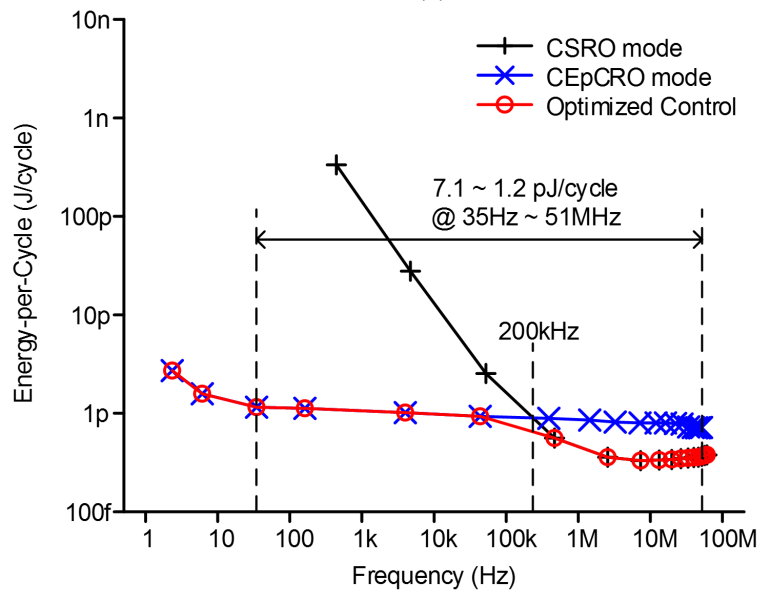


Figure 2.15: Measured performance of HRO over frequency (a) power (b) energy-per-cycle.

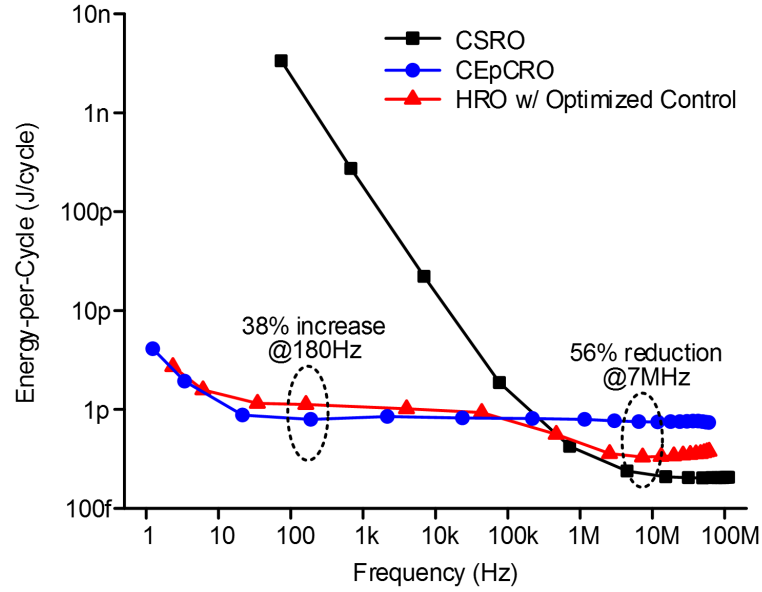


Figure 2.16: Measured energy-per-cycle of CSRO, CEpCRO, and HRO

Table 2.1: Performance summary of the proposed oscillator and comparison to other prior works

	This Work		CSRO	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]
	CEpCRO	HRO									
Process (nm)	180		350	350	180	800	180	600	180	130	
VDD (V)	1.8		3.3	3.3	2	5	3.3	3.0	1.8	1.2	
$f_{MAX}$ (Hz)	60 M	61 M	113 M	256 M	1.1 G	807 M	407 M	368.9 M	366 M	6.9 G	10 M
$f_{MIN}$ (Hz)	1.2	2.3	74	4.8	4 k	20 M	13	40	40	75 M	1.75 k
$\log(f_{MAX}/f_{MIN})$	7.7	7.4	6.2	7.7	5.4	1.6	7.5	7.0	7.0	2.0	3.8
Power @ $f_{MAX}$ (W)	44 $\mu$	23 $\mu$	23 $\mu$	1.76 m	N/A	N/A	29.2 m	30.05 m	70 $\mu$	9.32 m	3.6 $\mu$
Power @ $f_{MIN}$ (W)	5.1 p	6.4 p	247 n	N/A	N/A	N/A	N/A	N/A	70 $\mu$	70 $\mu$	1 n
Energy-per-Cycle @ $f_{MAX}$ (J/cycle)	0.73 p	0.38 p	0.20 p	6.88 p	N/A	N/A	71.7 p	81.5 p	0.19 p	1.35 p	0.36 p
Energy-per-Cycle @ $f_{MIN}$ (J/cycle)	4.25 p	2.78 p	3.34 n	N/A	N/A	N/A	N/A	N/A	1.75 $\mu$	0.93 p	0.57 p
Comments	Silicon Measurement						Spice Simulation				

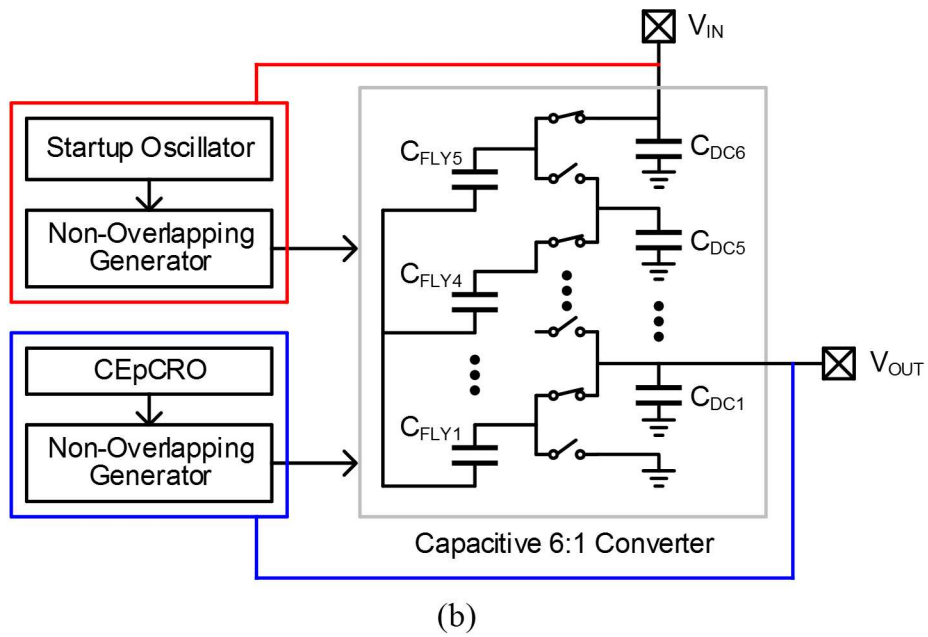
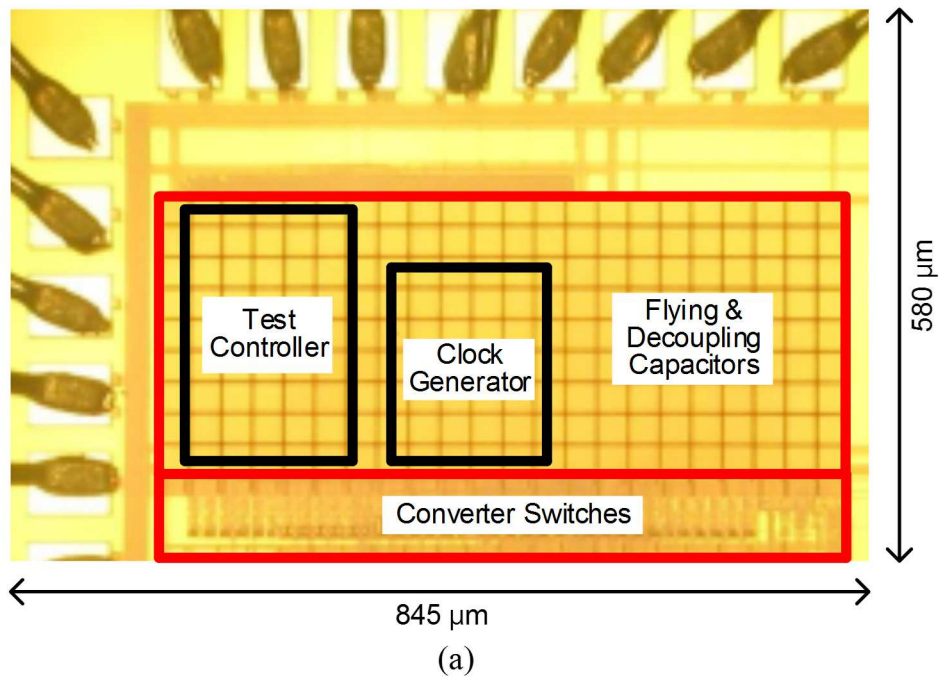


Figure 2.17: Test chip for a capacitive step-down converter (a) die photograph (b) converter diagram

are implemented to support wide range of switching frequency. It helps to cover wide range of load power for different mode of wireless sensor nodes (e.g. standby and active mode) with high efficiency.

In trade-off between switching power of the converter and driving strength, gate driving voltage is set to one third of input voltage ( $V_{IN}$ ). Converter switch drivers and CEpCRO operate under the same supply voltage, which is one tap of the converter ( $V_{OUT}$ ). Thus, the converter can operate by itself after it starts delivering power with a help of a startup oscillator that runs directly from the battery. Clock signals from CEpCRO are properly shifted for converter switches in different voltage levels by level-shifting gate drivers [35].

Fig. 2.18 shows measured input power, converter efficiency, and clock frequency over load power. The converter can support wide range of load power from 583 pW to 26  $\mu$ W and obtains the peak converter efficiency of 54 %. As shown in Fig. 18 (b), operating clock frequency is proportional to load power. Load power range of  $4.5 \cdot 10^4 \times$  can be achieved with frequency range of  $1.4 \cdot 10^4 \times$  from CEpCRO. As load power decreases, the converter requires to transfer less charge through switched capacitor network. Hence, switching speed can be slower, leading to lower input power with less switching and oscillator power. However, this is only true when oscillator power is scaled with frequency.

Fig. 2.19 shows measured power from CSRO and CEpCRO at oscillator supply voltage in this converter ( $\sim 1.2$  V). Since supply voltage is smaller than the sum of  $V_{TH}$  of NMOS and PMOS transistor, power of CSRO is limited at lower power (1 nW at 10 Hz) compared to one at 1.8 V supply voltage (144 nW). However, it still shows the impact of short-circuit current, which results in increasing energy-per-cycle at slow frequency.

Fig. 2.20 shows efficiency of converters using CSRO and CEpCRO. Efficiency for the converter using CSRO is calculated based on the measurement results in Fig. 2.20. Below 5.7 nW of load power, the converter with CEpCRO becomes more efficient than one with CSRO since power of CEpCRO scales to frequency. Converter efficiency in the converter with CEpCRO can be improved by 56 % for 583 pW load power compared to one with CSRO.

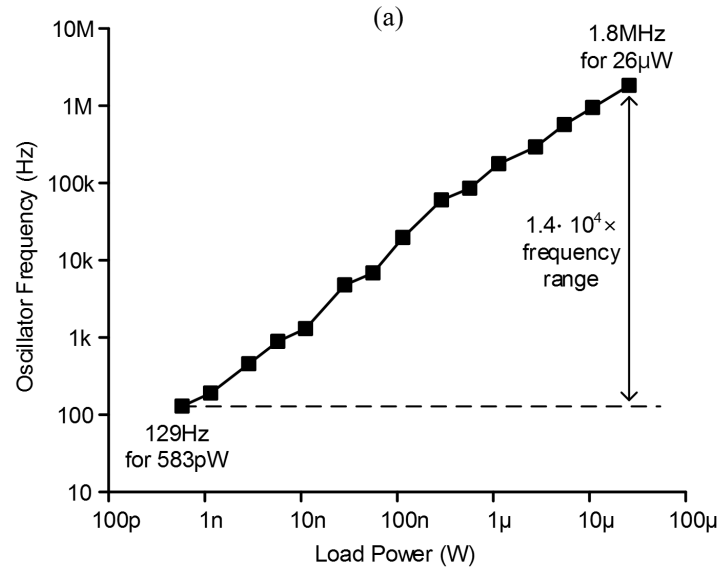
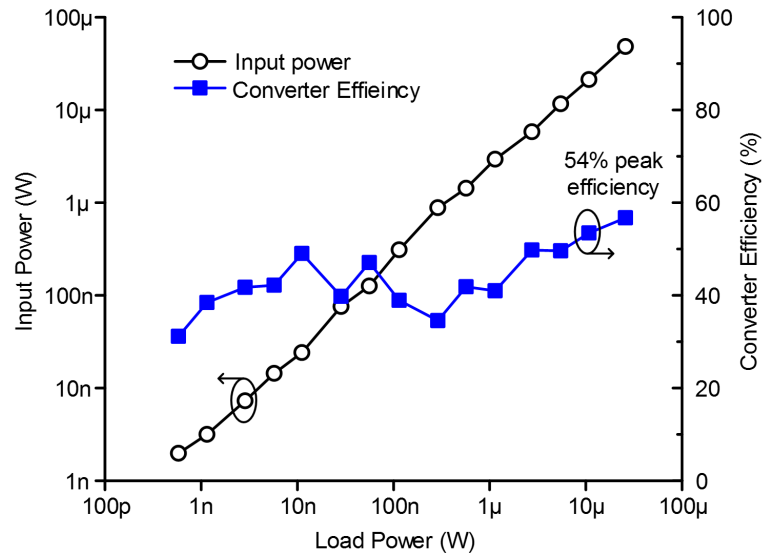


Figure 2.18: Measured converter over load power (a) input power and converter efficiency (b) operating frequency.



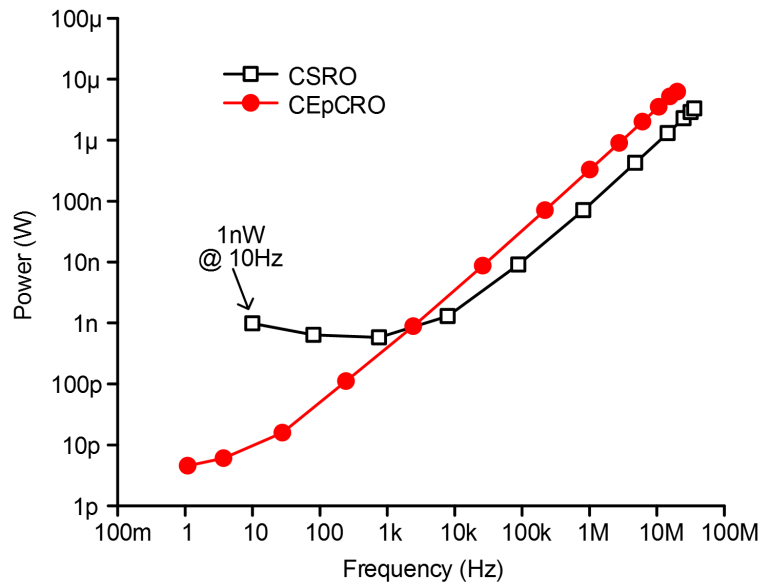


Figure 2.19: Measured power consumption of oscillators at oscillator supply voltage in the converter.

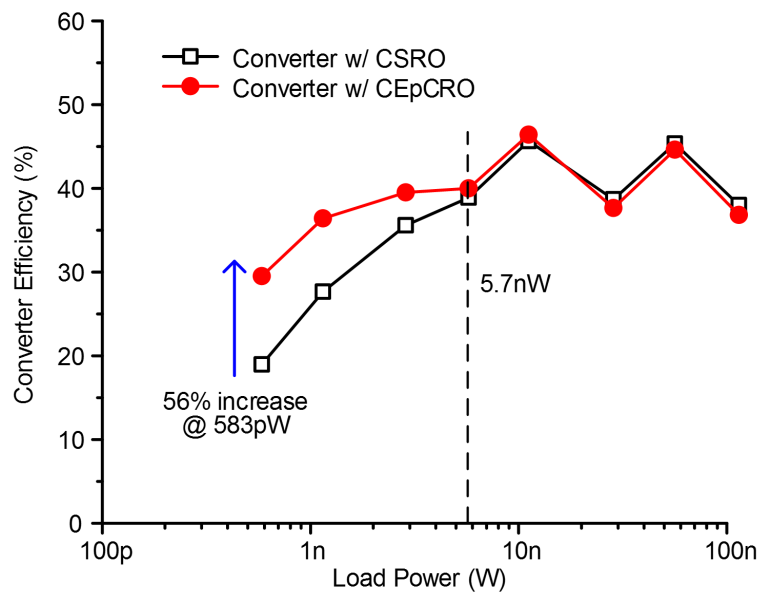


Figure 2.20: Efficiency of converters using CSRO and CEpCRO.

## 2.6 Summary

This work demonstrates energy-efficient oscillators for wireless sensor node applications. From the prototype chip, the proposed constant energy-per-cycle ring oscillator (CEpCRO) achieves constant 0.8 J/cycle over 21 Hz  $\sim$  60 MHz at 1.8 V supply voltage, which is lower energy efficiency than the conventional current-starved oscillator (CSRO) below 300 kHz. Also, another proposed hybrid oscillator (HRO) obtains higher energy efficiency above 80 kHz than CEpCRO by disabling more than a half circuits to reduce switching capacitance. This improved energy efficiency is enabled by rapid escape from voltage region causing short-circuit current and charging/discharging output capacitance over the other voltage region for delay generation. Also, current feeding scheme with gate voltage control offers wide frequency range of 1.2 Hz  $\sim$  60 MHz without efficiency loss. The proposed CEpCRO was implemented in a capacitive step-down converter, as an example of circuits in wireless sensor nodes. It improves converter efficiency by 56 % compared to a converter using CSRO for 583 pW load power.

## CHAPTER 3

### A Ripple Voltage Sensing MPPT Circuit

#### 3.1 Introduction

Miniature-scale systems, in general, are equipped with a harvesting unit (solar, thermal, etc) to recharge their battery. The small form factor of these sensors has led designers to opt for integrated switched capacitor boost converters (SCBCs) with a total capacitance in the range of 0.5 to 1.5 nF [9, 36]. Furthermore, the limited size of the harvesting unit makes efficient energy extraction from the energy source and up-conversion of the voltage a majority priority. However, the type of energy source and its operating point can vary greatly. For instance, in office lighting a 1 mm<sup>2</sup> solar cell reaches its optimal energy efficiency at  $\sim 250$  mV and produces 45 nA current. In sunlight, that same solar cell has optimal energy efficiency at  $\sim 350$  mV and produces 2  $\mu$ A. Clearly, the two conditions require vastly different capacitor switching frequencies, switch sizes, and voltage conversion ratios of the SCBC. A highly flexible SCBC is therefore needed that ideally performs maximum power point tracking (MPPT), allowing it to automatically search for and track the configuration that delivers maximum power to the battery.

In general, MPPT involves simultaneous measurement of both voltage and current delivered to the battery, which are multiplied and fed into a search algorithm. Given the small power budget of micro-sensors, the voltage/current measurement and search algorithm must be performed with minimum power overhead. A comprehensive MPPT method was proposed in [37] where the battery inflow current is measured (Fig. 3.1). While having the advantage of directly measuring energy delivered to the battery, it incurs a voltage drop over the current mirror transistor, resulting

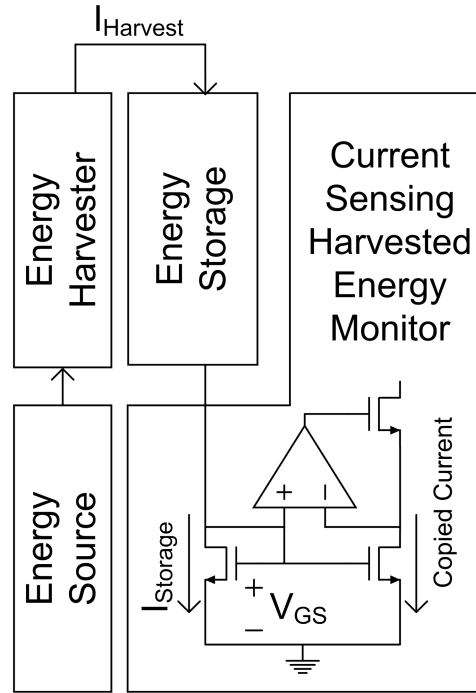


Figure 3.1: Conventional harvested energy monitor for maximum power point tracking (MPPT).

in significant energy loss. Furthermore, it requires a high bandwidth amplifier to track dynamic current influx.

This section demonstrates a MPPT circuit that takes advantage of the unique structure of SCBC - it places a small sampling capacitor in parallel with the flying or decoupling cap in the SCBC that eavesdrops on the voltage transfer that occurs in the voltage converter. By integrating the small voltage fluctuations using correlated double sampling (CDS), the power delivered to the battery can be determined. Since the sampling capacitor is  $64.8\times$  smaller in size than the flying cap, the impact on conversion efficiency is negligible. By directly tracking power delivered to the battery all parameters of the SCBC can be optimized, including switching frequency, switch size, and conversion ratio.

## 3.2 Ripple Voltage Sensing

Fig. 3.2 shows the circuit diagram of the proposed harvested energy monitor and its waveform. The SCBC has a ladder topology and its switches are driven by a set of non-overlapping clocks ( $\Phi_1$

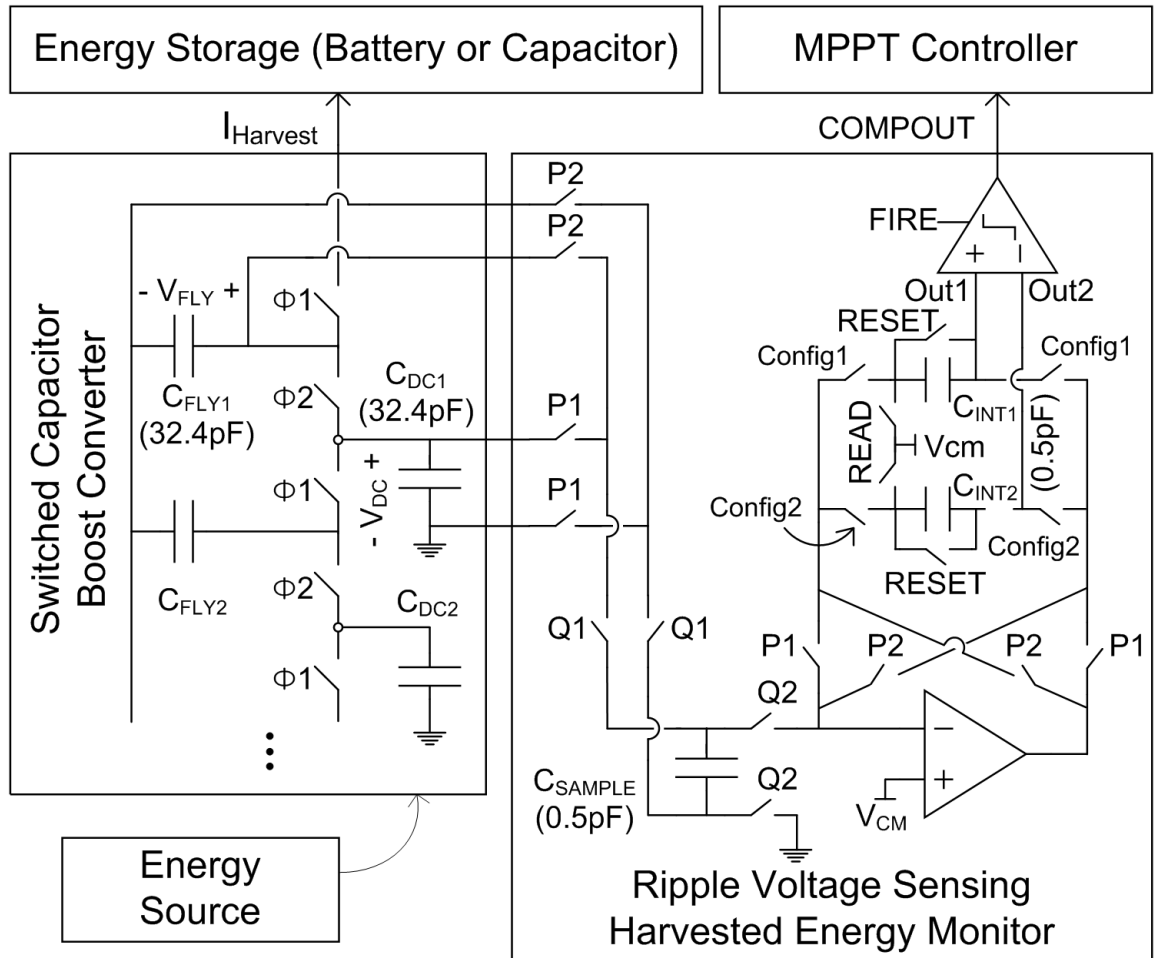


Figure 3.2: Proposed ripple voltage sensing harvested energy monitor.

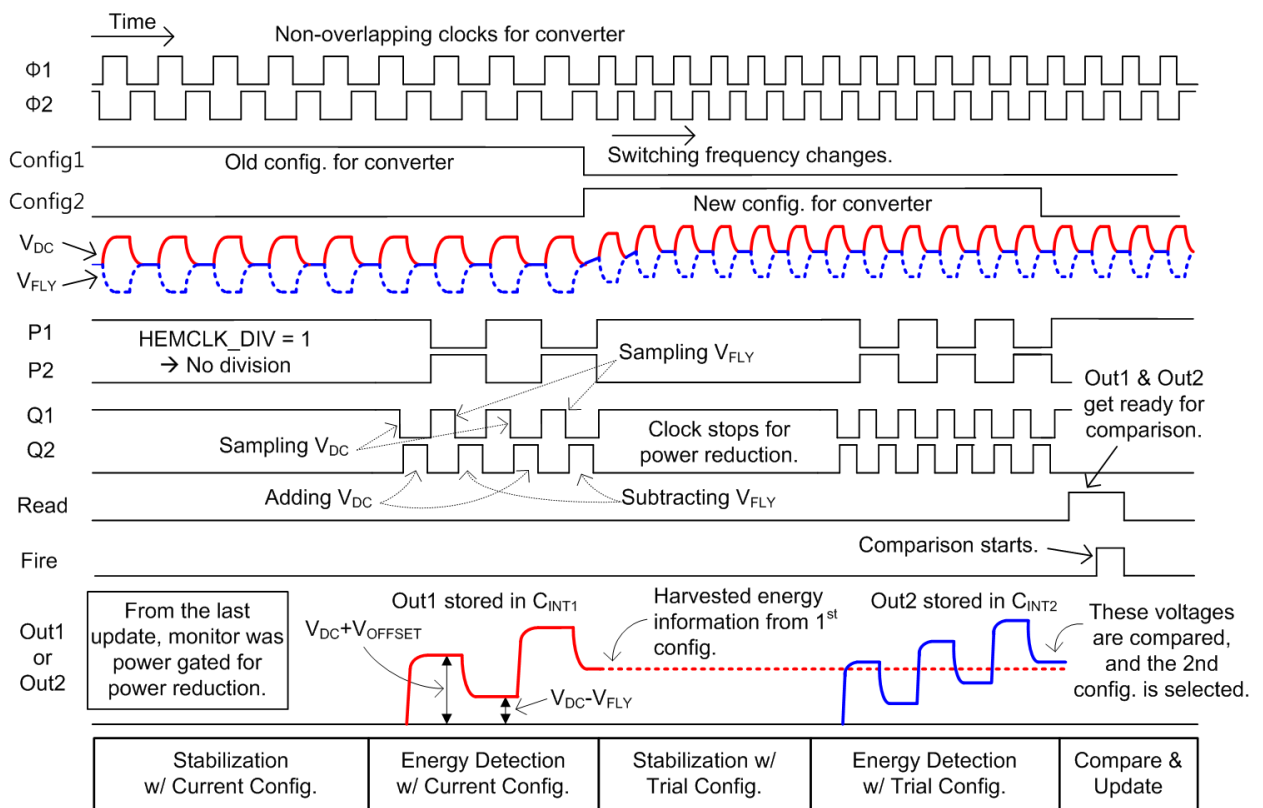


Figure 3.3: Waveform of ripple voltage sensing harvested energy monitor.

and  $\Phi_2$ ). This switching function transfers charge from the energy source to the battery, generating ripple voltages at SCBC internal nodes. In one phase ( $\Phi_1$ ), the flying capacitor of  $C_{FLY2}$  provides charge to the decoupling capacitor of  $C_{DC1}$  by charge sharing while the flying capacitor of  $C_{FLY1}$  transfers charge to and recharges the battery. Thus, voltage across  $C_{DC1}$  ( $V_{DC}$ ) increases while voltage across  $C_{FLY1}$  ( $V_{FLY}$ ) decreases when energy is harvested. In the other phase ( $\Phi_2$ ), charge moves from  $C_{DC1}$  to  $C_{FLY1}$  due to  $V_{DC} > V_{FLY}$  and  $V_{DC}$  decreases while  $V_{FLY}$  increases (Fig. 3.3). This voltages difference ( $V_{DC} - V_{FLY}$ ) is proportional to the amount of charge sent to the battery in a switching period. Hence, integrating the ripple voltages' difference for a fixed time provides a measure of harvested energy.

We implement the proposed ripple voltage sensing circuit using a small sampling capacitor ( $C_{SAMPLE}$ ) that is placed in parallel with  $C_{FLY1}$ , a correlated double sampling integrator, two integration capacitors ( $C_{INT1}$  and  $C_{INT2}$ ), and a clocked comparator. To sample  $V_{DC}$  and  $V_{FLY}$ ,  $C_{SAMPLE}$  is alternatively connected in parallel to  $C_{DC1}$  or  $C_{FLY1}$ . Its sampling frequency is divided down to  $\sim 1$  kHz from  $\Phi_1$  to relieve the bandwidth requirement of the integrator and hence its power consumption. The small size of  $C_{SAMPLE}$ , along with the fact it is decoupled from the SCBC only once in 138 cycles, results in negligible energy impact on SCBC ( $< 0.91$  % efficiency degradation, measurement-based calculation including phase drivers).

One challenge in measuring energy transfer in the proposed method is the small magnitude of the ripple, which is a requirement in high efficiency voltage conversion. As a result, the integrator's output voltage can easily saturate due to accumulation of the amplifier's offset or low frequency noise over multiple integration cycles. To address this, we use CDS to integrate the differences of  $V_{FLY}$  and  $V_{DC}$  ripple and amplify it sufficiently for use in the comparator. CDS is achieved by changing the polarity of  $C_{INT1}$  and  $C_{INT2}$  with P1 and P2. The energy transfer is calculated for two configurations successively and stored on  $C_{INT1}$  and  $C_{INT2}$ . These two capacitor voltages are then compared (READ and FIRE) to determine the optimal energy transfer configuration and the SCBC parameters are updated accordingly.

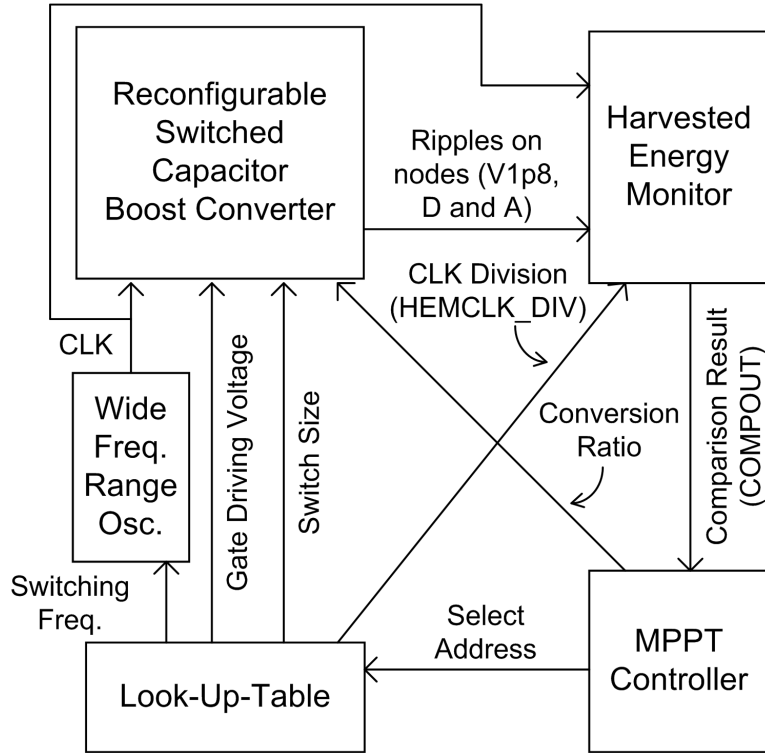


Figure 3.4: Block diagram of the designed energy harvesting unit.

### 3.3 Energy Harvester Using Ripple Voltage Sensing MPPT

The complete energy harvesting unit consists of a reconfigurable SCBC, harvested energy monitor, MPPT controller, look-up table, and a wide frequency range oscillator (Fig. 3.4). The MPPT controller can adjust four SCBC parameters through the look-up table: conversion ratio, switching frequency, switch size, and gate driving voltage. Mapping of switching frequency, switch size, and gate driving voltage is done in the programmable look-up table. This allows inefficient or non-functional parameter combinations to be excluded from the search. The look-up table also sends the clock division ratio (HEMCLK\_DIV) to the harvested energy monitor to set the integrator frequency.

The designed SCBC connects a successive approximation (SA) DC-DC converter [18] in series with a 1:6 converter (3.5). Each switch has transistor size controllability (1 to 63) to optimize switching loss and conduction loss for different switching frequencies. The smallest switches have separate smaller flying capacitors while larger switches share larger ones since the SCBC does not require large switches for slow switching frequency, while capacitance from large switches



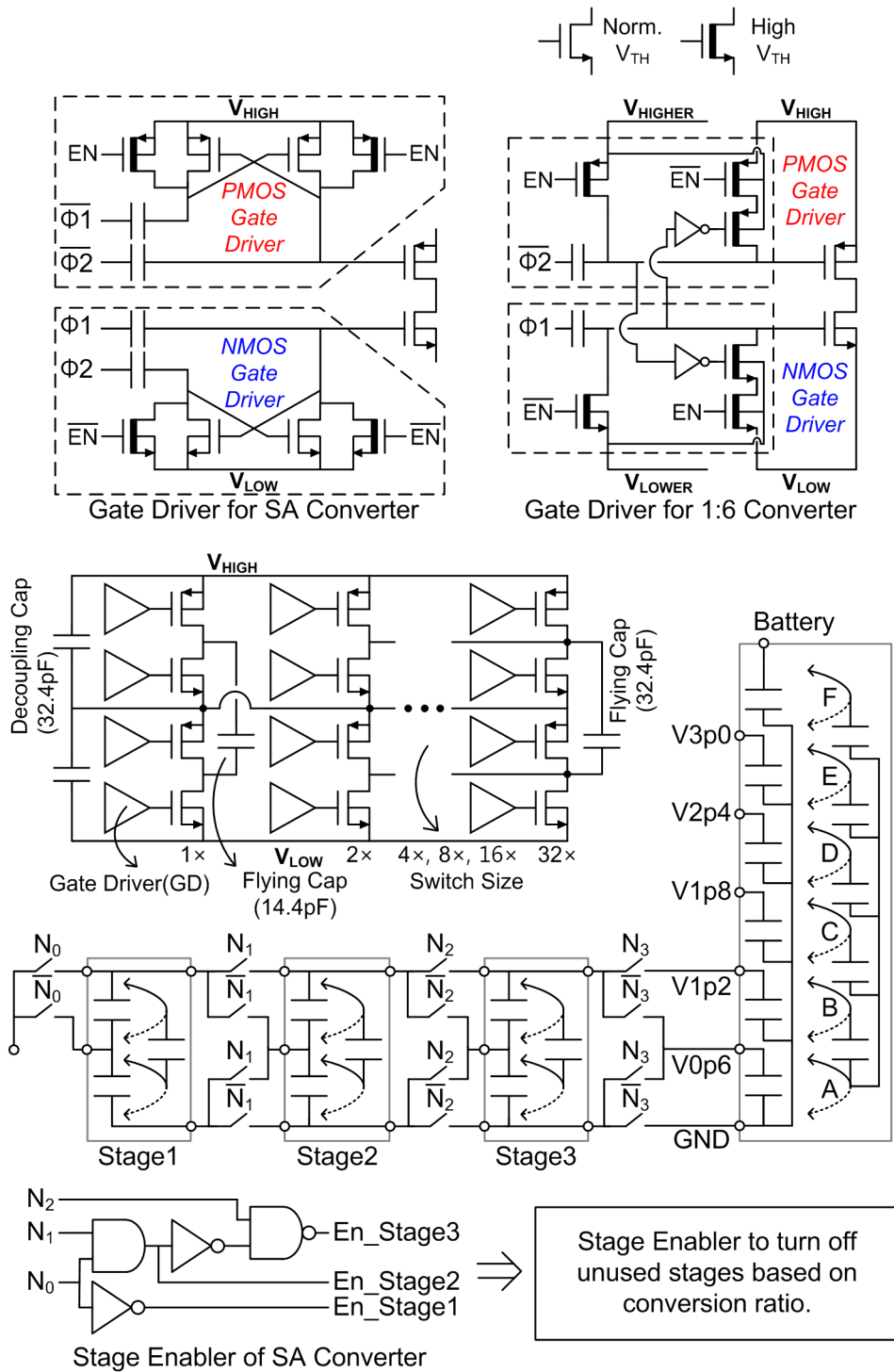


Figure 3.5: Reconfigurable switched capacitor boot converter.

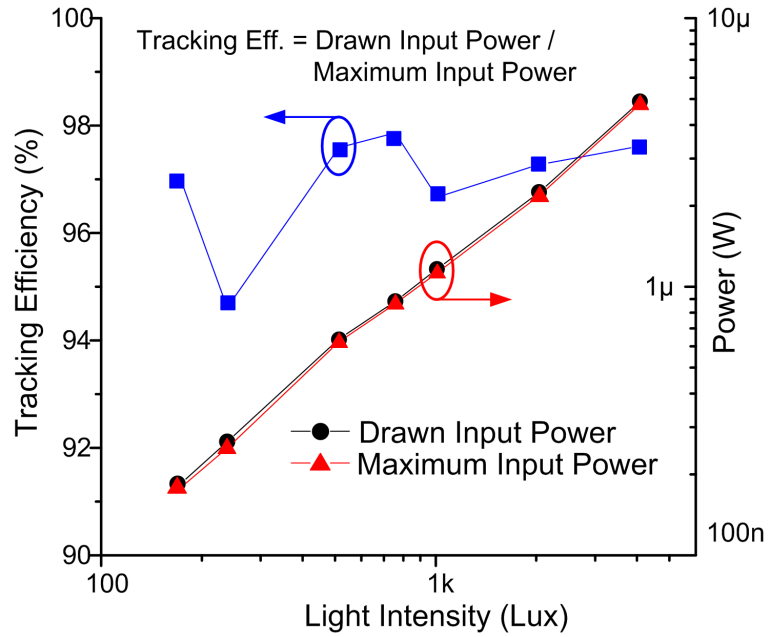


Figure 3.6: Tracking efficiency over light intensity.

deteriorate its efficiency [38]. AC coupling gate drivers enable the modulation of gate driving voltage by only changing the amplitude of  $\Phi_1$  and  $\Phi_2$ . They level shift  $\Phi_1$  and  $\Phi_2$  to the proper voltages based on switch source voltages, which is stabilized by decoupling capacitors. Compared to the conventional AC coupling gate drivers for the SA converter, new gate drivers are proposed for the 1:6 converter because of its single-phase topology and the fixed 0.6 V between  $V_{HIGH}$  and  $V_{LOW}$ . This design requires only half the capacitors by reusing signals from the complementary type of gate driver in order to short gate and source of switch transistors to prevent DC drift. Also, devices connected to  $V_{HIGHER}$  and  $V_{LOWER}$  help reduce leakage via super cut-off when the switches are disabled.

### 3.4 Measurement Results

Fig. 3.6 shows that the fine resolution of conversion ratio enables  $>94.6\%$  tracking efficiency across 170-to-4100 incident lux despite inherent limitations of SCBCs compared to inductive boost converters. The designed MPPT circuit consumes 35 nW (avg. over light intensity) and achieves a power overhead of 5 %, even at low harvested currents of 1.4  $\mu$ A (Fig. 3.7). Fig. 3.8 and Fig. 3.9 show example MPPT operation including changing conversion ratios and switch sizes. From

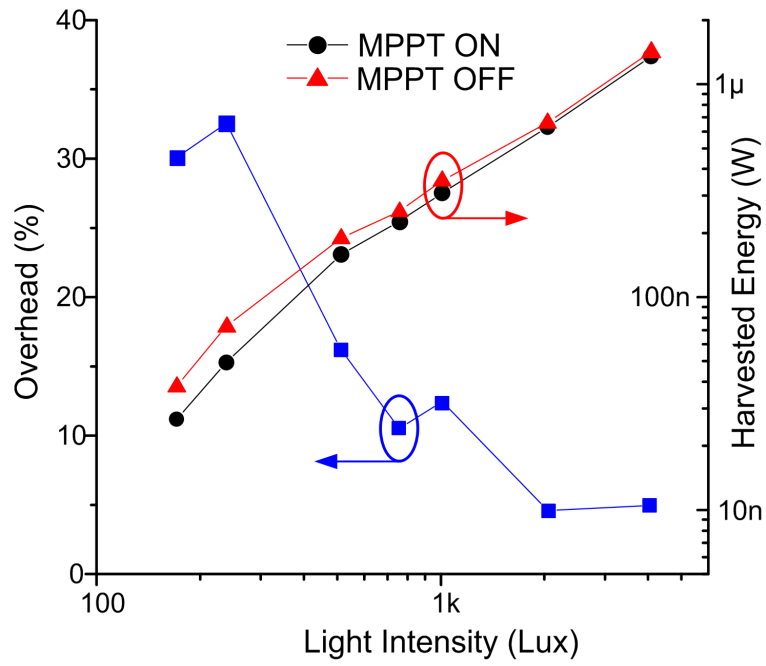


Figure 3.7: MPPT overhead over light intensity.

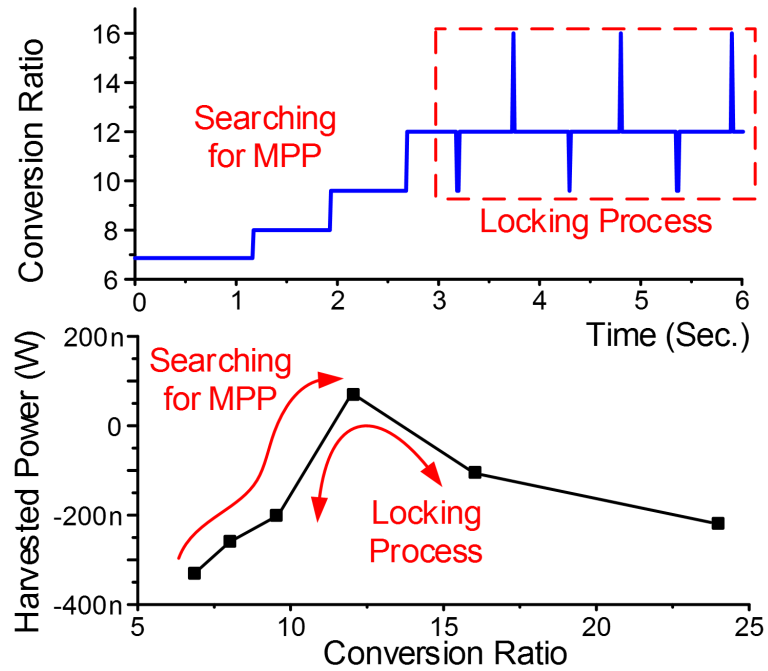


Figure 3.8: Examples of MPPT operation with conversion ratio.

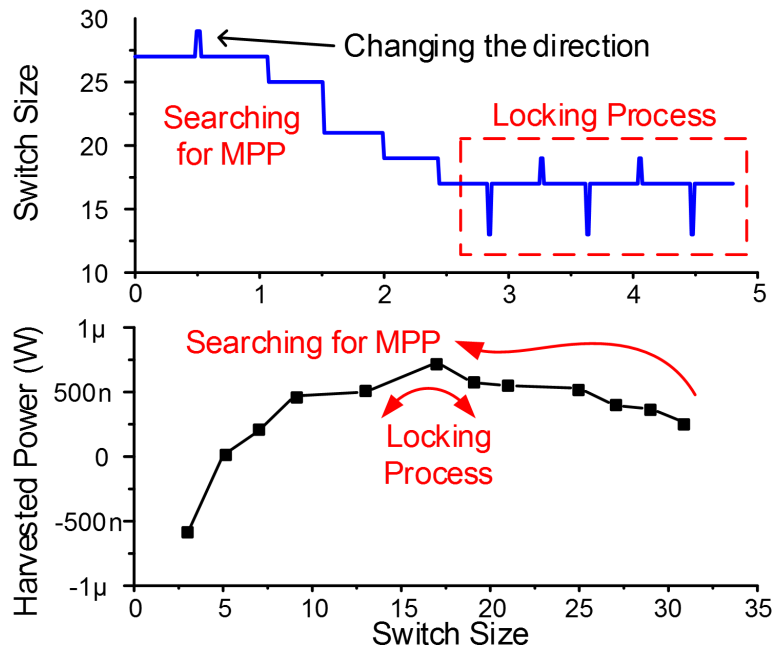


Figure 3.9: Examples of MPPT operation with switch size update.

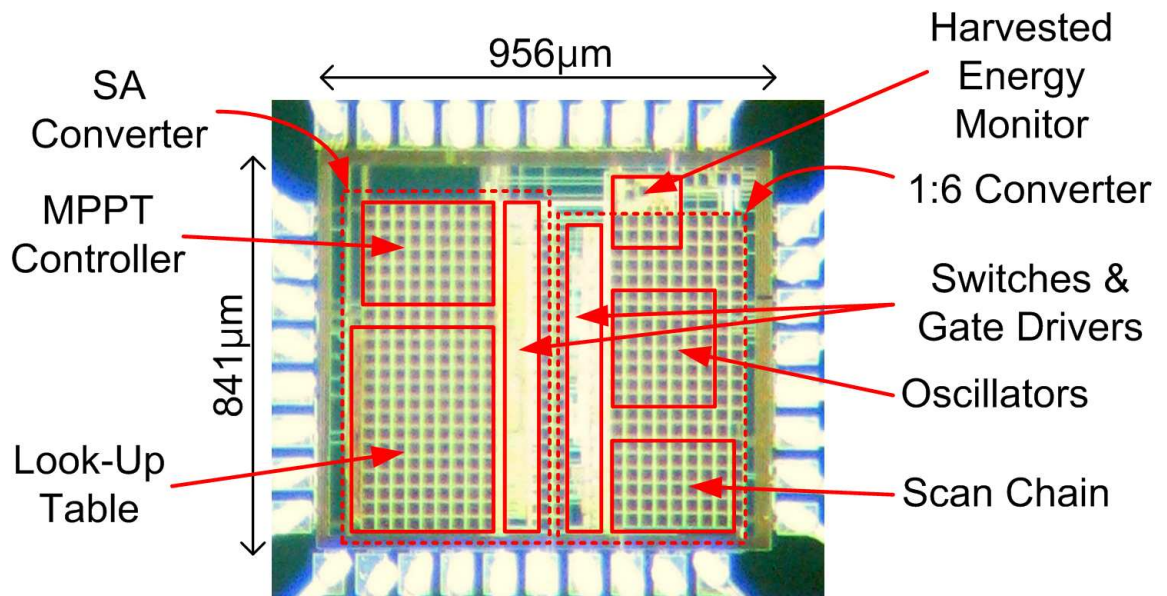


Figure 3.10: Die Photo.

Table 3.1: Performance summary of the proposed MPPT circuit and comparison to other prior works.

	This Work	[37]	[39]	[40]	[41]
Process	180 nm	350 nm	350 nm	250 nm	180 nm
Boost Converter Type	Capacitive	Capacitive	Inductive	Inductive	Inductive
Tracking Efficiency	94.6 %	N/A	95.0 %	80.5 %	99.6 %
MPPT Circuit Power	35 nW	2 $\mu$ W	6 $\mu$ W	2 $\mu$ W	234 nW
MPPT Method	Hill-Climbing	Hill-Climbing	Hill-Climbing	Analog	Mixed-Signal

the last position, the MPPT searches for the updated maximum power point (MPP). The MPPT locks converter configuration once finding MPP while it checks other configuration periodically for improved energy harvesting. A comparison to recent work is given in Table 3.1, showing  $>6\times$  improvement in terms of MPPT circuit power. Die photo is given in 3.10.

### 3.5 Summary

A maximum power point tracking circuit is designed for micro-scale sensor systems. It takes advantage of the unique structure of a switched capacitor energy harvester - it places a small sampling capacitor in parallel with the flying or decoupling cap in the SCBC that eavesdrops on the voltage transfer that occurs in the voltage converter. The power delivered to the battery is determined by integrating the small voltage fluctuations using correlated double sampling. Since the sampling capacitor is  $64.8\times$  smaller in size than the flying cap, the impact on conversion efficiency is negligible. By directly tracking power delivered to the battery all parameters of the switched capacitor energy harvester can be optimized, including switching frequency, switch size, and conversion ratio. Compared to conventional current mirror type MPPT circuits, this design incurs no voltage drop and does not require high bandwidth amplifiers. Using correlated double sampling, high accuracy is achieved with a power overhead of 5 %, even at low harvested currents of  $1.4 \mu\text{A}$  based on measured results in 180 nm CMOS.

## CHAPTER 4

### A Low Power Battery Supervisory Circuit

#### 4.1 Introduction

In general, mm-scale systems are equipped with a harvesting unit (e.g., solar cells [42]) to recharge their battery. They therefore require a battery supervisory circuit (BSC) to perform two critical functions (Fig. 4.1): 1) Power-On Reset (POR) detects power-on when the battery is initially connected or recharged by harvested energy and properly resets the sensor electronics; 2) Brown-Out Detection (BOD) detects dangerously low battery voltages that can damage the battery or cause unpredictable circuit operation, upon which it disconnects the battery from the system.

A BSC is one of the few components in a sensor node that is continually connected to the battery. Given a total average power limit of a few nW for typical mm-scale systems, BSC current draw is therefore limited to  $< 1$  nA to avoid dominating the overall power budget. While commercial POR/BODs are widely available, they typically consume on the order of 0.1-to-10 $\mu$ A as shown in Fig. 4.2 [43–47], motivating work on ultra-low power BSC designs to enable the emerging class of ultra-small, nW, sensor nodes.

This section proposes a novel ultra-low power BSC implemented in 180 nm CMOS, which is introduced in [48]. The BSC is integrated in a 1 mm<sup>3</sup>-sensor system [2] and complete system functionality is shown with silicon measurements. The BSC controls the reset functionality of electronics on its own die as well as orchestrates the reset of other chips in the sensor system by modulating power supply voltages that are monitored by secondary reset detectors on those dies.

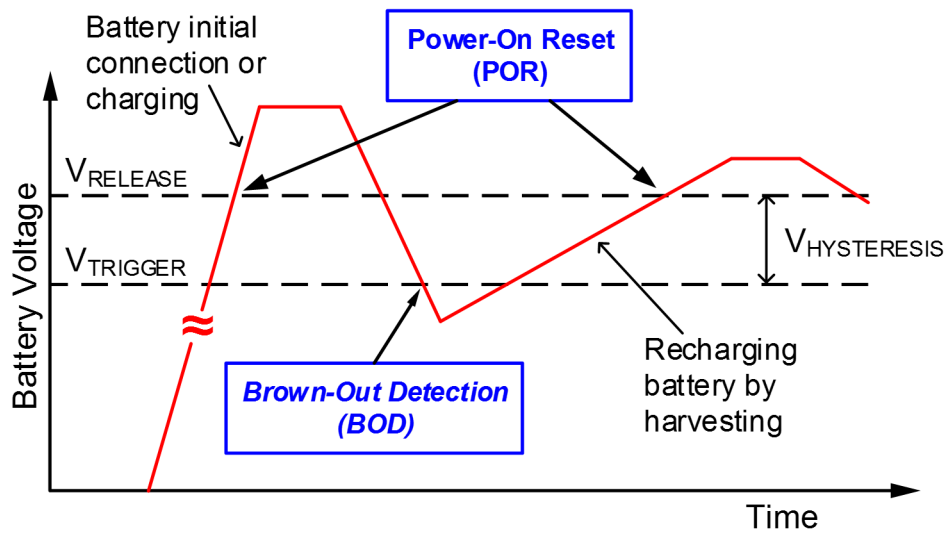


Figure 4.1: Varying battery voltage and required functions of battery supervisory circuit (BSC).

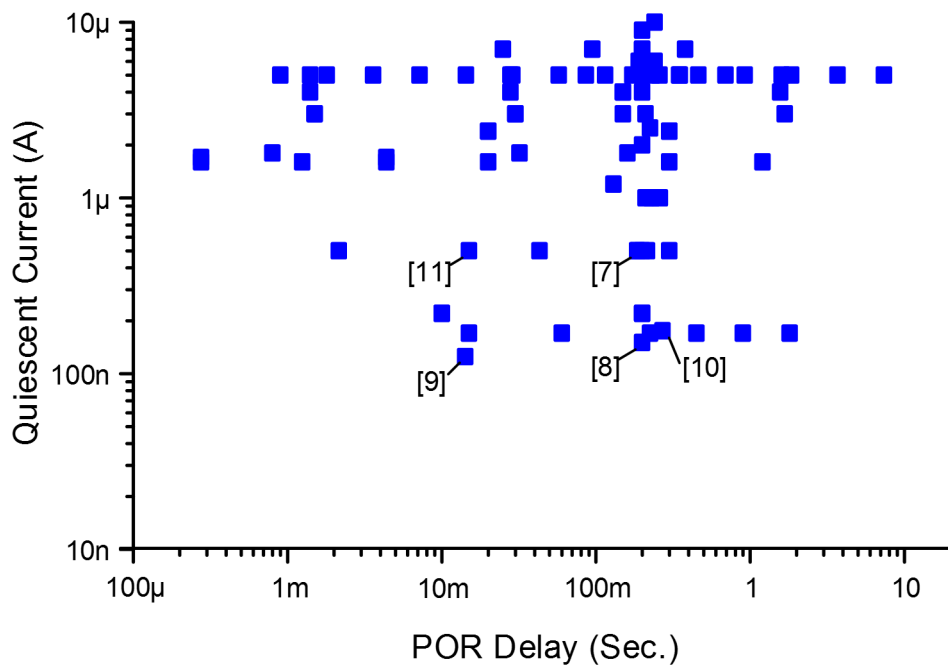


Figure 4.2: Quiescent current over power-on-reset (POR) delay of commercial POR/BOD circuits.

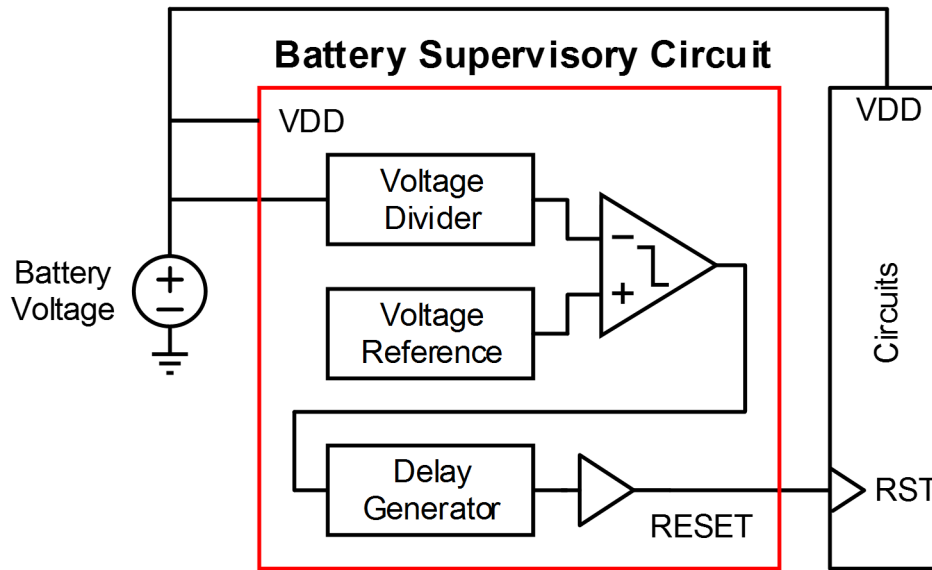


Figure 4.3: Conventional BSC structure.

## 4.2 Battery Supervisory Circuit

A conventional BSC typically consists of a voltage reference, a battery voltage divider, a comparator, and a delay generator as shown in Fig. 4.3. The comparator generates an internal compare signal when the divided battery voltage is lower than the reference voltage. The delay generator then adds a minimum delay before releasing the reset signal. This delay is needed to allow various circuits in the system to stabilize, such as voltage regulators, references, and clock generators. In addition, a controlled amount of hysteresis in the comparator is necessary to avoid oscillation [49].

Fig. 4.4 shows the block diagram of the proposed BSC. It includes a diode-stack voltage divider, a leakage-based voltage reference, a two-stage comparator, a leakage-based clock generator, a delay generator, and a low-battery-voltage protector. Compared to the conventional BSC, the proposed approach includes low-power building blocks and additional circuits to achieve the ultra-low-power specification while maintaining its operation.

The first key novelty is the voltage reference to offer robust reset operation. Battery voltage can be changed in different rates according harvesting and load condition, thus the BSC should guarantee the POR and BOD operation over a wide range of battery voltage rising/falling speed. This voltage reference prevents the BSC from releasing a false reset or suppressing reset trigger.

The second is the combination of a clocked comparator and a leakage-based clock generator. A



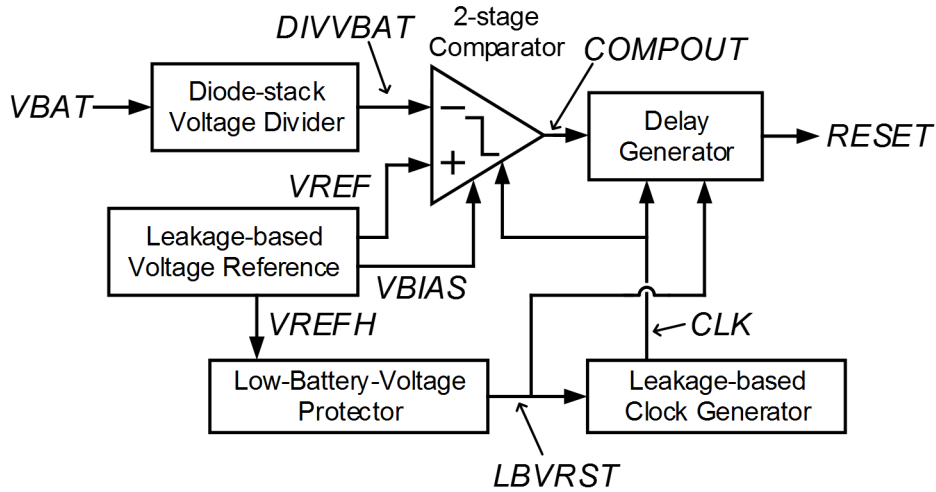


Figure 4.4: Proposed BSC structure.

preamplifier consistently consumes tail current. It becomes larger for higher bandwidth, especially for the case that input difference is small. On the other hand, a clocked comparator only requires instant power, but the total power including a clock generator can be large. In this design, low-power clocked comparator is implemented by incorporating a leakage-based clock generator. This clock is also reused for POR delay. Moreover, in the proposed BSC, using a reference voltage ( $V_{REFH}$ ) from the voltage reference, the low-battery-voltage protector detects a condition that battery voltage is very low and circuits in BSC are not able to operate, and generates a reset signal (LBVRST) which instantly forces RESET. The LBVRST resets the clock generator and delay generator for low-battery-voltage condition.

Fig. 4.5 conceptually shows how the reset is generated according to the battery voltage. Five phases are identified on a set of rising and falling  $V_{BAT}$  waveform. The basic operation of the BSC in each phase is as follows. In the first phase ( $\Phi_1$ ),  $V_{BAT}$  is too low to properly operate circuits in BSC. When  $V_{BAT}$  is lower than 1.1 V, LBVRST resets the clock generator and the delay generator, asserting also RESET. In the next phase ( $\Phi_2$ ),  $V_{BAT}$  is larger than 1.1 V, and LBVRST is released. Before the point of A,  $DIVVBAT$  is lower than  $V_{REF}$ , and COMPOUT and RESET stay as the same as in  $\Phi_1$ . At the point A,  $V_{BAT}$  crosses the reset-release-threshold voltage ( $V_{RELEASE}$ ). From this point,  $DIVVBAT$  is higher than  $V_{REF}$ , and COMPOUT becomes low at the negative edge of CLK. This change is transferred to RESET through the reset generator at the positive edge of CLK. Thus, a minimum of one half of the clock period is provided as the POR delay to allow circuits

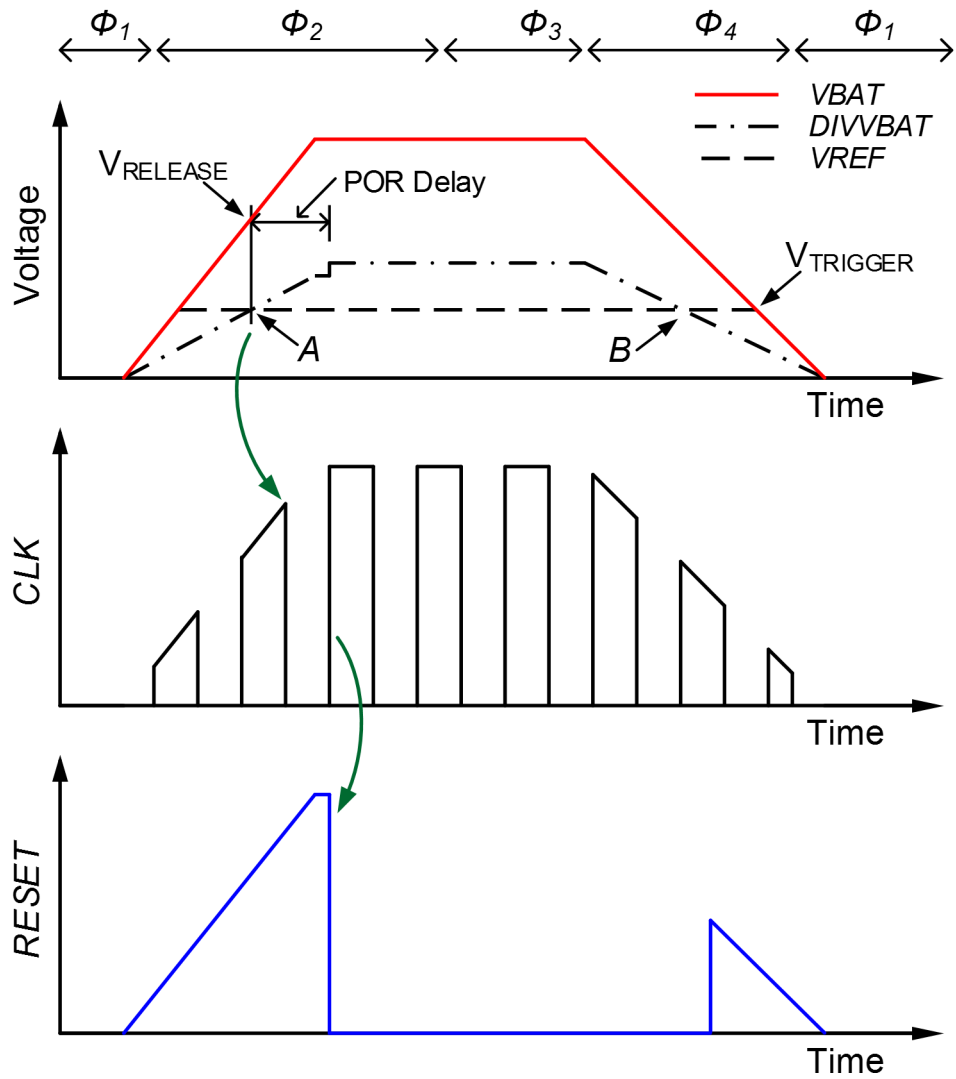


Figure 4.5: Conceptual BSC operation according to battery voltage ( $V_{BAT}$ ).

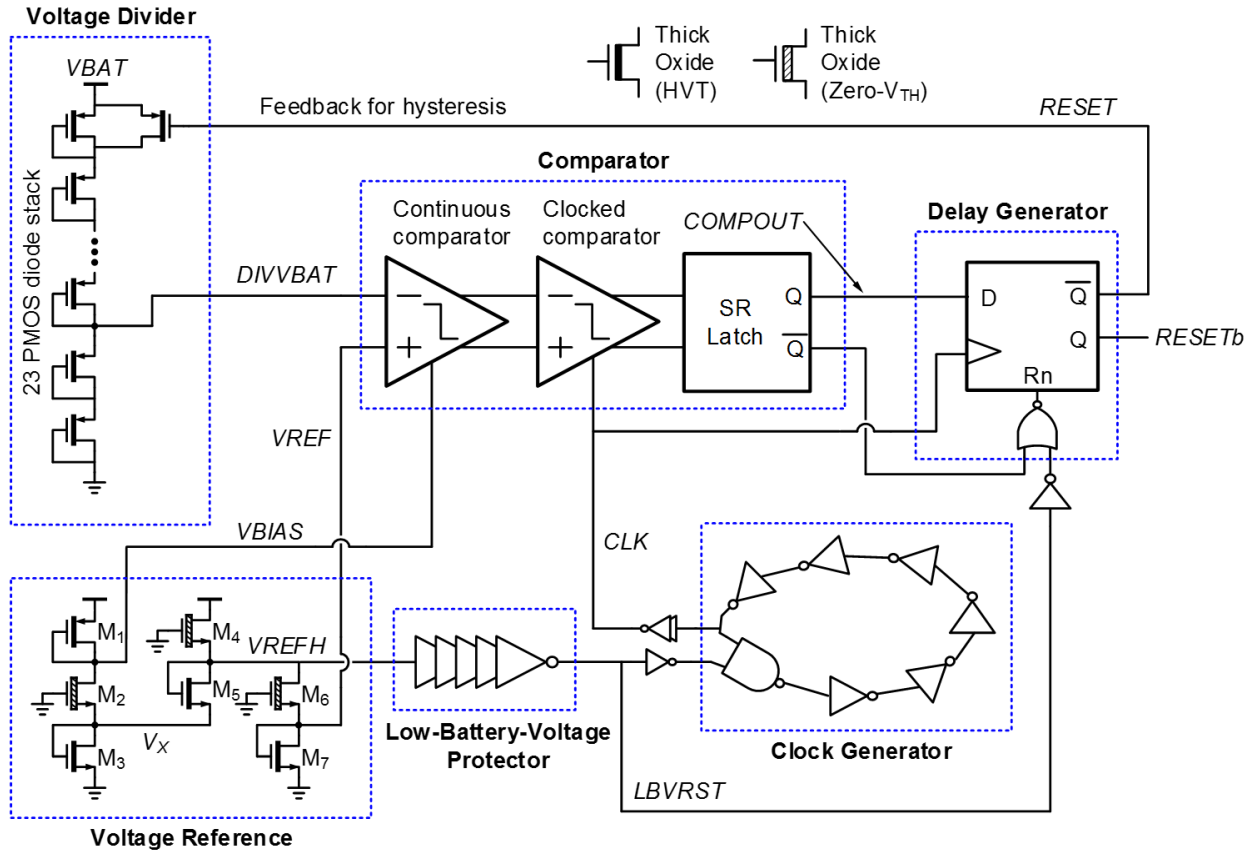


Figure 4.6: Circuit implementation of proposed BSC.

in the system component to stabilize. In the third phase ( $\Phi_3$ ), RESET is released, and the system operates in normal mode. In the last phase ( $\Phi_4$ ), as  $V_{BAT}$  decreases, DIVVBAT crosses over  $V_{REF}$  at the point of B and  $V_{BAT}$  becomes lower than the reset-trigger-threshold voltage ( $V_{TRIGGER}$ ). As soon as the comparator detects the crossing at the point of B, RESET is triggered to stop the system. Lastly, when battery voltage is lower than 1.1 V again, LBVRST is released again to prevent BSC circuit malfunction at the low  $V_{BAT}$  as  $\Phi_1$ .

### 4.3 Circuit Implementation

Fig. 4.6 shows the circuit implementation of the proposed BSC. The diode-stack voltage divider, the leakage-based voltage reference, the preamplifier (the 1st stage of the 2-stage comparator), and the low-battery-voltage protector are always working while the clocked comparator (the 2nd stage) is activated by the clock signal. To realize the current consumption of  $< 1$  nA, low-power

building blocks are designed for always turned-on components. Also, a low-power leakage-based oscillator is designed to operate the clocked comparator within the limited power budget. More detailed explanation follows below.

### 4.3.1 Diode-Stack Voltage Divider

The diode-stack voltage divider generates  $DIVVBAT$  that indicates  $V_{BAT}$  at the level of  $V_{REF}$ . The divider is implemented using a 23-transistor PMOS diode stack to reduce the power consumption of the voltage divider. Their gate leakage current is negligible since thick-gate transistors are used. When the system is in reset mode ( $RESET = 1$ ), the diode stack has the division ratio of 11.5 by turning off the top feedback PMOS. In this case,  $V_{RELEASE}$  is set to  $11.5 \times V_{REF}$ . On the other hand, when the system is released from the reset (operation mode), the feedback signal ( $RESET$ ) shorts out the top PMOS and change the division ratio to 11.0, which sets  $V_{TRIGGER}$  to  $11.0 \times V_{REF}$ . Hence, a voltage of  $0.5 \times V_{REF}$  is introduced as hysteresis by this adjustment of the division ratio in response to  $RESET$  using a switch and a feedback signal, similar to [50].

This hysteresis generation is vital in the miniaturized sensing system to avoid system oscillation between reset and operation mode. In reset mode, it draws only a few of nA by turning off unnecessary blocks and keeping only required blocks on for energy harvesting. In contrast, in active mode, the system can consumes up to  $10 \mu A$  for a variety of tasks such as radio transmission and temperature measurement. This  $1,000 \times$  current consumption change between two modes has not become a problem in the systems using conventional coin cell or AA batteries with  $\leq 100 \Omega$ . However, the miniaturized batteries have limited performance and as such a high resistance due to its small form factor. For instance, a commercialized Li thin-film battery has  $\sim 10 \text{ k}\Omega$  with  $0.7 \text{ mm}^3$  [51]. The high battery resistance results in a large voltage drop difference.

For example as shown in Fig. 4.7, if the system has a battery with  $10 \text{ k}\Omega$  and consumes  $10 \text{ nA}$  and  $10 \mu A$  for reset and operation mode, battery voltage drops by  $100 \mu V$  and  $100 \text{ mV}$ , respectively. Once battery voltage increases above  $V_{RELEASE}$ , the system moves from reset to operation mode. Increased current consumption decreases battery voltage to ' $V_{RELEASE} - 100 \text{ mV}$ '. With less than  $100 \text{ mV}$  hysteresis, the battery voltage will go down below  $V_{TRIGGER}$ , and the system enter the reset mode again. Therefore, the sensor node becomes unstable by oscillating between two modes.

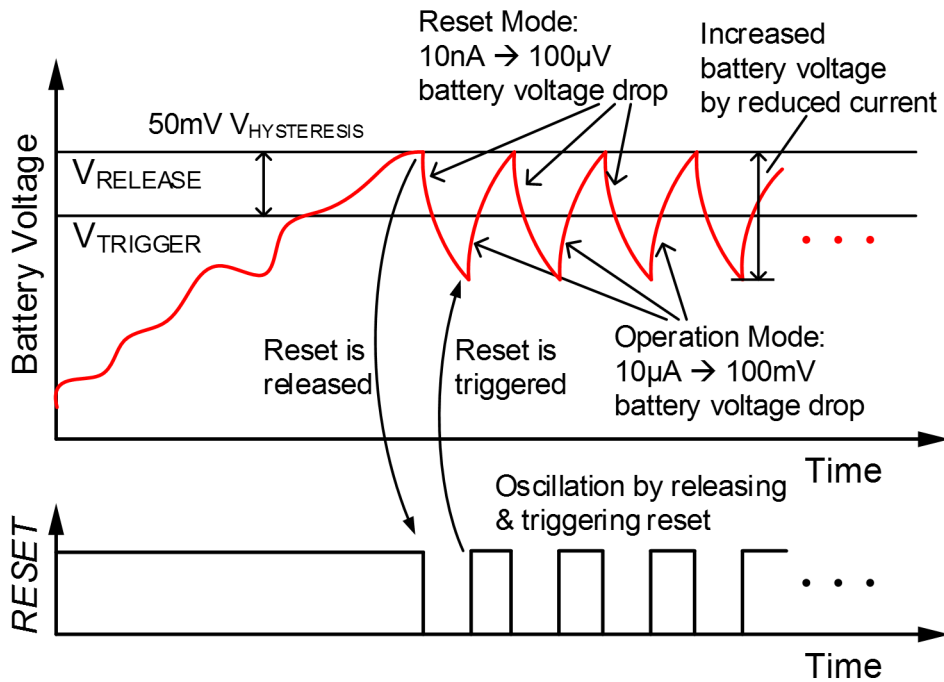
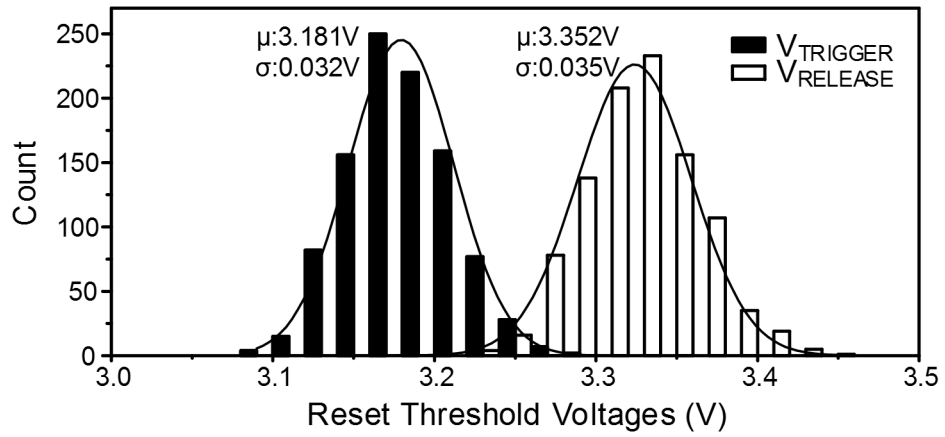


Figure 4.7: Problem from small  $V_{HYSTERESIS}$  in a system with high battery internal resistance.

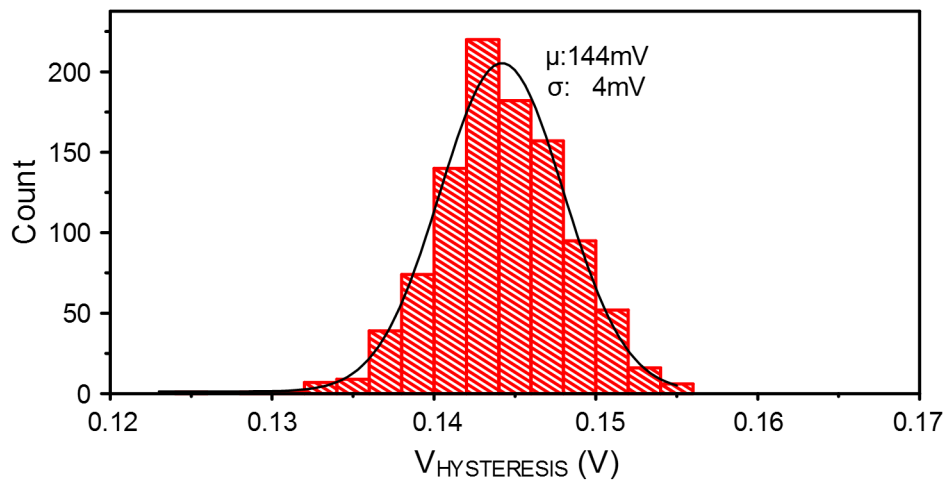
To guarantee the stability, the generated hysteresis of  $0.5 \times V_{REF}$  should be larger than 100 mV, so  $V_{REF} > 200$  mV.

Fig. 4.8 shows  $V_{TRIGGER}$ ,  $V_{RELEASE}$ , and their hysteresis voltage ( $V_{HYSTERESIS} = V_{RELEASE} - V_{TRIGGER}$ ) from the simulated voltage divider with process variation and mismatch. In Fig. 4.8 (a), the distribution of  $V_{TRIGGER}$  and  $V_{RELEASE}$  is overlapped but it does not mean that  $V_{HYSTERESIS}$  can be a negative, leading to an unstable system. The positive hysteresis is guaranteed by the structure of the voltage divider that uses diode stacks and a switch, which physically changes the number of transistors serially connected. As shown in Fig. 4.8 (b),  $V_{HYSTERESIS}$  is always a positive and no zero crossing although it has variation due to device mismatch. Here,  $V_{HYSTERESIS}$  of 144 mV tells that internal battery resistance can be covered up to 14.4 k $\Omega$  with 10  $\mu$ A current consumption.

Due to the extremely small power budget, transistor size of the diode stack is chosen by limiting the worst-case power condition within 10 % of the total BSC power. Current through a diode is sensitive to threshold voltage as well as assigned voltage that scales with supply voltage. In a target application, the maximum battery voltage can be 4.2 V. Fig. 4.9 shows simulated power



(a)



(b)

Figure 4.8: Impact of process variation and mismatch on reset threshold voltages (a)  $V_{TRIGGER}$  and  $V_{RELEASE}$  (b)  $V_{HYSTERESIS}(=V_{RELEASE}-V_{TRIGGER})$ .

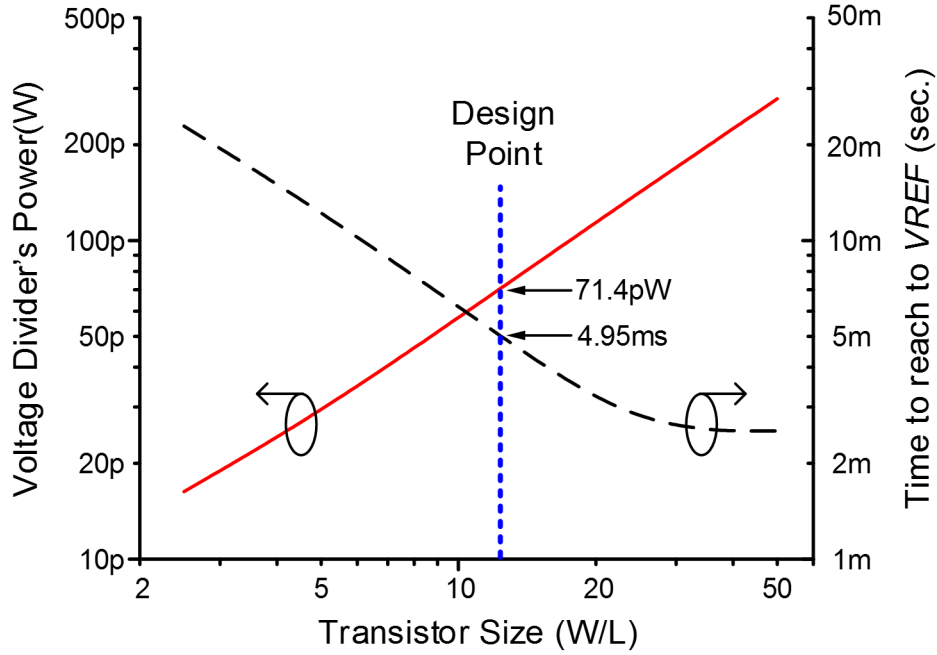


Figure 4.9: Simulated power consumption and speed of voltage divider.

consumption of the voltage divider in fast corner with 4.2 V supply voltage as the worst case and time to reach 0.3 V (the stabilized voltage value of  $V_{REF}$ ) in nominal corner as the battery voltage increases from ground to 4.2 V in 1  $\mu$ s. With the selected size, DIVVBAT can reach 0.3 V in 5 ms in nominal corner simulation. Thus,  $V_{REF}$  should stabilize before 5 ms to properly generate RESET as discussed later.

### 4.3.2 Voltage Reference

A leakage-based voltage reference topology using two different threshold voltage transistors is used for its low power consumption [52]. However, its original implementation employs a large decoupling capacitance to ground for noise purposes, leading to a large settling time of 8.4 ms (with 1 pF decoupling capacitor), which is slower than the voltage divider. This introduces the risk that, with a fast rising  $V_{BAT}$ , DIVVBAT exceeds  $V_{REF}$  temporarily while  $V_{REF}$  is stabilizing, causing a false reset release that could be fatal to system operation as shown in Fig. 4.10 (a). Hence, we connect the decoupling capacitance to  $V_{BAT}$  instead of ground and reduce gate length to decrease settling time.

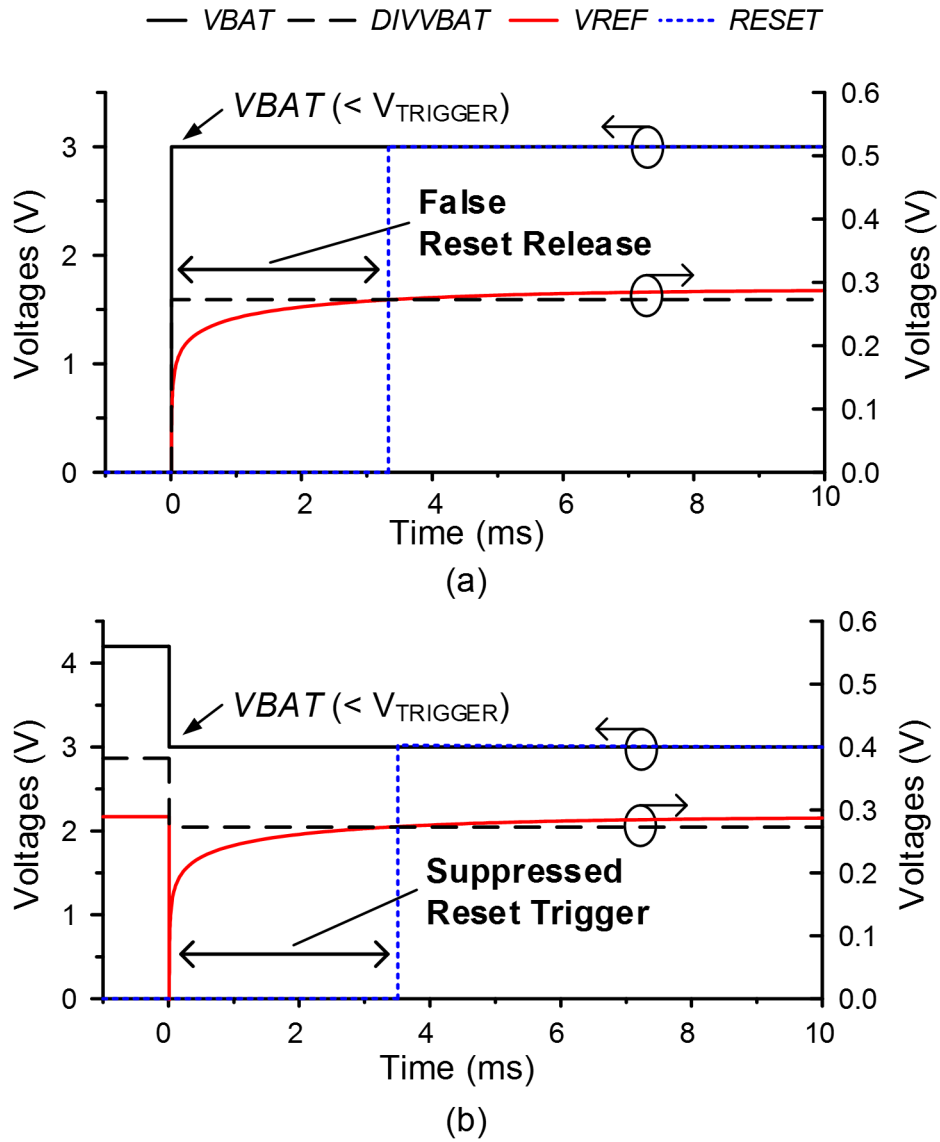


Figure 4.10: Problems from using conventional low-power voltage reference (a) false reset release using decoupling capacitor to ground (b) suppressed reset trigger by using decoupling capacitor to supply.



However, as  $V_{BAT}$  drops fast, the decoupling capacitor coupled to  $V_{BAT}$  lowers  $V_{REF}$ , leading to the danger of an invalid triggering of reset as shown in Fig. 4.10 (b). To avoid coupling to  $V_{BAT}$ , we instead propose a two-stage reference structure without using the decoupling capacitor to  $V_{BAT}$ . The first stage reference ( $M_1 - M_5$ ) provides a reference voltage of about 0.6 V by stacking the leakage-based voltage references. This acts as a preconditioner and generates a supply voltage for the second reference stage ( $M_6, M_7$ ) as shown in Fig. 4.6. This decouples the reference from  $V_{BAT}$  while the elimination of decoupling capacitance and reduced gate length ensure fast stabilization (0.39 ms) with a total reference current draw of 59 pA (in simulation with 4.2 V).

In simulation, compared to the conventional 2T leakage-based voltage reference, the proposed reference improves the line sensitivity and PSRR by the two-stage structure as shown in Fig. 4.11. The line sensitivity is decreased by  $287\times$  from 1 V to 4.2 V, and the PSRR is similar with the conventional one with a decoupling capacitor of 10 pF up to 1.2 MHz.

Typically, the leakage-based voltage reference requires an analog buffer to load circuits drawing current due to its own low power consumption. However, the buffer consumes higher power and occupy area than the voltage reference itself. In this proposed voltage reference, since the second reference stage only dissipates 11 pA, the first-stage preconditioner can be designed to drive the load circuit without a buffer with 48 pA.

In addition, the voltage reference generates a proportional to absolute temperature (PTAT)  $V_{BIAS}$  to bias the tail current of the following preamplifier (Fig. 4.6).  $V_{BIAS}$  in the voltage reference can be obtained based on the following subthreshold current equation.

$$I_{SUB} = \mu C_{OX} \frac{W}{L} (m-1) V_T^2 e^{-\frac{V_{GS}-V_{TH}}{mV_T}} (1 - e^{-\frac{V_{DS}}{V_T}}). \quad (4.1)$$

where  $\mu$  is mobility,  $C_{OX}$  is oxide capacitance,  $W$  is transistor width,  $L$  is transistor length,  $m$  is subthreshold slope factor ( $m = 1 + C_d/C_{OX}$  where  $C_d$  is depletion capacitance),  $V_T$  is thermal voltage ( $kT/q$ ),  $V_{GS}$  is gate-source voltage,  $V_{TH}$  is transistor threshold voltage, and  $V_{DS}$  is drain-

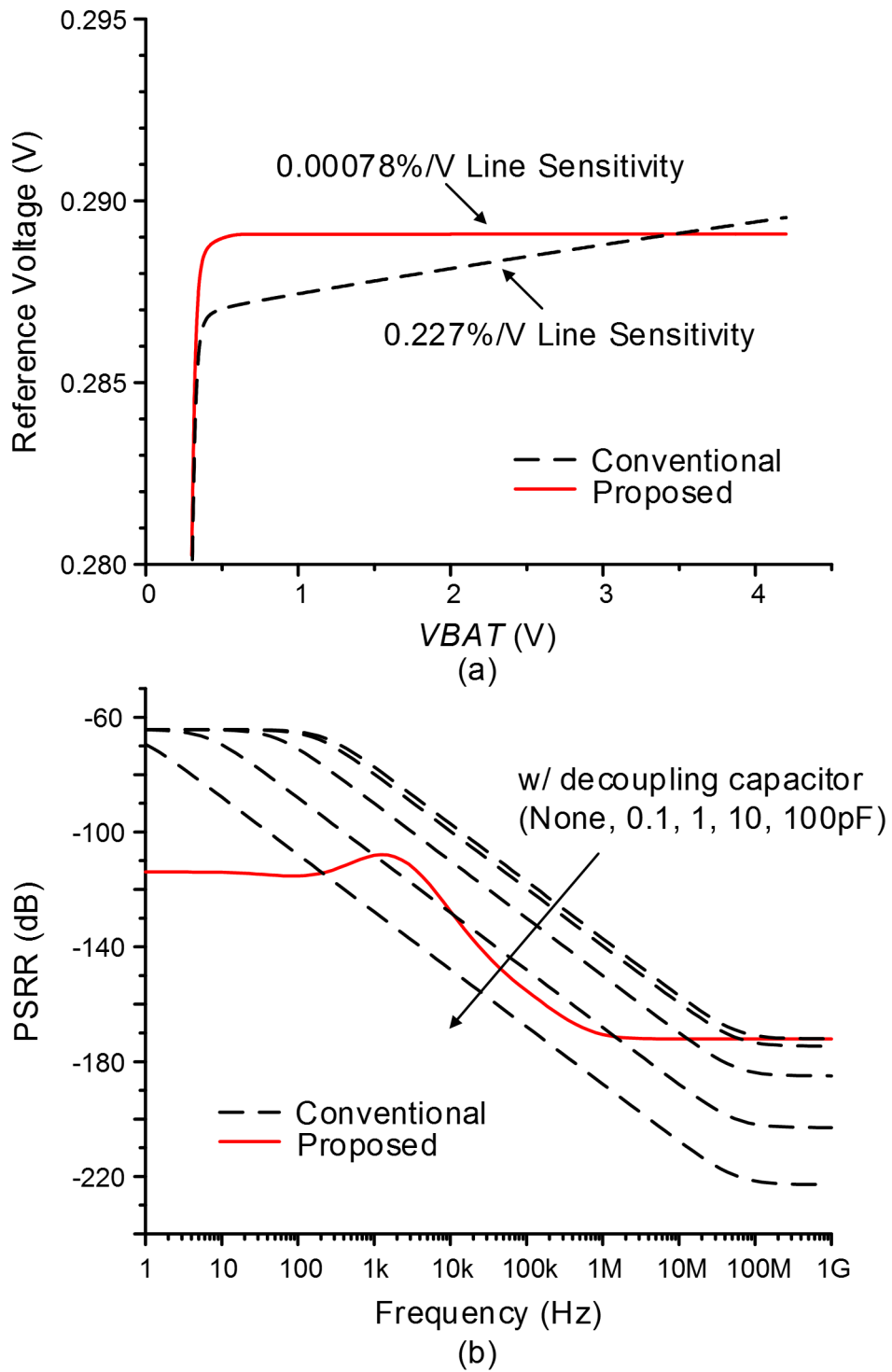


Figure 4.11: Simulated conventional and proposed voltage reference (a) line sensitivity (b) power supply rejection ratio (PSRR).

source voltage. Since the same current flows through  $M_1$ ,  $M_2$ , and  $M_3$ ,

$$\begin{aligned}
I &= \mu_1 C_{OX1} \frac{W_1}{L_1} (m_1 - 1) V_T^2 e^{\frac{V_{BAT} - V_{BIAS} - |V_{TH1}|}{m_1 V_T}} \\
&= \mu_2 C_{OX2} \frac{W_2}{L_2} (m_2 - 1) V_T^2 e^{\frac{-V_X - V_{TH2}}{m_2 V_T}} \\
&= \mu_3 C_{OX3} \frac{W_3}{L_3} (m_3 - 1) V_T^2 e^{\frac{V_X - V_{TH3}}{m_3 V_T}}
\end{aligned} \tag{4.2}$$

Here, we assume all devices are in weak inversion, their  $V_{DS}$  are greater than  $5V_T$ , and  $M_2$  follows the subthreshold current equation as  $V_{GS}$  is  $-V_X$ . When  $V_{DS} > 5V_T$ , ' $1 - e^{-\frac{V_{DS}}{V_T}}$ ', of equation 4.1 is negligible with less than 1% error. Analogous to  $V_{REF}$  in [52],

$$V_X = \frac{m_2 V_{TH3} - m_3 V_{TH2}}{m_2 + m_3} + \frac{m_2 m_3}{m_2 + m_3} V_T \ln \left( \frac{\mu_2 C_{OX2} W_2 L_2 (m_2 - 1)}{\mu_3 C_{OX3} W_3 L_3 (m_3 - 1)} \right) \tag{4.3}$$

Using  $V_X$ ,  $V_{BIAS}$  can be calculated as

$$V_{BIAS} = V_{BAT} + \frac{-m_1 V_X - m_1 V_{TH2} + m_2 V_{TH1}}{m_2} + m_1 V_T \ln \left( \frac{\mu_1 C_{OX1} W_1 L_2 (m_1 - 1)}{\mu_2 C_{OX2} W_2 L_1 (m_2 - 1)} \right) \tag{4.4}$$

Note that MOSFET  $V_{TH}$  is complementary to absolute temperature (CTAT) while  $V_T$  has PTAT with 0.085 mV/K. Thus, the temperature dependency of  $V_{BIAS}$  can be controlled by width and length of transistors. This  $V_{BIAS}$  is designed with proper transistor sizing for TC of 30.4 mV/°C in order to relieve the increased PMOS tail current at high temperature.

### 4.3.3 Comparator and Clock Generator

The two-stage comparator consists of a preamplifier followed by a clocked comparator as shown in Fig. 4.12. The first stage uses a PMOS input stage to accommodate the relatively low  $V_{REF}$  of 0.3 V. Previously described PTAT  $V_{BIAS}$  generated from the reference preconditioner mitigates increased tail current of the preamplifier at high temperature, reducing power consumption by 38 % at 80 °C as shown in Fig. 4.13. It consists of a simple PMOS-input differential amplifier with a NMOS cross-coupled latch. Since tail current is low for low power consumption, the output voltage is also low ( $\sim 0.3$  V).

The second stage converts the low preamplifier output voltage to battery voltage (from  $\sim 0.3$  V

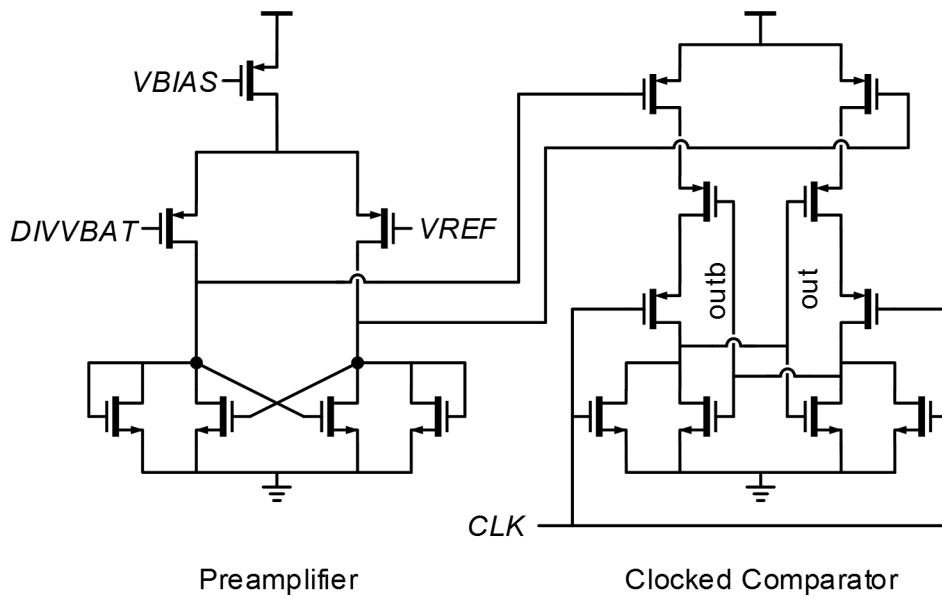


Figure 4.12: Comparator transistor diagram.

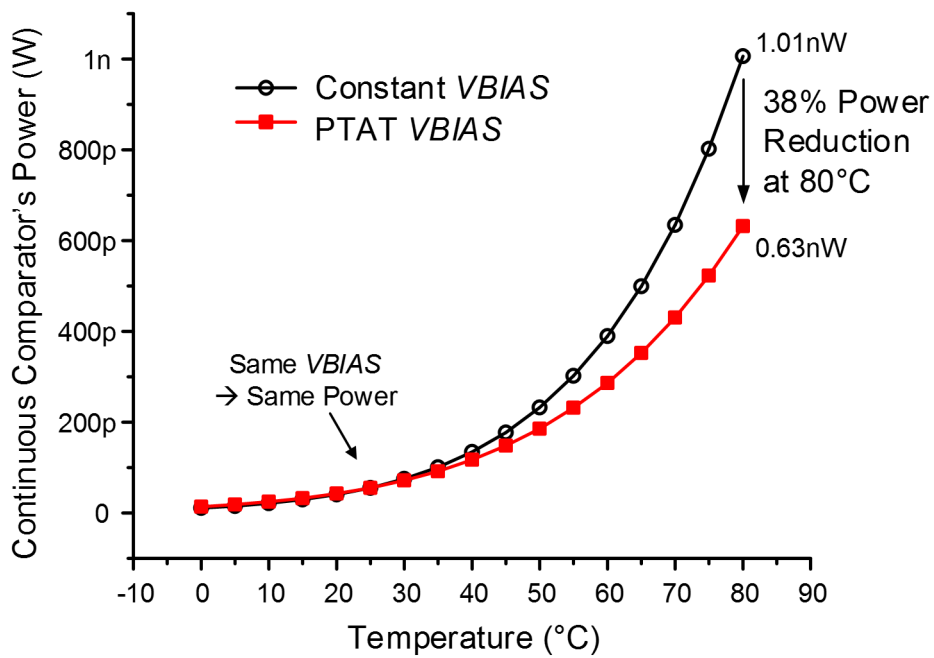


Figure 4.13: Simulated power consumption of preamplifier over temperature.

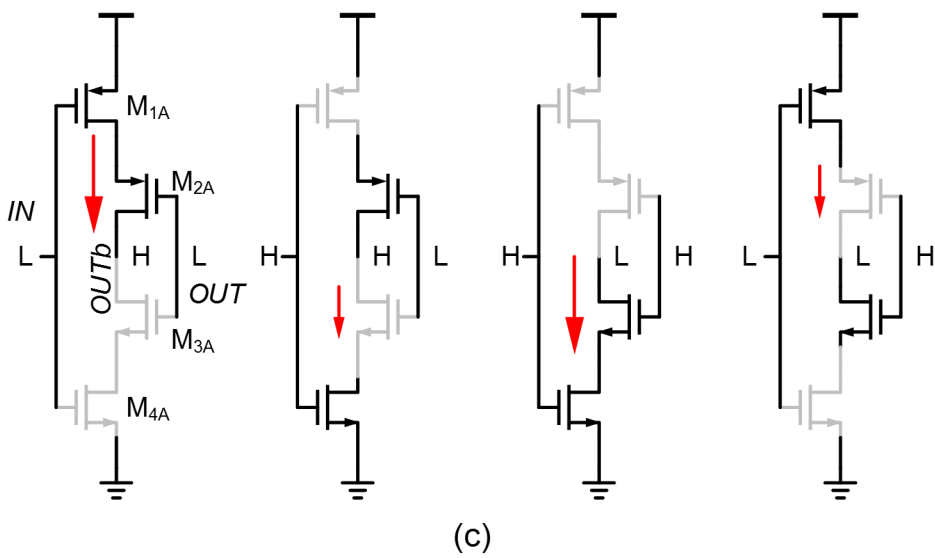
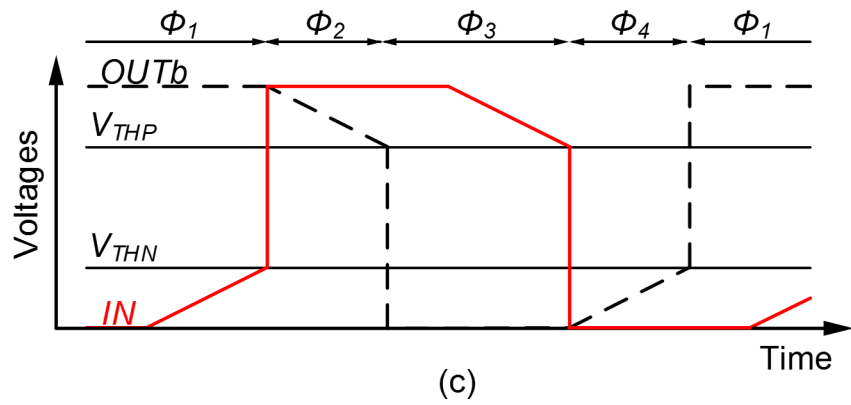
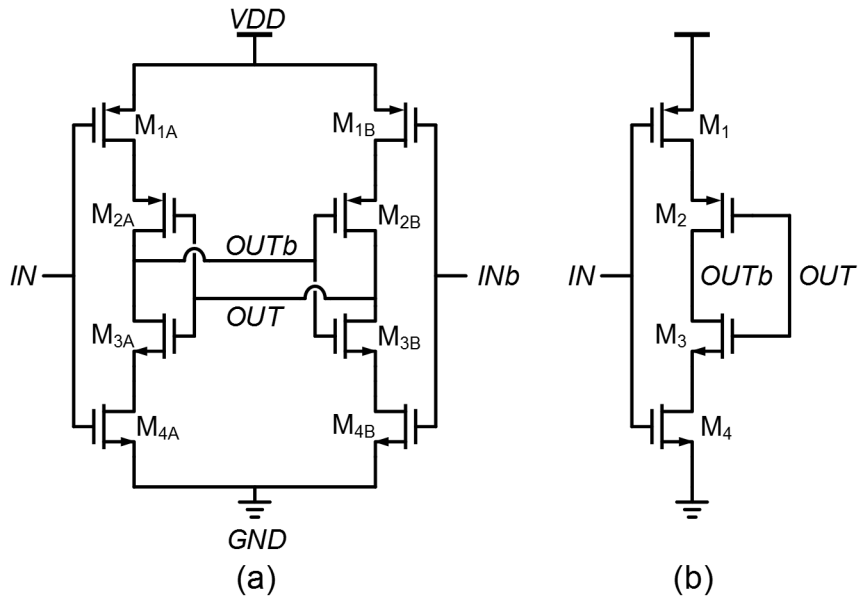


Figure 4.14: Leakage-based oscillator (a) delay cell (b) its half circuit (c) waveform (d) half circuits for each phase of operation.

to 3-to-4V). It is a clocked comparator driven by a leakage-based oscillator to reduce power to 343 pW (in simulation with 4.2 V), including the oscillator. The oscillator uses leakage-based delay stages to provide CLK as shown in Fig. 4.14 (a) [42, 53]. Fig. 4.14 (b) and (c) shows waveforms and equivalent half circuit diagram for each phase.

In the first phase ( $\Phi_1$ ), IN and OUT are low while INb and OUTb are high. Here,  $M_{1A}$  and  $M_{2A}$  pull up OUTb whereas  $M_{3A}$  and  $M_{4A}$  are turned off, and output voltages (OUT and OUTb) stay at the same values until IN changes. In the next phase ( $\Phi_2$ ), IN is changed to  $V_{DD}$  by the previous stage in the oscillator.  $M_{1A}$  is turned off while  $M_{4A}$  is on. Current charging OUTb is decided by the leakage current through  $M_{1A}$  and  $M_{3A}$  which are both turned off. Here,  $V_{DS}$  is larger at  $M_{3A}$  than  $M_{1A}$  since OUTb is  $V_{DD}$ . Thus, the net current discharges OUTb to lower voltage. On the other side, OUT is increased by leakage current through  $M_{2B}$  larger than  $M_{4B}$  due to larger  $V_{DS}$ . In the third phase ( $\Phi_3$ ), 'VDD-OUTb' crosses  $V_{THP}$  (PMOS threshold voltage) while OUT complementally increases to  $V_{THN}$  (NMOS threshold voltage), and thus  $M_{3A}$  and  $M_{2B}$  are turned on. It accelerates discharging OUTb and charging OUT since the pull-down current is increased from leakage to active current. The delay stage is stable and does not have any voltage change until the previous stage changes IN to ground. In the last phase ( $\Phi_4$ ), when IN changes, OUTb decreases while OUT increases slowly due to leakage current, which is complementary version of  $\Phi_2$ .

Although the voltage divider, the voltage reference, and the preamplifier consume a constant power, the power consumption from the clocked comparator and oscillator is proportional to the operating frequency. Fig. 4.15 shows the power consumption versus the operating frequency (in simulation with 4.2 V) by changing the transistor size in the oscillator. We set the operating frequency to 5.4 Hz to save energy, which gives detection period of 185 ms. The comparator consumes 343 pW (59 %) and allows to design the total power consumption of  $< 1$  nW.

#### 4.3.4 Other Blocks

RESET is controlled by a D flip-flop (Delay Generator) with COMPOUT and CLK as shown in Fig. 4.6, and its waveform is displayed in Fig. 4.16. As  $V_{BAT}$  increases higher than  $V_{RELEASE}$ , COMPOUT is captured at the rising edge of CLK. It introduces a minimum reset delay of a half

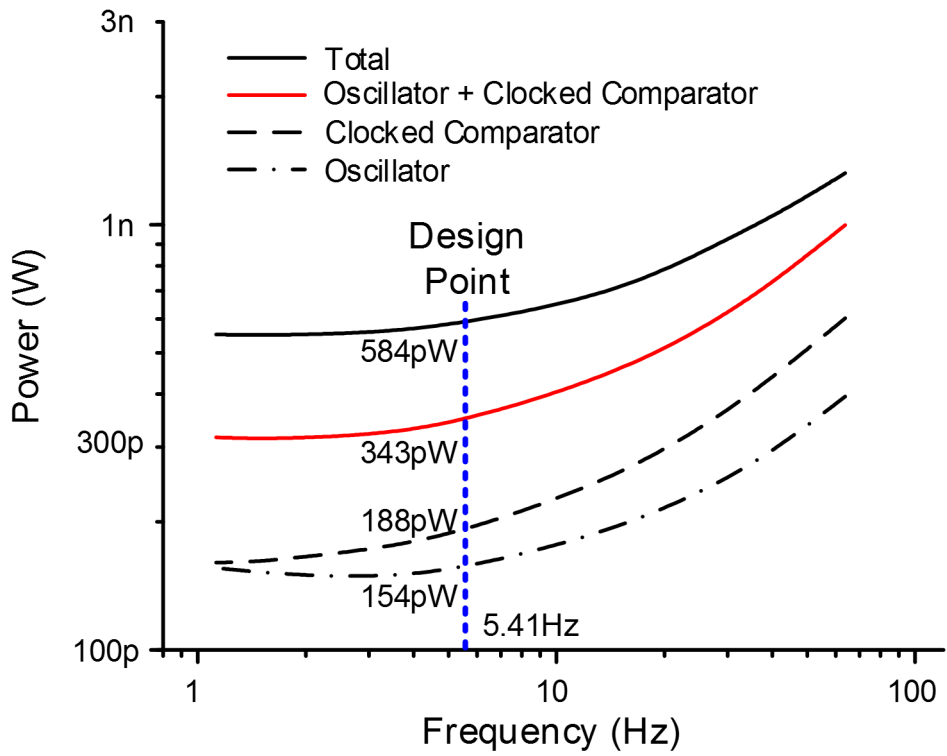


Figure 4.15: Power consumption versus operating frequency.

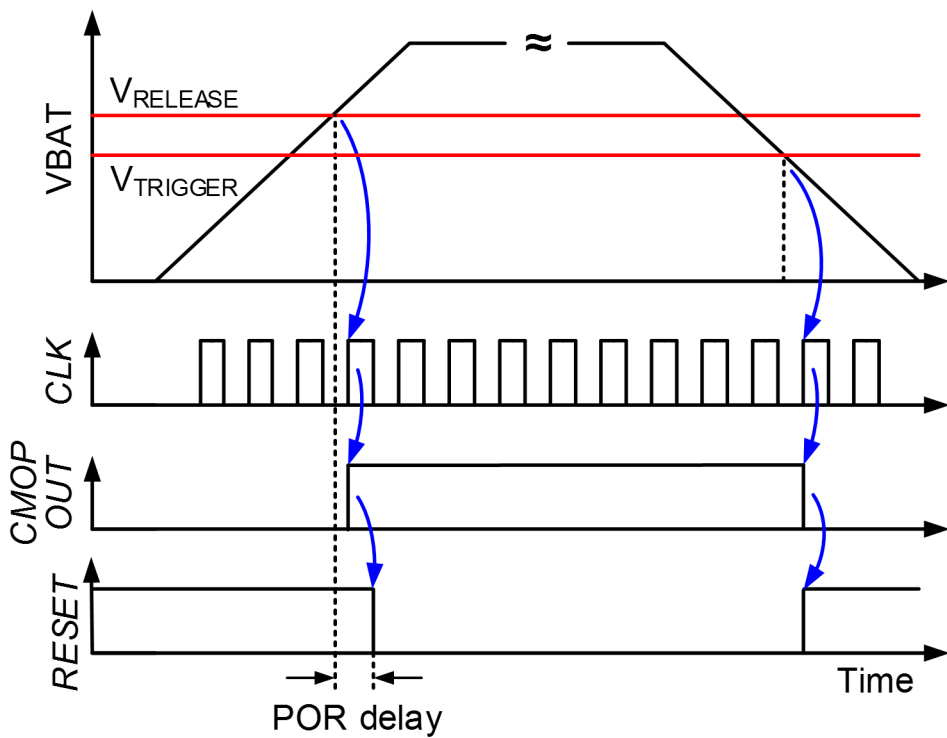


Figure 4.16: *RESET* control.

a clock period (92 ms in simulation with 4.2 V). However, when  $V_{BAT}$  drops below  $V_{TRIGGER}$ , COMPOUT is lowered at the falling edge of CLK, and RESET is immediately asserted without additional delay. This is desirable since faster reset prevents circuits from malfunctioning at low battery voltage.

A low-battery-voltage protector overrides the BSC below 1.1 V to prevent comparator and D flip-flop malfunction. This circuit consists of a chain of inverters and decoupling capacitors and uses transistor stacking and diodes to reduce static current to 39 pA (in simulation with 4.2 V). The input of the inverter chain is connected to  $V_{REFH}$  from the reference preconditioner, resulting in triggering LBVRST at a battery voltage of 1.1 V, providing guardband to ensure correct BSC circuit operation.

## 4.4 Reset Propagation Strategy

### 4.4.1 Reset Propagation Strategy in mm-scale Multi-layer System

The proposed BSC was implemented in the control processor of a 1 mm<sup>3</sup>-sensor system as shown in Fig. 4.17, consisting of 5 stacked die layers: 1) solar cells and timer; 2) thin-film Li battery; 3) DSP processor; 4) control processor and power management unit (PMU); and 5) radio and sensor interface [2]. The BSC must reset and control the processor on its own layer as well as the electronics on other layers. Since the mm-scale form factor prevents additional reset signals from being wirebonded between the layers, the BSC instead overrides the PMU to send a reset “command” to the other dies using the power supplies.

This is accomplished by manipulating power lines and secondary reset detector in each layer. Fig. 4.18 shows the operation of reset propagation in the system. As battery voltage is increased higher than  $V_{RELEASE}$ , RESET is released from BSC in CTRL CPU layer. RESET disables the 0.6 V supply being output from the PMU while the 1.2 V supply from the PMU remains enabled. Secondary reset detectors on the other layers detect this timing difference between the 0.6 V and 1.2 V supply and then reset their individual layers.



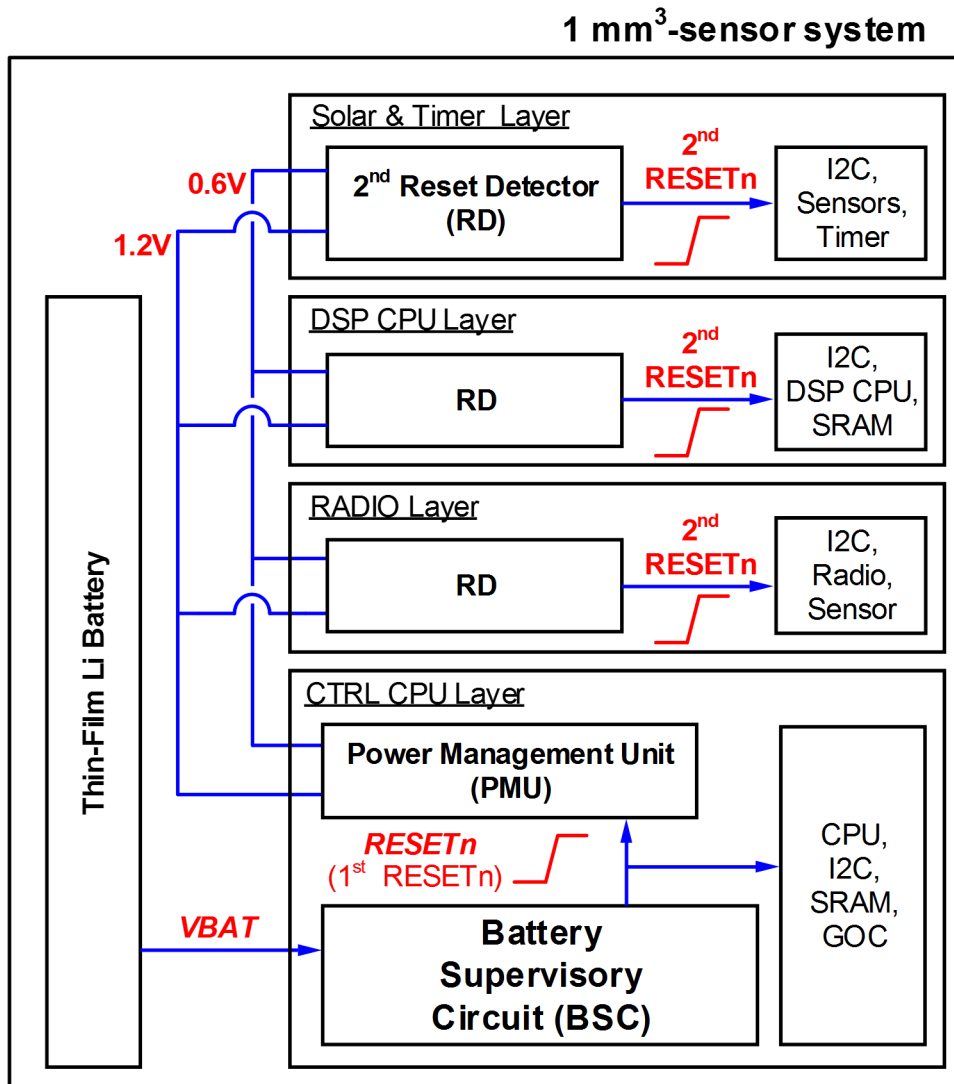
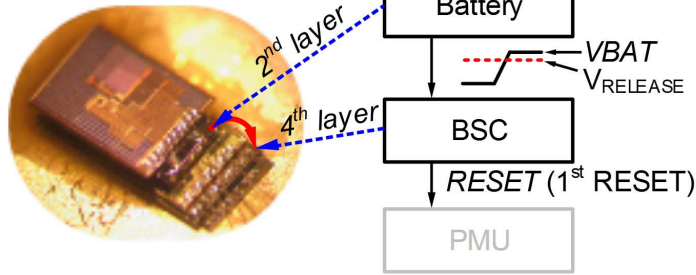
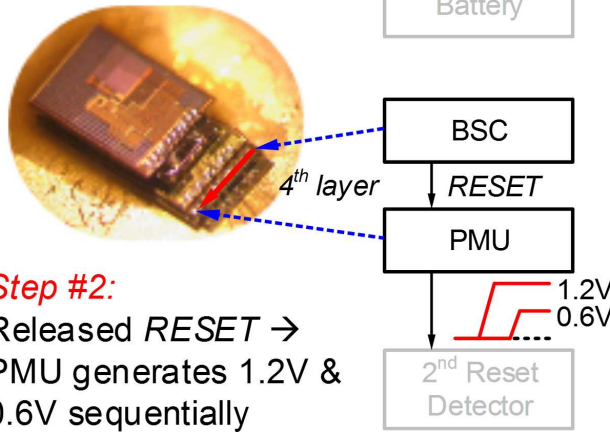


Figure 4.17: 1 mm<sup>3</sup>-sensor system where proposed BSC is integrated.

### 1 mm<sup>3</sup>-sensor system



**Step #1:**  
 $V_{BAT} > V_{RELEASE}$   
 $\rightarrow$  RESET is released



**Step #2:**  
 Released RESET  $\rightarrow$   
 PMU generates 1.2V &  
 0.6V sequentially



$\downarrow$  2<sup>nd</sup> RESET

**Step #3:**  
 Timing difference  
 between 1.2V & 0.6V  $\rightarrow$   
 2<sup>nd</sup> RESET is released

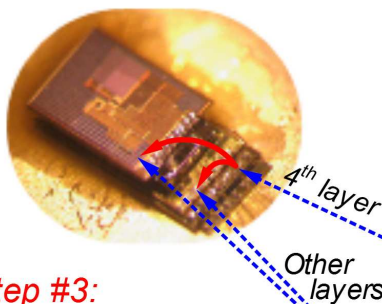


Figure 4.18: Reset propagation in 1 mm<sup>3</sup>-sensor system.

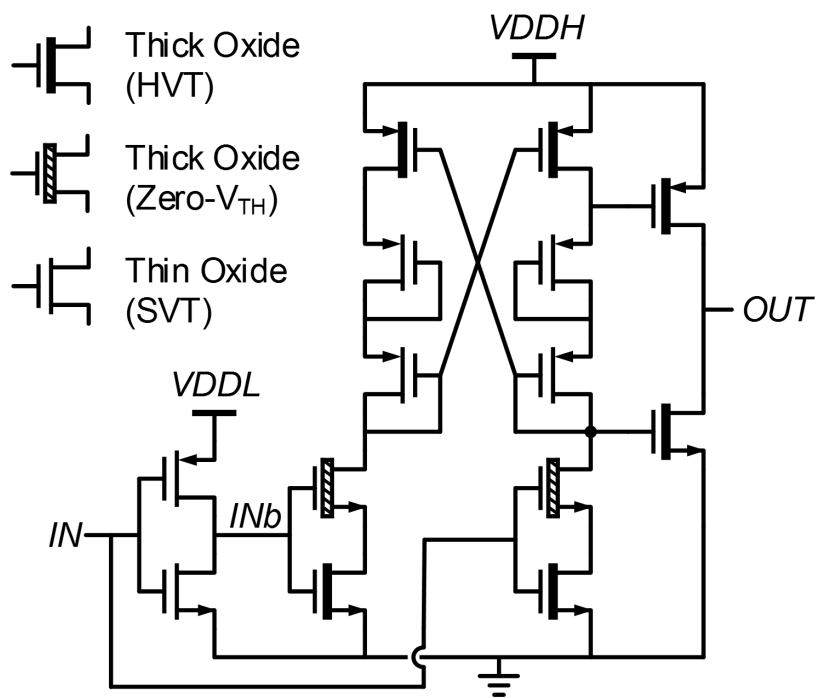


Figure 4.19: Conventional level converter.

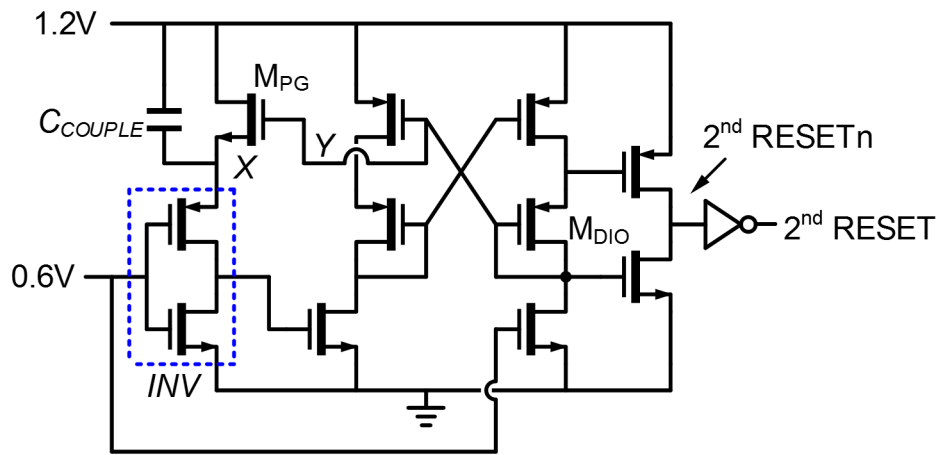
## 4.4.2 Secondary Reset Detector

The secondary reset detector is required to generate a reset signal for its own layer when 1.2 V is high and the 0.6 V supply is low. The desirable reset signal can be obtained from a conventional level converter [50] with modification. The conventional level converter (Fig. 4.19) powered by the 1.2V supply ( $V_{DDH}$ ) is able to provide a reset signal if the low-voltage differential inputs are properly applied. The low-voltage differential inputs are generated by an inverter powered by the lower supply voltage ( $V_{DDL}$ ). The same approach cannot be applied to the secondary reset detector since the 0.6 V supply is applied as both a power supply and also a signal. For example, when the 0.6 V supply is at 0 V, the differential input of the level converter becomes zero for both inputs.

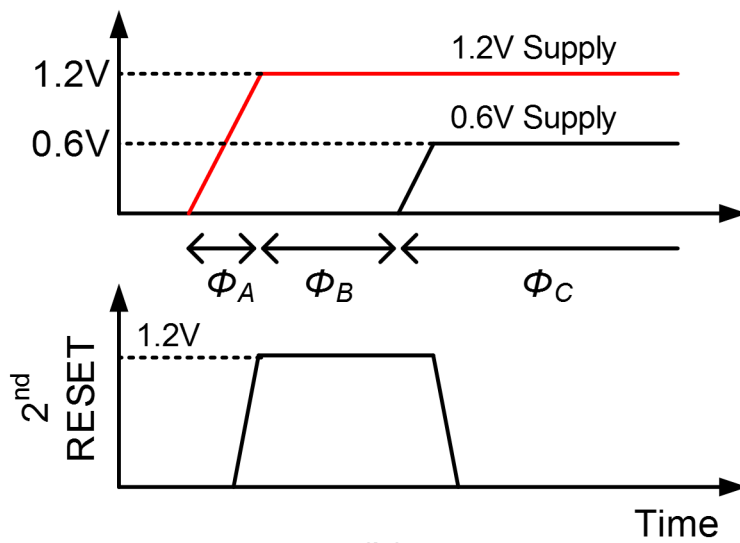
Thus, a new circuit is proposed for the secondary reset detector as shown in Fig. 4.20 (a). The problem in the conventional circuit is solved by a coupling capacitor ( $C_{COUPLE}$ ). It generates the supply voltage of the inverter (INV) that provides differential inputs to the level converter. Fig. 4.20 (b) shows the operation procedure. In the first phase ( $\Phi_A$ ), PMU increases the 1.2 V supply voltage, a coupling capacitor ( $C_{COUPLE}$ ) pulls up supply voltage of the inverter (voltage of node X,  $V_X$ ) to 1.2 V. The following level converter receives differential inputs with the help with INV, pulls up  $V_Y$  (voltage of node Y) by a latch, and triggers 2nd RESET (local).

However, in the second phase ( $\Phi_B$ ),  $V_X$  can be reduced by leakage current after long time. To hold  $V_X$  high enough to continuously operate the following circuit,  $M_{PG}$  is added in parallel with  $C_{COUPLE}$ .  $M_{PG}$  is turned on when  $V_Y > 'V_X + V_{TH,PG}'$ , where  $V_{TH,PG}$  is threshold voltage for  $M_{PG}$ . Here, required  $V_X$  is voltage that overwhelms the other input transistor of the differential pair and enables  $V_Y$  to be high. Considering voltage across a diode-connected transistor ( $M_{DIO}$ ),  $V_{DIO}$ , 1.2 V supply voltage needs to be higher than the required  $V_X$  by ' $V_{TH,PG} + V_{DIO}$ ' in order to guarantee the circuit operation even few seconds after high  $V_X$  is provided by coupling.

As PMU increases the 0.6 V supply, in the last phase ( $\Phi_C$ ), the 2nd RESET is released and  $V_Y$  becomes ground. If INV is powered by voltage higher than 0.6 V supply voltage, there will be short circuit current through INV since the input is the same as 0.6 V supply voltage. To prevent this issue,  $M_{PG}$  is turned off by  $V_Y$  and lowers  $V_X$  to ground. In this way, the proposed secondary reset detector in each layer propagates a reset signal from BSC with low power consumption.



(a)



(b)

Figure 4.20: Secondary reset detector (a) proposed reset detector (b) waveform.

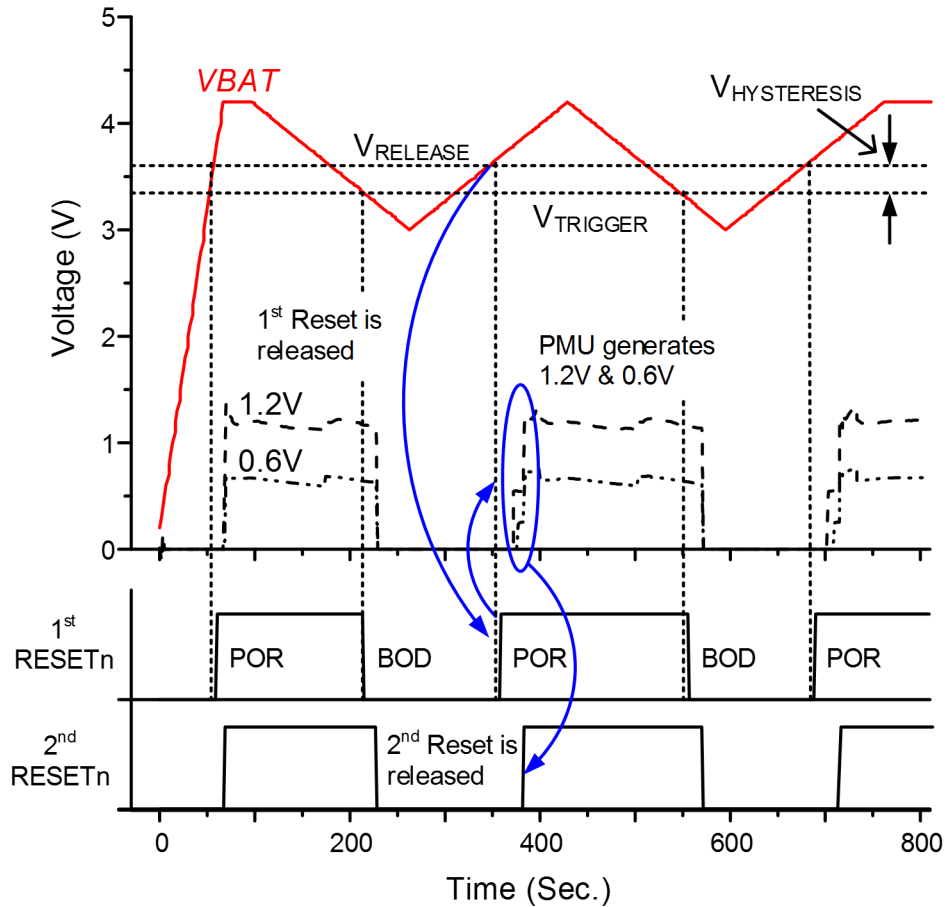
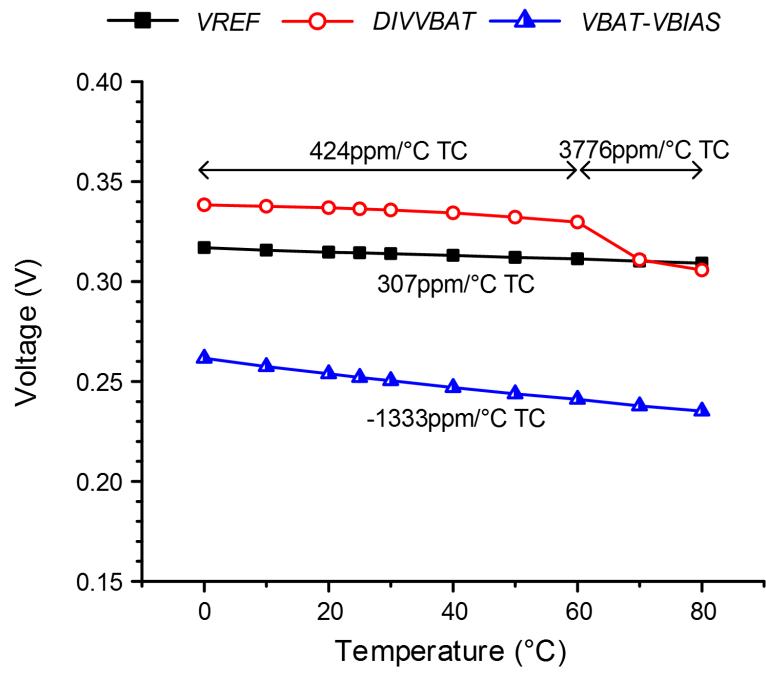


Figure 4.21: Measured operation of BSC and secondary reset detector in the complete sensor system.

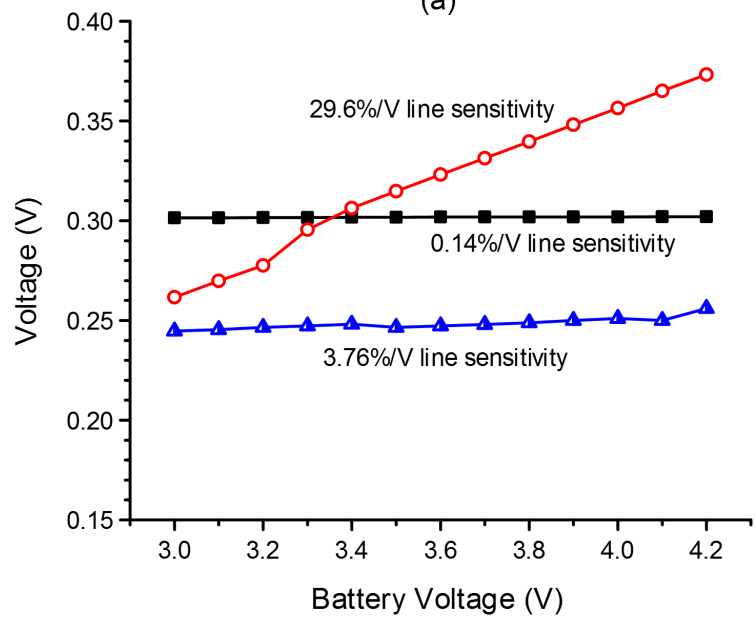
## 4.5 Experimental Results

Fig. 4.21 shows measured operation of the BSC and the secondary reset detector in the complete sensor system as observed in silicon under several different battery voltage behaviors. Good control of the primary and secondary reset signal is seen in all cases.

Fig. 4.22 shows measured  $V_{REF}$ ,  $V_{BIAS}$ , and  $DIVVBAT$  across temperature and battery voltage. The proposed two-stage voltage reference provides a stable  $V_{REF}$  over temperature and supply voltage variation ( $-307 \text{ ppm}/^\circ\text{C}$  temperature coefficient (TC) and  $0.14 \text{ %}/\text{V}$  line sensitivity). ' $V_{BAT}-V_{BIAS}$ ' has CTAT characteristic with the TC of  $-1333 \text{ ppm}/^\circ\text{C}$ , which mitigates increased tail current of preamplifier at high temperature by 31 %. Also, over supply voltage,  $V_{BIAS}$  tracks the battery voltage to maintain  $V_{SG}$  of the PMOS transistor controlling the tail current. ' $V_{BAT}-V_{BIAS}$ '



(a)



(b)

Figure 4.22: Measured  $V_{REF}$ ,  $DIVVBAT$ , and ' $V_{REF}-V_{BIAS}$ ' (a) temperature dependency (b) battery voltage dependency.

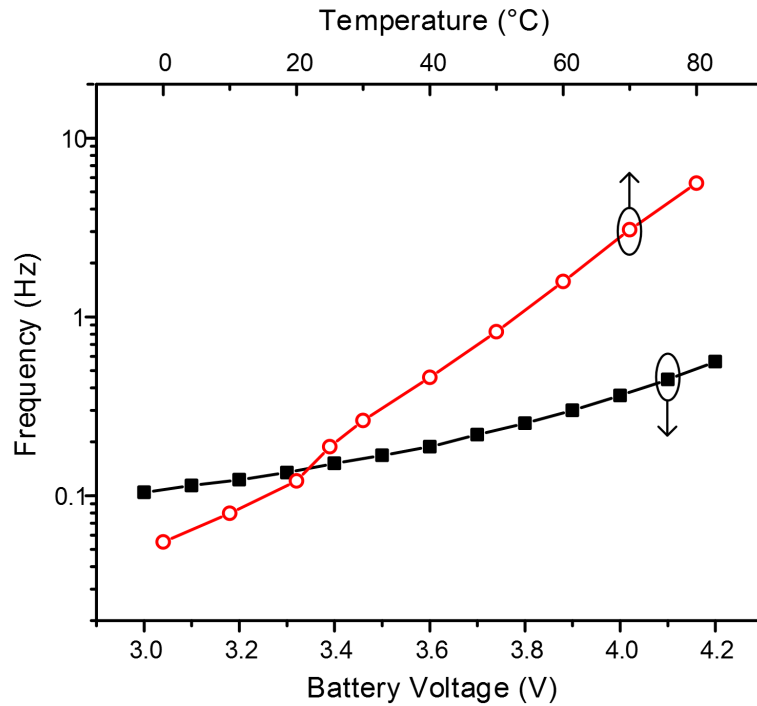


Figure 4.23: Measured operating frequency of oscillator over temperature and battery voltage.

has 3.76 %/V line sensitivity.

DIVVBAT shows rapid drop from 70 °C in Fig. 4.22 (a) while it scales well with the battery voltage, Fig. 22 (b). Its TC is 424 ppm/°C over 0-to-60 °C, but it becomes 3776 ppm/°C for 60-to-80 °C. This is possibly because uneven leakage current between n-well to p-substrate over the diode stacks. As will be seen in Fig. 4.24, DIVVBAT shifts  $V_{RELEASE}$  from 3.58 V to 3.71 V while moving  $V_{TRIGGER}$  from 3.35 V to 3.47 V. Since  $V_{HYSTERESIS}$  is maintained and  $V_{RELEASE}$  and  $V_{TRIGGER}$  are changed to higher value, it does not cause any issue such as system oscillation and circuit malfunction from low  $V_{BAT}$ . Although the sensor system will be started from and enter a reset state at higher  $V_{BAT}$ , it can be acceptable since most of charge is stored  $\sim 3.8$  V in a Li thin-film battery of the target application.

Fig. 4.23 displays CLK over temperature and the battery voltage. The frequency is decided by sub-threshold leakage current, transistor threshold voltage, and internal capacitance. Here, temperature affects both current and threshold voltage while supply voltage changes current only. Thus, the frequency of the leakage-based oscillator is more sensitive to temperature than supply voltage. Fast oscillator frequency results in increasing power consumption of the clocked comparator,



Table 4.1: Measured reset threshold voltages from 15 chips at 25 °C with different battery voltage transition speed.

	0.25mV/s Battery Voltage Transition		0.8MV/s Battery Voltage Transition	
	$\mu$	$\sigma$	$\mu$	$\sigma$
$V_{RELEASE}$	3.58	0.081	3.58	0.080
$V_{TRIGGER}$	3.36	0.066	3.36	0.064
$V_{HYSTERESIS}$	0.22	0.032	0.22	0.033

leading to higher power of the total BSC. Since most circuits in the target system are designed in sub-threshold region, power required for other circuits also increases with higher temperature. Therefore, the total power of the system is not limited by this BSC.

Fig. 4.24 shows measured parameters of the BSC. Fig. 4.24 (a) shows measured, constant battery voltage triggering low-battery-voltage protector output, LBVRST (Fig. 4.4), ( $V_{TH,LBVRST}$ ) across temperature with two different battery transition speeds (0.25 mV/s and 0.8 MV/s). Fig. 4.24 (b) gives measured  $V_{RELEASE}$ ,  $V_{TRIGGER}$ , and  $V_{HYSTERESIS}$  ( $V_{RELEASE}-V_{TRIGGER}$ ) across temperature with two different battery transition speeds. From 0 to 80 °C, both  $V_{RELEASE}$  and  $V_{TRIGGER}$  are increased by 3.6 % due to the diode-stack. However,  $V_{HYSTERESIS}$  is maintained  $\sim 230$  mV, which prevents the system oscillation from battery voltage drop.

$V_{HYSTERESIS}$  Results from 15 dies in Table 4.1 show these threshold voltages for two battery transition speeds at 25 °C and demonstrate tight spreads ( $<2.3\%$   $\sigma/\mu$ ) and excellent immunity from coupling to the battery ( $<20$  mV). Fig. 4.24 (c) offers POR delay as a function of final battery voltage and temperature, which is mainly determined by the period of the leakage-based oscillator. Profile of the delay is similar to the inverse of CLK frequency in Fig. 4.23. This is a desirable feature since the circuits designed in sub-threshold region are stabilized in shorter time by operating faster as temperature and supply voltage increase.

Fig. 4.25 gives the measured average power consumption over 15 dies across temperature and battery voltage, and includes the power breakdown for each component based on simulation. As the clock frequency increases, power consumption from the oscillator itself and the clocked comparator go up. Thus, the power consumption graph is considerably analogous to the CLK

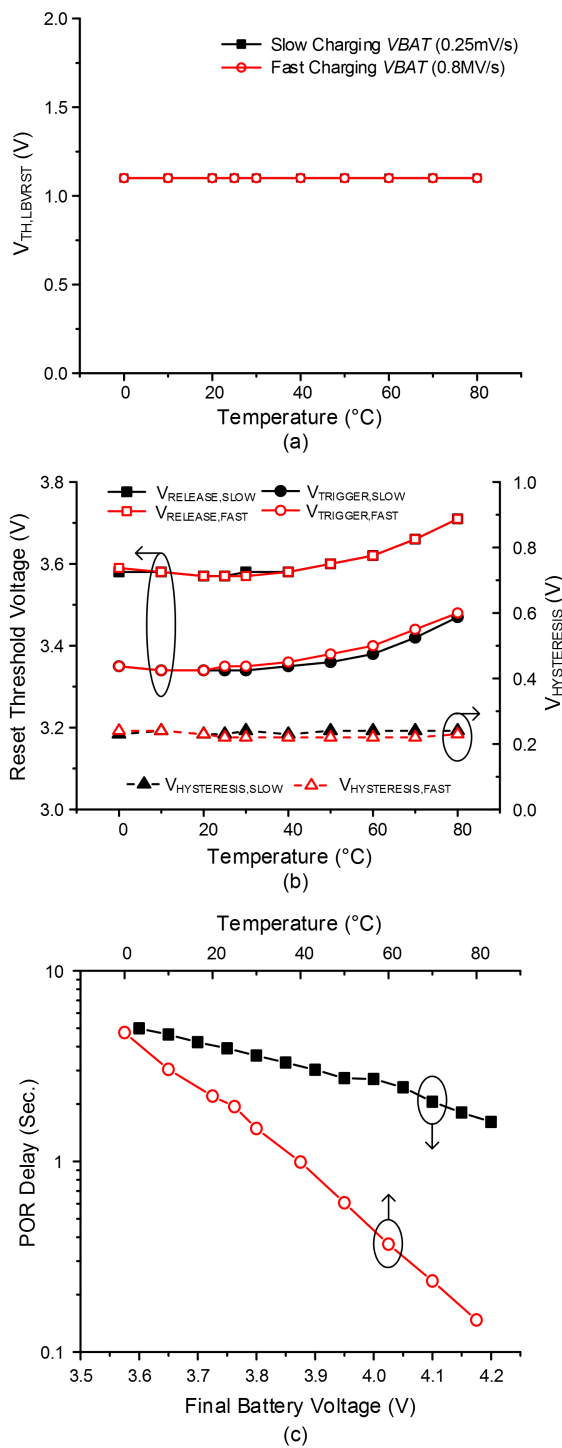
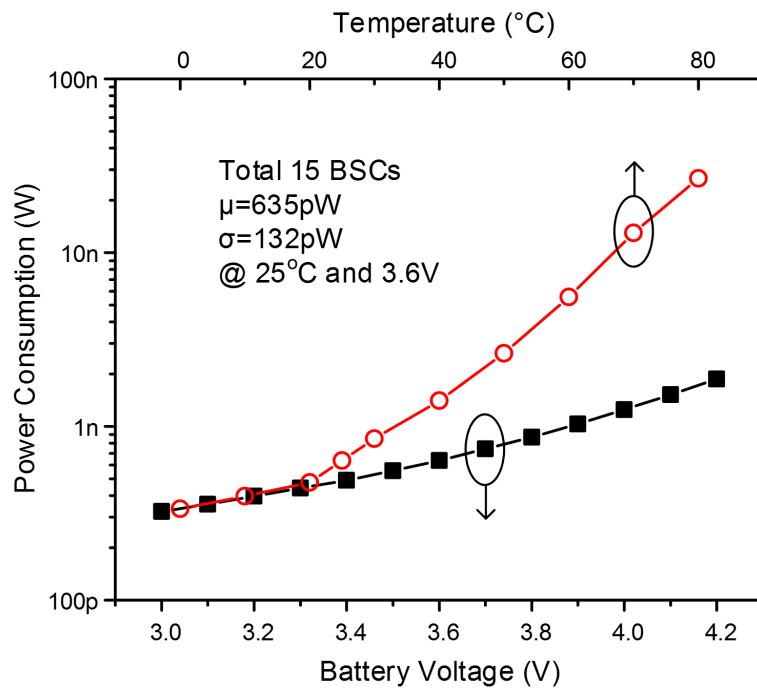
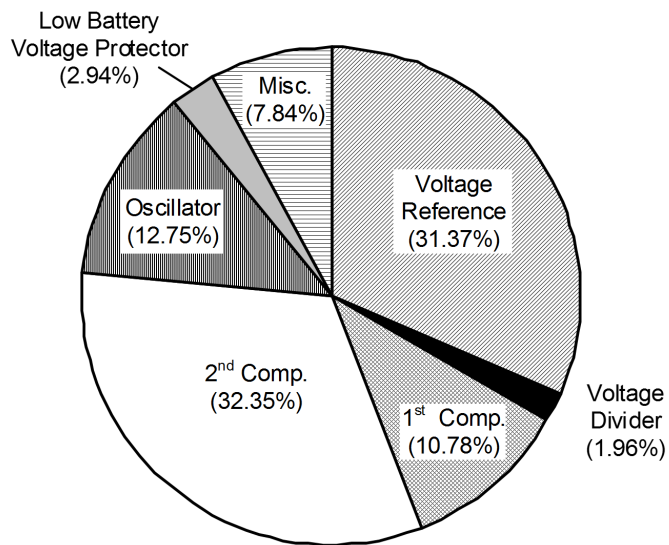


Figure 4.24: Measured parameters of BSC (a)  $V_{TH, LBVRST}$  over temperature from different battery voltage transition speed (0.25 mV/s and 0.8 MV/s) (b)  $V_{TRIGGER}$ ,  $V_{RELEASE}$ , and  $V_{HYSTERESIS}$  over temperature from different battery voltage transition speed (0.25 mV/s and 0.8 MV/s) (c) POR delay over temperature and battery voltage.



(a)



(b)

Figure 4.25: Power consumption of BSC (a) Average power consumption from 15 chips over temperature and battery voltage (b) Power breakdown at 25 °C and 3.6 V.

Table 4.2: Performance summary of the proposed BSC and comparison to other prior works.

	This Work	[50]	[55]	[43]	[44]	[45]	[46]	[47]
Process	180 nm	90 nm	180 nm	N/A	N/A	N/A	N/A	N/A
Supply Voltage	3.6 V	1.0 V	1.8 V	3.0 V	0.9 V	1.8 V	1.2 V	3.6 V
Power	635 pW	540 nW	3.6 $\mu$ W	1.5 $\mu$ W	135 nW	225 nW	210 nW	1.8 $\mu$ W
POR Delay	1.94 sec.	150 ns	100 ms	185 ms	200 ms	14.2 ms	270 ms	15 ms
$V_{\text{HYSTERESIS}}$	200 mV	432 mV	N/A	6.3 mV	11 mV	7.88 mV	31.6 mV	20 mV
Comments	3.6 V supply voltage is chosen for fair comparison	Voltage reference's power is not included.	$V_{\text{RELEASE}}$ is not available	Commercial Product				

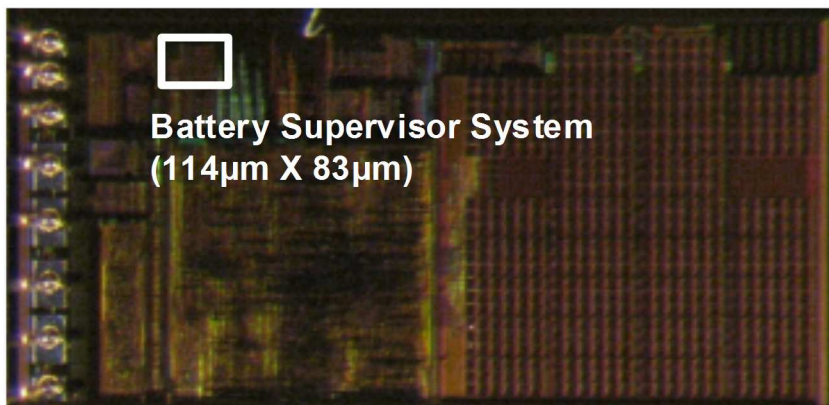
frequency in Fig. 4.20 (c) over temperature and the battery voltage.

The die photo and comparison to recent work are shown in Fig. 4.26 and Table 4.2, respectively. The POR delay of the proposed BOD is longer than typical, which was desirable to allow the ultra-low power PMU of the  $1\text{mm}^3$  sensor node to stabilize. The designed BSC consumes  $213\times$  lower power than prior art, enabling its use in general miniaturized battery-operated and harvesting-capable nodes with aggressive power budgets.

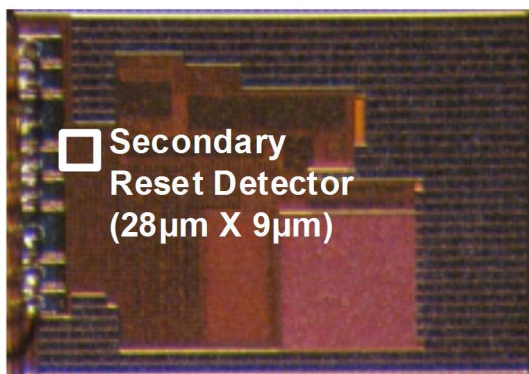
## 4.6 Summary

This work demonstrates a low-power battery supervisory circuit (BSC) integrated with a complete  $1\text{mm}^3$  sensor system. Providing power-on reset and brown-out detection, the BSC fabricated in 180 nm CMOS consumes 635 pW at 3.6 V supply voltage, which is  $213\times$  reduction over the best prior work. This ultra-low power is achieved using a 57 pA, fast stabilizing two-stage voltage reference and an 81 pA leakage-based oscillator and clocked comparator. The two-stage voltage reference has a stacked reference preconditioner that generates a supply voltage for the second reference stage. It improves settling speed of the reference voltage by removing a decoupling capacitor, which is required in the conventional 2T leakage-based voltage reference due to noise

**CTRL CPU Layer in the mm<sup>3</sup>-scale sensor**



**Battery Supervisor System**  
(114µm X 83µm)



**Secondary Reset Detector**  
(28µm X 9µm)

**Solar & Timer Layer**  
Example of other layers that include secondary reset detectors

Figure 4.26: Die photograph.

purpose. The 0.2 Hz clock signal from the oscillator is shared for the clocked comparator and delay generation for power reduction. The clock signal is used in the clocked comparator to convert low output voltage from the preamplifier to high battery voltage. Once the comparator detects enough high battery voltage, the clock is reused to make a sufficiently long minimum power-on-reset delay of 0.8 sec. Moreover, the BSC is tested combined with a complete 1 mm<sup>3</sup> sensor system. It controls the reset functionality of electronics on its own die as well as orchestrates the reset of other chips by modulating power supply voltages that are monitored by secondary reset detectors on those dies.

## CHAPTER 5

# A Low Power Battery Supervisory Circuit with Adaptive Battery Health Monitor

### 5.1 Introduction

Wireless sensor nodes often include an energy harvester that takes energy from a source (e.g., solar cell) and transfers it to a battery (Fig. 5.1). Battery voltage ( $V_{BAT}$ ) varies over time depending on the amount of harvested energy vs. system energy consumption. To avoid unpredictable circuit behavior, a battery supervisory circuit (BSC) monitors  $V_{BAT}$  and only enables the system when  $V_{BAT}$  exceeds a certain threshold. Conventional BSCs [44,48,55] typically include a  $V_{BAT}$  divider, voltage reference, comparator, and delay generator (Fig. 5.1 bottom). The divided  $V_{BAT}$  ( $V_{DIV}$ ) is compared to a predetermined threshold voltage ( $V_{TH}$ ) (generated using a voltage reference) by a comparator. The output (compout) either immediately disables the sensor system or enables it after a delay that provides stabilization time to the circuits.

To prevent oscillation, conventional BSCs employ two fixed threshold voltages, controlled by an enable signal (Fig. 5.1). The lower threshold voltage,  $V_{DISABLE}$ , sets the lowest  $V_{BAT}$  voltage at which circuits operate properly. The higher threshold voltage,  $V_{ENABLE}$ , provides hysteresis ( $V_{HYST} = V_{ENABLE} - V_{DISABLE}$ ) to prevent the system from oscillating between enabled and disabled modes.

In a battery-operated system, the required  $V_{HYST}$  value is directly related to the battery internal resistance ( $R_{BAT}$ ). When  $V_{BAT}$  first reaches  $V_{ENABLE}$  and the sensor node turns on, the additional

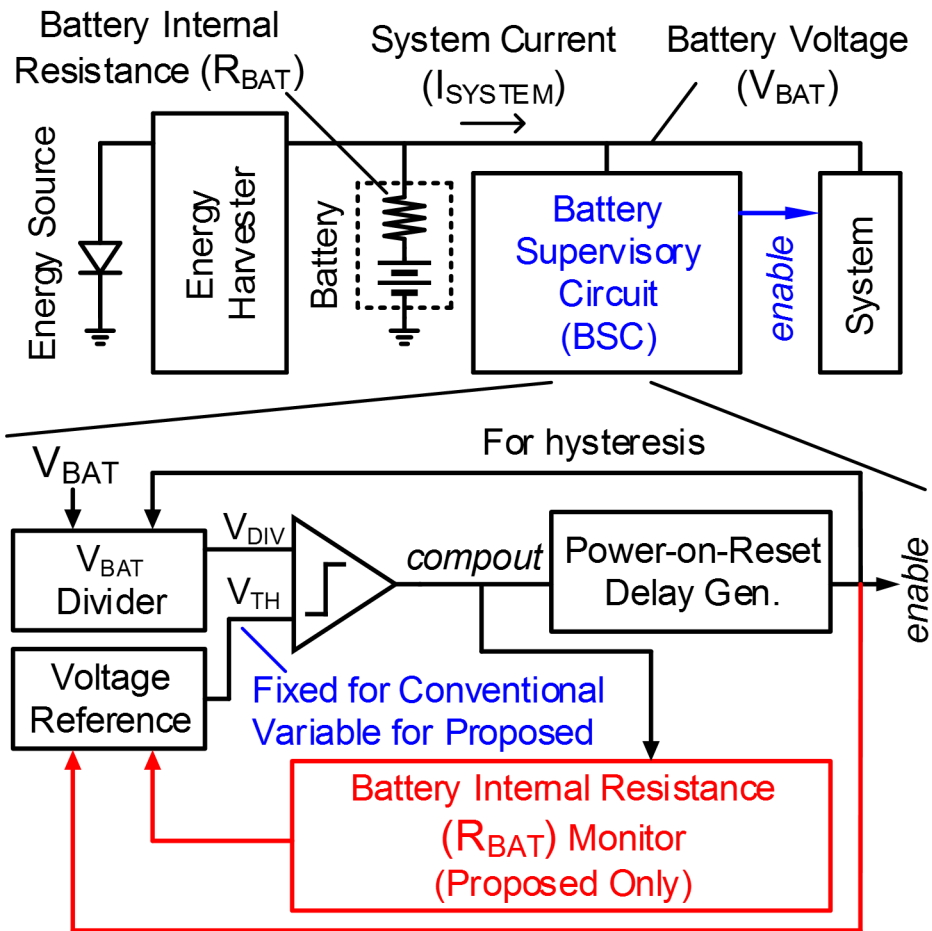


Figure 5.1: Battery supervisory circuit (BSC) for a wireless sensor node (Red: Proposed only).



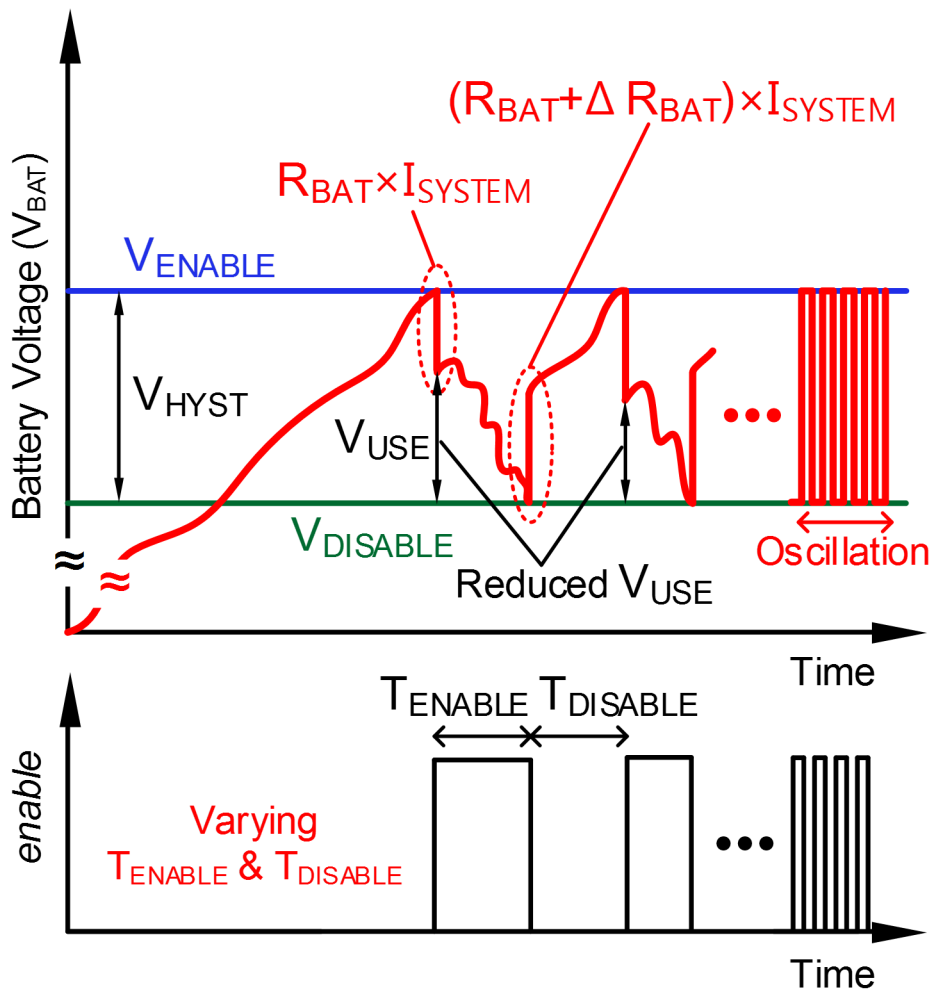


Figure 5.2: Operation of conventional BSC with fixed-threshold voltages.

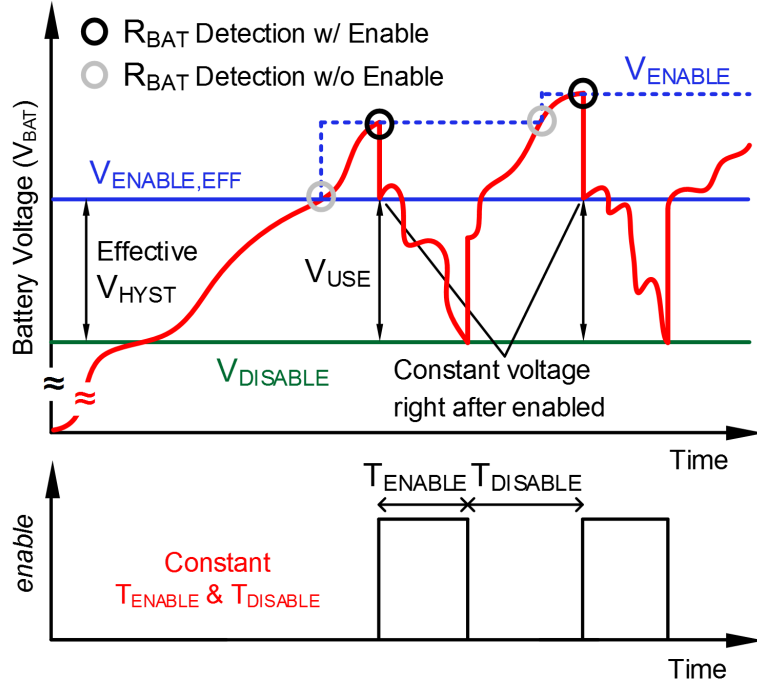


Figure 5.3: Operation of proposed BSC with adaptive-threshold voltage ( $V_{ENABLE}$ ).

current draw from the system ( $I_{SYSTEM}$ ) causes an immediate  $I_{SYSTEM} \times R_{BAT}$  battery voltage drop. Conversely, when the system is disabled, the reduced  $I_{SYSTEM}$  creates an upward spike in  $V_{BAT}$ . If these IR spikes exceed  $V_{HYST}$ , the system will oscillate (Fig. 5.2).

Miniature wireless sensor nodes are unique in that they employ very small batteries with high  $R_{BAT}$ , e.g., 7 k $\Omega$  [51], leading to large IR drops. Battery health declines with discharge cycles, increasing  $R_{BAT}$  (e.g., from 7 ~ 31 k $\Omega$  over 1000 cycles [51]) and is also temperature dependent [56]. As a result, the current BSC approach requires a large  $V_{HYST}$  to accommodate the worst-case  $R_{BAT}$  over its lifetime, which both delays system turn-on time and reduces the usable range of battery voltages ( $V_{USE}$ ) over which the system can operate.

## 5.2 Proposed BSC

We propose a new BSC that dynamically modifies  $V_{ENABLE}$  (and hence  $V_{HYST}$ ) to adapt to the varying  $R_{BAT}$ , obtaining an  $V_{ENABLE,EFF}$  that is constant and independent of  $R_{BAT}$  (Fig. 5.3). When  $V_{BAT}$  reaches  $V_{ENABLE}$ , the  $R_{BAT}$  monitor first measures  $R_{BAT}$  by inducing a test current using decoupling capacitors and measuring the RC response.  $V_{ENABLE}$  is then updated to

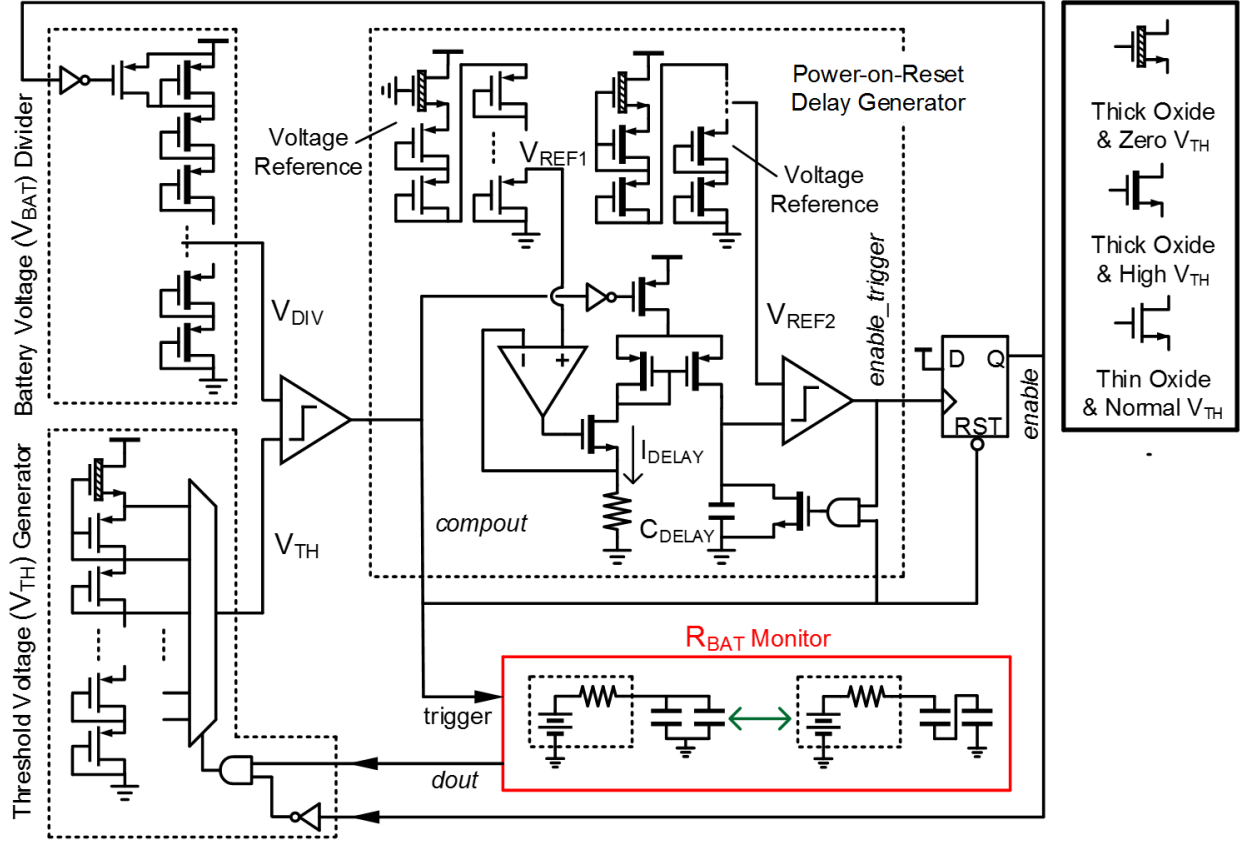


Figure 5.4: Circuit diagram of proposed BSC with  $R_{BAT}$  monitor.

' $V_{ENABLE,EFF} + R_{BAT} \times I_{SYSTEM,MAX}$ ' using a low-power divided voltage reference.  $V_{BAT}$  is compared against the new  $V_{ENABLE}$  and enabled if  $V_{BAT} > V_{ENABLE}$ . Otherwise, the system waits for  $V_{BAT}$  to increase until  $V_{BAT} > V_{ENABLE}$ , at which point the process repeats. This approach ensures that  $V_{BAT}$  remains higher than  $V_{ENABLE,EFF}$  after the system is enabled. The technique requires knowledge of  $I_{SYSTEM,MAX}$ , which is feasible in small wireless systems that typically have well-defined operation. In the proposed approach, the effective  $V_{HYST} = V_{ENABLE,EFF} - V_{DISABLE}$  and is independent of  $R_{BAT}$ . Hence,  $V_{HYST}$  does not need to be margined for changes in  $R_{BAT}$ , maximizing the useable voltage range over system lifetime.

Fig. 5.4 shows the proposed BSC circuit diagram. The  $V_{BAT}$  divider uses 65 diode-connected PMOS transistors that give a division ratio of 3.25 / 3.05 when enable = 0 / 1. The  $V_{TH}$  generator includes a leakage-based voltage reference/divider and provides 64 possible analog reference voltages from 1.06 V to 1.28 V for the adaptive  $V_{TH}$ . This reference consumes 77 pA while providing 319 ppm/ $^{\circ}$ C TC and 0.17 %/V line sensitivity. It is constructed with a zero- $V_{TH}$  NMOS

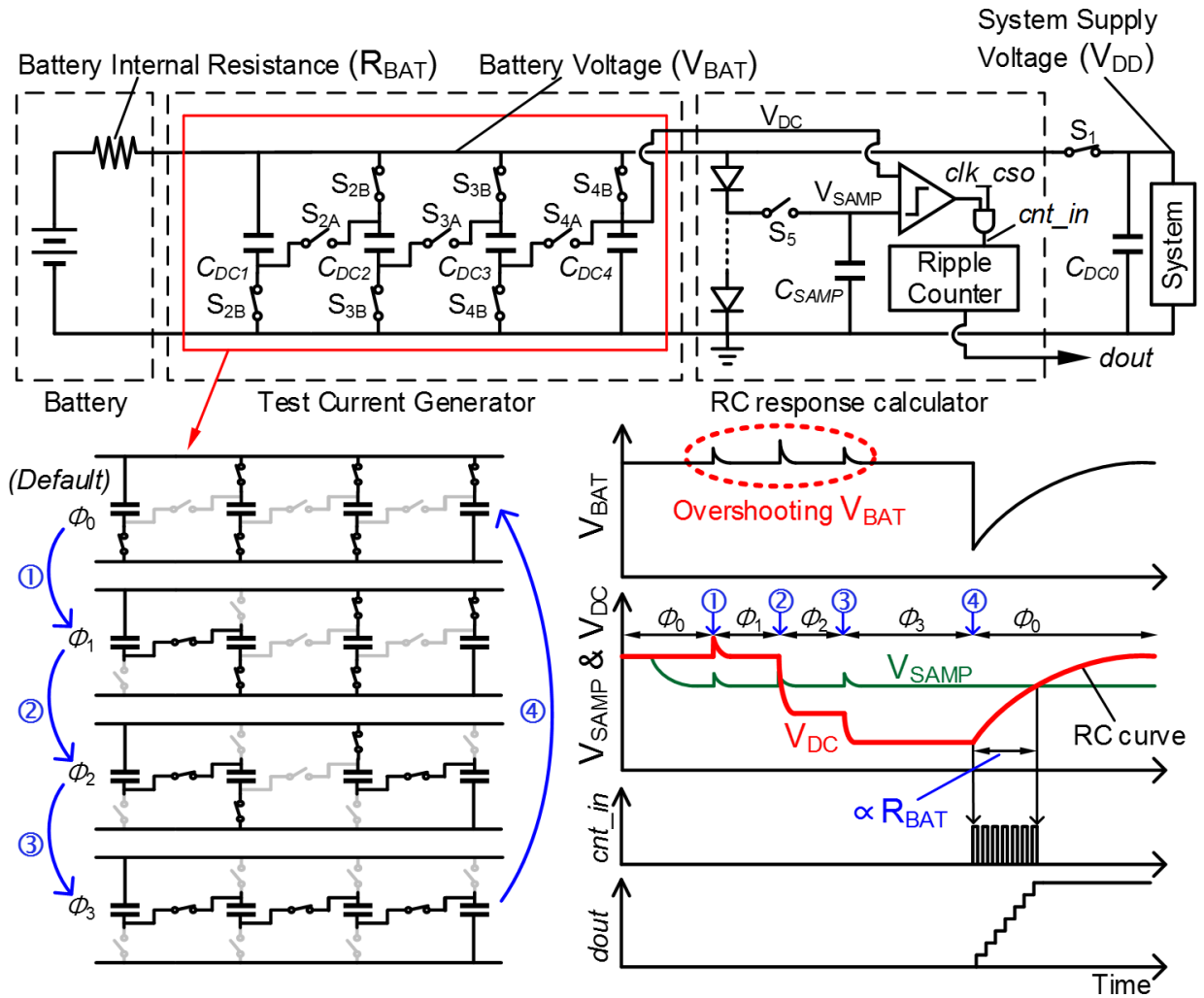


Figure 5.5: Circuit diagram and operation of proposed  $R_{BAT}$  monitor.

transistor for leakage generation at the top of a stack and diode-connected PMOS transistors that provide multiple outputs. When  $V_{DIV} > V_{TH}$ , the  $R_{BAT}$  monitor is triggered and produces  $dout$  (6-bit code), which updates the  $V_{TH}$  generator based on the current  $R_{BAT}$  value. If this causes  $V_{DIV} < V_{TH}$ ,  $enable\_trigger$  will remain low since  $R_{BAT}$  detection (17.8 ms) is much faster than the power-on-reset (PoR) delay ( $>50ms$ ).

Fig. 5.5 shows the proposed  $R_{BAT}$  monitor including the test current generator and RC response calculator. The test current generator operates by first placing decoupling capacitors in series to discharge them (Steps 1-to-3). This is done gradually to avoid  $V_{BAT}$  overshoot, which can damage circuits in the system. In the final step (4) all capacitors are placed in parallel simultaneously, creating a large current draw from the battery. This results in an RC voltage curve on  $V_{BAT}$  with a

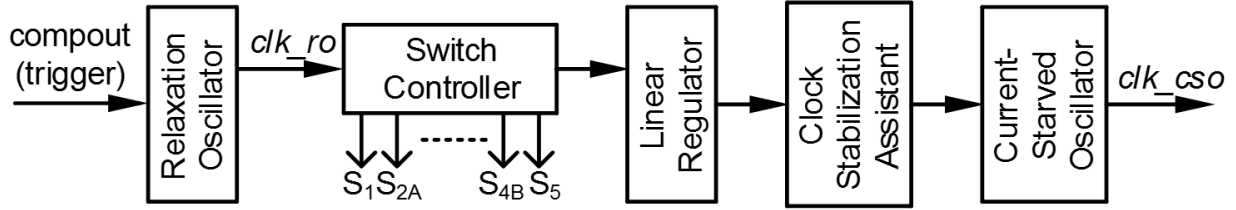


Figure 5.6: Clock and control signal generation for  $R_{BAT}$  monitor.

time constant of  $R_{BAT} \times (C_{DC,i})$ . This time constant is measured by comparing  $V_{DC}$  with its earlier sampled and divided version  $V_{SAMP}$ . A fast ripple counter quantifies the time when  $V_{DC} < V_{SAMP}$ . Since  $V_{SAMP}$  is relative to  $V_{BAT}$ ,  $dout$  is insensitive to  $V_{BAT}$ .

Note that switch  $S_1$  is open during Step 4, protecting the system from the test-induced voltage drop. Since the system operates from a decoupling capacitance during this time, the test event is kept short ( $< 65 \mu s$ , measured). Note that the test capacitors ( $C_{DC1}-C_{DC4}$ ) act as standard decoupling capacitors in normal operation. The test chip implementation uses 8 test capacitors to limit  $V_{BAT}$  overshoot to 5.6 % of  $V_{BAT}$  (measured). Fig. 5.6 describes clock generation, which includes a slow clock generator for Steps 1-to-3 and a fast clock generator for counting  $dout$ . The fast clock generator runs off a supply regulator that isolates it from the test-induced voltage drop on  $V_{BAT}$ .

The delay generator (Fig. 5.4) uses a voltage reference ( $V_{REF1}$ ) to drive a current source ( $I_{DELAY} = 3.3 \text{ nA}$ ). This charges a capacitor ( $C_{DELAY}$ ) that is compared to a second (configurable) voltage reference ( $V_{REF2}$ ) to set the PoR delay. Reference  $V_{REF1}$  compensates the TC of the resistor, resulting in a temperature insensitive delay (0.9

### 5.3 Measurement Results

Fabricated in 180 nm CMOS, the BSC was tested with a miniature  $2 \mu\text{Ah}$  thin-film battery ( $1.375 \times 0.85 \text{ mm}^2$ ) and a sensor system with  $I_{SYSTEM,MAX} = 11 \mu\text{A}$ . The BSC draws 1 nA during battery monitoring and 10 nJ/conv. for  $R_{BAT}$  detection. Fig. 5.7 shows measured  $V_{TH}$  waveforms as it adjusts to  $R_{BAT}$  detection. Fig. 5.8 shows measured  $dout$  and  $V_{ENABLE}$ , demonstrating good matching across battery resistance. Fig. 5.9 shows a 500 cycle test of the BSC with the  $2 \mu\text{Ah}$  battery, showing measured change in  $R_{BAT}$  from 16 k $\Omega$  - 54 k $\Omega$ . The BSC has a maximum  $V_{HYST}$  tracking error of 27 mV. Assuming 50 mV margin, the proposed system requires an effec-

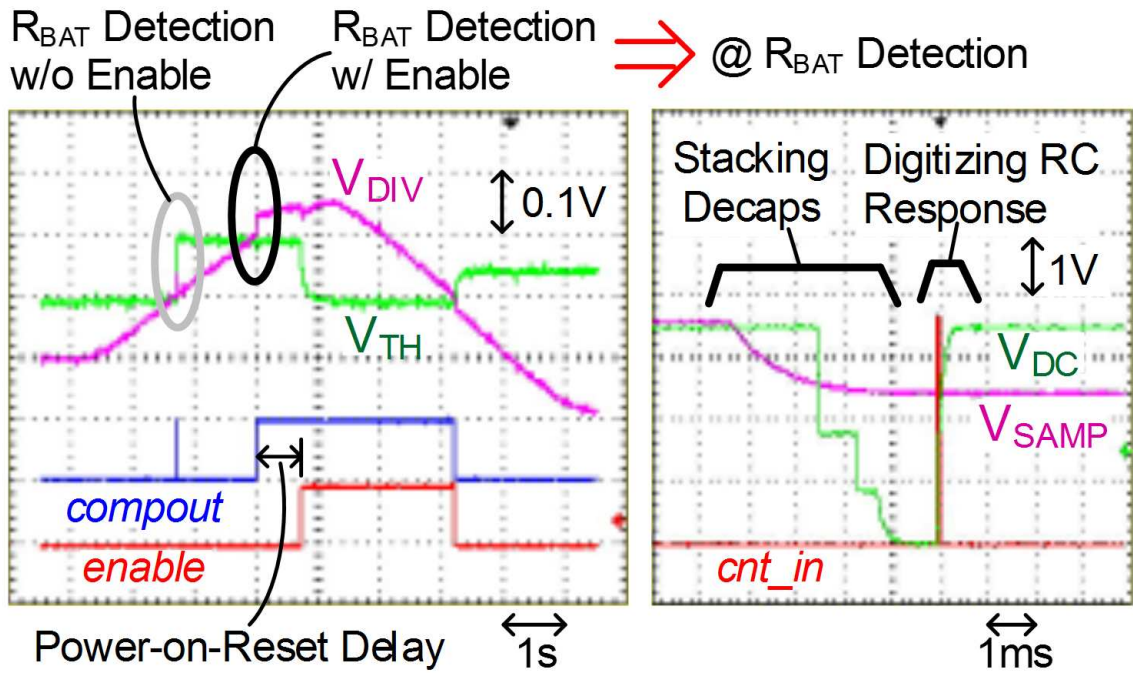


Figure 5.7: Measured oscilloscope waveforms.

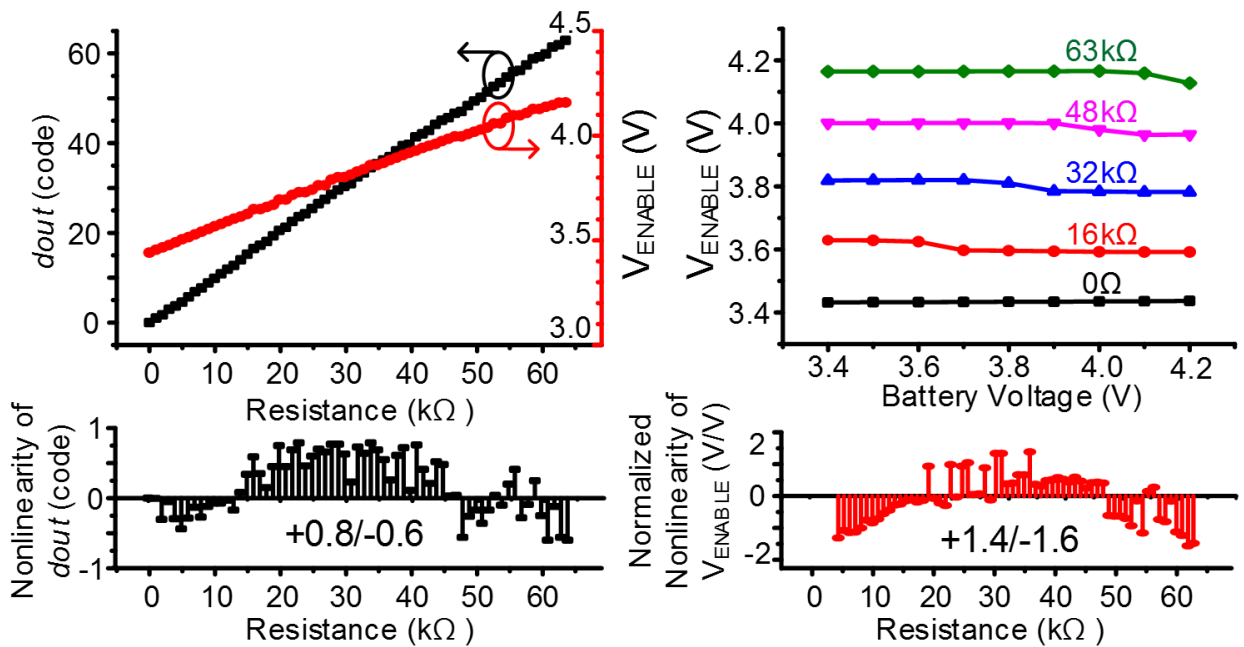


Figure 5.8: Measured  $dout$  &  $V_{ENABLE}$  over  $R_{BAT}$  &  $V_{BAT}$ .

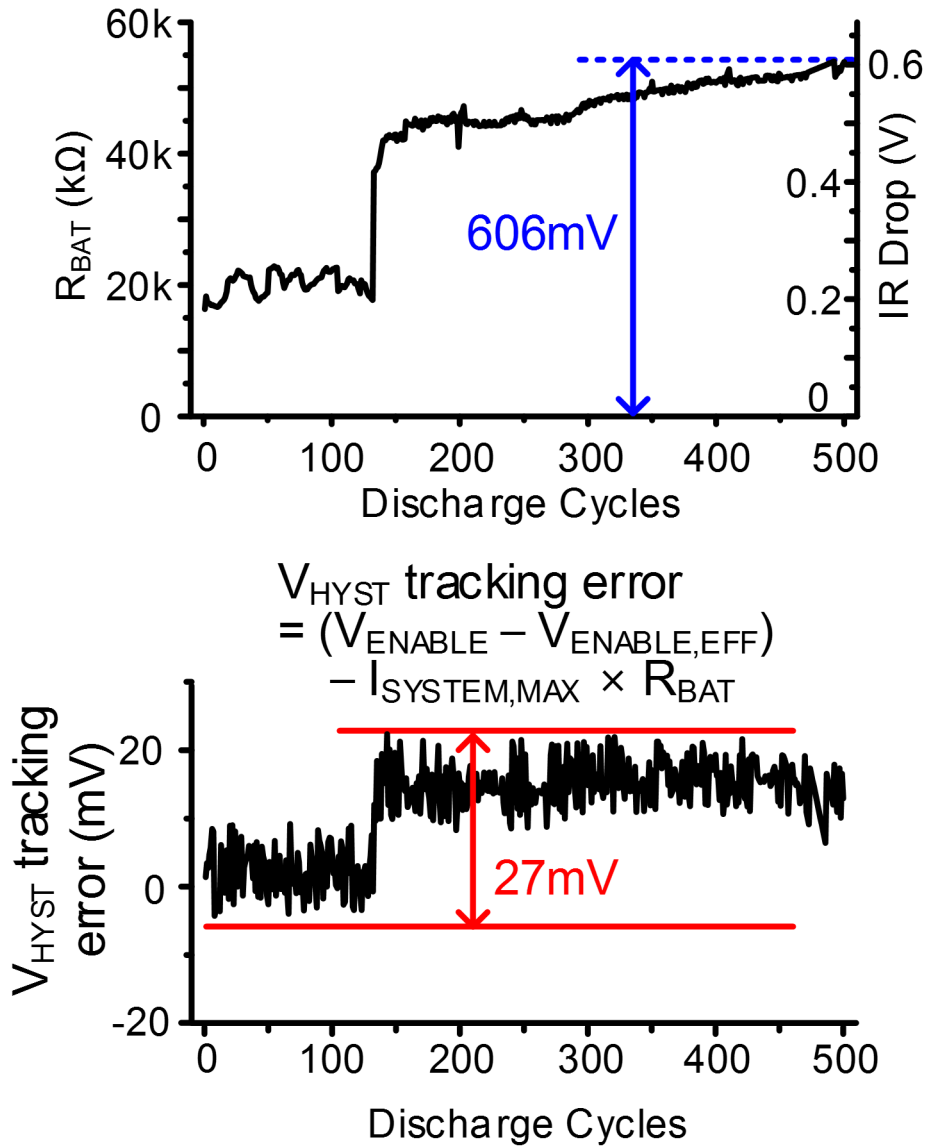


Figure 5.9: Measured  $R_{BAT}$  over discharge cycles &  $V_{HYST}$  tracking error.

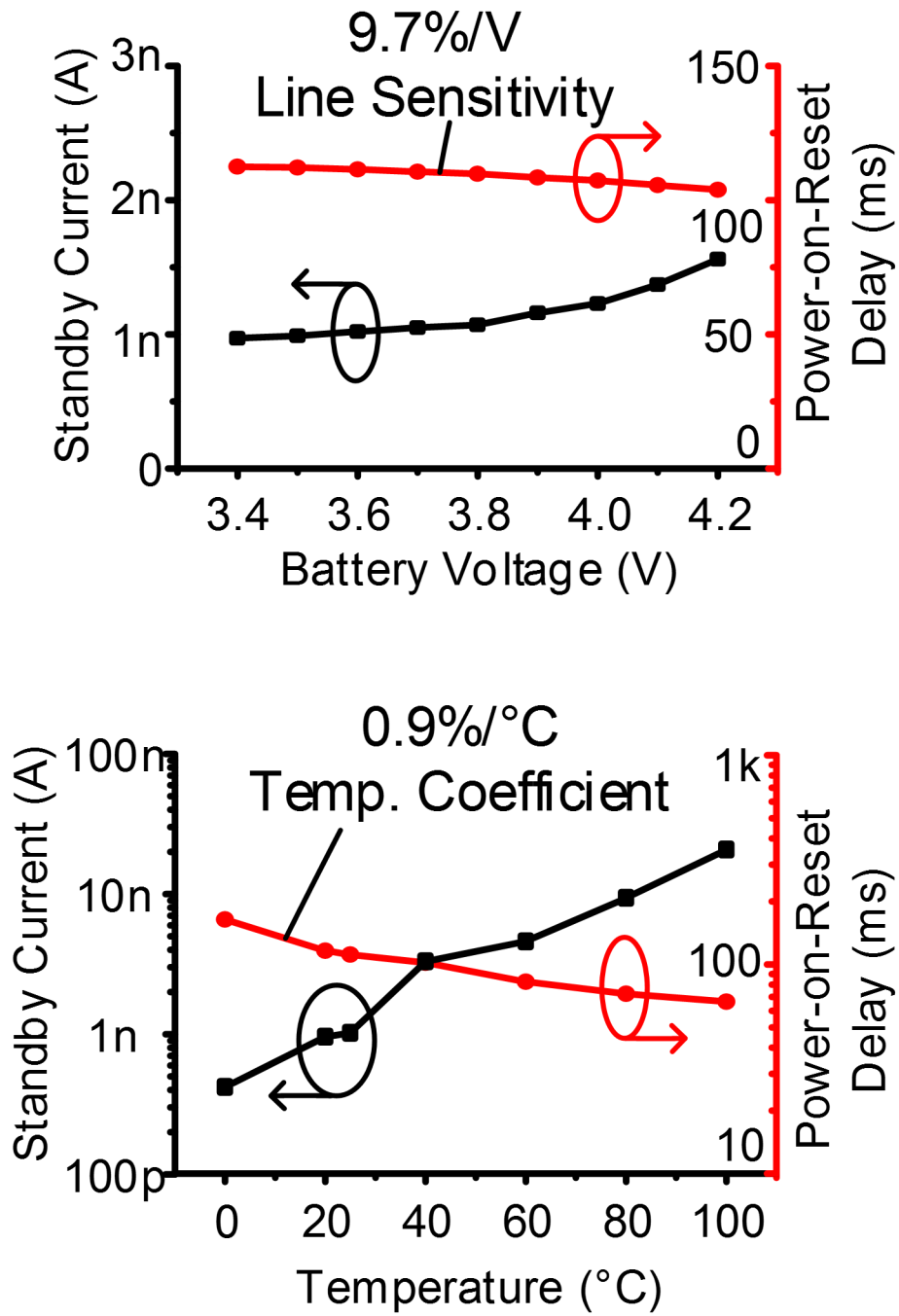


Figure 5.10: Measured standby power & power-on-reset delay.



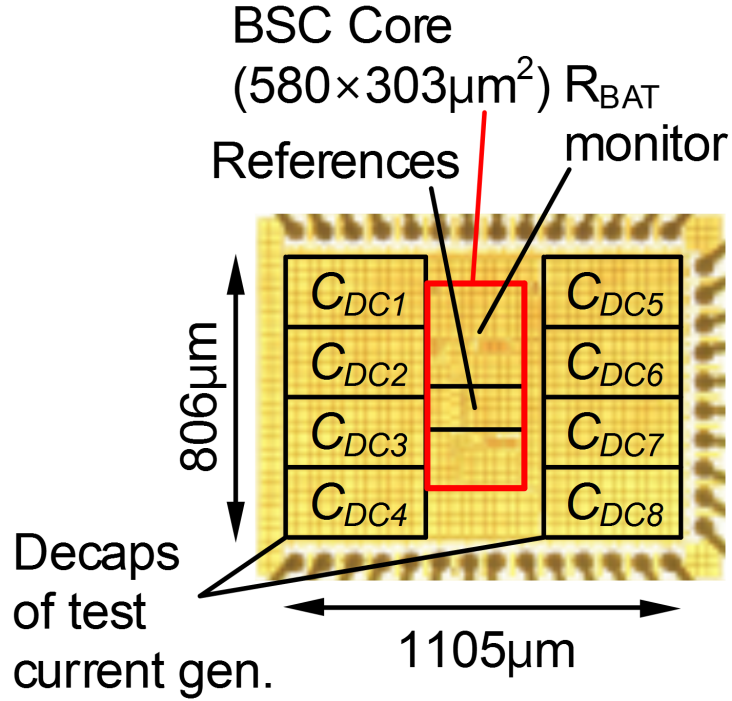


Figure 5.11: Die photo.

Table 5.1: Performance summary of the proposed adaptive BSC and comparison to other prior works.

	This Work	[55]	[48]	[44]
Process (nm)	180	180	180	N/A
Current (A)	1 n	1 $\mu$	176 p	150 n
PoR Delay (Sec.)	0.05 – 0.5 <sup>†</sup>	0.5	1.9	0.2
$V_{\text{HYST}}(\text{mV})^{\dagger\dagger}$	77	656		
Threshold Voltage	Adaptive to $R_{\text{BAT}}$	Fixed w/o considering $R_{\text{BAT}}$		

<sup>†</sup>Programmable

<sup>††</sup>50mV margin added

tive  $V_{HYST} = 50 + 27 = 77$  mV. In comparison a conventional BSC requires 656 mV hysteresis to accommodate the worst-case  $R_{BAT} = 54$  k $\Omega$  condition after 500 cycles. The proposed BSC therefore provides  $2.7\times$  usable battery voltage range ( $V_{BAT}$  min/max = 3.2 V / 4.2 V). Fig. 5.10 shows standby-mode power and PoR delay. Figs. 5.11 and 5.1 show the die photo and a performance summary with comparison table.

## 5.4 Summary

This section proposed a battery supervisory circuit (BSC) for wireless sensor nodes that automatically adapts to varying battery health, as reflected by its internal resistance ( $R_{BAT}$ ), and establishes a constant effective threshold voltage. Compared to a conventional fixed-threshold BSC, the new design avoids oscillation and widens the usable range of battery voltages, independent of  $R_{BAT}$ .  $R_{BAT}$  is measured by inducing a test current using decaps and measuring the resulting battery RC response time. When tested with a 2  $\mu$ Ah battery and 11  $\mu$ A sensor system, the BSC reduces the required hysteresis from 656 mV to 77 mV, increasing the usable battery voltage range by  $2.7\times$ .

## CHAPTER 6

### Conclusion

Miniature sensor nodes have recently enabled new application spaces in VLSI. In the continuation of Bell's Law, the size of computing systems have been shrunk down to cubic-millimeter scale (e.g. Michigan micro-mote). Especially, since the term "Smart Dust" was coined, rapid advances in low-power wireless sensor nodes have been driving the realization of Internet of Things. With a unique feature set such as wireless communication, energy harvesting, the small form-factor, thus enabling non-invasive and secure placement, the sensor nodes have been developed for a number of applications such as medical, infrastructure, and surveillance.

There are many challenges to realize miniature sensing systems. One of the most critical challenges is the small battery storage capacity; the maximum physical battery size is severely limited, so is the battery storage capacity. As a result, low-power circuit design and energy harvesting techniques need to be investigated to allow the system operation within a very small power budget. In these miniature sensing systems, there are four different energy flows: 1) energy harvested from a source to the battery; 2) power delivery circuits; 3) always-on circuits; 4) duty-cycled circuits. Available energy from the source of the harvester changes depending on the environmental condition, and the load current also changes considerably due to the duty-cycled operation. In such a dynamic system, an optimization of the energy harvester and the power converter is a key issue. In order to minimize the average power consumption to achieve a longer lifetime, always-on circuits should be designed to meet the extremely low standby power requirement of the system. Also, duty-cycled circuits need to be power-gated to keep the low standby power. In this dissertation, several new circuits were discussed that satisfy those requirements.

First, in Chapter 2, two different energy-efficient oscillators that can be used for power converters were discussed. They are based on a leakage-based oscillator where the intermediate voltage region that causes a short-circuit current is quickly restored to the full-rail voltage, and the amount of the cell delay is determined by charging/discharging the internal nodes through the leakage. Also, the oscillators provide wide frequency range without any loss in energy efficiency thanks to a current feeding scheme with gate voltage control. From the fabricated test chip, the proposed Constant Energy-per-Cycle Ring-Oscillator (CEpCRO) achieves the constant energy-per-cycle of 0.8 J/cycle in 21 Hz  $\sim$  60 MHz, which is more energy-efficient than a conventional Current-Starved Ring-Oscillator (CSRO) if operating below 300 kHz at 1.8 V supply voltage. It was also implemented in a capacitive step-down converter and showed a 56 % improvement in the converter efficiency with 583 pW load power, compared to a converter using CSRO. Also, another proposed circuit, Hybrid Ring-Oscillator (HRO), improves energy efficiency by 56 % for  $>$  80 kHz operations, compared to CEpCRO, by utilizing different modes to reduce switching capacitance.

Second, in Chapter 3, Maximum-Power-Point-Tracking (MPPT) circuit designed for micro-scale sensor systems was discussed. It takes advantage of the unique structure of a switched capacitor energy harvester - it has a small sampling capacitor in parallel with the flying or decoupling cap in the SCBC that eavesdrops on the voltage transfer that occurs in the voltage converter. The power delivered to the battery can be determined by integrating the small voltage fluctuations using correlated double sampling. Since the sampling capacitor is  $64.8\times$  smaller in size than the flying cap, the impact on the conversion efficiency is negligible. By directly tracking the power delivered to the battery, all parameters of the SCBC can be optimized, including the switching frequency, the switch size, and the conversion ratio. Compared to the conventional current-mirror type MPPT circuits, the proposed design incurs no voltage drop and does not require high bandwidth amplifiers. Using correlated double sampling, the measured results in 180 nm CMOS shows that high accuracy is achieved with only 5 % overhead in the power consumption even at low harvested currents of  $1.4\ \mu\text{A}$ .

Third, in Chapter 4, a low-power battery supervisory circuit (BSC) integrated with a complete  $1\ \text{mm}^3$  sensor system was discussed. With the power-on reset and brown-out detection, the BSC fabricated in 180 nm CMOS consumes 635 pW at 3.6 V supply voltage, which is a  $213\times$  reduction over the best prior work. Ultra-low power is achieved using a 57 pA, fast stabilizing two-stage

voltage reference, an 81 pA leakage-based oscillator, and a clocked comparator. The two-stage voltage reference has a stacked reference pre-conditioner that generates a supply voltage for the second reference stage. It improves settling speed of the reference voltage by removing a decoupling capacitor, which is required in the conventional 2T leakage-based voltage reference for noise reduction. The 0.2 Hz clock signal from the oscillator is shared for the clocked comparator and the delay generation in order to help reduce power consumption. The clock signal is used in the clocked comparator to convert the low output voltage from the preamplifier to the high battery voltage. Once the comparator detects a sufficiently high battery voltage, the clock is used again to generate the power-on-reset delay of 0.8 sec. Integrated with a complete 1 mm<sup>3</sup> sensor system, the BSC controls the reset functionality of electronics on its own die as well as orchestrates the reset sequence in other chip layers by modulating power supply voltages that are monitored by secondary reset detectors on those dies.

Finally, in Chapter 5, an adaptive battery supervisory system with a battery quality monitor was described. It automatically adapts to the battery health, which can be estimated from its internal resistance ( $R_{BAT}$ ), and establishes a constant effective threshold voltage. Compared to a conventional fixed-threshold BSC, the new design avoids oscillation and widens the usable range of battery voltages, independent of  $R_{BAT}$ .  $R_{BAT}$  is measured by inducing a test current using decap and measuring the resulting RC response time. When tested with a 2  $\mu$ Ah battery and the 11  $\mu$ A sensor system, the BSC improves the required hysteresis from 656 mV to 77 mV, increasing the usable battery voltage range by 2.7 $\times$ .

The aforementioned circuits in this dissertation can be used to overcome design challenges caused by the severe size constraints and thus extend the system lifetime. This will usher in an era of unprecedented applications, which have not been realized using existing technologies.

## **BIBLIOGRAPHY**

- [1] G. Bell, "Bell's Law for the birth and death of computer classes," *Commun. ACM*, vol. 51, no. 1, pp. 86-94, Jan. 2008.
- [2] Y. Lee, S. Bang, I. Lee, Y. Kim, G. Kim, M. H. Ghaed, P. Pannuto, P. Dutta, D. Sylvester, and D. Blaauw, "A Modular 1 mm<sup>3</sup> Die-Stacked Sensing Platform With Low Power I2C Inter-Die Communication and Multi-Modal Energy Harvesting," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 229-243, Jan. 2013.
- [3] J. M. Kahn, R. H. Katz, K. S. J. Pister, "Next Century Challenges: Mobile Networking for "Smart Dust"," *ACM/IEEE Intl. Conf. on Mobile Computing and Networking*, Aug. 1999, pp. 271-278.
- [4] K. Ashton, "That 'Internet of Things' Thing," *RFID Journal*, Jul. 2009.
- [5] R. Muller, H.-P. Le, W. Li, P. Ledochowitsch, S. Gambini, T. Bjorninen, A. Koralek, J. M. Carmena, M. M. Maharbiz, E. Alon and J. M. Rabaey, "A miniaturized 64-channel 225 $\mu$ W wireless electrocorticographic neural sensor," newblock *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 412-413.
- [6] M. H. Nazari, M. Mujeeb-U-Rahman and A. Scherer "An Implantable Continuous Glucose Monitoring Microsystem in 0.18 $\mu$ m CMOS," *IEEE Symp. VLSI Circuits Dig.*, June 2014, 194-195.
- [7] Y. Hu, L. Huang, W. S. A. Rieutort-Louis, J. Sanz-Robinson, J. C. Sturm, S. Wagner and N. Verma "A Self-Powered System for Large-Scale Strain Sensing by Combining CMOS ICs With Large-Area Electronics," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 838850, Apr. 2014.
- [8] G. Kim, Y. Lee, Z. Foo, P. Pannuto, Y.-S. Kuo, B. Kempke, M. Ghaed, S. Bang, I. Lee, Y. Kim, S. Jeong, P. Buta, D. Sylvester and D. Blaauw, "A millimeter-scale wireless imaging system with continuous motion detection and energy harvesting," *IEEE Symp. VLSI Circuits Dig.*, June 2014, 178-179.
- [9] G. Chen, H. Ghead, R. Haque, M. Wieckowski, Y. Kim, G. Kim, D. Fick, D. Kim, M. Seok, K. Wise, D. Blaauw, and D. Sylvester, "A Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2011, pp. 310-311.
- [10] D. Jeon, Y.-P. C., Y. Lee, Y. Kim, Z. Foo, G. Kruger, H. Oral, O. Berenfeld, Z. Zhang, D. Blaauw, and D. Sylvester, "An Implantable 64nW ECG-Monitoring Mixed-Signal SoC for Arrhythmia Diagnosis," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 416-417.
- [11] G. Chen, S. Hanson, D. Blaauw, and D. Sylvester, "Circuit Design Advances for ireless Sensing Applications," *Proceeding of the IEEE*, Nov. 2010, pp. 1808-1827.
- [12] S. Jeong, Z. Foo, Y. Lee. J.-Y. Sim, D. Blaauw, D. Sylvester "A Fully-Integrated 71 nW CMOS Temperature Sensor for Low Power Wireless Sensor Nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1682-1693, Aug. 2014.

- [13] S. Oh, Y. Lee, J. Wang, Z. Foo, Y. Kim, D. Blaauw, D. Sylvester “Dual-Slope Capacitance to Digital Converter Integrated in an Implantable Pressure Sensing System,” *IEEE Eur. Solid-State Circuits Conf.*, Sep. 2014.
- [14] P. P. Mercier, A. C. Lysaght, S. Bandyopadhyay, A. P. Chaandrakasan and K. M. Stankovic “Energy extraction from the biologic battery in the inner ear,” *Nature Biotechnology*, vol. 3, no. 12, pp. 1240-1243, Dec. 2012.
- [15] W. Jung, S. Oh, S. Bang, Y. Lee, D. Sylvester and D. Blaauw “A 3nW Fully Integrated Energy harvester Based on Self-Oscillating Switched-Capacitor DC-DC Converter,” *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 398-399.
- [16] L. G. Salem and P. P. Mercier “An 85 *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 88-89.
- [17] M. Vidojkovic, X. Juang, X. Wang, C. Zhou, A. Ba, M. Lont, Y-H. Liu, P. Harpe, M. Ding, B. Busze, N. Kiyani, K. Kanda, S. Masui, K. Philips and H. de Groot “A 0.33nJ/b IEEE802.15.6/Proprietary-MICS /ISM-Band Tranceiver with Scalable Data-Rate from 11kb/s to 4.5Mb/s for Medical Applications,” *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 170-171.
- [18] S. Bang, A. Wang, B. Giridhar, D. Blaauw and D. Sylvester “A Fully Integrated Successive-Approximation Switched-Capacitor DC-DC Converter with 31mV Output Voltage Resolution,” *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 370-371.
- [19] M. Konijnenburg, Y. Cho, M. Ashouei, T. Gemmeke, C. Kim, J. Hulzink, J. Stuyt, M. Jung, J. Huisken, S. Ryu, J. Kim and H. de Groot “Reliable and Energy-Efficient 1MHz 0.4V dynamically Reconfigurable SoC for ExG Applications in 40nm LP CMOS,” *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 430-431.
- [20] G. Kim, Y. Lee, S. Bang, I. Lee, Y. Kim, D. Sylvester and D. Blaauw “A 695 pW standby power optical wake-up receiver for wireless sensor nodes,” *IEEE Custom Integrated Circuits Conference*, Sept. 2012, pp.9-12 .
- [21] M. H. Ghaed, G. Chen, R.-U. Haque, M. Wieckowski, Y. Kim, G. Kim, Y. Lee, I. Lee, D. Fick, D. Kim, M. Seok, K. D. Wise, D. Blaauw and D. Sylvester “Circuits for a Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.60, no.12, pp.3152-3162, Dec. 2013.
- [22] H.-P. Le, S. R. Sanders and E. Alon “Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters,” *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120-2131, Sep. 2011.
- [23] M. D. Seeman and S. R. Sanders “Analysis and Optimization of Switched-Capacitor DCDC Converters,” *IEEE Trans. Power Electron.*, vol.23, no.2, pp.841-851, Mar. 2008.
- [24] M.-L. Sheu, T.-W. Lin and W.-H. Hsu “Wide frequency range voltage controlled ring oscillators based on transmission gates,” *IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 2731-2734.



- [25] I.-C. Hwang, C. Kim and S.-M. Kang “A CMOS Self-Regulating VCO With Low Supply Sensitivity,” *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 42-48, Jan. 2004.
- [26] J. Choi, K. Lim and J. Laskar “A Ring VCO with Wide and Linear Tuning Characteristics for a Cognitive Radio System,” *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 395-398, June 2008.
- [27] X. Zhao, R. Chebli and M. Sawan “A wide tuning range voltage-controlled ring oscillator dedicated to ultrasound transmitter,” *International Conference on Microelectronics*, pp. 313-316, Dec. 2004.
- [28] N. Gupta “Voltage-Controlled Ring Oscillator for Low Phase Noise Application,” *International Journal of Computer Applications*, vol. 14, no. 5, pp. 23-27, Jan. 2011.
- [29] R. A. Nicodimus, S. Takagi and N. Fujii “Wide Tuning Range Voltage-Controlled Ring Oscillator,” *IEICE Trans. Electron.*, vol. E86-C, No. 6, June 2003.
- [30] X. Lei, Z. Wang, L. Shen and K. Wang “A Large Tuning Range Ring VCO in 180nm CMOS,” *Progress In Electromagnetics Research Symposium Proceedings*, pp. 1147-1149, Mar. 2013.
- [31] F. Veirano, P. Prez, S. Besio, P. Castro and F. Silveira “Ultra Low Power Pulse Generator Based on a Ring Oscillator with Direct Path Current Avoidance,” *IEEE Latin America Symposium on Circuit and System*, pp. 1-4, Feb. 2013.
- [32] G. Chen, M. Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M.-T. Chen, Z. Foo, D. Sylvester and D. Blaauw “Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells,” *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2010, pp. 288-289.
- [33] U. Denier “Analysis and Design of an Ultralow-Power CMOS Relaxation Oscillator,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1973-1982, Aug. 2010.
- [34] D.-W. Jee, D. Sylvester, D. Blaauw and J.-Y. Sim “A 0.45V 423nW 3.2MHz multiplying DLL with leakage-based oscillator for ultra-low-power sensor platforms,” *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 188-189.
- [35] I. Lee, S. Bang, D. Yoon, M. Choi, S. Jeong, D. Sylvester and D. Blaauw “A ripple voltage sensing MPPT circuit for ultra-low power microsystems,” *IEEE Symp. VLSI Circuits Dig.*, June 2013, C228-C229.
- [36] Yi-Chun Shih and Brian P. Otis, “An Inductorless DC-DC Converter for Energy Harvesting With a 1.2- $\mu$ W Bandgap-Referenced Output Controller,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 832-836, Dec. 2011.
- [37] Inge Doms, Patrick Merken, Chris Van Hoof, and Robert P. Mertens, “Capacitive Power management Circuit for Micropower Thermoelectric Generators With a 1.4  $\mu$ A Controller,” *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2824-2833, Oct. 2009.
- [38] Yogesh K. Ramadass, Ayman A. Fayed, and Anantha P. Chandrakasan, “A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557-2565, Dec. 2010.

- [39] Saurav Bandyopadhyay and Anantha P. Chandrakasan, "Platform Architecture for Solar, Thermal and Vibration energy combining with MPPT and single inductor," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2011, pp. 238-239.
- [40] Yifeng Qiu, Chris Van Liempd, Bert Op het Veld, Peter G Blanken, Chris Van Hoof, "5 $\mu$ W-to-10mW Input Power Range Inductive Boost Converter for Indoor Photovoltaic Energy Harvesting with Integrated Maximum Power Point Tracking Algorithm," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2011, pp. 118-119.
- [41] Chao-Jen Huang, Wei-Chung Chen, Chia-Lung Ni, Ke-Horng Chen, Chien-Chun Lu, Yuan-Hua Chu, and Ming-Ching Kuo, "Thermoelectric Energy Harvesting with 1mV Low Input Voltage and 390nA Quiescent Current for 99.6 in *Proc. Eur. Solid-State Circuits Conf. (ESS-CIRC)*, 2012, pp. 105-108.
- [42] M. Fojtik, D. Kim, G. Chen, Y.-S. Lin, D. Fick, J. Park, M. Seok, M.-T. Chen, Z. Foo, D. Blaauw, and D. Sylvester, "A Millimeter-Scale Energy-Autonomous Sensor System With Stacked Battery and Solar Cells," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 801-813, Mar. 2013.
- [43] ADM6326 Datasheet, Analog Devices.
- [44] TPS3839 Datasheet, Texas Instruments.
- [45] MAX16057 Datasheet, Maxim Integrated.
- [46] CAT8801 Datasheet, ON Semiconductor.
- [47] LTC2934 Datasheet, Linear Technology.
- [48] I. Lee, S. Bang, Y. Lee, Y. Kim, G. Kim, D. Sylvester, and D. Blaauw, "A 635pW battery voltage supervisory circuit for miniature sensor nodes," in *IEEE Symp. VLSI Circuits Dig.*, 2012, pp. 202-203.
- [49] I. Lee, Y. Lee, D. Sylvester, and D. Blaauw, "Low Power Battery Supervisory Circuit with Adaptive Battery Health Monitor," in *IEEE Symp. VLSI Circuits Dig.*, 2014, pp. 22-23.
- [50] J. Guo, W. Sh. K. N. Leung, and C.-S. Choy, "Power-on-reset circuit with power-off auto-discharging path for passive RFID tag ICs," in *Proc. IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, 2010, pp. 21-24.
- [51] "CBC005 Datasheet," CYMBET Corporation.
- [52] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534-2545, Oct. 2012.
- [53] M. Wieckowski, G. Chen, S. Mingoo, D. Blaauw, and D. Sylvester, "A hybrid DC-DC converter for sub-microwatt sub-1V implantable applications," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2009, pp. 166-167.

- [54] Y. Kim, Y. Lee, D. Sylvester, and D. Blaauw, "SLC: Split-control Level Converter for dense and stable wide-range voltage conversion," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2012, pp. 478-481.
- [55] H.-B. Le, X.-D. Do, S.-G. Lee, and S.-T. Ryu, "A Long Reset-Time Power-On Reset Circuit With Brown-Out Detection Capability," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 11, pp. 778-782, Nov. 2011.
- [56] H. J. Bergveld, W. S. Kruijt, and P. H. L. Notten "Battery Management Systems Design by Modeling," *Philips Research Book Series*, vol. 1, Kluwer Academic Publishers, 2002.