Efficient Continuous-Time Sigma-Delta Converters for High Frequency Applications

by

Mehmet Batuhan Dayanik

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
2017

Doctoral Committee:

Professor Michael P. Flynn, Chair
Professor David Wehe
Associate Professor David D. Wentzloff
Associate Professor Zhengya Zhang

Mehmet Batuhan Dayanik

bdayanik@umich.edu

ORCID iD: 0000-0003-4895-3751

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

ADC	Analog-to-digital converter
BW	Bandwidth
CML	Current mode logic
CTΣΔ	Continuous-time delta sigma
DAC	Digital-to-analog converter
DEM	Dynamic element matching
DR	Dynamic range
DWA	Data weighted averaging
ENOB	Equivalent number of bits
FoM	Figure of merit
FMCW	Frequency modulated continuous wave
MAST	Micro-Autonomous System Technologies
OPM	One-point modulation
PLL	Phase lock loop

RDWA	Reference data weighted averaging
SFDR	Spurious free dynamic range
SNDR	Signal to noise and distortion ratio
SNR	Signal to noise ratio
TDC	Time-to-digital converter
TI-RDWA	Time interleaved reference data weighted averaging
TPM	Two-point modulation
UWB	Ultra wide bandwidth
VCO	Voltage controlled oscillator

ABSTRACT

Over the years Continuous-Time (CT) Sigma-Delta (ΣΔ) modulators have received a lot of attention due to their ability to efficiently digitize a variety of signals, and suitability for many different applications. Because of their tolerance to component mismatch, the easy to drive input structure, as well as intrinsic anti-aliasing filtering and noise shaping abilities, CTΣΔ modulators have become one of the most popular data-converter type for high dynamic range and moderate/wide bandwidth. This trend is the result of faster CMOS technologies along with design innovations such as better architectures and faster amplifiers. In other words, CTΣΔ modulators are starting to offer the best of both worlds, with high resolution and high bandwidth.

This dissertation focuses on the bandwidth and resolution of CTΣΔ modulators. The goal of this research is to use the noise shaping benefits of CTΣΔ modulators for different wireless applications, while achieving high resolution and/or wide bandwidth. For this purpose, this research focuses on two different application areas that demand speed and resolution. These are a low-noise high-resolution time-to-digital converter (TDC), ideal for digital phase lock loops (PLL), and a very high-speed, wide-bandwidth CTΣΔ modulator for wireless communication.

The first part of this dissertation presents a new noise shaping time-to-digital converter, based on a CTΣΔ modulator. This is intended to reduce the in-band phase noise of a high frequency digital phase lock loop (PLL) without reducing its loop bandwidth. To prove the

effectiveness of the proposed TDC, 30GHz and a 40GHz fractional-N digital PLL are designed as a signal sources for a 240GHz FMCW radar system. Both prototypes are fabricated in a 65nm CMOS process. The standalone TDC achieves 81dB dynamic range and 13.2 equivalent number of bits (ENOB) with 176fs integrated-rms noise from 1MHz bandwidth. The in-band phase noise of the 30GHz digital fractional-N PLL is measured as -87dBc/Hz at a 100kHz offset which is equivalent to -212.6dBc/Hz^2 normalized in-band phase noise.

The second part of this dissertation focuses on high-speed (GS/s) CTΣΔ modulators for wireless communication, and introduces a new time-interleaved reference data weighted averaging (TI-RDWA) architecture suitable for GS/s CTΣΔ modulators. This new architecture shapes the digital-to-analog converter (DAC) mismatch effects in a CTΣΔ modulator at GS/s operating speeds. It allows us to use smaller DAC unit sizes to reduce area and power consumption for the same bandwidth. The prototype 5GS/s CTΣΔ modulator with TI-RDWA is fabricated in 40nm CMOS and it achieves 156MHz bandwidth, 70dB dynamic range, 84dB SFDR and a Schreier FoM of 158.3dB.

CHAPTER 1. Introduction

1.1. High-Speed Wireless Applications

In 1901, Guglielmo Marconi, successfully transmitted radio signals across the Atlantic Ocean and wireless technology came into existence. Over more than a century, from 1901 until today, thousands of scientist and engineers have worked to make wireless technology more affordable, and deliver wider bandwidth and more dynamic range with less power consumption. Thanks to those advancements, today, we use wireless technology in all aspects of our lives. According to GSMA Intelligence, there are now more mobile wireless gadgets on earth than people [1]. This huge increase in interest in wireless technology has resulted in a demand for complete systems on integrated circuits for many different applications.

Over the years, wireless technology has created several different application areas with great potential for rapid growth. Even though wireless technology was initially only for voice communication, today several different application areas, such as wireless voice and data communication (i.e. 4G-LTE, 5G, WLAN, Bluetooth, UWB), radio detection and ranging (radar), terahertz imaging, global positioning systems (GPS), etc. use wireless technology. Although each of these applications uses similar circuit structures, they each have their own set of challenges and requirements.

1.1.1. Radio Detection and Ranging (Radar)

Radar uses electromagnetic waves to determine the range, direction, speed and altitude of both moving and fixed objects. Basically, a radar transmits radio waves through its antenna and receives the signal bounced off an object. By processing certain properties of the returned signal (i.e. frequency, power, etc.), radar can determine some parameters of the object such as distance, speed, and direction. Even though the first widespread use of radar was for the military during World War 2, today we use radar for auto cruise control systems (ACC), air traffic management (ATM), collision sensing, blind spot detection, autonomous landing guidance, autonomous vehicles, weather forecasting, security and surveillance.

Radar systems can be classified into two main parts: Pulse radars and continuous wave radars. Pulse radars transmit a high power and high frequency impulse signal and wait for the echo signal to be received before a new transmitted signal is sent out. The distance can be determined from the propagation time of the pulse signal, while the direction of the object is calculated through couple consecutive measurements. Pulse radars require high pulse power for maximum range and a very short pulse to achieve good resolution. One drawback for pulse radar is that it cannot determine the distance to the object correctly, if an echo signal from a long-range target is received after transmission of the second transmitting pulse. In this case, the radar determines the wrong time interval and therefore the wrong range. This maximum range that a pulse radar can correctly measure is called the maximum unambiguous range. Unlike pulse radars, continuous wave radars constantly transmit and receive a high-frequency signal. Frequency modulated continuous wave

(FMCW) radar is a subset of continuous wave radar and FMCW radar is becoming very popular in the automotive industry for auto cruise control systems.

1.1.1.1. FMCW Radar

The millimeter-wave wavelengths (1mm-1cm) are long enough to allow signal propagation through severe atmospheric conditions like snow, mist, or fog while they are short enough to allow fabrication of small form factor devices [2]. With recent improvements in silicon technology, it has become possible to implement highly integrated millimeter-wave radar transceiver circuits. Although there are several different ranging methods such as pulse-radar [3], [4], UWB radar [5], and frequency modulated continuous wave (FMCW) radar [6], [7], FMCW radars have gained significant attention because of their coherent transceiver structure, and also because they are easy to implement with solid state devices. Unlike the case with other types of radar, FMCW radar performance depends on the properties of a linear frequency sweep called the chirp signal (Fig. 1).

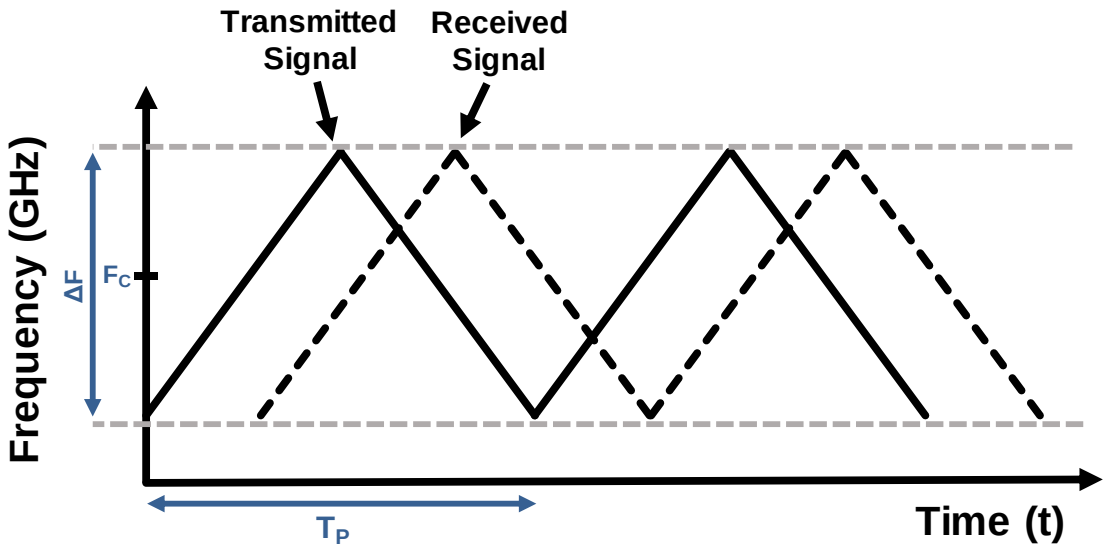

Fig. 1. Transmitted and received signals in a FMCW system with triangular sweep formation.

The velocity and range resolution of FMCW radar are determined by the speed, phase noise and linearity of the chirp signal, leading to challenges in the design of the PLL (Fig. 1). While the absolute frequency sweep (ΔF) and linearity of the chirp signal define the range resolution (ΔR) by $\Delta R = c/(2*\Delta F)$, the modulation period (T_P) and the operating center frequency (F_C) affect the velocity resolution (ΔV) by $\Delta V = c/(2*T_P*F_C)$ where c is the speed of light [8]. A fast chirp signal (<150usec) is desirable for short range (<200m) FMCW radar systems, because this keeps the receiver's down converted baseband frequency outside the flicker noise range of the active devices [7]. In addition, a fast chirp suppresses the additional noise due to the reflected power, or ground clutter, from large targets beyond the radar range [9]. On the other hand, a fast chirp reduces velocity resolution and is challenging to generate especially with good linearity. Chirp linearity is critical because, although the worsened velocity resolution can be offset by increasing the operating center frequency (F_C), any nonlinearity in the chirp signal creates frequency error in down conversion and worsens the radar resolution [10]. To keep frequency deviation of a chirp signal within 1% relative to a perfect sawtooth waveform, the first 100 harmonics of the chirp signal fundamental modulation frequency is required [10]. In addition to the linearity requirements, the ramp signal should have low phase noise, because phase noise makes difficult to detect moving targets and estimate their velocity against ground clutter [11], [12]. Moreover, chirp phase noise is important because FMCW radar uses the same chirp to down-convert the received signal. Therefore, an FMCW radar system requires a low phase noise, fast settling, high frequency chirp generator.

Over the years, digital fractional-N phase lock loops (PLLs) have emerged as the most common way to generate this chirp signal, because digital PLLs can efficiently create and

linearly modulate high frequency clock sources. Generating a fast-moving frequency ramp requires a fast settling PLL with a wide loop bandwidth. However, a fundamental problem for one-point modulation (OPM) PLLs is the conflict between the requirements for wide loop bandwidth and low in-band phase noise. This is because a wide PLL loop bandwidth passes more reference clock jitter, more charge pump noise, and in a fractional-N PLL, more quantization noise from the ΣΔ-modulator-controlled divider. Therefore, existing low phase high-frequency (>10GHz) PLLs are limited to integer-N PLL operation [13] and/or are restricted to low loop bandwidths and slow settling [14]. Recent research decouples settling time and phase noise by using Two-Point Modulation (TPM) [15]. However, TPM architectures either require gain calibration [16], or extra settling time [15] thereby restricting TPM schemes to only a single type of chirp signal. Another important drawback of existing high-frequency(>10GHz) PLLs is that they are analog PLLs [13], [14]; though applications favor digital PLLs due to their greater flexibility and smaller die area. Despite the advantages of small area and flexibility, digital PLLs are challenging because their noise performance is limited by the accuracy and noise of existing time-to-digital converters (TDCs) [17]. Even though there are some reported sub-picosecond TDCs [18], current high-frequency digital PLLs (>10GHz) have at least a 10dB higher in-band phase noise [19] compared to their analog counterparts. Hybrid PLLs can combine the advantages of both analog and digital PLLs [20] but having dual loops increases the design complexity and overall area.

1.1.2. High Speed Wireless Communication Systems

Thanks to the advancements in the semiconductor technology, the market for wireless communication has seen exponential growth in recent years. Millions of people around the

globe exchange information every day using consumer devices such as cellular telephones and other wireless communication products. However, as the number of devices increases, the need for bandwidth surges. According to Cisco – Global Mobile Data Traffic Forecast White Paper [21], the overall mobile data traffic is expected to grow to 49 Exabytes per month by 2021, which is a sevenfold increase over 2016 (Fig. 2).

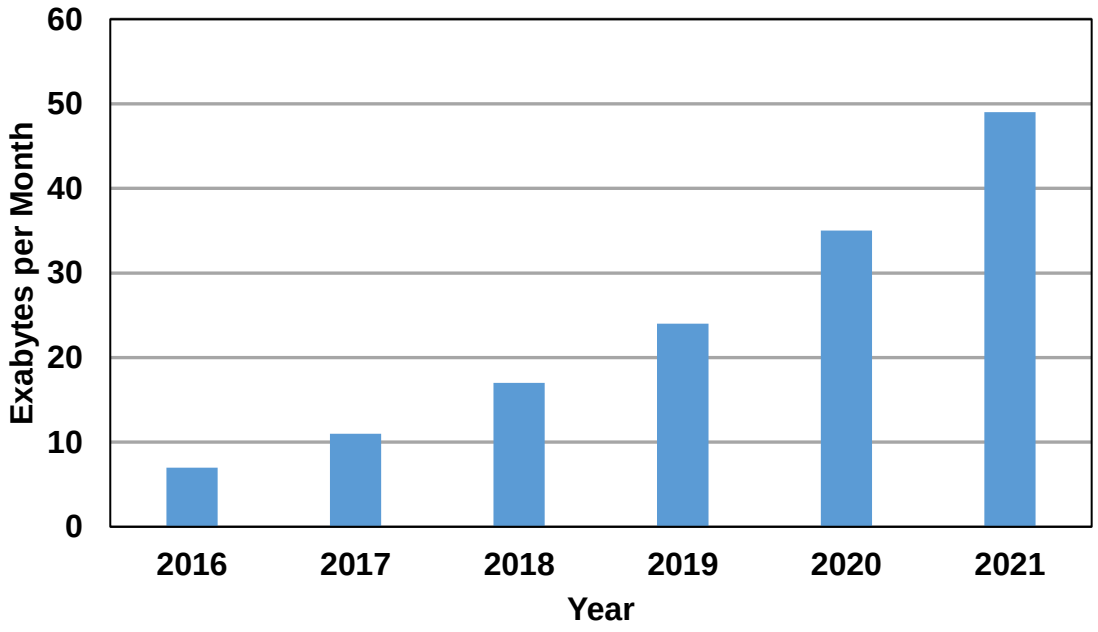

Fig. 2. Overall expected mobile data traffic from 2016-2021 [21].

To satisfy the enormous demand for mobile data, new wireless systems are proposed almost every ten years. 5G, the 5th generation wireless system, is the next telecommunication standard after 4G-LTE Advanced. 5G is a network system that targets much higher speeds and capacity with much lower latency than the current 4G-LTE-Advanced. It supports massive and reliable device-to-device communication, allowing a higher density of mobile broadband users per unit area. Due to its higher capacity compared to 4G LTE-A, 5G is expected to create new applications. For example, unlike 4G-LTE, 5G networks will accept small, inexpensive, low-power devices, which will increase the usage

of sensors for Internet of Things (IoT). Another new application area for 5G is virtual and augmented reality. While low latency of 5G can enable the internet-augmented world, its high data speed can enable streaming wireless virtual reality. Another application area is the driverless car. The future generation of driverless cars needs to interact both with other cars and smart roads to improve safety. The enhanced throughput, low latency and reliability of 5G technology will make vehicle-to-vehicle (V2V) and vehicle-to-everything (V2X) connections possible.

Besides cellular communication, the data rates for wireless local area network (WLAN) standards have also increased dramatically over the years. While the first IEEE 802.11 protocol from 1997 has a bandwidth of 22MHz with 2.4GHz, the latest IEEE 802.11ac standard provides 866Mbits/s data rates with a 5GHz carrier [22]. Moreover, by using orthogonal frequency division multiplexing (OFDM), IEEE 802.11ad achieves 6.75Gbits/s data rate from 60GHz carrier signal.

1.1.2.1. Key Building Blocks in Wireless Transceivers

A very common transceiver architecture for wireless communication is the super heterodyne architecture (Fig. 3). In the receive path, the radio frequency (RF) signal is amplified by a low-noise amplifier (LNA). Then, a down-converter, usually a mixer, translates the input RF signal down to an intermediate frequency (IF). Down conversion requires a reference frequency, or LO signal, which is usually generated by a frequency synthesizer that can cover a wide tuning range. After the down-conversion, an analog-to-digital converter (ADC) samples the IF signal so that demodulation and data processing occur in the digital domain. In the transmit side, the modulation happens in the digital domain in the back-end. Then, a digital-to-analog converter (DAC) transforms the digital

information to an analog intermediate frequency. After the DAC, a mixer converts the modulated IF carrier up to the desired RF frequency. To compensate the loss through the channel, a power amplifier (PA) must be used to increase the signal power before transmission via an antenna.

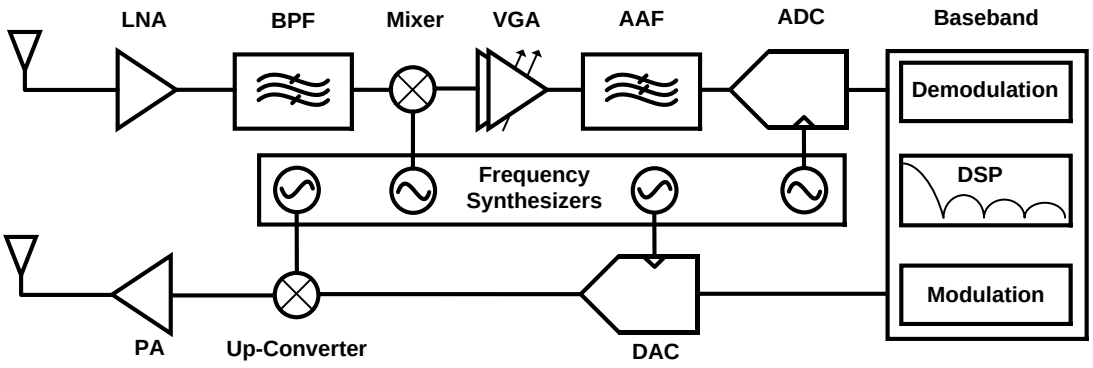

Fig. 3. Typical superheterodyne transceiver block diagram.

In radio transceiver circuits, the performance of a transceiver can be quantified in terms of maximum distance for satisfactory reception. This distance depends on the operation of individual components. Although each component has a different effect on transceiver operation, the frequency synthesizers and ADCs play a crucial role in the overall transceiver performance.

Most wireless communication systems are frequency multiplexed systems, which require precise channel selection. An important part of channel selection is synthesizing signals with the correct frequency. To satisfy this, almost all radio transceiver circuits relay on precise fractional-N phase lock loops as their frequency synthesizer. To reduce leakage from adjacent channels, and to reduce the effect of blockers, the phase noise performance of the PLL is crucial for high quality high speed communication systems.

In wireless communication systems, receivers are expected to operate properly and to sense weak transmitted signals, even when there is a high-power blocker close to the channel. With so many different wireless platforms, this is a very common scenario today. Nevertheless, the receiver must not degrade the quality of the wanted signal due to aliasing, folding or distortion [23]. In addition, high speed wireless communication techniques such as 4G LTE-A rely on extensive digital modulation techniques, which motivates the direct conversion to simplify the design and reduce the cost. An advantage is that, unlike super heterodyne receivers, direct conversion does not require several stages of sharp filtering. However, placing the ADC close to the antenna within a high-blocker environment puts a lot of demands on the ADC performance. For instance, today LTE-advance requires ADCs with more than 100MHz bandwidth and 70dB dynamic range [24].

1.2. Research Contributions

Low noise, high resolution, high speed circuits with low power are very important for wireless applications. For instance, FMCW radar transceivers require very precise, highly linear, low noise chirp signals which requires digital PLLs for small area and flexibility with low TDC quantization noise. On the other hand, high-speed wireless communication circuits like 4G-LTE-A requires ADCs both with high dynamic range (>70dB) and high bandwidth (>100MHz). The objective of this dissertation is to introduce new circuit architectures that satisfy the resolution, noise and speed requirements of different wireless systems. To achieve this goal, we take advantage of the noise shaping properties of CTΣΔ modulators. This dissertation focuses on two different application areas: the first one is low noise high resolution time-to-digital converters (TDCs) for digital phase lock loops (PLLs)

that can be used in FMCW radars, while the second topic is high-speed, wide-bandwidth CTΣΔ modulators for wireless transceivers.

In the first area, we apply the benefits of noise shaping in CTΣΔ modulators to achieve high-resolution time-to-digital conversion for high-frequency digital PLLs. A fundamental problem for one-point-modulation (OPM) digital or analog PLLs is the conflict between fast settling time and low in-band phase noise. Fast settling necessitates a wide loop bandwidth, but results in increased phase noise due to reference clock jitter and charge pump noise for analog PLLs, and TDC quantization noise for digital PLLs. Among these noise sources, TDC quantization noise is the most dominant one. Therefore, existing high frequency PLL solutions (>10GHz) are usually analog PLLs, though applications favor the digital PLLs due to their greater flexibility and smaller die area. This dissertation introduces a new CTΣΔ modulator based noise shaping time-to-digital converter (TDC) architecture for high frequency digital PLLs that can shape the TDC quantization noise and reduce in-band phase noise of a digital PLL. This new TDC architecture achieves 81dB dynamic range and 13.2 equivalent number of bits (ENOB) with 176fs integrated-rms noise from 1MHz bandwidth. The effectiveness of the TDC to PLL in-band phase noise is verified within a 30GHz and a 40GHz fractional-N digital phase lock loop and they achieve -87dBc/Hz measured phase noise at 100kHz offset, which gives -212.6dBc/Hz^2 normalized in-band phase noise and 545fs jitter. Thanks to the noise shaping TDC, the normalized phase noise of the PLL is 5dB better than any published digital integer or digital fractional-N high frequency (>20GHz) PLL at the time of publication of this research.

The second topic covered in this dissertation is the high-speed (GS/s) CTΣΔ modulators for wireless communications. DAC linearity is very important for CTΣΔ modulator

performance. However, conventional methods for dealing with feedback DAC mismatch do not work well in high speed CTΣΔ modulators because they add extra delay to the critical feedback loop and make the modulator completely unstable. This research introduces a new time-interleaved reference data weighted averaging (TI-RDWA) architecture for high speed CTΣΔ modulators. This TI-RDWA makes it possible to use DAC mismatch shaping techniques in high speed CTΣΔ modulators and allows us to use high sampling clock frequencies (5GS/s) and achieve 156MHz bandwidth from a CTΣΔ modulator with 70dB dynamic range.

1.3. Organization

The organization of this dissertation is as follows. Chapter 2 reviews some background information about how CTΣΔ modulators operate, describes the major non-idealities in CTΣΔ modulators and gives an overview of high speed CTΣΔ modulators. In addition, chapter 2 briefly describes the operation of a phase lock loop (PLL) and current state-of-the-art PLLs over 10GHz. Chapter 3 explains the new CTΣΔ modulator based noise-shaping TDC architecture for digital PLLs. In addition, both stand-alone measurement results of the prototype TDC and its effect on the phase noise performance of a 30GHz and a 40GHz PLL for a frequency modulated continuous wave radar, is presented. Chapter 4 introduces the time-interleaved reference data weighted averaging architecture for high-speed CTΣΔ modulators and presents the measurement results of the prototype. Chapter 5 suggests some future work and chapter 6 concludes the dissertation by emphasizing the research contributions.

CHAPTER 2. Background Information

2.1. ΣΔ Modulators

With the advancements at the silicon technology, signal processing tasks are now almost always performed in the digital domain. This is because digital signal processing is simple, flexible, always produces the same results and occupies a very small area. This pervasive trend increases the requirements on the analog-to-digital interface and makes the analog-to-digital converters (ADCs) the main bottleneck for the whole system, in terms of speed and resolution. Although there are several different types of architecture for analog-to-digital conversion, ΣΔ ADCs cover the widest conversion region in the resolution-versus-bandwidth plane [25]. The reason for this tendency is that ΣΔ ADCs can achieve high accuracy and bandwidth by using two important techniques known as oversampling and noise shaping.

The quality of analog-to-digital conversion is defined by its resolution and it is measured by the signal-to-noise ratio (SNR). As the name implies, signal-to-noise ratio is the ratio of the signal power to the total noise power. Theoretically, the signal-to-noise ratio of an ADC with a full-scale sinusoidal is given by SNR=6.02*N + 1.76 where SNR is the signal-to-noise ratio in dB scale and N is the resolution. One main factors that limits the SNR of an ADC is the truncation of the analog input signal during the digitization operation. This truncation process is known as quantization operation and adds white noise, referred to as

quantization noise, to the signal. Thus, this additive quantization noise creates a fundamental limit to the ADC resolution [26].

One way that ΣΔ ADCs improve their resolution is by using oversampling. Under certain conditions, quantization noise behaves like a white noise and is uniformly distributed between DC and $F_S/2$ where F_S is the sampling frequency. For Nyquist ADCs, the sampling frequency (F_S) must be greater than the Nyquist sampling rate (F_N) which is twice of the ADC bandwidth. On the other hand, oversampling ΣΔ ADC, use a much higher sampling frequency (Fs) than the minimum required Nyquist sampling rate (F_N) [27], where the ratio between F_S and F_N is defined as the oversampling ratio (OSR). Because of this over sampling ratio, the quantization noise in ΣΔ ADCs is distributed over a wider frequency range and quantization noise floor in ΣΔ ADCs power spectral density within the ADC bandwidth is reduced.

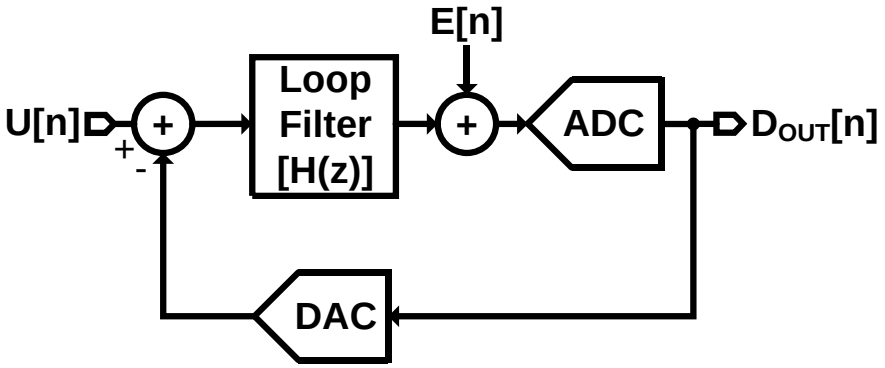

Fig. 4. Block diagram of an ΣΔ ADC.

In ΣΔ ADCs a technique called noise shaping further increases resolution. A typical ΣΔ ADC configuration has a loop filter with a transfer function of H(z), a low-resolution ADC and a digital-to-analog converter (DAC) in feedback configuration (Fig. 4). The digital

output $D_{OUT}[n]$ depends on both the input signal U[n] and quantization noise E[n] and it can be represented as

$$D_{OUT}(z) = \frac{H(z)}{1 + H(z)} * U(z) + \frac{1}{1 + H(z)} * E(z) \quad (1)$$

where H(z) is the loop filter transfer function. Here H(z)/(1+H(z)) is known as the signal transfer function (i.e. STF) while 1/(1+H(z)) is referred as the noise transfer function (i.e. NTF). Although both STF and NTF are defined by the same loop filter their outcome can be quite different from each other depending on H(z). For instance, if the loop filter transfer function H(z) is

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (2)$$

then equation 1 can be simplified to:

$$D_{OUT}(z) = z^{-1} * U(z) + (1 - z^{-1}) * E(z) \quad (3)$$

where STF is equal to z^{-1} and NTF is equal to $(1-z^{-1})$. Here, STF is an all pass filter. On the other hand, NTF has a high pass filter characteristics which means that the quantization noise distribution is not uniform over frequency and it is suppressed at lower frequencies, close to DC (Fig. 5). In other words, the quantization noise at the output of the ADC is shaped. Noise shaping is a very useful technique because it allows ΣΔ ADCs to achieve higher resolutions values with low resolution ADCs.

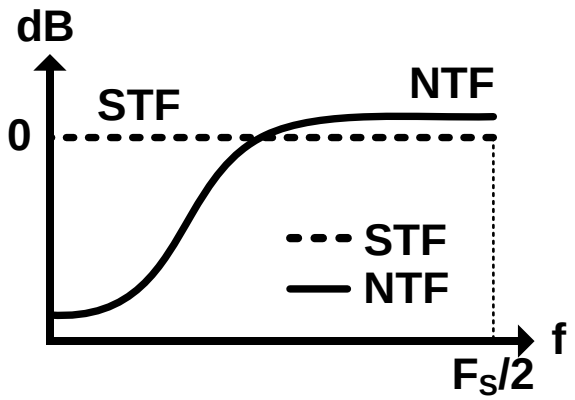

Fig. 5. STF and NTF of ΣΔ ADC given in Equation 1.

Another important benefit of oversampling ΣΔ ADCs is that they are more tolerant to component variations. Oversampling ΣΔ ADCs uses a much higher sampling rate than the minimum required by Nyquist criterion and generate their output based on all prior input values [26]. In other words, unlike Nyquist type ADCs, ΣΔ ADCs incorporates memory elements in their structure. Due to this memory effect, any component mismatch does not directly affect the digital output because the digital output is a combination of previous inputs as well. This unique property of ΣΔ ADCs makes them less sensitive to component mismatches, compared to Nyquist counterparts [28, 29]. Because of these benefits (i.e. oversampling, noise shaping and lower sensitivity to component variations), ΣΔ ADCs are a good choice for many systems [30, 31, 32, 33, 34].

2.1.1. Continuous Time ΣΔ Modulators

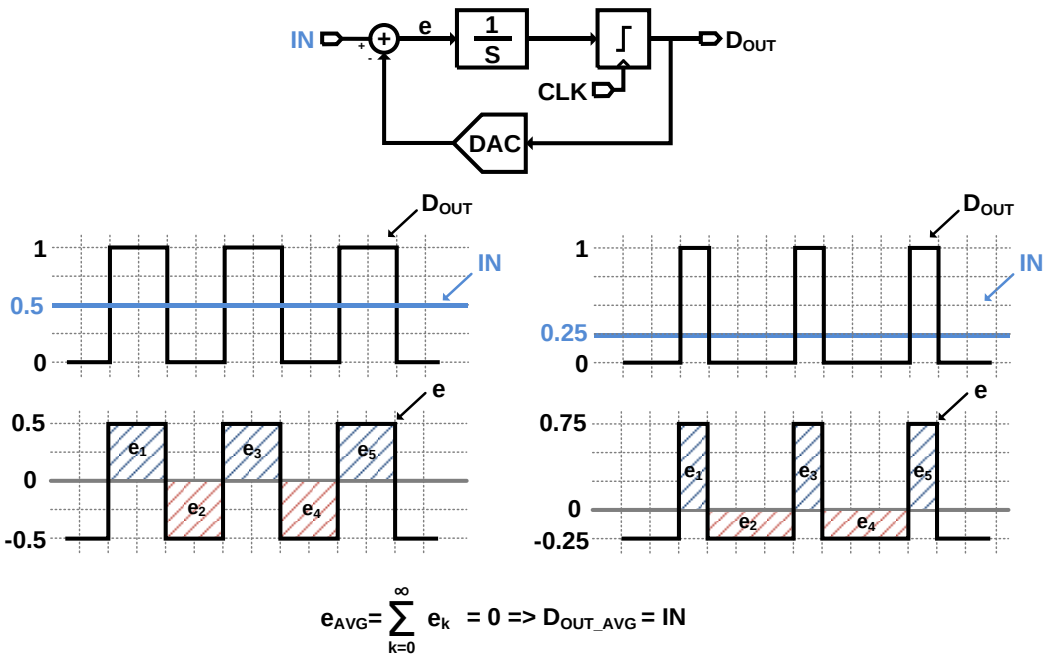

Fig. 6. Simplified schematic of a 1st order 1-bit low pass CTΣΔ modulator and its timing diagram when a dc voltage is applied to its input.

Continuous-time (CT) ΣΔ Modulators are a specific type of ΣΔ modulator that use continuous time loop filters. The loop filter can be implemented with active RC filter using opamps or OTAs, with gmC filters or even as LC resonator structures. Depending on the loop filter characteristics, continuous-time ΣΔ Modulators can be categorized as either low-pass [35, 36, 37] or band-pass [38, 39].

CTΣΔ modulators are feedback systems that digitize the input by adjusting digital output, such that the loop filter error input is zero on average. A good example for understanding the operation of a low pass CTΣΔ modulator is a first-order 1-bit modulator with a dc input (Fig. 6). Even though its 1-bit digital output (i.e. D_{OUT}) toggles with the sampling clock, on average the analog output voltage representation of the modulator digital output is identical to the input dc voltage (i.e IN). This is possible because the CTΣΔ

modulator is a feedback system where the integrator guarantees that sum of all the error inputs (i.e. e_1,e_2,e_3,etc.) is zero, so that the average of 1-bit digital output is equal to the average value of its input.

CTΣΔ modulators have several distinct differences compared to their discrete time (DT) counterparts. Among these, the most important advantage is the location where sampling operation takes place. In CTΣΔ modulators, the sampling occurs right at the quantizer, whereas DTΣΔ requires a sample and hold circuit before the modulator. This is quite a big difference because, in CTΣΔ modulators all the non-idealities of sampling process are subject to noise shaping, just as with the shaping of the quantization noise. In addition, the loop filter is in front of the quantizer and therefore acts like an anti-aliasing filter. Therefore, the input signal anti-aliasing requirements can be substantially reduced in CTΣΔ modulators. Finally, CTΣΔ modulators do not suffer from nonlinear resistance effects of the sample-and-hold switch, and so do not require additional bootstrapping circuits.

2.1.2. Non-Idealities in Continuous Time ΣΔ Modulators

CTΣΔ modulators are affected by circuit non-idealities including DAC non-linearity, noise, limited opamp bandwidth and excess loop delay in the feedback loop. Each of these non-idealities creates different performance problems. For instance, while DAC nonlinearities reduce the spurious free dynamic range (SFDR) of the ADC and create distortion, excess loop delay or limited opamp bandwidth can easily make the CTΣΔ modulator completely unstable. Therefore, each of these non-linearity effects needs to be carefully considered during the design of a CTΣΔ modulator. This section discusses two important non-idealities in CTΣΔ modulators: DAC non-linearity and excess loop delay.

2.1.2.1. DAC Non-linearity

Although there are a number of different digital-to-analog converter (DAC) structures for CTΣΔ modulators, the most commonly used one is the current steering architecture (Fig. 7). This is because of its fast operating speed. This DAC architecture is very similar to a charge pump circuit. While the two current sources, one is NMOS (N_1) and other is PMOS (P_1), sink and source current to the loop filter, the switches (i.e. N_3-N_4 and P_3-P_4) define the direction of the current depending on the digital input (D_P and D_N). In this way, the digital one bit code is converted into an analog current value.

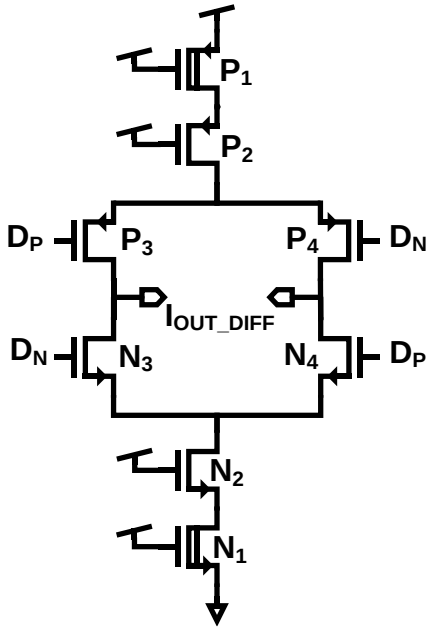

Fig. 7. Differential current steering DAC structure for CTΣΔ modulators

The performance of any feedback circuit is as good as its feedback structure. In CTΣΔ modulators, the feedback is usually satisfied by a multi-bit DAC and therefore it is the most important block that defines the linearity requirements of the modulator. These multi-bit structures usually suffer from two different mismatch types, namely static mismatch and dynamic mismatch.

A multi-bit DAC has several different current sources and depending on the size of the transistors and transistor threshold voltage variation, the unit DAC currents vary from one unit element to another. This dc current variation is the main source for static DAC mismatch in CTΣΔ modulators. Since the DAC is in the feedback path, any error in the DAC will appear directly at the output of the modulator. The amount of error depends on the input signal and, hence, this mismatch creates distortion at the output. Therefore, for N-bits of ADC linearity, the DAC needs to be at least N-bits linear unless some mismatch shaping techniques are used in the CTΣΔ modulator.

In addition to static mismatch, multi-bit CTΣΔ modulators also suffer from dynamic mismatch. Dynamic mismatch, as its name implies, is related to the transition of signals and one of the main sources is rise and fall time differences of the DAC pulses. If the rise time and the fall time of a DAC unit cell are different from each other, the amount of integrated current for positive and negative pulses is different, and this creates harmonic distortion at the output.

The easiest way to understand this concept is to consider a 1^{st} order 1 bit CTΣΔ modulator (Fig. 8). The output of a 1-bit 1^{st} order CTΣΔ modulator output toggles between +/-1 and the average area under the digital output is equal to its input voltage as explained in section 2.1.1. In the ideal case, if there is not any rise and fall time difference between the DAC outputs ($D_{OUT}[n]$), the area under the DAC output changes linearly and the overall transfer function of the modulator is also linear (as shown in blue colors in. Fig. 8(b)). On the other hand, if the rise and fall times differ (i.e. ΔT as shown in Fig. 8(a)), the two trapezoids under the rise time (shown in red in Fig. 8(a)) cancel each other and the remaining positive and negative rectangle areas (i.e A_1 and A_2) will be different from each

other, creating an offset for zero input (shown in red colors in Fig. 8(b)), and the overall transfer function will be nonlinear.

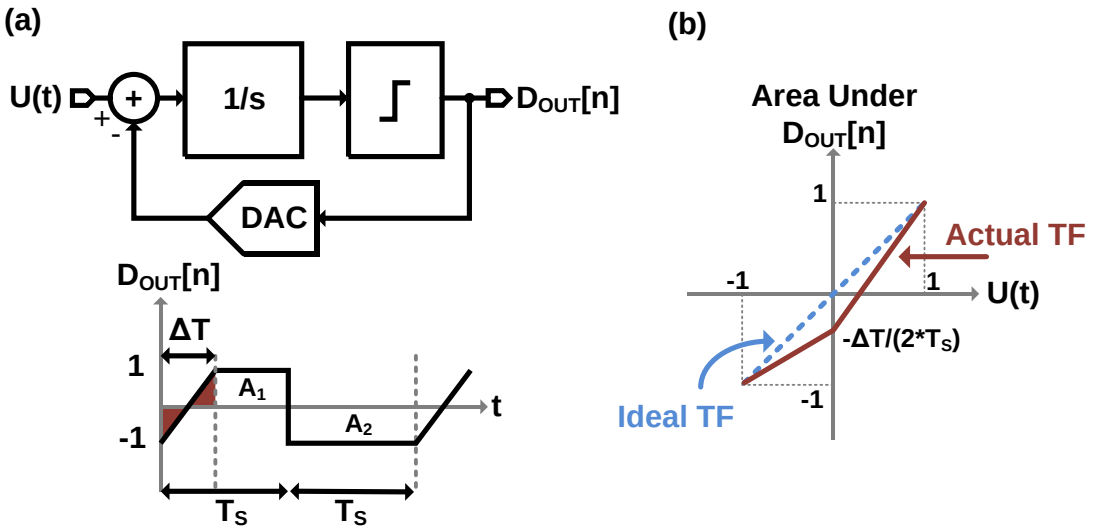

Fig. 8. (a) First order CTΣΔ modulator block diagram and asymmetric DAC output ($D_{OUT}[n]$) rise and fall times (finite rise time and zero fall time) (b) Transfer characteristics of the overall system (ideal and actual).

Timing skew of the signals in a multi-bit DAC also creates dynamic matching problems in CTΣΔ modulators, and distorts the output signal. For a multi-bit feedback DAC, the size of the unit elements needs to be sized large to reduce static mismatch between the DAC unit elements. However, this increases the overall DAC area, causing longer routing for the critical signals such as DAC outputs and CLK (Fig. 9). Because of this, each DAC unit cell current output ends up having a different propagation delay from the DAC switches to the integrator input. Moreover, for the same reason, the CLK routing has also different propagation delays for the unit cells. A tree formation can reduce the clock skew, but it expands the overall area and increases parasitics. In CTΣΔ modulators, this timing skew at the DAC outputs and CLK signal creates dynamic mismatch and distorts the output signal. This problem is especially challenging for high-speed CTΣΔ modulators, because high-

speed CTΣΔ modulators use GS/s sampling speeds and their tolerance to timing skew is substantially reduced.

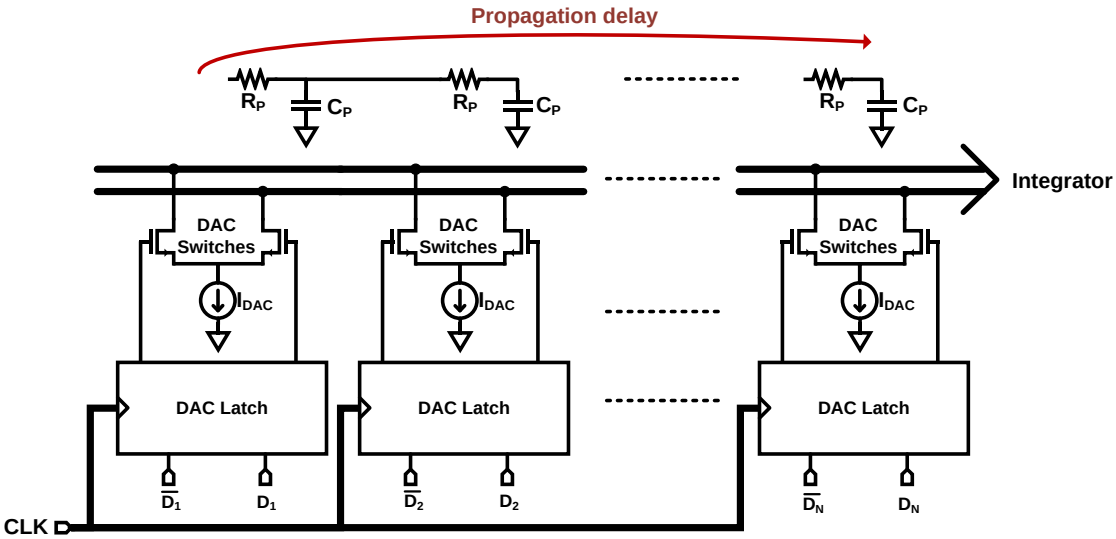

Fig. 9. Timing skew due to the multi-bit DAC layout in CTΣΔ modulators.

2.1.2.2. Excess Loop Delay

CTΣΔ modulators are feedback systems, and like every other feedback system they need to be stable. In CTΣΔ modulators, the loop stability relies on the amplitude and phase response of the loop filter including the DAC characteristics. However, in reality there are extra propagation delays coming from the DAC latch and the quantizer, due to the limited transistor speeds. These extra delays need to be considered during the modulator design. Otherwise, these delays can either change the loop filter characteristics and affect the noise shaping or even make the loop completely unstable.

The most common way to eliminate the effect of excess loop delay is to embed the quantizer and DAC propagation delays in the design of the loop filter. This is deliberately done by allocating some controlled time delay in the feedback path during the system level design and compensating this within the design of the analog loop filter. In this way, the

maximum delay is kept under control. However, the total loop delay of the CTΣΔ modulator from input of the quantizer, where sampling happens, to the output of the DAC, still needs to be less than one clock cycle to keep the modulator stable; otherwise the internal signals in the modulator loop filter grow and saturate the quantizer and thus the modulator itself. In other words, as the excess loop delay increases, the sampling clock of the modulator needs to decrease to keep the modulator stable. This is especially important for the GS/s CTΣΔ modulators since their clock speed is very fast and the tolerance for any kind of delay in the feedback path is limited.

2.1.3. Overview of High Speed CTΣΔ Modulators

Thanks to advancements in nanometer CMOS technology, ΣΔ modulators are becoming a competitive solution for power efficient ADCs and today ΣΔ modulators cover the widest conversion region on the resolution-vs-bandwidth plane for the state-of-the-art ADCs (Fig. 10). Among these, GS/s CTΣΔ modulators have gained significant attention over the past couple of years. In fact, CTΣΔ modulators have become the most common ADC architecture in commercial direct-receiver architectures for mobile handsets [25].

Over the years, several implementation have pushed the envelope for wideband ΣΔ modulators. [24] uses the input capacitance of the multi-bit quantizer as the integration capacitance for the loop filter to eliminate the extra delay that comes from the summing node and achieves 125MHz bandwidth by increasing the clock frequency. [39] has multiple tunable band-pass and low-pass CTΣΔ modulators to adjust the ADC conversion band from DC-to-1GHz with 150MHz bandwidth. [40] benefits from the calibration capabilities of 16nm CMOS technology to achieve 160MHz bandwidth. In addition to these single loop CTΣΔ modulators, others combine the benefits of different ADC architectures with CTΣΔ

modulators. [35] uses a 0-3 MASH architecture to increase the dynamic range of the CTΣΔ. [41] uses a 1-2 MASH architecture to reach 465MHz BW with 930mW power. On the other hand, [42] combines the benefits of pipeline ADCs and CTΣΔ modulators by using an analog delay cell to accomplish a 1GHz bandwidth in 28nm CMOS device.

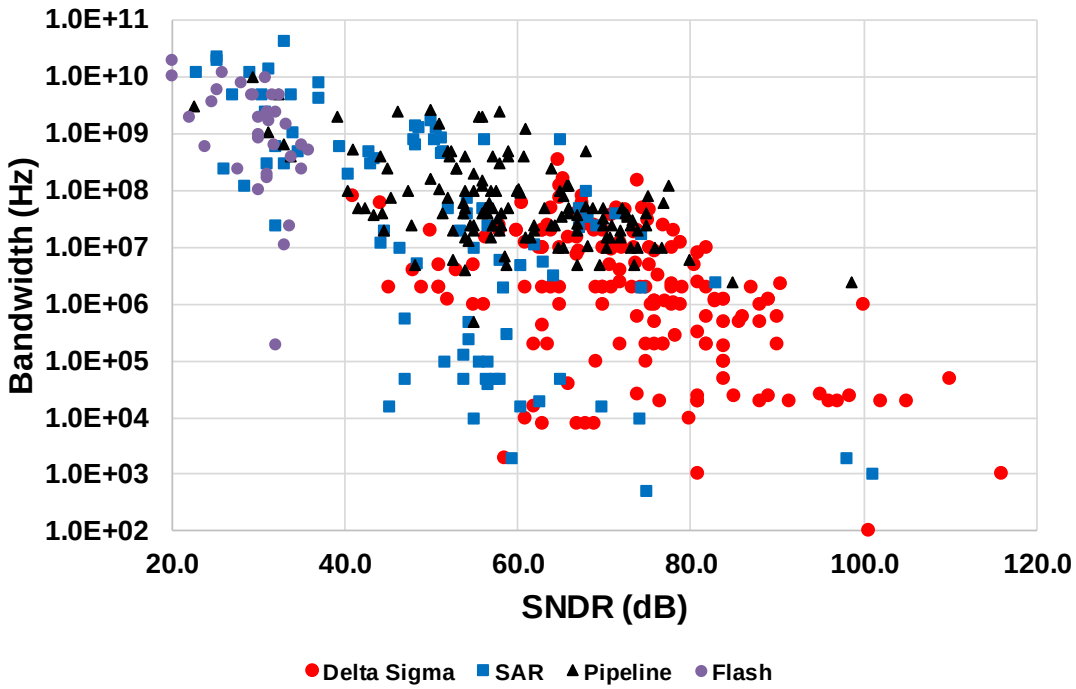

Fig. 10. Bandwidth vs SNDR plot of state-of-the-art ADCs [43].

2.2. Phase Lock Loops

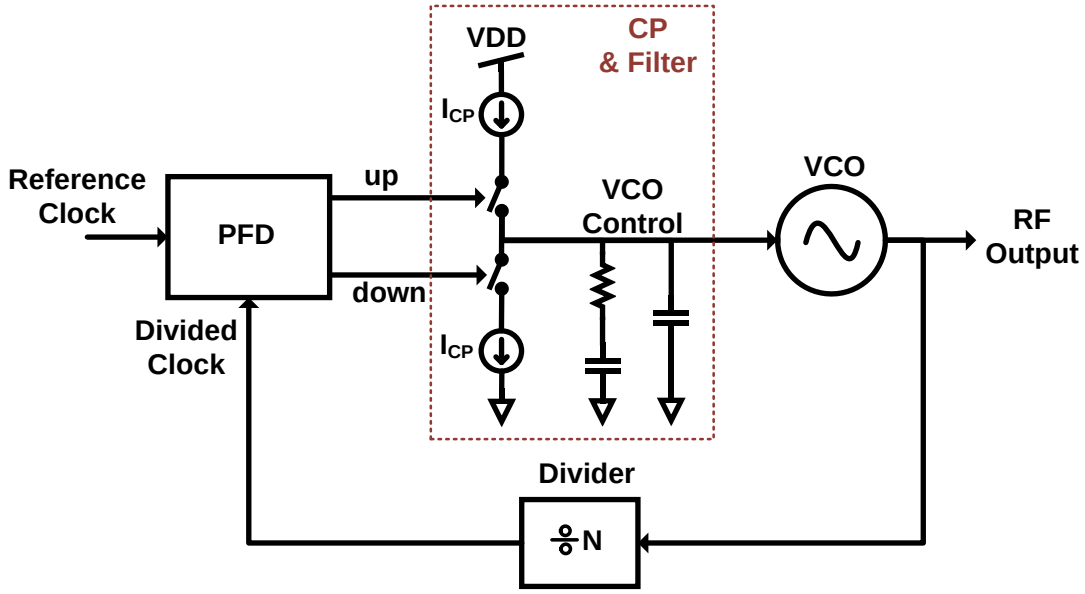

Fig. 11. Block diagram of a modern integer-N analog charge pump (CP) PLL.

The concept of a phase lock loop (PLL) was first developed in early 1930s [44]. Basically, a PLL is a feedback control system that generates a periodic output signal whose phase is locked to its reference input. Just like a regular opamp feedback system, the output frequency of the PLL can be adjusted by controlling its feedback ratio which is a frequency divider, to create multiples of the input reference frequency. Fig. 11 shows a practical example of a modern integer-N analog charge-pump (CP) PLL. The core components of an integer-N analog charge-pump PLL are the phase frequency detector (PFD), charge pump loop filter, voltage controlled oscillator (VCO) and integer-N divider. The VCO generates a periodic high frequency output signal where its output frequency is proportional to its input control voltage (i.e. VCO control). The divider, located in the feedback of the PLL, divides the VCO output frequency. The phase frequency detector compares the phase difference between the reference clock and divided clock, and generates a pulse-width modulated (PWM) voltage signal depending on the phase

difference between these two clocks. The duty cycle of the PWM signal depends on the phase difference between the reference and divided clock, while the location of the pulse (i.e. whether it is at the up or down output) indicates whether the reference clock or divided clock is leading. Finally, the PFD output is converted to current domain through a charge pump and filtered by the loop filter. The loop filter is a lead-lag filter to stabilize the PLL and is implemented by two capacitors and one resistor. The output of the loop filter sets VCO control voltage to close the loop. One of the main problems of an analog charge pump PLL is that the PFD and CP are high performance analog circuits and they are prone to variations. In addition, the required amount of area for loop filter capacitors depends on the PLL parameters and usually they occupy most of the PLL area.

2.2.1. A Fractional-N PLL

In a PLL, the output frequency can be changed by changing the division ratio (i.e. N). However, for an integer-N PLL the division ratio, N, is restricted to integer numbers. Therefore, for an integer-N PLL the frequency-step size at the output is limited by the reference frequency. In other words, to reduce the frequency step size at the output, one needs to reduce the PLL reference clock frequency, which is not practical in most of the cases. This is because the reference clock frequency of a PLL also needs to be much larger than its loop bandwidth, and most of the applications requires wide loop bandwidths (a typical value is 500KHz) to suppress the VCO phase noise.

One way to reduce the output step size is to use a ΣΔ modulator to convert a high precision division value into a stream of quantized lower precision values while keeping the average value of the output equal to its input. In this way, the targeted fractional value can be achieved on average and the quantization noise can be shaped at higher frequencies

just as explained in section 2.1. By modulating the division ratio with a digital ΣΔ modulator, any frequency value can be achieved at the output of the PLL without reducing the reference frequency or compromising the PLL loop bandwidth. This type of PLL is called as a Fractional-N PLL (Fig. 12).

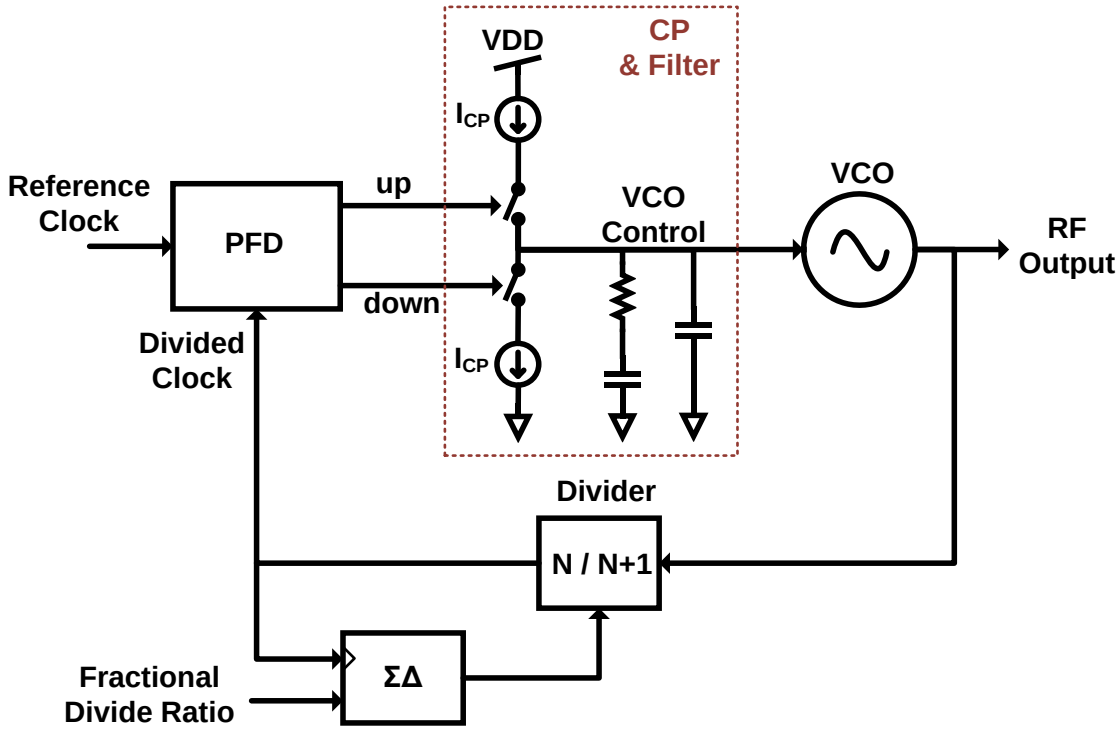

Fig. 12. Block diagram of a modern fractional-N PLL.

2.2.2. Overview of PLLs faster than 10GHz

Phase lock loops are one of the key elements in wireless transceiver architectures. Many wireless applications require low phase noise, fast settling fractional-N PLLs with wide frequency tuning range. However, fast settling requires wide loop bandwidth and PLLs have a fundamental contradiction between wide loop bandwidth and low in-band phase noise. [13] reduces the in-band phase of an analog PLL by using a method called sub-sampling PLL. A sub-sampling PLL does not require a divider at the feedback path to create higher output frequencies, and therefore does not suffer from the in-band phase noise

increase due to the divider. [7] uses a two-point modulation scheme to break the loop bandwidth and fast settling relationship in a PLL and therefore can optimize the loop bandwidth considering only the noise requirements. [45] is a hybrid PLL and cancels the fractional-N noise in digital domain within the PLL loop to reduce the phase noise of the PLL. [46] describes a digital PLL that uses several on-chip calibration techniques to reduce the in-band phase noise of the PLL and also uses gear selection mechanism to satisfy the fast settling time requirements.

CHAPTER 3. A Third-Order Noise Shaping Time-to-Digital Converter for Digital PLLs Used as a Reference Generator for a 240GHz FMCW Radar System

3.1. Review of 240GHz Radar Architecture

Recent developments in the silicon technology allow the implementation of commercial 77GHz FMCW short range (<200m) radars. However, these radars still require bulky and heavy antennas to operate. In order to solve these problems, [2] proposes a 240GHz FMCW radar architecture with a compact and light-weight frequency scanning antenna array for Micro-Autonomous System Technologies (MAST). The prototype PLL in this work is designed as a signal source for this 240GHz radar architecture.

The aim of this radar project is to utilize electronic beam steering to provide a +/-25° field of view at 30 frame-per-second (fps) with a 2° beam width and a 40cm range resolution. The 40cm resolution requires at least a 375MHz frequency modulation bandwidth, while the 50° field of view with 2° beam width needs a 25-segment traveling wave frequency scanning antenna array. To satisfy these specifications, a 25-step chirp signal ranging from 230GHz-to-245GHz at 33msec is chosen (Fig. 13). Each step is composed of a 4096-point 400MHz linear chirp at 1.33msec and a 200MHz jump afterwards.

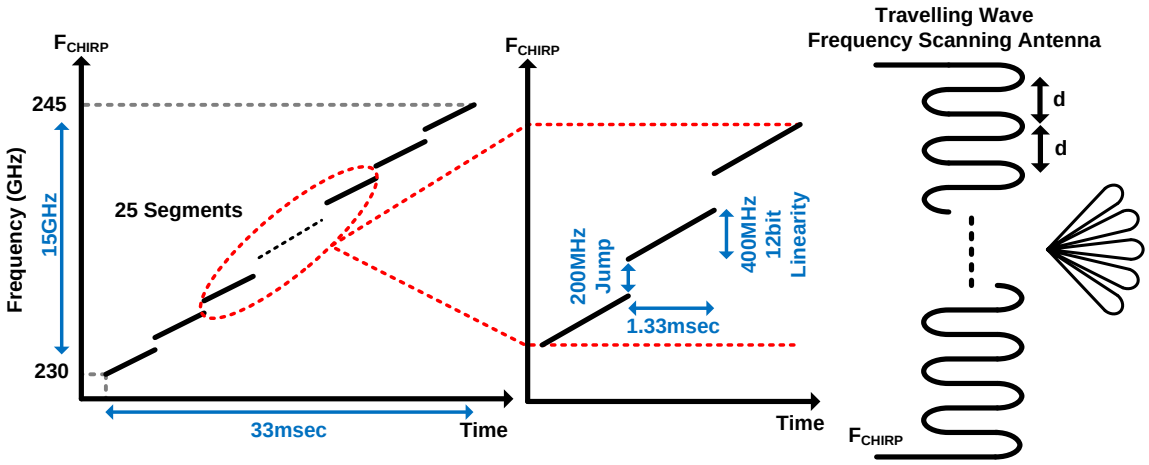

Fig. 13. 25-segment linear chirp signal for the 240GHz MAST FMCW radar system.

A block diagram of the 240GHz FMCW radar prototype is shown in Fig. 14. On the transmitter side, the PLL generates a 25-step high frequency chirp signal. Then, a frequency doubler and a tripler convert the PLL output to the required 230GHz-to-245GHz frequency range. Finally, the traveling wave frequency scanning antenna emits the electromagnetic wave and satisfies the +/-25° field of view by electronic beam steering. The received signal is collected by a second antenna array and passed to a low-noise amplifier (LNA). The output of the LNA is connected to a mixer which down converts the received signal by using the transmitted chirp as its reference LO input and afterwards, an intermediate frequency amplifier prepares the down converted signal for baseband process.

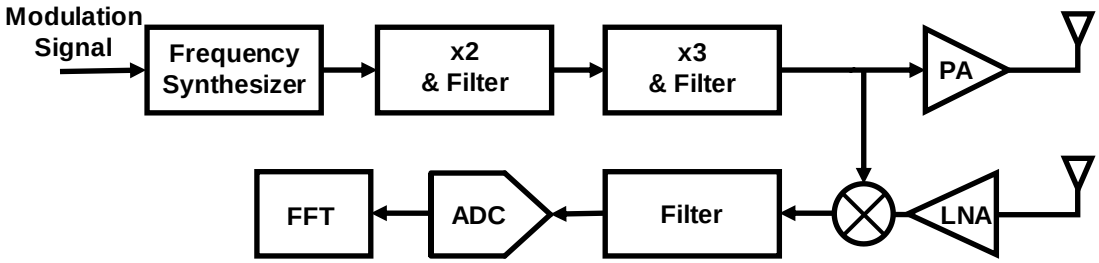

Fig. 14. Block diagram of the MAST 240GHz FMCW radar system.

The performance of an FMCW radar transceiver is mostly defined by the generated signal source. That's because, it drives both the transmitter and the receiver side. Thus, the

proper operation of PLL is crucial for the application. While linearity of the chirp signal and PLL lock time are important parameters for the transmitter, low in-band phase noise is crucial for the receiver. Due to our system specifications, the PLL needs to generate a 25 step sawtooth signal from 38.33GHz-to-40.83GHz with 66.66MHz linear chirp and 33.33MHz jump on each step. Moreover, despite the 33msec sweep time, the lock time of the PLL should be less than 4usec between each frequency jumps to maximize the directivity of the electronic beam steering. As a result, the required PLL loop bandwidth is larger than 1MHz. At the same time, the in-band phase noise around 100kHz offset frequency should be less than -85dBc/Hz to satisfy the necessary sensitivity and resolution requirements of the application.

3.2. Overview of Time-to-Digital Converters for Digital PLLs

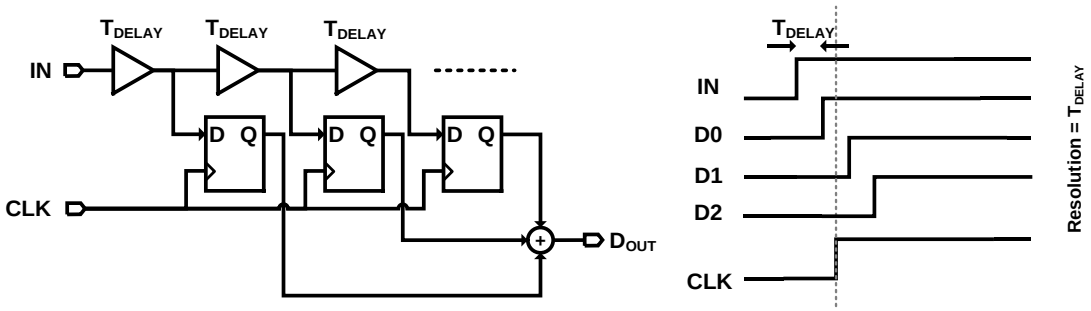

Fig. 15. Schematic of the delay line TDC.

In general, the quantization noise of a TDC is the limiting factor for the in-band phase noise of a wideband digital PLL. Thus, various architectures have been proposed to reduce TDC time resolution so far. A good example is may be one of the earliest and probably the most popular TDCs, called as the delay line TDC (Fig. 15). The idea is very similar to a flash-ADC. While the input signal pass through several unit delay elements, which act like a quantizer in time domain, the reference clock samples their output and digitize the delay.

Even though it is a simple and direct approach, the TDC resolution highly depends on unit cell delay (e.g. ~6ps for 40nm technology).

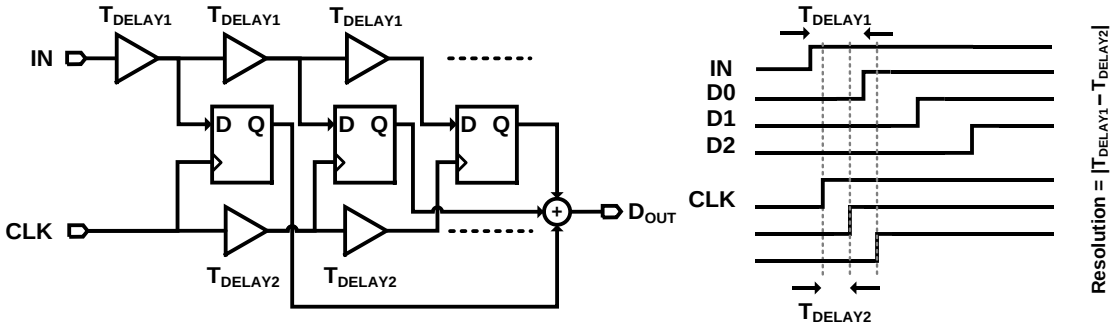

Fig. 16. Schematic of Vernier delay line TDC.

Another time domain method, called the Vernier TDC (Fig. 16), improves the time resolution of the TDC by delaying both the input and reference clock. By doing so, the resolution depends on the time delay difference between two separate cells rather than their absolute value. However, the downside of this method is that it doubles the number of required delay cells [47]. [48] uses a similar architecture to a two-step ADC to improve the time resolution of the TDC without increasing the number of delay cells. It is composed of a coarse and a fine TDC, with a time amplifier between them to amplify the quantization noise of the coarse TDC. Although this architecture increases the time resolution and reduces the number of required delay cells, the time amplifier limits the linearity of the whole TDC. In [49] a synchronous pipeline TDC is presented to reduce the time resolution. All of these approaches are Nyquist TDCs and hence the minimum resolution that can be achieved is limited by the quantization noise of the delay cells. Therefore, 1.12ps is the best resolution that is achieved with these Nyquist type TDCs so far. To further improve the time resolution values [18], [50], [51] introduced noise shaping TDCs. Even though these approaches reduce integrated rms noise within the TDC bandwidth to sub-picosecond

levels, they either suffer from dead-zone problems [50] which reduces the effective number of bits of the TDC or cannot support full 2π range of the reference clock [18].

3.3. Third-Order Continuous-Time Sigma-Delta Based Noise Shaping TDC

We introduce a third-order noise-shaping TDC [52] that takes advantage of noise shaping in a CTΣΔ modulator to achieve excellent time resolution. It breaks the time-to-digital converter quantization noise limitation in a digital PLL, and allows us to reach the noise performance of an analog PLL with a digital PLL. In the new TDC (Fig. 17), a phase/frequency detector (PFD) converts the phase difference between the TDC input and reference clock to a pulse-width-modulated (PWM) signal where the PWM duty cycle, in other words, its dc component, represents the phase difference of the two periodic signals. Then, a charge pump converts this PWM voltage signal to the current domain, and feeds it to a single-bit third-order CTΣΔ modulator. Finally, the CTΣΔ modulator filters the higher order harmonics of the PWM signal and digitizes its dc component while shaping the quantization noise.

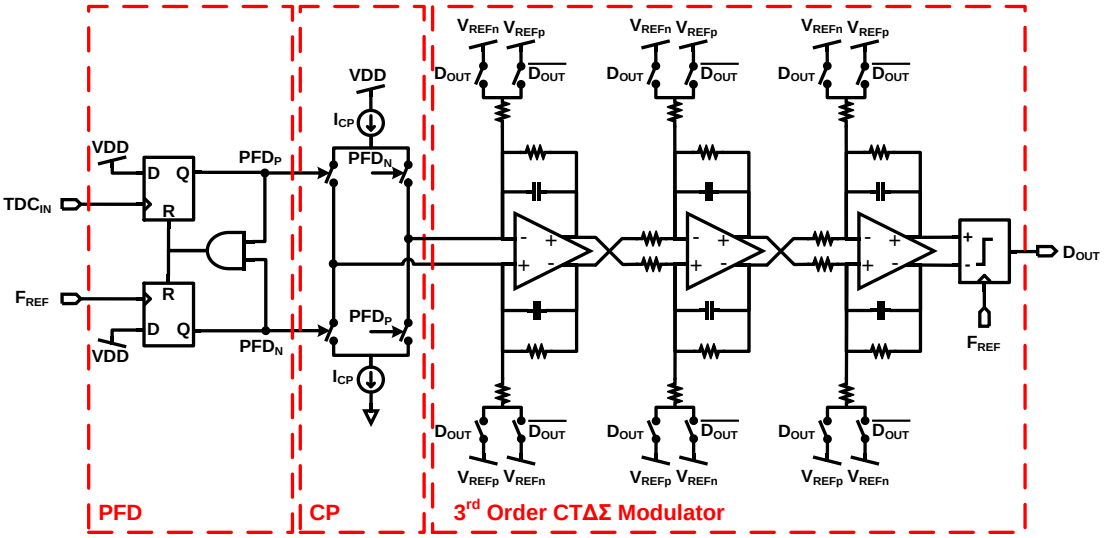

Fig. 17. Schematic of the third-order continuous time sigma delta (CTΣΔ) based noise shaping TDC.

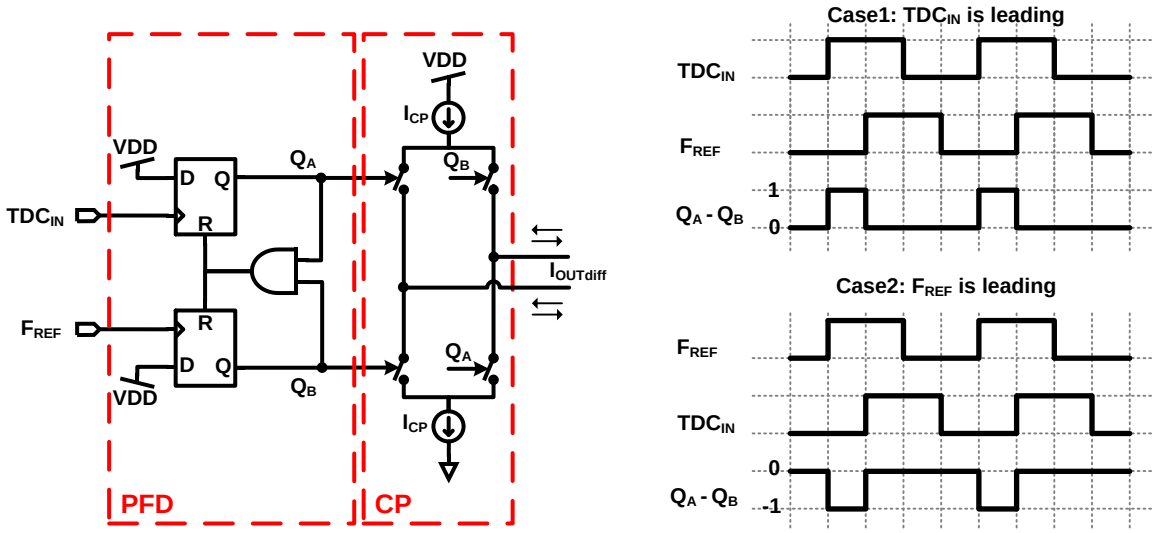

Fig. 18. Schematic of the phase/frequency detector with two possible timing diagrams.

The first two blocks of the TDC are a conventional phase/frequency detector and a charge pump circuit (Fig. 18). PFD is formed with two D-flip flops and an AND logic gate and generates a PWM voltage signal. The duty cycle of the PWM signal depends on the phase difference between the input (i.e. TDC_{IN}) and the reference clock (i.e. F_{REF}), while the location of the pulse (whether it is at the Q_A or Q_B output) indicates whether the TDC input or the reference clock is leading. After PFD, we use a charge pump circuit to convert the PWM voltage to a current waveform and feed this current signal to a CTΣΔ modulator. The CTΣΔ modulator filters the PWM waveform and digitizes the DC component, which represents the phase difference between the PLL reference and the feedback signal. As with any PWM signal, the output of the PFD and charge pump shown in Fig. 19 can be represented as a sum of cosines:

$$x(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi F_{REF} t n) \ \ where \ a_0 = Ad - \frac{A}{2}, \ a_n = \frac{2A}{n\pi}\sin(n\pi d) \qquad (4)$$

where the a_n coefficients are the amplitudes of cosine waves with frequencies that are multiples of fundamental reference frequency (i.e. F_{REF}), d is the duty cycle and A is the

amplitude of the PWM signal. As Fig. 19 and equation (4), the dc component (i.e. a_0) is linearly related to the duty cycle of the PWM signal and therefore represents the phase difference between the TDC input and reference clock. On the other hand, the amplitudes of the higher order harmonics are non-linear functions of the phase difference and so this harmonics need to be filtered out.

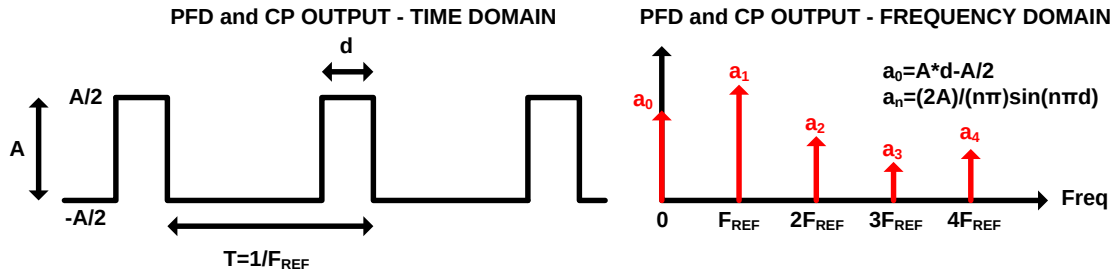

Fig. 19. PFD and CP output in time domain and frequency domain.

Thanks to their unique architecture, CTΣΔ modulators can digitize and filter an analog input and shape the quantization noise at the same time. A CTΣΔ modulator (Fig. 20(a)) can be modelled as a two input (i.e. V_{IN} and E) and one output (i.e. D_{OUT}) system where V_{IN} is the actual analog input and E is the representation of the uniformly distributed quantization noise. The digital output (i.e. D_{OUT}) of a CTΣΔ modulator is linear combination of V_{IN} and E

$$D_{OUT} = STF * V_{IN} + NTF * E \tag{5}$$

where STF is the signal transfer function and NTF is the noise transfer function. As an example, for a first order CTΣΔ modulator, the STF and NTF are:

$$STF = \frac{1 - z^{-1}}{s} \; and \; NTF = 1 - z^{-1} \; where \; z = e^{s} \tag{6}$$

As Fig. 20(b) and equation (6) show, the STF has low pass filter characteristics with notches at the reference clock frequency (i.e. F_{REF}) and its harmonics while the NTF has high pass filter characteristics.

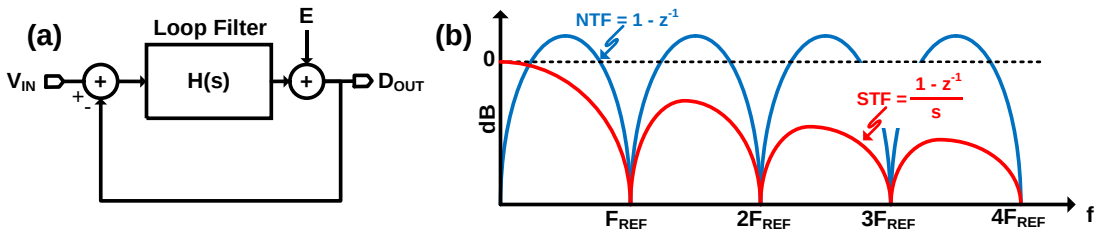

Fig. 20. (a) CTΣΔ modulator linearized model. (b) Signal and noise transfer functions of a first order CTΣΔ modulator.

Our TDC architecture uses the signal and noise transfer functions of a CTΣΔ modulator to both enhance the TDC resolution and to filter out the higher order harmonics of the PFD/CP output while only digitizing the dc component. In our architecture (Fig. 17), the PWM modulated output of the PFD/CP structure is fed into a CTΣΔ modulator. Because both the CTΣΔ modulator and the PFD use the same reference clock, thanks to its STF, the CTΣΔ modulator filters the multiples of the reference frequency (i.e. F_{REF}) in the PWM signal (Fig. 21(a)). In other words, the notches of the STF cancel out the reference frequency multiples in the PFD signal. As a result, the CTΣΔ modulator only passes the dc component of the PWM signal to its digital output. In addition to that, NTF of the CTΣΔ modulator high-pass filters the uniformly distributed quantization noise (Fig. 21(b)) and therefore enhances the TDC resolution within the PLL bandwidth. In this way, as shown in noise Fig. 21(c), a CTΣΔ modulator can digitize the phase difference between the reference clock and TDC input while at the same time achieves excellent time resolution within the PLL bandwidth. Although the NTF amplifies the high frequency portion of the

quantization noise, this shaped noise is filtered out by the PLL loop filter before going to VCO which will be explained later.

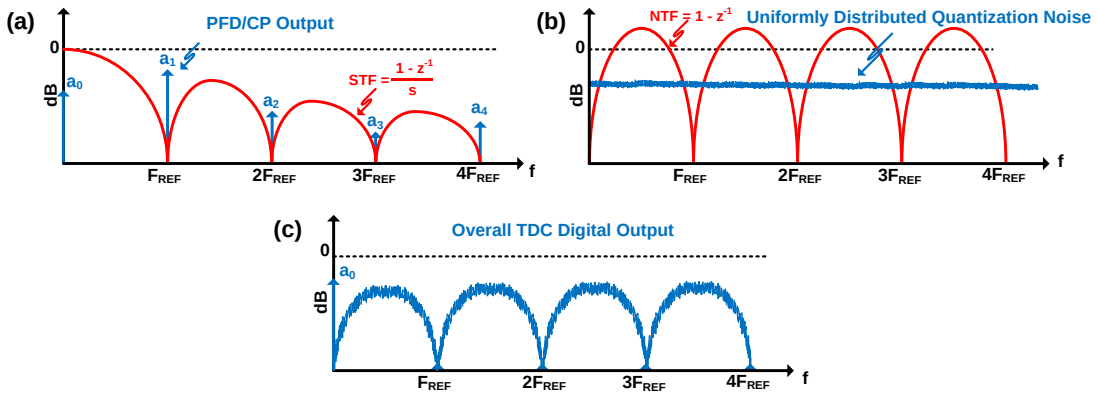

Fig. 21. (a) PFD/CP frequency domain output and CTΣΔ modulator STF. (b) Normally distributed quantization noise and CTΣΔ modulator NTF. (c) Overall TDC digital output in frequency domain.

We can analyze the behavior of a CTΣΔ modulator in time domain as well. As explained in the introduction part, CTΣΔ modulators are feedback systems that digitize the input by adjusting the digital output such that the loop filter error input becomes zero on average. If a pulse width modulated input signal is applied to a CTΣΔ, the loop filter is going to change its comparator input voltage such that the loop filter error input becomes zero on average. Fig. 22 shows a good time domain example to understand the operation of a CTΣΔ modulator in a first-order 1-bit modulator with pulse-width-modulated input signal operating at the sampling clock frequency. Here, the integrator is going to change the comparator input voltage (i.e. V_{COMP}) such that its error input is going to be zero on average (i.e. $\sum_{k=1}^{\infty} e_k = 0$), and for that to happen the average value of the digital output (i.e. $D_{OUT}[n]$) must be equal to average value of input (i.e. IN). Since the average value of our PFD output has the phase difference information, we can directly feed the output of the

charge pump from the phase/frequency detector to a CTΣΔ modulator and digitize the time difference between the CLK and the TDC input.

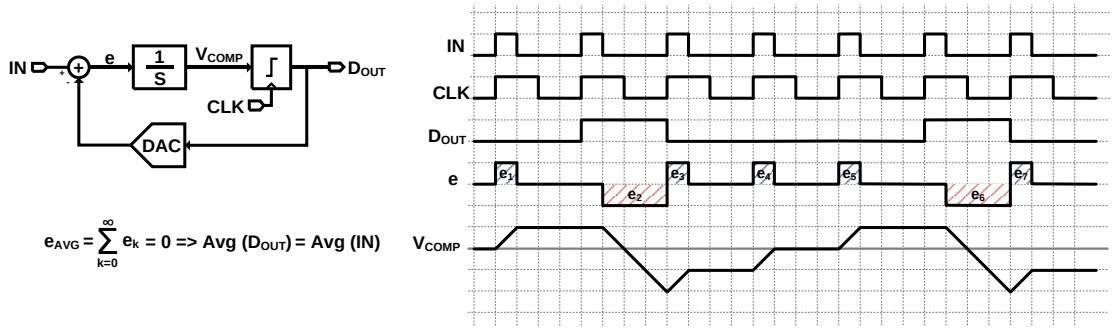

Fig. 22. Timing diagram of a 1st order 1-bit modulator when a pulse width modulated signal is applied to its input.

A third-order CTΣΔ modulator (Fig. 23) is used in this TDC structure because, a low order CTΣΔ modulator (i.e. 1st and 2nd order) can create additional tones at the output spectrum called as the limit cycles, whereas a third-order modulator eliminates those tones. More importantly, in this way the quantization noise is third-order noise shaped, allowing us to achieve a finer resolution in the chosen bandwidth. In addition, a third-order modulator has a third- order low pass filter characteristics which suppresses the high frequency tones coming from the reference clock and it acts as an antialiasing filter, because in a CTΣΔ modulator the sampling operation happens right before the comparator. To suppress the high frequency tones at the output and to have a good antialiasing filter, the third-order loop filter is implemented with a distributed feedback topology and active RC integrators. Compared to feed-forward topologies, the distributed feedback architecture does not suffer from peaking in its signal transfer function. Thus, it helps to suppress high frequency tones, as well as the charge pump and input noise at the output of the TDC. Finally, to improve the linearity of the time-to-digital converter, we use a single-bit

quantizer due to its inherent linearity. Linearity of a TDC is important to keep the loop dynamics of a PLL to be constant during operation.

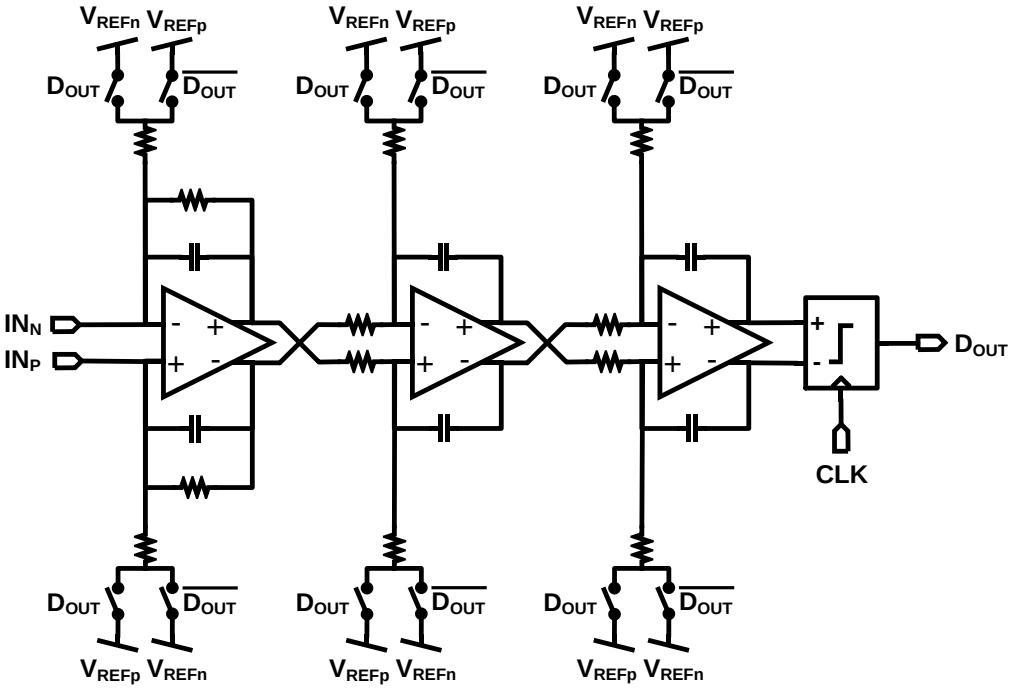

Fig. 23. Schematic of 3rd order 1-bit continuous time ΣΔ modulator.

3.3.1. Third-Order CTΣΔ-TDC Noise Analyses within a PLL

We now analyze the noise performance of the TDC within an integer-N digital PLL to show that the quantization noise is shaped and that in-band phase noise of the digital PLL's is no longer limited by it. In fact, any digital PLL with this TDC can reach the noise performance of an analog PLL. The noise performance of the TDC within an integer-N digital PLL is analyzed with the small signal model shown in Fig. 24. The signal transfer function of the CTΣΔ modulator is represented as $H_{STF}(\omega)$ while the quantizer noise transfer function is shown as $H_{NTF}(z)$. Although there are several noise sources in the PLL, only reference feedthrough (i.e. S_{Spur}), charge pump noise (i.e. S_{ICP}), and quantization noise

(i.e. S_q) come from the TDC. From Fig. 24 the effect of the TDC noise sources on the PLL phase noise (i.e. S_{OUT}) is

$$S_{OUT}(\omega) = \left|\frac{N}{K_{PFD}} * G(\omega)\right|^2 * S_{Spur}(\omega) + \left|\frac{N}{K_{PFD} * I_{CP}} * G(\omega)\right|^2 * S_{I_{CP}}(\omega) + \frac{1}{T} * \left|\frac{N * T}{I_{CP} * H_{STF}(\omega) * K_{PFD}} * G(\omega)\right|^2 * \left|H_{NTF}\left(e^{j\omega T}\right)\right|^2 * S_q(\omega) \quad (7)$$

where $G(\omega)=(PLL\_LoopGain)/(1+PLL\_LoopGain)$, $H_{NTF}(\omega)=(1-e^{j\omega T})^L$, N is division ratio, K_{PFD} is PFD gain, I_{CP} is charge pump gain, $H_{STF}(\omega)$ is signal transfer function of the CTΣΔ modulator, T is the sampling clock period, L is the loop filter order, S_{ICP} is the charge pump noise, S_q is the TDC quantization noise and S_{OUT} is the PLL phase noise. At low frequencies, within the bandwidth of the PLL, *PLL_LoopGain* is much larger than 1 and therefore the magnitude of G(ω) is equal to 1. Furthermore, the magnitude of CTΣΔ modulator STF (i.e. $H_{STF}(\omega)$) is equal to 1 and the PLL phase noise due to TDC can be simplified as

$$S_{OUT}(\omega) = \left(\frac{N}{K_{PFD}}\right)^2 * \left(\frac{S_{I_{CP}}(\omega)}{{I_{CP}}^2} + S_{Spur}(\omega)\right) + \left(\frac{N}{I_{CP} * K_{PFD}}\right)^2 * \left|1 - e^{j\omega T}\right|^{2L} * T * S_q(\omega)$$

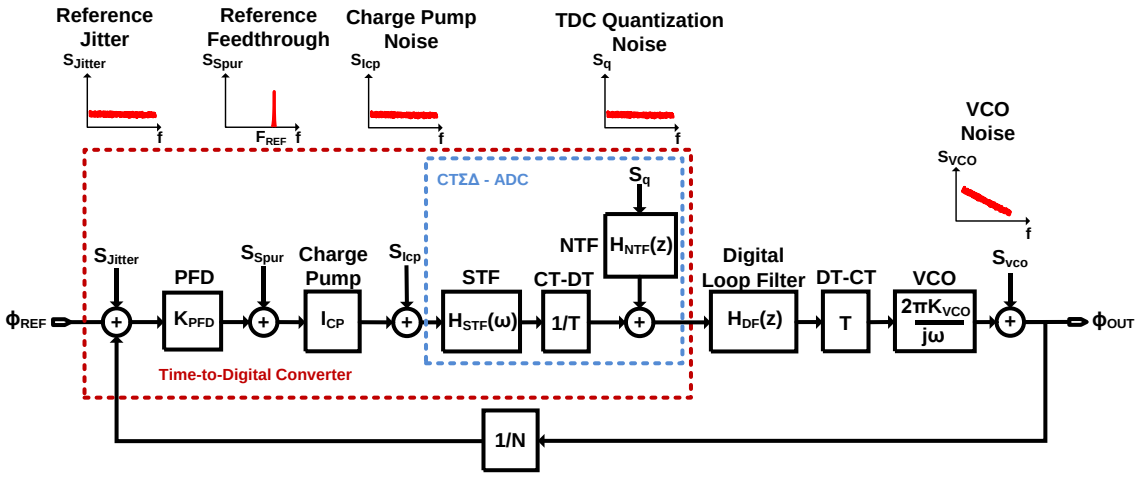

Fig. 24. Small signal model of the CTΣΔ – TDC within an integer-N digital PLL.

We see that the effect of charge pump noise (i.e. S_{ICP}) and reference feedthrough (i.e. S_{Spur}) on the PLL phase noise are identical to an analog PLL. Compared to an analog PLL, the only additional noise source is the TDC quantization error (i.e. $S_q(\omega)$). However, $S_q(\omega)$ is modified by $\left(1 - e^{j\omega T}\right)^{2L}$, which has a high pass filter characteristic, so that the quantization noise is substantially suppressed at low frequencies. For instance, the prototype TDC has a 250MHz reference sampling clock, a 1MHz bandwidth, a third order loop filter and therefore at 1MHz the spectral density of the quantization noise is attenuated by 200dB. Including the thermal noise, noise simulations of the TDC, indicate an integrated noise of 141fs within a 1MHz bandwidth. On the other hand, thanks to the noise shaping characteristics of the TDC and the 200dB attenuation factor, the simulated integrated quantization noise is only 43fs within the same bandwidth, even with the one bit quantizer. According to [53], the equivalent number bits (ENOB) of a TDC is calculated by $ENOB = (20 * log_{10}\left(\frac{Range_{2\pi}}{int_{noise}}\right) - 1.76)/6.02$ where $Range_{2\pi}$ is half of the reference period and int_{noise} is the integrated rms-noise within the bandwidth. Therefore, from the simulation results, the ENOB of our third-order TDC is 13.5 bits. The effect of TDC noise on the PLL in-band phase noise can be calculated from $S_{OUT}(f) = \frac{(2\pi)^2}{12} * \left|\frac{\Delta T}{T_0}\right|^2 * \frac{1}{F_{REF}}$ [17] where $\Delta T = \sqrt{12 * OSR} * int_{noise}$ [53], T_0 is the VCO oscillation period, OSR is the ratio of the PLL reference frequency to the TDC bandwidth, int_{noise} is the TDC integrated noise and F_{REF} is the reference frequency. Therefore, the effect of our noise shaping TDC on the in-band phase noise of a 30GHz PLL with a 250MHz reference frequency is predicted as -91.5dBc/Hz.

3.4. PLL Architecture and Implementation

This research presents two similar digital fractional-N PLLs for the MAST radar system both of which uses the third order TDC and several other common blocks. The main difference between them is that one of the these PLLs is operating at higher frequency (at 40GHz) with a ramp generation function, while the other one is operating at 30GHz and does not have the ramp generation function. Fig. 25 shows the block diagram of the 40GHz prototype. It uses one-point-modulation scheme with a third-order CTΣΔ-TDC, a digital loop filter, a 2nd order ΣΔ-DAC, an LC-VCO, a multi-modulus divider for fractional-N division, and a ramp generation block that modulates the frequency division ratio for the chirp generation.

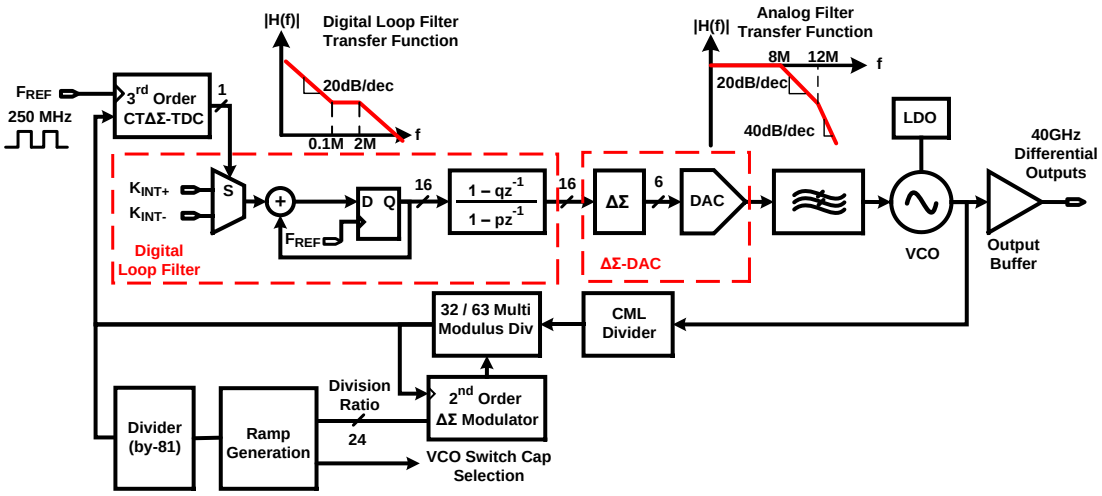

Fig. 25. Block diagram of the 34.2GHz-39GHz PLL prototype for MAST radar system.

The third-order CTΣΔ-TDC converts the phase difference between the reference clock and divided clock to an oversampled and noise shaped 1-bit digital output. The output of the TDC is connected to a digital accumulator that acts like an integrator and thus it makes the PLL a type-II system. The value of the digital word K_{INT} that is accumulated at each clock cycle has two important parameters: sign and absolute value. While the TDC output

defines the sign of this K_{INT} digital word, we can adjust its absolute value digitally from output through a serial interface. Thus, we can control the open loop gain of the PLL and therefore its closed loop bandwidth. After the integrator, a 16-bit digital filter, attenuates the high frequency noise of the TDC and stabilizes the loop. The filter pole is at 2.2MHz while it has a zero at 110kHz. This allows us to filter as much high frequency noise as noise possible while setting the closed loop bandwidth at 1MHz with a 50° of phase margin. Following the filter, first a 2nd ΣΔ modulator reduces the number of digital bits from 16-to-6, and a resistor string digital-to-analog converter (DAC) converts the 6-bit binary digital word to an analog voltage. At the output of the DAC, a second order RC low pass filter with poles at 8MHz and 12MHz filters the high frequency noise portions of the TDC even further. The filtered analog voltage controls the output oscillation frequency of an LC voltage-controlled-oscillator (LC-VCO) by changing the varactor capacitance. After the LC-VCO, the high frequency signal is divided by 4 with a current mode logic (CML) high speed divider. After the CML divider, a CMOS 32/63 multi-modules divider, controlled by the ramp generator, produces the final divided clock for the TDC and satisfies the fractional-N operation.

The higher frequency portion of the TDC quantization noise is filtered both in digital and analog domain in the PLL. The prototype TDC has a 3^{rd} order noise shaping architecture which means the PLL requires at least a fourth order low pass filter, in other words four poles. The prototype PLL is a type-II system therefore it inherently has two poles at dc; one is due to the accumulator and the other is due to the VCO. To achieve fourth order filtering, the prototype PLL has an additional second-order analog RC low pass filter with poles at 8MHz and 12MHz. This analog filter not only suppresses the TDC

quantization noise but also the ΣΔ -DAC noise as well. Thanks to the PLL filtering characteristics, there is no dedicated decimator at the output of the TDC.

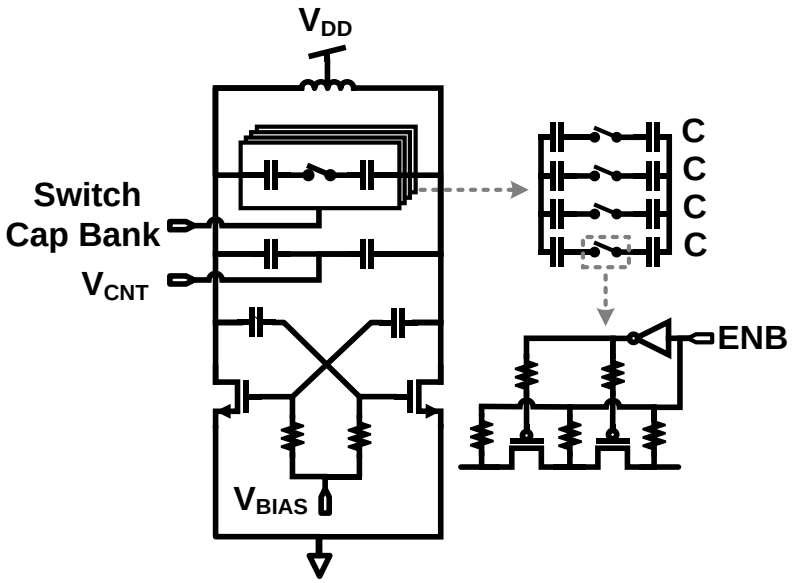

Fig. 26. Schematic of the 34.2GHz-39GHz LC-VCO.

The VCO (Fig. 26) is one of the most important blocks in a PLL design and to achieve high frequency operation, we use NMOS LC-VCO architecture rather than a CMOS approach. A varactor together with a switched capacitor bank circuit satisfy a 13% tuning range. The varactor voltage is controlled by the PLL itself, while the switch capacitor bank is operated by the ramp generator. To reduce the phase noise of an LC-VCO, it is crucial to bias the MOSFETs in saturation, while increasing the oscillation amplitude as much as possible. For this reason, we use the amplitude redistribution technique presented in [54]. This approach keeps the cross coupled transistors away from the triode region by setting the gate dc voltage less than its drain voltage, and allows more room for voltage swing without putting the transistors into triode region. Thus, it reduces the VCO phase noise without increasing its current.

3.4.1. Ramp Generator Specifications

Ramp generator block (Fig. 27) controls the output frequency of the PLL to create the 25 stepped linear frequency sweep for the radar by producing the necessary division ratio values for the divider, and by controlling the coarse tuning of the VCO. Ramp generator block uses a custom designed synchronous logic circuit to control the output frequency of the PLL, while reducing the required number of memory units. The prototype PLL uses one-point-modulation scheme, and therefore, we tune the output frequency by changing the division ratio of the divider and by selecting the correct number of switched capacitors in the VCO. Although it is possible to do this by storing each required division ratio along with the corresponding switched capacitor, such an approach consumes a lot of die area. Instead, we minimize the required number of memory elements with a custom synchronous logic circuit. We only store the division ratio value for the starting point of each 25 segment and not for the entire ramp. Therefore, the division ratio look-up table uses only 25 registers. Similarly, the switched capacitor look-up table also has 25 registers and stores one switched capacitor value for each segment. Since the VCO has a large enough frequency tuning range for each segment, we do not need to change the switch cap configuration within each segment.

The ramp generator block has two up counters, one is changing from 0-to-4095 to generate 4096 small steps and the other is changing from 0-to-24 to define the starting points of each segment which is where each frequency jump occurs. The synchronous logic adds a constant value, called the division ratio step, to the previous value of the division ratio whenever the first counter increases its output by one. When the first counter completes all the 4096 cycles, the second counter increases its output by one and selects

both the next starting point for the division ratio and the switch capacitor value for the VCO course tuning.

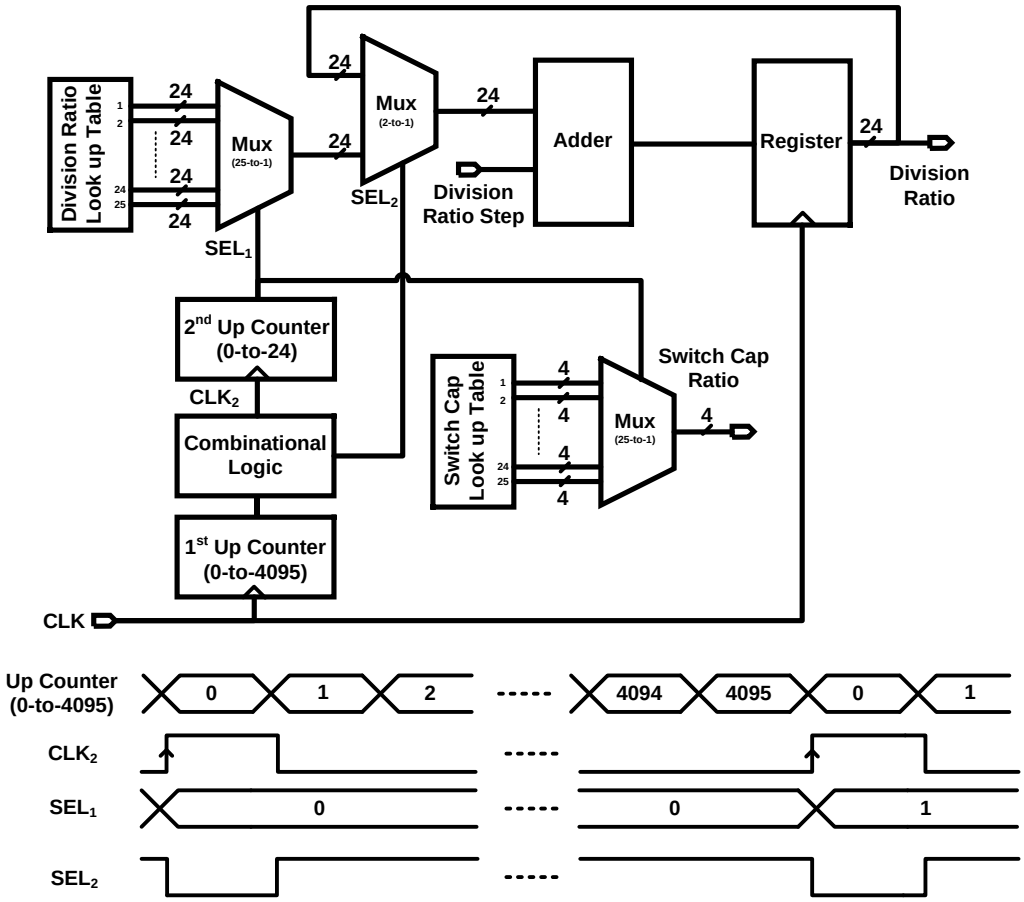

Fig. 27. Block diagram and timing diagram of the ramp generator.

3.5. Measurement Results

This dissertation presents two similar digital fractional-N PLLs for the MAST radar system. Both PLLs has the same fractional-N architecture and has several common blocks. The difference between them is that one of the these PLLs is operating between 34.2GHz-to-39GHz with a ramp generation function, while the other one is a 28.5-33.5GHz PLL without the ramp generation function. Both PLL prototypes are fabricated in 65nm CMOS and all testing is done with QFN packaged devices. To fully quantify the performance of

the fabricated prototypes, we performed both the stand-alone TDC measurements and PLL measurements.

3.5.1. Time-to-Digital Converter Measurements

A time-to-digital converter digitizes the time difference between the edges of two different signals, however, the measurement results will significantly depend on the overall jitter performance of the test environment. Therefore, to minimize the overall jitter in the system we used two low phase noise Keysight 5183B signal generators, one for the reference clock and one for the input source to the TDC. The measurement setup to perform the TDC integrated-rms noise measurements is shown in Fig. 28. The two signal generators are locked to each other by using a low phase noise 10MHz reference input. The reference clock frequency is set to constant 250MHz, and a phase modulated signal around 250MHz is applied to the TDC input. However, the generated phase modulated sinusoidal signal from the signal generator is non-linear itself and the input phase spectrum contains several harmonics. Therefore, the TDC is tested with small signal inputs which represents the case when the PLL is locked. Because when it is locked, the input to the TDC is going to be a small signal. We used bandpass filters to suppress the signal generators harmonics.

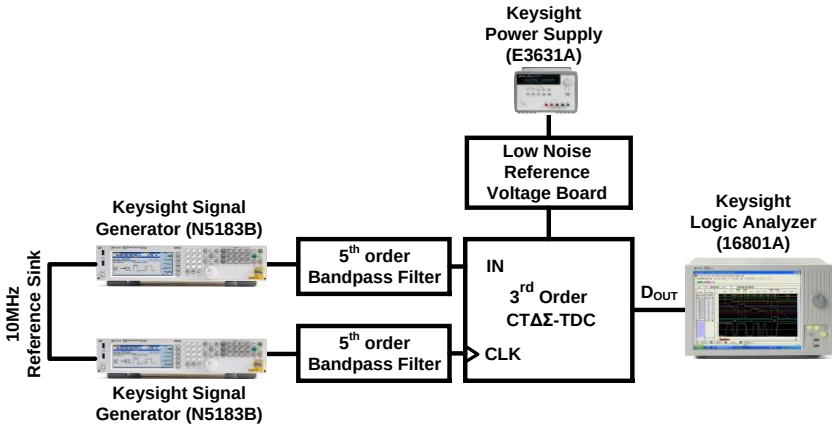

Fig. 28. Time to digital converter integrated noise test measurement setup.

Fig. 29(a) shows the frequency domain TDC outputs when an input with $6ps_{pp}$ amplitude at 100KHz is applied to the TDC input. To measure the power spectral density of the TDC output a 65,536 point FFT is performed. The TDC output power spectral density shows third-order noise shaping characteristics with a 60dB/decade slope. By integrating the noise at the TDC output up to 1MHz signal bandwidth, we calculate the rms noise as 182fs. The minimum delay that can be achieved with TSMC 65nm process is on the order of 10psec and Fig. 29(a) shows the noise power spectral density of an ideal delay line TDC with 10psec and 1psec delay cells. Clearly, the noise floor of the third-order CTΣΔ-TDC within 1MHz bandwidth is much lower than the 65nm process can achieve with a delay line TDC. Fig. 29(b) shows the time domain digital output of the TDC after its digitally filtered with a 1MHz bandwidth and decimated by 125. Clearly, the TDC can resolve a $6ps_{pp}$ signal which was the smallest signal that we can give from our test setup.

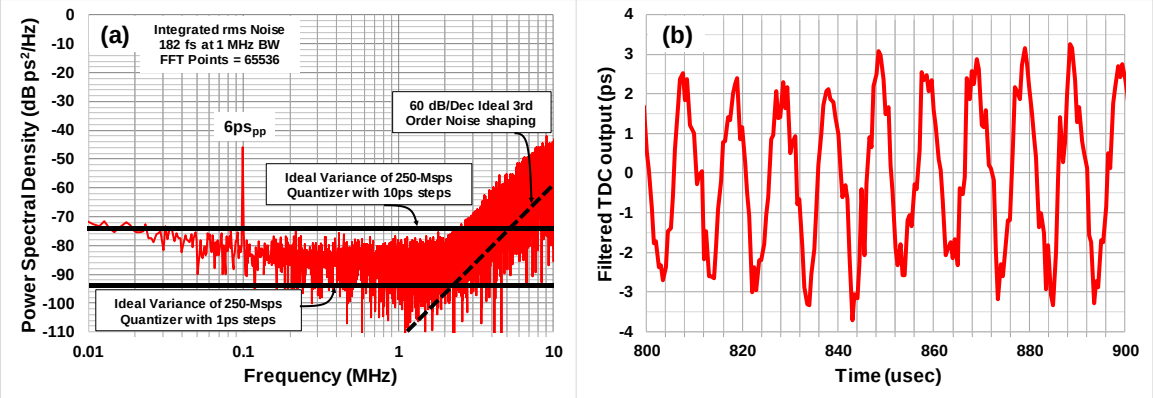

Fig. 29. (a) Measured output spectrum of the TDC when a $6ps_{pp}$ amplitude at 100KHz sinusoidal signal is applied to its input (TSMC 65nm process has a minimum delay of 10psec). (b) Measured TDC output after it is filtered by a 1MHz digital LPF and decimated by 125 for a $6ps_{pp}$ input at 100KHz.

Fig. 30(a) shows the frequency domain measurement results of the TDC when the input amplitude is increased to $64ps_{pp}$. Again, the TDC output shows third-order noise shaping characteristics and the calculated integrated-rms noise in 1MHz bandwidth is 176fs

(excluding the harmonic tones due to the phase modulated input source). Fig. 30(b) shows the time domain digital output of the TDC of the $64ps_{pp}$ signal at 100KHz after its digitally filtered with a 1MHz bandwidth and decimated by 125.

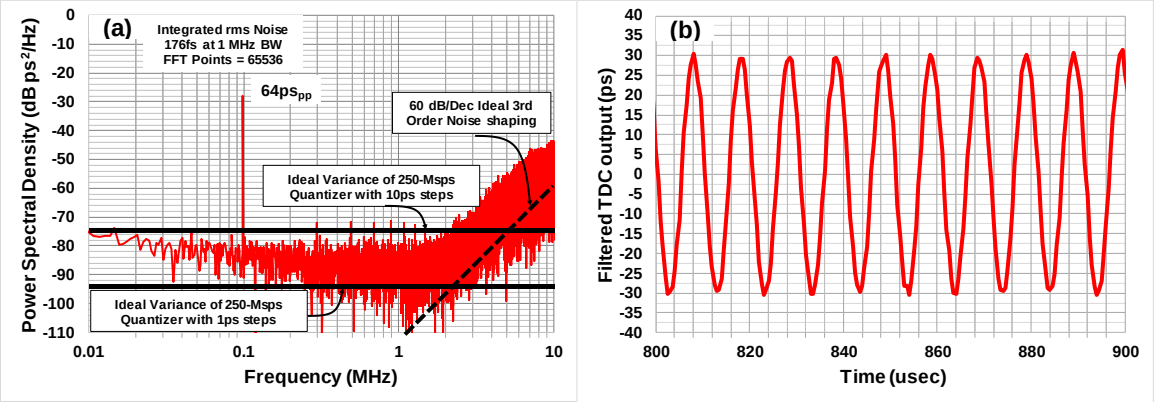

Fig. 30. (a) Measured output spectrum of the TDC when a 64pspp amplitude at 100KHz sinusoidal signal is applied to its input. (176fs integrated rms-noise excluding the harmonic due to the phase modulated input signal). (b) Measured TDC output after it is filtered by a 1MHz digital LPF and decimated by 125 for a 64pspp input at 100KHz.

Based on these noise measurement results, the dynamic range of the modulator is calculated as 81dB by using the equation $DR = 20 * log(Range_{2\pi}/integrated\_noise)$ where $Range_{2\pi}$ is 2nsec and integrated noise is 176fs. Thus, the effective number of bits (ENOB) is calculated as 13.2bits. The TDC consumes 8.4mW of power thus the energy efficiency (FoM_W) of the TDC is calculated as 446fJ/conv-step by using $FoM_W = {Power}/{(2 * BW * 2^{ENOB})}$.

Table I shows the measured performance results of the TDC and compares it with the state-of-the-art noise shaping TDCs. The proposed TDC is fabricated with 65nm CMOS process and occupies $0.055mm^2$ while consuming 8.4mW power from 1.2V supply voltage. It does not require any kind of calibration and achieves 176fs integrated-rms noise in 1MHz bandwidth with third-order noise shaping. Due to the phase domain input, it can

cover the whole 2π range and thus the PLL does not require additional frequency lock loop. It has 81dB dynamic range with an ENOB of 13.2bits and FoM_W=446fJ/conv-step for 1MHz bandwidth operating at 250Msps.

Table I. TDC performance comparison with the state of the art noise shaping TDCs.

	This Work	Y. Wu [RFIC 2015]	A.Elshazly [ISSCC 2012]	Y. Cao [ISSCC 2011]	C. Hsu [ISSCC 2008]	B. Young [CICC 2010]
Technology [nm]	65	40	90	130	130	90
Supply [V]	1.2	1.1	1	1.2	1.5	1.2
Power [mW]	8.4	1.32	2	1.7	21	2.1
Bandwidth [MHz]	1	1.25	1	0.1	1	1
Type	CTΣΔ	Flash-ΣΔ	SRO	MASH	GRO	ΣΔ
Area [mm^2]	0.055	0.08	0.02	0.11	0.04	0.12
Fs [MHz]	250	50	500	50	50	156
$Integrated_{RMS}$ Noise [fs]	176	103	315	5600	80	2400
$Range_{2\pi}$ [ns]	2	0.32	5	10	0.564	3.2
DR[(a)] (dB)	81	70	84	65	77	62.5
ENOB[(b)] [bits]	13.2	11.3	13.7	10.5	12.5	10.1
$FoM_{2\pi}$[(c)] [pJ/step]	0.45	0.2	0.08	5.8	1.8	0.96

(a) $DR=20*\log_{10}(Range2\pi/Integrated_{RMS}\ Noise)$

(b) ENOB=(DR-1.76)/6.02

(c) $FoM_{2\pi}=Power/(2*BW*2^{ENOB})$

3.5.2. Phase Lock Loop Measurements

Both PLLs are fabricated in TSMC 65nm process and while the 28.5-33.5GHz fractional-N PLL has an active area of 0.18mm^2 (Fig. 31(a)), the 34.2GHz-to-39GHz one has an active area of 0.217mm^2 (Fig. 31(b)). In terms of power consumption, the 30GHz PLL consumes 34.8mW from 1.2V supply, while the 40GHz one uses 40mW of power excluding the power consumed by the power amplifiers at the output. For both of these PLLs, the divider chain dissipates the largest portion of the power which is 13.2mW for the 30GHz PLL and 16mW for the 40GHz one. For the VCOs, the 40GHz one uses 12.6mW power, while the 30GHz VCO consumes 9.6mW power. Since the rest of the circuit is same for both PLLs, their power consumptions are identical too. The TDC consumes 8.4mW and the digital circuits uses 3mW of power from 1.2V supply voltage.

The PLL is wired bonded in a 20-pin QFN package and soldered on a high-frequency printed circuit board.

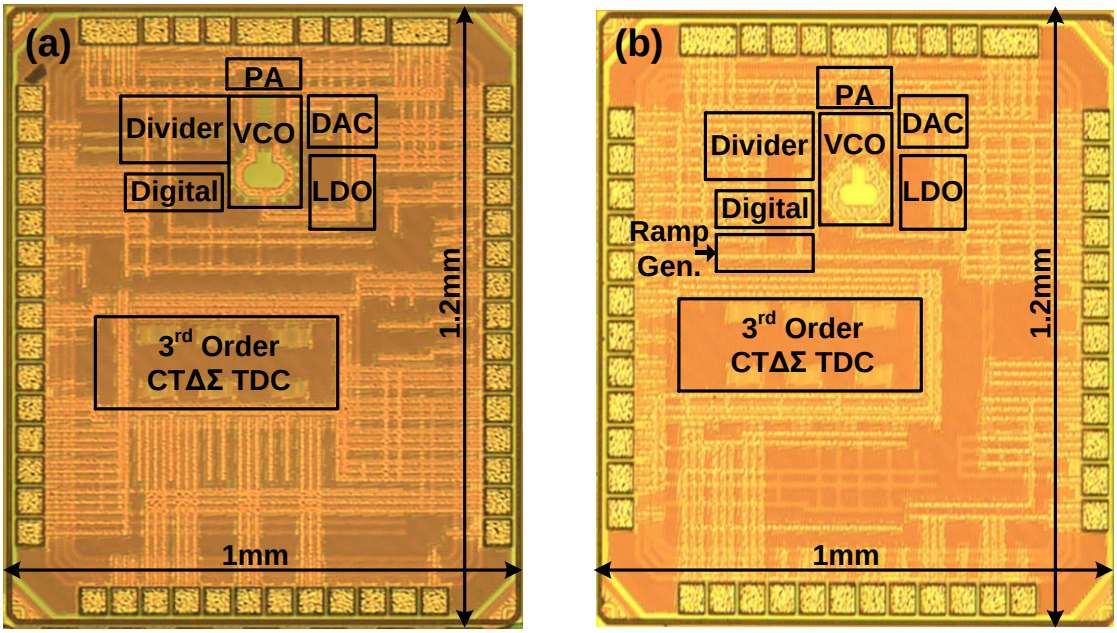

Fig. 31. (a) 30GHz fractional-N PLL die micrograph. (b) 40GHz fractional-N PLL die micrograph.

Fig. 32(a) shows the open loop LC-VCO oscillation frequency measurement results for 30GHz VCO while Fig. 32(b) shows the 40GHz LC-VCO open loop oscillation frequency. While the 40GHz LC-VCO has a linear gain of 2.5GHz/V and its oscillation frequency is extended to 34.2GHz-to-39GHz with a switch capacitor bank, the 30GHz LC-VCO has a 1.5GHz/V linear gain and its frequency range is extended to 28.5GHz-to-33.5GHz.

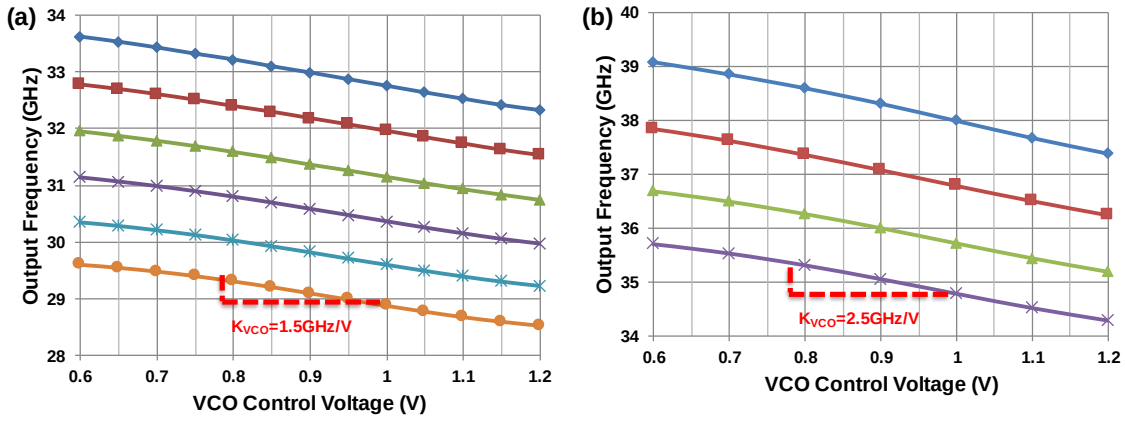

Fig. 32. (a) 30GHz LC-VCO open loop oscillation frequency vs control voltage. (b) 40GHz LC-VCO open loop oscillation frequency vs control voltage.

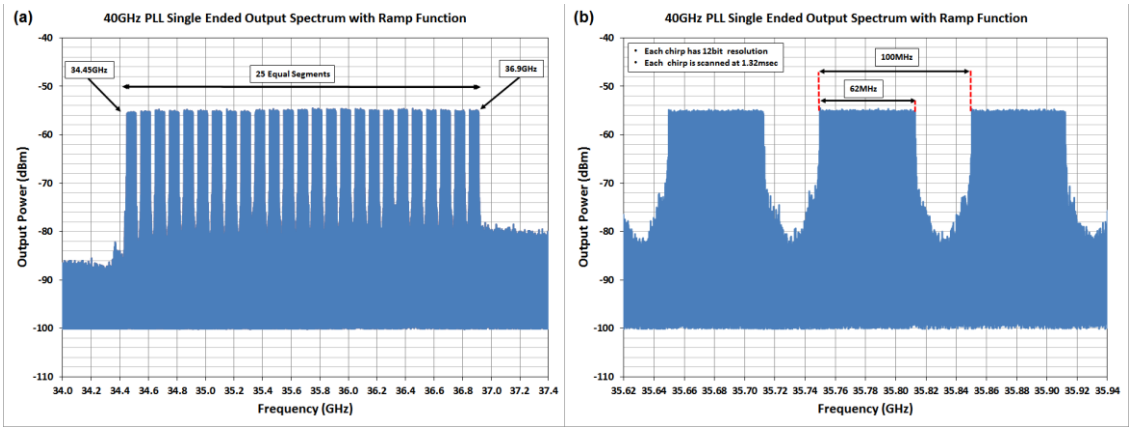

Fig. 33. Measured output spectrum of the 40GHz PLL when the ramp generation function is enabled. (a) Full spectrum from 34.4GHz-to-36.9GHz. (b) Zoomed spectrum from 35.6GHz-to-35.9GHz to see 3 segments.

The ramp generation function of the 40GHz PLL is tested by looking at the output spectrum of the PLL. In order to measure the ramp generation function first, the 40GHz PLL is locked to 250MHz reference frequency, then the ramp generation function is enabled and the output spectrum of the PLL is recorded with a spectrum analyzer. Fig. 33 shows the measured output spectrum of the PLL when the ramp generation function is enabled. The output of the PLL composed of 25-step chirp signal ranging from 34.45GHz-to-36.9GHz, where each step is composed of 62MHz linear chirp and 38MHz step afterwards. Each chirp has 12bit resolution and scanned in 1.32ms.

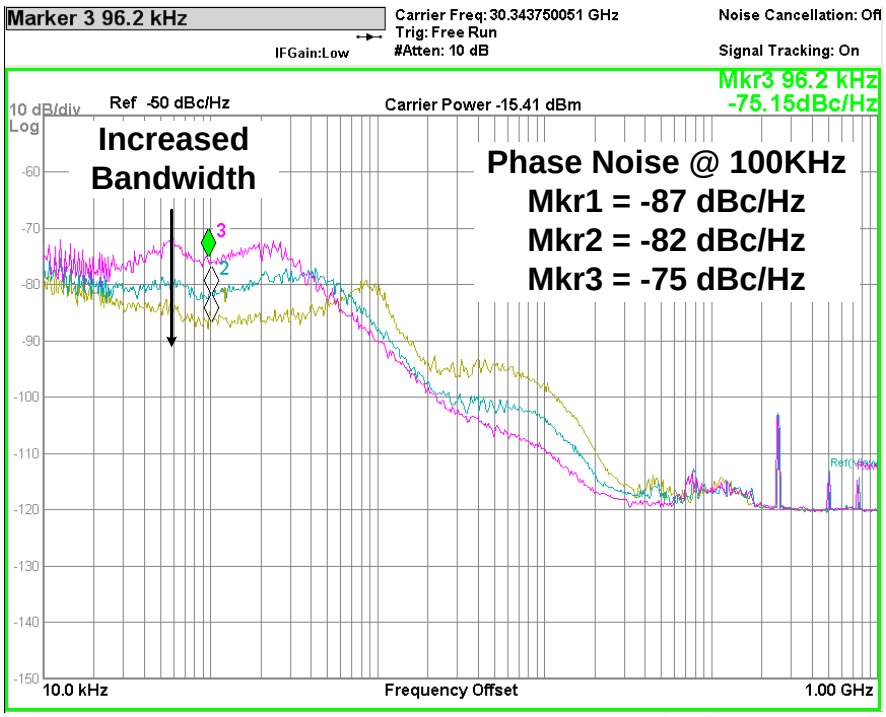

Fig. 34. Phase noise measurements of single ended output of the 30GHz PLL for low (200KHz), medium (500KHz), and high (1MHz) bandwidth settings at 30GHz measured with Keysight N9010A signal analyzer.

The effectiveness of the TDC to the in-band phase noise of a PLL is measured with the 28.5-33.5GHz fractional-N PLL [52] and it is measured for three different PLL bandwidth conditions (Fig. 34). For the highest loop bandwidth case (1MHz) the in-band phase noise is measured as -87dBc/Hz at 100KHz offset which gives an integrated-rms jitter from 10KHz-to-1MHz is 545fsec resulting an -230dB FoM_{Jitter} and normalized in-band phase noise of -212.6dBc/Hz^2. In addition to that thanks to the third-order filtering characteristics of the TDC, the measured worst case reference spur when the PLL is locked is -40dBc for single ended output as shown in Fig. 35.

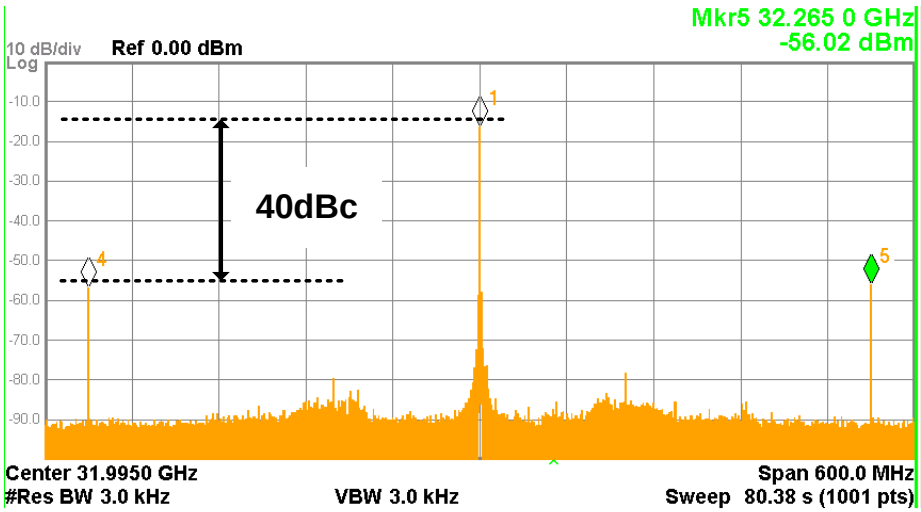

Fig. 35. Single ended output spectrum of the 30GHz PLL when it is locked to 32.2GHz.

Table II summarizes the performance of both 30GHz and 40GHz PLLs and compares it the state of the art digital and analog PLLs over 10GHz. Fig. 36(a) shows the normalized phase noise comparison of the 30GHz PLL with the state of the art digital and analog PLLs over 10GHz and Fig. 36(b) show the FoM_{Jitter} comparison of the 30GHz PLL with the state of the art digital PLLs over 10GHz. Compared to the previous state of the art high frequency (>10GHz) digital PLLs, the normalized phase noise of the 30GHz PLL is 5dB better than any published high frequency digital PLLs.

Table II. PLL (Over 10GHz) performance summary and comparison

	This Work [30GHz PLL]	This Work [40GHz PLL]	V. Szortkya [ISSCC 2014]	X.Yi [ISSCC 2013]	W. Wu [JSSC 2014]	M. Ferris [VLSI 2013]	M. Ferris [ISSCC 2015]	A. Rylyakov [ISSCC 2009]	C. Li [VLSI 2016]
Technology [nm]	65	65	40	65	65	32 [SOI]	32 [SOI]	65	10 [Finfet]
Type	DigFrac-N	DigFrac-N	AnalogInt-N	AnalogInt-N	DigFrac-N	Hybrid Int-N	Hybrid Frac-N	DigInt-N	DigFrac-N
Tuning Range [GHz]	28.5 – 33.5	34.2 - 39	53.8 - 63.3	57.9 - 68.3	56.4 - 63.4	23.8 – 30.2	13.1 – 28	16.3-22.3	10.8-19.3
Ref. Freq [MHz]	250	250	40	135	100	200	100	275	150
Freq. Resolution [MHz]	0.004	0.004	40	135	10 – 100	NA	NA	275	NA
Bandwidth [MHz]	1	1	NA	NA	0.5	1	1	1	1
Phase Noise @ 100kHz [dBc/Hz]	-87	NA	-87	-85.5	-72	-84	-80	-85	-87
Area [mm^2]	0.18	0.217	0.16	0.19	0.48	0.03	0.24	0.11	0.034
Power [mW]	34.8	40	42	24.6	48	32	31	64.15	11.9
Supply [V]	1.2	1.2	0.9/1	1.2	1.2	1	1	1.1/1.2	0.8
Norm. Phase Noise @100kHz [dBc/Hz^2] [a]	-212.6	NA	-226.2	-220.2	-207.6	-209.9	-206.4	-206.6	-206.8
$Jitter_{RMS}$ [fs] [b]	545	NA	287	238	779	468	945	NA	565
FoM_{Jitter} [dB] [c]	-229.9	NA	-234.6	-238.6	-225.4	-231.5	-225.6	NA	-234.2

[a.] Norm Phase Noise = Phase Noise – 20log(Division Ratio) – 10log(Reference Frequency)

[b.] $Jitter_{RMS}$ is calculated from phase noise plots from 10kHz-to-1MHz for all PLLs

[c.] $FoM_{Jitter} = 10\log[(Jitter_{RMS}/1s)^2 * Power/1mW]$

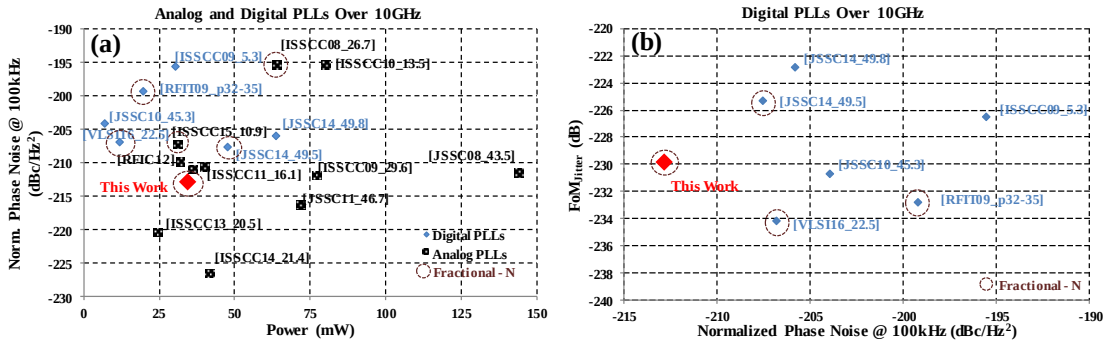

Fig. 36. (a) 30GHz PLL normalized phase noise @100KHz comparison with analog and digital PLLs over 10GHz. (b) 30GHz PLL FoMJitter comparison with digital PLLs over 10GHz.

3.6. Conclusion

This dissertation introduces a new third-order continuous-time sigma delta (CTΣΔ) based noise-shaping time-to-digital converter for high frequency digital PLLs. With this new noise shaping TDC technique, the digital PLL in-band phase noise is no longer limited by quantization noise, and it has the advantages of an analog PLL while retaining the benefits of digital PLLs. Thus, it became possible to benefit the advantages of digital techniques while satisfying the low phase noise and fast settling time requirements in a digital PLL. To show the effectiveness of this new technique, we present two high frequency digital PLLs which are designed as signal sources for an imaging and navigation radar system operating at 240GHz center. The first PLL is a 34.2-39GHz fractional-N one with a ramp-generator while the second one is a 28.5-33.5GHz fractional-N PLL [52] without the ramp generation function. The prototype TDC has an excellent measured time resolution n of 176fs in a 1MHz bandwidth. The new TDC enables a measured in-band phase noise of -87dBc/Hz (at a 100kHz offset), a normalized phase noise of -213dBc/Hz^2, and an FoM_{Jitter} of -230dB from the prototype mostly digital fractional-N 28.5GHz-to-33.5GHz PLL.

CHAPTER 4. 5GS/s CTΣΔ ADC with Time-Interleaved Reference Data Weighted Averaging (TI-RDWA)

4.1. Limitations with High Speed Sampling CTΣΔ Modulators

Emerging wireless communication standards with Gbit/s data rates, such as LTE-advanced, will transform mobile devices, but depend on wide bandwidth (>100MHz), high dynamic range (DR) (>70dB), high SFDR (>80dB) analog to digital converters (ADCs). Continuous time (CT) ΣΔ ADCs are very attractive because they provide many system-level advantages including simplified filtering and an easy to drive input. However, the combination of high bandwidth and high dynamic range is challenging due to feedback DAC mismatch and loop delay. A 100MHz+ bandwidth high DR modulator requires a high-order loop filter, a GHz+ sampling clock and a multi-bit quantizer [24]. A significant challenge for multi-bit operation is that DAC mismatch limits the linearity and thus also the SFDR and DR of a multi-bit ΣΔ modulator. Furthermore, these linearity requirements are especially hard for GS/s operation because GS/s modulators also suffer from dynamic mismatch effects, such as timing skew, which get worse with the increased DAC area.

Conventional methods for dealing with feedback DAC mismatch do not work well at high speed. Static DAC mismatch can either be suppressed by using large devices or by adding small amounts of dither, but large devices increase DAC area, which in turn means more timing skew, and dither increases in-band noise. Conventional Dynamic Element Matching (DEM) techniques, such as data-weighted-averaging (DWA), allow smaller

DAC unit elements for the same linearity, and therefore can also reduce the timing skew. Unfortunately, traditional DWA architectures are not practical for high modulator speeds because they introduce too much delay in the modulator feedback.

For these reasons, state-of-the-art high-speed (GS/s) CTΣΔ modulators either use big DACs [24, 39, 40] and consequently burn extra power to reduce timing skew, or alternatively employ extensive DAC calibration [41]. [55] presents the intriguing alternative of shuffling the reference voltages of the quantizer comparators, but it introduces a new delay due to reference switching that limits the shuffling rate.

4.2. Data Weighted Averaging (DWA)

In CTΣΔ the accuracy of the feedback DAC defines the linearity performance of the analog-to-digital converter. CTΣΔ modulators are feedback systems where the digital-analog-converter is located at the feedback. Therefore, like in any feedback system their linearity performance is limited by the feedback circuit. For instance, for a CTΣΔ modulator with N-bits of resolution, the feedback DAC needs to satisfy N-bits of linearity. However, as it is explained in section 2.1.2.1, multi-bit DACs suffer from mismatch effects, and limit the CTΣΔ modulator's SFDR. Data-weighted-averaging (DWA) algorithm rotates the DAC unit elements (Fig. 37) to make the long-term average use of each unit element to be same. For instance, consider a multi-bit DAC with 13 unit elements. If the first code is 2, then the first two unit elements (i.e. S[0:1]) will be used. Suppose the next cycle is 5, then this time the next 5 unit elements (i.e.S[2:6]) will be selected. Let the next code be 7, then the DAC will wrap around and use elements from S[7:12] and S[0]. In this way, the DWA algorithm guarantees that each DAC unit element is selected in equal probability on average and therefore shape the DAC mismatch effects.

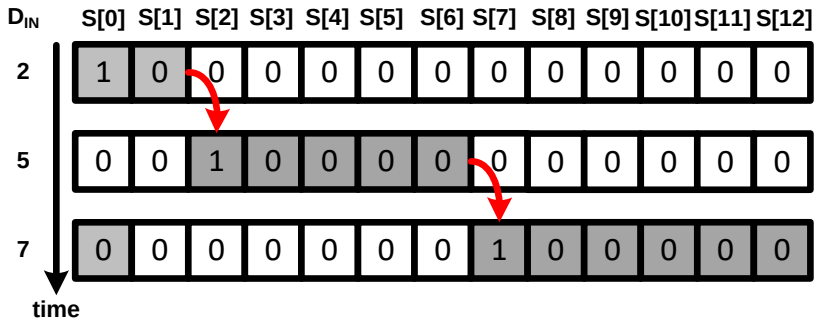

Fig. 37. Data-weighted averaging algorithm

4.3. CTΣΔ TI-RDWA ADC Architecture

In ΣΔ modulators, the traditional DWA algorithm sequentially selects DAC elements, starting with the next available unused one. In this way, each unit cell of the DAC array is selected with equal probability and mismatch effects are first-order shaped. However, conventional dynamic element matching (DEM) methods to counter DAC mismatch, such as DWA, introduce too much delay in the feedback to be effective at high speeds and thus not suitable for high speed CTΣΔ modulators.

In a CTΣΔ ADC, each DAC unit element is physically connected to a corresponding comparator in the flash quantizer. Therefore, shuffling the reference voltage connections (Fig. 38(a)), or in other words, reference data weighted averaging (i.e. RDWA), is equivalent to digitally shuffling the quantizer outputs in traditional DWA. An important advantage of RDWA is that it removes the digital delay of the DWA decoder from the ΣΔ loop. However, with RDWA the maximum operating frequency is now limited by the reference switching delay and this delay increases with the number of levels in the quantizer. As an example, in 40nm CMOS process, the minimum RC time constant (τ) of a 13-level reference switching matrix is around ~50ps, assuming a 25fF comparator input

capacitance (Fig. 38(b)). Thus, the reference switching is restricted to a maximum operating frequency of ~3GHz for a 5% settling error.

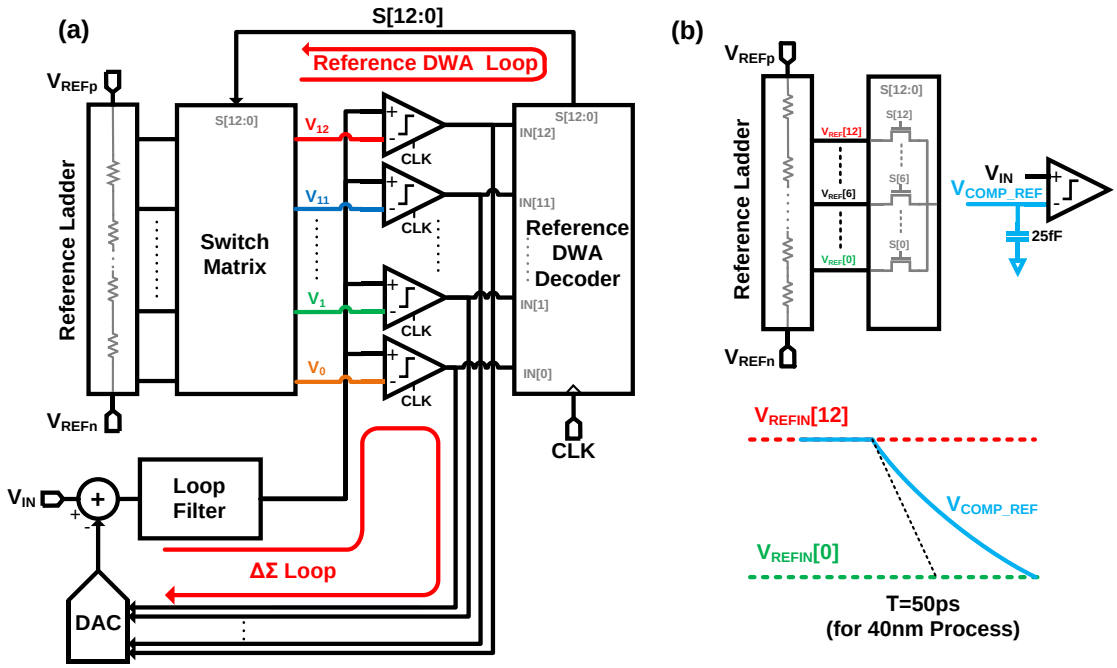

Fig. 38. (a) Block diagram of the high speed CTΣΔ modulator with Reference DWA architecture. (b) RDWA speed limitation due to reference shuffling RC time constant

We introduce a 5GS/s CTΣΔ ADC that uses a Time-Interleaved Reference Data Weighted Averaging (TI-RDWA) architecture (Fig. 39) to eliminate the DEM decoder delay in the feedback loop, and to solve the delay problem due to reference settling in RDWA. In TI-RDWA, we double the effective reference shuffling time by interleaving two quantization channels (i.e. CH1 and CH2). These channels operate at the half clock rate from complimentary clock signals. While one channel quantizes the loop filter output, the other shuffles (i.e. rotates) its reference voltages based on the previous ADC output.

Fig. 39 shows a block diagram of the new CTΣΔ TI-RDWA ADC architecture. It is composed of two separate loops: a ΣΔ loop for the quantization noise shaping and TI-RDWA loop for DAC mismatch shaping. The ΣΔ loop is composed of the loop filter, two

time-interleaved quantizers (i.e. CH_1 and CH_2) and a full rate feedback DAC. The TI-RDWA has a reference DWA decoder, a 13-level resistor ladder and two time-interleaved quantization channels. Each quantization channel has a 13-level flash quantizer, a re-timer and a reference switch matrix. The reference DWA decoder keeps track of the reference rotation, and generates a new one-hot code every clock cycle (i.e. S[12:0]) depending on the quantizer output. This one-hot pointer (S[12:0]), operating at full clock rate, alternately sets the reference connections for each of the quantizers.

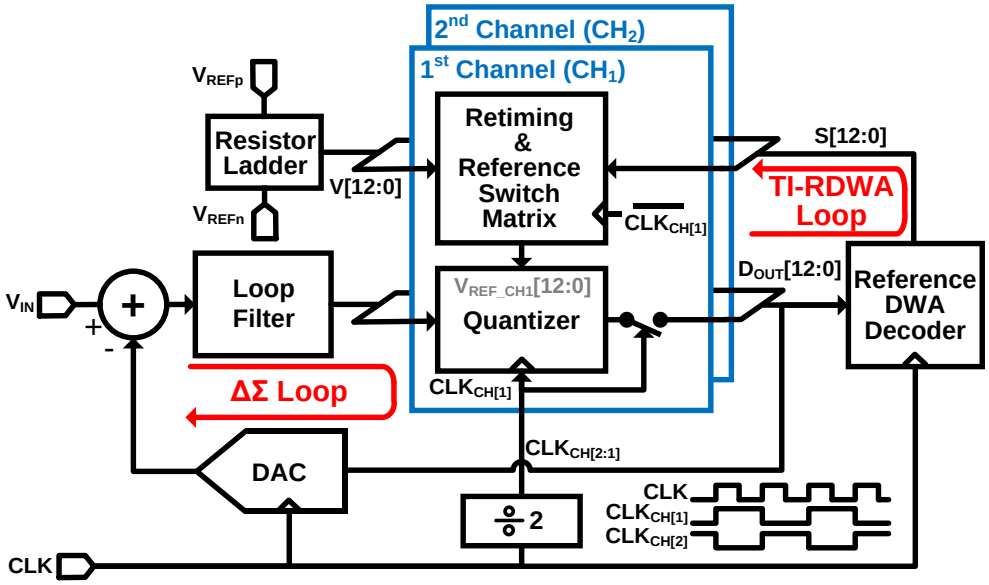

Fig. 39. (a) Block diagram of the high speed CTΣΔ modulator with the proposed Time-Interleaved Reference DWA architecture.

Fig. 40 shows the detailed single-ended block diagram of a single channel in the TI-RDWA structure. Each channel has 13 clocked comparators. Each interleaved channel latches S[12:0] using its own half-rate clock to generate an internal one-hot pointer (i.e. S_{CH1}[12:0] and S_{CH2}[12:0]). These internal pointers control the reference switch matrix in each channel. For the 13 possible rotations indicated by the one-hot code (i.e. S_{CH1} or S_{CH2}), one of 13 switches for each comparator connects the comparator reference input to the

appropriate ladder tap. Thanks to interleaving-by-two, both the quantization and reference shuffling operate at the half clock rate from complimentary clock signals (i.e. $CLK_{CH[1]}$ and $CLK_{CH[2]}$). The reference DWA decoder still operates at the full rate clock (i.e. CLK).

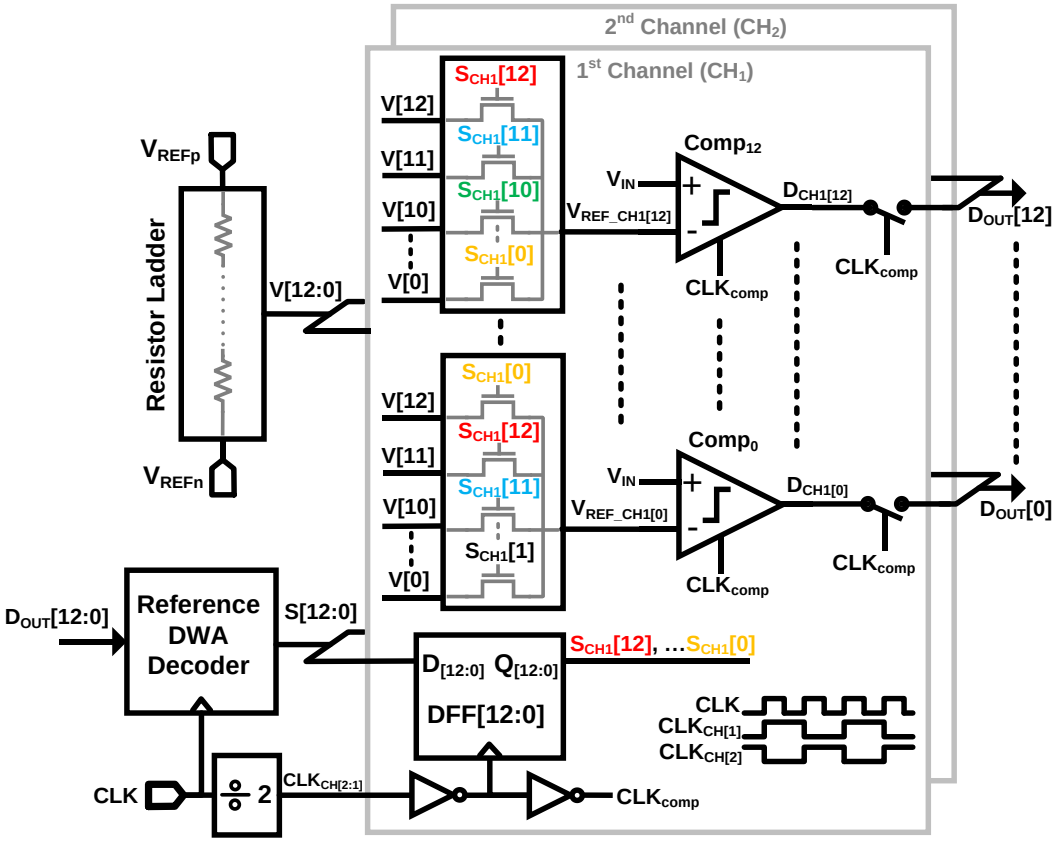

Fig. 40. Single ended block diagram of TI-RDWA loop.

The one-hot pointer, S[12:0] is first sampled with the half rate clock generating internal one-hot pointers (i.e. $S_{CH1}[12:0]$ and $S_{CH2}[12:0]$) in each of the channels. $S_{CH[2:1]}[12:0]$ controls the operation of the reference switch matrix by closing one of the 13 switches for every comparator and connecting the necessary reference voltages to comparator inputs. Therefore, as S[12:0] shuffles, the reference voltages shuffle. Since the amount of rotation, decided by the reference DWA decoder, depends on the output of the quantizer, the DAC mismatch effects are first-order shaped. Meanwhile, the comparator sampling operation in

each channel is controlled by the comparator clock (i.e. CLK_{comp}) which is an inverted version of the internal reference shuffling operation. In this way, we guarantee that the sampling happens well after the reference shuffling. Fig. 41 shows the timing diagram for reference shuffling and examples of how the reference connection for three of the 13 comparators in both channels changes with time.

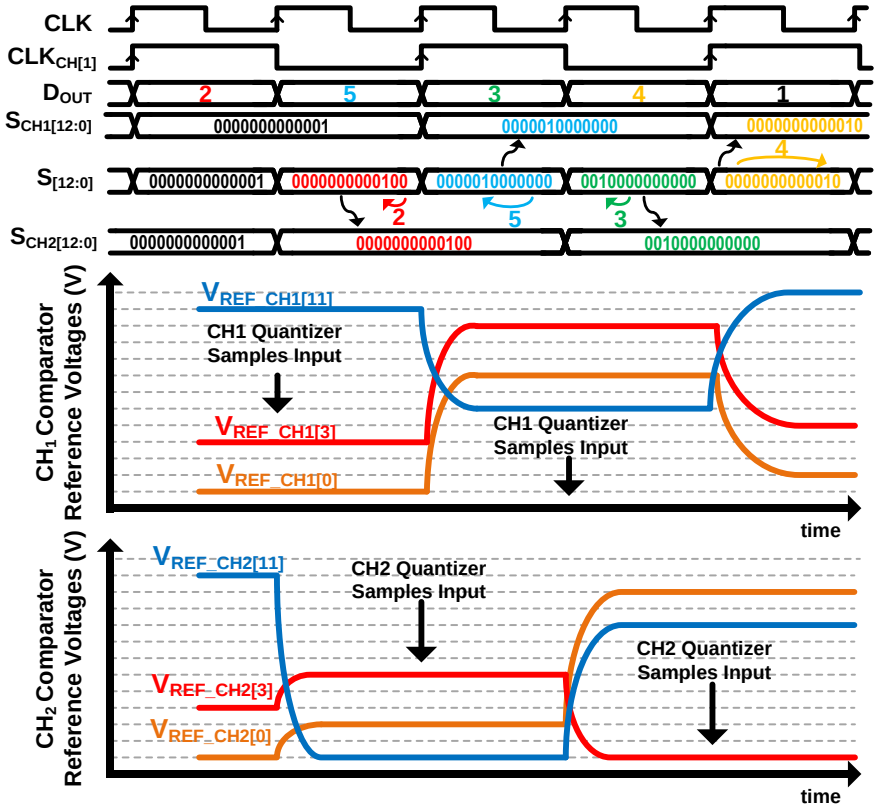

Fig. 41 Timing diagram for reference shuffling and sample comparator reference voltage rotation for three comparators (0,3 and 11) in channels 1 (CH_1) and channel 2 (CH_2).

The key advantage of TI-RDWA is that the noise-shaping loop and the mismatch-shaping loop are totally separated from each other. Thus the DWA decoder propagation delay does not affect the modulator loop delay while it still first-order shapes the DAC static mismatch effects. Therefore, the same linearity is satisfied with a smaller DAC size, which means less DAC area, less parasitics and thus less timing skew. Because of this, we

can either increase the operating frequency of the modulator for the same power or decrease its power consumption for the same bandwidth.

4.4. Circuit Implementation

4.4.1. Reference Data-Weighted Averaging Decoder

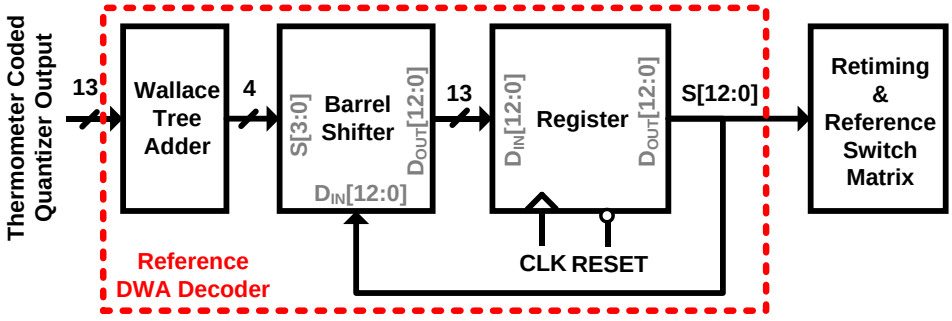

Fig. 42 Block diagram of the reference DWA decoder.

The element selection logic (Fig. 42) is at the core of TI-RDWA and generates S[12:0], the one-hot digital control word that controls the reference switch matrix. The TI-RDWA algorithm is implemented with four sub-circuit blocks: a 13 input Wallace-tree adder, a barrel shifter, a 13-bit register, and a reference switch matrix. Every clock cycle a high-speed adder sums the thermometer code output of the 13-level quantizer. Encoding with a summer eliminates bubbles and sparkles. Next, depending on this 4-bit binary code, a barrel shifter rotates the 13-bit one-hot pointer. Afterwards, the output code of the barrel shifter is re-timed and stored in a 13-bit register which is fed back to the barrel shifter to set its next state input. At the same time, the output of the register (S[12:0]) drives the reference switch matrix. Since the barrel shifter and the register form a closed loop, the starting code for the barrel shifter input is defined by the reset state (i.e. RESET) of the 13-bit register. Although, the barrel shifter requires several multiplexers, thanks to the TI-

RDWA, it does not slow down the modulator, because the ΣΔ loop and DWA loop are separated. Therefore, any digital operation in the reference shuffling loop can be pipelined.

4.4.2. Third Order CTΣΔ Modulator Architecture

A third-order feed-forward modulator architecture (Fig. 43) minimizes the amplifier output swing and the power consumption of the ADC for high speed operation. The loop filter is implemented as RC integrators with feed-forward coefficients (R_{F1}, R_{F2}, and R_{F3}), which are then summed by a passive resistive summer (R_{SUM}), before the quantizer, to further reduce the power consumption. The time-interleaved multi-bit quantizer has 13 two-stage fully dynamic comparators per channel. Because of the dynamic operation of the comparators, the quantizer power consumption does not increase with interleaving. Any excessive loop delay in the feedback path is corrected by adjusting the delay of the feedback DACs clock signal. The excess loop delay compensation is achieved when the delay is set to 3/4th of the clock period.

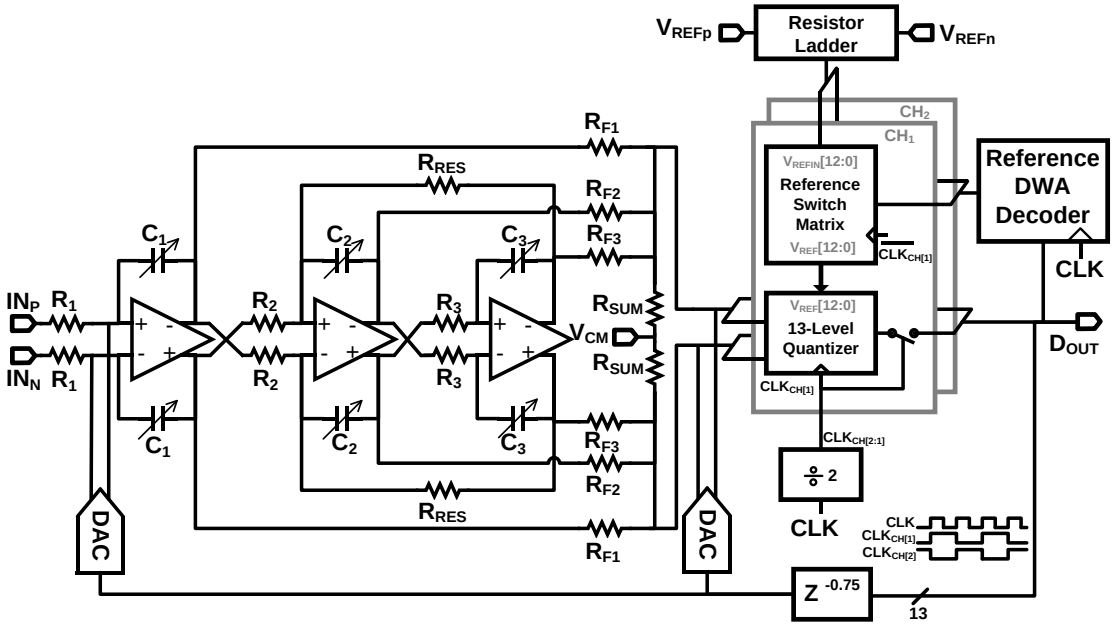

Fig. 43 Architecture of the third-order CTΣΔ modulator with the Time-Interleaved Reference DWA structure.

4.4.3. Comparators

Fig. 44 shows a schematic of the time interleaved comparator along with its timing sequence. The two interleaved comparators operate from inverted half rate (2.5GHz) clock signals ($CLK_{comp\_CH[1]}$ and $CLK_{comp\_CH[2]}$). When $CLK_{comp\_CH[1]}$ is low, the first channel (CH_1) is in the reset phase and its references are shuffled. On the other hand, during the same time the second channel (CH_2) is in the regeneration phase, and connected to the ΣΔ loop. After regeneration, the output of CH_2 is latched with the positive edge of the full rate CLK. Afterwards, the operation repeats, only this time CH_1 is connected to the ΣΔ loop while reference voltages of CH_2 are shuffled. The reference shuffling happens during the reset phase, because during that time the quantizer input is disconnected from the sigma-delta loop, and therefore, reference voltage changes cannot affect the quantizer decision.

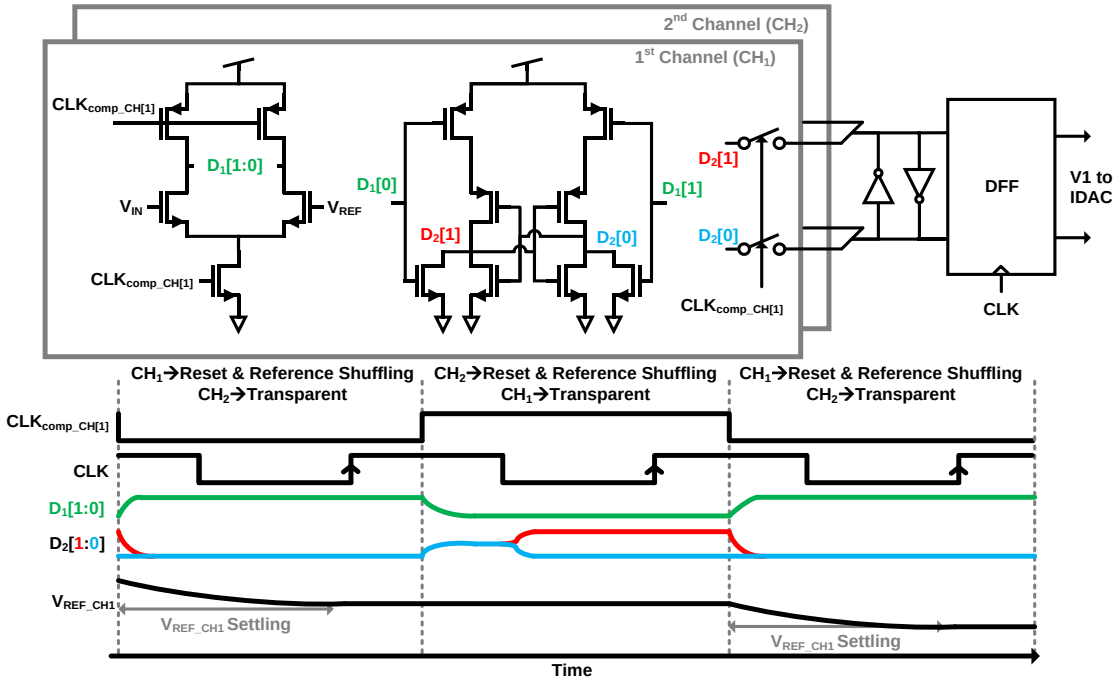

Fig. 44 Schematic of time-interleaved comparator and its timing diagram.

4.4.4. Op-Amp

CTΣΔ amplifiers must satisfy two gain requirements, while having enough phase margin (>60 Degrees), so that performance of the CTΣΔ modulator is not limited by the amplifier. There should be enough gain within the bandwidth of the modulator to ensure sufficient coefficient accuracy. A typical requirement is to have an amplifier gain of around 40-50dB loop gain within the bandwidth of the modulator. In addition, 10-20dB of gain at is required Fs/2 to process the feedback DAC current. However, it is difficult to use cascode structure to achieve both gain and bandwidth requirements of the amplifiers, while ensuring more than 60degres phase margin. A multi-stage amplifier is a good alternative for continuous-time modulators. In our ADC, we use a third order multistage multipath feed-forward topology where the first amplifier (Fig. 45) has three multi-stage paths (55dB gain), while the second and third amplifiers are formed only by two stages (35dB gain). The unity-gain-bandwidth of all the amplifiers is 12GHz to ensure at least 13dB gain at half of the sampling clock frequency (2.5GHz). With this architecture, we can achieve both the high gain and high bandwidth requirements while still satisfying 60-degree phase margin requirements.

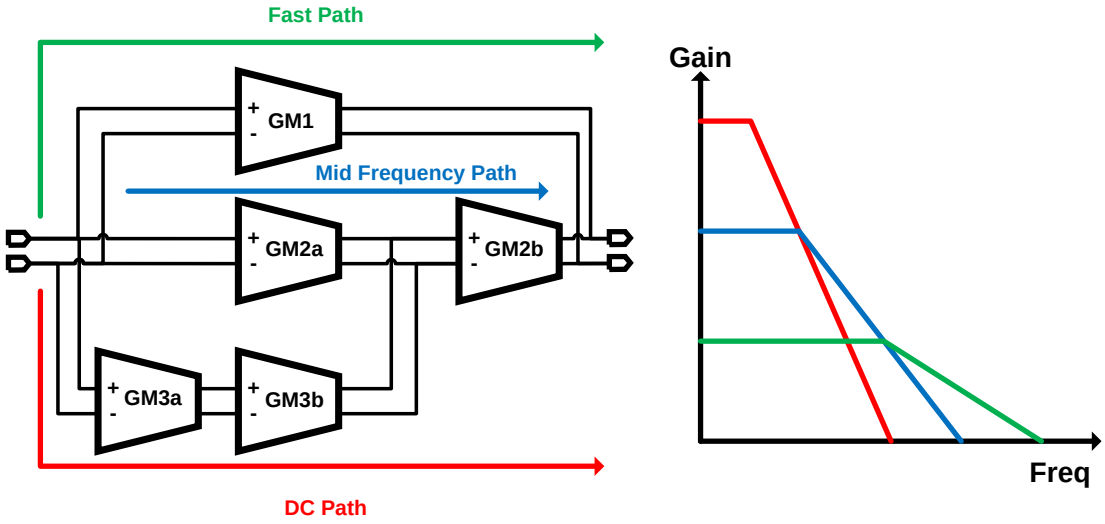

Fig. 45. Conceptual diagram of multipath multistage feed-forward amplifier.

Fig. 46 shows the schematic of the third order multipath multistage feedforward amplifier. In this architecture, the fast path consumes 40mW, while the middle stage consumes only 5mW. The input stage power consumption is determined by the noise requirements of the amplifier. The total power consumption of the first amplifier is 60mW, while the second and third amplifiers use 32mW each.

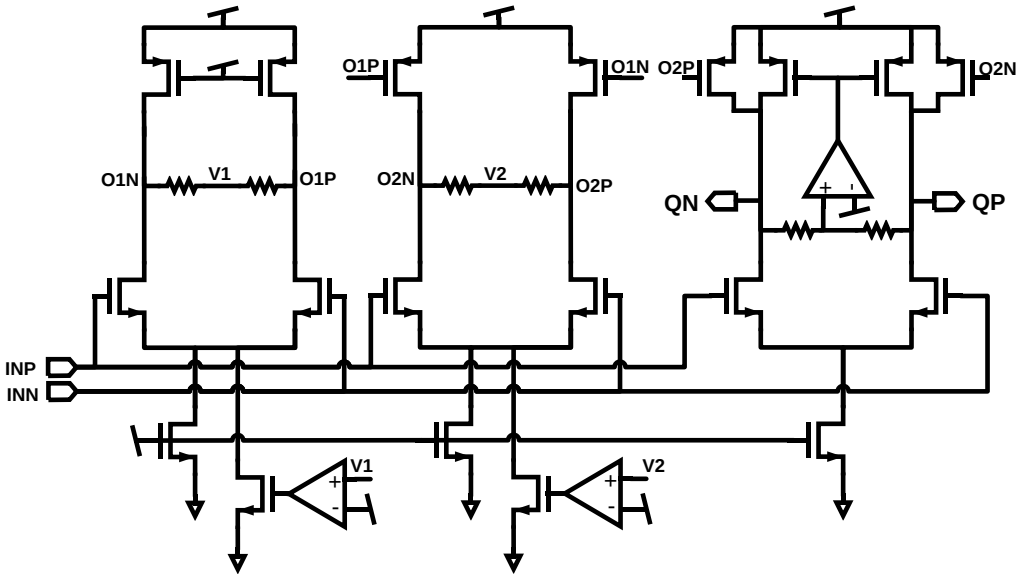

Fig. 46. Third order multipath multistage feed-forward op-amp.

4.4.5. Current Steering DAC Unit Element

The unit element of the multi-bit DACs is implemented as a fully complementary current-steering structure (Fig. 47), formed by a combination of thick oxide and thin oxide PMOS and NMOS devices. The output impedance of the DAC current sources is increased with cascode transistors. 1.95V and -0.55V supply voltages are used for the current sources. Thanks to the use of TI-RDWA, the biasing current and cascode transistors are sized for only 9-bit linearity. Thin oxide transistors and minimum size devices help satisfy the high speed switching requirements.

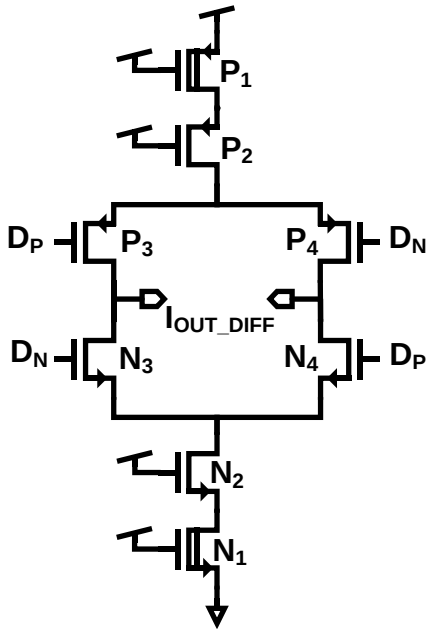

Fig. 47. Schematic of current steering DAC unit element.

4.5. Measurement Results

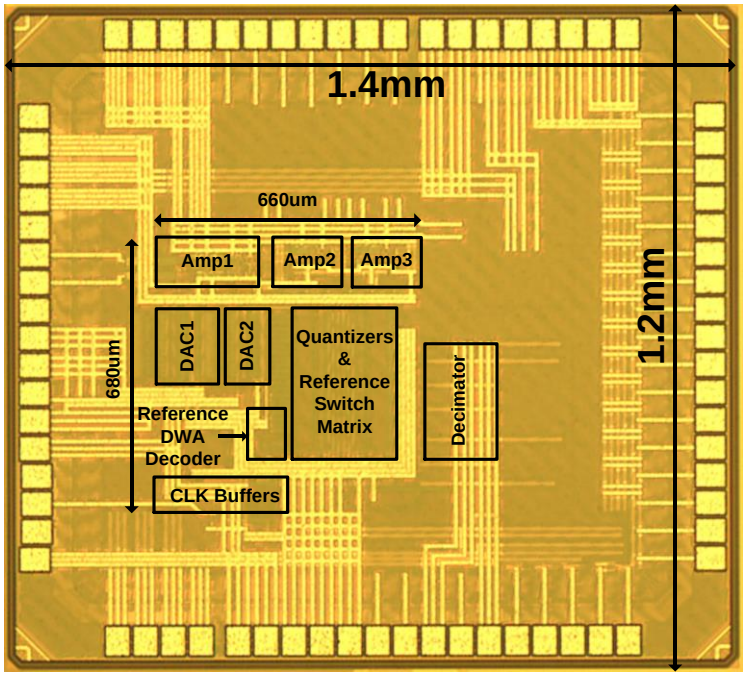

Fig. 48 Microphotograph of the third-order CTΣΔ modulator in 40nm CMOS.

The prototype 5GS/s modulator with TI-RDWA, is implemented in 40nm CMOS and occupies an active area of 0.45mm^2 (Fig. 48), excluding the active area of on-chip decimation filter. The prototype uses three positive supply voltages - the amplifiers run from 1.2V, all digital circuitry runs from 1.1V and the DACs have 1.95V and -0.55V supply voltages. The total measured power consumption is 233mW. Fig. 49 shows the measured power consumption distribution of the prototype modulator. The amplifiers consume the largest portion of the power (125mW), while the quantizers and reference decoder use 48mW and the clock buffers consume 18mW. The total DAC power consumption is 42mW. The decimator power is 30mW, and is not included in the total power consumption.

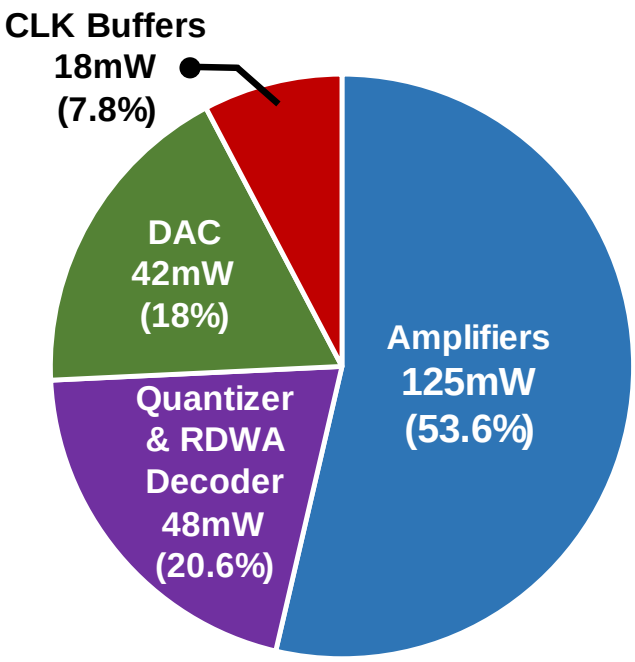

Fig. 49. Measured power consumption distribution of the prototype.

Fig. 50 shows the digital output power spectral density measurement results when DWA is both disabled (Fig. 50 (a)), and enabled (Fig. 50 (b)). When TI-RDWA is enabled, the measured SFDR improves by 17dB and the measured SNDR and SFDR for a 15MHz full-scale input signal are 66.1dB and 84dB, respectively, without requiring any DAC calibration.

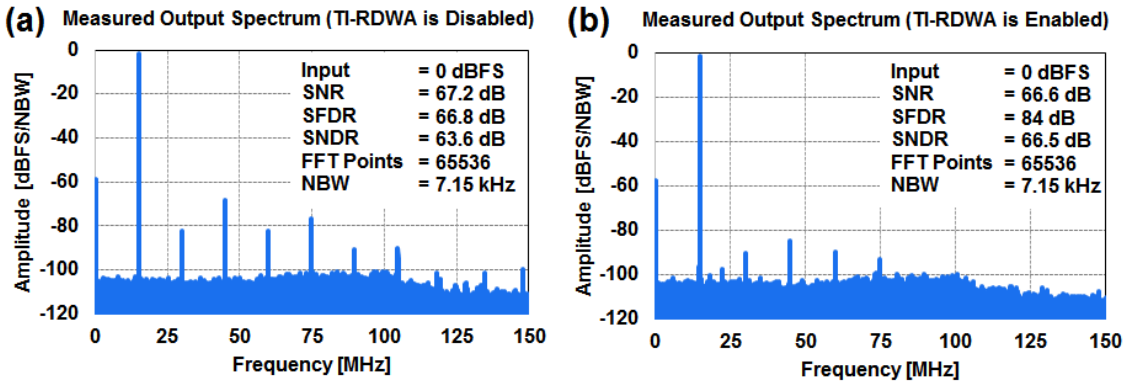

Fig. 50. Measured output spectrum of the CTΣΔ modulator with 0dBFS 15MHz input. (a) TI-RDWA is disabled. (b) TI-RDWA is enabled.

Fig. 51(a) shows the digital output power spectral density measurement results for a 100MHz full-scale input signal is applied to the input of the modulator. The measured SNDR for 100MHz input is 64dB when the TI-RDWA is enabled. Fig. 51(b) shows the measured SNDR and SNR of the modulator for 0dBFS input from 10MHz-to-100MHz when the TI-RDWA is enabled. The SNDR drops 2.4dB up to 100MHz input.

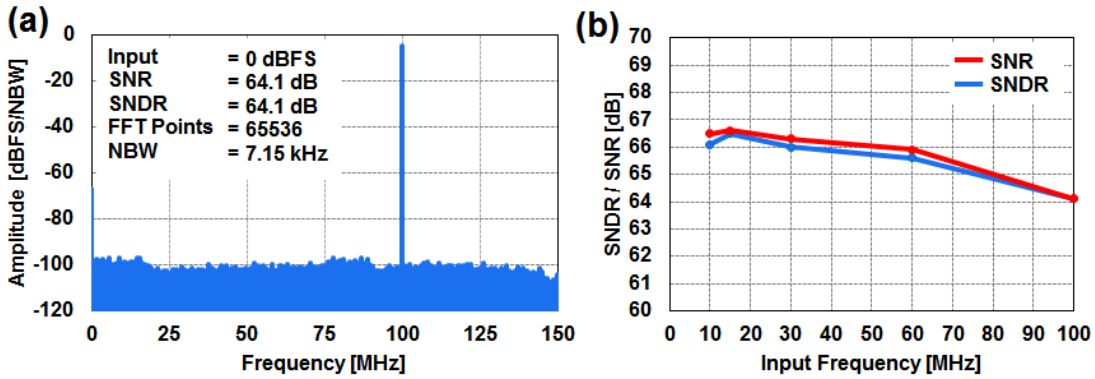

Fig. 51. (a) Measured output spectrum of the CTΣΔ modulator with 0dBFS 100MHz input (TI-RDWA is enabled). (b) Measured output SNDR and SNR of the modulator for 0dBFS input from 10MHz-to-100MHz (TI-RDWA is enabled)

The dynamic range of the prototype were measured by using a 15MHz input signal. As shown in Fig. 52, the ADC achieves a measured dynamic range (DR) of 70dB in a 156MHz bandwidth.

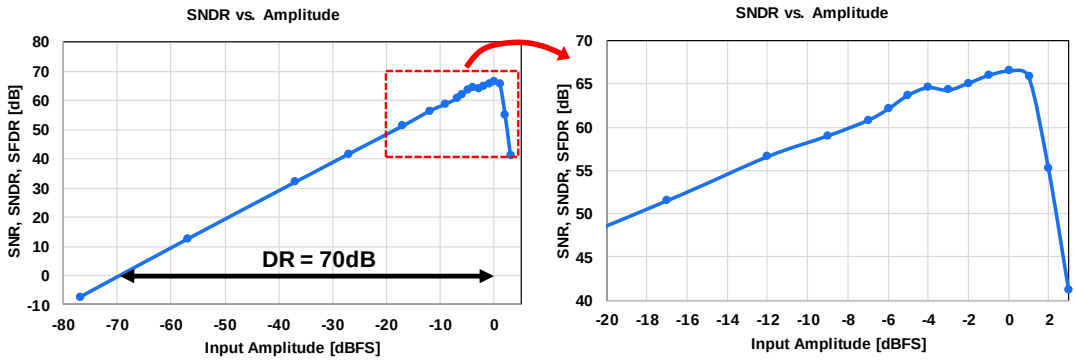

Fig. 52 Measured dynamic range of the modulator for 15MHz input when the TI-RDWA is enabled.

Table III summarizes the performance of the ADC and compares it with the state-of-the-art high-speed CTΣΔ modulators. The TI-RDWA architecture enables first-order DAC element shuffling in a 40nm CMOS CTΣΔ modulator at 5GHz, and the prototype achieves 70dB DR in a 156MHz bandwidth and a Schreier FoM of 158.3dB, without calibration.

Table III. Comparison with the state-of-the-art

Author	**This Work**	**Bolatkale**	**Shibata**	**Wu**	**Dong**
Publication		**JSSC 2011**	**JSSC 2012**	**ISSCC 2016**	**ISSCC 2016**
Architecture	CTΣΔ	CTΣΔ	CTΣΔ	CTΣΔ	CTΣΔ
Technology (nm)	40	45	65	16	28
Sampling Frequency (GHz)	5	4	4	2.88	8
Bandwidth (MHz)	156	125	150	160	465
Supply Voltage (V)	1.1/1.95/-0.55	1.1 / 1.8	1/±2.5	1.4/1.5/0.8	1/1.8/-1
Power (mW)	233	256	750	40	890
Area (mm^2)	0.45	0.9[a]	5.5[b]	0.155	1.4
DAC Error Control Technique	First-order Shaping	Sizing of the DACs	Sizing of the DACs	Sizing of the DACs	Calibration & Dithering
Dynamic Range (dB)	70	70	73	72.1	69.3
SNR (dB)	66.6	65.5	71	68.13	68
SFDR (dB)	83.3	78.2	78[c]	75	NA
SNDR (dB)	66.5	65	71	65.33	67
ENOB (bits)	10.75	10.50	11.50	10.56	10.84
FOM_S (dB)	158.3	156.9	156.0	168.1	156.5
FOM_W (fj/conversion-step)	432.4	704.7	862.2	82.8	523.1

[a] Including the decimation filter and clock buffers, [b] Including the bandpass CTΣΔ modulators
[c] For the RC low-pass modulator

4.6. Conclusion

This dissertation introduces a 5GS/s Continuous-Time (CT) ΣΔ ADC, based on a new Time-Interleaved Reference Data Weighted Averaging (TI-RDWA) architecture. The proposed TI-RDWA architecture eliminates the propagation delay of traditional DEM by shuffling quantizer reference voltages instead of shuffling the DAC elements. To achieve higher speed, we add time-interleaving to overcome the delay due to the reference voltage settling. This enables a CT ΣΔ modulator with the TI-RDWA architecture to operate at high sampling speed (5GS/s), while maintaining the advantages of first-order shaping of

DAC mismatch. This allows us to use 2x smaller DAC unit area for the same linearity and thereby reduces the parasitics and timing skew, which enables higher sampling speeds for the same power consumption.

Thanks to TI-RDWA, the prototype CTΣΔ modulator has a 5GS/s sampling frequency and a 1.25x wider signal bandwidth than state-of-the-art ΣΔ modulators with the same power consumption [24]. It dissipates one third of the power for the same bandwidth [39] without needing any feedback DAC calibration [41].

CHAPTER 5. Future Work

This research investigated the noise shaping benefits of CTΣΔ modulators and applied these benefits to the circuits for high speed wireless applications. In the first part of the dissertation, we introduce a new noise-shaping time-to-digital converter for high-frequency digital PLLs. Our particular application is a signal source for an FMCW radar. The following improvements can be considered for better system performance.

- The bandwidth of the TDC can be increased for wider PLL loop bandwidths to further improve the lock time of the PLL and increase linearity.
- A multi-bit quantizer with a second order modulator can be used to reduce total power of the TDC and to reduce the slope of the out-of-band noise shaping from 60dB/decade to 40dB/decade
- The oversampling ratio of the PLL and TDC can be decreased to reduce the total power consumption.

In the second part of this dissertation, we focus on the non-idealities in the high-speed CTΣΔ modulators and propose a new dynamic element matching techniques applicable to high sampling speeds. Some potential improvements include:

- To reduce clock jitter and increase SNR of the overall ADC, an on-chip 5GHz low phase noise PLL can be implemented.

- An offset calibration for the input DAC can be implemented to suppress the even harmonics at the output spectrum.

CHAPTER 6. Conclusion

CTΣΔ modulators cover the widest conversion region in the ADC resolution-versus-bandwidth plane and therefore they are very efficient for both high resolution and high speed applications. This dissertation focuses on two different application areas where CTΣΔ modulators can be very useful and improve the performance of the overall system.

The first part of this dissertation focuses on the high-resolution characteristics of CTΣΔ modulators. The key contribution is a new third-order noise shaping time-to-digital converter (TDC) based on a CTΣΔ modulator for high-frequency digital phase lock loops. A CTΣΔ modulator in the TDC shapes the quantization noise and reduce the integrated rms noise of the TDC within the PLL bandwidth. For the prototype TDC measured integrated rms noise within 1MHz bandwidth is 176fs. Because of the low integrated rms noise, the in-band phase noise of high-frequency digital PLLs is decreased without affecting the PLL loop bandwidth. Therefore, it becomes possible to benefit from the advantages of digital techniques in the PLL while still satisfying the low phase noise and fast settling time requirements.

To prove the effectiveness of the TDC to PLL in-band phase noise, 30GHz and a 40GHz prototype fractional-N digital phase lock loop are fabricated. The 30GHz PLL achieves a measured phase noise of -87dBc/Hz at 100kHz offset which corresponds -212.6dBc/Hz^2 normalized in-band phase noise and 545fs jitter. Thanks to the noise shaping TDC, the

normalized phase noise of the PLL is 5dB better than any published digital integer or digital fractional-N high frequency (>20GHz) PLL.

The second part of this dissertation focuses on the non-idealities of high-speed CTΣΔ modulators for wireless communications. A new time-interleaved reference data weighted averaging architecture is suitable for GS/s CTΣΔ modulators. The proposed TI-RDWA shapes the DAC static mismatch effects and therefore enables the use of smaller DAC unit elements. This allows a 2x reduction in DAC unit area for the same linearity and thereby reduces the parasitics and timing skew, which enables higher sampling speeds for the same power consumption [24].

The proposed TI-RDWA architecture is used in a 5GS/s CTΣΔ modulator and the prototype achieves 156MHz bandwidth, 70dB dynamic range, 66.1dB SNDR and 84dB SFDR from a 15MHz full-scale input signal while consuming one third of the power for the same bandwidth [39].

BIBLIOGRAPHY

[1] [Online]. Available: https://www.gsmaintelligence.com/.

[2] M. Vahidpour, "A Millimeter-Wave Radar Microfabrication Techniques and Its Application in Detection of Concealed Objects,"PhD. dissertation, Dept. Electrical Eng., Univ. Michigan, Ann Arbor, 2012.

[3] B. P. Ginsburg, S. M. Ramaswamy, V. Rentala, E. Seok, S. Sankaran and H. Baher, "A 160GHz Pulsed Radar Tranceiver in 65nm CMOS," *JSSC*, vol. 49, no. 4, pp. 984-995, 2014.

[4] A. Arbabian, S. Callender, S. Kang, M. Rangwala and A. M. Niknejad, "A 94-GHz mm-Wave-to-Baseband Pulsed-Radar Tranceiver with Applications in Imaging and Gesture Recognition," *JSSC*, vol. 48, no. 4, pp. 1055-1071, April 2013.

[5] V. Jain, S. Sundararaman and P. Heydari, "A 22-29-GHz UWB Pulse-Radar Receiver Front-End in 0.18um CMOS," *Transaction on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 1903-1914, August 2009.

[6] J. Lee, Y.-A. Li, M.-H. Hung and S.-J. Huang, "A Fully-Integrated 77-GHz FMCW Radar Tranceiver in 65-nm CMOS Technology," *JSSC*, vol. 45, no. 12, pp. 2746-2756, December 2010.

[7] W. Wu, R. B. Staszewski and J. R. Long, "A 56.4-to-63.4 GHz Multi-Rate All-Digital Fractional-N PLL for FMCW Radar Applications in 65nm CMOS," *JSSC*, vol. 49, no. 5, pp. 1081-1096, May 2014.

[8] K. Pourvoyeur, R. Feger, S. Schuster, A. Stelzer and L. Maurer, "Ramp Sequence Analysis to Resolve Multi Target Scenarios for a 77-GHz FMCW Radar Sensor," in *11th International Conference on Information Fusion*, 2008.

[9] P. D. L. Beasley, "The Influence of Transmitter Phase Noise on FMCW Radar Performance," in *European Microwave Conference*, 2006.

[10] S. O. Piper, "FMCW Linearizer Bandwidth Requirements," in *Proceedings of the 1991 IEE National Radar Conference*, 1991.

[11] K. S. Kulpa, "Novel Method of Decreasing Influence of Phase Noise on FMCW Radar," in *CIE International Conference on Radar*, 2001.

[12] D. B. Leeson and G. F. Johnson, "Short-Term Stability for a Doppler Radar:Requirements, MEasurements, and Techniques," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 244-248, 1966.

[13] V. Szortyka, Q. Shi, K. Raczkowski, B. Parvais, M. Kuijk and P. Wambacq, "A 42mW 230fs-Jitter Sub-sampling 60GHz PLL in 40nm CMOS," in *ISSCC*, 2014.

[14] X. Yi, C. C. Boon, H. Liu, J. F. Lin, J. C. Ong and W. M. Lim, "A 57.9-to-68.3GHz 24.6mW Frequency Synthesizer with In-Phase Injection-Coupled QVCO in 65nm CMOS," in *ISSCC*, 2013.

[15] H. Yeo, S. Ryu, Y. Lee, S. Son and J. Kim, "A 940MHz Banwidth 28.8us-Period 8.9GHz Chirp Frequecy Synthesizer PLL in 65nm CMOS for -X-Band FMCW Radar Applications," in *ISSCC*, 2016.

[16] S. Jang, S. Kim, S.-H. Chu, G.-S. Jeong, Y. Kim and D.-K. Jeong, "An All-Digital Bang-Bang PLL Using Two-Point Modulation Background Gain Calibration for Spread Spectrum Clock Generation," in *Symposium on VLSI Circuits*, 2015.

[17] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg and P. T. Balsara, "Time-to-Digital Converter for RF Frequency Synthesis in 90nm CMOS," in *RFIC Symposium*, 2005.

[18] A. Elshazly, S. Rao, B. Young and P. K. Hanumolu, "A Noise-Shaping Time-to-Digital Converter Using Switched-Ring Oscillators-Analysis, Design, and Measurement Techniques," *JSSC*, vol. 49, no. 5, pp. 1184-1197, May 2014.

[19] W. Wu, X. Bai, R. B. Staszewski and J. R. Long, "A 56.4-to-63.4GHz Spurious-Free All-Digital Fractional-N PLL in 65nm CMOS," in *ISSCC*, 2013.

[20] M. Ferriss, A. Rylyakov, H. Ainspan, J. Tierno and D. Friedman, "A 28GHz Hybrid PLL in 32nm SOI CMOS," in *Symposium on VLSI Circuits*, 2013.

[21] [Online]. Available: http://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/mobile-white-paper-c11-520862.html.

[22] [Online]. Available: https://standards.ieee.org/about/get/802/802.11.html.

[23] A. Baschirotto, P. Harpe and K. A. Makinwa, Wideband Continuous-time SD ADCs,Automotive Electronics, and Power Management, Switzerland: Springer International Publishing, 2016.

[24] M. Bolatkale, J. Breems, R. Rutten and K. A. A. Makinwa, "A 4GHz Continuous-Time ΔΣ ADC with 70dB DR and -74dBFS THD in 125MHz BW,," *JSSC,VOL. 46, No. 12,* pp. 2857-2868, 2012.

[25] J. M. de la Rosa, R. Schreier, K. Pun and S. Pavan, "Next-Generation Delta-Sigma Converters:Trends and Perspectives," *JSSC,* vol. 5, no. 4, pp. 484-499, 2015.

[26] R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters, New Jersey: John Wiley & Sons, 2004.

[27] F. Gerfers and M. Ortmanns, Continuous-Time Sigma-Delta A/D Conversion, Springer-Verlag Berlin Heidelberg, 2006.

[28] B. Boser and B. Wooley, "The Design of Sigma Delta Modulation Analog-to-Digital Converters," *JSSC,* vol. 23, no. 6, pp. 1298-1308, 1988.

[29] R. Schreier and B. Zhang, "Delta-Sigma Modulators Employing Continuous-Time Circuitry," *IEEE Transactions on Circuits and Systems,* vol. 43, no. 4, pp. 324-332, 1996.

[30] J. Jeong, N. Collins and M. P. Flynn, "A 260 Mhz IF Sampling Bit-Stream Processing Digital Beamformer With an Integrated Array of Continuous-Time Band-Pass Delta Sigma Modulators," *JSSC,* vol. 51, no. 5, pp. 1168-1176, 2016.

[31] H. Chae and M. P. Flynn, "A 69dB SNDR, 25 MHz BW, 800 MS/s Continuous-Time Bandpass Delta Sigma Modulator Using a Duty-Cycle-Controlled DAC for Low Power and Reconfigurability," *JSSC,* vol. 51, no. 3, pp. 649-659, 2016.

[32] S. Ho, C. Lo, J. Ru and J. Zhao, "A 23mW, 73dB Dynamic Range, 80MHz BW Continuous Time Delta Sigma Modulator in 20nm CMOS," *JSSC,* vol. 50, no. 4, pp. 908-919, 2015.

[33] D. Yoon, S. Ho and H. Lee, "A Continuous-Time Sturdy-MASH Delta Sigma Modulator in 28nm CMOS," *JSSC,* vol. 50, no. 12, pp. 2880-2890, 2015.

[34] C. Ho, C. Liu, C. Lo, H. Tsai, T. Wang and Y. Lin, "A 4.5mW CT Self-Coupled Delta Sigma Modulator With 2.2MHz BW and 90.4 dB SNDR Using Residual ELD Compensation," *JSSC,* vol. 50, no. 12, pp. 2870-2879, 2015.

[35] Y. Dong, W. Yang, R. Schreier, A. Sheikholeslami and S. Korrapati, "A Continuous Time 0-3 MASH ADC Achieving 88dB DR With 53MHz BW in 28nm CMOS," *JSSC,* vol. 49, no. 12, pp. 2868-2877, 2014.

[36] J. Kauffman, P. Witte, M. Lehmann, J. Becker, Y. Manoli and M. Ortmanns, "A 72 dB DR, CT Delta Sigma Modulator Using Digitally Estimated, Auxilary DAC Linearization Achieving 88fJ/conv-step in a 25MHz BW," *JSSC,* vol. 49, no. 2, pp. 392-404, 2014.

[37] A. Sukumaran and S. Pavan, "Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback," *JSSC,* vol. 49, no. 11, pp. 2515-2525, 2014.

[38] H. Chae, J. Jeong, G. Manganaro and M. P. Flynn, "A 12mW Low Power Continuous-Time Bandpass Delta Sigma Modulator With 58dB SNDR and 24MHz Bandwidth at 200MHz IF," *JSSC,* vol. 49, no. 2, pp. 405-415, 2014.

[39] H. Shibata, R. Schreier, W. Yang, A. Shaikh, D. Paterson, T. Cadwell, D. Allred and P. W. Lai, "A DC-to-1 GHz tunable RF ΔΣ ADC achieving DR= 74dB and BW= 150MHz at f0= 450MHz using 550mW," *JSSC, VOL. 47, No. 12,* pp. 2888-2897, 2012.

[40] S. Wu, T. Kao, Z. Lee, P. Chen and J. Tsai, "A 160MHz-DW 72 dB-DR 40mW continuous-time ΔΣ Modulator in 16nm CMOS with analog ISI-reduction technique," in *ISSCC*, 2016.

[41] Y. Dong, J. Zhao, W. Yang, T. Cadwell, H. Shibata, R. Schreier, Q. Meng, J. Silva, D. Paterson and J. Gealow, "A930mW 69dB-DR 465MHz-BW CT 1-2 MASH ADC in 28nm CMOS," in *ISSCC*, 2016.

[42] H. Shibata, V. Kozlov, Z. Ji, A. Ganesan, H. Zhu and D. Paterson, "A 9GS/s 1GHz-BW Oversampled Continuous-Time Pipeline ADC Achieving -161dBFS/Hz NSD," in *ISSC*, 2017.

[43] [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

[44] F. M. Gardner, Phase-Lock Techniques, New York: Wiley, 1966.

[45] M. Ferriss, B. Sadhu, A. Rylyakov, H. Ainspan and D. Friedman, "A 13.1-to-28GHz Fractional-N PLL in 32nm SOI CMOS with DS Noise-Cancellation Scheme," in *ISSCC*, 2015.

[46] A. Hussein, S. Vasadi, M. Soliman and J. Paramesh, "A 50-to-66GHz 65nm CMOS All-Digital Fractional-N PLL with 220fsrms Jitter," in *ISSCC*, 2017.

[47] P. Dudek, S. Szczepanski and J. V. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," *IEEE Transactions on Solid State Circuits*, vol. 35, no. 2, pp. 240-247, Feb 2000.

[48] M. Lee and A. A. Abidi, "A 9b 1.25ps Resolution Coarse-Fine Tie-to-Digital Converter in 90nm CMOS that Amplifies a Time Residue," *JSSC*, vol. 43, no. 4, pp. 769-777, April 2008.

[49] K. Kim, W. Yu and S. Cho, "A 9bit, 1.12ps Resolution 2.5b/Stage Pipelined Time-to-Digital Converter in 65nm CMOS Using Time-Register," *JSSC*, vol. 49, no. 4, pp. 1007-1016, April 2014.

[50] M. Z. Straayer and M. H. Perrott, "A Multi-Path Gated Ring Oscillator TDC with First-Order Noise Shaping," *JSSC*, vol. 44, no. 4, pp. 1089-1098, April 2009.

[51] Y. Cao, W. De Cock, M. Steyaert and P. Leroux, "1-1-1 MASH DS Time-to-Digital Converters With 6ps Resolution and Third-Order Noise Shaping," *JSSC*, vol. 47, no. 9, pp. 2093-2106, September 2012.

[52] M. B. Dayanik, N. Collins and M. P. Flynn, "A 28.5-33.5GHz Fractional-N PLL Using a 3rd Order Noise Shaping Time-to-Digital Converter with 176fs Resolution," in *ESSCIRC*, 2015.

[53] Y. Wu, P. Lu and R. B. Staszewski, "A 103fsrms 1.32mW 50MS/s 1.25MHz Bandwidth Two-Step Flash-DS Time-to-Digital Converter for ADPLL," in *RFIC*, 2015.

[54] B. Sadhu, M. A. Ferriss, J.-O. Plouchart, A. S. Natarajan, A. V. Rylyakov, A. Valdes-Garcia, B. D. Parker, S. Reynolds, A. Babakhani, S. Yaldiz, L. Pileggi, R. Harjani, J. Tierno and D. Friedman, "A 21.8-27.5GHz PLL in 32nm SOI Using Gm Linearization to Achieve -130dBc/Hz Phase Noise at 10MHz Offset from 22GHz Carrier," in *RFIC*, 2012.

[55] W. Yang, W. Schofield, H. Shibata, S. Korrapati, A. Shaikh, N. Abaskharoun and D. Ribner, "A 100mW 10MHz-BW CTΔΣ Modulator with 87dB DR and 91dBc IMD," in *ISSCC*, 2008.

[56] Y. Dong, W. Yang, R. Schreier, A. Sheikholeslami and S. Korrapati, "A Continuous-Time 0-3 MASH ADC Achieving 88dB DR With 53MHz BW in 28nm CMOS," *JSSC*, vol. 49, no. 12, pp. 2868-2877, 2014.