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Model predictive current control based on a generalised adjacent voltage vectors approach for multilevel inverters

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Paul Gistain Ipoum-Ngome[1], Daniel Legrand Mon-Nzongo[1,2], Rodolfo C.C. Flesch[3], Joseph Song-Manguelle[4], Mengqi Wang[5], Tao Jin[1] ✉

[1]*Electrical Engineering and Automation, Fuzhou University, 350116 Fuzhou, People's Republic of China*
[2]*Pearl Electric, Co. Ltd., Guangzhou 511400, Guangdong Province, People's Republic of China*
[3]*Department of Automation and Systems, Federal University of Santa Catarina, 88040-900 Florianópolis, SC, Brazil*
[4]*Université du Québec a Trois Rivières, 14847 Trois-Rivières, Québec, Canada*
[5]*Department of Electrical and Computer Engineering, University of Michigan-Dearborn, MI 48128, USA*
✉ *E-mail: jintly@fzu.edu.cn*

Abstract: Model predictive current control (MPCC) uses the discrete-time model of a system to predict the future behaviour of the current for all voltage vectors (VVs) generated by a power converter. In multilevel inverters, the large number of VVs imposes a long computation time for the prediction and selection of the optimal state to be applied to the converter, which increases the sampling time and decreases the closed-loop performance. An MPCC is proposed based on the idea of generalised adjacent voltage vectors (GAVVs) for multilevel cascaded H-bridge inverters with a DC-link voltage fed by photovoltaic (PV) cells. This method deals with the voltage drop and often small inter-bridge voltage imbalance and irradiance issues that occur in PV power plants. The proposed GAVV method is analytically formulated to provide three types of subsets for a given number of inverter levels. The use of the newly added subsets of four and five VVs contributes to boosting the converter output voltage and achieving acceptably balanced current and line-to-line voltage under low irradiance compared with the classical approach. Simulation and experimental results show good current response and reduced switching frequency even under a high current reference with DC-link voltage drop.

1 Introduction

Multilevel cascaded H-bridge (ML-CHB) inverters are widely used in high- and medium-power drive systems. In industry, they are a natural choice for supplying variable frequency medium-voltage power to electric motors used to drive large industrial loads, such as pumps and gas compressor trains. They are also used in renewable energy technologies [1]. Compared to other topologies, ML-CHB inverters are mainly used because they are modular and use low-voltage power devices, meaning they can generate a medium-voltage output with reduced voltage stress across power semiconductors. The large number of output voltage steps also ensures low-harmonic pollution, with an apparent switching frequency that is substantially high, leading to a reduced output filter size or even its complete avoidance [2, 3]. This multilevel topology is based on the series connection of single-phase three-level H-bridge cells. When it operates as an inverter, the cells require separated and insulated DC voltages, which can be provided by the association of AC/DC converters supplied by a multi-secondary low-frequency power transformer or a photovoltaic (PV) power plant. In a multilevel scenario, as the number of output voltage steps increases, the number of redundant switching states also increases, leading to an increased combination of voltage vectors (VVs) from which a given output voltage step can be generated. Unfortunately, the increase in the number of degrees of freedom in the inverter is also associated with an increase in the complexity of its control scheme [3, 4].

The classical scheme to control ML-CHB inverters and avoid the complexity related to the increased number of levels is to use linear controllers, often in association with a pulse width modulator (PWM) scheme. Usually, the current controller is the inner-loop and generates reference voltages relative to the modulator. These voltages are compared with a set of carrier signals adapted from a two-level inverter to generate the pulse signals for ML-CHB inverters. In industry, space vector modulation (SVM), which is the equivalent of PWM with a third harmonic injection, is often preferred since it is suitable for digital implementation and provides a wider linear modulation range with lower baseband harmonics [5]. Controllers based on PWM or SVM have been intensively investigated over the last decade, with consideration for numerous design objectives, such as low-voltage and current output harmonics, small torque and current ripples, switching loss minimisation and system reliability to generate fault-tolerant solutions [6, 7].

Model predictive current control (MPCC) is another control approach that has gained importance in recent years for the control of inverters, mainly because it can handle all of the aforementioned objectives without a modulation stage and can achieve fast dynamic response [8]. There are several MPCC formulations in the literature, but for their specific application in switched converters the finite control set MPCC is the most used [9–15]. This controller uses the discrete nature of the converter to predict the current behaviour of the system for all possible VVs and then select the best one [10]. However, by increasing the number of levels, as in an ML-CHB inverter, the number of candidate VVs also increases, leading to a higher computation time to predict system behaviour and find the best VV through an optimisation process [11–15]. The high number of states has the potential to increase the converter switching frequency due to the higher number of degrees of freedom given to the MPCC to find the best state. There are also some impacts on the common mode voltage (CMV) because redundant VVs with higher CMV can be selected as optimal VVs, and several phases of the inverter can simultaneously change their levels, which may lead to high CMV spikes at some sample points.

Different approaches have been developed to mitigate the negative effects observed when MPCC is used to control multilevel inverters. The simplest one is based on the reduction of the candidate VVs at a sampling instant and it can be divided into two types [11, 12]. The first one, known as MPCC-7adj, is a predictive controller that uses the seven adjacent VVs with smaller CMV and distance to the previous optimal vector as VV candidates [11]. The

second one uses the principle of SVM to reduce the amount of VVs considered as candidate solutions [12], such that only the three VVs that are closest to the VV reference are potential solutions. The latter type is known as MPCC-3VVs and its main drawback is that the VV reference is based on the measured and predicted currents and system parameters, which might fluctuate. Despite a long transient time compared with that of MPCC-3VVs, MPCC-7adj has a shorter computation time and is less sensitive to parameter changes. Other advanced algorithms based on multi-step model predictive control are also reported in the literature [13–15], but they have a considerably higher complexity, which can represent a barrier for their use in embedded systems to drive plants with fast dynamics [15].

An accurate analysis of the space vector of a multilevel inverter and the corresponding positions of each VV on the $\alpha\beta$-axis reveals the existence of two other subsets whose VVs are located in the last two outer hexagons of the space vector. This means all the VVs that belong to these new subsets have high voltage amplitudes compared with the subset with seven VVs, thus offering the ability to boost the output voltage. This paper proposes a generalised adjacent voltage vectors (GAVVs) approach which can be used to predict the seven, five or four adjacent VVs to be used by MPCC in ML-CHB inverters. At nominal DC-link voltage, the proposed approach will behave like MPCC-7adj most of the time, since VVs with high amplitude are not expected to be used under nominal conditions. However, under limited DC link the extended subsets can be exploited to supply VVs with larger amplitudes. Thus, compared to existing approaches, the proposed one is expected to provide better performances under DC-link voltage drop in the CHB modules, since the MPCC will consider more VVs with larger amplitude as candidate solutions, which helps to compensate for the voltage drop.

This paper is organised as follows. Section 2 presents MPCC-7adj with ML-CHBs associated with an RLE load. Section 3 describes the MPCC based on the proposed generalised adjacent VVs scheme. Simulation results are shown in Section 4. Section 5 describes the experimental set-up used and presents the experimental results achieved with the proposed controller. Finally, conclusions are formulated in Section 6.

2 MPCC for ML-CHB-based adjacent VVs

2.1 ML-CHB inverters

The power unit shown in Fig. 1 is an ML-CHB inverter connected to a three-phase load. An ML-CHB requires C cells connected in series per phase (see Table 1), and each phase has n top switches, equal to twice the number of modules in series per phase. To generate L voltage levels, each phase has m_s combinations of top switches, as shown in Table 1, and a given combination produces an output voltage

$$V_{xn} = \sum_{j=1}^{C} (T_{2j-1} - T_{2j}) V_{\mathrm{dc},j} \Big|_x \text{ and } S_x = \sum_{j=1}^{C} (T_{2j-1} - T_{2j}) \tag{1}$$

with $S_x \in \{-C, -C+1, \ldots, 0, \ldots, C-1, C\}$ as the inverter modulated signal, $V_{\mathrm{dc},j}$ as the DC-link voltage per CHB, $T \in \{0, 1\}$ as the state of the top switches per CHB and $x \in \{a, b, c\}$. The number of commutations between two consecutive sampling instants is given by

$$N = N_{swa} + N_{swb} + N_{swc} \text{and} N_{swx} = \sum_{j=1}^{C} \left| T_j(k) - T_j(k-1) \right| \Big|_x \tag{2}$$

where N_{swx} is the number of commutations observed in phase x and $T_j(k)$ is the switching state at the kth sample. It is important to limit this term to reduce losses in high-power applications with medium-voltage converters.

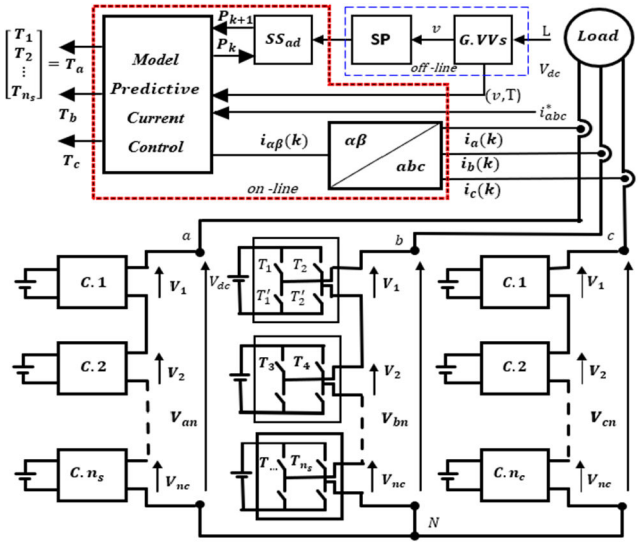

Fig. 1 *Proposed MPCC based extended adjacent VVs approach*

Table 1 Parameters for ML-CHB inverters

L-CHB inverter		3-CHB	5-CHB	7-CHB	9-CHB
number of levels (L)	L	3	5	7	9
number of cells by phase (C)	$(L-1)/2$	1	2	3	4
number of switches by phase (n)	$2C$	2	4	6	8
number of combinations of switches by phase (m_s)	$2n$	4	16	64	256
number of state vectors (m_{V0})	L^3	27	125	343	512
number of state vectors without redundances (m_V)	$12C^2 + 6C + 1$	19	61	127	217
number of seven adjacent vector groups (G_7)	$12C^2 - 6C + 1$	7	37	91	169
number of five adjacent vector groups (G_5)	$12C - 6$	6	18	30	42
number of four adjacent vector groups (G_4)	6	6	6	6	6

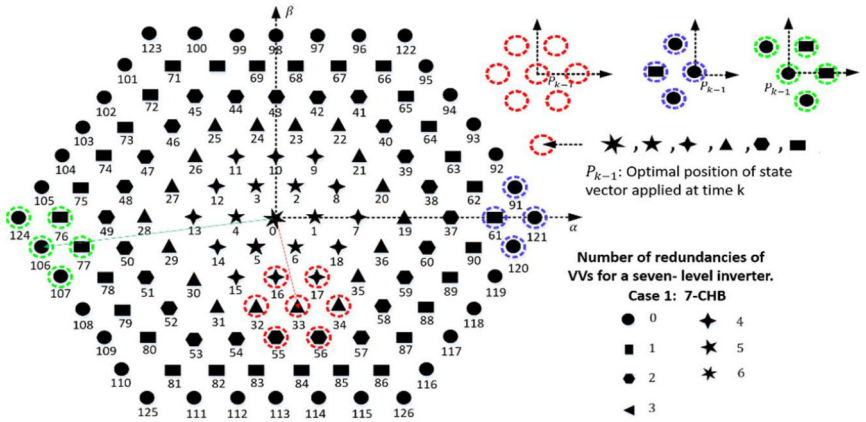

Fig. 2 *Space and sub-spaces (subsets) VVs in an orthogonal stationary reference frame for a seven-level inverter*

2.2 Model of the RLE load

The differential continuous-time model of a three-phase RLE load, given in (3), is expressed in $\alpha\beta$ reference frames after a Park transformation as in (4). After having discretised (4) based on Euler approximation, the predicted current is obtained through (5)

$$L\frac{\mathrm{d}(i_{abc})}{\mathrm{d}t} = v_{abc} - Ri_{abc} - e_{abc} \tag{3}$$

$$L\frac{\mathrm{d}(i_{\alpha\beta})}{\mathrm{d}t} = v_{\alpha\beta} - Ri_{\alpha\beta} - e_{\alpha\beta} \tag{4}$$

$$i^P(k+1) = \frac{T_s}{L}(v(k) - e(k)) + \left(1 - \frac{RT_s}{L}\right)i(k), \tag{5}$$

where i_{abc} represents each of the measured three phase currents, e_{abc} is often the back electromotive force (e.m.f.) of the motor or the grid voltage and v_{abc} is the output voltage of the inverter for each of the three phases. $v(k)$, $i(k)$ and $e(k)$ are, respectively, the output voltage, load current and back-e.m.f. in the alpha-beta frames at time instant k; $i^P(k+1)$ is the current prediction for time instant $k+1$ evaluated at k.

The back-e.m.f. at k is usually not measured, so it is assumed to be equal to the value at $k-1$, i.e. $e(k) \cong e(k-1)$, which produces a negligible error if the sampling frequency is large enough. By making this approximation, it is possible to write the back-e.m.f. as a function of known parameters, as in (6). Based on this approximation the discrete-time model of the system for the prediction of all the currents with time delay compensation [16] is given in (7).

$$e(k-1) = \frac{T_s}{L}(i(k) - i(k-1)) + Ri(k-1) + v(k-1) \tag{6}$$

$$i^p(k+2) = \frac{T_s}{L}(v(k+1) - e(k)) + \left(1 - \frac{RT_s}{L}\right)i^p(k+1) \tag{7}$$

2.3 Optimisation

The cost function defined in (8) considers the current error between each predicted current $i^P(k+2|k)$ generated by each VV and the current reference given by (9), where the asterisk is used to refer to reference values. In a regular finite control set MPCC implementation, the m_{V0} possible combinations of VVs for the ML-CHB inverter (as shown in Table 1) are evaluated in the prediction model of (7) and the one which results in the minimum value for the cost function in (8) is selected and used. However, the value of m_{V0} grows rapidly with an increase in the number of levels. Since (7) and (8) need to be executed m_{V0} times, for multilevel converters, the sampling time needs to be high enough to allow all the necessary computation. The solutions of increasing the sampling time and using a control board with a higher frequency execution decrease the control performance and increase the control board cost, respectively. To allow better trade-offs between performance and cost, an alternative method is to reduce the number of VVs to be computed at each sample. The most widely known approach to achieve this goal is known as adjacent VVs, which reduces the number of VVs evaluated at each sample from m_{V0} to 7 by considering just one subset among the G_7 possibilities [11].

$$g = \left|i^*(k+2) - i^P(k+2)\right| \tag{8}$$

$$i^*(k+2) = 6i^*(k) - 8i^*(k-1) + 3i^*(k-2) \tag{9}$$

2.4 MPC using seven adjacent vectors (MPCC-7adj)

The principle of MPC-7adj is founded on the assumption that during normal operation, the VV applied at a given time instant is very similar to the one applied at the previous one [11]. To achieve this assumption, first, redundant VVs are avoided by looking only for the state voltage that minimises the CMV (V_{N0}, as defined in (10)) among VVs with the same amplitude. Consequently, all the existing redundant states used to generate the same VV with a CMV higher than the minimal one are ignored. Therefore, all the remaining ones are non-redundant. In addition, for each VV it is necessary to search for those that minimise the Euclidean distance from its position to the remaining. The adoption of both constraints leads to a number of G_7 subsets with seven VVs each.

$$V_{No} = \frac{1}{3}(V_{aN} + V_{bN} + V_{cN}) \tag{10}$$

Among the seven VVs, one of them is placed equidistant from the remaining in the subset and this VV is considered as the previous optimal VV by MPCC to search for the next subset of VVs to compute among the G_7 possibilities [11].

MPCC-7adj is restricted to using only one subset having seven adjacent VVs at each sample (Fig. 2, in red). For example, in a seven-level inverter there are 91 subsets, and each subset has one VV that is equidistant to the other six. All these equidistant VVs are disposed of in all hexagons, except the outer one. Therefore, the positions of these VVs go from 0 to 90, as shown in Fig. 2. For example, if the previous VV at the $(k-1)$th sample is located at position value 33, as indicated in Fig. 2, the subset that will be used at sample k contains the VVs with the positions 16, 17, 32, 33, 34, 55 and 56. The main drawback of this approach is that it does not use the outer hexagon to predict the next subset. Thus, if the optimal VV is located in the outer hexagon, the number of candidate VVs that are also located in this hexagon is limited by the method, as discussed below.

If a case in which MPCC working with a reduced DC-link voltage under a high current reference is considered, the controller needs to take into account the VVs in the outer hexagon and around it as much as possible, since they contain the highest amplitudes. However, this does not happen when MPC-7adj is

considered. Imagine that the optimal VV is 106 as in Fig. 2, such that the equidistant VV to define the subset will be either 76 or 77. In the first case, VV number 107 will not be considered as a candidate solution in the next iteration, even though it is just beside VV number 106. In the second case, the same will happen with VV number 124. This limitation excludes from the solution subsets of VVs that are natural candidates for the next iteration, which means that the principle of adjacent VVs is not upheld when it comes to an optimal VV located in the outer hexagon, since if the actual optimal VV is 106 the next subset should contain at least the VVs located at 76, 77, 106, 107 and 124. Therefore, to ensure better behaviour of MPCC under several operating modes, other groups of subsets must be defined when dealing with VVs located in the outer hexagon especially under a limited DC link. To address this problem, two extended subsets are proposed in Section 3.

3 Proposed predictive current control with GAVVs

3.1 Analytical formulation of the proposed GAVVs approach

Fig. 2 shows the space vector that can be generated in a seven-level CHB inverter. There are three families of subsets. The first type, denoted by G_7, is a group of seven VVs which is used in the algorithm presented in [11]. The second family, denoted by G_5, is a group of subsets of five adjacent VVs. The third family, denoted by G_4, is a group of four adjacent VVs. Some VVs of each family can generate a higher CMV, especially for G_5 and G_4, since three of their VVs are located in the outer hexagon. The main advantage related to these new subsets is that they contain VVs with higher amplitude, which is useful to fully track the current reference during the operation with a DC-link voltage drop. This voltage drop can be observed in PV systems subjected to partial shading or low irradiance conditions.

For an ML-CHB with L levels, the m_{V0} number of VVs in the $\alpha\beta$ frame and their associated CMV can be formulated as shown in (11). When the CMV is minimised, as mentioned earlier in Section 2, the m_{V0} VVs are reduced to m_V states without redundancies. These non-redundant VVs are divided into three types of subsets, consisting of seven, five and four adjacent VVs, respectively. By retaining only the positions of the arranged non-redundant VVs, m_V positions are stored in a vector, denoted by P, which is defined in (12). As a result, the subset position vector SP can be subdivided into three subset positions, $SP_{ad,7}$, $SP_{ad,5}$ and $SP_{ad,4}$, and used to index the VVs contained in subsets G_7, G_5 and G_4 arranged, for example, as presented in Fig. 2

$$v_{\alpha\beta o} = \begin{bmatrix} v_{\alpha\beta.0} & v_{cm.0} \\ v_{\alpha\beta.1} & v_{cm.1} \\ \vdots & \vdots \\ v_{\alpha\beta.m_{V0}} & v_{cm.m_{V0}} \end{bmatrix} \tag{11}$$

$$v_{\alpha\beta} = v_{\alpha\beta o}\big|_{V_{\rm cm} \le \frac{1}{3}V_{\rm dc}} = \begin{bmatrix} v_{\alpha\beta.0} \\ v_{\alpha\beta.i} \\ \vdots \\ v_{\alpha\beta.m_V} \end{bmatrix} \rightarrow P = \begin{bmatrix} P_0 \\ P_i \\ \vdots \\ P_{m_V} \end{bmatrix} \tag{12}$$

The subset positions $SP_{ad,7}$, $SP_{ad,5}$ and $SP_{ad,4}$ shown in (13a) to (13c) are made available to the online system through the selection of the subset (SS_{ad}) of adjacent vectors for the next sample (Fig. 1). This scheme selects the next subset from among the three families of subsets. The choice is dictated by the previous position of the optimal vector. Thus, when the optimal vector at the kth sample has a position value equal to P_{k-1}, the subset at the kth sample is given by (14).

As an example, the 343 VVs for a seven-level CHB are reduced to 127 VVs by minimising the CMV. By looking for the equidistant VVs for each VV achieved after CMV minimisation, the subset position of each type goes from 0 to 90 for SP_{7ad}, from 91 to 120 for SP_{5ad} and from 121 to 126 for SP_{4ad}. For the same example considered in Section 2, if $P_{k-1} = 106$ is the previous optimal state position, the subset of candidate solutions used at the next sample is $SP_{106} = [106\ 124\ 107\ 77\ 76]$, which contains both VVs number 124 and 107. Thus, MPCC will compute VVs only for SP_{106} positions to find the best state at the kth sample

$$SP_{7ad} = \begin{bmatrix} SP_0 \\ SP_i \\ \vdots \\ SP_{G_7-1} \end{bmatrix} = \begin{bmatrix} P_{0.1} & P_{0.2} & \cdots & P_{0.7} \\ P_{i.1} & P_{i.2} & \cdots & P_{i.7} \\ \vdots & \vdots & \vdots & \vdots \\ P_{(G_7-1).1} & P_{(G_7-1).2} & \cdots & P_{(G_7-1).7} \end{bmatrix} \tag{13a}$$

$$SP_{5ad} = \begin{bmatrix} SP_{G_7} \\ SP_i \\ \vdots \\ SP_{(G_{75}-1)} \end{bmatrix} = \begin{bmatrix} P_{(G_7).1} & P_{(G_7).2} & \cdots & P_{(G_7).5} \\ P_{(i).1} & P_{(i).2} & \cdots & P_{(i).5} \\ \vdots & \vdots & \vdots & \vdots \\ P_{(G_{75}-1).1} & P_{(G_{75}-1).2} & \cdots & P_{(G_{75}-1).5} \end{bmatrix} \tag{13b}$$

$$SP_{4ad} = \begin{bmatrix} SP_{G_{75}} \\ SP_i \\ \vdots \\ SP_{(m_V-1)} \end{bmatrix} = \begin{bmatrix} P_{(G_{75}).1} & P_{(G_{75}).2} & \cdots & P_{(G_{75}).4} \\ P_{(i).1} & P_{(i).2} & \cdots & P_{(i).4} \\ \vdots & \vdots & \vdots & \vdots \\ P_{(m_V-1).1} & P_{(m_V-1).2} & \cdots & P_{(m_V-1).4} \end{bmatrix} \tag{13c}$$

$$SP_k = SP_i = \left[P_{(i).1} \quad P_{(i).2} \quad \cdots \quad P_{(i).[7-(7-j)]}\right], \text{if} P_{k-1} = P_i \tag{14}$$

where $1 \le i \le m_V$, $G_{75} = G_7 + G_5$ and $j \in \{7, 5, 4\}$.

3.2 Guidelines for implementing the proposed MPCC based on GAVVs

The upper part of Fig. 1 presents the block diagram of the proposed algorithm, which is subdivided into two parts: the offline and online algorithms. Depending on the number of levels of the converter, the offline algorithm can be computed first to make the different subset positions (SP) available to the MPC through the block SS_{ad}, which runs online. Among the m_V non-redundant VVs, only one subset, the one with position SP_i, is selected based on the previous optimal position. Thus, the MPCC algorithm is computed in a way similar to the standard MPCC, but it only considers the VVs indexed by the block SS_{ad} for the positions contained in SP_k.

The proposed controller offline and online algorithms are summarised below.

3.2.1 Offline algorithm:

Step 1: Read L and $V_{\rm dc}$;
Step 2: Generate the m_{V0} VVs (GVVs) by using the product of $V_{\rm dc}$ and the modulation signal in the $\alpha\beta$-axis. The modulation signal is obtained based on the Gray code principle with $[-C, -C+1, \ldots, 0, \ldots, C-1, C]$ as the fixed states instead of [0, 1] or [−1, 1] as used for a 2L-VSI;
Step 3: Calculate $v_{\alpha\beta 0}$ for all m_{V0} VVs where v_0 is CMV;
Step 4: Search the non-redundant VVs that minimise CMV (11) and then arrange their positions in ascending order from 1 to m_V in P with respect to their amplitude and phase;
Step 5: Search for each VV position (12) and, its corresponding subset position SP_i (13) with the nearest VVs.

3.2.2 Subset selection scheme (first online block): The previous optimal state position (P_{k-1}) is used to find the VVs subset position that will be computed during sample k.

Step 1: Read P_k
Step 2: $SP_{k+1} \leftarrow SP_i$, if $P_k = P_i$
Step 3: Send SP_k to MPCC, and return to step 1.

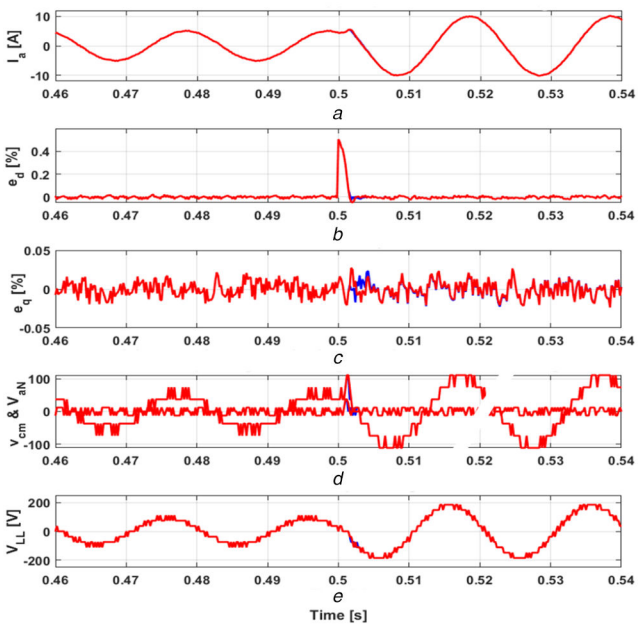

Fig. 3 *Simulation results under a nominal DC link (V_{dc}): MPCC-7adj (blue) and MPCC-GAVV (red)*

(a) Load current, ***(b)*** Current error in d-axis, ***(c)*** Current error in q-axis, ***(d)*** Inverter phase ground voltage and common mode voltage, ***(e)*** Line-line output voltage

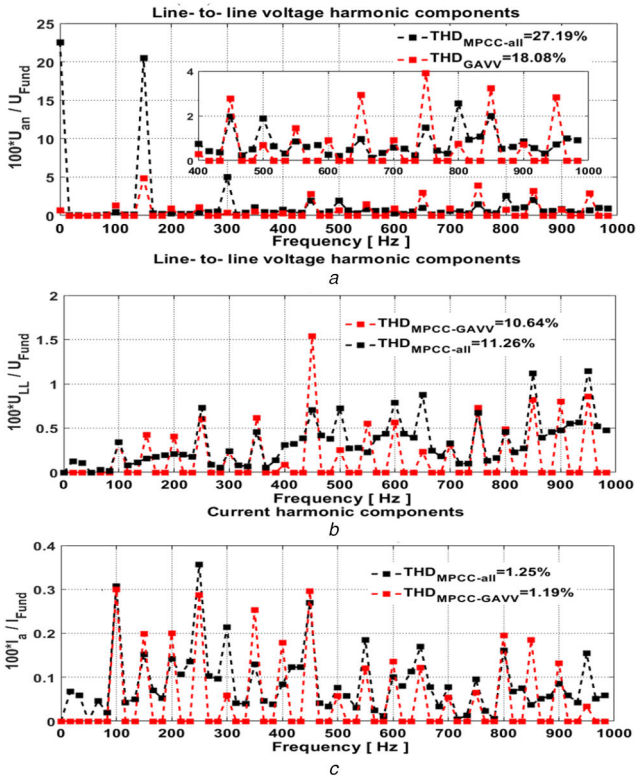

Fig. 4 *Voltage and current spectra under normal operation*

(a) Phase-ground voltage harmonics components, ***(b)*** Line-line voltage harmonics components, ***(c)*** Current harmonic components

3.2.3 MPCC based on extended adjacent states (second online block): The predictive control algorithm is similar to [11], with delay compensation:

Step 1: Measure $i(k)$;
Step 2: Apply the optimal VV $v(k)$;
Step 3: Predict the current $i^p(k+1)$ (5);
Step 4: Send P_k to the subset selection online block and read SP_{k+1} according to (14);
Step 5: Predict the j load currents using (7) at SP_{k+1} positions;
Step 6: Evaluate g using (8) for all j positions SP_{k+1};
Step 7: Find the optimal position P_{k+1};
Step 8: Store P_{k+1} and return to step 1.

The above algorithm uses subsets G_7, G_5 and G_4 with seven, five and four VVs, respectively. To avoid the use of VVs with high CMV, or the use of only two types of subsets, a restriction should be placed on steps 4 and 8 of the second online block. For example, to avoid VVs with the highest CMV, located at positions 121–126, P_k cannot be updated if one of these VVs is the optimum VV, which means that the previous subset will be used again during the next sample. Moreover, to use only subsets with seven and five VVs (G_7 and G_5), P_k should be updated only if $P_k \leq (G_{75} - 1)$; otherwise, P_{k-1} should be sent in step 4 of the online block. In contrast to the control strategies reported in the literature, MPCC-GAVVs do not need to include additional terms in the cost function to avoid VVs with a higher CMV located in the outer hexagon.

4 Numerical validation

The numerical validation presented in this section considers the general structure shown in Fig. 1 with a seven-level inverter connected to an RL load. MPCC-all (in black), MPCC-7adj (in blue) and MPCC-GAVV (in red) have been implemented using MATLAB/Simulink with some of the H-bridges operating with a reduced DC-link voltage to illustrate the voltage variation among PV cells. In the analysis in the time domain, only the proposed controller and MPCC-7adj are represented for the sake of clarity.

The first analysis considers the inverter in normal mode, and the DC-link per CHB is at least equal to 37 V, which is obtained by considering the maximal current through the load resistance and a 10% fluctuation. The simulation is performed for 1 s with a current step change from 5 to 10 A at 0.5 s, but to better highlight the transience, the results are presented just around the current reference change. The results of this case are presented in Fig. 3. MPCC-GAVV and MPCC-7adj presented essentially the same transient time and small current errors, which were bounded by ±0.04% in the steady state, as can be seen in Figs. 3*a*–*c*. In addition, voltages are balanced with a CMV equal to one-third of the DC-link per CHB for both controllers (Figs. 3*d* and *e*). The main advantage of using the adjacent states approach compared with MPCC based on all states is that the low-frequency harmonic components of the line-to-neutral output voltages have reduced magnitudes due to the symmetry of the signal. Moreover, the average switching frequency is almost constant at around 400 Hz. This is not the case for MPCC with all states, since the phase-to-neutral voltage is not symmetric even though the line-to-line voltages are symmetric [11]. Therefore, its phase-to-neutral voltage contains several harmonic components, which leads to higher THD when compared with the proposed approach (Fig. 4).

The second analysis considers a voltage drop condition, which is more likely to require a higher number of VVs that belong to the outer hexagon. This mode often occurs in PV systems, which are subject to the fall of irradiance or partial shading and dust settlement on PVs connected to CHBs. In addition, in power grids, a drop in or even failure of DC-link voltage may occur in several of the three-phase AC/DC converters or in the primary or secondary winding of the multipulse transformer (for more details, refer to [16]).

The results of both controllers for a voltage drop per CHB cell of 25% are presented in Figs. 5 and 6. For higher current reference, the proposed controller still presents good tracked current with fewer ripples than MPCC-7adj. However, the steady-state current error, in the *d*-axis, increases with respect to the nominal case, as can be seen in Fig. 5*b* (red colour). This happens because the controller is unable to track the full rated load current value with a limited DC-link voltage. However, the results are better than the ones of MPCC-7adj for both axes when the rated current reference is considered. In addition, the number of commutations with MPCC-GAVV is expected to be smaller than with MPCC-7adj,

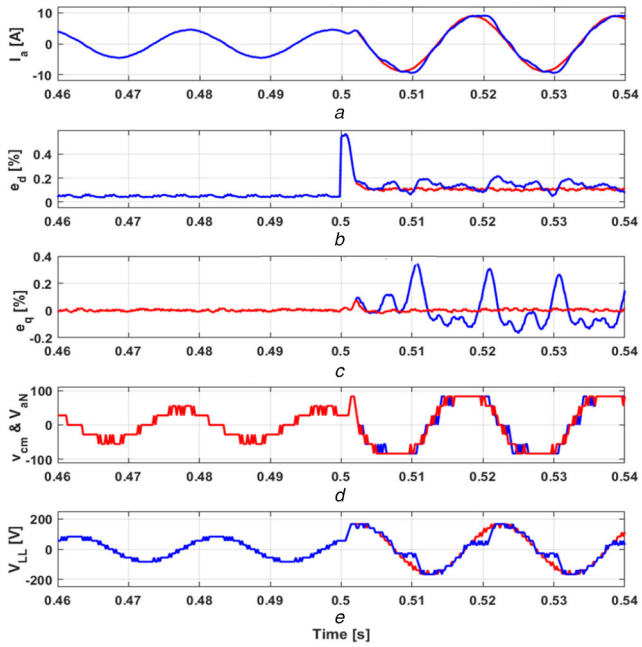

Fig. 5 *Time-domain results for a simulation with 0.75 V_{dc}*

(a) Load current, ***(b)*** Current error in d-axis, ***(c)*** Current error in q-axis, ***(d)*** Inverter phase ground voltage and common mode voltage, ***(e)*** Line-line output voltage

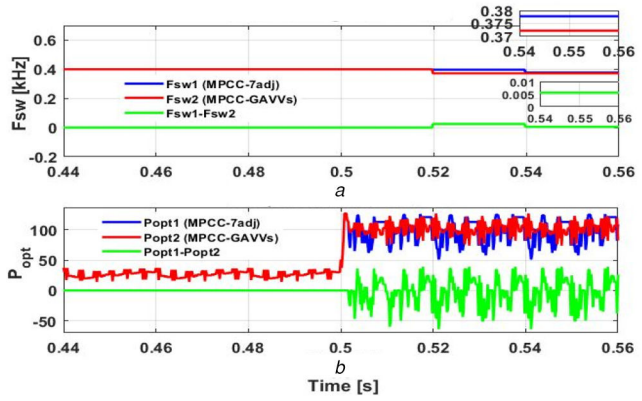

Fig. 6 *Results of the optimisation process for a simulation with 0.75 V_{dc}*

(a) Switching frequencies, ***(b)*** Optimal state positions

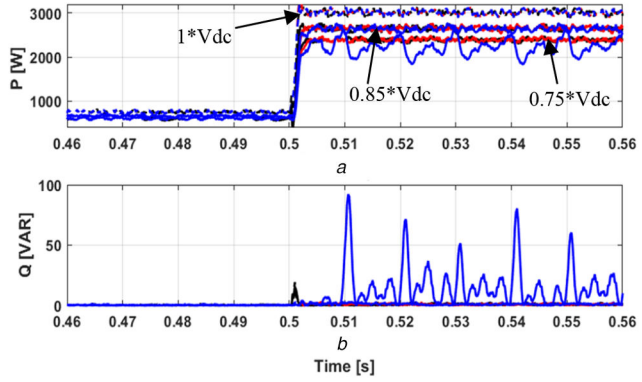

Fig. 7 *Active and reactive power results with 1V_{dc}*

(a) Active power, ***(b)*** Reactive power

since in the proposed approach most of the VV candidates require changes in only one phase, as can be seen in Fig. 6.

As shown in Fig. 7, the proposed controller achieves a power balance which is equivalent to MPCC-all and is better than MPCC-7adj. From the results, the proposed controller is a good choice for grid-connected PV systems, since it is able to extract the actual maximum power from the power plant and also send to the grid a symmetric and balanced output voltage and current with good power quality without having to set a new current reference during a period of low irradiance.

Under inductance variation both controllers achieve the same results with the current ripples increasing by the decrease of the inductance value (Figs. 8*b* and *c*). Even though not shown in Fig. 8, both controllers have good response for a small resistance change but for the load resistance which increases widely by 50% for instance (Fig. 8*a*), the current with MPCC-7adj (in blue) is distorted under full current reference due to the inability to predict the right subsets in the saturation zone.

To validate the robustness of the proposed controller over a DC-link unbalance across the capacitor, two cases of inter-phase voltage imbalance have been considered, and the simulation results are presented in Figs. 9 and 10. In the first case (case 1), the inter-phase imbalance is considered in phase *b* $v_b = V_{dc}[0.85 \quad 0.2 \quad 0.85]$ and the other phases observe only a voltage drop, $v_a = v_c = V_{dc}[0.85 \quad 0.85 \quad 0.85]$. The second case (case 2) considers a voltage drop associated with the inter-phase voltage imbalance in all phases, such that: $v_a = V_{dc}[0.85 \quad 0.85 \quad 0.625]$, $v_b = V_{dc}[0.85 \quad 0.85 \quad 0.2]$ and $v_c = V_{dc}[0.85 \quad 0.4 \quad 0.85]$. In both cases, even without using an additional compensation strategy, the proposed controller still has the ability to follow the current with admissible balanced current and line-to-line voltage (Figs. 9 and 10 in red). The resulting power absorbed by the load when the proposed controller is used is not balanced as in the normal mode operation, but the active power fluctuation is quite limited. Since operation in the saturation zone decreases the controller performance, the DC-link voltage should be increased or the current reference should be limited, but in some situations none of the solutions is possible and the proposed controller can present a satisfactory response. In conclusion, the proposed approach provides acceptable performance even under inter-bridge voltage imbalance mode operation. These characteristics are the key advantages of the proposed method over the classical MPCC based on adjacent VVs.

5 Experimental validation

5.1 Experimental set-up

A picture and the block diagram of the reduced scale experimental set-up used to validate the proposed controller is shown in Fig. 11. Further details are presented in [16, 17]. A scheme with three series-connected H-bridges per phase is considered. Each H-bridge uses only two legs of a three-phase inverter module SK 15 DGDL 126 ET. The supply of these modules was done using a phase-shifting transformer for isolation, as discussed in [17]. To emulate the voltage drop which is characteristic in PV plants, three variable AC transformers (variacs) are used: one before the transformers to allow a DC-link change across all CHBs, and the remaining ones used to generate a voltage drop across two given cells to achieve inter-bridge voltage unbalance among the phases.

The MPCC-7adj and MPCC-GAVVs algorithms were implemented in a field-programmable gate array: Altera Cyclone II EP2C8Q208C8N with the Quartus II software [18, 19]. The DSP TMS 320F2812PGFA generates the current reference setpoints and also embeds the offline algorithm that can be updated, depending on the number of levels and DC-link voltage used by the power converter. The acquisition of the measured current is carried out by the Simulink Real-Time System through a DAQ board PCI 6229. The parameters used for this experiment are shown in Table 2.

The results with MPCC-GAVV under a nominal DC-link voltage (Fig. 12) present a good ability to track the current reference value. The switching frequency and the optimal VV positions are similar to the ones of MPCC-7adj, as shown in Fig. 13. However, the difference between the switching frequencies and the selected optimal VV is not zero, a different result from what was observed in simulation. This is due to the fact that both controllers have been recorded with a difference in phase, as well as due to system parameter uncertainties and DC-link fluctuation.

For a total DC-link voltage drop equal to 15% (5% per cell), both controllers can track the half current reference. However, under maximal load current MPCC-7adj is unable to accurately

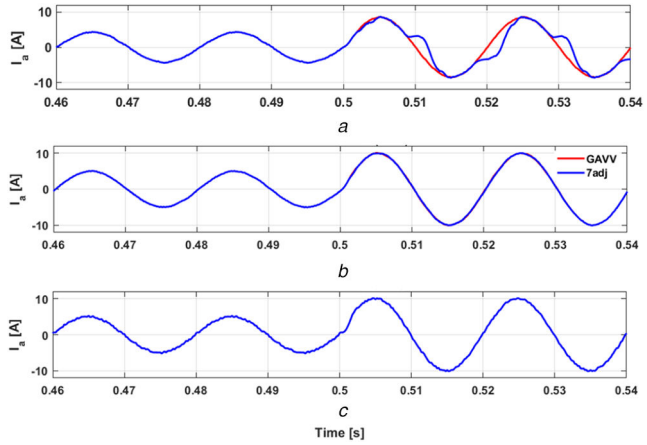

Fig. 8 *Current response under load resistance and inductance variation*
(a) Load current (+R/2), ***(b)*** Load current (+L/2), ***(c)*** Load current (-L/2)

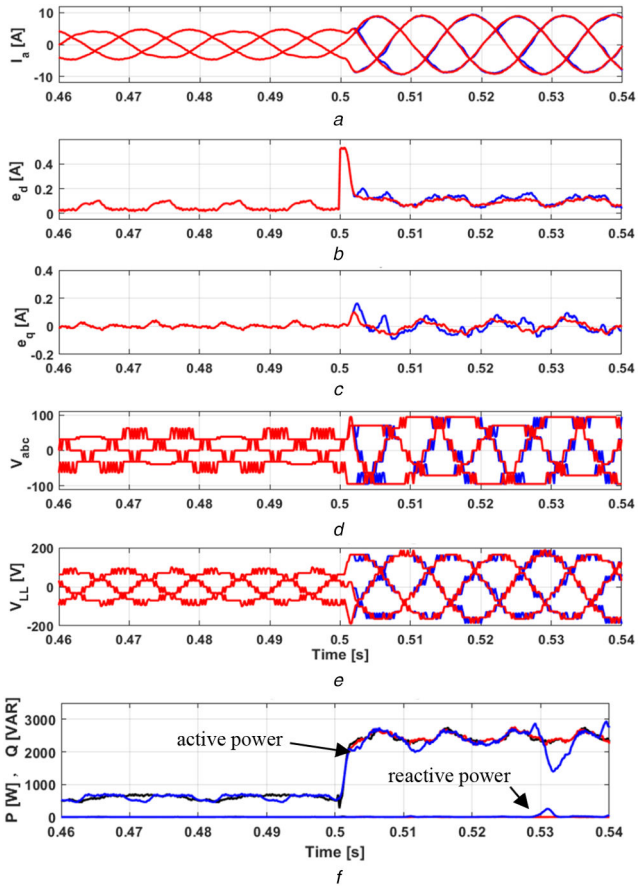

Fig. 9 *Simulation results under drop with inter-bridge voltage imbalance on phase b: proposed controller (red); MPCC-7adj (blue) and MPCC-all (black)*
(a) Load current, ***(b)*** Current error in d-axis, ***(c)*** Current error in q-axis, ***(d)*** Inverter phase ground voltage and common mode voltage, ***(e)*** Line-line output voltage, ***(f)*** Active and reactive powers

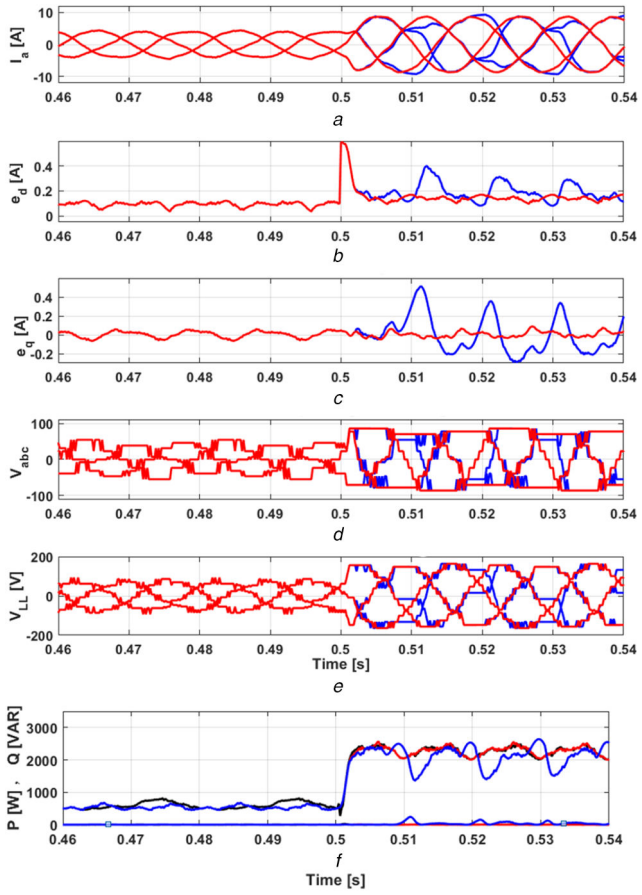

Fig. 10 *Simulation results under drop with inter-bridge voltage imbalance on all phases: MPCC-GAVV (red); MPCC-7adj (blue) and MPCC-all (black)*
(a) Load current, ***(b)*** Current error in d-axis, ***(c)*** Current error in q-aixs, ***(d)*** Inverter phase ground voltage and common mode voltage, ***(e)*** Line-line output voltage, ***(f)*** Active and reactive powers

track the reference (Fig. 14 in blue), while the proposed controller keeps its ability to follow the current reference as in the normal operation mode. In this case, the switching frequency of the proposed controller is about 300 Hz, which represents a reduction of around 100 Hz compared to the value obtained in normal operation (Fig. 15).

Fig. 16 summarises an analysis of the trade-offs in the performance parameters for DC-link voltage drop from 0 to 20% V_{dc} across all the cells with a step change of 5% V_{dc}. To investigate the impact of working under voltage drop compared to the nominal operation, three performance indices have been chosen to summarise the trade-offs between the proposed and the classical controllers: current total harmonic distortion, switching frequency and average steady-state current error (Fig. 16*a*–*c*).

Under half reference (3.5 A) both controllers achieve similar performance with a total harmonic distortion of <5% and a switching frequency under 500 Hz. Moreover, smaller average current errors are also observed.

The DC-link voltage drop does not affect the tracking ability of the controllers under half reference since the remaining voltage is still high enough for both controllers to track the current with good performance without the need for VVs located in the outer hexagon. However, under full current reference (7 A) with a voltage drop ranging from 5 to 20%, only the proposed controller

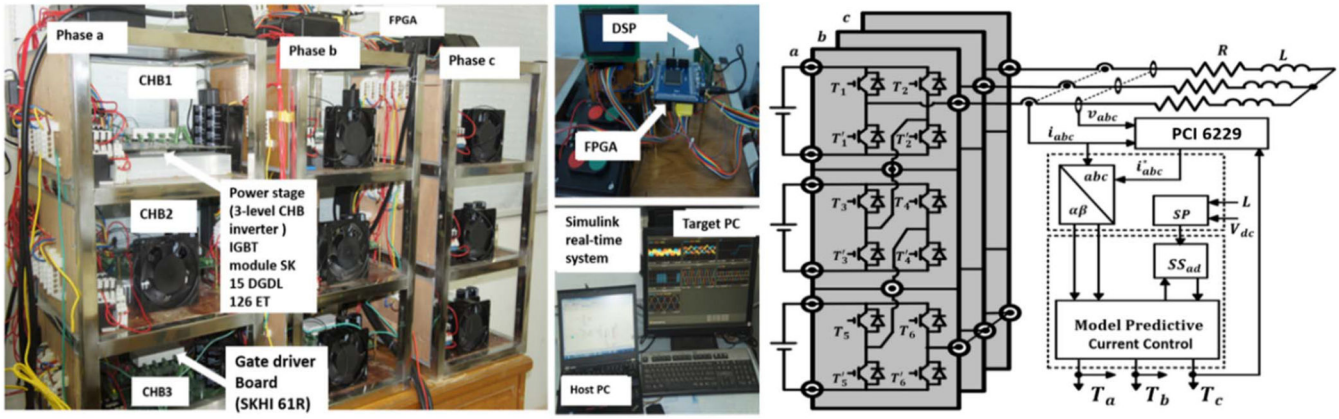

Fig. 11 *Experimental set-up: (left) actual set-up; (right) simplified overview*

Table 2 Simulation and experimental parameters

Parameters	Simulation	Experiment
DC-link voltage per cell	37 V	37 V
resistance, R	$R = 10\ \Omega$	$R = 15\ \Omega$
inductance, L	$L = 10$ mH	$L = 30$ mH
sampling frequency	$f_s = 5$ kHz	$f_s = 5$ kHz

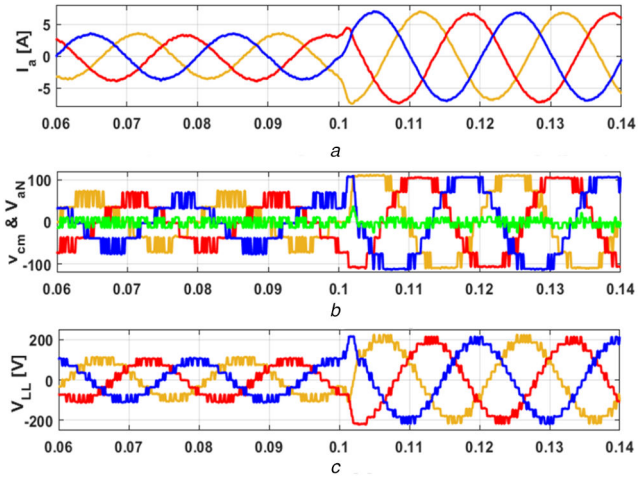

Fig. 12 *Experimental results under nominal V_{dc} with MPCC-GAVV*

(a) Load current, ***(b)*** Inverter phase ground voltage and common mode voltage, ***(c)*** Line-line output voltage

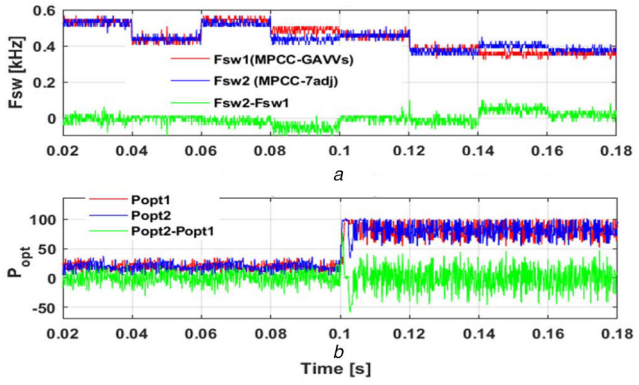

Fig. 13 *Switching frequencies and optimal VV positions under V_{dc}*

(a) Switching frequencies, ***(b)*** Optimal state positions

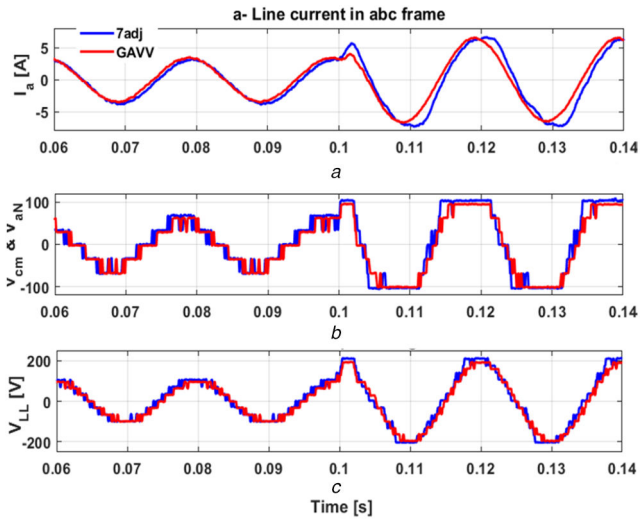

Fig. 14 *Experimental results under 0.95 V_{dc} with MPCC-GAVV*

(a) Load currents, ***(b)*** Inverter phase ground and common mode voltages, ***(c)*** Line-line output voltages

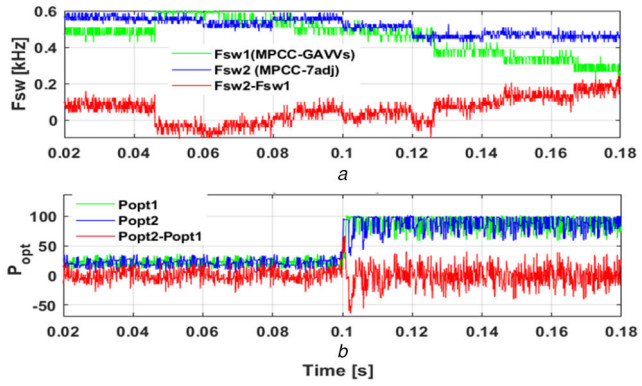

Fig. 15 *Switching frequencies and optimal VV positions under 0.95 V_{dc}*

(a) Switching frequencies, ***(b)*** Optimal state positions

achieves reasonable performance, with a THD still smaller than 5% and the switching frequency decreasing considerably by up to 200 Hz, with the DC-link drop voltage. Even though the mean steady-state current error increases with the DC-link voltage drop, the increase is not as fast as in MPCC-7adj.

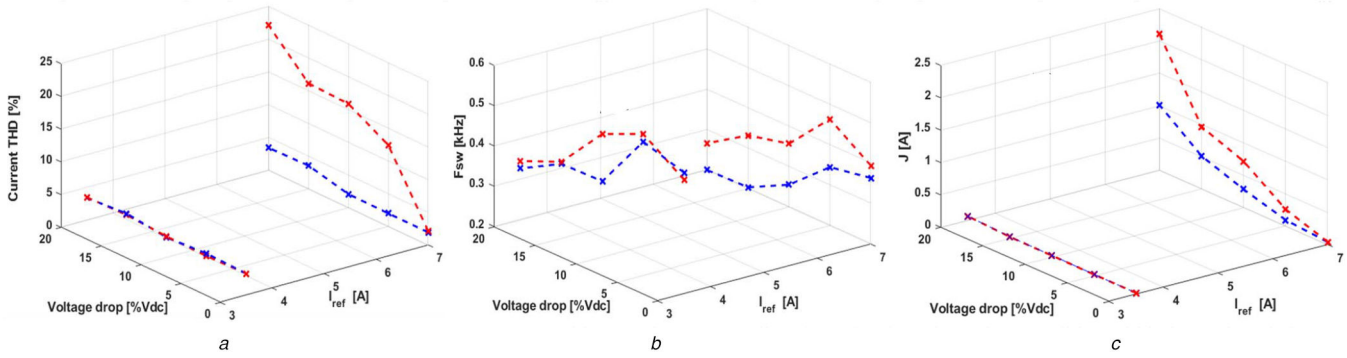

Fig. 16 *Experimental performance indices of MPCC-GAVVs (blue) and MPCC-7adj (red) under the voltage drop condition within inter-phase balance*
(a) Current THD, ***(b)*** Switching frequency, ***(c)*** Average steady-state current error

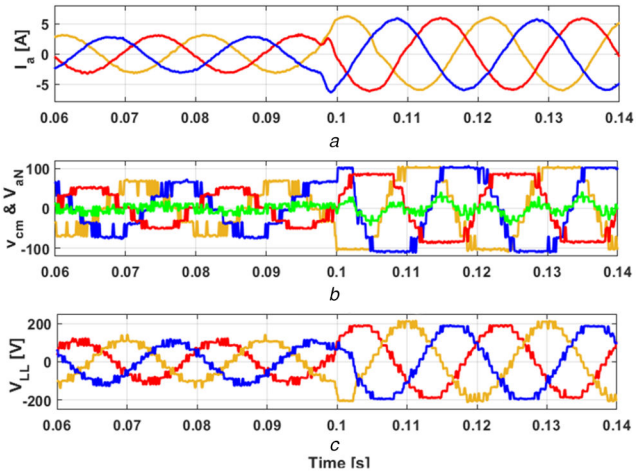

Fig. 17 *Experimental results with the same voltage drop scenario as in case 1*
(a) Load currents, ***(b)*** Inverter phase ground and common mode voltages, ***(c)*** Line-line output voltages

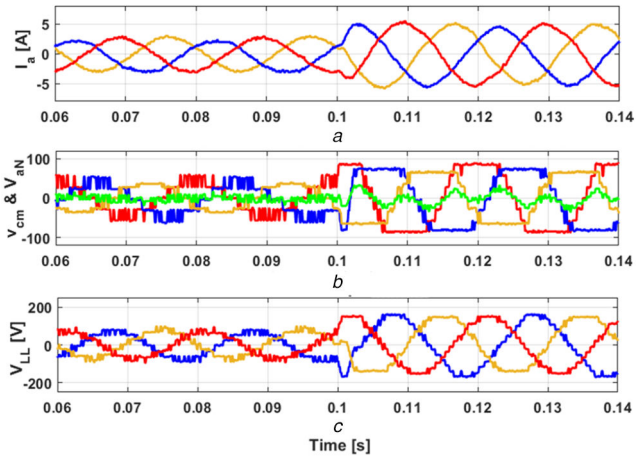

Fig. 18 *Experimental results with a voltage drop scenario similar to case 2*
(a) Load currents, ***(b)*** Inverter phase ground and common mode voltages, ***(c)*** Line-line output voltages

The proposed controller still achieves acceptable current performance during voltage imbalance across the cells (Figs. 17 and 18). However, the current harmonics performance parameters (THD and current error) decrease and the power imbalance increases as well. This result can be improved by explicitly taking the capacitor voltage balance into account in the cost function. Moreover, it is important to note that MPCC-GAVV does not consider an additional control scheme to specifically deal with the imbalance coming from either the DC-link [6] of CHB or from the unbalanced grid [20, 21].

6 Conclusion

A model predictive current controller is proposed in this paper to solve some of the problems faced by MPCC based on seven adjacent VVs (MPCC-7adj) in multilevel converters under DC-link voltage drop, which is often observed in PV power plants. To obtain better behaviour while keeping the computational burden at a reasonable level, a GAVV approach for MPCC has been proposed. As a result, an MPCC with three types of subsets instead of one with seven VVs, as used in one of the classical approaches is suggested. The proposed method has been presented using a generic analytical formulation which is independent of the number of levels in the inverter.

The simulation and experimental results show that the proposed controller is equivalent to MPCC-7adj when a nominal DC-link voltage is used. However, when the ML-CHB inverter is subjected to DC-link voltage drops with or without an inter-phase voltage imbalance, the proposed controller is able to keep a reasonable response even at high current references, which is challenging to achieve with the classical MPCC-7adj. The use of the VVs of the outer hexagon under the voltage drop operating mode increase the CMV and also the steady-state current error compared to under normal operation and should be avoided. However, when it is not possible to avoid this situation, such as during partial shading in PV power plants, the proposed controller is a potential solution to maintain good current tracking, since it is able to avoid the problems faced by MPCC-7adj while retaining fast computation times and limited switching losses.

7 Acknowledgment

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