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Single pole switch leg based multi-port converter with an energy storage

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Abstract: This study presents a new multi-functional control system for a multi-port energy converter that interfaces one bi-directional battery port, one dc input port, and three output ports. Only one single-leg active switching element (a module type can be used) is employed in the system, and hence the single leg requires digital switching signals for a multi-functional operation to regulate output voltages and to simultaneously manage the battery port. The proposed system has buck–boost conversion capabilities to accommodate wide range, various input sources and output loads. In addition, the single leg requires no dead time due to an integrated impedance network, which will improve the system reliability and performance. Furthermore, the proposed structure can charge a battery even when the input and capacitor voltages are much lower than the battery voltage and hence it significantly improves charging behaviours. The proposed multi-functional control strategy and the converter structure are explained in detail. Then the feasibility and performance of the converter are verified both by computer simulations and experiments based on the Texas Instruments TMS320F28335 digital signal processor.

1 Introduction

The multi-port converters (MPCs), which have multi-input and multi-output (MIMO), are gaining an increasing interest for energy system applications [1–16]. The MIMO converter has advantages over several independent converters, including fewer circuit elements and conversion stages which will result in a more compact size and a lower cost. In spite of the advantages, MIMO converters suffer interdependency between outputs and their complex control structures. To achieve a more intelligent power management, energy storages play an important role for variety of application areas including renewable energy generation systems, electric vehicles, and robots. Therefore, MPCs, which include an energy storage port(s), are increasingly required.

This paper aims to research a new MPC including an energy storage (battery or ultra-capacitor) port based on a multi-functional, single-leg converter with an impedance network. The impedance network based converters require no dead time since two switches in one leg can be turned on at the same time, which will increase system reliability and output waveform quality [17–19]. Thus, impedance network based structure is typically used for single output converters and is not suitable for multi-output converters (especially for multi-independent adjustable ac loads) because of the shoot-through period [17–19]. For a multi-output converter, the shoot-through period (which makes an output voltage zero) from one inverter (or from one output side) will limit the performance of the other inverters (or the other output sides) if they need to operate independently. Therefore, in this paper, a new structure and a multi-functional control method are proposed for a multiple output converter which integrates an impedance network and an energy storage (battery or ultra-capacitor) port.

This structure employs just one leg (a module type switching element can be used) which requires no dead time. The outputs are not directly influenced by a shoot-through action and hence the MPC can accommodate multiple dc or ac loads. In addition, the proposed structure has a better charging characteristic in terms of the limitation of input and capacitor voltage levels. For the proposed MPC, a charging is still possible even when the input and capacitor voltages are much lower than the energy storage voltage, which will significantly improve charging behaviours. Furthermore, the proposed MPC operates both in the buck and boost modes and hence it has a wide operational range suitable for various input sources and output loads.

A possible industrial application example can be plug-in hybrid electric vehicles and 48 V mild hybrid electric vehicles. Those systems have both a high-voltage battery (main battery) and a low-voltage battery (second battery) which can be connected to the input (main battery) port and to the energy storage port (second battery). The output port voltages can be decided based on electrical loads to optimise the voltage–current matching to improve the power density of the electrical loads.

The feasibility and performances are verified by computer simulations and a prototype experimental test bed. In the experiment, Texas Instruments' TMS320F28335 digital signal processor (DSP) has been used to control the MPC. Various steady-state and transient responses from different operating modes and load conditions have been presented to verify the proposed concept and control strategy.

2 Proposed multi-functional control and converter

Fig. 1*a* illustrates a conceptual block diagram of the proposed MPC and controller presenting a basic structure of the system. The converter contains total of five ports (one source port, one energy storage port, and three output ports). The output ports 1 and 2 provide approximately the same voltage level since they are connected to capacitors in a balanced impedance network. A buck–boost conversion is possible for the ports 1 and 2. The output port 3 voltage level is always higher than the input voltage (boost) and its voltage is dependent on the voltage regulation of the output 1, and hence this port is for an insensitive load. One bi-directional energy storage port is to charge/discharge either a battery or an ultra-capacitor. All three loads (loads 1–3) can be variable ac loads with inverters or dc loads. For this MPC operation, only two switches (single leg) and one diode are

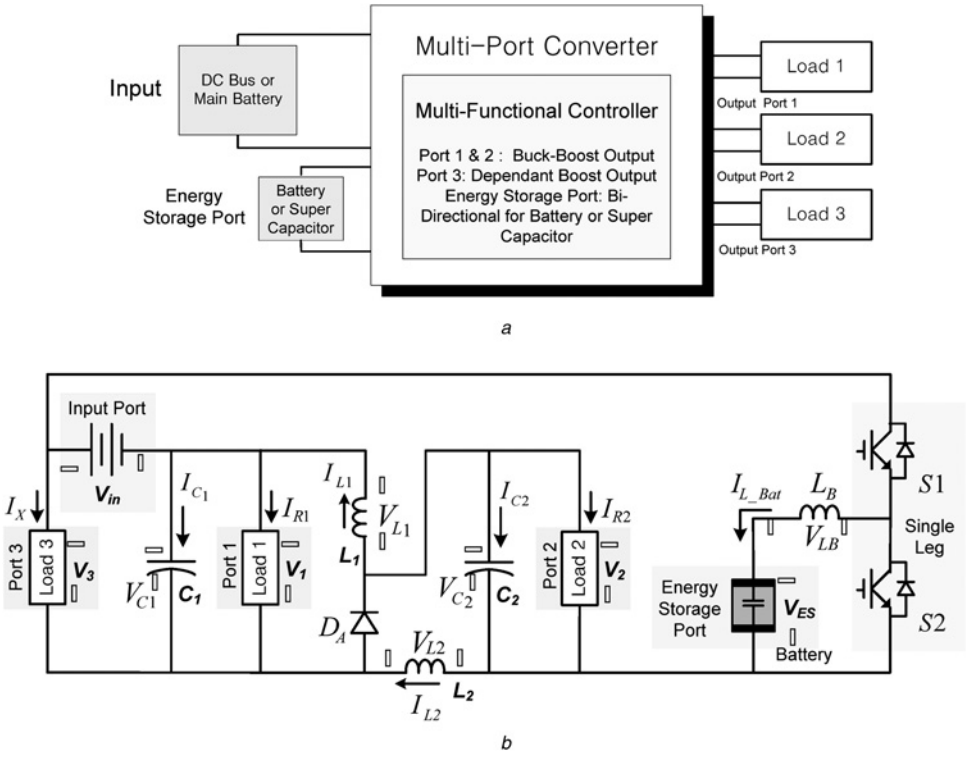

Fig. 1 *Proposed converter structure*

a Conceptual structure of the proposed converter and controller
b Circuit configuration of the proposed MPC with a bi-directional energy storage port

employed and hence the single leg requires a multi-functional operation.

2.1 Operational principles

As illustrated in Fig. 1*b*, the circuit structure of the proposed MPC contains two active switches (single leg in a module), a diode, and an impedance network (L_1, L_2, C_1, C_2). The switches ($S1$ and $S2$) require no dead time due to the existence of the impedance network. The ports 1 and 2 voltages are tightly regulated by a multi-functional controller while simultaneously managing the energy storage port's charging and discharging operations. The load port 3 is for a less sensitive load that needs a higher voltage than that of the ports 1 and 2 since the port 3 voltage

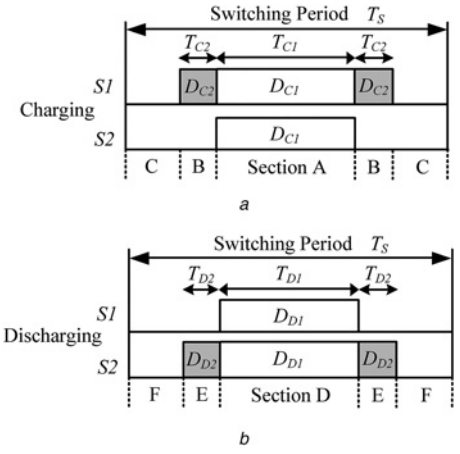

Fig. 2 *Switching strategy*

a Switching strategy for a charging case
b Switching strategy for a discharging case

($V_3 = V_{in} + V_{C_1}$) can vary if the input voltage is not constant. The preferred input source is a dc bus or a main battery which provide a stable dc voltage. For a straightforward explanation, the operational modes are divided into two cases, charging and discharging cases. For the charging case, the converter will charge an energy storage through its port while controlling the ports 1 and 2 voltages. To simplify the circuit analysis and controller design, three assumptions have been made:

(i) The capacitors and inductors are balanced and symmetrically connected and hence capacitor and inductor voltages and currents are approximately equal ($V_{L_1} \simeq V_{L_2} = V_L$; $V_{C_1} \simeq V_{C_2} = V_C$; $I_{L_1} \simeq I_{L_2} = I_L$; $I_{C_1} \simeq I_{C2} = I_C$). This is one of the ideal characteristics of the impedance network [17, 18]. However, at various load conditions, inductor currents will be different for the proposed MPC, and hence this assumption's influence on the controller has been analysed and discussed in a later section.
(ii) Two load currents for loads 1 and 2 are assumed to be approximately equal ($I_{R1} \simeq I_{R2} = I_R$) for a simper circuit analysis. The influence of different load currents is discussed and analysed in detail in a later section.
(iii) Analysis and controller design have been performed assuming a continuous conduction mode.

To charge the energy storage port, the $S1$ switch needs to be turned on for a longer time than the lower switch $S2$. A switching strategy for the charging case is depicted in Fig. 2*a*.

In Fig. 2*a*, D_{C_1} is a duty ratio (T_{C_1}/T_S) to simultaneously turn on both $S1$ and $S2$ switches, and D_{C_2} is the duty ratio (T_{C_2}/T_S) for the additional ON period of the $S1$ switch to charge an energy storage. The equivalent circuits during the charging case are illustrated in Fig. 3 based on their switching statuses. During the section A period ($S1 = S2 = 1$) shown in Fig. 3*a*, the D_A diode is reverse biased (cathode terminal voltage is greater than that of the anode terminal) because of the shoot-through action and hence it is open circuited.

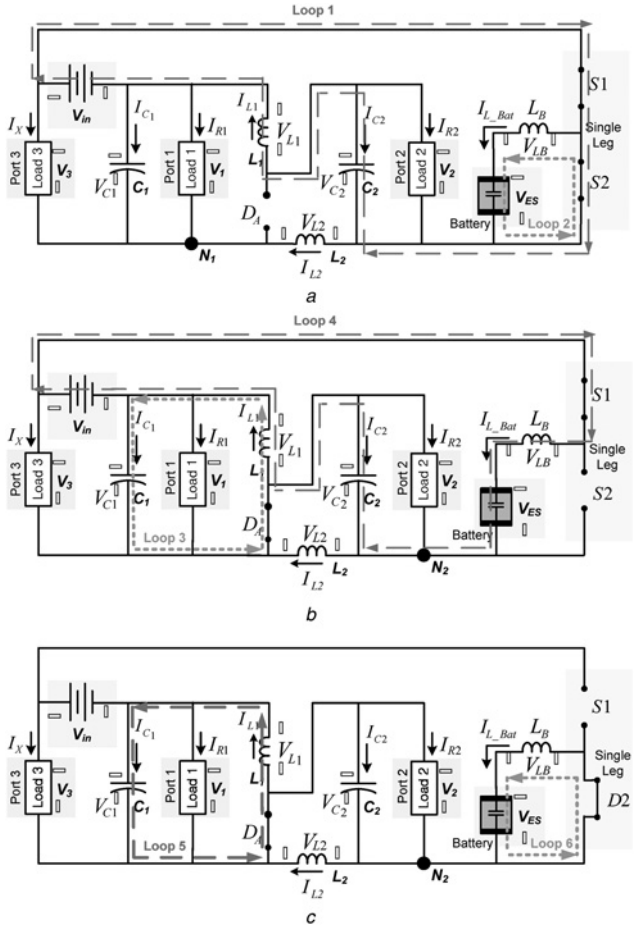

Fig. 3 *Equivalent circuits based on switching statuses for a charging case*

a $S1 = 1$, $S2 = 1$ (during section A in Fig. 2*a*)
b $S1 = 1$, $S2 = 0$ (during section B in Fig. 2*a*)
c $S1 = 0$, $S2 = 0$ (during section C in Fig. 2*a*)

From the loop 1 shown in Fig. 3*a*, $V_{L_1} = V_{\text{in}} + V_{C_2}$ is derived. Based on the aforementioned assumptions, the equation becomes $V_{\text{L}} = V_{\text{in}} + V_{\text{C}}$ as presented in Table 1. From the loop 3 shown in Fig. 3*b*, $V_{L_1} = -V_{C_1}$ is derived and from the assumptions, we have $V_{\text{L}} = -V_{\text{C}}$. In addition, based on the loop 4 shown in Fig. 3*b*, the energy storage side inductor voltage is derived ($V_{\text{LB}} = V_{\text{in}} + V_{C_2} - V_{L_1} - V_{\text{ES}} = V_{\text{in}} + 2V_{C_2} - V_{\text{ES}}$). The energy storage port current, $I_{\text{L\_Bat}}$, is positive during the charging case. Therefore, the anti-parallel diode, $D2$, is conducting (loop 6 shown in Fig. 3*c*) when both switches are off (section C) for a charging current's freewheeling.

On the basis of the three assumptions and equivalent circuits for a charging case ($I_{\text{L\_Bat}} > 0$), Table 1 is created for the inductor voltages, V_{L} ($= V_{L_1} = V_{L_2}$) and V_{LB} (energy storage port side inductor voltage). To simplify the analysis, the forward voltage drops of the switches and diode are ignored.

In Table 1, the V_{L} voltage is obtained based on the loops 1, 3, and 5 and V_{LB} voltage is from the loops 2, 4, and 6 at each section.

For the energy storage side inductor voltage, V_{LB}, the charging current will increase when V_{LB} is positive (section B case in Table 1). In other words, a charging is possible if $V_{\text{in}} + 2V_{\text{C}} > V_{\text{ES}}$. Therefore, even when the input voltage (V_{in}) and a capacitor voltage (V_{C}) are much lower than the energy storage voltage (V_{ES}), the summation ($V_{\text{in}} + 2V_{\text{C}}$) can be greater than the energy storage voltage and a charging is still then possible. This characteristic of the proposed structure can improve a charging behaviour.

Table 1 Inductor voltages during a charging case based on the switching status and the assumptions

Inductor voltages	Section A, $S1 = 1$, $S2 = 1$	Section B, $S1 = 1$, $S2 = 0$	Section C, $S1 = 0$, $S2 = 0$
V_{L}	$V_{\text{in}} + V_{\text{C}}$ (by loop 1)	$-V_{\text{C}}$ (loop 3)	$-V_{\text{C}}$ (loop 5)
V_{LB}	$-V_{\text{ES}}$ (by loop 2)	$V_{\text{in}} + 2V_{\text{C}} - V_{\text{ES}}$ (loop 4)	$-V_{\text{ES}}$ (loop 6)

Table 2 Capacitor current during a charging case

Parameter	Section A, $S1 = 1$, $S2 = 1$	Section B, $S1 = 1$, $S2 = 0$	Section C, $S1 = 0$, $S2 = 0$
I_{C}	$-I_{\text{L}} - I_{\text{X}} - I_{\text{R}}$	$I_{\text{L}} - I_{\text{L\_Bat}} - I_{\text{R}}$	$I_{\text{L}} - I_{\text{R}}$

In a steady state, average inductor voltages should be zero, and hence the following steady-state equations are derived based on Fig. 2*a* and Table 1

$$\overline{V_{\text{L}}} = (V_{\text{in}} + V_{\text{C}}) \cdot D_{C_1} - V_{\text{C}} \cdot 2 \cdot D_{C_2} - V_{\text{C}} \cdot \left(1 - D_{C_1} - 2 \cdot D_{C_2}\right) = 0 \quad (1)$$

$$\overline{V_{\text{LB}}} = -V_{\text{ES}} \cdot D_{C_1} + (V_{\text{in}} + 2 \cdot V_{\text{C}} - V_{\text{ES}}) \cdot 2 \cdot D_{C_2} - V_{\text{ES}} \cdot \left(1 - D_{C_1} - 2 \cdot D_{C_2}\right) = 0 \quad (2)$$

where $\overline{V_{\text{L}}}$ and $\overline{V_{\text{LB}}}$ are the average voltages of the impedance network inductor and the energy storage side inductor, respectively.

From (1), D_{C_1} in a steady state is derived as

$$D_{C_1} = \frac{V_{\text{C}}}{V_{\text{in}} + 2 \cdot V_{\text{C}}} . \quad (3)$$

Similarly from (2), D_{C_2} in a steady state is obtained as

$$D_{C_2} = \frac{V_{\text{ES}}}{2 \cdot (V_{\text{in}} + 2 \cdot V_{\text{C}})} . \quad (4)$$

Typical dc–dc converters use an inductor current to regulate an output capacitor voltage [20]. However, in the proposed circuit, two capacitors and inductors are cross-connected (impedance network) and hence controlling a capacitor voltage directly using an inductor current is not preferable if the load is widely changing (which is the case of the proposed converter since two loads are connected directly to the two capacitors).

Therefore, to control the capacitor voltage, a capacitor current is indirectly utilised for the inner current control loop. Then, output of the capacitor voltage controller can be a capacitor current command instead of an inductor current command. In this way, a linkage equation between the voltage controller and the inner current controller, relating the capacitor current and the inductor current, is required. Unlike in the case of the small signal model based voltage controller design, based on a linkage equation, a voltage controller that is not sensitive to wide operating points can be designed.

From Figs. 2*a* and 3, the average capacitor current can be derived. The node analysis is applied to the $N1$ node for the section A switching status (Fig. 3*a*) and the $N2$ node for the sections B and C as indicated in Fig. 3. Table 2 indicates the capacitor current at each section using the $N1$ and $N2$ nodes (based on the aforementioned assumption for simplification, $I_{\text{C}} = I_{C_1} = I_{C_2}$; $I_{\text{R}} = I_{R1} = I_{R2}$).

For the controller design, Tables 1 and 2 parameters will be expressed by average representations. This average representation means an average value during one cycle period. The average values are measurable setting analogue to digital conversion instants according to pulse width modulation (PWM) duty ratios.

The average capacitor current is obtained based on Table 2 and Fig. 2*a* as follows

$$\overline{I_C} = \left(-\overline{I_L} - \overline{I_X} - \overline{I_R}\right) \cdot D_{C_1} + \left(\overline{I_L} - \overline{I_{L\_Bat}} - \overline{I_R}\right) \cdot 2 \cdot D_{C_2} + \left(\overline{I_L} - \overline{I_R}\right) \cdot \left(1 - D_{C_1} - 2 \cdot D_{C_2}\right) \quad (5)$$

$$= \left(1 - 2 \cdot D_{C_1}\right) \cdot \overline{I_L} - D_{C_1} \cdot \overline{I_X} - D_{C_2} \cdot \overline{I_{L\_Bat}} - \overline{I_R} \,. \quad (6)$$

From (6)

$$\overline{I_L} = \frac{\overline{I_C} + D_{C_1} \cdot \overline{I_X} + D_{C_2} \cdot \overline{I_{L\_Bat}} + \overline{I_R}}{\left(1 - 2 \cdot D_{C_1}\right)}. \quad (7)$$

As mentioned previously, (7) is a linkage equation which relates the impedance network capacitor current and the inductor current, and hence the average inductor current command for the inner current controller will be derived by replacing D_{C_1} and D_{C_2} defined from (3) and (4)

$$\overline{I_L^*} = \frac{2 \cdot \left(2 \cdot V_C + V_{in}\right) \cdot \left(\overline{I_C^*} + \overline{I_R}\right) + 2 \cdot V_C \cdot \overline{I_X} + V_{ES} \cdot \overline{I_{L\_Bat}}}{2 \cdot V_{in}}. \quad (8)$$

where $\overline{I_L^*}$ and $\overline{I_C^*}$ are the average inductor and capacitor current commands. Using the linkage equation (8), the average inductor current command, which is required for the inner current controller, is calculated. In this way, the capacitor voltage controller outputs an average capacitor current command instead an average inductor current command unlike traditional dc–dc converter control structures. This process makes the design of the capacitor voltage controller more straightforward. In other words, by controlling $\overline{I_L}$, the average capacitor current, $\overline{I_C}$, can be indirectly controlled to make use of the simpler relationship between V_C and $\overline{I_C}$ instead the relationship between V_C and $\overline{I_L}$.

The average inductor voltages in (1) and (2) were derived at a steady state. Therefore, the general forms of those equations including transients are

$$\overline{V_L} = \left(V_{in} + V_C\right) D_{C_1} - V_C \cdot 2 \cdot D_{C_2} - V_C \left(1 - D_{C_1} - 2 \cdot D_{C_2}\right) = \left(V_{in} + 2 \cdot V_C\right) \cdot D_{C_1} - V_C \quad (9)$$

$$\overline{V_{LB}} = -V_{ES} \cdot D_{C_1} + \left(V_{in} + 2 \cdot V_C - V_{ES}\right) \cdot 2 \cdot D_{C_2} - V_{ES} \cdot \left(1 - D_{C_1} - 2 \cdot D_{C_2}\right) = 2 \cdot D_{C_2} \cdot \left(V_{in} + 2 \cdot V_C\right) - V_{ES} \quad (10)$$

From (9) and (10), the required duty ratios, $D_{C_1}^*$ and $D_{C_2}^*$ are finally calculated as

$$D_{C_1}^* = \frac{\overline{V_L^*} + V_C}{2 \cdot V_C + V_{in}} \quad (11)$$

$$D_{C_2}^* = \frac{\overline{V_{LB}^*} + V_{ES}}{2 \cdot \left(2 \cdot V_C + V_{in}\right)}. \quad (12)$$

where $\overline{V_L^*}$ and $\overline{V_{LB}^*}$ are the outputs of the inner current controller (for the outer capacitor voltage control) and the energy storage current controller, respectively. For the discharging case, the switching strategy needs to be modified to turn on the $S2$ switch longer as depicted in Fig. 2*b*.

For the discharging case, three switching statuses are used and the inductor voltages are summarised in Table 3 based on the three statuses as follows. The equivalent circuits for the discharging case are not presented here since the charging case was exemplified beforehand.

Table 3 Inductor voltages during a discharging case based on switching statuses

Parameters	Section D, $S1 = 1$, $S2 = 1$	Section E, $S1 = 0$, $S2 = 1$	Section F, $S1 = 0$, $S2 = 0$
V_L	$V_{in} + V_C$	$-V_C$	$-V_C$
V_{LB}	$-V_{ES}$	$-V_{ES}$	$V_{in} + 2V_C - V_{ES}$

Similar to the aforementioned charging case procedure, the final $D_{D_1}^*$ and $D_{D_2}^*$ duty ratio equations for discharging can be derived based on Fig. 2*b* and Table 3. Since the derivation procedure is similar to that of the charging case, only the resultant equations are presented in the following equations

$$D_{D1}^* = \frac{\overline{V_L^*} + V_C}{2 \cdot V_C + V_{in}} \quad (13)$$

$$D_{D2}^* = \frac{1}{2} \cdot \left(1 - D_{D1}^*\right) - \frac{\overline{V_{LB}^*} + V_{ES}}{\left(2 \cdot V_C + V_{in}\right)} \quad (14)$$

where D_{D1}^* is the required duty ratio to turn on both $S1$ and $S2$ switches and D_{D2}^* is for the additional ON period of the $S2$ switch for a discharging case. In addition, $\overline{V_L^*}$ is the output of the inner current control loop and $\overline{V_{LB}^*}$ is the output of the energy storage current controller. The resultant $\overline{I_L^*}$ equation (refer (8)) for discharging case is the same as the charging case, and hence it is not specified here.

2.2 Multi-functional controller design

The proposed MPC simultaneously controls port voltages and the energy storage port's charging/discharging current at the same time. Both voltage charging and current charging modes are possible for the energy storage (battery case) port. In this paper, a current charging/discharging for an energy storage is exemplified. Due to the characteristics of the balanced impedance network, the two capacitor voltage difference is negligibly small due to the interchanging current between two capacitors [17–19]. Therefore, in the control structure, one capacitor voltage (V_{C_1}) in the impedance network is directly controlled to regulate both of the port voltages (V_1 and V_2) while simultaneously managing the energy storage port. Then, the V_{C_2} voltage is approximately equal to V_{C_1}, and V_3 voltage will be $V_{C_1} + V_{in}$. The possible voltage difference between V_{C_1} and V_{C_2} (or V_1 and V_2) under various load conditions is discussed in a later section in detail.

For instance, if the nominal input voltage is 18 V and regulate V_{C_2} at 24 V dc while controlling the energy storage current at +2 A (charging case), then ports 1 and 2 voltages are tightly controlled at 24 V dc and the dependent port 3 voltage will stay at 42 V dc (if the input dc voltage is constant) while controlling the energy storage current at the commanded value (2 A).

As illustrated in Fig. 4*a*, the impedance network capacitor voltage control (V_{C_2}) has a dual loop. For the outer voltage control loop, an integral–proportional (IP) type controller is employed, outputting an average capacitor current command ($\overline{I_C^*}$). For a better step response and less overshoot, the IP voltage controller is used instead of the PI controller [21]. Based on the linkage equation (8), the average inductor current command is calculated ($\overline{I_L^*}$). For the inner current control loop, a proportional–integral (PI) current controller is used, outputting the average inductor voltage command ($\overline{V_L^*}$). Based on (11) and (12), the required duty ratios ($D_{C_1}^*$ and $D_{C_2}^*$) are calculated for a charging case. The inner current control loop is shown in Fig. 4*c*, where R_{L_1} is an equivalent series resistor in the impedance network inductor 1 (L_1).

The additional ON periods for $S1$ switch (charging case) and $S2$ switch (discharging case) are calculated from a PI current controller for the energy storage port. The output of the energy storage port's current controller is the average inductor voltage command, $\overline{V_{LB}^*}$. For a charging case, (12) is used to calculate a

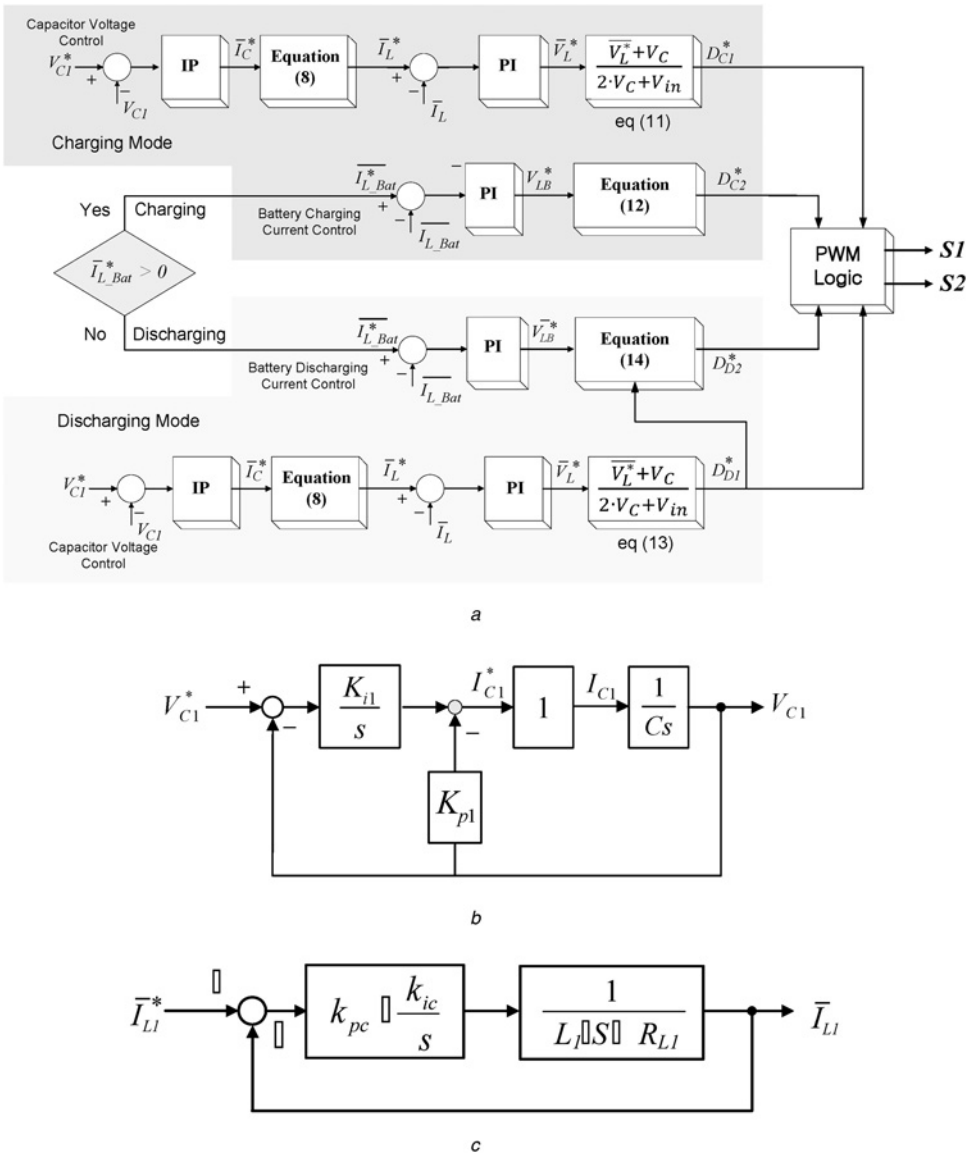

Fig. 4 *Control structure*

a Block diagram of the control structure for the MPC
b Simplified capacitor voltage control loop for ports 1 and 2
c Simplified block diagram of the current controllers

required duty ratio of the additional ON period for the $S1$ switch. For a discharging case, D^*_{D2} is calculated using (14) for the $S2$ switch.

Fig. 4*b* presents the simplified capacitor voltage control (IP controller) loop to regulate the V_1 ($=V_{C_1}$) voltage. The capacitor voltage is controlled through the indirect capacitor current control which can provide a linearised transfer function to the capacitor voltage control (as shown in Fig. 4*b*), and thus, the capacitor voltage controller can be easily designed. The inner current control loop is simplified as unity since the bandwidth of the inner current control loop is set to approximately ten times higher than that of the outer voltage control loop. The port 2 voltage ($V_2 = V_{C_2}$) is approximately the same as V_{C_1} for a balanced impedance network. As previously mentioned, this is due to the impedance network's characteristic of interchanging currents between two capacitors. The transfer function can be obtained from Fig. 4*b* as

$$\frac{V_{C_1}}{V^*_{C_1}} = \frac{(K_{i1}/C)}{S^2 + \left(K_{p1}/C\right)S + \left(K_{i1}/C\right)}. \tag{15}$$

Then, the gain K_{p1} and K_{i1} are selected according to the natural frequency, ω_n, and the damping ratio, δ, as

$$K_{p_1} = 2 \cdot C \cdot \delta \cdot \omega_n \tag{16}$$

$$K_{i_1} = C \cdot \omega_n^2. \tag{17}$$

3 Simulation and experimental results

The proposed MPC and the multi-functional control strategy are verified both by simulations and experiments. The circuit specifications are listed in Table 4.

For simulations, the Power Electronics Simulator (PSIM) package has been utilised and for the experiment, the Texas Instruments' TMS320F28335 DSP board has been used.

3.1 Case 1: responses of step voltage commands

Fig. 5*a* presents a simulation result of a step voltage command response. In the first test, the 18 V dc input voltage is applied and V_1 ($=V_{C_1}$) and V_2 ($=V_{C_2}$) voltages are initially controlled at 18 V.

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Table 4 Circuit parameters

Parameters	Value
capacitances (C_1, C_2)	470 μF
impedance network inductances (L_1, L_2)	2 mH
energy storage side inductor (L_B)	2 mH
battery nominal voltage	12 V
switching frequency	10 kHz

The port 3 voltage (V_3) is then 36 V in this case ($V_{in} + V_1 = 36$ V) as shown in Fig. 5*a*. The energy storage (battery) port current is regulated at +1.8 A (positive sign indicates a charging current). In the middle of the waveform, a 24 V step voltage command (18–24 V) is given for ports 1 and 2 (boosting operation). In this case, the port 3 voltage will step change from 36 to 42 V. The corresponding voltage responses indicate that the proposed MPC and its control method can regulate output voltages (V_1–V_3) and the battery port charging current simultaneously with an acceptable overshoot.

Fig. 5*b* presents an experimental result under the same step voltage command as the simulation case. As shown, very similar responses are observed. The oscilloscope used for the experiment has four measurement channels and hence V_3, V_1, I_{L_1}, and I_{L_Bat} are selectively presented among six parameters shown in the simulation result. Fig. 5*c* presents an experimental result of a buck-mode operation. In this case, initial voltage command is 18 V (for V_1), and in the middle of the time, a step-down voltage (12 V) command is given. The output ports 1 and 2 voltages are operating under a buck mode (at 12 V) and the port 3 voltage is decreased to 30 V (18 + 12 V). The battery port current command is negative (−1.8 A) in this case to discharge the battery (discharging mode). The influence on the battery port's discharging current control is almost negligible from the step voltage command change.

As shown in Fig. 5, the output voltages and charging/discharging currents are regulated at their reference values with satisfactory dynamic responses.

3.2 Case 2: PWM switching signals in charging and discharging modes

As previously mentioned, the additional ON period of $S1$ and $S2$ switches for charging/discharging is based on (12) and (14) in the proposed control algorithm. For a charging case, the upper switch $S1$ has the additional ON period as presented in Fig. 6*a*. The V_1 and V_2 voltages are controlled at 24 V (boosting) and V_3 voltage is dc 42 V since the input voltage supplied is a constant dc 18 V. In this case, a charging current at 1.8 A is commanded to the energy storage port.

Fig. 6*b* presents PWM patterns for a discharging case. The energy storage port current command is −1.8 A which means a discharging current. In this case, the lower switch ($S2$) should be ON for a longer time based on (14).

3.3 Case 3: step voltage and step battery current responses

To verify the proposed multi-objective control, both a step voltage command and a step battery current command responses are presented in Fig. 6*c*. The V_1 and V_2 voltages are controlled at 18 V initially and a step voltage command of 24 V (boosting) is given.

After the voltage transient is over, a step charging current command (0–1.8 A) is given to observe the current response. As presented, an acceptable overshoot and a perturbation have been observed.

Fig. 6*d* presents a step-down (from a boost to a buck mode transition) operation. Initially, V_1 and V_2 are regulated at 24 V (boost mode) and then 12 V (buck mode) voltage command is given. As presented in Fig. 6*d*, the port voltages and energy storage port current are regulated at their commanded values with satisfactory transient responses.

3.4 Case 4: step load change response

In this case, the V_1 and V_2 voltages are initially regulated at 24 V. The input voltage is dc 18 V and hence output port 3 voltage stays at 42 V (18 + 24 V). Initially no load was connected to the output port 1. Then, a 15 Ω resistor load is connected to impose a step load change to the port 1 (I_{R1} is stepped up from 0 to 1.6 A).

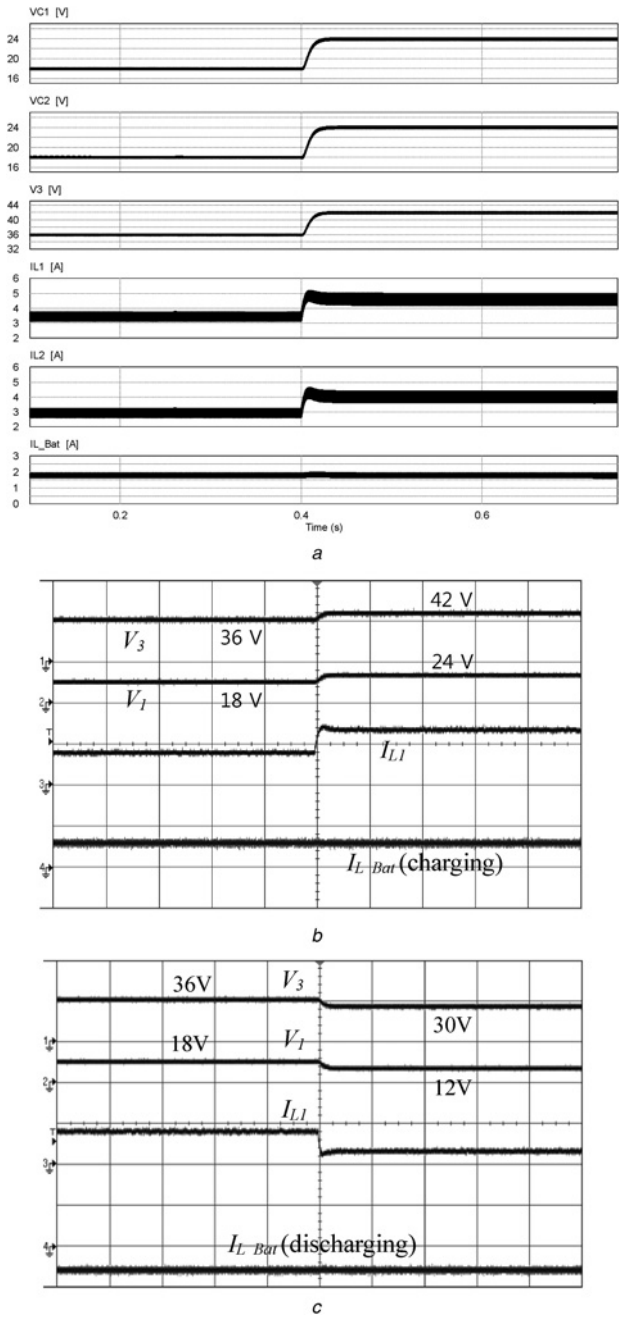

Fig. 5 *Step voltage responses*

a Simulation result: a step voltage command responses during a charging case. Top to bottom: 1. output port 1 ($V_1 = V_{C_1}$) voltage; 2. output port 2 ($V_2 = V_{C_2}$) voltage; 3. output port 3 (V_3) voltage; 4. inductor 1 current (I_{L_1}); 5. inductor 2 current (I_{L_2}); 6. energy storage port current (I_{L_Bat})

b Experimental result: a step voltage command response during a charging case. Top to bottom: 1. output port 3 (V_3) voltage, 36 V/div; 2. output port 1 (V_1) voltage, 36 V/div; 3. inductor 1 current (I_{L_1}), 4 A/div; 4. energy storage port current, 3 A/div (200 ms/div)

c Step-down voltage command response during a discharging case. Top to bottom: 1. output port 3 (V_3) voltage, 36 V/div; 2. output port 1 (V_1) voltage, 36 V/div; 3. inductor 1 current (I_{L_1}), 4 A/div; 4. energy storage port current, 3 A/div (200 ms/div)

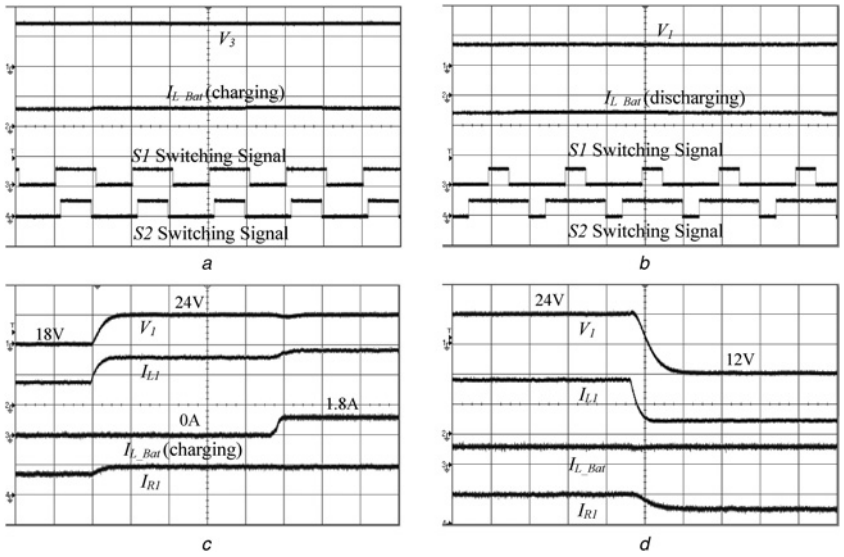

Fig. 6 *PWM patterns and step voltage and current responses for charging and discharging cases*

a Experimental result: PWM pattern during a charging case. Top to bottom: 1. port 3 voltage (V_3), 32 V/div; 2. energy storage (battery) current, 3 A/div; 3. *S*1 switch PWM signal, 5 V/div; 4. *S*2 switch PWM signal 5 V/div (50 μs/div)

b PWM pattern during a discharging case. Top to bottom: 1. port 1 voltage (V_1), 32 V/div; 2. energy storage (battery) current, 3 A/div; 3. *S*1 switch PWM signal, 5 V/div; 4. *S*2 switch PWM signal 5 V/div (50 μs/div)

c Experimental result: step voltage and battery current responses during a charging case (resistive loads are connected). Top to bottom: 1. output port 1 (V_1) voltage, 6 V/div (ground voltage: 18 V); 2. inductor 1 (I_{L_1}) current, 3 A/div; 3. energy storage port current (I_{L_Bat}), 3 A/div; 4. port 1 load current (25 Ω resistor is connected to the port 1), 1 A/div

d Experimental result: step-down voltage (boost to buck mode) response during a charging case (resistive loads are connected). Top to bottom: 1. output port 1 (V_1) voltage, 6 V/div (ground voltage: 18 V); 2. inductor 1 (I_{L_1}) current, 3 A/div; 3. energy storage port current (I_{L_Bat}), 3 A/div; 4. port 1 load current (25 Ω resistor is connected to the port 1), 1 A/div

After the first step change, a second step change is created (from 15 Ω loading to no load). As shown in Fig. 7*a*, subsequent to the load changes, voltage control for the port 1 is ensured and the voltage reaches its commanded value with a short settling time not disturbing the battery current (discharging in this case) control significantly.

3.5 Case 5: ac load test

In this case, two ac loads are connected to two output ports. Two permanent magnet synchronous motors are employed for this ac load test. Two same motors are rated at 24 V, 4.5 A, 4000 rpm. One motor is connected to the port 1 and the other motor is

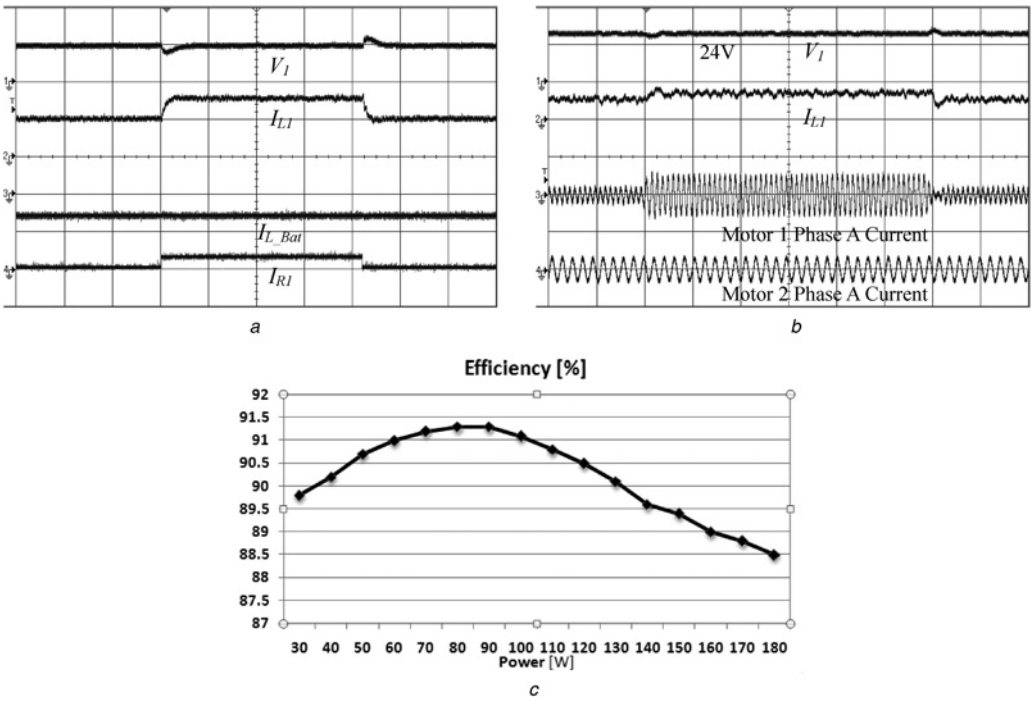

Fig. 7 *Responses of a step load change and an ac motor load test and a measured efficiency curve*

a Experimental result: step load change response for the port 1. Top to bottom: 1. output port 1 (V_1) voltage, 24 V/div; 2. inductor 1 (I_{L_1}) current, 4 A/div; 3. energy storage port current (I_{L_1}), 3 A/div; 4. port 1 load current (I_{R1}), 4 A/div

b Experimental result: response to ac motor loads running at different speeds (port 1: running at 2000 rpm, port 2: running at 1000 rpm). Top to bottom: 1. output port 1 (V_1) voltage, 18 V/div; 2. inductor 1 (I_{L_1}) current, 5 A/div; 3. motor 1 phase A current, 5 A/div; 4. motor 2 phase A current, 5 A/div, (140 ms/div)

c Measured efficiency curve

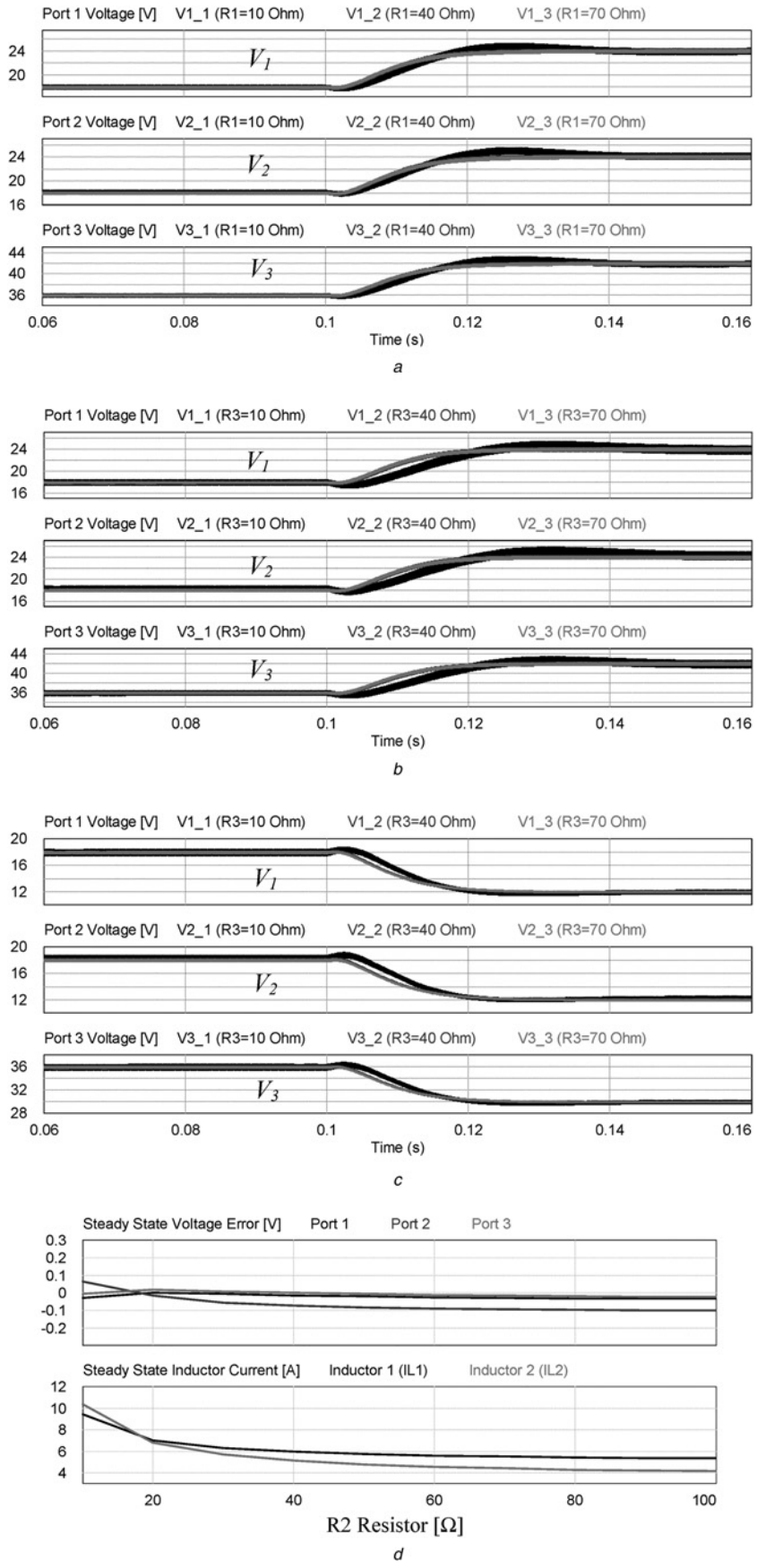

Fig. 8 *Performance analysis under unbalanced loads*

a Step voltage (boost mode) response comparison under unbalanced loadings (port 1 load resistor, $R1$, is changed from 10 to 70 Ω)
b Step voltage (boost mode) response comparison under unbalanced loadings (port 3 load resistor, $R3$, is changed from 10 to 70 Ω)
c Step-down (buck mode) voltage response comparison under unbalanced loadings (port 3 load resistor, $R3$, is changed from 10 to 70 Ω)
d Steady-state voltage errors from the commanded values (upper) and steady-state inductor current comparison (lower) according to the port 2 load ($R2$ resistor) change

connected to the port 2 through metal oxide semiconductor field effect transistor (MOSFET) inverters. The port 1 voltage is regulated at 24 V and the speed of the motor connected is regulated at 2000 rpm (as shown in Fig. 7*b*). The other motor is connected to the port 2.

This motor speed is controlled at 1000 rpm. Both motors are controlled using a standard field oriented control and each motor is coupled to a dc load motor. In this case, the port 3 where the voltage is 42 V (since the input dc voltage is 18 V) is connected to a resistive load (25 Ω).

A step motor load change is created by changing a resistor connected to the dc load motor side for the motor 1 while the motor 2 is running at a constant speed (1000 rpm) without a load change. Initially the motor 1 was running under 20% load and a step load change to 50% load was occurred first. Then, another load change from 50 to 20% load is created. The voltage controller can handle the load changes with acceptable perturbations and the two motors can be controlled independently at different loads and speeds. The two port voltages (V_1 and V_2) are well regulated (only V_1 voltage is displayed in Fig. 7*b*) with the sample ac loads as shown in Fig. 7*b*. The results of Figs. 5–7 verify the feasibility and effectiveness of the proposed structure and control at various operating points with various load conditions with satisfactory dynamic responses. Fig. 7*c* presents a measured efficiency curve of the MPC.

3.6 Performance analysis under unbalanced loads

As aforementioned, for the simplification, the proposed circuit was analysed and the controller was designed under the three assumptions made in Section 2. Since the circuit analysis and controller design have been performed assuming a balanced load, the performance analysis under unbalanced load conditions are indispensible.

The test conditions for the unbalanced loading are:

(i) Ports 2 and 3 load resistors are fixed at 30 and 50 Ω, and change port 1 load resistor from 10 to 70 Ω. Each port voltage responses are presented in Fig. 8*a* (for a step voltage command).
(ii) Ports 1 and 2 load resistors are fixed at 30 Ω, and change port 3 load resistor from 10 to 70 Ω. Each port voltage responses are presented in Fig. 8*b* (for a step voltage command) and Fig. 8*c* (for a step-down voltage command).

Fig. 8 illustrates each port voltage responses under three different unbalanced load conditions. As shown, the port voltages stay regulated at their desired values showing negligible differences in transients.

The upper graph of Fig. 8*d* presents each port voltage errors in a steady state from the commanded value (24 V for ports 1 and 2 and 42 V for port 3 in this test) under unbalanced loading ($R1$ and $R3$ are fixed at 30 Ω and $R2$ is varying). The horizontal axis is the varying $R2$ resistor value.

In addition, the lower graph of Fig. 8*d* indicates the steady-state values of inductors 1 (L_1) and 2 (L_2) currents under the unbalanced load conditions. The difference between inductors 1 and 2 currents is increasing when the load difference increases (between load 1 and load 2 resistors), which is an expected behaviour. The battery current stays well at its reference value in this test and hence it is not analysed here.

It should be noted that the voltage error of the port 2 (which has the biggest error in this case since the port 2 load is changing) is <0.5% from the commanded value at a full load which is negligibly small under the unbalanced loadings.

The results of Fig. 8 highlight the capability and effectiveness of the proposed MPC and its controller under various load conditions.

4 Conclusions

In this paper, a MPC including a bi-directional energy storage port was introduced. In the proposed structure, only one single-leg active switching element has been used to decrease the system cost. A capacitor (in an impedance network) voltage was directly controlled while managing the energy storage charging/discharging operation to provide two buck–boost output voltages (ports 1 and 2) and one boost (port 3) output voltage. Due to the multi-objective nature of the proposed converter, a multi-functional controller was designed and implemented in the MPC. The balanced voltage control of ports 1 and 2 under various unbalanced loading conditions was confirmed based on the proposed control strategy. Since no dead time is required for the single-leg switches in the MPC, more reliable converter operation is possible. Simulation and experimental results under various load conditions verified the capability and effectiveness of the proposed MPC and the corresponding control structure.

5 Acknowledgment

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