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REVIEW

Comprehensive review of nonisolated bridgeless power factor converter topologies

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Abstract

The intention of this study is to provide a critical review of single-phase nonisolated bridgeless power factor converter topologies, which will be useful for novice researchers in the power electronics field. The bridgeless nature of the converter reduces the number of switching devices in the current path and achieves higher efficiency. Nonisolated topologies are considered in this review due to the inherent advantages they offer such as lower cost, weight and size and higher efficiency, which are desirable for systems such as on-board electric vehicle battery chargers, direct current power supplies and variable speed drives. These topologies are derived from conventional boost, buck and buck/boost converters. Moreover, the topologies can be operated in continuous or discontinuous conduction modes subject to their applications. Each topology is described in terms of its advantages and limitations. In addition, a comparative study is conducted for each group (boost, buck and buck/boost).

1 | INTRODUCTION

Single-phase alternating current (AC) to direct current (DC) converters with a power factor correction (PFC) stage are most commonly used for power conversion systems and can be applied in many residential and industrial applications such as power supplies for consumer electronics, electric vehicle charging and variable speed drives. To maintain rigorous grid regulation, for example., international electrotechnical commission (IEC)-61000-3-2 harmonic limits, sinusoidal current regulation and a high power factor (PF) converter are required for the aforementioned applications. Single-phase PFC converters are very prevalent components for achieving the IEC harmonic regulation and current regulation limits [1]. Therefore, in the existing literature, various types of single-phase PFC converters have been presented that are essentially derived from conventional boost and buck/boost converters, although boost PFC converters are widely used in many applications due to their simplicity, cost effectiveness, and high performance in terms of efficiency and high PF. With the boost PFC converters, the inherent limitation is that output voltage is always higher than the peak AC supply voltage [2–8]. On other hand, in buck derivative PFC converters, the output voltage is always lower than the peak AC input voltage. When a wide range of output voltage is desired, for example, for plug-in electric vehicles' (PEVs) battery charging, where the battery sets at variable voltage levels in the range between 50 V and 700 V in order to satisfy the different vehicles and battery types [9], while conventional buck/boost converters and their derived forms are employed [10–14] for such applications.

However, the above-mentioned topologies whether boost, buck or buck/boost based, have a bridge rectifier at the input stage, which is responsible for a considerable portion of the conduction losses in the converter. To mitigate the conduction loss in the bridge rectifier, many bridgeless variants of boost, buck and buck/boost converters have been given in [15–29]. The bridgeless approach decreases the number of devices in the current path, which results in a reduction of the losses and achieves higher efficiency at lower line voltages [15]. To further improve the efficiency in bridgeless converters, they are operated in discontinuous conduction mode (DCM) of operation. The DCM operation provides zero-current turn-on of the switches and zero-current turn-off of the diodes, which reduce the switching losses during the turn-on and turn-off times of the switches and diodes, respectively. Moreover, some bridgeless topologies utilise resonant components to achieve soft switching in the continuous conduction mode (CCM) of

operation and those topologies are used in high power applications with high efficiency.

As has been discussed in the literature, there is a consistent demand for high-efficiency, high-PF, small-sized and lightweight single-phase PFC converters for various power applications. Some of these demands are met by conventional diode bridge-based single-phase PFC converters using buck, boost or buck-boost converters. Isolated PFC converters using bridge rectifiers pose serious concerns for efficiency. The bridgeless nature of the converter reduces the number of switching devices in the current path and achieves higher efficiency. Moreover, the nonisolated nature of the converter further assists in raising the efficiency and lowering the weight of the converter system, which are desirable for systems such as onboard electric vehicle battery chargers, DC power supplies and variable speed drives. The goal is to provide a critical review, based on various parameters, of single-phase nonisolated bridgeless PFC topologies, which will be useful for novice researchers in the power electronics field.

The rest of the article is organised as follows: Section 2 gives a review of bridgeless boost PFC topologies and a comparative analysis among them. Section 3 is a review of bridgeless variants of buck PFC topologies and a comparison among them. In Section 4, buck/boost-based bridgeless topologies are reviewed. Finally, conclusions drawn from this review study are given in Section 5.

2 | BRIDGELESS BOOST AND ITS DERIVED TOPOLOGIES

In this section, boost and its derived version of bridgeless PFC topologies is reviewed and a comparison among the topologies is tabulated in Tables 1 and 2.

2.1 | Classical bridgeless boost PFC converter

The bridgeless boost PFC converter shown in Figure 1 is an attractive solution for power levels greater than 1 kW where power density and efficiency (reduction in gate driver loss) are especially critical parameters. In this topology, both switches are turned-ON using a single driver circuit; thus, the gating signal of the switches is identical, as shown in Figure 1(b). Therefore, power density (elimination of an additional gate driver circuit) and efficiency of the converter improve in comparison with those bridgeless boost PFC converters where separate driver circuits are used. Also, this topology avoids the heat management problem of diode bridge rectifiers while it does introduce electromagnetic interference (EMI) problems [30]. Moreover, in this topology, the input line is floating with respect to the PFC ground; therefore, it is not possible to sense the input voltage without a low frequency transformer or an optical-coupler.

TABLE 1 Comparison of bridgeless boost PFC converters

Topology	Input current ripple	EMI/noise	Magnetic size	Efficiency	Cost
Figure 1(a)	High	High	Large	Poor	Low
Figure 2(a)	High	Fair	Large	Fair	Low
Figure 3(a)	High	Fair	Large	Poor	Medium
Figure 3(b)	High	High	Large	High	Low
Figure 4	Low	Low	Small	High	High
Figure 5	Low	Fair	Medium	Fair	Medium
Figure 6(a)	High	High	Large	High	Medium
Figure 6(b)	High	High	Large	High	Medium

TABLE 2 Comparison of component count in bridgeless boost PFC converters

Topology	Switches	Diodes	Capacitors	Inductors	On-path devices	Off-path switches
Figure 1(a)	2	2	1	2	1S+1D	2D
Figure 2(a)	2	2	1	2	1S+1D	2D
Figure 3(a)	2	4	1	2	1S+1D	2D
Figure 3(b)	2	2	1	1	1S+1D	2D
Figure 4	4	4	1	4	2S+2D or 1S+1D	2D
Figure 5	2	4	1	3 (Coupled)	1S+1D	2D
Figure 6(a)	3	4	3	2	1S+1D	2D
Figure 6(b)	2	6	3	3	1S+1D	2D

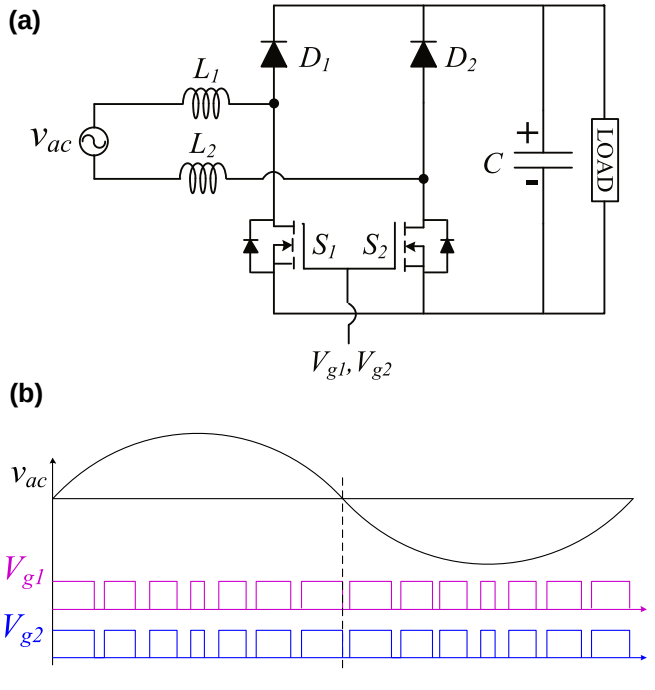

FIGURE 1 (a) Classical bridgeless boost PFC converter and (b) gating signals of switches

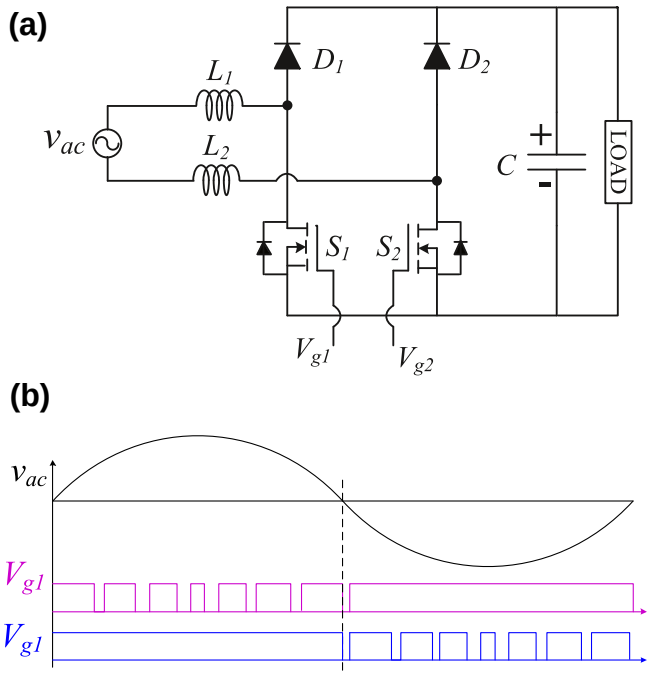

FIGURE 2 (a) Phase shifted bridgeless boost PFC converter and (b) gating signals of switches

Because of current does not share the same path during each half cycle of input voltage, complex circuitry is needed to sense the input current.

For further improvement in the bridgeless converter shown in Figure 1(a), a phase shifted bridgeless PFC converter,

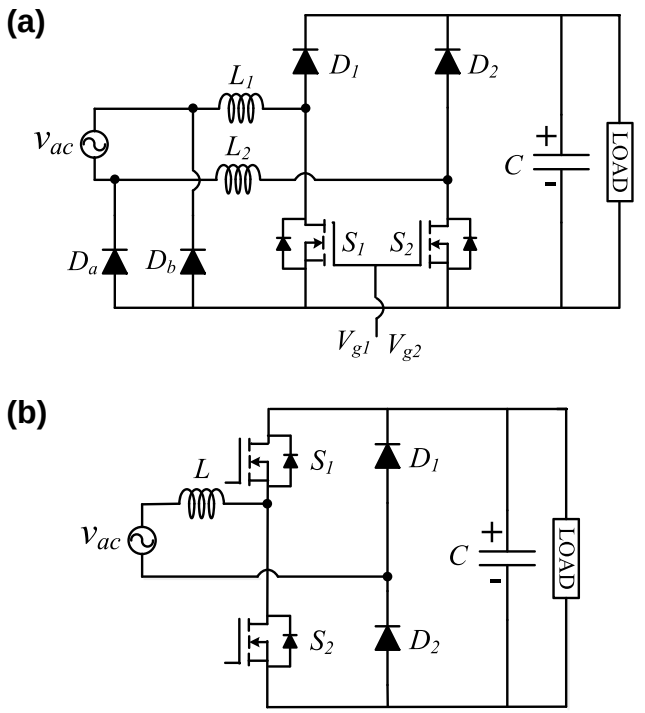

FIGURE 3 (a) Semibridgeless or dual boost PFC converter and (b) totem-pole bridgeless PFC converter

which is also known as a dual-boost PFC converter [26] is introduced, as shown in Figure 2(a). In this topology, the gates of the MOSFET switches are decoupled and one of the switches remains ON during each half cycle of the input supply. Figure 2(b) shows the gating scheme of the switches. This topology reduces the gate conduction loss and at light load conditions, the conduction loss can be reduced until the voltage drop across the MOSFET body diode becomes equal to the voltage drop across the MOSFET channel r_{ds}(on), since beyond this point, additional current flows through the body diode. The light load efficiency improvement is achieved at the expense of additional driver circuits.

2.2 | Semibridgeless converter

The semibridgeless configuration is derived from conventional bridgeless topology (Figure 1(a)) by adding two additional slow diodes, namely: D_a and D_b, as shown in Figure 3(a). These additional slow diodes connect the input to the ground of the PFC and solve the EMI-related problems. The associated conduction loss in these two diodes is low because current does not always return through them. This is due to low inductor impedance at line frequency; therefore, a large portion of the current flows through the body diodes of the MOSFET. With this topology, it is possible to sense the input voltage through a string of voltage dividers. In this topology, the two boost converters will work alternatively during the positive and negative half cycles of the input supply. The low utilisation of the inductors and devices reduces the power density and

increases the cost of the converter compared to the conventional boost PFC.

The totem-pole bridgeless PFC, as shown in Figure 3(b), has only one switch and one low frequency diode conducting at any time. Thus, it has the lowest conduction loss compared with the conventional boost PFC and the semibridgeless dual-boost PFC. Therefore, the totem-pole bridgeless converter achieves higher efficiency and power density compared to aforementioned converters. In the totem-pole PFC topology, the body-diode of S_1 or S_2 provides the freewheeling path for the inductor current. The recovery speed of body diode in the MOSFET is so slow that it makes S_1 and S_2 conduct at the same time leading to the destruction of the circuits. Therefore, a MOSFET with fast recovery speed should be used in the totem-pole topology.

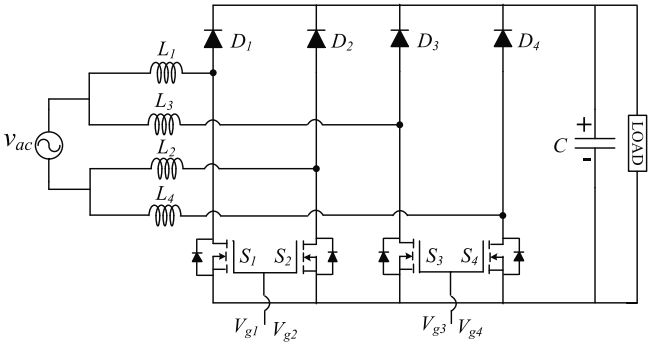

FIGURE 4 Bridgeless interleaved boost PFC converter

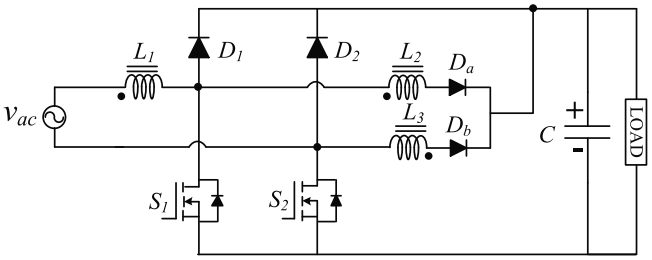

FIGURE 5 Ripple free bridgeless boost PFC converter

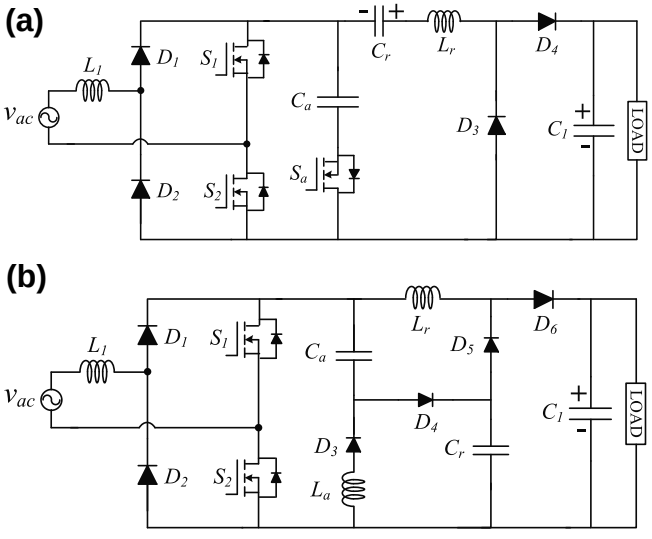

FIGURE 6 (a) Hybrid resonant PWM bridgeless boost PFC converter and (b) soft switching based bridgeless boost PFC converter

2.3 | Bridgeless interleaved converter

The bridgeless interleaved (BLIL) converter has the same number of semiconductor devices as in a conventional interleaved boost (ILB) PFC converter [5]. In comparison to the ILB converter, the BLIL converter has two additional MOSFETs and two fast diodes in place of four slow diodes. From the operational point of view of the converter, the gating signal of switches S_1 and S_2 is 180° out of phase with switches S_3 and S_4; similar to the conventional ILB converter.

The peak efficiency of the BLIL is reported as 98.5% at 1.2 kW load and 70 kHz switch frequency [16]. The efficiency improvement at high power load (above 3 kW) is the major contribution of this topology. Moreover, due to the interleaving structure, current stress in switches is low and hence the reliability and fault tolerance of the converter are improved compared to other bridgeless converters. However, the significant drawback of this topology is its higher cost due to the increased number of magnetic components.

2.4 | Bridgeless converter with low conduction losses and reduced diode reverse recovery problems

The output diodes in the converters shown in Figures 1(a), 2(a) and 3 have the severe problem of high reverse recovery losses due to high diode forward current and high voltage. As the switching frequency increases, the large reverse recovery currents of the output diodes affect the switches in the form of additional turn-on losses and also produce EMI noises. To overcome these issues, various active and passive snubber approaches have been proposed for the bridgeless boost rectifier [31–35]. These topologies either have higher conduction losses due to a large amount of circulating current flowing through the auxiliary circuit and high stress on switching devices or require an isolated transformer to sense the AC input voltage and a Hall effect sensor to detect the input current, which limits the use of this topology in practical designs. The bridgeless boost PFC converter proposed in [15] reduces the conduction and diode reverse recovery losses without sensing the input voltage, as shown in Figure 5. With this topology, zero-current turn-off of the output diodes is achieved, and the reverse recovery currents of the additional diodes are slowed down to reduce the diode reverse recovery losses. The inductive components are wound on a single core by using the leakage inductance of the coupled inductor. This converter has an efficiency improvement at low line input voltage, for

TABLE 3 Comparison of component count in bridgeless buck PFC converters

Topology	Switches	Diodes	Capacitors	Inductors	On-path switches	Off-path switches
Figure 7(a)	2	3	3	2	1S+1D	1D
Figure 7(b)	1	3	3	2	1S+1D	1D
Figure 8	2	4	2	2	1S+1D	1D
Figure 9(a)	2	4	2	1	1S+1D	1D
Figure 9(b)	2	4	2	2 (coupled)	1S+1D	1D
Figure 9(c)	2	4	2	2	1S+2D	1D
Figure 9(d)	2	4	2	2	1S+1D	1D

TABLE 4 Voltage conversion ratio of bridgeless buck converter in CCM

Topology	$M = V_0/v_{ac}$
Figure 7(a) and (b)	D
Figures 8, 9(a)–(c)	2D
Figure 9(d)	$\frac{2D}{1+(1-D)^2}$

example, at 90 V, 300 W load and 100 kHz switching frequency it achieves a measured efficiency of 95.5%.

2.5 | Soft switching based bridgeless boost PFC converter

In [19], a soft switching based bridgeless boost PFC converter has been proposed for power supply and battery charging applications, as shown in Figure 6(a), which operates in CCM and achieves zero-voltage switching for all switches. The converter operates in both pulse width modulation (PWM) and resonant modes in each switching cycle. When switches S_1 and S_2 are turned-on converter operates in resonant mode, utilising capacitor C_r and inductor L_r and PWM mode when switches S_1 and S_2 are turned-off and auxiliary switch S_a is in ON mode. Thus, its switching operation is known as the hybrid resonant PWM. Moreover, the converter also reduces the turn-off losses of the PWM operating switches. The PWM switches of the converter are gated with the same PWM signal which simplifies the control design. Furthermore, the converter exhibits an approximately 1% efficiency improvement as well as lower device temperature rise at full load compared to a conventional hard switched boost PFC converter. The PWM switching frequency is selected as 150 kHz for experimentation.

In [20], a new bridgeless boost PFC based on a passive soft switching method was proposed for high power applications as shown in Figure 6(b). In this method, an extra auxiliary switch or additional control circuitry to realise soft switching has been eliminated. In fact a few passive components are employed in the converter. The driving signals of the two switches are in phase hence only one drive signal is needed. Therefore, the configuration is simple and easy to implement which yields a low cost solution for high power applications. All the power switches and diodes (S_1, S_2, D_4, D_5 and D_6) operate under a soft switching condition. The S_1 and S_2 switches operate with zero-current and zero-voltage turn-on and zero-voltage turn-off, and D_4, D_5 and D_6 operate with zero-voltage turn-on and turn-off.

2.6 | Comparative study of bridgeless boost PFC topologies

A comparative study of the bridgeless boost PFC topologies is conducted in terms of input current ripple, EMI/noise, magnetic size, efficiency and cost as presented in Table 1 using [16]. A qualitative comparison among the topologies has been done for the aforementioned parameters. The terms "high", "low", "small", etc. are used to only describe comparisons among the topologies and not in an absolute sense. Table 2 using [36] shows the number of active and passive components as well as the on-path and off-path devices for each topology.

3 | BRIDGELESS BUCK PFC CONVERTERS

In this section, buck-type derivative bridgeless converters for PFC applications are reviewed. A comparative study among the topologies in terms of voltage conversion ratios and component counts is presented in Tables 4 and 5, respectively.

3.1 | A discontinuous capacitor voltage mode operated bridgeless buck PFC converter

In [22], a bridgeless buck PFC converter operating in discontinuous capacitor voltage mode (DCVM) was presented. Compared to conventional full bridge buck DCVM PFC converters, the bridgeless buck PFC converter decreases the number of semiconductor devices in the current path. Therefore, the conduction losses and thermal stress on the semiconductor devices are reduced and converter efficiency gets improved as a result. Unlike the boost PFC converter, the proposed converter has the same advantages as the conventional full bridge buck DCVM converters such as: inherent inrush current protection during start-up conditions, lower

Topology	Switches	Diodes	Capacitors	Inductors	On-path switches	Off-path switches
Figure 10	3	4	3	1	2S+1D	2D
Figure 11(a)	2	3	3	3	1S+1D	2D
Figure 11(b)	2	3	3	3	1S+1D	2D
Figure 11(c)	2	2	3	3 (coupled)	1S+1D	2D
Figure 11(d)	2	2	4	3	1S+1D	1D
Figure 12	2	5	4	3	1S+1D	2D
Figure 13	2	3	2	2	1S+1D	2D
Figure 14(a)	2	3	2	3	1S+1D	2D
Figure 15	5	1	2	1	2S	1S+1D

TABLE 5 Comparison of component count in bridgeless buck/boost PFC converters

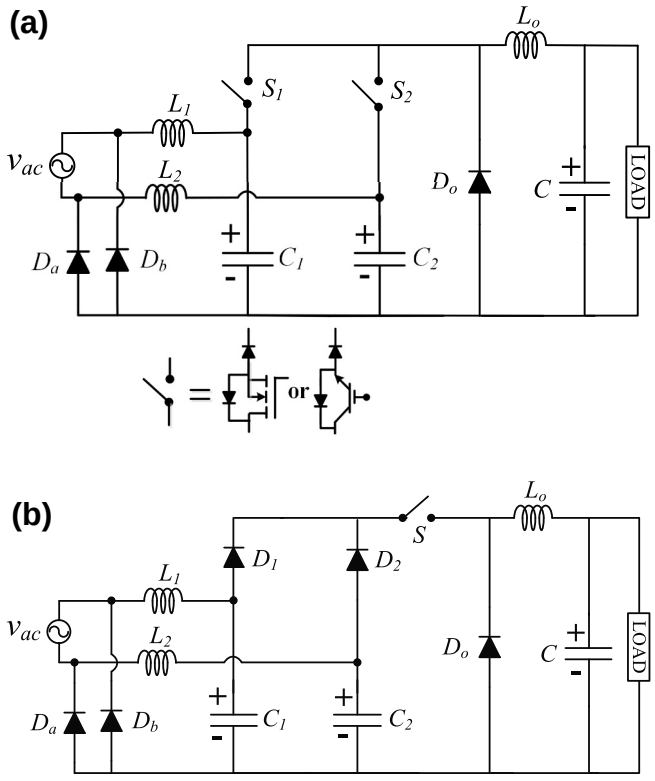

FIGURE 7 (a) Bridgeless buck PFC converter with discontinuous capacitor voltage mode using two switches and (b) bridgeless buck PFC converter with discontinuous capacitor Voltage mode (DCVM) using single switch

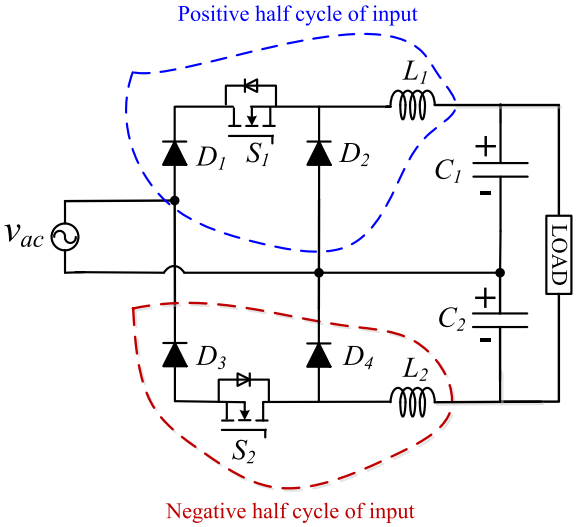

FIGURE 8 Bridgeless buck PFC converter with voltage doubler output using two inductors

input current ripple, fewer reverse recovery problems and low EMI noise. The major limitation of DCVM operation is the high switch voltage stress which increases in accordance with the load current; therefore, the converter is suitable for low power applications (<300 W).

Figure 7(a) and (b) shows two bridgeless DCVM buck PFC converters. The first topology in Figure 7(a), which uses two switches, S_1 and S_2, driven by the same PWM signal, simplifies the control circuit. It is noted that the two switches S_1 and S_2 are unidirectional switches (current flows in only one direction) and hence a diode is added in series with the switch. On the other hand, the second topology uses a single switch, as shown in Figure 7(b). Compared to the conventional full bridge DCVM PFC converters [37, 38] the proposed bridgeless converter utilises one additional capacitor and inductor, which is a disadvantage in terms of cost and size. However, two inductors have better thermal performance compared to a single inductor.

3.2 | Bridgeless converter with voltage doubler output and nonlinear output

In [23], voltage doubler and nonlinear output based bridgeless buck topologies were proposed. The first version of these configurations, which utilise two back-to-back buck converters, is shown in Figure 8; one unit of it operates in the positive half cycle of input and second unit operates in the negative half cycle of the input as indicated by the *dotted lines* in Figure 8. During converter's operation, the voltage across capacitors C_1 and C_2, i.e., V_1 and V_2 must be selected lower than the peak of

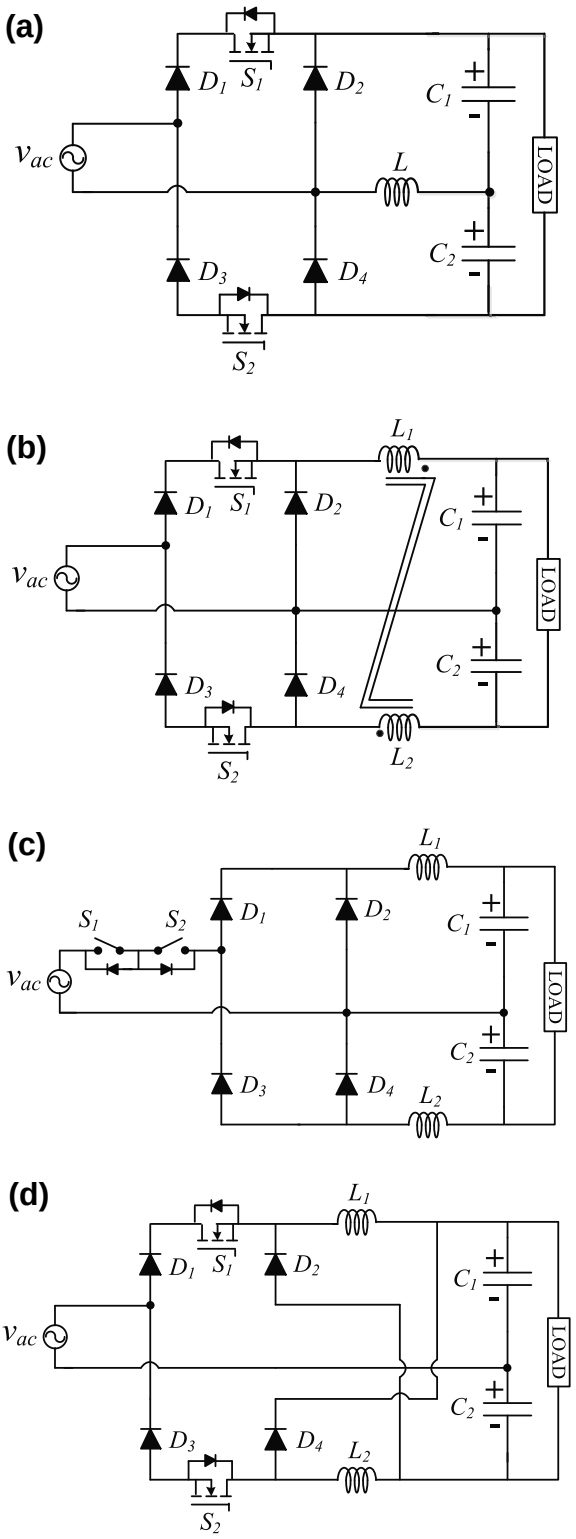

FIGURE 9 (a) Bridgeless buck PFC converter with voltage doubler output using two inductors, (b) bridgeless buck PFC converter with voltage doubler output using coupled inductors, (c) bridgeless buck PFC converter with voltage doubler output using two inductors and two bidirectional switches and (d) bridgeless buck PFC converter with nonlinear output using two inductors

input voltage, v_{acpeak}. The voltage output across load is V_0 which is sum of the voltages V_1 and V_2, and is given by:

$$V_0 = 2D|v_{ac}| \tag{1}$$

where D is the duty cycle and $|v_{ac}|$ is the instantaneous rectified AC input voltage. The relationship shown in Equation (1) is valid for input voltage $v_{ac} > V_0/2$. When v_{ac} falls below $V_0/2$, the energy cannot be delivered to the load and hence the load current is maintained by capacitors C_1 and C_2. The major advantage of this converter is that the low-line efficiency of the converter can be improved for 0–300 V output voltage range. Another important feature of this topology is the low common mode noise problem. With reference to Figure 8, the return path of the input source and the midpoint of C_1 and C_2 are connected to each other. Therefore, there is no high dV/dt problem between the input and output terminals and as result the converter can operate with low common-mode noise.

Furthermore, four topologies are derived from Figure 8 as shown in Figure 9. The inductors L_1 and L_2 in the Figure 8 are replaced by single inductor L shown in Figure 9(a). Since this topology uses only one inductor, magnetic component utilisation is better compared to the two inductor topologies. However, this topology has a high common mode noise problem because voltage developed across the inductor, L induces the high dV/dt between the input and output terminals.

Another topology presented in Figure 9(b) has the same common-mode noise as the topology shown in Figure 8. Moreover, the topology shown in Figure 9(b) reduces the number of magnetic components by coupling the inductor L_1 and L_2 of the Figure 8. Because windings of L_1 and L_2 utilise the same core as a result the utilisation of core increases. However, to accommodate both windings on a single core, it may require a customised core with a large window area since commercially available toroidal-type cores are typically designed to accommodate only a single winding.

A topology shown in Figure 9(c) is obtained by moving switches S_1 and S_2 in the Figure 8 to the AC side. For implementation of this topology, two bidirectional current carrying switches are employed in series with an AC source. The driving circuit of these two switches is simple because the source terminals of S_1 and S_2 are connected together. Another variation of the bridgeless converter (Figure 8) is shown in Figure 9(d). In this configuration (Figure 9(d)), the circuit exhibits a nonlinear gain which is given as:

$$V_0 = \frac{2D}{1 + (1 - D)^2}|v_{ac}| \tag{2}$$

According to Equation (2), if a duty cycle D is near unity, then Equation (2) is converted into Equation (1). However, if a duty cycle D is near zero, that is, a case when output voltage V_0

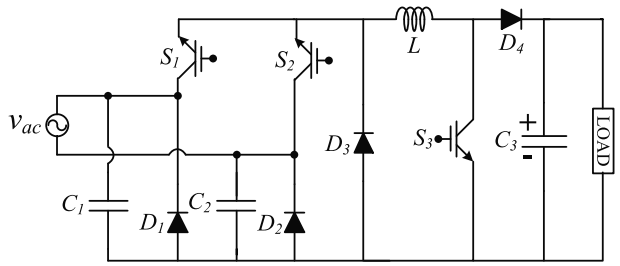

FIGURE 10 Bridgeless buck/boost PFC derived from the cascaded buck/boost converter

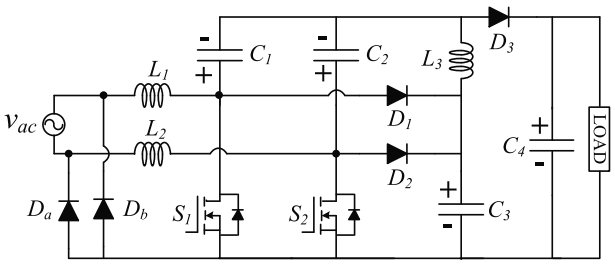

FIGURE 12 Bridgeless SEPIC PFC converter with extended gain

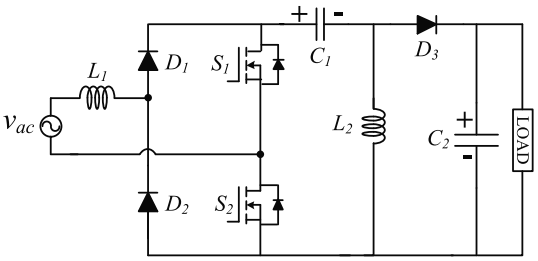

FIGURE 13 Bridgeless SEPIC PFC converter with reduced components

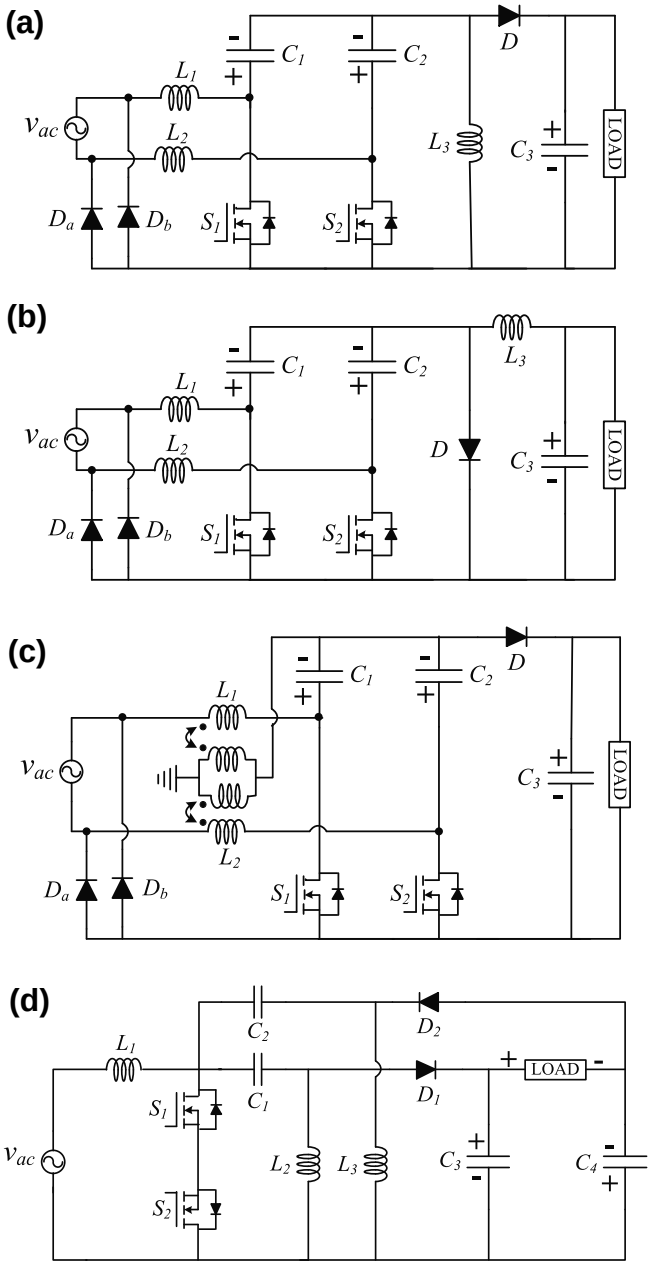

FIGURE 11 (a) Bridgeless SEPIC PFC converter, (b) bridgeless CuK PFC converter, (c) coupled inductors based bridgeless SEPIC PFC converter and (d) a modified bridgeless SEPIC PFC converter

is much lower than input voltage v_{ac}, then input-output gain becomes as Equation (3),

$$V_0 = D|v_{ac}| \tag{3}$$

which is similar to the conventional buck converter.

Table 3 summarises the part counts and the number of semiconductor devices in the current path for switch-on and off conditions. Table 4 shows the voltage conversion ratio for each topology.

4 | BRIDGELESS BUCK/BOOST PFC CONVERTERS

In this section, bridgeless buck/boost PFC topologies are reviewed. These topologies are derived using noninverting buck/boost, SEPIC, CuK and inverting buck/boost converters.

4.1 | Cascaded buck/boost derivative bridgeless PFC converter

The bridgeless buck/boost PFC converter shown in Figure 10 has been derived from the conventional cascaded buck/boost converter [17]. The important features of this converter are the low voltage and current stresses on the components. Therefore, this bridgeless converter can be used for higher power applications compared to other buck/boost derivative bridgeless converters (SEPIC, ZETA, CuK, etc.). During the positive half cycle of input voltage when the AC input voltage (v_{ac}) is lower than the output load voltage (V_0), the converter operates in the boost mode. The switch S_1 is continuously turned-on and S_3 is

gated through the PWM and then operation of the converter is exactly the same as the operation of a conventional boost converter. When the AC input voltage is higher than the output voltage, the converter operates in the buck mode and when the switch S_1 is turned-on, the capacitor C_1 discharges and the input voltage supplies power to the inductor and load. Moreover, when the switch S_1 is turned-off, the diode D_3 conducts and the inductor releases its stored energy to the load. The capacitor C_1 is charged through the input voltage. The operation of the converter in the negative half cycle of the input supply is described similarly to the operation in the positive half cycle.

4.2 | Bridgeless SEPIC and CuK PFC rectifiers with low conduction loss

In [18], the authors have presented SEPIC and CuK based bridgeless converters as shown in Figure 11(a) and (b), respectively, which is operated in DCM. During a switching cycle only two semiconductor devices are in the current path, which results in lower conduction losses and improves the thermal management problem. DCM operation brings the additional advantages of zero-current turn-on of the switches and zero-current turn-off of the output diode D. In addition, the DCM operation reduces the complexity of the control design. However, when a converter operates in DCM, the current stress on the components becomes relatively higher compared to CCM operation and hence DCM operating converter is suitable for low-power applications (<300 W). With this topology, the problem of common-mode EMI noise is reduced because of the two additional slow diodes (D_a and D_b) and the connection of the output ground to the AC main.

The voltage waveforms of the inductors in the converter shown in Figure 11(a) and (b) are identical, and hence they can magnetically be coupled on a single core which significantly reduces the overall size of the converter because the inductor is the heaviest component over any other components in a converter [6]. Figure 11(c) depicts the circuit arrangement of bridgeless SEPIC with coupled inductors. The voltage conversion ratio M, i.e., V_0/v_{ac} of the circuit shown in Figure 11 in the DCM operation is expressed as:

$$M = \sqrt{\frac{R_L}{2R_e}} \tag{4}$$

where R_L is the load resistance and R_e is given as:

$$R_e = \frac{2L_e}{D_1^2 T_s} \tag{5}$$

where

$$L_e = \frac{L_2L_3 + L_1L_3 + L_1L_2}{L_1L_2L_3} \tag{6}$$

and D_1 is duty cycle of the switches.

Another version of the bridgeless SEPIC PFC converter, which has advantages of reduced switch voltage stress and low EMI noise compared to the conventional SEPIC converter, is shown in Figure 11(d).

4.3 | A modified bridgeless SEPIC PFC converter with extended gain

In [24], the authors proposed a bridgeless SEPIC rectifier (Figure 12) with a voltage multiplier cell which is derived from the modified SEPIC converter in [39]. The bridgeless structure reduces the conduction losses, and multiplier cells (D_1, C_3) and (D_2, C_3) increase the gain and reduce the stress on the switches. However, the increase of voltage gain leads to efficiency improvement at the lower side of grid voltage; therefore, requirements for thermal management are drastically reduced compared to their conventional counterparts [18]. However, the common mode EMI generation of this topology is similar to the converter in [18]. Furthermore, to achieve low input current ripples all three inductors can be coupled on a single magnetic core. Therefore, the requirement for input filtering is minimised.

The voltage conversion ratio M in CCM operation is defined as:

$$M = \frac{V_0}{v_{ac}} = \frac{1-D}{1+D} \tag{7}$$

where D is the duty cycle.

The voltage conversion ratio in DCM operation is given as:

$$M = \frac{V_0}{v_{ac}} = \frac{D_1^2\alpha}{K} \tag{8}$$

where D_1 is duty cycle of the switches, and α and K are expressed as:

$$\alpha = -\frac{2}{\pi} - M + \frac{2M^2}{\pi\sqrt{M^2-1}}\left[\frac{\pi}{2} + \tan^{-1}\left(\frac{1}{\sqrt{M^2-1}}\right)\right] \tag{9}$$

$$K = \frac{2L_e}{T_s R_L} \tag{10}$$

where L_e is given the same as Equation (6).

4.4 | Bridgeless SEPIC PFC converter with reduced components and conduction losses

A bridgeless SEPIC PFC converter (Figure 13) in [25] has lower conduction losses and a reduced number of components compared to the other existing bridgeless SEPIC converters. This topology is designed to operate in DCM, where the switches operate as zero-current turn-on and the output diode operates as zero-current turn-off. In addition, in DCM

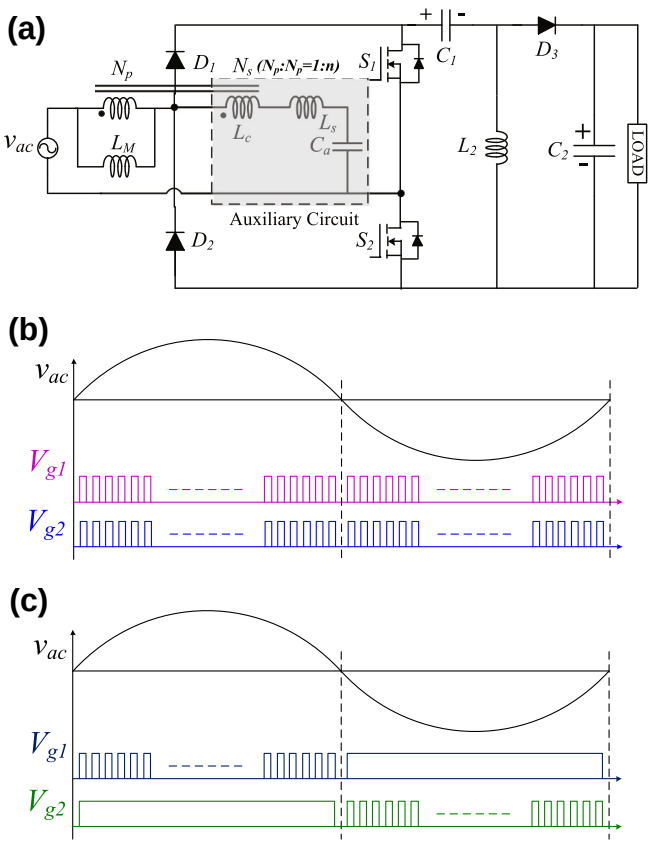

FIGURE 14 (a) Bridgeless SEPIC converter with a ripple-free input current, (b) conventional gating signals for switches in bridgeless SEPIC converter and (c) the gating signals used for bridgeless SEPIC converter of Figure 14(a)

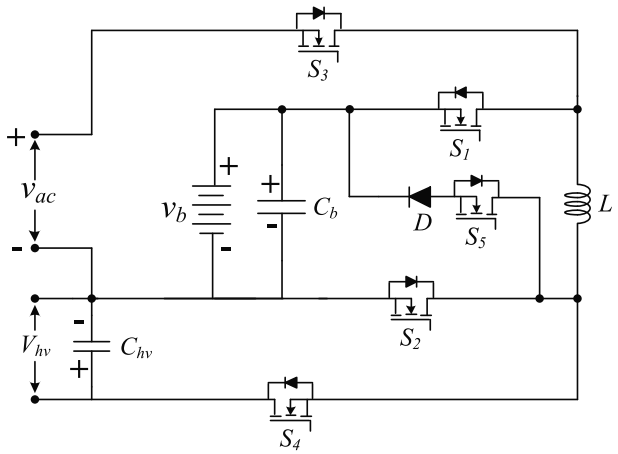

FIGURE 15 A bridgeless-based integrated converter for PEVs

operation the control circuit requires only a voltage loop for PFC; hence the controller design becomes simpler and easy to implement in the processor. Furthermore, the measured efficiency of this topology has a 1% improvement over a conventional SEPIC PFC converter. Moreover, this topology can be operated in CCM for higher power applications such as on-board EV charging systems. In an on-board charging system, a compact size converter is desirable due to space and weight constraint. In addition to this, a wide variation of battery voltage is reached during charging; therefore, buck-boost capability of the PFC converter is mandatory, which is easily met by the SEPIC converter.

TABLE 6 Voltage conversion ratio of the bridgeless buck/boost converter in CCM

Topology	$M = V_0/v_{ac}$
Figures 10, 11(a), (c), (d), 13 and 14(a)	$\frac{D}{1-D}$
Figure 11(b)	$-\frac{D}{1-D}$
Figure 12	$\frac{1+D}{1-D}$
Figure 15	$\frac{1}{1-D}$ and $-\frac{D}{1-D}$

4.5 | Bridgeless SEPIC converter with a ripple-free input current

The bridgeless SEPIC PFC converter shown in Figure 13 has a reduced number of components and gains higher efficiency due to the absence of the diode bridge rectifier. However, a large input inductance is used in order to reduce the input current ripples. In addition, conduction loss occurs in the body diode of the switches due to the use of a single PWM gate signal for both switches (S_1 and S_2).

In order to overcome the above-mentioned problems, a new bridgeless SEPIC PFC converter with a ripple free input current has been proposed in [26], as shown in Figure 14(a). An auxiliary circuit (*shaded area* in Figure 14(a)) consisting of a small inductor, a capacitor and an additional winding of input inductor is used to reduce the input current ripple. Usually, coupled inductors techniques are used to mitigate the current ripple [40–42]. Figure 14(c) shows PWM gating of switches S_1 and S_2. For a half cycle of the input supply, one switch is continuously turned-on and current is forced to flow through the channel of the switch rather than through the intrinsic body diode. As a result, conduction loss of switch is reduced and efficiency improves.

4.6 | A bridgeless integrated PFC converter for automotive applications

The authors in [29] proposed a bridgeless integrated PFC converter for PEVs application as shown in Figure 15. In plug-in charging mode, the converter operates in boost as well as buck/boost mode. During the positive half cycle of the input voltage, the converter operates in the boost mode and in the negative half cycle of the input voltage, it operates as an inverting buck/boost converter. Moreover, in either boost or buck/boost mode, two semiconductor devices are in the current path similar to other bridgeless converters. Therefore, efficiency of the converter will be similar to that of the other

existing bridgeless converters. Apart from plug-in charging mode, this converter works in other modes of vehicles, that is, propulsion and regenerative braking.

The comparative study of bridgeless buck/boost converters has been conducted based on the number of components and the number of semiconductor devices that come in the current path during switch-on and switch-off conditions shown in Table 5. The voltage conversion ratio of each topology has been shown in Table 6.

5 | CONCLUSIONS

In this study, a family of single-phase nonisolated bridgeless boost, buck and buck/boost PFC converters has been reviewed along with their relative merits and drawbacks. These topologies are operated in either CCM or DCM. CCM operation of the converter is used for high power applications, for example, electric vehicle charging, DC drive systems, etc. CCM operation with soft switching methods can be used for high power applications with higher efficiency. On the other hand, DCM operation is used for low power applications and high efficiency requirements. In some bridgeless topologies, coupled inductors are utilised to reduce the input current ripple as well as the magnetic size. Moreover, reduction in input current ripple leads to a lower size EMI filter, which results in a reduced overall converter size.

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