Low-Voltage Electrochemical Li_xWO_3 Synapses with Temporal Dynamics for Spiking Neural Networks

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Abstract

Neuromorphic computing has the great potential to enable faster and more energy-efficient computing by overcoming the von Neumann bottleneck. However, most emerging non-volatile memory based artificial synapses suffer from insufficient precision, nonlinear synaptic weight update, high write voltage and high switching latency. Moreover, the spatio-temporal dynamics, an important temporal component for cognitive computing in spiking neural networks, are hard to generate with existing complementary metal-oxide-semiconductor (CMOS) devices or emerging non-volatile memory. Here, we develop a three-terminal, Li_xWO_3-based electrochemical synapse (LiWES) with

low-programming voltage (0.2 V), fast programming speed (500 ns), and high precision (1024 states) that is ideal for artificial neural networks applications. We also demonstrate time-dependent synaptic functions such as paired-pulse facilitation (PPF), temporal filtering that are critical for spiking neural networks. In addition, by leveraging the spike-encoded timing information extracted from the short-term plasticity (STP) behavior in our LiWES, we build a spiking neural networks model to benchmark the pattern classification performance of our LiWES and the result indicates a large boost in classification performance (up to 128×), compared to those NO-STP synapses.

1. Introduction

Neuromorphic computing has emerged as a new computing paradigm to potentially overcome the von Neumann bottleneck for faster and more energy-efficient computing.[1] Despite recent advancement in computing, the human brain still outperforms computers in cognitive tasks owing to its superior energy efficiency, large-parallelism, organizational hierarchy, as well as time-dependent neuronal and synaptic functionality.[2] Hence, researchers have been developing artificial neural networks (ANNs) to mimic the neuro-biological architecture with electronics with a grand goal of building systems with general artificial intelligence (AI). Recently, deep neural networks (DNNs) have demonstrated tremendous progress for tasks like image classification and speech recognition.[3-10] However, these deep learning algorithms require huge amounts of computational resources, especially during the training process. Moreover, the temporal aspect in neural spiking, an integral component for all cognitive functions in the brain (e.g. the timing difference between spikes can represent causality), has been largely omitted in DNNs – limiting their ability in implementing causal relationships and logical inferences. Spiking neural networks (SNNs), which aims to mimic the biological neural network more closely through incorporating the temporal components,[2] offers a promising alternative to complement DNNs with their excellent energy efficiencies and bandwidths from their event-driven nature, as well as their potential for cognitive computing through

implementing logical inference.[11-16] However, it has been challenging and expensive to incorporate and process the spatio-temporal dynamics with existing CMOS devices.[2]

Artificial neuronal and synaptic functionality can be mimicked by emerging nanoelectronics such as phase change memory (PCM),[17-19] resistive random access memory (RRAM),[20-22] spin transfer torque random access memory (STT-RAM),[23, 24] Ferroelectric random access memory (FeRAM),[25, 26] and reconfigurable photonics.[27-30] However, most of these devices are originally optimized for non-volatile memory (NVM) applications and are thus unable to generate time-encoded spikes for SNNs without the use of intricate circuitries, which limits the overall cost and scalability. Recently, emerging three-terminal electrochemical redox transistors have become a promising candidate for mimicking the biologic synapse due to its low power, high precision, linear and symmetric response, low variations, and good endurance performance.[31-39] The channel conductance (i.e., synaptic weight) of the electrochemical synapses can be continuously and controllably modulated via electrochemical reactions (e.g. involving Li^+ or H^+ ion flows) through a gate terminal. While Li^+ ions in the gel electrolyte could potentially be a source of contamination for CMOS fabrications, it is a good material for proof-of-concept of our electrochemical redox transistors due to its well-known electrochemical behaviors. Most recently, we are able to leverage the long-term charge transfer doping effect and the short-term ionic gating effect in electrochemical transistors[39] to demonstrate tunable time-dependent spatiotemporal dynamics, which are critical for spike-based, event-driven computations.[11]

Tungsten oxide (WO_3), consisting of corner-sharing [WO_6]-octahedral structures, can be considered as a pseudo-perovskite oxide with absent A-site cations.[40, 41] The absence of A-site cations can be used as interstitial space for ion intercalation and extraction,[42-44] thus making WO_3 a good candidate for electrochemical synapses. Moreover, insulator-to-metal transition has been demonstrated in epitaxial WO_3 film via electrolyte gating,[45-48] which provides a large conductivity modulation window for building high-precision synapses with a large dynamic range that are ideal

for neuromorphic computing applications.[49] Another advantage of using WO_3 film as the channel material is that the high quality epitaxial WO_3 film can be deposited by radio-frequency (RF) magnetron sputtering,[48, 50] providing a route towards scalable fabrications that enable the wide-spread of smart electronics in the era of the Internet of Things (IoTs).

While WO_3-based electrochemical synapses have demonstrated promising potentials in prior pioneering studies,[51-53] more research efforts are necessary to lower the programming voltage (e.g. 4 V[53]) and improve the programming speed (e.g. 70 ms[51]), two key parameters in artificial synapses. In addition, most of the prior works on WO_3-based electrochemical synapses have been focused on improving the precision for DNNs applications with little to no effort devoted to producing time-coded spikes that are critical for SNNs applications.

In this work, we develop a three-terminal LiWES with low-programming voltage (i.e. ~0.2 V enabled by our self-gated design[34] with near-zero open circuit voltages (OCVs) between the gate and the channel), fast programming speed (500 ns), and high precision (1024 states) that is ideal for DNNs. We also demonstrate time-dependent synaptic functions such as paired-pulse facilitation and temporal filtering that are critical for SNNs. In addition, by utilizing the time-encoded spikes in our LiWES dynamic synapses, we build a SNNs model to benchmark the pattern classification performance, which shows a large boost (128× improvement) in classification performance in highly time-dependent scenarios.

2. Results and Discussion

2.1. Electrochemical Li_xWO_3 Synapse Structure

The structure of our LiWES is similar to that of biologic synapse, as illustrated in **Figure 1**a. In a biologic neural network, a synapse is the small gap (20-40 nm) between a pre-synaptic neuron and a post-synaptic neuron. This connection strength is referred to as the synaptic weight, which can be increased (potentiation) or decreased (depression) by modulating the Ca^{2+} concentration. The electrical signal from pre-synaptic neurons activates the opening of calcium channels, triggering the

release of neurotransmitters from pre-synaptic neurons into post-synaptic neurons. The schematic of our three-terminal LiWES is shown in Figure 1b, where the channel conductance, modulated by the gate terminal, represents the synaptic weight. Tungsten oxide, which contains a large number of vacant A-sites, is ideal for reversible intercalation and de-intercalation of Li ions (Li^+), as evident in its wide use in commercial electrochromic devices.[54] By intercalating (extracting) Li^+ into (out of) the Li_xWO_3 channel, we can potentiate (depress) the synaptic weight (represented by the channel conductance) of our synapse.[33, 39] An optical image of the electrochemical synapse is shown in Figure 1c, depicting a three-terminal planar transistor structure where WO_3 thin films (60 nm) are deposited on $LaAlO_3$ (100) substrate as both the gate and the channel. Adopting the same material for both the gate and the channel allows us to minimize the OCV between the two terminals,[34] hence achieving a low programming voltage. We deposited epitaxial WO_3 film on a $LaAlO_3$ (100) substrate using RF sputtering (See the Experimental Section for fabrication processes). X-ray diffraction (XRD) (Figure 1d) and atomic force microscopy (AFM) (Figure 1e) measurements confirm the good crystallinity of the deposited WO_3 film with an atomically-flat surface (root-mean-square roughness < 600 pm). Having a high-quality, crystalline thin film with a smooth surface is critical for promoting the conductance modulation efficiency in our electrochemical synapse, which involves the electrolyte gating process that is sensitive to the surface smoothness.[48, 50]

2.2. Electrochemical Modulation

In **Figure 2**a, we employ $Li_{0.6}FePO_4$ (LFP) as the Li^+ ion reservoir as well as the reference gate for us to modulate the Li content in both the Li_xWO_3 channel and self-gate, since it provides a near-constant electrochemical window (~3.4 V vs. Li/Li^+ as LFP's Li content changes from $Li_{0.02}FePO_4$ to $Li_{0.9}FePO_4$) to ensure stable operations.[55-57] We can achieve controllable tuning of the Li_xWO_3 channel conductance (i.e. synaptic weight) via changing the Li content through reversible Li intercalation and de-intercalation, where Li intercalation/de-intercalation is a combination of non-

volatile charge transfer doping and the volatile ionic gating effects.[39] We first performed galvanostatic discharge measurements of WO_3 with a constant current of 0.1 nA to establish how the electrochemical potential of Li_xWO_3 relative to the standard potential of Li/Li^+ electrodes (*V* vs. Li/Li^+) changes as a function of the Li concentration (Figure 2b). Consistent with prior studies,[42, 44] the electrochemical potential of Li_xWO_3 decreases as Li content increases. An advantage of our electrochemical approach over conventional resistive memory based synapse is that it allows us to control the Li content (and hence the synaptic weight) in the channel accurately, enabling us to build high-precision, analog synapses[49, 58] that are desirable for DNNs applications. As illustrated in Figure 2c, the channel conductance increases monotonically as the Li concentration increases. This is likely because that Li ions can act as n-type dopants, increasing the channel conductance by shifting *s*-band high above the Fermi level with the charge-balancing electrons occupying the *d* conduction band in Tungsten.[43] The channel conductance can be continuously modulated over four orders of magnitude, suggesting a large dynamic range that is necessary for high-precision synapse. We note that the dynamic range becomes slightly smaller after the 1st cycle of intercalation/de-intercalation, likely due to a small amount of Li ions trapped inside the WO_3 host.[54] The conductance modulation windows between the two cycles are fairly consistent, indicating a repeatable dynamic range for synaptic weight updates. Up to 4 consecutive cycles of the conductance modulation can be seen in **Figure S1**a, further demonstrating the good repeatability of conductance modulation in our LiWES. We also performed a control experiment with only the Poly(ethylene oxide) (PEO) electrolyte (i.e., no WO_3) (Figure S1b), where we observed no change in channel conductance confirming the Li_xWO_3's modulation. Previous studies suggest that Li intercalation can induce phase transformation in WO_3 crystal structure,[42, 44, 46, 47] where the Li_xWO_3 film goes through phase transformations from monoclinic ($0 < x < 0.01$), tetragonal ($0.05 < x < 0.12$), to cubic ($0.32 < x < 0.7$) with increased crystal symmetry as its Li content increases, partly accounting for the electrical properties change in Li_xWO_3 films.[42, 43, 46] As shown in Figure 2b and Figure 2c, non-linearity behavior exists due to the phase

transformation of WO_3 crystal, which is why it is important to lithiate the WO_3 channel and modulate its electrical conductance during the cubic phase region for obtaining a more linear response. Our in-operando Raman measurements (See the Experimental Section for Raman setup) in Figure 2d suggests similar crystal structure changes during the lithiation process. Two strongest peaks in Raman spectra of WO_3 film are located at ~ 715 cm^{-1} and ~ 804 cm^{-1}, corresponding to the asymmetric and symmetric stretching vibrations of W^{6+}-O bonds, while the peak at ~278 cm^{-1} is due to the bridging O-W-O bonds.[59, 60] The intercalation of Li ions induces a larger lattice distortion, forcing the crystal structure to become more symmetric which leads to the gradual diminishing of the peak at 715 cm^{-1} as well as a blue shift of the peak from ~804 cm^{-1} to ~ 806 cm^{-1} resulting from the slightly decreased lattice parameters of Li_xWO_3 bronzes.[44]

2.3. Low-Voltage and High-Precision Synapses

While LFP serves as a good reservoir of Li ions due to its stable electrochemical window, it is not an ideal control gate for a three-terminal artificial synapse because it would lead to a high programming voltage required to overcome the electrochemical potential difference (ranging from ~0.45 V to 1.45 V)[44] between the channel (Li_xWO_3) and the gate (LFP). Hence we adopt a self-gate structure, where we use the same material (Li_xWO_3) for both the channel and the control gate and hence minimizing the potential difference[34] as well as achieving sub-1 V operations. We first lithiated both as-deposited WO_3 gate and WO_3 channel to the same lithiation levels ($Li_{0.4}WO_3$) through applying a constant voltage bias V_{LixWO3} = -1.1 V on both the gate and channel while grounding the LFP reference,[34] allowing us to achieve a near-zero OCV (< 0.1 V) between the gate and the channel as well as a cubic WO_3 crystal structure for obtaining a more linear conductance response via pulse modulation. We envision that only one global LFP gate is needed as the ionic reservoir for a self-gated synaptic array, where pre-charge operations (to charge the self gate to the desired electrochemical level) are sparingly performed. This will enable low-voltage programming as well

as both short- and long-term plasticity while keeping the fabrication and circuity design complexity at a manageble level.

Combining this with the high-precision nature of our synapse originating from the large dynamic range as well as the good tunability enabled by the electrochemical intercalation, we demonstrate both potentiation and depression functions in **Figure 3**a with low programming voltages (0.5 V) and good precision (1024 distinct states). We applied 512/1024 potentiation pulses (0.5 V, 10 ms) and 512/1024 depression pulses (-0.5 V, 10 ms) at $Li_{0.4}WO_3$ self-gate, where we observed a relatively linear and symmetric weight updates. We note a trade-off the dynamic range and linearity/symmetry, where the linearity and symmetry of conductance response are slightly reduced when larger number of pulses are used to push the synapse to a larger dynamic range, likely associated with the saturation of accumulated electric charges at the interface between Li_xWO_3 channel/electrolyte and the asymmetry of electric charges accumulation (potentiation) and release (depression) processes under different directions of electric fields. In biological synapses, the amount of weight change (represented by the change in channel conductance ΔG_{SD} in our device) often varies for different neuronal signals.[61] We can mimic this behavior in our synapse to achieve different ΔG_{SD} by varying the amplitude, width and numbers of the programming pulse(s), as illustrated in Figure 3b-d. We observed pseudo-linear relationships between ΔG_{SD} with respect to the pulse amplitude (from 0.1 V to 2 V, Figure 3b) and width (from 10 ms to 500 ms, Figure 3c), respectively. This is likely because the ΔG_{SD} is dependent on the amount of Li ions being transferred into the Li_xWO_3 film during the programming pulse. We observe a similar pseudo-linear relationship between ΔG_{SD} and the pulse number up to 800 pulses, after which ΔG_{SD} starts to become saturated. This saturation behavior is likely due to the limited amount of Li ions that can be transferred into the channel at a given electrochemical potential between the channel and the gate, which is dictated by the pulse amplitude (i.e., 1 V in Figure 3d) and the lithiation concentration in the channel).

To study the endurance behavior of our synapse, we cycled our synapse over 2000 pulses (20 cycles of 50 potentiation (0.5 V, 10 ms) and 50 depression (-0.5 V, 10 ms) pulses, as shown in Figure 3e), where we observed reversible and repeatable conductance change with a 500% dynamic range. We also performed long-time endurance test for 10^5 pulses on LiWES (**Figure S2**), where the synapse showed no sign of degradation after 10^5 pulses. We carried out thermal stability test for two different states: pristine WO_3 (before lithiation) and $Li_{0.4}WO_3$ (initial conductance state for self-gate and channel after lithiation), where we observed minimal resistance drift over 11 hours at 80 °C for both states **(**Figure 3f**)**. By statistically analyzing the conductance change ΔG_{SD} per pulse in Figure 3e, we observe small temporal (pulse-to-pulse) variations for potentiation pulses and depression pulses, as shown in **Figure S3**a. Additionally, we studied ΔG_{SD} per pulse for four different devices and observed a small device-to-device variation of ~6.5% (Figure S3b), suggesting good repeatability and scalability of our devices.

2.4. Temporal dynamics

For SNNs, a dynamic synapse with both long-term and short-term plasticity (LTP and STP) is essential for learning applications. However, it has been difficult to implement such temporal dynamics with traditional CMOS devices. Our LiWES naturally possesses both LTP and STP, owing to a combination of the volatile ionic gating (**Figure 4**a) and the non-volatile charge transfer doping (Figure 4b) effects. Non-volatile charge transfer doping effect results in LTP as intercalated Li ions could stay at vacant A-sites in pseudo-perovskite tungsten oxide for a long time via the electrochemical reaction as $Li_{0.4}WO_3 + xLi^+ + xe^- \leftrightarrow Li_{0.4+x}WO_3$, while volatile ionic gating effect results in electrical double layer formation (Figure 4b). The ionic gating effect is short term because the accumulated electric charges (Li^+ ions in the PEO electroyte) at the interface between Li_xWO_3 channel and electrolyte would quickly diffuse back to the electrolyte when the external applied electric field (gate voltage) is removed. We are able to achieve the transition of STP to LTP by

switching from a Li_xWO_3 self-gate to a LFP reference gate. As shown in Figure 4c, the Li_xWO_3 self-gate is used to apply voltage pulses which enables a low programming voltage (~ 0.2 V) owing to the near-zero OCV between Li_xWO_3 self-gate and channel. We observed a spike in channel conductance after the programming pulse due to ionic gating effects. As the volatile ionic gating effect dissipates after the voltage pulse, the channel conductance returns towards its original value. In this case, we observed no obvious charge transfer doping effect (LTP) likely because the electrochemical reaction driving force (electrochemical potential differences between gate and channel) for LTP is weak since there is a near-zero OCV between Li_xWO_3 self-gate and channel. By switching from the self-gate to a LFP gate (Figure 4d), we observed a spike in channel conductance likely due to combined ionic gating [ΔG_{ST} (t)] and charge transfer doping effects [ΔG_{LT}]. Since the electrochemical OCV between LFP gate and Li_xWO_3 channel is ~ 1.1 V, there is enough electrochemical reaction driving force for charge transfer doping effect and thus the resulting time-dependent channel conductance consists of a long-term component [ΔG_{LT}] and a time-dependent, short-term component [ΔG_{ST} (t)] such that ΔG_{SD} (t) = ΔG_{LT} + ΔG_{ST} (t). We achieved long-term potentiation and depression via applying multiple pulses at LFP gate, as shown in **Figure S4**a. We also studied the long-time stability for the intermediate conductance states during long-term potentiation and depression (Figure S4b-c), where minimal stability degradation was observed. We also investigate how the pulse duration may affect the amount of weight change using Li_xWO_3 self-gate (Figure 4e). We still observe STP due to ionic gating with pulses as short as 500 ns, consistent with the time scale reported in literature for ionic gating and electrical double layer formation.[62] The amount of STP decreases as the pulse duration decreases, likely because smaller amount of electric charges accumulate at the interface between Li_xWO_3 channel/electrolyte and thus induce less electrons inside the Li_xWO_3 channel in shorter pulses. Additionally, we are able to achieve consistent weight updates over 20 cycles of 50 potentiation (1 V, 1 μs) and 50 depression (-1 V, 1 μs) pulses, with similar linearity and symmetry (Figure 4f) compared to long pulses (10 ms, Figure 3e).

In addition to LTP and STP, time-encoded spikes containing rich temporal information, which are responsible for learning and logical inference in biological neural network, are also desirable for SNNs applications. To better focus on studying temporal dynamics of our synapses, the benchmark of their performance in DNNs would be omitted here but we believe our LiWES synapses could potentially demonstrate decent DNNs performance because of their small energy consumption (~ 2 pJ) for a single pulse event (**Figure S5**), fast programming speed, high precision and low variations. Leveraging the natural decay in our synapses, we demonstrate time-dependent synaptic functions such as PPF and temporal filtering in **Figure 5**, which have been difficult to implement with traditional CMOS devices. Tunable conductance change ΔG for a pair of pulses can be achieved by adjusting the time interval (Δt) between these two pulses at $Li_{0.4}WO_3$ self-gate (Figure 5a), mimicking the short-term, dynamic phenomenon in biological neural network where the amplitude of the second response is dependent on how closely the two pulses are related.[63] In particular, the incremental effect ($G_2 - G_1$) in our synapse becomes less as the time interval becomes longer, as shown in Figure 5b. This resembles the biological learning behavior where the learning effect is better reinforced when two stimulations are more closely related. We also fit two characteristic timescales with a two-term exponential function: $\tau_1 = 19$ ms and $\tau_2 = 433$ ms, which are consistent with those found in biological synapse[63] and other previously reported artificial synapses.[32, 33] Those two characteristic timescales are likely related to the diffusion dynamics of Li ions[32, 33, 39, 51] and can be engineered by changing the device dimension as demonstrated in prior studies.[32, 39] We also examine how the programming energy scales as we vary the dimensions and observe promising scalability down to a channel area of $50 \times 200\ \mu m^2$ (Figure S5). STP can be used to generate filtering functions that are used in information processing, e.g. fish view the surrounding environment through the low-pass temporal filtering by which activated patterns of slow frequency (<10 HZ) are passed while repetitive patterns of fast frequency (> 10 HZ) are rejected.[64] The frequency-dependent high-pass temporal filtering can be mimicked by short-term facilitation (STF).[65, 66] By varying the signal frequency (i.e. time interval

between pulses), we can modulate the maximum conductance level of our device, mimicking a high-pass temporal filtering. As we increase the frequency of a pulse train consisting of 10 consecutive pulses (0.5 V, 10 ms for each pulse) from 1 Hz to 80 Hz at $Li_{0.4}WO_3$ self-gate (Figure 5c), the maximum obtainable conductance level increases.[65] We also studied frequency-dependent gains of high-pass temporal filtering (Figure 5d), where the gain is defined as the ratio of the maximum conductance level of the tenth pulse (G_{10}) to the first pulse (G_1), demonstrating our LiWES can act as a high-pass temporal filter for information processing that is highly desirable for temporal computation in SNNs.

2.5. SNNs computation implementing temporal spiking information

The goal of this section is to show how our LiWES devices' dynamic behaviors could be used to boost classification performance in highly time-dependent scenarios. The principle behind the proposed computation is that when the LiWES devices receive a set of spikes, their conductance value will change depending on the temporal structure (individual spike timings) of the input spike train (Figure 5). Furthermore, in absence of LTP when using Li_xWO_3 self-gate and channel, the conductance of the device will be uniquely determined by the input spiking pattern and the time of integration,[11, 67] granting the device the ability to integrate temporal information and distinguish between different spike patterns.

In standard neuromorphic SNNs with NO-STP synapses, the synaptic efficacy (or weight), which remains fixed during inference, is used to simply scale current pulses directed towards the post-synaptic neuron. In these models, the temporal integration of stimuli is left solely to the neuron; whereas in STP enabled networks, synapses also encode temporal information through weight changes, enriching network dynamics[65, 68, 69] and increasing the ability of neurons to discriminate between temporal stimuli.[70] For this reason, when compared to NO-STP synapses, a network including the proposed LiWES device should increase its performance in highly time-dependent tasks,

such as classification of different spike patterns. In order to test this hypothesis, we propose a test tailored to compare our LiWES to an IDEAL synapse (a noiseless LiWES device) and a standard NO-STP synapse. Here, we connect a post-synaptic neuron, modelled with Leaky Integrate and Fire profile (parametrized with the membrane decay constant τ_m and spiking threshold = ∞), to a pre-synaptic neuron, which is a Poisson Spike generator (**Figure 6**a). As shown in Figure 4c, the channel conductance response of our LiWES shows a spike profile, where the conductance quickly reaches the maximum conductance level followed by an exponential decay back to initial conductance level, due to ionic-gating governed STP effect. Thus, we are able to model the conductance response of our LiWES with a linear rise equation (gate-pulse applied) and a double exponential decay equation (gate-pulse removed). (See the Experimental section for model build details). Every time the synapse receives a new spike at the time t_i, the parameter G_{off} gets updated to the last conductance value while a set of parameters are drawn to generate a response as the one shown in Figure 6b.

In the proposed task, we generate multiple pre-synaptic neuron spike trains with a fixed maximum duration. Since each spike sequence is randomly generated at a fixed frequency, therefore it differs from the others mainly by its temporal characteristics (the timestamps of individual spikes) and it represents a single class of a classification problem. The beginning of each spike train is delimited by t_{onset}. A "sequence end spike" is added at the end of each spike train at a specific time t_{end} (Figure 6c) and the post-synaptic neuron membrane potential is read out at t_{read} (Figure 6d), representing the output of the system. Each spike train is presented to the synapse multiple times to obtain multiple membrane potential read-outs for the same "class" (or spike pattern). To calculate the class separability of the read-outs, we define a distance metric as the difference between the euclidean distance of points between different classes (inter-class distance) and the distance of the points within the same class (intra-class distance) in Figure 6e. Since the membrane potential of the post-synaptic neuron is always read out at the same time (t_{read}) after the last spike (t_{end}), a neuron unable to integrate temporal information will have similar membrane potential for different spike patterns and therefore

it will have an average inter-class distance of zero or close to zero, However, for an STP enabled neuron, its membrane value depends on previous spiking activity, which gives different values of inter-class distance based on different classes. This is the case shown in Figure 6f, where a fast spiking neuron (τ_m = 10 ms) is stimulated with Poisson generated spikes at a slow mean 10 Hz frequency. The number of classes used for this simulation was 50, each one presented 10 times (for intra-class measurement), for a total number of 500 points. In this case, class separability (inter-class distance – intra-class distance) is ~3.8×10^{-4} for the NO-STP synapse, ~4.9×10^{-2} for our LiWES device (~128× higher relative to NO-STP synapse), and ~8.6×10^{-2} for the IDEAL synapse (~226× higher compared to NO-STP synapse), with using a synaptic weight *k* of 4.3 (See the Experimental section for model build details). As both comparison synapses (NO-STP and IDEAL synapses) are totally deterministic, their mean intra-class distance is 0. The same simulation parameters were used in Figure 6g for a much slower post-synaptic neuron (τ_m = 100 ms). Even though the post-synaptic neuron is relatively slower to integrate temporal information, a boost in class separation (~1.4× in our LiWES and ~1.7× in the IDEAL synapse, relative to the NO-STP synapse) can still be achieved owing to the natural stochastic STP in our LiWES. The class separability are ~8.4×10^{-2} , ~1.2×10^{-1} , ~1.4×10^{-1} , for the NO-STP synapse, our LiWES device, and the IDEAL synapse respectively, with using a synaptic weight *k* of 16.7. By implementing the temporal spiking information in STP of our LiWES, we improve the pattern classification performance (up to 128× comparted to NO-STP synapse) in highly time-dependent scenarios.

3. Conclusion

In summary, we develop a WO_3-based, electrochemical synapse with low programming voltage (0.2 V), fast programming speed (500 ns), high precision (1024 levels), low variations, as well as a relatively linear and symmetric response. In addition, our dynamic synapse naturally exhibits both LTP and STP behaviors owing to the combined effects from charge transfer doping and ionic gating, which is desirable for SNNs applications. We demonstrate various time-dependent synaptic functions

such as pair-pulse facilitation and temporal filtering. By leveraging the spike-encoded timing information extracted from the short-term plasticity exponential decay behavior, we build a SNNs model to benchmark the pattern classification performance of our LiWES, which shows a large boost (128× improvement) in classification performance in highly time-dependent scenarios.

4. Experimental Section

Fabrication of Electrochemical WO_3 Synapses: Epitaxial tungsten oxide (WO_3) thin films were deposited on (100) $LaAlO_3$ substrates (MTI Ltd.) using radio-frequency (RF) magnetron sputtering with WO_3 target (99.99% purity from Sigma-Aldrich). A total RF power of 80 W was used. The process pressure was kept at 60 mTorr with a gas ratio of 1:2 for Ar : O_2, while the deposition temperature was kept at 650 °C to achieve a deposition rate at 1 nm per min. The resulting WO_3 film thickness was 60 nm, measured by a surface profiler (KLA-Tencor AlfaStep IQ). During the deposition of WO_3 film, a shadow mask was used for patterning. Devices of different channel areas (from 1000 × 200 μm^2 to 200 × 50 μm^2) were fabricated for variation study. For the electrical characterization and pulse measurement, devices of 400 × 200 μm^2 channel area were used. Au contacts (100 nm) with a Ti adhesion layer (5 nm) were deposited using an electron-beam evaporator and patterned by a shadow mask.

The reference gate LFP was placed about 2 mm away from the WO_3 channel. The LFP gate was prepared by manually coating the LFP slurry[34] onto a Au contact pad. The PEO electrolyte was prepared by mixing 30 wt % $LiClO_4$ (Sigma-Aldrich) with poly(ethylene oxide) (molecular weight 600, 000 from Sigma-Aldrich) in acetonitrile solvent. Subsequently, the PEO electrolyte (~ 1 μm)[71] was drop-casted to cover both the WO_3 gate/channel and the LFP reference gate. The PEO serves as an electrolyte for Li^+ ions transport in both cases: Li_xWO_3 self-gate and channel, LFP gate and Li_xWO_3 channel. The difference between self-gate and LFP gate is the OCV between gate and channel as well as the required programming voltage. To remove the residual solvent, the sample was

heated at 80 °C on a hot plate overnight. All the chemical preparation and operation steps were performed in an Ar-gas glovebox.

XRD and AFM characterization: The Bruker D8 Discover instrument was used for XRD measurement. The WO_3 film sample for XRD was annealed at 650 °C in air for 1 hour. The asylum MFP-3D was used for AFM measurement and a scan area of 1 μm × 1 μm was chosen for surface roughness analysis.

Raman Spectroscopy: The Horiba Scientific system with a 633 nm laser (1800 gr mm^{-1} grating) was used for in-operando Raman measurements. The absorbed laser power was kept low (< 5 mW) to avoid excessive laser heating.

Electrochemical Characterization: Electrochemical galvanostatic discharge measurement was carried out with an SP-200 Biologic workstation. A constant discharge/charge current of 0.1 nA was applied with the WO_3 channel connected to the working electrode and the LFP reference gate connected to the counter/reference electrodes.

Electrical Characterization and Pulse Measurement: Electrical characterization and pulse measurement were performed with Keithley Semiconductor Parameter Analyzer (4200-SCS) with pulse measuring units. During the test, the sample was transferred into the vacuum probe station (JANIS ST-500-UHT) and annealed at 350 K for ~2 hours to eliminate the residual moisture before the electrical measurements. For fast-speed pulse tests, an arbitrary function generator (Tektronix AFG3252C) and a mixed domain oscilloscope (Tektronix MDO 3034) with a high-speed current amplifier (FEMTO DHPCA-100) were used via a customized LABVIEW program.

SNN computation model: We model our LiWES device behavior using a linear rise (Equation 1) and a double decay exponential model (Equation 2), using equation (3) to define the rise and decay parts, respectively.

$$G_{rise}(t) = \left(\widehat{A_1} + \widehat{A_2}\right)\frac{t-t_i}{w} + \eta + G_{off} \quad (1)$$

$$G_{decay}(t) = \left(\widehat{A_1} + \frac{G_{off}}{2}\right)e^{-\left(\frac{t-t_i}{\widehat{\tau_1}}\right)} + \left(\widehat{A_2} + \frac{G_{off}}{2}\right)e^{-\left(\frac{t-t_i}{\widehat{\tau_2}}\right)} + \eta \quad (2)$$

$$G(\mathrm{t}) = \begin{cases} G_{rise}(t)\ when\ (t-t_i) < w \\ G_{deacy}(t)\ when\ (t-t_i) \geq w \end{cases} \quad (3)$$

The model parameters $(\widehat{A_1}, \widehat{A_2}, \widehat{\tau_1}, \widehat{\tau_2})$ are drawn from Gaussian distributions fitted on experimental recordings obtained with a single pulse stimulus of a given amplitude and pulse width *w*. Additive Gaussian noise η with a mean of 0 is also added to simulate device and recording setup noise.

In order to obtain the Gaussian distributions of the LiWES parameters $(\widehat{A_1}, \widehat{A_2}, \widehat{\tau_1}, \widehat{\tau_2})$ and the standard deviation the additive noise, we fit the decay equation (Equation 2) on the device response to a single pulse (1 V, 200 µs) for 20 consecutive trials. Every trial produces a set of parameters (A_1, A_2, τ_1, τ_2, η), which can be then averaged to produce the **Table 1**.

Table 1. Model parameters for a single pulse (1 V, 200 µs). Results of an averaged fit over 20 consecutive recordings. All parameters are presented with their mean ± standard deviation except for η, which is the mean standard deviation of each individual fit.

A_1	τ_1 [ms]	A_2	τ_2 [ms]	η
0.57± 0.27	5 ± 2	0.5 ± 0.05	92 ± 18	0.11

When simulating the noise-free, IDEAL synapse, we use the same parameters presented above but set all standard deviations and additive Gaussian noise η to 0. Finally, the NO-STP synapse is modelled as a weighted Dirac pulse centered on the input spike timestamp t_i (Equation 4):

$$G(t) = \sum_{t_i} k\delta(t - t_i) \quad (4)$$

where *k* is the synaptic weight chosen so that the peak response of the post-synaptic neuron to a single spike is the same to the IDEAL synapse.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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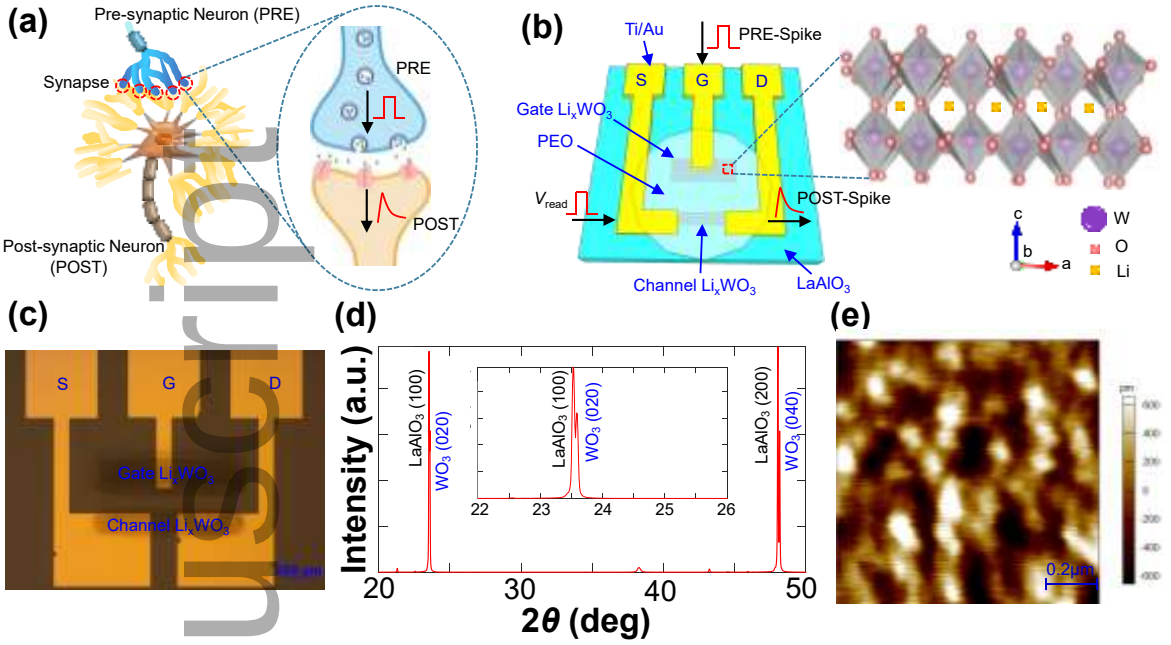

Figure 1. Biologic synapse compared to our LiWES and the characterization of epitaxial WO_3 film. a) Biologic neuron and synapse structure. b) Schematic of our LiWES and the inset shows the crystal structure of WO_3 octahedrons. c) Optical image of the LiWES without electrolyte coating. d) X-Ray Diffraction of the epitaxial WO_3 film on $LaAlO_3$ (100) substrate. e) Atomic Force Microscopy image of the epitaxial WO_3 film, showing the atomically flat surface with a root-mean-square (rms) roughness less than 1 nm.

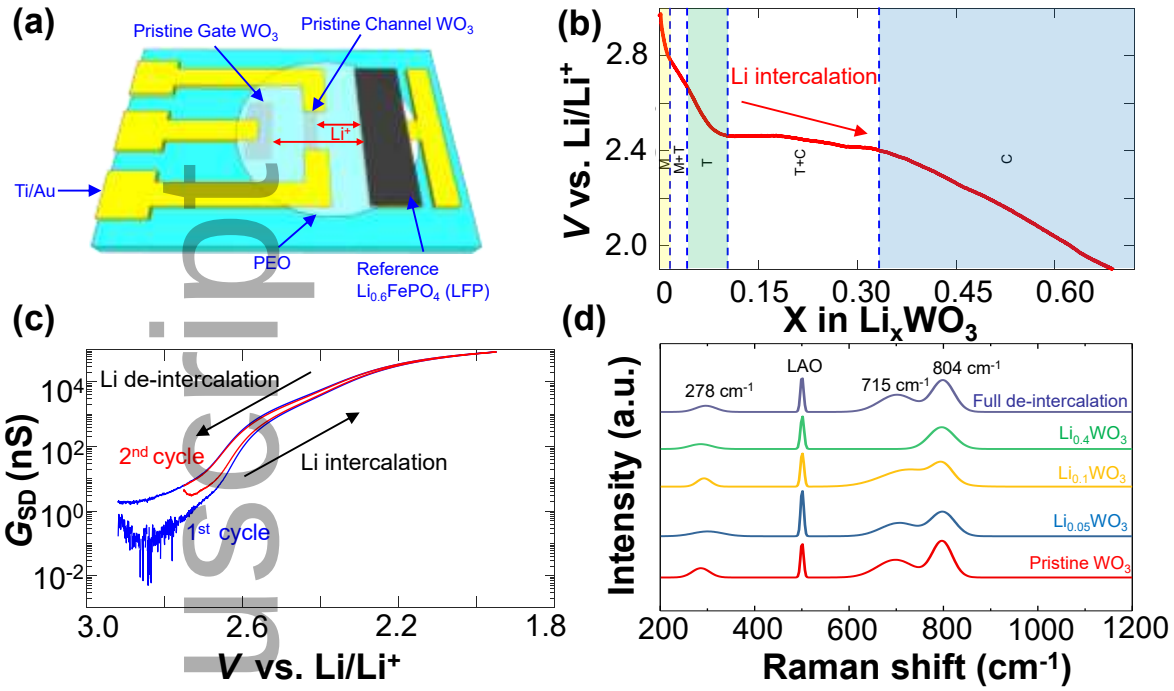

Figure 2. Electrochemical characterization of WO_3 film during Li intercalation/de-intercalation. a) The schematic of the electrochemical cell for Li intercalation and de-intercalation. b) Galvanostatic discharge (intercalation) of WO_3 film using constant current 0.1 nA during in-operando Raman spectra, indicating the electrochemical potential of Li_xWO_3 change relative to the standard potential of Li/Li^+ electrodes (V vs. Li/Li^+) as a function of Li concentration. c) The electrical channel conductance change as a function of the electrochemical potential of Li_xWO_3 change during Li intercalation/de-intercalation. d) In-operando Raman spectra change of WO_3 film during Li intercalation/de-intercalation.

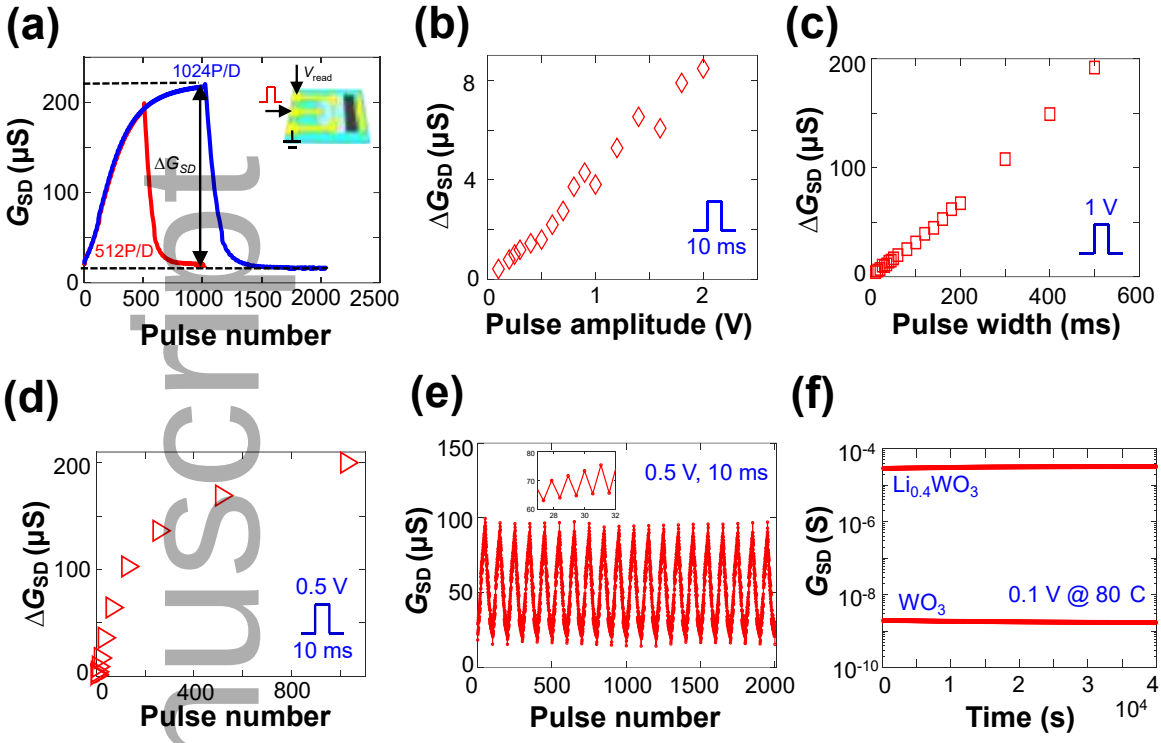

Figure 3. Synaptic weight modulation for DNNs application using our low-voltage LiWES. a) Dynamic range and precision controlled by using different numbers of programming potentiation pulses (0.5 V, 10 ms) and depression pulses (-0.5 V, 10 ms) at $Li_{0.4}WO_3$ gate (the inset). b) Synaptic weight change as a function of pulse amplitude. c) Synaptic weight change as a function of pulse width. d) Synaptic weight change as a function of pulse number. e) Endurance test using 20 cycles of 50 potentiation pulses (0.5 V, 10 ms) and 50 depression pulses (-0.5 V, 10 ms) at $Li_{0.4}WO_3$ gate. f) Stability test for two different states: pristine WO_3, $Li_{0.4}WO_3$ (initial conductance state for self-gate and channel), using reading voltage of 0.1 V at 80 °C.

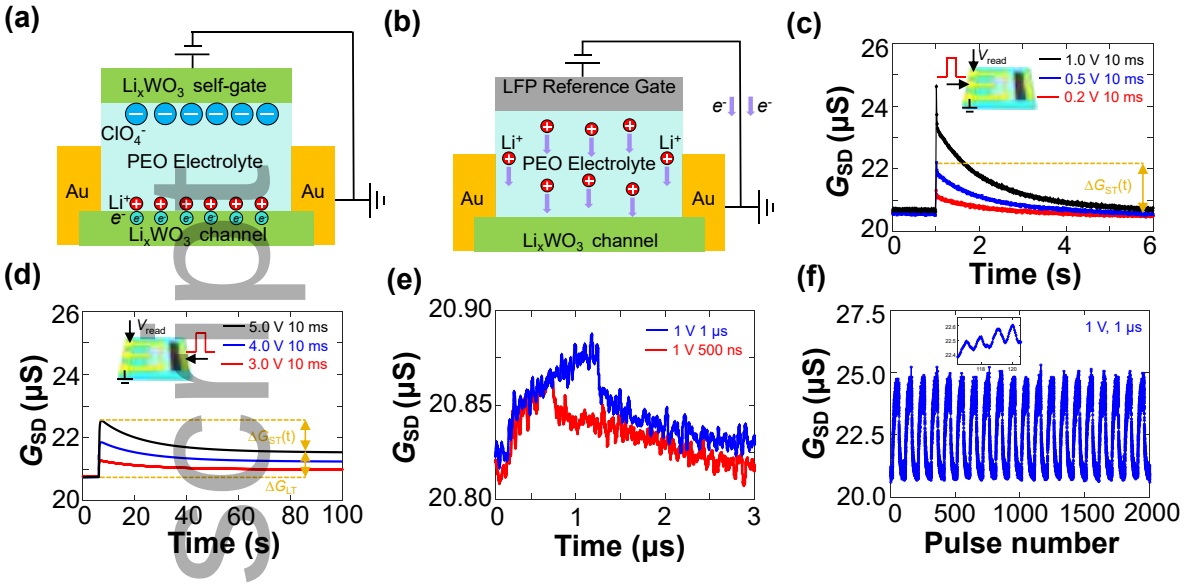

Figure 4. STP, LTP and high-speed programming of our LiWES. a) Ionic gating effect for STP. b) Charge transfer doping effect for LTP, where the electrochemical reaction occurs as $Li_{0.4}WO_3 + xLi^+ + xe^- \leftrightarrow Li_{0.4+x}WO_3$, which is a type of donor doping. c) STP using $Li_{0.4}WO_3$ gate and $Li_{0.4}WO_3$ channel, controlled by different amplitudes of single pulse at $Li_{0.4}WO_3$ gate side. The inset shows the test setup. d) LTP using LFP gate and $Li_{0.4}WO_3$ channel, controlled by different amplitudes of single pulse at LFP gate. The inset shows the test setup. e) High-speed programming using different width of single pulse applied at $Li_{0.4}WO_3$ self-gate. f) Synaptic weight modulation via 20 cycles of 50 potentiation pulses (1 V, 1 μs) and 50 depression pulses (- 1 V, 1 μs) applied at $Li_{0.4}WO_3$ self-gate.

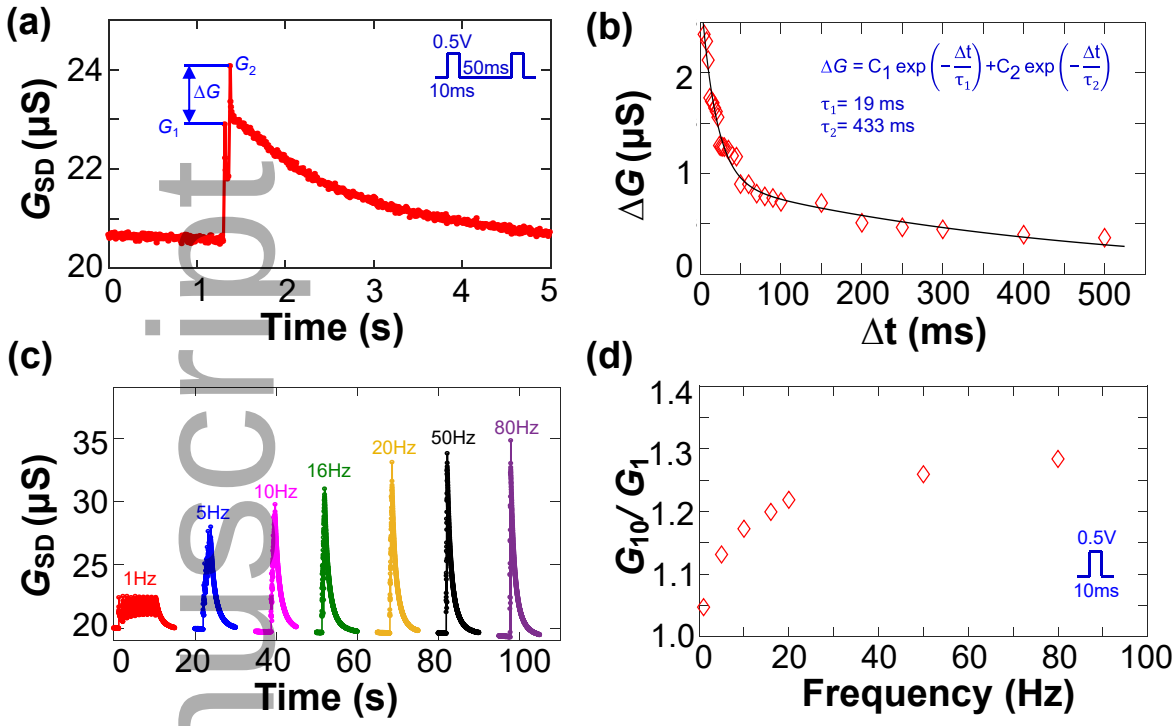

Figure 5. Bio-realistic, time-dependent synaptic functions for SNNs. a) Two consecutive pulses (0.5 V, 10 ms, Δt = 50 ms) at $Li_{0.4}WO_3$ gate showing paired-pulse facilitation. b) Paired-pulse facilitation with exponential decay fitting. c) High-past temporal filtering characteristics of the our LiWES via applying 10 potentiation pulses (0.5 V, 10 ms) with different frequencies (1/Δt) at $Li_{0.4}WO_3$ gate. d) The frequency-dependent conductance gain.

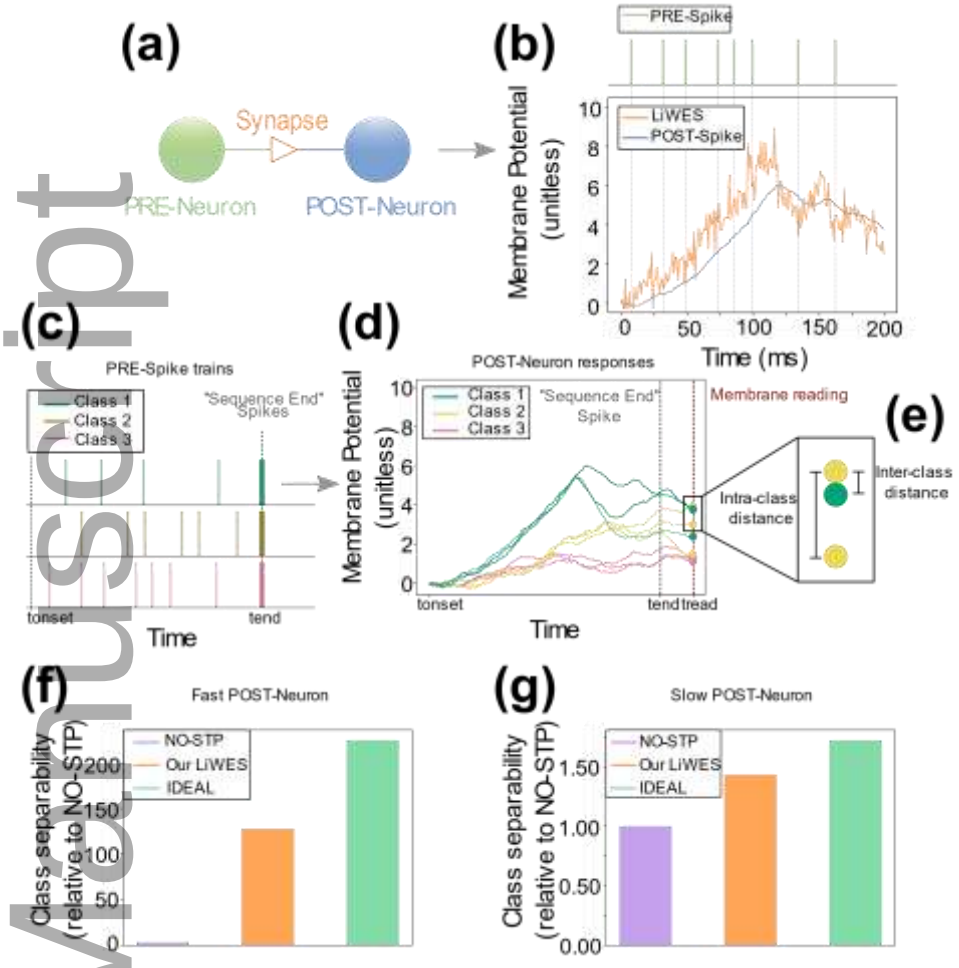

Figure 6. SNNs computation based STP of our LiWES. a) The diagram of our network, a Poisson pre-synaptic (PRE) neuron connected to a Leaky and Integrate and Fire post-synaptic (POST) neuron through a synapse (NO-STP, our LiWES or IDEAL synapse). b) An example of a Poisson train spike eliciting activity in our LiWES and the consequently generated membrane potential. c-e) An example of the proposed spike-based SNNs computation model for classification performance benchmark. c) The PRE-Neuron produces multiple random spike trains, at the end of each one we add a "sequence end" spike occurring always at the same timestamp(t_{end}). Each spike train represents a different class in a classification problem. d) We then record multiple POST-Neuron responses (three responses per each spike train), in order to better characterize the device noise and cycle-to-cycle variation, and finally we save the membrane value after the "sequence end spike" (at t_{read}). e) Lastly, for each point we calculate the inter-class distance between points of different spike trains, and the intra-class distance between points of the same spike train class.

These measures indicate how much each point position encodes for temporal information and how well the points are separable in a classification task. f,g) The classification result of the benchmarked synapses. f) The classification comparison for a 10 Hz Poisson PRE-Neuron and a fast POST-Neuron (τ_m= 10 ms). g) The classification comparison for the same 10 Hz Poisson PRE-Neuron but a much slower POST-Neuron (τ_m= 100 ms).

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Supporting Information

Low-Voltage Electrochemical Li_xWO_3 Synapses with Temporal Dynamics for Spiking Neural Networks

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1. Repeatability of conductance change and control sample during the Li intercalation/de-intercalation

We prepared a new LiWES device (200 × 50 μm^2) for exploring the repeatability of the conductance modulation during the Li intercalation/de-intercalation. During the test, a small DC reading voltage (0.1 V) was applied between the Source and Drain to continuously monitor the current/conductance level, while a gate dual-sweeping voltage ranging from 1.95 V to 2.75 V (*V* vs. Li/Li^+) was applied to the LFP for Li intercalation/de-intercalation. Up to 4 cycles of test were performed (**Figure S1**a) and we observed a fairly consistent dynamic range, which demonstrates the good repeatability of the conductance modulation of our LiWES during the Li intercalation/de-intercalation.

We fabricated a control sample without depositing WO_3 film and only deposited the Au (100 nm)/Ti (5 nm) metal contacts for Source and Drain. The reference gate LFP was placed about 2 mm away from the Source/Drain contacts and was manually coated with LFP slurry. PEO electrolyte was prepared[1] and drop-casted to cover both the Source/Drain contacts and LFP reference gate. The sample was heated at 80 °C on a hot plate to remove the residual solvent in Ar-gas glovebox. During the test, the sample was transferred into the vacuum probe station (JANIS ST-500-UHT) and annealed at 350 K for ~2 hours to eliminate the residual moisture before the electrical measurements. During the test, a small DC reading voltage (0.1 V) was applied between the Source and Drain to continuously monitor the current/conductance level, while a gate dual-sweeping voltage ranging from 1.95 V to 2.82 V (*V* vs. Li/Li^+) was applied to the LFP for Li intercalation/de-intercalation. As shown in Figure S1b, there is negligible current/conductance change during the gate dual-sweeping processes, which confirms that the 4 orders of magnitudes of conductance changes are due to the Li intercalation into WO_3 films, rather than electrical conductance changes of the PEO electrolyte.

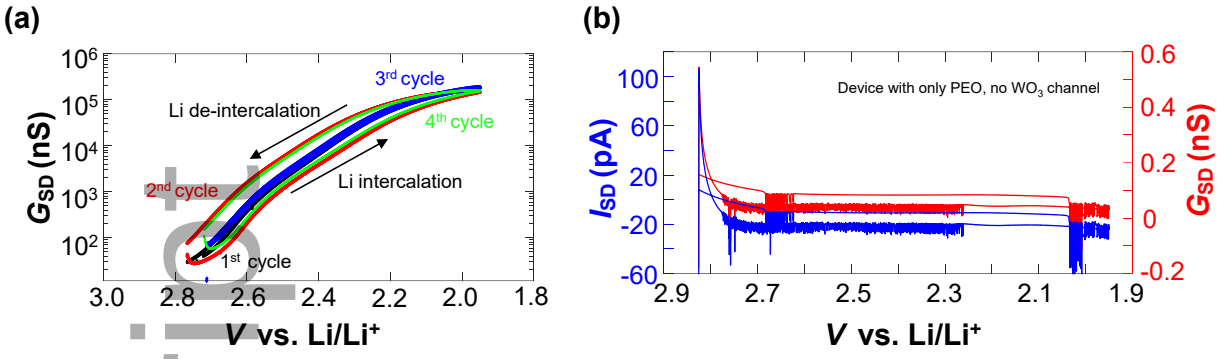

Figure S1. a) The electrical channel conductance change as a function of the electrochemical potential of Li_xWO_3 change during 4 consecutive cycles of Li intercalation/de-intercalation, demonstrating good repeatability. b) I_{SD} and G_{SD} response as a function of the gate sweeping voltage (V vs. Li/Li^+) when no WO_3 film is deposited as the channel and only PEO electrolyte is coated to cover the LFP reference electrode and channel area.

2. Endurance performance

For long-time endurance, we adopted a similar test method as reported in previous work.[2] We cycled our LiWES using 1000 cycles of 50 potentiation (0.5 V, 10 ms) and 50 depression (-0.5 V, 10 ms) pulses with a dynamic range ~ 500 %, shown in **Figure S2**. After the 10^5 pulses, our LiWES device is still working and shows no obvious degradation.

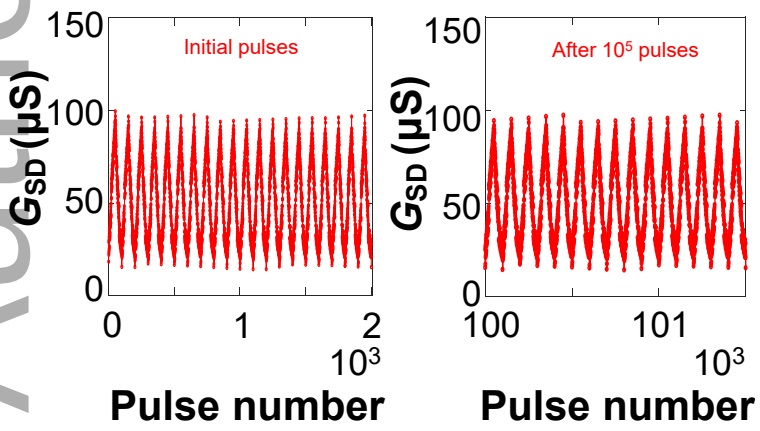

Figure S2. Long-time endurance performance of our LiWES. Endurance test for 10^5 pulses on our LiWES using 1000 cycles of 50 potentiation (0.5 V, 10 ms) and 50 depression (-0.5 V, 10 ms). No degradation of the device is found even after the 10^5 pulses.

3. Variation

Pulse-to-pulse variation and device-to-device variation are very important parameters for evaluating the synaptic device performance for DNNs application.[3] We leveraged the data from Figure 3e and statistically analyzed the conductance change ΔG_{SD} per pulse over the whole dynamic range window. As shown in **Figure S3**a, we find a relatively small variation ~11% of ΔG_{SD} per pulse for potentiation pulses (red) and ~13% for depression pulses (blue). For device-to-device variation (Figure S3b), we fabricated four different devices of the same dimensions (400 × 200 μm^2) in one single batch and applied a single potentiation pulse (0.5 V, 10 ms) to the Li_xWO_3 gate while monitoring the channel conductance change using a small reading voltage (0.1 V) between Li_xWO_3 Source/Drain. We find a small variation of 6.5 %, which demonstrates the good repeatability of our devices.

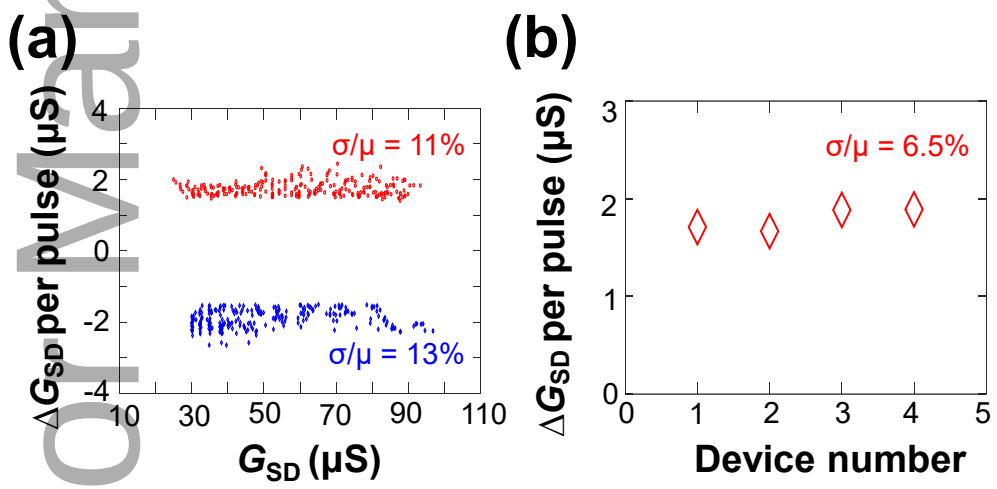

Figure S3. Variation test**.** a) Cycle-to-cycle (pulse-to-pulse) variation, plotted using data from Figure 3e. Small variation ~11% of ΔG_{SD} per pulse is found for potentiation pulses (red) and ~13% variation of ΔG_{SD} per pulse is found for depression pulses (blue). b) Small device-to-device variation ~6.5% of ΔG_{SD} per pulse using single potentiation pulse (0.5 V, 10 ms).

4. Long-term potentiation and depression via LFP gate

We further explored the long-term potentiation and depression by switching to use the LFP gate. For synaptic weight modulation via multiple pulses, we applied 50 potentiation pulses (3 V, 10 ms) and 50 depression pulses (- 1 V, 10 ms) applied at LFP gate as shown in **Figure S4**a. A dynamic range (~ 200 %) was achieved. During the test, a small DC reading voltage (0.1 V) was applied between the Source and Drain to continuously monitor the current/conductance level, while programming pulses were applied at LFP gate. Since the electrochemical OCV between LFP gate and $Li_{0.4}WO_3$ channel is ~ 1.1 V, we need to use potentiation pulses (3 V) and depression pulses (-1 V) at LFP gate to achieve a base voltage level (1 V) that can offset the OCV difference in order to obtain a more linear and symmetric conductance response.

For confirming the intermediate conductance level stability in Figure S4a, we applied 5 potentiona pulses (3 V, 10 ms) at LFP gate (Figure S4b) and then used a small DC reading voltage (0.1 V) at 80 °C to monitor the channel conductance and observed small gradual stability degradation that is likely due to to the slow self-extraction of the pulse-injected Li ions under high temperature at 80 °C. We also studied the long-time stability of the device after applying 5 depression pulses (-1 V, 10 ms) (Figure S4c) and no obvious stability degradation was observed.

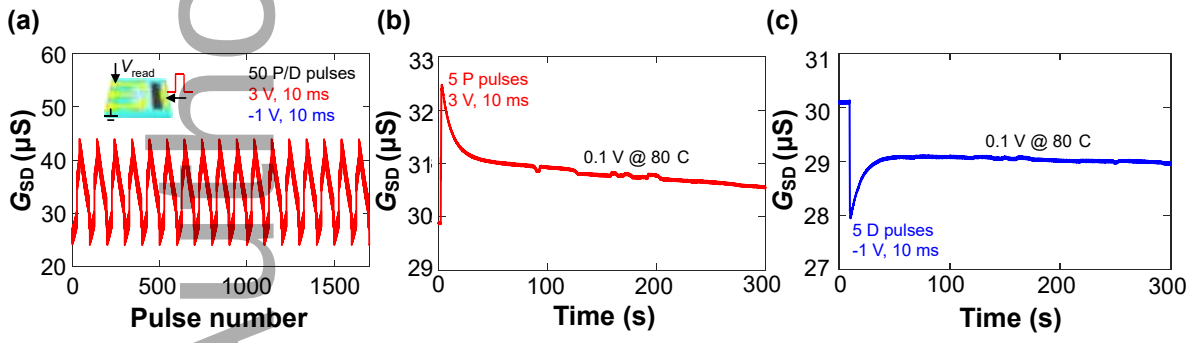

Figure S4. a) Synaptic weight modulation via multiple cycles of 50 potentiation pulses (3 V, 10 ms) and 50 depression pulses (- 1 V, 10 ms) applied at LFP gate. b) Long-time stability test of the LiWES device after 5 potentiation pulses (3 V, 10 ms) were applied. There is small gradual stability degradation, likely due to the slow self-extraction of the pulse-injected Li ions under high

temperature at 80 °C. c) Long-time stability test of the LiWES device after 5 depression pulses (- 1 V, 10 ms) were applied. No obvious stability degradation was observed.

5. Scaling performance

We fabricated devices of different channel areas (from 1000 × 200 μm^2 to 200 × 50 μm^2) and applied single potentiation pulse at Li_xWO_3 gate while monitoring the channel conductance change. We define the programming energy as $E = I \times V \times$ t, which is enough to induce 10% increase of conductance change ($\Delta G_{SD}/ G_0$). Since there is near-zero open-circuit voltage (OCV) between our Li_xWO_3 gate and channel, V and t denote the programming voltage pulse amplitude[4] and programming voltage pulse width, respectively, while we define the current I as the average current between our Li_xWO_3 gate and channel. As shown in **Figure S5**, our smallest device (200 × 50 μm^2) demonstrates a very small programming energy (~ 2 pJ) and it shows a pseudo-linear scalability trend as previously reported.[5]

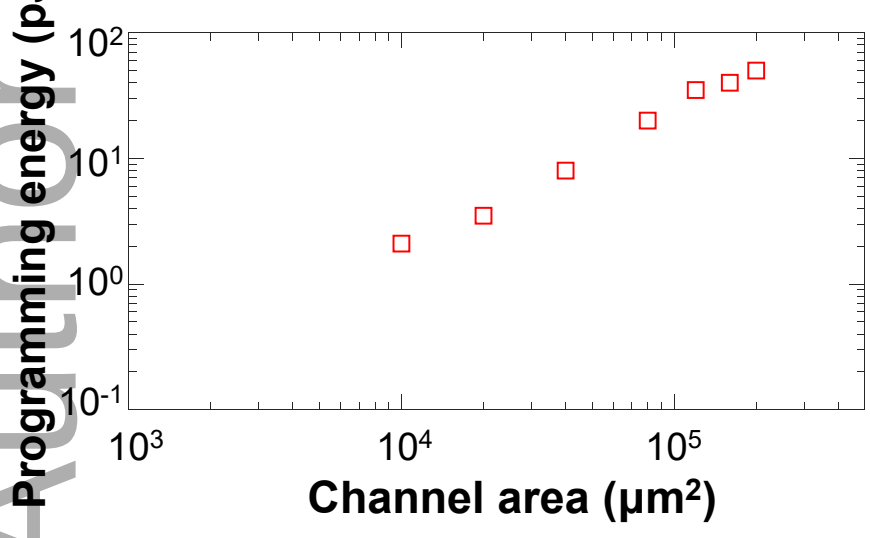

Figure S5. Scaling performance of programming energy as a function of channel area.

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