Thin-Film III-V Devices for Low-Cost Detection and Energy Conversion

by

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Dedication

To my loving family and a better world

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Abstract

III-V compound semiconductors are excellent candidates for high-performance optoelectronic devices due to their superior optical and electrical properties compared to elemental semiconductors. However, their expensive manufacturing cost compared to silicon-based optoelectronics often hinders their widespread use in general applications. Separating thin-film III-V epitaxial active layer from its growth substrate allows for potential reuse of the remaining substrate, which can reduce the substrate cost by a factor of total number of recycling. Moreover, thin-film structures allow fabrication of lightweight, flexible devices with improved photon recycling or light trapping, which can enhance device performance compared to conventional substrate devices.

In this thesis, we introduce various applications using thin-film III-V photovoltaics (PV) and photodetectors. With non-destructive epitaxial lift-off (ND-ELO) technique, we demonstrate a thin-film GaAs PV cell fabrication and substrate recycling on a 4" GaAs wafer. We then integrate the thin-film PV cells with a low-cost mini parabolic concentrator array, which can potentially maintain a low profile compared to conventional bulky concentrated PV (CPV) modules. We also demonstrate a GaAs *p*-*n* junction focal plane array that resembles the shape and size of the human eye. Moreover, we deploy thin-film $In_{0.53}Ga_{0.47}As$ (InGaAs) *p*-*n* junction thermophotovoltaic (TPV) device with Au surface back reflector and demonstrate a near-field heat transfer, with nearly an order of magnitude enhanced power conversion efficiency.

In addition, we estimate manufacturing cost of single junction GaAs PV cells with potential cost reduction scenarios such as improved throughput or increased number of substrate recycling. Our study reassures that substrate recycling plays a critical role in reducing the final cost. We also find that past claims that enhanced throughput can bring down the cost of GaAs PV to levels comparable to Si in terrestrial applications may be misleading.

Finally, we demonstrate a Si TPV cell using air-bridge back surface reflector, with low series-resistance and high out-of-band reflectance (~97%). We estimate ~10% power conversion efficiency even under 1500K blackbody radiation, a source temperature where Si is considered impractical due to its high bandgap. We expect this advance could expedite the widespread of TPV system via reduced cost compared to conventional TPV materials such as InGaAs or InSb.

Chapter 1

Introduction

III-V compound semiconductors are made from group III (In, Ga, Al, etc.) and group V (As, P, Sb, N, etc.) elements in the periodic table. Consisting elements mostly form zinc-blend (Arsenides, Phosphides, etc.) or wurtzite crystal structures (Nitrides) via covalent bonding. Compound semiconductors provide superior optoelectronic properties such as strong absorption, bandgap tunability or high carrier mobility compared to conventional elemental semiconductors (Si, Ge). Such properties make them suitable for variety of optoelectronic devices including light emitting diodes (LEDs), lasers, photodetectors and energy harvesting devices. Yet their high-cost compared to Si hinders their use in some applications despite superior device performance. Exploiting the full benefit of III-V compound semiconductors requires achieving reasonable economics while pushing the device performance to its limits. This thesis includes our work on achieving low-cost III-V thin-film devices, and a brief overview will be covered in the chapter, as well as an introduction to III-V semiconductor technologies.

1.1 Thesis overview

Achieving thin-film structures with III-V semiconductor layers plays a crucial role in high-performance solid-state semiconductor optoelectronics, as thin-film devices provide several advantages over their counterparts grown on bulk substrates (GaAs, InP, InAs or GaSb). On top of achieving high-performance with novel device structure or processing, maintaining reasonable

manufacturing costs is extremely important for widespread use of such technologies. Among diverse optoelectronic devices, this thesis focus on efficient and low-cost energy harvesting and light detection applications using thin-film III-V semiconductors. Basic properties of III-V semiconductors and optoelectronic devices will be covered in the later part of the chapter 1. Then, chapter 2 introduces methods of acquiring thin-film structures and potentially reusing the substrate that is left after the separation of the thin film. Chapter 3 introduces our efforts on scaling the GaAs substrate recycling process for up to 4" diameter wafers. Chapter 4 introduces a concentrated photovoltaic (CPV) system with a tracking array using thin-film GaAs photovoltaics (PV) and low-cost mini-concentrators. The manufacturing cost of single-junction, GaAs PV cells is analyzed in chapter 5. Itemized manufacturing cost is estimated in each fabrication step and compared with several different growth technologies, including proposed linear-molecular beam epitaxy (LMBE) system with improved system throughput.

Using thin-film separation and wafer recycling methods introduced in earlier chapters, several different III-V thin film light detection and energy harvesting systems are summarized in later chapters. A thin-film GaAs photodetector array on a hemispherical surface is introduced in chapter 6. Transferring thin-film structures to unconventional surfaces are covered in detail. Chapter 7 summarizes our work on a high-efficiency InGaAs near-field thermophotovoltaic (TPV) system. Methods for maintaining particle-free, extremely smooth device surfaces as well as the approach of two parallel surfaces into sub-hundread nanometer gap is introduced. In chapter 8, Si TPVs with air-bridge back surface reflector are introduced. Improved out-of-band reflectance can potentially allow use of Si TPV cells under relatively low temperature emitters (~1500K), which was considered impractical due to high bandgap. Finally, conclusion and future works are covered in chapter 9.

1.2 III-V semiconductors

1.2.1 Bonding in solids

Atoms are held with repulsive and attractive forces which determines the interatomic distance.[1] As shown in Fig. 1.1, Coulombic and repulsive forces compete, while repulsive force dominates at short distance and Coulombic force dominates at longer distance. The lowest potential energy point determines the stable interatomic distance, which is the 'lattice constant' in a single crystalline solid.[2]

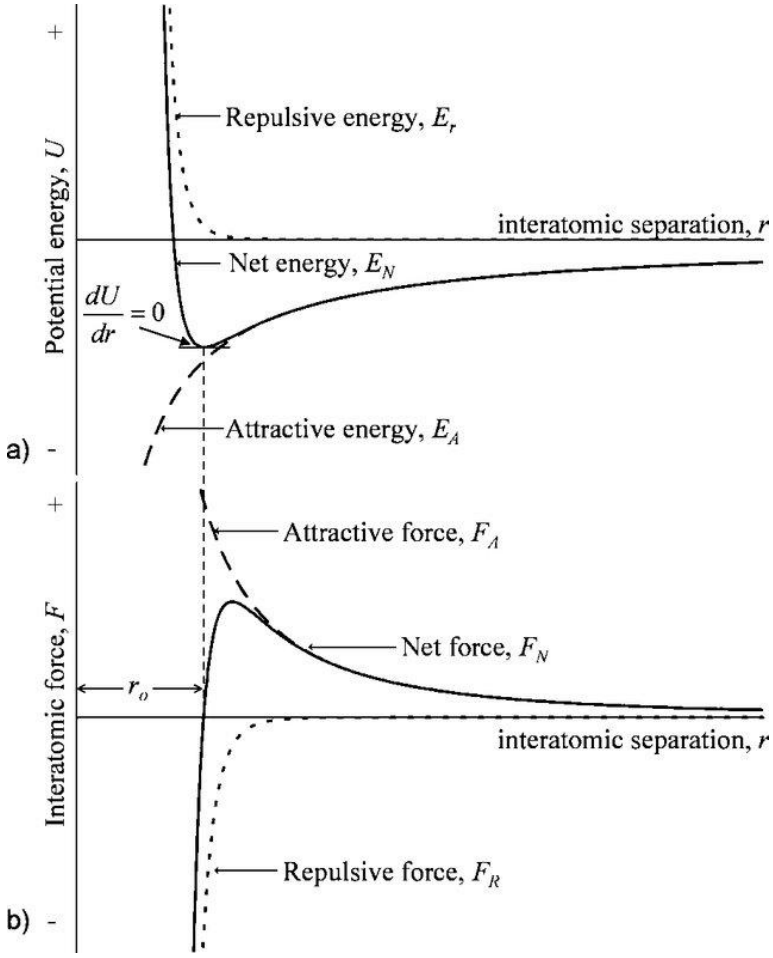

Figure 1.1 : Interatomic forces in a solid
(a) Net potential energy and (b) Interatomic forces between atoms as a function of interatomic separation, r. The distance with the lowest potential energy point where attractive force and repulsive force cancels out each other becomes the equilibrium lattice constant. Reproduced from reference 2.

The type of bonding determines the bond strength between the atoms and their binding energy, which is the minimum energy required to break the bond. The types of bonding can be divided into four groups depending on the major attractive force. v*an der Waals bonding* is characterized by the dipole formation, where atoms or molecules form dipoles and interact with adjacent dipoles, with a small attractive force. *Ionic bonding* is formed between positively and negatively charged ions, where Coulombic attraction dominates. As these types of bonding yield no loosely bound or free electrons, solids formed with ionic bonding are usually insulating. *Covalent bonding* arises when neighboring atoms share electrons existing at the outermost shell to close the orbital shell. Elemental semiconductors such as Si and Ge are covalently bonded. Compound semiconductors form dominantly covalent bond, but there exists a partial ionic bonding as well since atoms from in the different groups in the periodic table form the bond.[2] Finally, metallic bonding is when valence electrons are shared within many atoms, resulting in a high conductivity due to nearly free electrons in the solid.

1.2.2 Crystalline structure of III-V semiconductors

Crystallinity of the solids can be classified into three different types: Crystalline, polycrystalline and amorphous. If the solid shows long range periodicity of atoms without any disorder or boundaries, it is considered crystalline. If a solid shows multiple crystalline domains but each domain is oriented in a random manner, it is polycrystalline, where atoms in each domain remain crystalline. The solid is considered amorphous when there is no periodicity between the atoms.[3] Figure 1.2 shows the schematic illustration of three different types of crystallinity. Crystalline solids tend to have better optoelectronic properties such as minority carrier lifetime and mobility, but amorphous solids are also used in certain applications such as thin film transistors or solar cells due to the ease of fabrication and processing.[4]

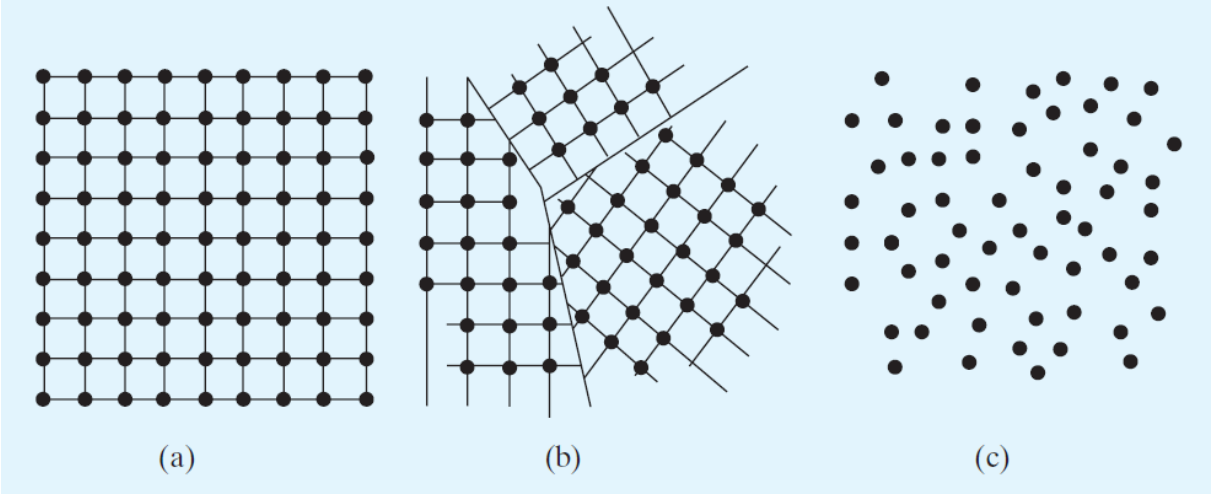

Figure 1.2: Schematic diagram of solids with different crystallinity.
Atoms are described as black dots, showing (a) crystalline, (b) polycrystalline and (c) amorphous solid. Reproduced from reference 3.

Most III-V semiconductors form single-crystal, zinc-blende structure which is similar to diamond structure of Si or Ge. Each atom is covalently and partially ionically bonded to 4 adjacent atoms as shown in Fig. 1.3. The structure is a diamond structure if a single type of atom comprises the crystal, and zinc-blende if two different type of atoms comprise the crystal. For III-V compound semiconductors, group III and group V atoms are placed adjacently, forming a zinc-blende structure. Some III-Vs such as GaN or InGaN form wurtzite structure.

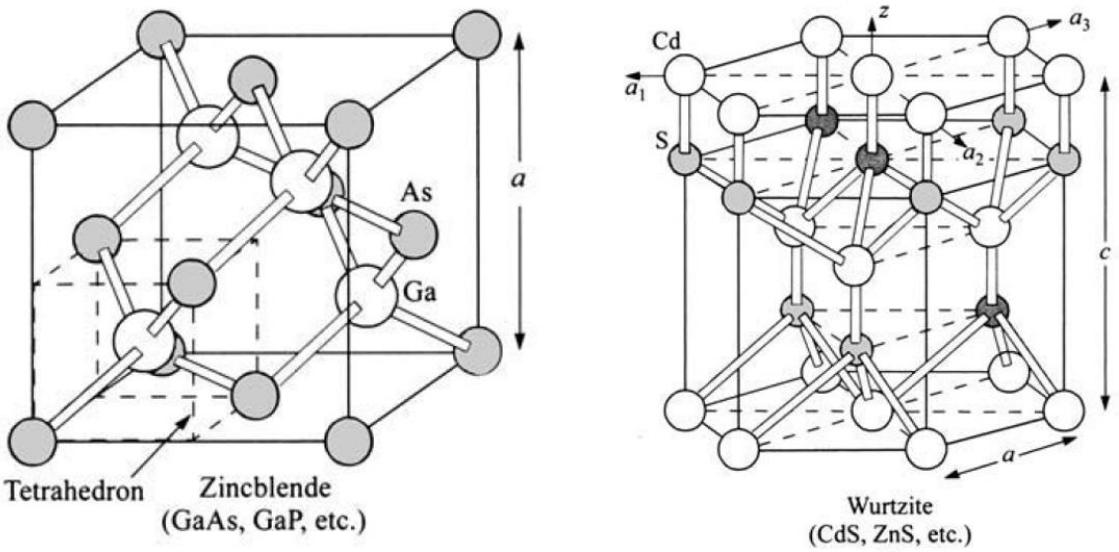

Figure 1.3: Zinc-blende and wurtzite structure
(Left) Zinc-blende structure (Right) wurtzite structure. Reproduced from reference 4

1.2.3 Bandgap and lattice constant of compound semiconductors

III-V semiconductors can form ternary or quaternary compounds, made up of three or four group III and group V atoms. Different fraction of atoms yield different lattice constants and band gaps, as shown in Fig. 1.4. Curves indicate a continuous and monotonic tuning of bandgap and lattice constant can be achieved. Since the growth of the material requires being lattice matched to the substrate, compounds between GaAs and AlAs, InGaAs and InP are of great importance, as GaAs and InP substrates are widely used for growth. Lattice mismatched compounds can be grown, but the thickness will be limited due to dislocation induced by strain coming from lattice mismatch.

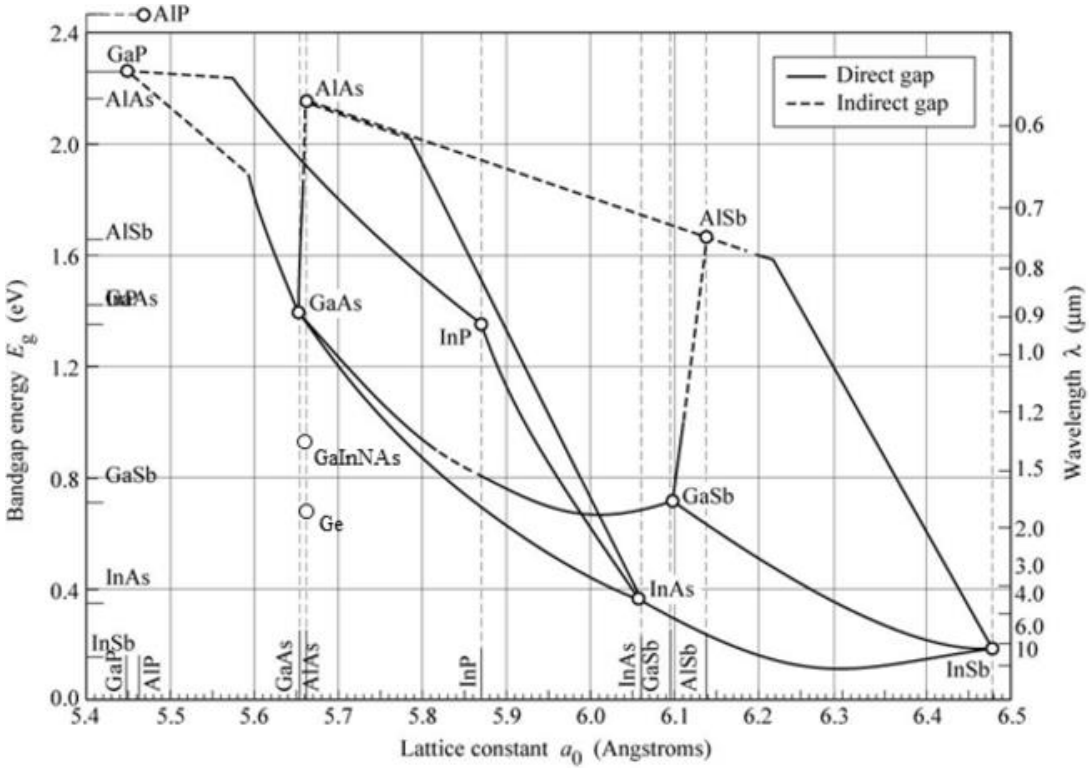

Figure 1.4 : III-V lattice map
Bandgap vs. lattice constant for common elemental and compound semiconductors. Solid line indicates direct bandgap materials and dashed line indicates indirect bandgap semiconductors. Vertical lines passing through InP, GaAs and GaSb indicate same lattice constant materials. Reproduced from reference 2.

1.3 Epitaxial growth

Epitaxy is a method to grow a single crystal layer on top of a single crystal substrate. Epitaxy can be used to grow diverse structures including junctions, quantum wells and doped layers. Most commonly used epitaxy methods are liquid phase epitaxy (LPE), vapor phase epitaxy (VPE) and molecular beam epitaxy (MBE). LPE was the first successful epitaxial process used to grow compound semiconductors. It grows a crystal on a parent substrate by precipitation of a crystalline phase from a saturated solution of the constituents.[2] LPE provides excellent purity of the resulting film, but is limited with fine control of the resulting layer thickness. VPE, also known as chemical vapor deposition (CVD), is currently most widely used growth technique in industry. Epitaxial growth results from a chemical reaction or decomposition from a gaseous ambient. Metal-organic VPE (MOVPE) uses metal-organic precursors for compound semiconductor growth and is widely used for its high throughput compared to MBE or LPE. Recently hydride VPE (HVPE) with extremely high growth rate was reported,[5] showing a potential for the next generation industry-scale growth technology.

MBE is widely used in research environments due to its flexibility of growth. Unlike VPE or LPE where growth occurs in equilibrium condition, MBE growth is done under nonequilibrium conditions, and is principally dominated by the surface kinetics. MBE is a vacuum thermal evaporation process under an ultra-high vacuum (UHV) environment with pressures under 10^{-10} torr[6]. For III-V compound semiconductor growth, elemental sources are used for group III to maintain ultra-high purity, instead of metalorganic sources used in the early days. Gas sources – phosphine (PH_3) for phosphorus and arsine (AsH_3) for arsenic – were used initially for group V elements. Gases were delivered from the source to the chamber through a cracker, which separated hydrogen atoms from phosphorus or arsenic atoms.[7] Growth kinetics are dominated by the amount

of materials being deposited from the source onto the substrate and the substrate temperature. Group V and III fluxes are measured and controlled using flux gauge. A schematic diagram of an MBE system configuration is shown in Fig. 1.5.

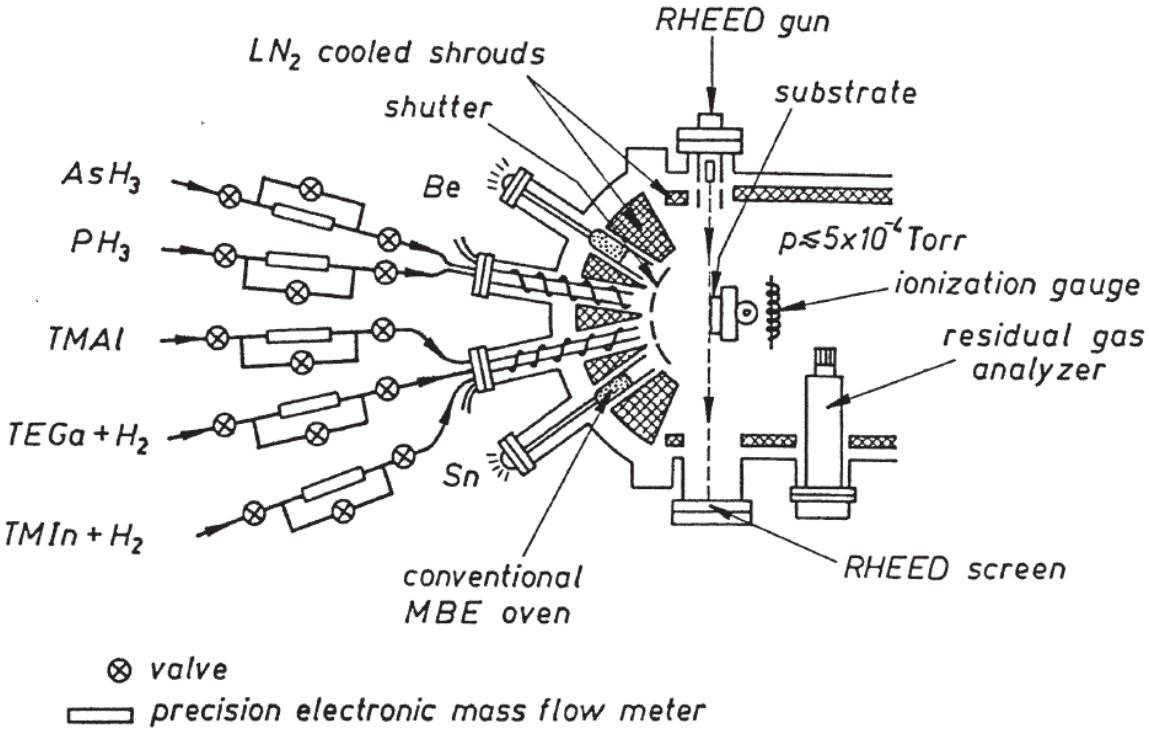

Figure 1.5 : A schematic diagram of MBE configuration
Elemental and solid sources can be used for group V sources as well. Liquid nitrogen shroud is used to keep the chamber pressure at a UHV condition. RHEED gun and screen is used for in-situ measurement of growth quality and rate. Reproduced from reference 6.

1.4 Energy harvesting and light detection applications

Optoelectronic devices use electrons to generate photons, or vice versa. Even though Si is the most widely used material in semiconductor circuits, its indirect bandgap limits its application to optoelectronic circuits. On the other hand, compound semiconductors are widely used in optoelectronics due to their flexibility in bandgap engineering and excellent optical properties from their direct bandgap. In this thesis, we mainly focus on light absorption applications – energy harvesting and light detection using III-V semiconductors such as GaAs or InGaAs.

1.4.1 Energy harvesting devices

One of the most widely used energy harvesting devices to date and photovoltaic cells. Solar cells operate by absorbing light using the semiconductor and separating the electron and hole at a junction and collecting them at the contacts. Most of the current commercial and industrial solar are dominated by Si.[8] However, compound semiconductor-based photovoltaics still hold world record in both single-junction and multi-junction cells.[9] The bandgap of GaAs (1.44eV) is almost identical to the ideal bandgap energy (1.43eV) to reach the thermodynamic limit.[10] Its high absorption direct bandgap allows for a few micron thick film to fully absorb the solar spectrum compared to few hundred microns required for Si. This enables a thin-film devices that can potentially be flexible and lightweight compared to bulky substrate Si devices. Combined with tunable bandgap and multijunction growth, compound semiconductor photovoltaics still have huge potential where cost is not a dominating factor, such as space applications or energy scavenging in small scale applications like wireless sensor nodes.

Thermophotovoltaic (TPV) cells utilize radiation from high-temperature thermal sources, similar to PV cells utilizing radiation from the sun. The major difference between TPV and PV is the source temperature and distance between the cell and the source.[11] Since the light source for a solar cell is always the sun, the view factor defined as the ratio between the radiation which leaves the surface of the source and which hits the surface of the PV cell is extremely small. The incident spectrum is fixed to the solar spectrum, which is a 5778K blackbody spectrum passed the earth atmosphere. On the other hand, for TPV applications, the distance between the emitter and receiver (cell) is not limited, and the emitter temperature also varies. Therefore, the optimal bandgap of the receiver material depends on the emitter temperature, and the view factor of the TPV cell can be as high as 1, which means all reflected or emitted photons from the cell can be re-absorbed from

the emitter. This gives engineering opportunity for device optical properties, especially the reflectance of out-of-band (OOB) photons,[12] which have lower energy than the TPV cell material bandgap. Also, varying the distance between the cell and the emitter also gives a potential for improving efficiency by near-field heat transfer, which utilizes evanescent mode photons from the emitter by placing the cell within a few tens of nanometers to the emitter.[13] Figure 1.6 shows a comparison between photovoltaics and thermophotovoltaics.

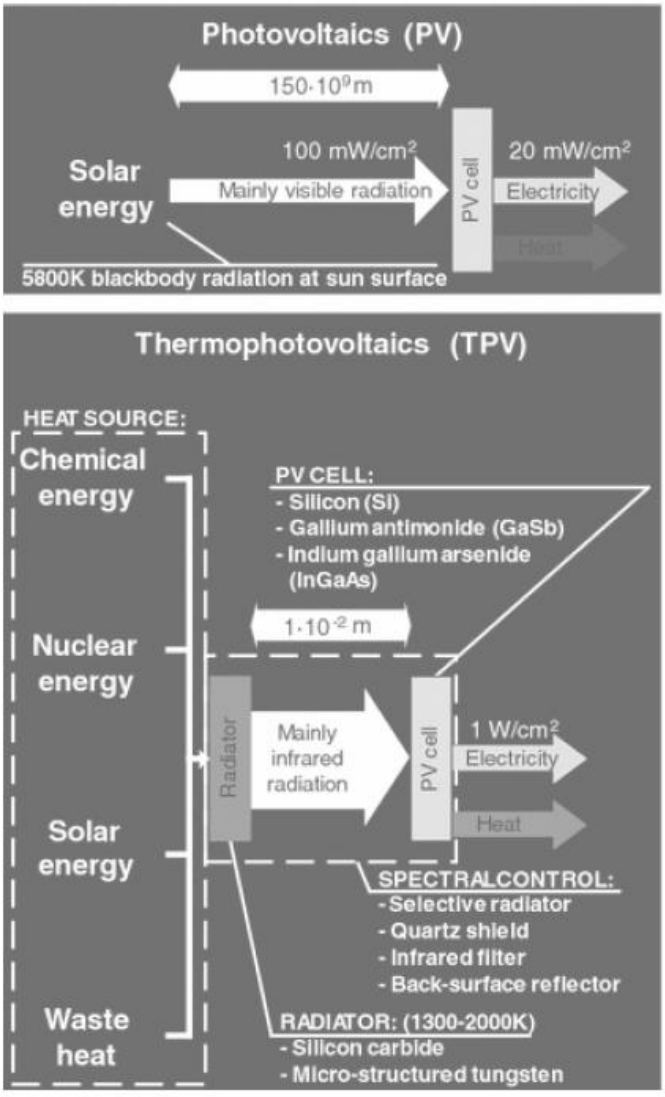

Figure 1.6 : Comparison between TPV and PV energy conversion
Reproduced from reference 11.

1.4.2 Light detection

III-V semiconductors are widely used in light detection applications due to their efficient light absorption from their direct bandgap and high electron and hole mobility.[2] There are major three different applications: photoconductors, avalanche detectors, and *p*-*i*-*n* photodiodes. Photoconductor comprise a slab or block of semiconductor with ohmic contacts at two ends. Due to the mobility difference between the hole and electron, the photoconductor can produce more than a single charge from an absorbed photon. Avalanche photodiodes utilize the avalanche effect from high reverse biased *p*-*n* junction. Both photoconductors and avalanche photodiodes result in a photocurrent gain. *p*-*i*-*n* photodiodes provide a wide bandwidth without gain due to a fully depleted *i*-region that can allow fast sweep of charges after light absorption. Photodetectors based on InGaAs lattice matched to an InP substrate dominate optical fiber communication receiver applications due to their high speed, reliability, sensitivity and low noise.

Chapter 1

Bibilography

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Chapter 2

Thin-Film Technologies and Substrate Reuse for III-V Semiconductors

As discussed in chapter 1, epitaxial growth of III-V semiconductors requires a crystalline substrate. Without additional process to separate and handle the active device layer, the initial substrate will always be the part of the resulting device. Separation of the active layer from the substrate can provide advantages in mechanical properties, device performance and degree of freedom in device engineering. Therefore, utilizing thin-film structures in III-V optoelectronics is crucial in achieving advanced, high-performance devices. Two important processes in achieving thin-film devices are bonding, and separation of the epitaxial active layer. Bonding the device active layer onto a secondary substrate allows simpler handling and fabrication of thin-film devices after the separation. Separating the device active layer can be done by inserting a sacrificial layer between substrate and device layer and selectively etching the sacrificial layer, or mechanically peeling the active layer from substrate. Both cases can be expedited with an assist of strain. The order of bonding and separation can vary, but bonding is usually performed prior to the separation since the secondary handle that is bonded on to the device layer can provide protection during the separation. After separation, the remaining substrate can be treated for subsequent growth, which can potentially reduce the cost of III-V optoelectronics. This chapter introduces different techniques used for bonding, separation and substrate recycling, as well as benefits of thin-film structures in compound semiconductor optoelectronics.

2.1 Advantages of thin-film optoelectronics

Thin-film optoelectronic devices have unique advantages in both mechanical and optical properties compared to conventional substrate devices. Replacing the substrate with secondary handle allows fabrication of flexible, lightweight devices on non-planar surfaces[1–8] and even on non-developable surfaces.[9–11] Non-developable differs from a developable surface, which is a smooth surface with zero Gaussian curve,[12] meaning a surface which can be acquired by transforming a plane without distortion. On the other hand, a non-developable surface exhibits a topological distortion when a plane is transformed to a 3D structure. Such deformation can be achieved by several different mechanisms such as stretching, buckling, or folding.[13–20] Advantages in optical performance will be discussed in more detail below.

2.1.1 Photon recycling

Photon recycling is a re-absorption process of photons generated within the semiconductor.[21] Re-absorption effectively increases the minority carrier lifetime, which can contribute to improved open circuit voltage (V_{oc}) of solar cells. Several literature reports the diffusion length and minority carrier lifetime in thin-film GaAs that was higher than measured values from the bulk GaAs.[21–23] Various optoelectronic devices including lasers and solar cells utilize photon recycling to achieve higher minority carrier lifetimes.[24–28]

According to the photon recycling model, The saturation current density (J_0) of a thin-film solar cell can be approximated by:[25]

$$J_0 = \mathrm{q}\frac{{n_i}^2}{N_A}\mathrm{W}\left[\frac{1}{\tau_{nr}} + \frac{1}{\varphi\tau_r} + \frac{S}{W}\right] \tag{2.1}$$

where τ_{nr} is the nonradiative carrier lifetime, τ_r is the radiative lifetime, φ is a photon recycling factor, W is width of the base layer, n_i is the intrinsic carrier concentration, N_A is the base doping concentration, and S is the back-surface recombination velocity. The equation indicates that photon recycling can reduce the dark current and thus increase the open circuit voltage, as the simplified relationship between V_{oc} and J_0 can be described as:

$$V_{OC} \approx \frac{kT}{q} \ln\left(\frac{J_{sc}}{J_0}\right) \tag{2.2}$$

Utilizing a thin-film structure can improve this effect by preventing the absorption of re-emitted photons at the bottom substrate.[21] Lundstrom, et al. demonstrated an improved minority carrier lifetime in a GaAs/AlGaAs thin film by removing the substrate.[27] Figure 2.1 shows the effect of improved photon recycling on minority carrier lifetime in a GaAs/AlGaAs thin film structure.

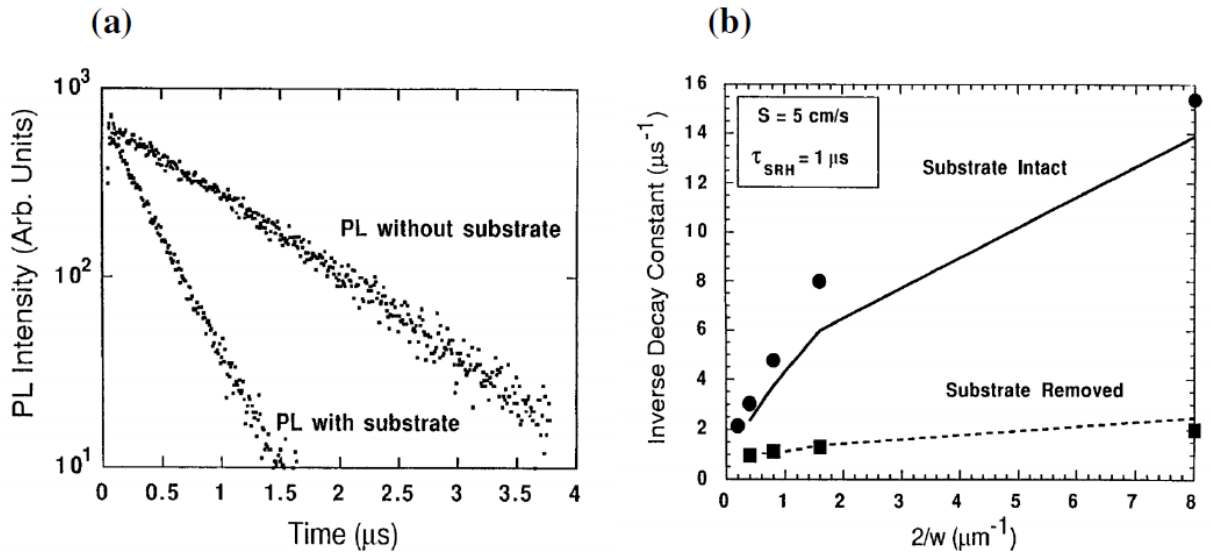

Figure 2.1 : Effect of substrate removal on minority carrier lifetime
(a) Transient photoluminescence measurement on GaAs/AlGaAs thin film with and without substrate. (b) Inverse decay constant extracted from TRPL measurement, with varying active layer thickness. Reproduced from reference 27.

2.1.2 Light trapping

Light trapping was initially proposed for Si photodetectors to improve its response speed using total internal reflection, while maintaining their external quantum efficiency (EQE) in the near-infrared (IR) range.[29,30] Light trapping structures using textured surface to overcome weak absorption in Si photovoltaics were also proposed.[31] A schematic illustration of light trapping increasing the light path is shown in Fig. 2.2. Given a refractive index of *n*, an ideal light trapping structure with perfect rear-side mirror and sufficiently textured surface can improve the internal intensity by $2n^2$.[29] This can enhance the total absorption by a factor of ~$4n^2$, by considering the angular average of oblique rays with a longer light path length.[29]

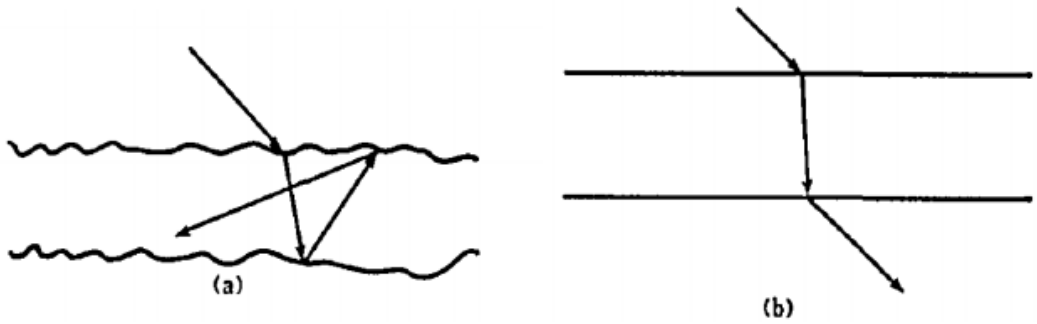

Figure 2.2 : A schematic illustration of effect of light trapping on light path
Light path within a semiconductor layer (a) with and (b) without textured surface. Reproduced from reference 29.

Improving absorption using light trapping was of little interest to the III-V photovoltaic community due to high absorption coefficient of compound semiconductors. Implementing back surface reflectors on a substrate grown device was also a technical challenge. However, with the techniques to separate and transfer the epitaxial layer from the crystalline substrate, light trapping structures with a back side reflector can be achieved. This can effectively double the optical path by reflecting the incident photons back into the cell active area, which can decrease the active layer thickness required to half that of the substrate device, and thus reduce the cost of overall growth process.[32,33] Moreover, a narrow escape cone near the surface due to high refractive indices of III-

V semiconductors naturally enhances the light trapping of internally generated or absorbed photons.

Light trapping with a rear-side metal reflector can benefit multiple optoelectronic devices including solar cells, photodiodes and light emitting diodes (LED). Photodiodes which mainly absorb NIR/IR with its longer absorption path compared to visible light can employ a relatively thin active layer by implementing back surface reflector, and thus improve the response speed. Light trapping can also improve the external quantum efficiency (EQE) of LEDs by reducing the absorption loss at the original substrate, by placing a rear surface reflector at the bottom of the device layer.[34]

Photovoltaic devices can specifically benefit from light trapping when combined with the photon recycling discussed above. Internally generated photons from recycling can be effectively confined within the device active layer. Since light trapping can also reduce the required active layer thickness for light absorption, bulk recombination loss in the active layer can also be reduced. However, back surface field layer (BSF) becomes more important in such structures since photogeneration near the back surface is increased due to thinner active layer thickness. Alta Devices, Inc. demonstrated a very high efficiency (28.8%) thin film GaAs solar cell which combined light trapping and photon recycling effect.[24] The comparison between substrate device and thin-film device with back surface reflector is shown in Fig. 2.3. Even with similar short circuit current densities, V_{oc} can be significantly improved with light trapping and photon recycling.

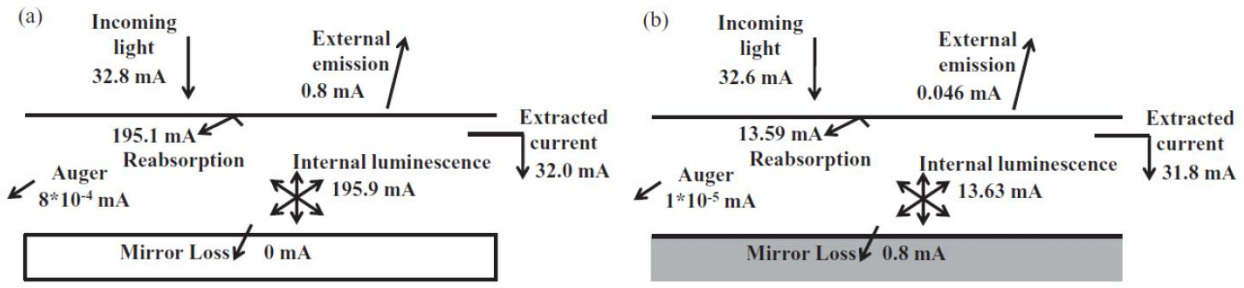

Figure 2.3 : Current at each operating point of photovoltaic cells
Photovoltaic cells with identical active layer structure (a) with back surface reflector and (b) with original substrate. Even with similar level of actual current output, back surface mirror device show improved V_{oc} due to photon recycling. Reproduced from reference 24.

2.2 Bonding

Bonding combines two different layers into a single body. It allows handling of the thin active layer after separation from the substrate and enables fabrication of thin-film optoelectronic devices on the secondary handle. High-process temperatures of conventional fusion bonding can easily exceed the glass transition temperature of a host substrate or induce strain and defects on the thin-film layer due to mismatch of thermal expansion between different layers. Here, we introduce several alternative bonding techniques that can be used for compound semiconductor thin-film technologies without compromising the material properties.

2.2.1 Van der Waals bonding

Van der Waals bonding utilizes the attractive intermolecular forces that are relatively weak compared to covalent or metallic bonding. It is a simple, low-temperature electrostatic process, but usually must be performed after the separation of the active layer due to its weak bonding forces. Therefore, an additional handle layer that can hold the epitaxial layer during the separation process increases complexity of processing. Its weak bonding forces can potentially limit the device fabrication process post-separation, due to risk of film damage during processes such as plasma etching. Yablonovitch, et al. demonstrated van der Waals bonding of thin-film GaAs

epitaxial layers onto arbitrary substrates.[35] They utilize attractive forces from a de-ionized water droplet which is placed between the thin epitaxial layer and handle substrate. By applying pressure and squeezing the water droplet out, the thin-film GaAs can be van der Waals bonded onto an arbitrary substrate.

2.2.2 Cold-welding

Cold-welding is a bonding process that brings two clean metal surfaces into contact and forms an intimate metallic junction.[18,36–39] Bonding happens when the spacing between atomically flat surfaces are brought within a critical thickness. Any type of surface defect or contaminants can hinder the bond formation, but this can be overcame with the assist of heat and pressure. Cold-welding is an ancient process which has been used since Mycenaean civilization, where shock pressure via hammering was used to bond a soft metal to a hard metal.[40] Smith et al. demonstrated Ni-Ni bonding by bringing two surfaces together and applying pressure across the interface.[36] Cold-welding of an Au-Au interface with a very low force with a support of elastomeric polymer even in the presence of ambient air and organic contaminants on the surface was demonstrated by Ferguson et al.[37] A schematic illustration of cold-welding process is shown in Fig. 2.4.

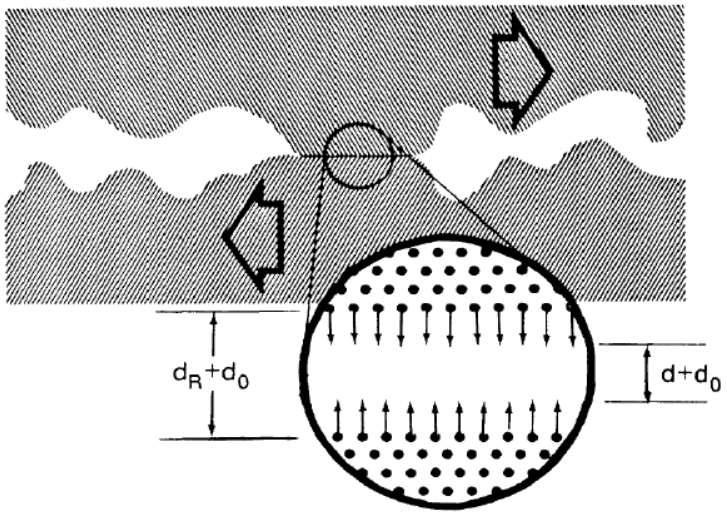

Figure 2.4 : Cold-welding within the metal interface
Two metallic surface can bond together when the separation at the interface are reduced below the critical thickness. Reproduced from reference 36.

Metal-metal interfaces in cold welding can be especially beneficial for thin-film compound semiconductor devices as metal formation on the surface for bonding can naturally act as a back surface reflector. This simplifies a process step for back metal mirror formation for photon recycling and light trapping. K.Lee, et al. demonstrated several different thin-film devices with back surface gold reflectors that used cold-welding to transfer the compound semiconductor onto a flexible substrate.[38,39,41]

2.3 Active layer separation

2.3.1 Epitaxial lift-off

Epitaxial lift-off (ELO) is the most widely used technology for separating the hin film device active layer from the growth substrate. It utilizes wet etching of a sacrificial layer grown between the substrate and device active layer. Choosing a sacrificial layer with high etch selectivity and preferably lattice-matched to the growth substrate is important for achieving efficient ELO. For GaAs based devices, AlAs or high Al-content AlGaAs layer are ideal sacrificial layers since they have extremely high etch selectivity in hydrofluoric acid (HF), and are lattice matched to GaAs. Lattice-matched InAlP layers can also be used with hydrochloric acid (HCl)[42], but can potentially limit the use of In-based layers such as InGaP in the device layer. For InP-based systems, AlAs layer can still be used as a sacrificial layer despite the lattice mismatch, as long as the layer thickness is kept ~10 nm to minimize dislocation defects.[41] InGaAs layers can also work as a sacrificial layer in the InP system since hydrogen peroxide and citric acid based etchants are selective to InGaAs. For Si thin film devices, HF can potentially work as a selective etchant of SiO_2 layer in Si-On-Insulator (SOI) wafers. However, device size could be limited due to H_2O produced during SiO_2-HF reaction diluting the HF concentration near the interface.

Despite the careful selection of sacrificial layer material with sufficiently high etch selectivity, ELO can usually take several hours to even days depending on the size of the sample. This is a shortcoming of a lateral etch process, where the etch needs to be done through 10-35 nm of sacrificial layer thickness. And often the opening can be blocked during the etching by a flexing of thin-film layer or bubble formed by the etch byproduct gas. To minimize such risk and expedite the process, several different modified versions of ELO have been developed. One common method is weight-induced ELO (WI-ELO), which attaches either a heavy weight or a cylindrical roller onto the flexible substrate that holds the epitaxial active layer.[33] The weight or rolling keeps the partially separated epitaxial layer bent away from the substrate, to ensure the exposure of the remaining sacrificial layer to the etchant. Another method to keep the epitaxial layer separated from the substrate is to utilize the surface tension of the etchant solution, where the separated epitaxial layer floats on the surface while the substrate is still submerged in the solution.[42] Process schemes of WI-ELO and surface tension assisted ELO are shown in Fig. 2.5.

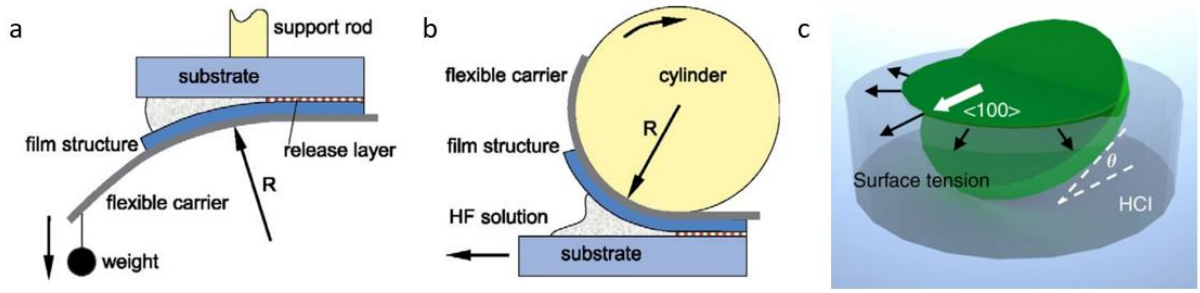

Figure 2.5 WI-ELO and tension-assisted ELO
A schematic diagram of (a) Weight-induced ELO, (b) Cylinder-assisted ELO and (c) Surface tension-assisted ELO. All processes keeps the edge of remaining sacrificial layer exposed to the etchant solution

Even if the WI-ELO or tension-assisted ELO can help prevent the blockage of sacrificial layer opening, ELO time is still limited by the size of the substrate, and longer exposure time at the edge can potentially induce surface damage of the epitaxial layer. One way to avoid this especially in scaling up to larger substrate can be pre-patterning the device mesa area so that the sacrificial layer

at the inner part of the wafer is also exposed in the etchant.[44] Figure 2.6 shows a process step for pre-patterned ELO and the resulting epitaxial thin film layer bonded onto secondary handle.

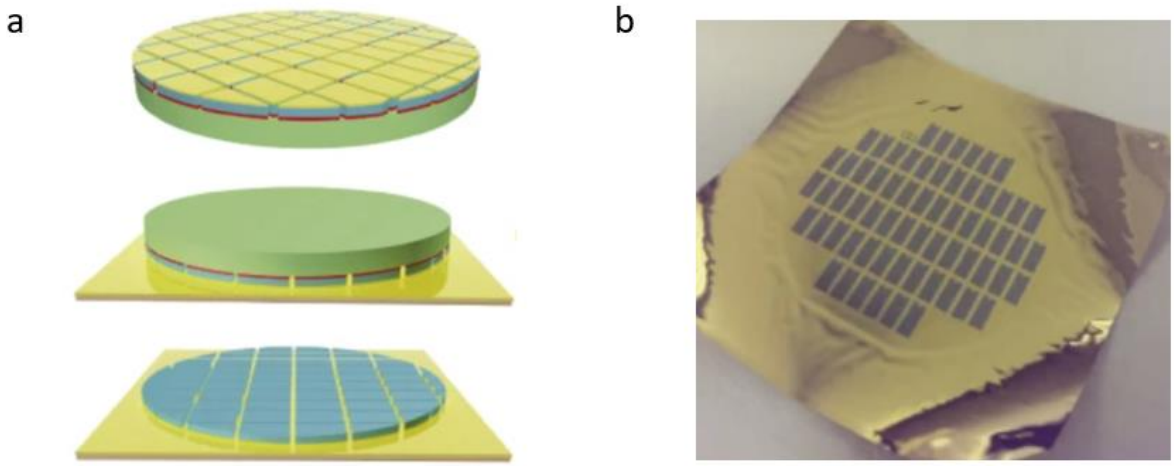

Figure 2.6 : Pre-patterned ELO
(a) A schematic of pre-patterned ELO process flow. (Top) Epitaxial layer and Au patterned after the growth and deposition. (Middle) Pre-patterned epitaxial layer cold-welded onto secondary handle layer coated with Au (bottom) Epitaxial layer transferred onto the secondary handle, after ELO process. (b) A picture of array of GaAs mesa transferred onto handle layer, resulting from pre-patterned ELO process. Reproduced from reference 45.

2.3.2 Mechanical spalling

Mechanical spalling is a method to separate a thin-film semiconductor layer by propagating a spalling mode fracture within the substrate, parallel to the surface. [45–47] A tensile stress layer and flexible handle that guides the fracture front is required. Figure 2.7 shows a process flow of mechanical spalling and the resulting device. As this process does not include a wet etching step, the material choice is not limited by the etch selectivity and lattice-matching of the sacrificial layer. Thin-film layers besides GaAs, such as Si or Ge, have been demonstrated.[45] However, spalling tends to leave a rough interface after separation, thus achieving smooth surface for optoelectronic device fabrication or substrate reuse may be tricky.[46,48]

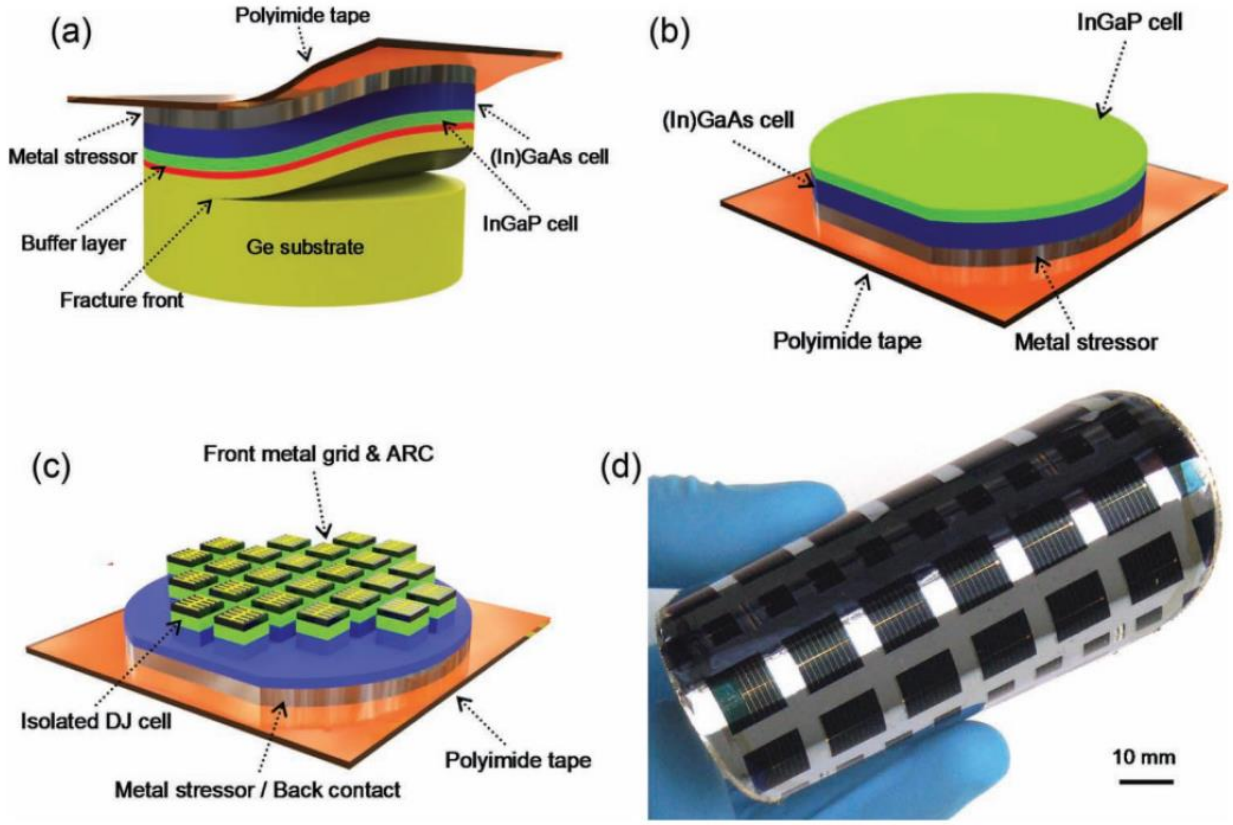

Figure 2.7 : Illustration of controlled spalling process and picture of fabricated thin-film solar cells.
A schematic of (a) structure used in controlled spalling process. (b) lifted-off thin-film layers bonded on polyimide tape. (c) fabricated thin-film solar cells on flexible substrate. (d) Photograph of fabricated thin-film tandem solar cells on flexible substrate. Reproduced from reference 46.

2.3.3 Laser lift-off

Laser lift-off (LLO) is a technique that uses short-wavelength excimer laser to decompose the sacrificial layer, instead of wet chemical etching used in ELO. Sacrificial layers used in LLO need to have a lower bandgap compared to the substrate and device layer. This allows selective, strong absorption of laser light in the sacrificial layer, while other layers remain transparent to the laser wavelength. LLO of GaN and InGaN from sapphire substrates,[49–52] or InP layers from InP substrate using an InGaAs sacrificial layer[53] has been demonstrated. One potential issue is that the strong absorption by the sacrificial layer increases the temperature of the interface, and thus roughening or even decomposing the active layer surface.[49–52] Also, for systems where low-

bandgap material is inaccessible, a metal layer that blocks the laser light to protect the active layer material is required, which can increase the complexity of fabrication.[49]

2.4 Substrate recycling

After active layer separation, the remaining substrate can potentially be reused for subsequent growth. This can potentially reduce the manufacturing cost of optoelectronic devices by reducing the cost of the substrate by the number of cycles. This can be of less interest for applications with small device size such as photodetectors or LEDs. However, applications that require large-area devices such as solar or thermal energy harvesting can experience manufacturing cost reduction via substrate reuse.[44,54,55] Therefore, understanding surface contamination mechanisms of GaAs substrate during ELO process is crucial for successful substrate recycling. The GaAs layer is slowly etched in HF solution during the ELO process and a thin layer of As is generated on the surface as an etch byproduct.[56] The As layer can react with H_2O molecules in ambient environment and form As_2O_3 micro-crystallites, possibly due to convection diffusion of AsO_2^- ions.[57,58] This can be accelerated by light exposure, possibly due to photogenerated electrons participating in the reaction.[59,60] Figure 2.8 shows a schematic diagram of the GaAs contamination mechanism. Results suggest ELO processing in the dark and removal of thin As layer immediately after the ELO is important for effective substrate recovery.

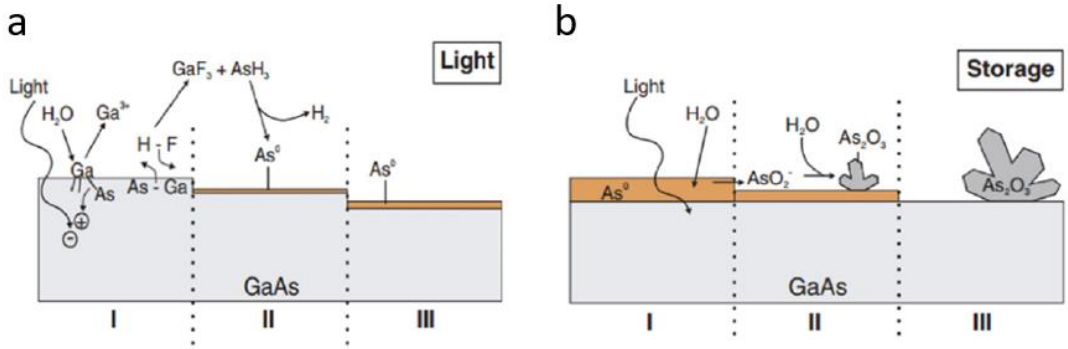

Figure 2.8 : Surface contamination mechanism of GaAs during and after ELO
Schematic illustration of GaAs wafer with (a) HF exposure under light (b) Stored after ELO, under ambient condition. Reproduced from reference 56.

2.4.1 Chemical and Chemo-mechanical polishing

Chemo-mechanical polishing (CMP) is a method to recover an epi-ready growth substrate by combining chemical and mechanical polishing. This can provide a smoother and cleaner surface compared to conventional recovery methods of chemical polishing.[61,62] CMP processed wafers show almost identical device performance to the fresh grown devices, while chemically polished wafers exhibit significant degradation. This is mostly due to surface roughening of the GaAs substrate during ELO, which is difficult to recover by chemical polishing. Figure 2.9 (a) and (b) shows different mixtures used for chemical polishing and device comparison between regrowth after ELO processing and chemical polishing and CMP. Despite the effective recovery of the original substrate, CMP may not be an ideal candidate for wafer reuse due to substrate thinning during the process, which can ultimately limit the number of total cycles.[54,61] Processing cost is also high.

a

Constituents	Volume ratio	R_a (nm)		
		Etchant	Anneal	Buffer
$H_2SO_4/H_2O_2/H_2O$	1:1:10	0.8	—	—
Br_2/CH_3OH	1:99	0.4	—	—
$NH_4OH/H_2O_2/H_2O$	2:1:10	0.5	0.4	0.2
$NH_4OH/H_2O_2/H_2O$	1:1:50	0.9	0.4	0.2
$HCl/H_2O_2/H_2O$	1:1:30	2.4	0.8	0.4
$NH_4OH/H_2O_2/H_2O$ +	1:1:50	0.8	0.7	0.3
$HCl/H_2O_2/H_2O$	1:1:30	—	—	—
$HCl/H_2O_2/H_2O$ +	1:1:30	1.5	1.3	0.5
$NH_4OH/H_2O_2/H_2O$	1:1:50	—	—	—
$HCl/H_2O_2/H_2O$ +	1:1:30	2.4	1.7	1.7
$NH_4OH/H_2O_2/H_2O$	2:1:10	—	—	—

b

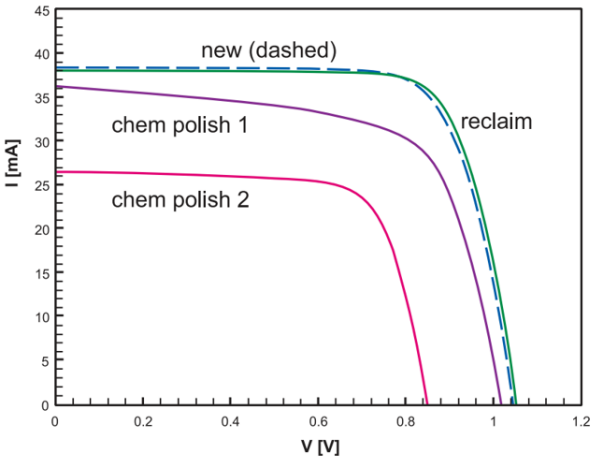

Figure 2.9 : Substrate cleaning after ELO process
(a) A table of chemicals used for chemical polishing of ELO processed GaAs wafer. (b) Current-voltage characteristics of thin-film GaAs photovoltaic cells grown on fresh, chemical polished, and chemo-mechanically polished wafers. Reproduced from reference 61.

Avoiding HF-based etch chemistry can potentially resolve the issue of surface roughening during ELO. Cheng, et al.[42] demonstrated an ELO process with InAlP sacrificial layer and HCl etchant. As the GaAs surface is passivated under HCl solution, the surface is kept smooth and

clean. Figure 2.10 shows a comparison between HF-based and HCl-based ELO processes. Even though such process can achieve a smooth substrate surface after the ELO, HCl-based chemistry can potentially etch any type of In-based layer within the active device layer as well. This ultimately limits the choice of growth structures, or adds a complexity of processing for sidewall passivation to protect the In-containing layers.[39]

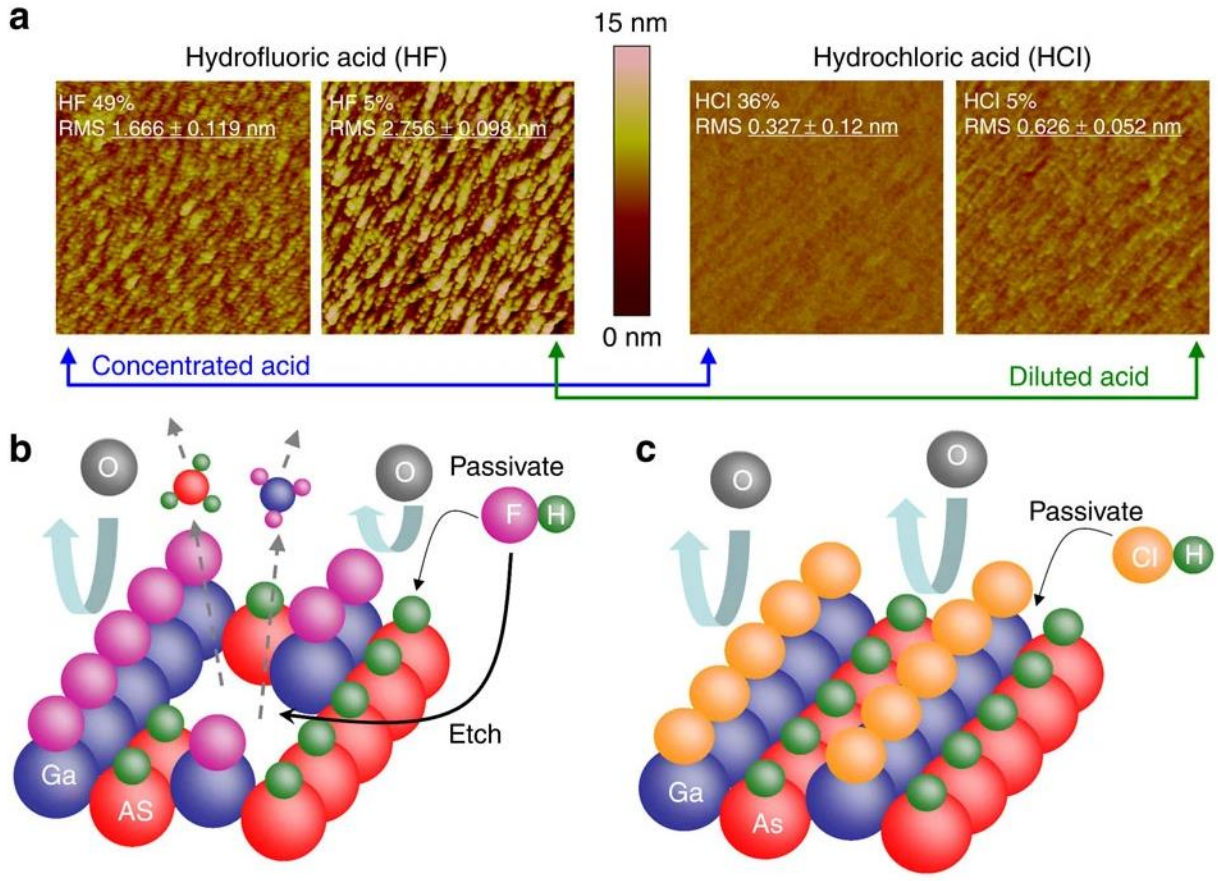

Figure 2.10 : Comparison between HCL and HF based ELO process
(a) AFM images of the substrate surface after the ELO process, and schematic illustration of surface chemistry during (b) HF-based and (c) HCl-based ELO process. Reproduced from reference 42.

2.4.2 Non-destructive ELO

Non-destructive epitaxial lift-off (ND-ELO) uses an additional epitaxial protection layer between the substrate and sacrificial layer, and keeps the original substrate from being etched or contaminated during ELO.[38,39,41] By combining more than two protection layers, a smooth

substrate surface can be recovered even with the surface contamination at the top of the protection layer during ELO. An ND-ELO structure including device active layer, sacrificial layer and protection layer is shown in Fig. 2.11(a). Various devices including photovoltaics and LEDs were tested after multiple regrowths, and no performance degradation was observed. Performance of GaAs photovoltaic cells with a different number of regrowths is shown in Fig. 2.11(c). As high etch selectivity between each layer and wet etching is enough for recovering a clean surface of the bottom substrate, this process can potentially become more economic and robust compared to CMP.

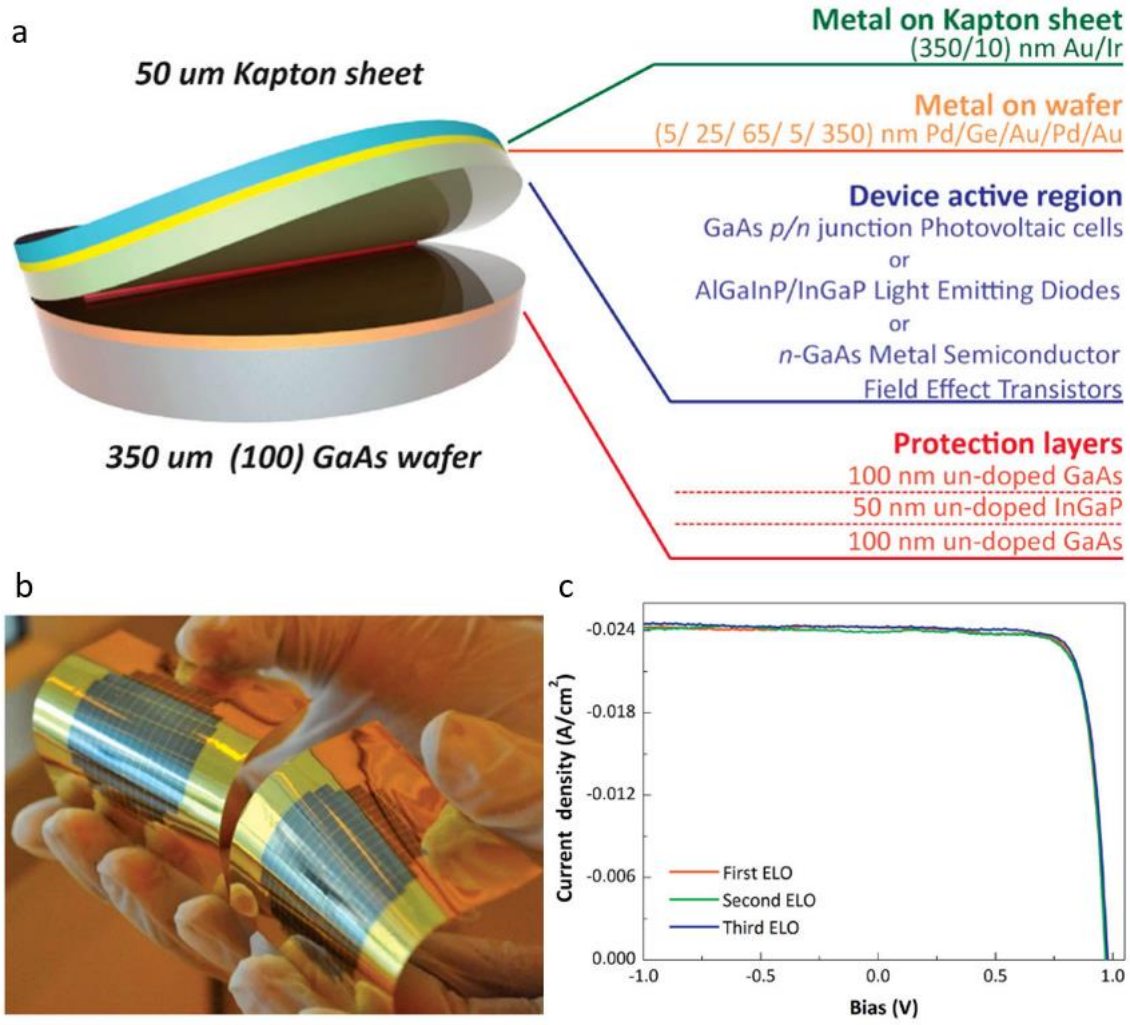

Figure 2.11 : ND-ELO processed GaAs photovoltaics
(a) A schematic illustration of ND-ELO structure with GaAs photovoltaic cell, sacrificial layer and protection layer. (b) Photograph of fresh grown and regrown GaAs PV cells (c) *J-V* characteristic of GaAs PV cells with different number of regrowth. Reproduced from reference 39.

2.5 Summary

This chapter briefly introduced advantages of thin-film optoelectronics both in device performance and potential cost reduction, especially in III-V semiconductors. After the growth, the wafer needs to go through additional process steps including the bonding of the device active layer onto a secondary handle, and separation of the device active layer. Using a sacrificial layer and selective etching, ELO is a commonly used process for device layer separation. Chemical or chemo-mechanical polishing can be used for surface cleaning of the remaining substrate for subsequent growth, but has its own limits in terms of regrowth quality or number of recycling steps. ND-ELO can potentially overcome such difficulties by introducing an epitaxial protection layer before the growth of the sacrificial layer. Efforts on scaling up the ND-ELO process from 2" wafers to 4" wafers will be further discussed in chapter 3.

Chapter 2

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Chapter 3

Non-Destructive Epitaxial Lift-Off on 4-inch GaAs Substrates

Compound semiconductors can almost always be found in high-performance optical and high-power devices in modern electronics. Despite their superior material properties, widespread use in commercial applications has been limited mostly due to expensive substrate costs compared to elemental semiconductors, mostly Si. As discussed in chapter 2, substrate reuse of III-V semiconductors, especially GaAs has been intensively studied. With epitaxial lift-off and chemo-mechanical polishing (CMP) of the remaining wafer, successful regrowth has been reported. To overcome the potential limitations of wafer thinning during the CMP, non-destructive epitaxial lift-off (ND-ELO) has been developed. Implementing an epitaxial protection layer structure and substrate cleaning via dry and wet etching allowed successive regrowth of devices on 2” GaAs substrates without any device performance degradation or substrate damage. While ND-ELO is a promising candidate for substrate recycling, scaling up to larger area wafers is crucial in achieving high throughput in manufacturing. In this chapter, we discuss our effort and challenges on scaling the ND-ELO process up to 4 inch GaAs wafers.

3.1 Introduction

Expensive wafer costs of compound semiconductors such as InP or GaAs hinders their widespread use in optoelectronics. One of the promising and important methods to overcome such challenge is substrate recycling by separating the device active layer from original substrate. Various

methods of active layer separation have been researched, including mechanical spalling,[1–4] laser lift-off (LLO)[5–7] and epitaxial lift-off (ELO).[8–11] Mechanical spalling uses a strain layer to mechanically cleave the part of the substrate, but can potentially leave a kerf on the separation interface, and achieving precise control of the separation position can be tricky. [1–4] LLO uses strong absorption from laser light to decompose the sacrificial layer, but heat from the absorption process can potentially damage the device active layer, and often limits the selection of device layer material or requires additional processing to selectively absorb the laser light from the sacrificial layer. [5–7] ELO uses a wet etching process to selectively remove the sacrificial layer. In GaAs or InP based system, an AlAs sacrificial layer with HF etching is widely used. Even with high etch selectively, device active layers and substrate surfaces can slowly be etched [12–14]

After active layer separation, the remaining substrate can be treated for regrowth. Among different separation techniques, substrate recycling after ELO has been demonstrated with several different cleaning methods including chemical polishing,[9] chemo-mechanical polishing (CMP)[9] and addition of epitaxial protection layers.[10,14,15] Non-destructive epitaxial lift-off (ND-ELO) allows multiple regrowths of GaAs optoelectronic devices without performance degradation by growing protection layer both on the substrate and device active layer, and using dry and wet etching to recover the original substrate after the ELO.[10] Such processes have been demonstrated on 2" wafers, which are mostly used in a research laboratories. Scaling the ELO and substrate recycling process can be tricky as the lift-off time increases as substrate gets larger. Yet this is an important goal to achieve manufacturing cost reduction of III-V based optoelectronic devices. In this chapter, we demonstrate our effort to scale the ND-ELO process to 4", MOCVD grown wafers, in collaboration with SolAero, Inc. ND-ELO still shows excellent surface recovery at a microscopic scale even with different growth technologies and orientation of the wafer. GaAs

single junction solar cells show identical performance after regrowth, while there remains a potential problem of particle generation control and edge contamination.

3.2 ND-ELO process

Growth of GaAs/InGaP/GaAs (100/100/500nm) protection layer, AlAs (25nm) sacrificial layer an GaAs single junction photovoltaic active layer was grown via MOCVD at SolAero, Inc. An Ir/Au (0.5/200nm) layer was coated on a 25μm thick Kapton® polyimide film, and 200nm Au was deposited on the GaAs wafer after buffered HF treatment for oxide removal. The wafer was bonded onto the Kapton® substrate by cold-welding, under 10^{-4} Torr, 30kN and 200°C for 5 minutes. The bonding process and image after the bonding are shown in Fig. 3.1.

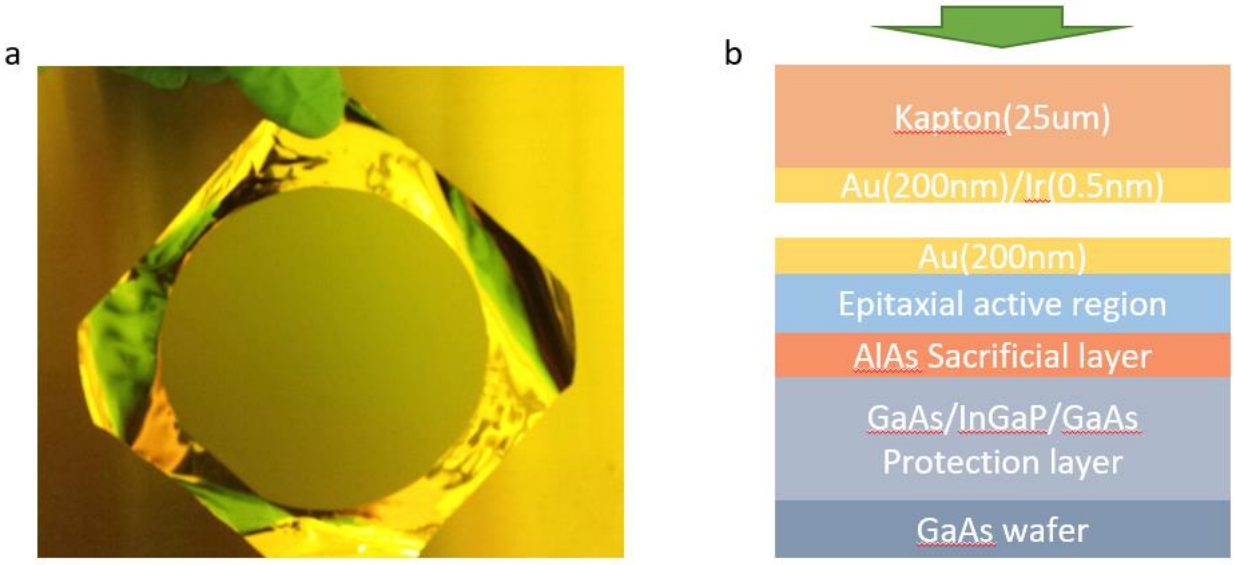

Figure 3.1 : ND-ELO process flow
(Left) Metallization and bonding process for 4" GaAs substrate. (Right) Epitaxial layer transferred onto Kapton® substrate, and remaining original GaAs substrate.

After the bonding, the structure was submerged in 16.7% 60°C HF, with the flexible substrate side up. For a full 4" substrate, the lift-off process took ~12 hours to fully etch the AlAs sacrificial layer. Both the substrate and the epitaxial film were immediately rinsed with DI water and transferred into 80°C RemoverPG solvent to prevent As_2O_3 formation.[12,16] Epitaxial film

transferred on to a Kapton® substrate and a separated original GaAs substrate are shown in Fig.3.2. Thin film epitaxial layers were stored in ambient for future comparison with regrown wafers. GaAs substrates were further processed for protection layer removal and regrowth.

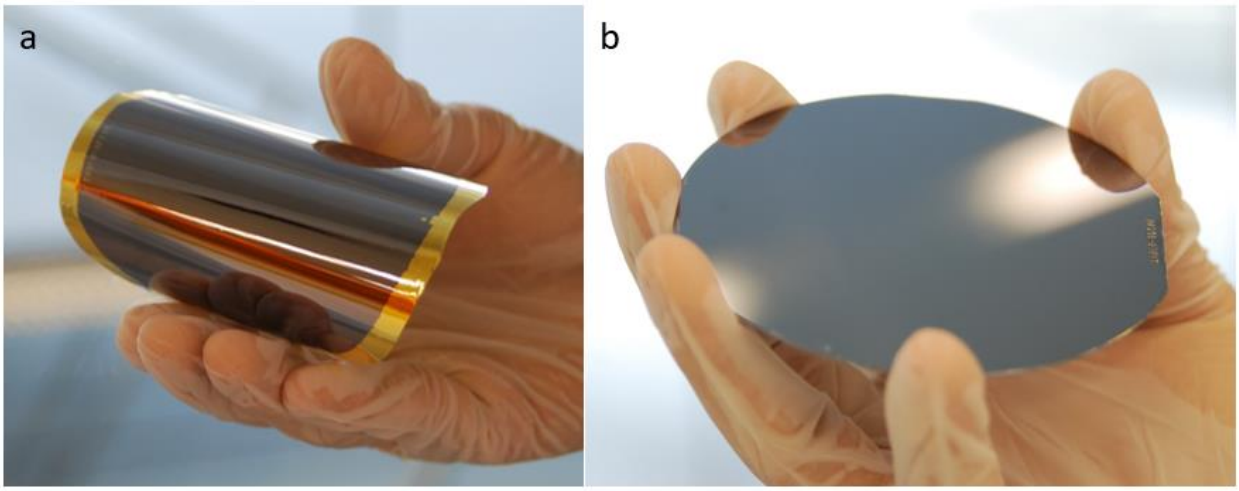

Figure 3.2 : Thin-film epitaxial layer separated from original GaAs substrate
Photo image of (Left) epitaxial thin-film layer transferred onto Kapton® substrate and (Right) GaAs substrate after ND-ELO process.

3.3 Substrate cleaning

After ND-ELO, the protection layer was etched to recover the GaAs substrate. As_2O_3 formation on the surface during ELO can act as a mask during wet etching of the GaAs/InGaP protection layer.[10] BCl_3/Ar plasma was used to etch ~120 nm of top GaAs layer. The remaining GaAs layer was etched using $NH_4OH:H_2O_2:H_2O$ (3:1:25) solution, reaching InGaP. High etch selectivity ensures a smooth InGaP surface across the wafer, even with different HF exposure times across the wafer. A 100 nm thick InGaP layer was then etched using $HCl:H_3PO_4$ (3:1) solution. Figure 3.3 shows atomic force microscopy (AFM) measurement results after each step of ND-ELO and protection layer removal. Small particle spots observed right after ELO are removed after the plasma clean, and the surface roughness due to plasma etching was recovered by wet etching and etch selectivity between InGaP and GaAs.

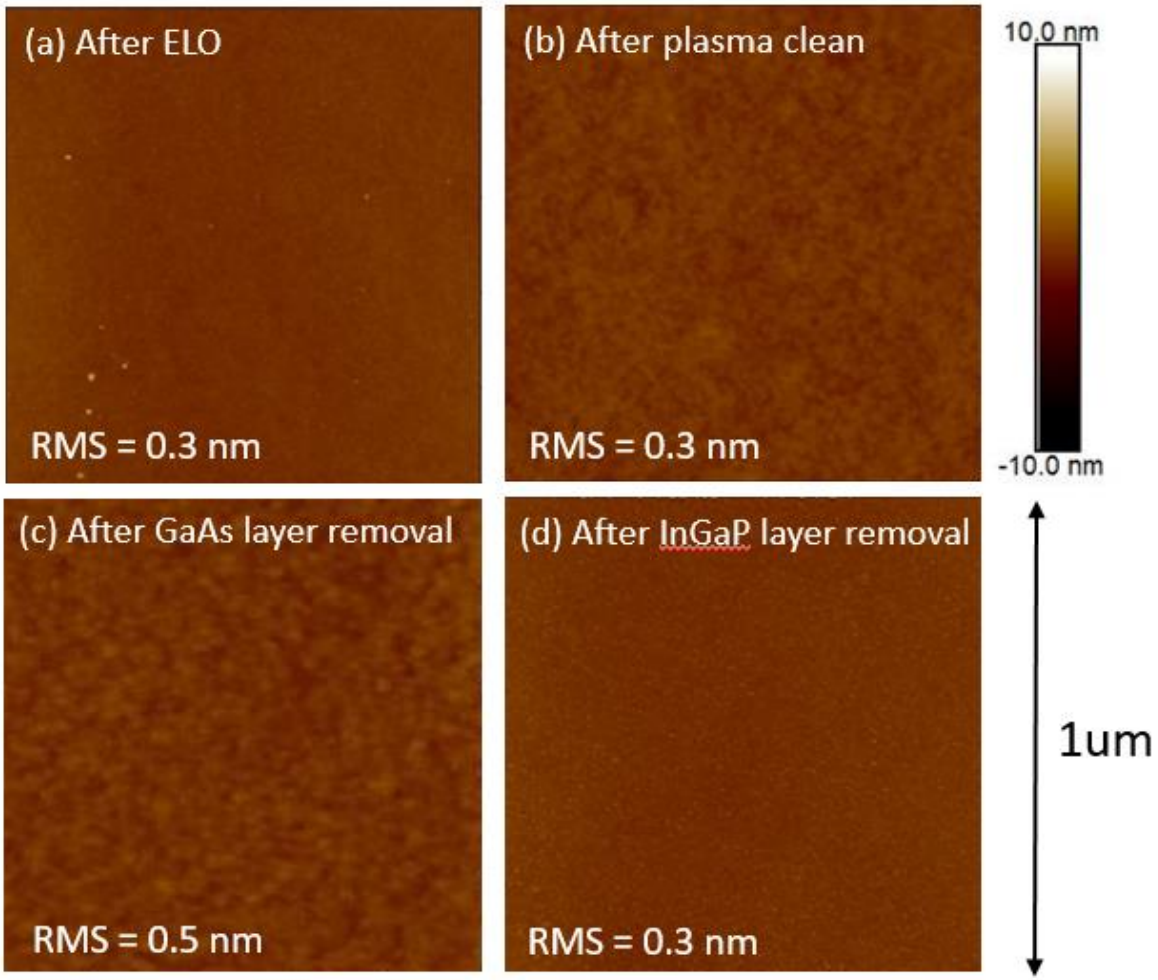

Figure 3.3 : AFM measurements during ND-ELO and substrate cleaning
(a) After ELO (b) After plasma etching top GaAs protection layer, (c) After wet etching of remaining GaAs layer (d) After wet etching of InGaP layer, reaching GaAs surface

After successfully removing the protection layer and reaching the smooth GaAs surface, X-ray photoelectron spectroscopy (XPS) was measured on the surface to ensure the recovery of GaAs surface without any contaminants. Figure 3.4 shows the XPS measurement of both fresh and cleaned GaAs substrates after ND-ELO and protection layer removal. The peaks align well without additional contaminants on the surface. Combined with the AFM results, this confirms the compatibility of the ND-ELO process for substrate recovery at a microscopic scale, even with much longer exposure in the HF solution. Yet this is not sufficient for complete wafer recycling, as macroscopic scale contaminants such as particle generation is another important issue.

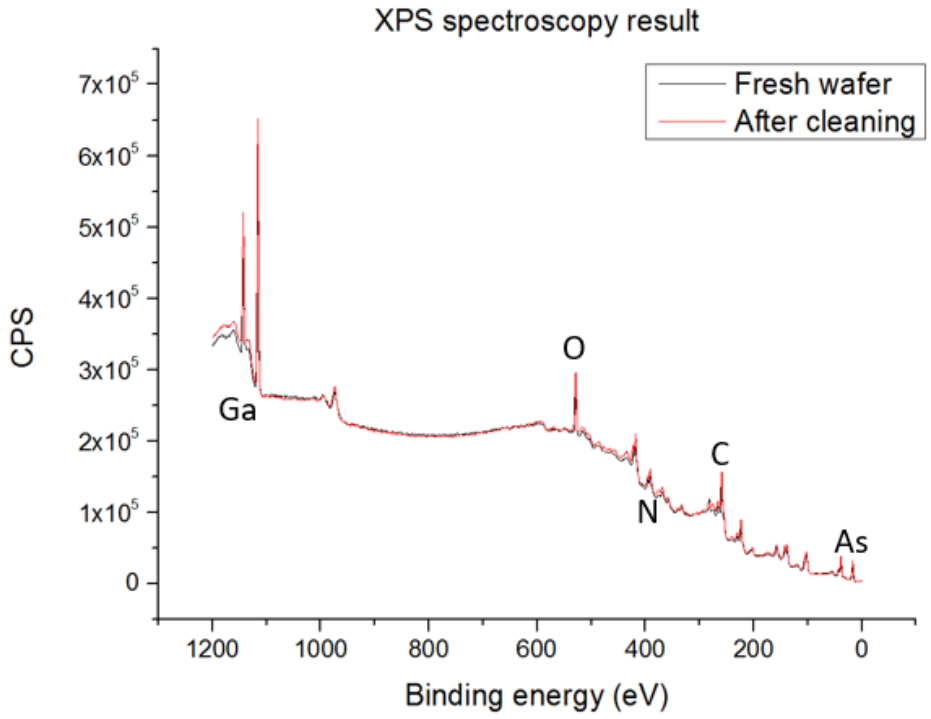

Figure 3.4 : XPS measurement of GaAs substrate after protection layer removal

A full wafer surface scan is ideal for measurement and characterization of particle or haze generation on the surface. Laser scans that map particle size and location on the wafer were performed at SolAero, Inc. After the surface scan, the wafer was prepared for subsequent growth, and initial structure was grown for the second time on the cleaned wafer. Figure 3.5 shows the surface scan data after the substrate cleaning. Colors indicate the diameter of particles, varying from 20µm to 60µm. Area colored in navy indicate haze formation. After initial round of ELO and protection layer removal, a total of 17 particles were observed via surface scan. This is a modest increase compared to 5-10 particles on fresh wafers, but still acceptable for growth. We expect the bonding process and peeling-off at the center during the ELO could potentially contribute to the particle accumulation on the wafer.

As different measurements had to be done in the different labs, shipping samples back and forth and moving in and out of cleanroom environment could also have affected the particle generation in multiple iterations. Although such conditions may sound trivial and mundane,

keeping them well controlled while collaborating with the laboratories in two different locations was difficult and slowed down the iteration process.

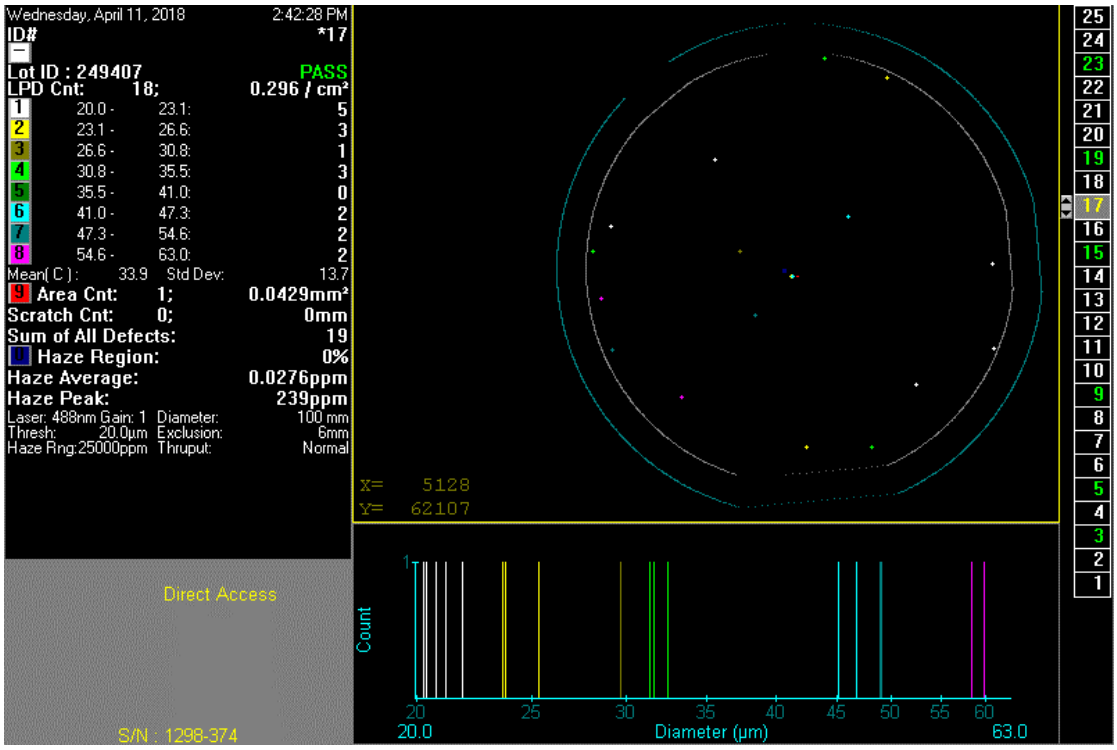

Figure 3.5 : Surface scan measurement on 4" GaAs wafer after protection layer removal
Data acquired from SolAero, Inc.

3.4 Device fabrication

GaAs photovoltaic cells were fabricated with the epitaxial film lifted off from the initial regrown wafer. ND-ELO process including bonding was performed on the regrown wafers, and device fabrication was done at the same time with the fresh epitaxial layer films stored after the initial ND-ELO. Device fabrication processes and images at each step are shown in Fig. 3.6. After lift-off and storing in RemoverPG, the protection layer was removed via same process described above. Then, mesa patterns were defined using standard photolithography and wet etching of device layers. Top metal contact was patterned using standard photolithography and metal lift-off

process. After the contact deposition, GaAs contact layer was removed using wet etching, while the metal contacts served as an etch mask.

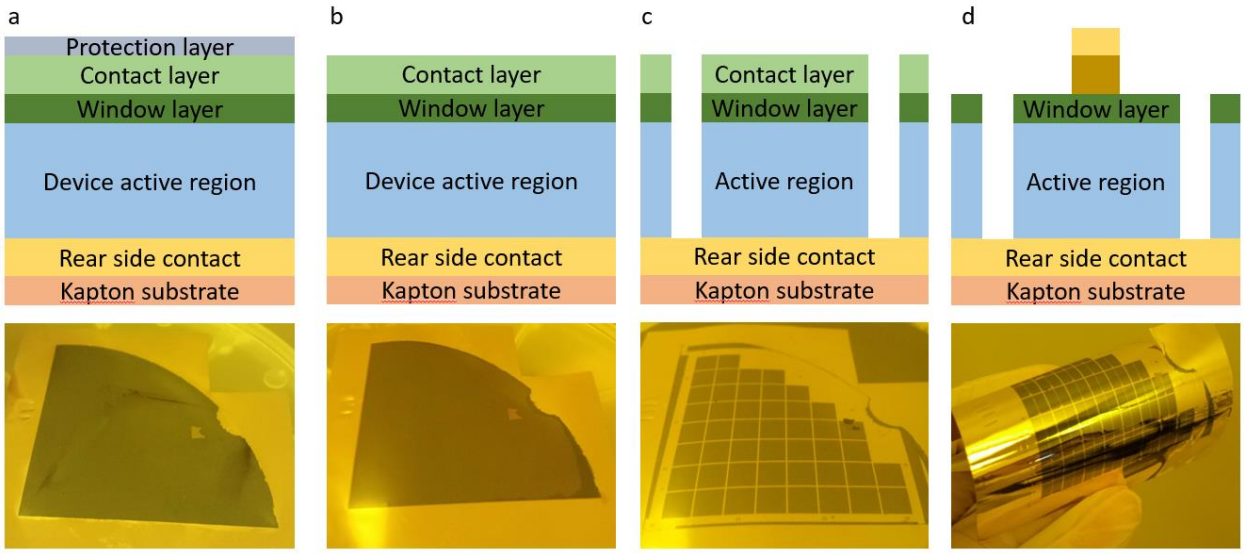

Figure 3.6 : Thin-film GaAs PV fabrication
A schematic diagram and photo image at different steps of GaAs PV cell fabrication. (a) Right after ND-ELO and storage in removerPG (b) Protection layer removal (c) Mesa patterning (d) Top contact deposition and contact layer removal. Photos were taken during the demo cell fabrication using quarter-wafers, while actual measurement was done after full wafer lift-off and cutting the film into quarters.

Fabricated devices were measured under illumination of simulated AM1.5G solar spectrum. Devices from fresh growth showed V_{oc} = 0.97 ± 0.01V, J_{sc} = 25.31± 0.93 mA/cm^2, *FF* = 0.79 ± 0.04, *PCE* = 19.5 ± 1.3%. Regrown devices showed V_{oc} = 0.97 ± 0.01V, J_{sc} = 26.28± 0.63 mA/cm^2, *FF* = 0.80 ± 0.01, *PCE* = 20.5 ± 0.7%. The measured J-V characteristics are shown in Fig. 3.7. Devices from both fresh grown and regrown wafers show nearly identical performance within error bar, indicating ND-ELO can successfully recover the surface with proper particle generation control.

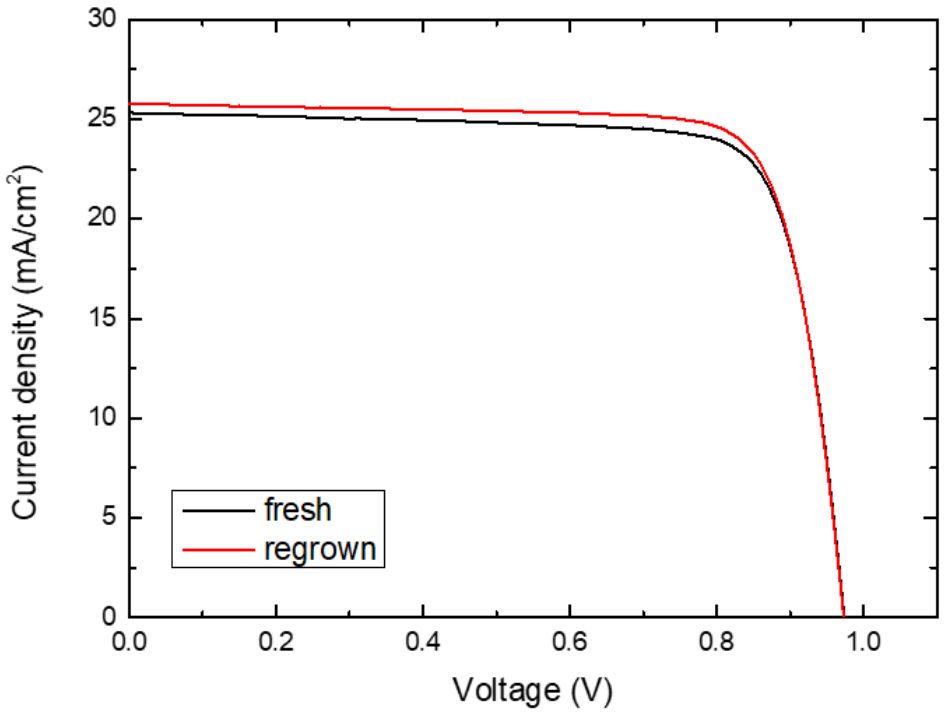

Figure 3.7 : *J-V* characteristic of GaAs PV cells from fresh and recycled GaAs substrate.

3.5 Conclusion

We demonstrated an ND-ELO process scaled up to 4" diameter GaAs wafers. Even with different growth technique and larger substrate sizes, ND-ELO shows its capability to recover the original substrate under microscopic scale AFM and XPS measurements. This shows the effectiveness of epitaxial protection layer in preventing HF contamination of original substrate, even under prolonged HF exposure. Due to relatively uncontrolled environment of sample handling, we experienced more particle generation than expected, which affected the regrowth quality of the wafer in terms of higher particle and haze density. Yet, devices fabricated from epitaxial layers lifted-off from haze-free regions of regrown wafers show nearly identical performance to fresh grown devices. This result suggests that ND-ELO has potential for production-scale processes under careful particle generation control.

Chapter 3

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Chapter 4

Integrated Single-Axis Kirigami Solar-Tracker Photovoltaic Mini-Concentrator array

Solar energy harvesting in space- and weight-constrained environments such as on residential rooftops, is often limited by the moderate efficiency of Si solar cells. In contrast, group III-V semiconductors, such as GaAs, have achieved record high efficiency photovoltaic devices, but are significantly more expensive. Concentrated photovoltaic systems can increase the efficiency and decrease the cost of solar energy generation by concentrating light onto a small photovoltaic cell area. Here, we demonstrate a lightweight, potentially low-cost, thermoformed, and laser cut kirigami-based solar tracking, 35x concentrator array with application to solar electricity generation in space-and weight-constrained environments. The tightly packed parabolic concentrator with a hexagonal aperture allows for coordinated rotation of individual concentrators by applying global axial strain along the length of the array. We find that in one embodiment of this new concept, GaAs photovoltaic cells produced by non-destructive epitaxial lift-off (ND-ELO), combined with a 50x geometrical concentration tracking concentrator array, can generate power at $\$0.47/W_p$; an approximately 90x reduction in cost compared with GaAs cells without concentration or tracking. These results provide a pathway to dramatic reductions in the cost of concentrated photovoltaic modules, potentially enabling their widespread use.

4.1 Introduction

Currently, there are about 1.6 million solar installations in the United States that generate > 49 GW, enough to power 9.5 million homes[1] . According to the National Renewable Energy Laboratory, rooftop solar photovoltaics have the potential to produce 40% of the U.S. electricity generation [2]. The report stated small building rooftops could produce 731 GW of PV capacity, or ~ 65% of the total potential of rooftop photovoltaics [2]. However, the inefficiencies of typical solar panels and their high cost limit the expansion of solar rooftops across the nation. Concentrated photovoltaic (CPV) systems that focus light onto high efficiency, and perhaps higher cost solar cells, provides an alternative approach that can enable the widespread acceptance of rooftop solar. Unfortunately, the narrow acceptance angle of concentration optics makes solar tracking necessary, while many conventional CPVs require complex and costly systems to achieve the required tracking precision, increasing system size and weight. In space- and weight-constrained environments, including rooftops, there is thus a trade-off between the ability to concentrate light and maintain compactness and light weight. Recently, miniature concentrators and microcell arrays have gained prominence as an effective means to reduce cost and weight[3–6]. These approaches are often not easily scalable or they are confined to low (<10) optical concentration factors. In most cases, solar tracking is accomplished using large and costly assemblies, and impractical calibration requirements.[7]

Here, we demonstrate an array of very lightweight, miniature parabolic concentrators integrated with a single-axis planar tracking mechanism based on kirigami design principles. Kirigami is an ancient Japanese art that uses cutting and folding techniques to transform two-dimensional sheets into three-dimensional structures[8]. In our approach, the parabolic concentrator array is fabricated from a thermoformed plastic sheet, which is coated with a reflective metal

coating, subsequently cut and fused to a transparent sheet carrying small area GaAs solar cells. The resulting structure comprises an integrated single-axis tracker/PV module that is scalable, and potentially low cost, eschewing complex, bulky support and tracking structures required by conventional concentrator designs. The concentrator array with a geometric concentration factor of 50x, achieved a maximum concentration factor of 33x in optical flux and 22x in maximum power compared to a planar cell. Furthermore, combined with simple axial rotation, the kirigami array boosts the annually generated power by a factor of approximately 35x compared to a flat cell of the same area without tracking.

4.2 Design and experimental methods

Figure 4.1(a) shows a top schematic view of the tracking array module. For this proof-of-concept demonstration, a 0.5mm thick glycol-modified polyethyleneterephthlate (PETG) sheet is attached to the top of an Al mold and heated to 110°C which is above its softening temperature. The sheet is subsequently deformed into the parabolic concentrator array by applying vacuum at the base of the mold. The mold is cooled to room temperature, hardening and subsequently released from the mold. The inner surface of the concentrator array is coated via e-beam evaporation with a 5 nm thick Ni adhesion layer, followed by a 500 nm thick, reflective Ag layer. A 50 μm thick PET sheet is used as a transparent planar cover sheet. A 10 nm thick Ti adhesion layer followed by 3 μm thick Au leads are deposited on the sheet to contact the solar cells. The thin film GaAs photovoltaic cells are fabricated using non-destructive epitaxial lift-off to substantially reduce cost,[9] and are bonded to Au contacts on the sheet using conductive Ag epoxy. The sheet with the GaAs PV cells is aligned with the corresponding molded array of parabolic reflectors to align each cell with the focal point of the corresponding paraboloid. The assembly is cut using a CO_2 laser, which simultaneously fuses the sheet to the parabolic array to make a compact, sealed unit.

The parallel cut pattern is deformed from its original shape under axial strain that tilts the paraboloids, providing single-axis tracking simply by applying tensile stress perpendicular to the cuts[8]. Arms that support the concentrators along their perimeter limit distortion of the paraboloids when strain is applied. Thus, only the arms, and not the concentrators, are deformed under axial strain.

Figure 4.1(b) shows a side view of the tracker under different axial strains. When strain is applied, the array is extended along the strain direction, separating unconnected neighboring parabolic reflectors. At the same time, arms maintain a constant distance between two edges of adjacent concentrators, causing them to rotate. As shown in Fig. 4.1(c), the arms and concentrator apertures form an acute triangle. At a rotation angle, θ, the axial strain ε is:

$$\varepsilon = 2\cos\theta - 1 - \sqrt{4\cos^2\theta - 3} \tag{4.1}$$

Apparently, θ cannot exceed 30°, at which point $\varepsilon = 0.73$. Further stretching will decrease θ since the arms and apertures now form an obtuse triangle. The translation of strain to rotational motion is a function of the elasticity of the tracking material, which can fail when strain exceeds the elastic limit of the material at the arm-concentrator junction. Figure 4.1(c) shows images of tracker array at rest (left) and under axial strain (middle and right).

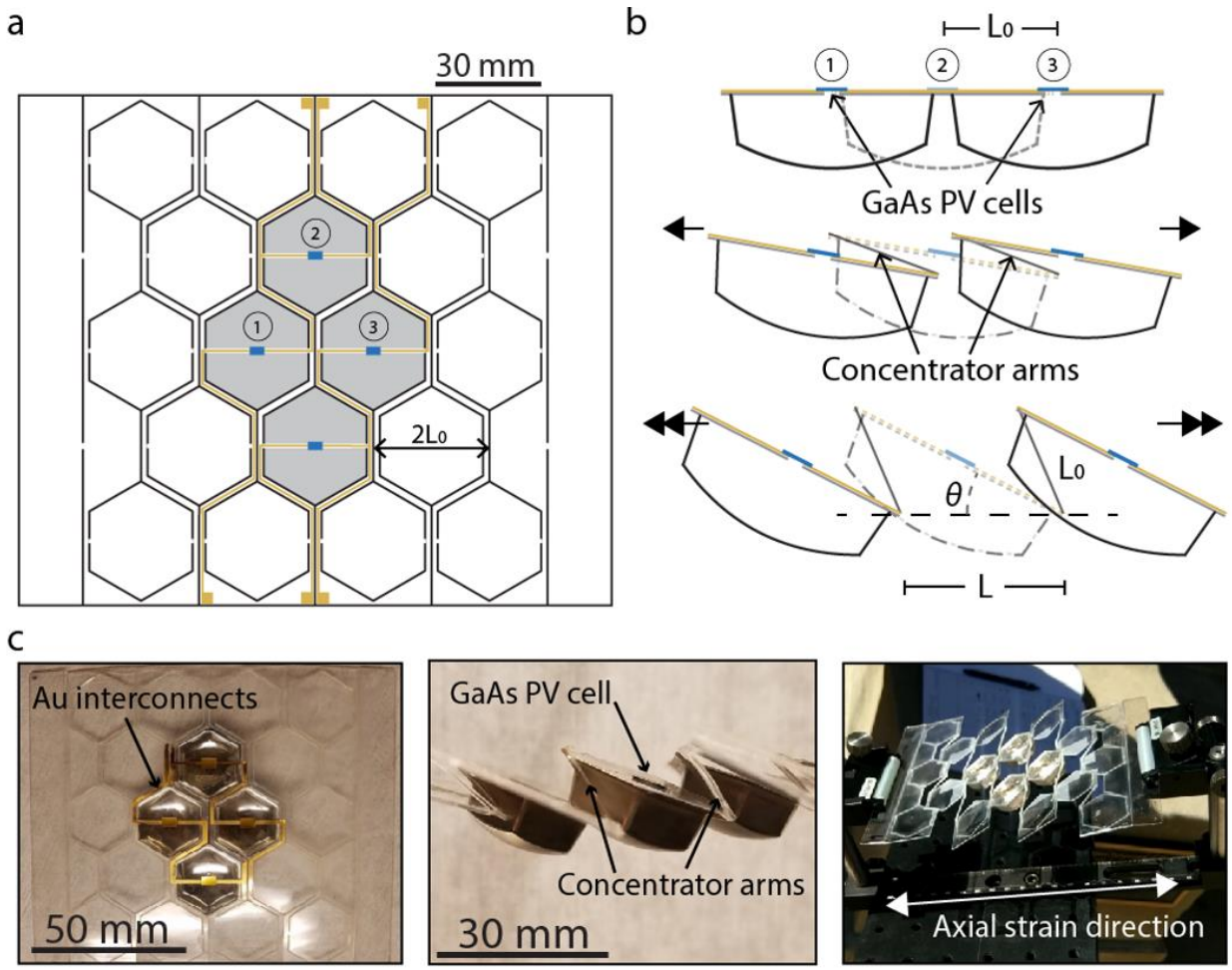

Figure 4.1 : Schematic and photo image of concentrator tracker array
(a) Schematic illustration of a top view of integrated tracking concentrated photovoltaic (CPV). The solar cells are attached to plastic top sheet, facing downwards. (b) Schematic illustration of a side view of integrated tracking CPV array under different axial strains. (c) Image of the tracking CPV array at rest (left), and tracking array under axial strain (middle and right)

For a fixed aperture, the angle at the opening of the parabola (the rim angle) determines its focal length. Large rim angles result in a low concentrator depth, but they increase the average angle of incidence of reflected rays on the solar cell. Since the anti-reflective coating (ARC) of the GaAs solar cell is optimized for normal incidence, there is a tradeoff between concentrator rim angle and optical coupling efficiency into the solar cell. We calculated the transmittance of the ARC as a function of incidence angle using the transfer matrix method[10] over wavelengths from 300nm to 900nm, as shown in Fig. 4.2(a). The optical coupling efficiency for a concentrator with a given rim angle, ψ, is:

$$\eta(\psi) = \frac{\int_0^{\psi} \int_{300nm}^{900nm} I(\lambda)T(\lambda,\phi)(\frac{dA(\phi)}{d\phi})d\lambda d\phi}{A_0 \int_{300nm}^{900nm} I(\lambda)d\lambda}, \quad (4.2)$$

where ϕ is the angle of incidence at the ARC/air interface, $I(\lambda)$ is solar spectrum, $T(\lambda,\phi)$ is the transmittance through the ARC, $dA(\phi)$ is the incremental aperture area illuminated by rays reflected to the ARC/air interface, and A_0 is the total aperture area. A plot of $\eta(\psi)$ and a schematic of the geometry is shown in Fig. 4.2(b), indicating a rapid drop in $\eta(\psi)$ at rim angles larger than 75°. To maintain an optical coupling efficiency > 99% compared to normal incidence, a rim angle of 60° was chosen for our array.

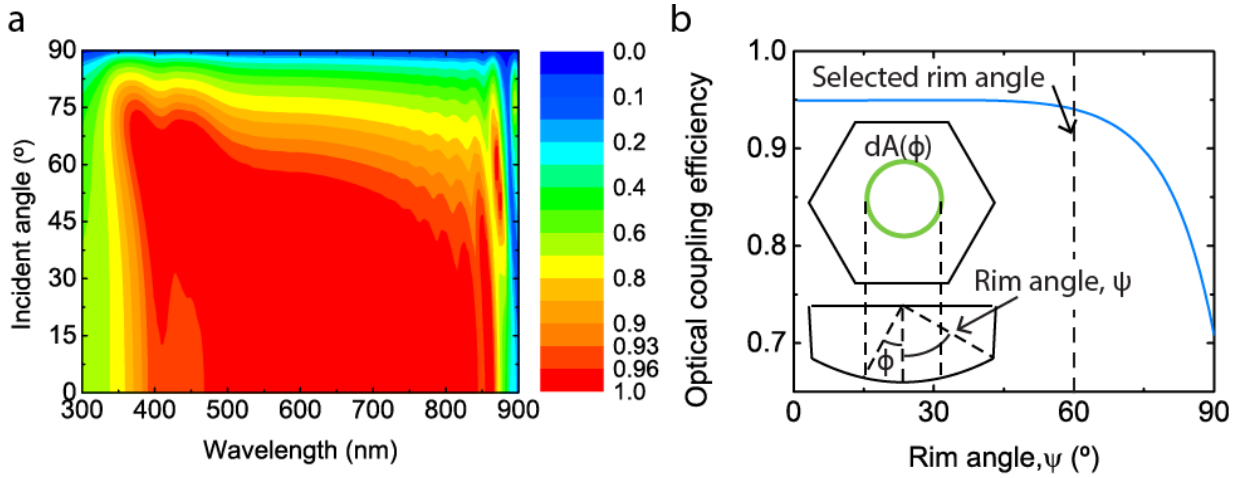

Figure 4.2 : Design principles for individual concentrator
(a) Calculated transmittance of anti-reflective coating at different wavelength and incident angle. (b) Calculated optical coupling efficiency depending on the concentrator rim angle and schematic illustration of calculation range (inset).

4.3 Deciding optimal concentration factor for single concentrator

For maximum energy conversion of a CPV system, reducing cell heating to maintain a high cell efficiency is necessary[11,12]. For conventional CPV systems with an optical concentration factor <500, passive cooling such as a heat dissipating panel is used[13], while active cooling methods (e.g. water cooling, forced air convection) are required at higher concentrations[13,14]. Due to the added complexity of cooling components of a high-concentration CPV system, a trade-off exists between

the cost of the semiconductor, and the complexity required for cell cooling and tracking accuracy. Moreover, thin PET substrates are incompatible with passive or active cooling. Therefore, understanding cell thermal properties as a function of optical concentration is necessary to optimize the module design. A concentrator with a geometric concentration factor (the ratio between the aperture size and the PV cell area) of 200 was used to study the effects of optical concentration. The current density-voltage (*J*-*V*) characteristics of 2 mm × 1.8 mm GaAs solar cells with and without a parabolic concentrator were measured under a simulated, 1 sun intensity AM1.5G solar spectrum. Neutral density optical filters were used to explore the departure from linearity of the output power vs. optical concentration, with results in Fig. 4.3. The maximum optical concentration of 100x with an average concentration of 81 was measured under a 1 sun intensity, AM 1.5G spectral illumination. The difference between the geometric concentration factor and measurement arises from surface roughness of the parabolic mold, uneven solar lamp collimation and errors in measuring the short circuit current density. The fit was obtained using a steady state heat thermal equilibrium model of solar cell efficiency[15] along with the temperature dependence of the GaAs solar cell efficiency[11]. Although the efficiency becomes nonlinear at high solar concentrations, the total output power increases monotonically with only a modest reduction in the cell's power conversion efficiency with increasing concentration.

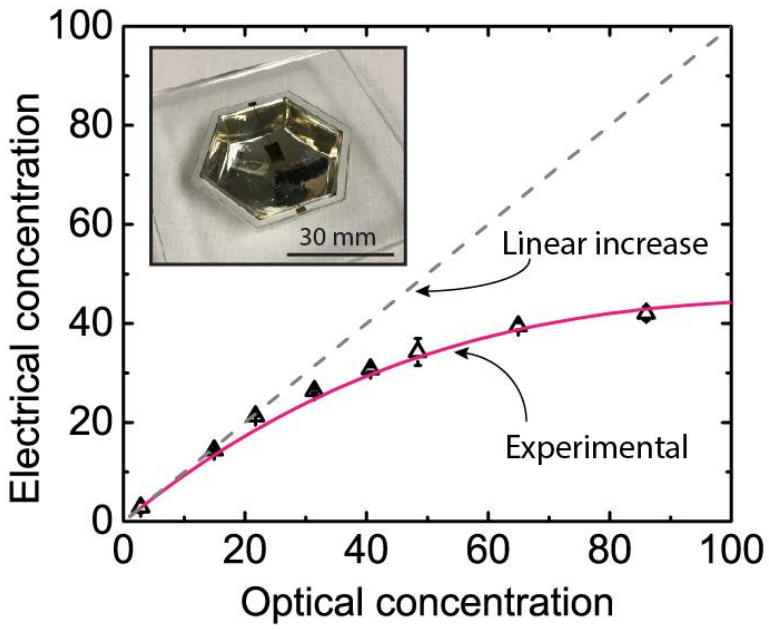

Figure 4.3 : Electrical concentration vs optical concentration

4.4 Kirigami tracker array performance

The kirigami array was stretched and contracted 6000 times, the equivalent of 16 years of operation. The range of rotation of the arrayed cells was set to ± 27° (i.e. total 54° angle). Figure 4.4(a) shows the actuation energy of the concentrator measured every 125 cycles. Discontinuities are due to instrument limitations, which required the resetting of the tracking mechanism after reaching 875 repeat cycles. A linear fit shows that the actuation energy changes by only 5% after 6,000 cycles of operation. Also, the response of the tracker array was measured before and after multiple cycles. As shown in Fig. 4.4(b), the response follows predictions of Eq. (2) within experimental error.

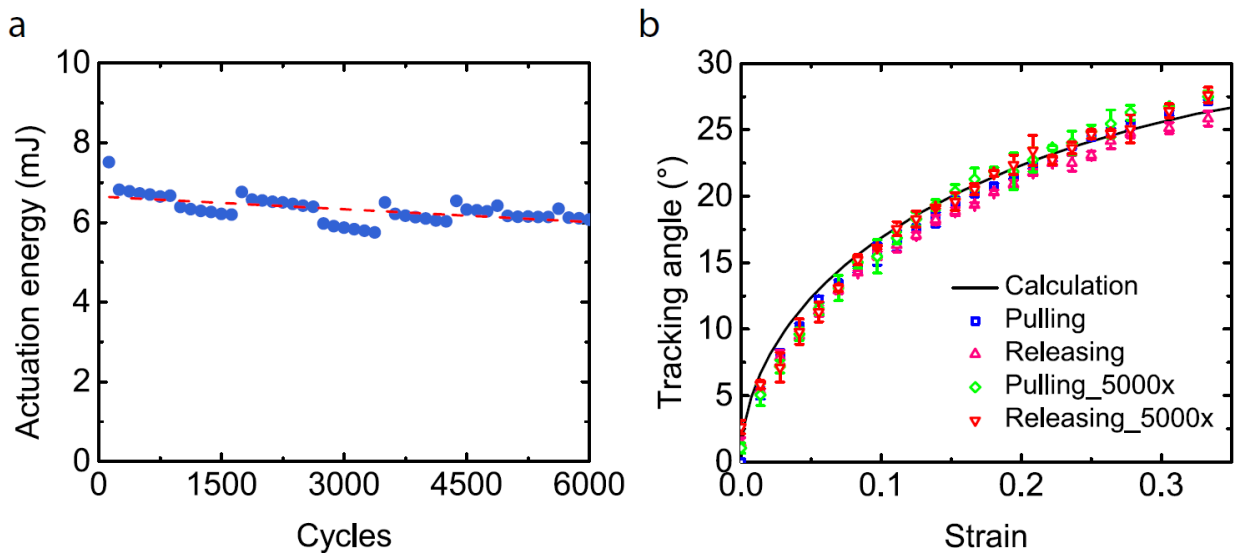

Figure 4.4 : Kirigami tracker array robustness
(a) Actuation energy of kirigami tracker per single concentrator, measured every 125 cycles over 6000 cycles. (b) Calculated (black curve) and measured (dots) geometric response of the tracker array before and after repeating 6000 cycles of operation.

A 2x2 tracking concentrator array was used to verify the simultaneous and accurate tracking of multiple concentrators. Based on the results in Fig. 4.3(b), a geometric concentration factor of 50x was chosen to reduce heating effects. The J_{sc} of GaAs solar cell with and without concentration is shown in figure 4.5(a). The J_{sc} of solar cells in the concentrator array vs. tracking angle was measured at Ann Arbor, MI, October 18, 2017, 14:00 – 15:00, at a solar elevation angle of 40°. The concentrators with a measured optical concentration of 33x were rotated about an angle θ, by applying strain as calculated from Eq. (4.1). Figure 4.5(b) shows the total short circuit current density generated by the array vs. tracking angle. The J_{sc} remains unchanged within the error range at different tracking angles. This indicates that misalignment between the four concentrators is minimal as the system is rotated to follow the solar path.

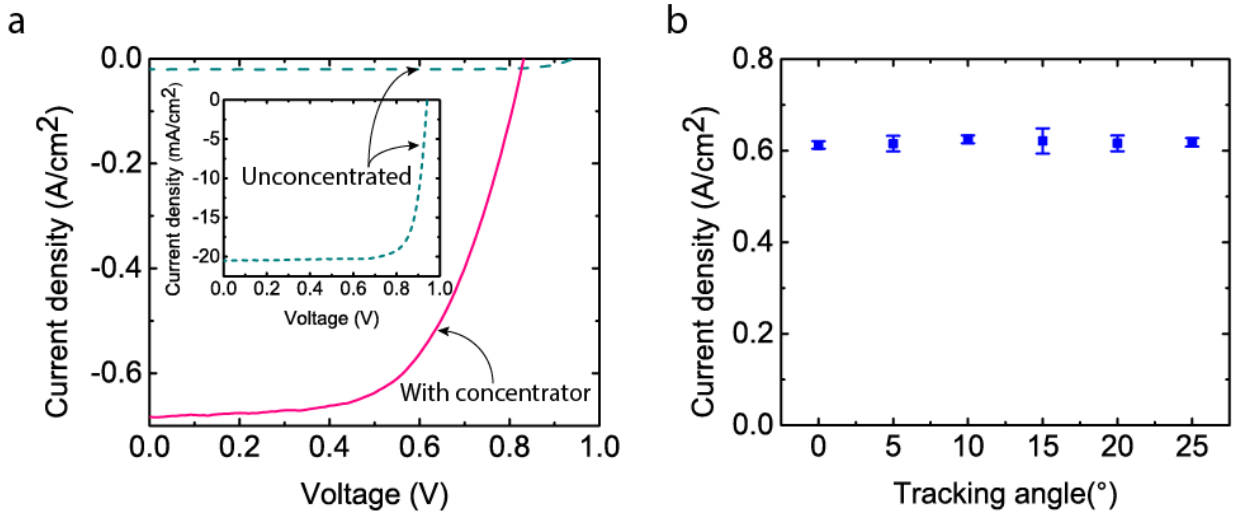

Figure 4.5 : Performance of Kirigami tracker array
(a) Current density–voltage characteristics of a GaAs solar cell with and without (inset) a parabolic concentrator. **(b)** Short circuit current of 4 GaAs solar cells attached to a kirigami tracking concentrator array vs. tracking angle, measured out of doors at Ann Arbor, MI, on October 18, 2017, 14:00 – 15:00, at a solar elevation angle of 40°. Inset: Image of the measurement setup.

4.5 Discussion

Due to the narrow acceptance angle of the parabolic concentrators, precise solar tracking is required[16,17]. Since the kirigami tracker introduced in this study only supports single-axis tracking under uniaxial strain, rotating the entire array module about the normal to the plane is required for dual axis tracking. Figure 4.6(a) shows calculated annual solar path at Phoenix, AZ (33.45° N, 112.07° W). The solar position is determined by its elevation β, and azimuth angle, ω. Since the variation of β is much smaller than for ω, the array is used to track the solar elevation, and the rotational motion tracks along the azimuth. To maximize energy harvesting, the array plane is rotated about the axis normal to ground plane while tilted at angle δ (See Fig. 4.6(b)). For space-constrained applications such as building integrated photovoltaics or rooftop tracking, the axis of rotation is kept normal to the tracker array. The tracking range δ is shown in Fig. 4.6(c).

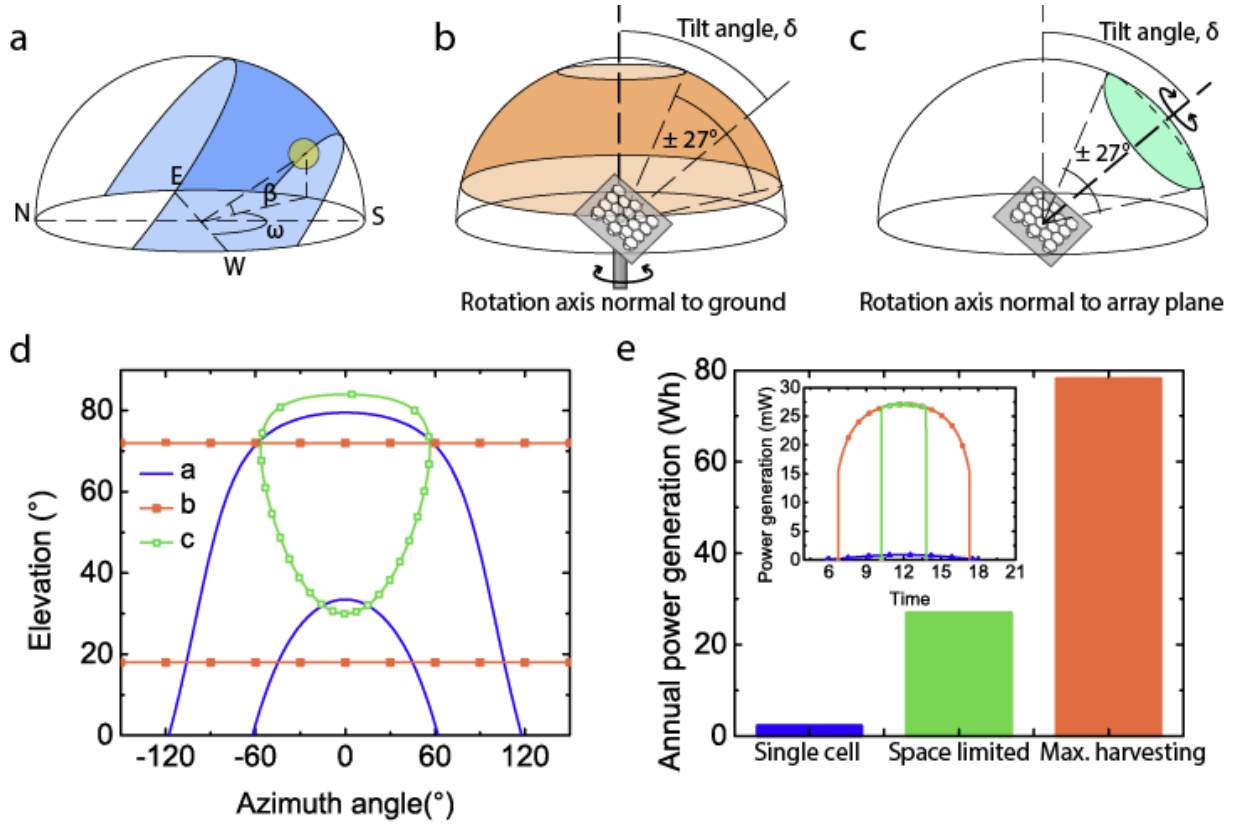

Figure 4.6 : Configurations and power collection using the Kirigami tracker array
(a) Schematic view of annual solar path at Phoenix, AZ (33.45° N, 112.07° W). (b) Tracking range for maximum energy harvesting. The array plane is tilted with offset angle, and rotates along axis normal to ground. (c) Tracking range for space-limited application. Axis of rotation is normal to array plane. (d) Tracking range of space limited application (green) and maximum energy harvesting (orange) optimized for annual solar path at Phoenix, AZ (blue). (e) Time dependent power generation over one day at equinox (inset) and annual power generation of single cell without tracking (blue), space limited application (green), maximum energy harvesting (orange) at Phoenix, AZ.

The total annual solar energy output is the sum of the electrical energy produced by the overlap between tracking range and the annual solar path. Due to atmospheric effects, the solar radiation intensity at elevation β can be approximated as $I_0 \times 0.7^{(AM^{0.678}-1.5^{0.678})}$ where $AM = \frac{1}{\sin(\beta)}$, and I_0 is the solar radiation intensity at AM 1.5G.[18] Therefore, the total solar energy coupled into a photovoltaic cell is $I_0 \times CF_0 \times 0.7^{(AM^{0.678}-1.5^{0.678})}$, where CF_0 is the optical concentration factor of the aperture. Figure 4.6(d) shows the annual solar path at Phoenix, AZ (blue), and the tracking range for the maximum energy harvesting (orange) and space-constrained (green) cases. With the measured optical concentration factor of 33, the electrical concentration factor is 22,

without active cooling. Figure 4.6(e), inset, shows time-dependent power generated by a planar cell without tracking (blue), space-constrained (green) and maximum energy harvesting (orange) over one day with the sun at its equinox. The calculated total annual power generation per unit cell area is shown in Fig. 4.6(e). For maximum energy harvesting, the average daily power generation is 770 J, compared with the measured tracker actuation energy per individual concentrator per cycle of 6.5 mJ. This represents a minimal expenditure (0.001%) of the average generated power, primarily due to the ultralight weight of the miniconcentrator array. Compared to a planar cell without tracking, the annual energy collection per solar cell area is improved by a factor of 11.9 and 34.5, respectively. The total electrical energy concentration factor is larger than for normal incidence since the cosine loss of the flat cell is increased at low elevation angles.

Compared to the geometric concentration factor of an individual concentrator (50x), 35x concentration in annual power generation indicates that the overall output power is decreased by 30% compared to an unconcentrated, untracked flat GaAs cell of the same area as the concentrator aperture. For 50x geometric concentration, an optical concentration of 45x can be achieved assuming 10% optical loss from reflective losses and an imperfect concentrator surface. Cell heating results in 32x power concentration. Combined with tracking, a 42-fold increase in annual power generation is simulated.

Using previous analyses of non-destructive epitaxial lift-off processed GaAs PV cells[3] with a single axis tracking module [19], the costs of GaAs solar cells using different production methods with and without concentrators are calculated, with results in Table 4.1. For all cases, a 35% power conversion efficiency of the cell was assumed. Due to high starting wafer price, substrate GaAs PV cells without wafer recycling or concentration results in a module cost of \$42.06/ W_p. Epitaxial lift-off that separates the epitaxial active region from the substrate can reduce the wafer cost by

substrate recycling [20]. However, only a few recycles are possible due to substrate thinning and damage incurred by chemo-mechanical polishing (CMP) required between each epitaxial regrowth[20].Assuming a 3x reduction in substrate cost by ELO recycling, a cost of \$14.44/W_p is estimated. The ND-ELO process can further reduce the cost by eliminating the CMP process, thereby increasing the number of substrate recycles (50x assumed). In this case, the cost is reduced to \$5.55/W_p. Finally, combining ND-ELO GaAs cells with miniconcentrators can further, and dramatically reduce the overall cost. Assuming a concentration factor of 38 due to a 10% packing density loss, and a \$0.22/W_p tracker module cost [19], our approach leads to a cost of \$0.47/W_p, which is a 90x reduction compared to conventional substrate GaAs cells, and is comparable with Si PV technology. These dramatic reductions in the production cost of high efficiency GaAs PV modules can further allow for efficient solar energy harvesting in space-limited applications.

Table 4.1 : Cost estimation for cells with different manufacturing and concentration conditions

	Substrate cell	ELO cell	ND-ELO cell	ND-ELO cell plus mini-concentrators[(c)]
Wafer	$33.64	$8.83 [(b)]	$0.67	$0.02
Material	$2.31	$1.78	$1.78	$0.05
Depreciation	$1.80	$1.80	$1.80	$0.05
Module cost	$0.1	$0.1	$0.1	$0.33[(d)]
Margin[(a)]	$4.62	$1.19	$0.46	$0.01
labor, utilities, maintenance	$0.73	$0.73	$0.73	$0.02
Total	$42.06	$14.44	$5.55	$0.47

(a) 9% fixed margin is assumed

(b) Fixed CMP cost of $8/repolish with a 70 % process yield is assumed.

(c) 10% packing density loss assumed.

(d) $0.22 tracker module value added for single axis tracking and kirigami tracking.

4.6Conclusion

We have demonstrated an integrated kirigami-based solar tracking miniconcentrator array that is lightweight, has a low-profile, and potentially cost-efficient. Its attributes make its use attractive for space- and cost-constrained applications such as on residential rooftops and in building integrated photovoltaics. The nearly linear geometric response of the tracker enables simultaneous rotation of concentrators via the application of uniaxial strain. When combined with a rotational tracking engine, the GaAs PV module production cost can be reduced by a factor of 90 compared to a conventional GaAs cell. Moreover, only 0.001% of the total power generated is used for actuating the kirigami tracker. Based on these results, the kirigami solar tracker may lead to a significant growth of solar photovoltaic rooftop installations.

Chapter 4

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Chapter 5

A High Throughput, Linear Molecular Beam Epitaxy System for Reduced Cost Manufacturing of GaAs Photovoltaic Cells

Solar cells based on GaAs and related compounds provide the highest reported efficiency single junction and multijunction solar cells. However, the cost of the cells is prohibitive when compared with Si and other thin film solar technologies. One significant differentiator is the high cost required to grow the epitaxial layers. Here, we propose a molecular beam epitaxy (MBE) system design that has the potential to increase the epitaxial layer growth throughput, thereby significantly reducing production costs. A rack-and-pinion based linear transfer system sequentially transfers multiple substrate platens between interconnected growth positions within the chamber, thereby synchronously growing layers on many wafers in the desired order and at the required thicknesses. The proposed linear MBE platform is the basis for a realistic analysis of GaAs single junction photovoltaic cell production cost. Our model projects a nearly 55% cost reduction in epitaxial growth via linear MBE when compared to conventional MBE, and a 85% reduction when further process optimization is assumed and combined with non-destructive epitaxial lift off. Even when considering all of these factors in an optimistic light, the cost of unconcentrated GaAs solar cells using *any* existing growth process is unlikely to drop below $3/Wp in the foreseeable future.

5.1 Introduction

Despite the high power conversion efficiency (*PCE*) of GaAs photovoltaic cells,[1] their widespread adoption for solar-to-electricity energy conversion has been limited due to the exceptionally high cost of materials and epitaxial growth of the active solar cell layers. Several different approaches have been engineered to reduce the cost of GaAs photovoltaic cells, such as substrate recycling through epitaxial lift-off (ELO) followed by wet and dry etching of a substrate recovery layer[2–5] or chemical mechanical polishing (CMP).[6–8] Controlled spalling by removal of a surface layer from the substrate using an intervening stress layer[9,10] could potentially be an alternative substrate recycling method, although it can leave behind a rough wafer surface.[9,10] Use of low-cost, non-III-V substrates such as Si or Ge[11,12] is also considered as a potential cost reduction pathway, although growth of high quality GaAs cell is yet limited due to dislocation from the lattice mismatch.[13,14] Besides substrate recycling, the expensive photovoltaic active cell area can be reduced by the use of low-cost concentrators.[4,15] However, none of these approaches alone can effectively reduce the cost to levels that approach Si photovoltaics due to the limited number of substrate reuses through ELO[2,3] or the complexity and cost of concentrator tracking systems.[16] Moreover, the cost of ownership of GaAs epitaxial growth equipment such as metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE), contributes substantially to the solar cell cost.[7,17] This is due, in part, to the low throughput of the epitaxial growth technology for MBE, or the use of costly, highly refined chemical precursors for MOCVD. Analysis of the manufacturing costs of a single junction GaAs cell based on MOCVD [7] predicts the cost of GaAs cells can be as low as \$3.50 - \$4.50/Wp, with an optimized cell structure, >50 epitaxial lift off cycles from a single wafer, and unspecified improvements of growth technology and reductions in materials cost. This is compared to the current, approximately \$80/Wp where

only a handful of ELO steps are employed using conventional growth and fabrication methods. Another analysis of the costs of dual junction GaInP/GaAs solar cells grown by so-called dynamic hydride vapor phase epitaxy (D-HVPE)[6] also claims an optimistic reduction of GaAs cell cost to $2.00 - $3.00/Wp via increased wafer throughput using a potentially high growth rate of 200-300 μm/hr for GaAs[18] and 50 μm/hr for GaInP.[19] However, some of the assumptions for both cases are yet to be specified, such as improved material utilization, use of inexpensive yet-to-be-identified growth future precursors for MOCVD. Also, one critical cost reduction comes from unspecified future wafer cost reductions that rely heavily on improved substrate reuse of > 50 times, although current demonstrations remain near < 5.[2,3] Furthermore, the rapid HVPE growth of some alloys needed in high efficiency and low cost III-V solar cells necessary to enable ELO (e.g. AlAs) remains problematic.

Here, we propose a high throughput linear MBE (LMBE) system that can reduce costs even further than is realized using multiple wafer recycles via the recently introduced process of non-destructive ELO (ND-ELO).[2–4,15] The objective underlying this proposal is to determine whether GaAs solar cells costs are primarily driven by capital expenses related to a particular growth technology, or by other potentially less cost-elastic sources. While conventional MBE is a proven technology for the growth of high quality III-V solar cells using pure elemental (and hence relatively low cost) source materials, its exceptionally low growth rates (1 -3 μm/hr) severely limit wafer throughput. This has led to prohibitively high capital expense that has prevented its use in relatively low cost solar cell manufacturing. The LMBE design considered here alleviates some of these concerns by replacing a single, multi-purpose growth chamber with a continuous line of interconnected chambers, each whose purpose is to grow a separate layer needed in the solar cell structure. The in-line system is connected at opposite ends by rapid wafer loading and unloading

chambers. Realistic production costs of archetype single junction GaAs solar cells based on modified, previous estimates of the cost of MOCVD growth[7] using this tool are estimated.

Our analysis shows the solar-to-electricity energy conversion cost using GaAs thin film photovoltaic cells is reduced from $24.82/Wp for conventional MBE, to $13.63/Wp, using LMBE. With further optimized processes such as ND-ELO, the cost can be reduced to $3.67/Wp. A comparative analysis of growth by LMBE, MOCVD and D-HVPE indicates that all processes are projected to yield approximately the same cost-per-Watt for GaAs solar cells, indicating that the capital expense of these three growth methods is less of a factor in determining cell cost than the cost of materials and fabrication processes. However, savings from improved throughput is independent of reductions in substrate cost, which is primarily determined by the efficacy of the substrate reuse technology. We conclude that even under the *most optimistic* assumptions made for growth, processing conditions, and cell configurations, the cost of GaAs-based solar cells is over ten times that of current Si solar cells, and will remain as such for the foreseeable future.[20]

5.2 Linear MBE System Design: Reducing the cost of epitaxial growth

A schematic top view of a conventional, production-scale MBE cluster tool is shown in Fig. 5.1(a).[17] The system consists of a growth chamber, buffer chamber, and loading and unloading chambers. The substrate platen holds 7, six-inch diameter wafers. The platen is transferred into and out of the central distribution chamber via a manipulator arm. During a growth cycle, the platen is mounted on a substrate heater in the growth chamber facing downwards towards the Knudsen cells containing the elemental source materials. Since there are several different layers comprising the device structure, multiple effusion cells are continuously heated, with the material flux from each cell controlled by individual shutters.

Figure 5.1(b) shows a top schematic view of the proposed LMBE system comprising a main chamber with multiple, interconnected growth positions along a row, and loading and unloading chambers at each end. The substrate preparation and storage chambers can also be placed in-line or vertically relative to the loading and unloading chambers. The desired epitaxial structure is realized by growing layers of similar thicknesses and growth times at each position to prevent delays incurred by the entire line while a particularly thick layer is grown. For example, if the typical layer thickness required in the device is d, but the active region thickness is larger, e.g. $3d$, then each of the layers are grown at separate positions within the line, whereas the active region is grown by consecutive steps at three adjacent positions. Thus, the throughput of this example line is:

$$TP = N/(d/r+t_{tr}), \tag{5.1}$$

where r is the rate of growth of a layer (in μm/h), $N = 7$ is number of wafers per platen, and t_r is the cumulative transfer time from loading, to transfer between growth sections, to unloading. Since each growth position is used to grow layers of approximately equal thickness, N wafers are produced at each the position.

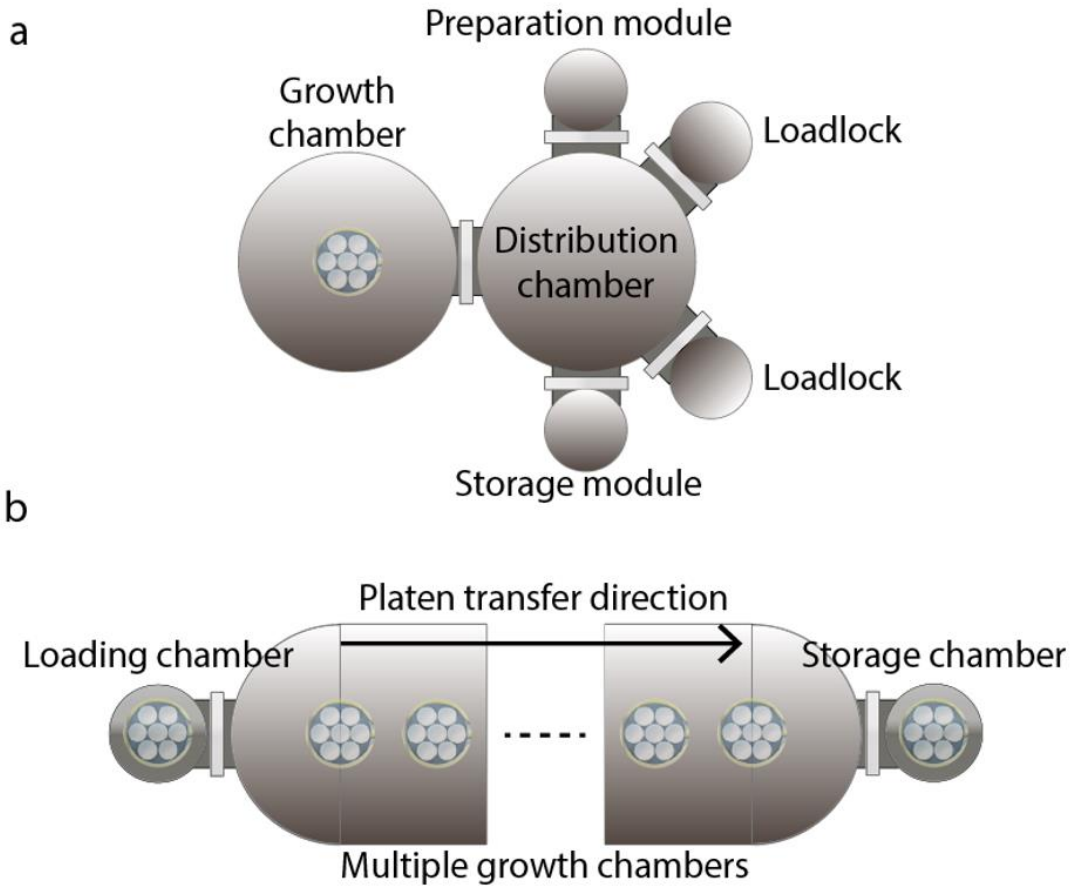

Figure 5.1 : Schematic illustration of conventional and proposed MBE systems
(a)Top view of conventional, production scale MBE comprising a distribution chamber, growth chamber and small peripheral chambers. (b) Proposed linear MBE machine with expanded growth chamber

Substrate platens with the same nominal size as used in a conventional MBE system are transferred in a "bucket brigade" fashion from the loading chamber, through the several growth positions, to the unloading chamber. After each layer growth, the substrates are transferred in unison from their current positions to the next position, and the growth cycle starts again. The complete multilayer structure is obtained after a platen transits the length of the system from loading to unloading. This configuration allows for increased utilization of effusion cells, and replaces multiple manipulator arms with a simple linear transfer system (see below). Each growth position consists of a substrate heater with only those effusion cells required for the growth of a

particular layer. As a consequence, the total chamber volume occupied by a growth section is smaller than that of a conventional MBE system. Therefore, supporting equipment such as pumps and electronics are shared between multiple sections.

A limitation of the LMBE architecture is that its flexibility in growing a variety of different structures is restricted, since each growth position is optimized to achieve a pre-determined layer composition within a designated device structure. Changing the number of growth positions (and hence the total number of layers) requires an extension of the main chamber. Flexibility can be improved by inserting blank effusion cells and growth sections along the system length that can be activated as needed at a low incremental expense.

5.3 LMBE platen transfer mechanism

Conventional MBE systems use a complex manipulator arm to transfer the substrate platen between the main growth and buffer chambers. The LMBE eliminates the need for a manipulator arm between growth sections, since platen transfer occurs via a linear movement, thereby reducing machine cost and footprint. Figure 5.2(a) shows a schematic of the linear transfer mechanism. A rack-and-pinion track transfers platens between growth positions distributed along the system length (the *x*-axis). Platen holders, or tabs, are placed in the rack at intervals equal to the distance between growth positions. Platens have protrusions, or "ears" that fit into the tabs attached to the rack. A rotating substrate heater whose axis is along the *z*-direction is located each growth position. A schematic of the substrate heater with sidewall openings and a substrate platen with ears is shown in Fig. 5.2(b).

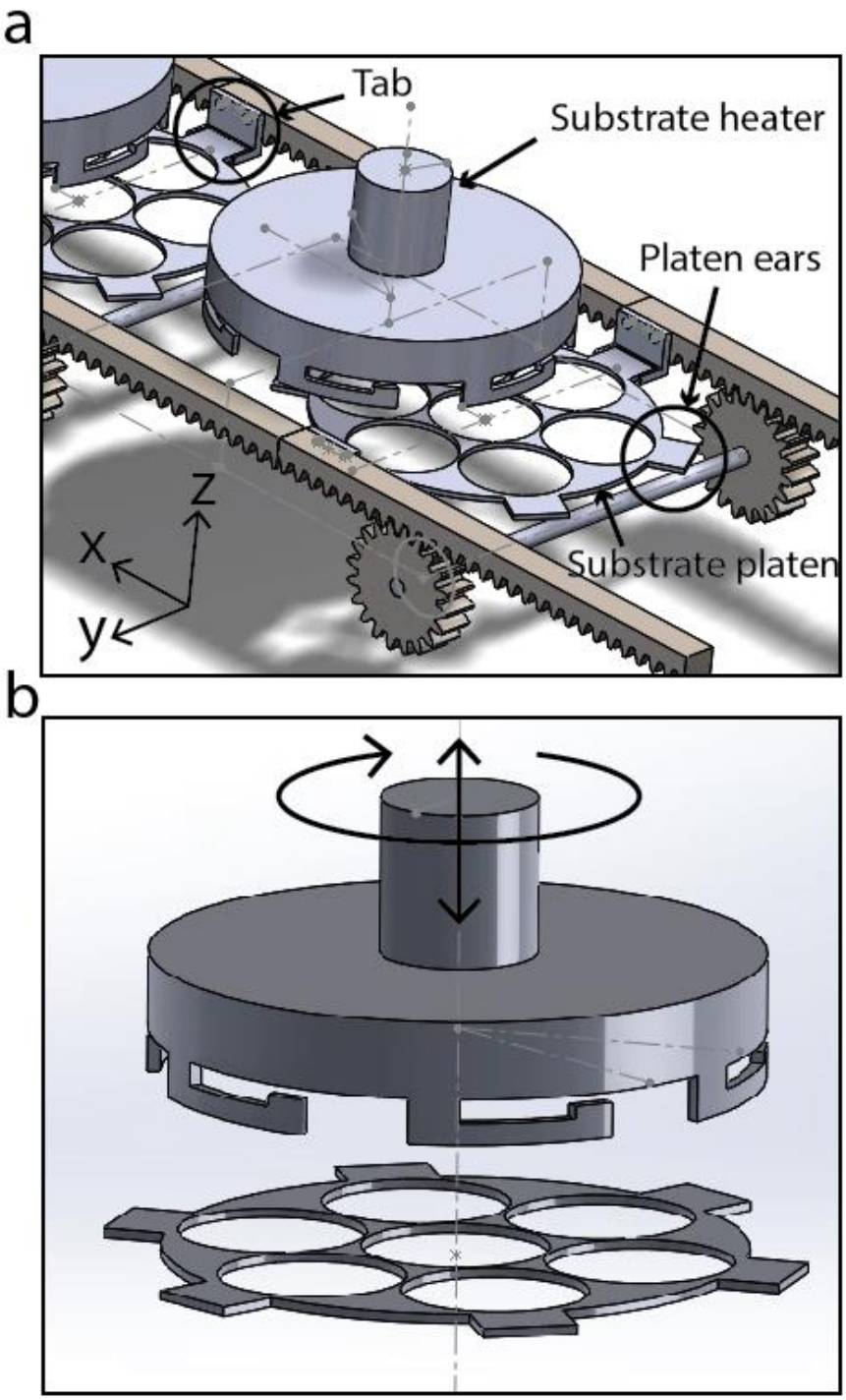

Figure 5.2 : Building blocks of LMBE platen transfer system
(a) Schematic illustration of a rack and pinion linear transfer system with tabs attached to the rack and substrate heaters at growth positions. (b) Substrate heater and platen, showing the range of motion of the heater for picking up and laying down of platen.

Vertical and rotational movements of the substrate heater locks the platen into the heater by holding the platen ears in the sidewall openings. Unlocking the platen from the heater entails the reverse of the locking sequence. During growth, substrate platens are held by the substrate heaters. The tabs are located at the midpoints of the growth positions, as shown in Fig. 5.3(a). After each layer is grown, the "transfer in" step commences. The rack moves in the -*x* direction by half the distance between growth positions. Then the $(N+1)^{th}$ tab is aligned with N^{th} growth position (Fig. 5.3(b)). Substrate platen heaters move down along *z*-axis, leave the platen at the tabs by unlocking, and then retract. A new substrate platen is transferred from the loading chamber to the first platen holder, which is now empty. In the final step – "transfer out"— the rack moves in the +*x* direction by the distance between each growth position until the first platen tab is aligned with first growth position, as shown in Fig. 5.3(c). Once growth is complete, the platen at the end of the rack is transferred to the unloading chamber, and the rack moves in the -*x* direction by half the distance between growth chambers, returning to the first step of the growth cycle.

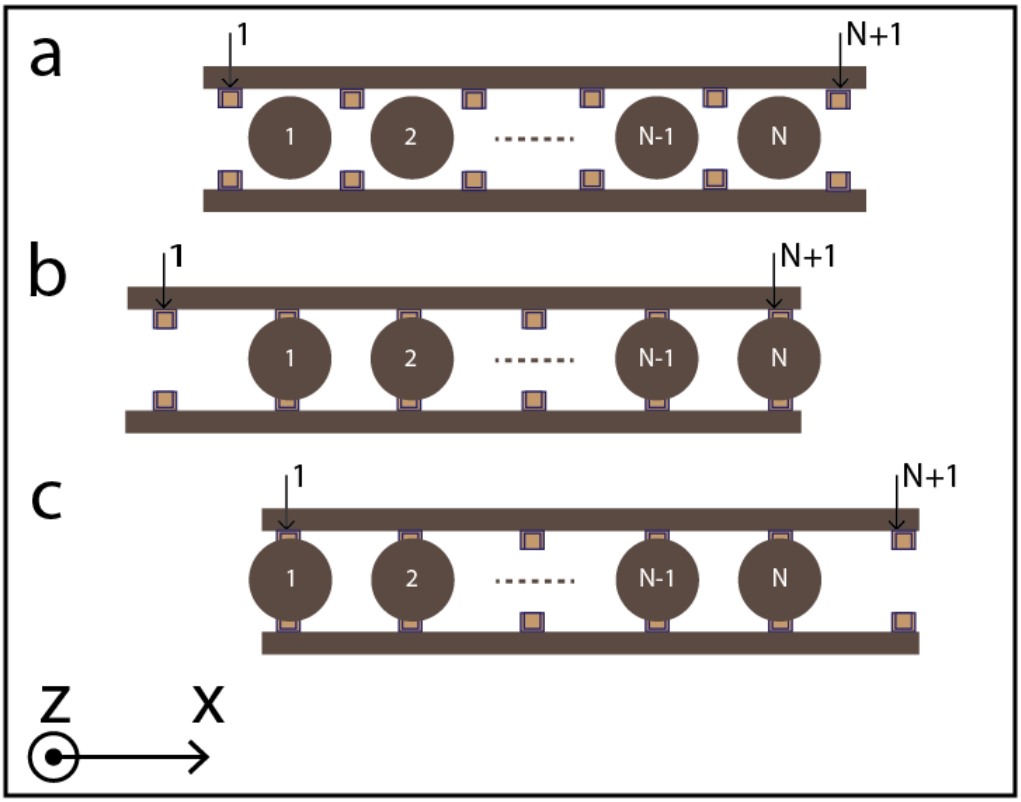

Figure 5.3 : LMBE platen transfer mechanism
Rack at (a) the growth position, (b) the transfer into the growth position, shifted by half the distance between growth positions in the backwards direction, and (c) the transfer-out position, shifted by the distance between growth positions in the forward direction.

5.4 LMBE setup for single junction GaAs PV cell growth

The number of growth positions is determined by the particular structure being grown. An example inverted GaAs single junction photovoltaic cell used for ND-ELO processing is shown in Fig. 5.4. The structure can be divided into three different sections: sacrificial and protection layers used to separate the epitaxy from the parent wafer, the emitter/front contact, and the base/back contact layers. The ND-ELO structure comprises a 425 nm thick sacrificial-plus-protection layer structure (blue rows). The emitter/front contact (green rows) layers are 335 nm thick, and the 2.82 μm thick base/back contact layers (yellow and orange rows) are divided into 6 identical, 470 nm thick sections to equalize the time spent growing each layer in the sequence. The growth chamber thus requires 8 growth positions starting with AlAs and InGaP sacrificial and protection layers,

then the emitter layer, and 6 base layers. Figure 5.5 shows the LMBE chamber configuration and the 30 effusion cells required for this single junction device. The effusion cells used for each growth section are summarized in Table 5.1.

Thickness (nm)	Material	Description	Dopant	Layer type	Growth position
15	GaAs	Contact (p++)	C	Back contact	8
20	GaAs	Contact (p+)	Zn		
100	Al(0.26)GaAs	BSF (p+)	C		
2500	GaAs	Base (p+)	Zn	Base	3~7
34	GaAs	NID	-	Emitter / Top contact	2
150	GaAs	Emitter (n+)	Si		
25	Ga(0.49)InP	Window (n+)	Si		
100	GaAs	Setback (n+)	Si		
25	GaAs	Contact (n++)	Si		
50	Ga(0.49)InP	Etch Stop	-	Epitaxial lift-off structure	1
100	GaAs	Protection	-		
25	AlAs	Release Layer	-		
100	GaAs	Protection	-		
50	Ga(0.49)InP	Etch Stop	-		
100	GaAs	Buffer	-		

Figure 5.4: An inverted single junction GaAs photovoltaic cell structure used for analysis.
The sacrificial layer used in epitaxial lift off with protection layers (blue), emitter and front contact layers (green), base layers (yellow) and back contact layers (orange) are indicated.

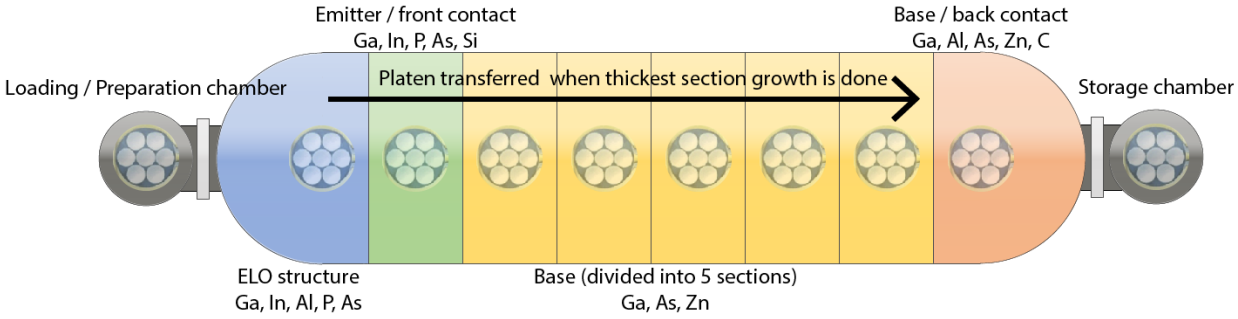

Figure 5.5: Schematic illustration of proposed LMBE system chamber configuration for GaAs PV cell growth

Table 5.1 : Effusion cells required for different layers

Layer	Material	K-cell sources	Number of layers	Number of K-cell sources
ELO structure	GaAs, GaInP, AlAs	In, Ga, Al, As, P	1	5
Emitter, Top contact	GaAs(n), GaInP(n)	In, Ga, As, P, Si	1	5
Base	GaAs(p)	Ga, As, Zn	5	3
Base, Bottom contact	GaAs(p), AlGaAs(p)	Ga, Al, As, Zn, C	1	5

5.5 Assumptions for cost analysis of single junction GaAs solar cells via LMBE

We now estimate the system cost and ultimately the solar cell production cost for the example structure in Fig. 5.4. As shown in Fig. 5.5, the base layer growth sections require only 3 effusion cells per section, and the other sections require 5 effusion cells each. Conventional MBE growth chambers accommodate at least 10 effusion cells. The increase in chamber volume by the addition of a growth section is based on the number of effusion cells required per section. The chamber cost and required pumping capacity are assumed to be proportional to the added volume. We assume that the first and last chamber sections occupy 50% of the volume of a conventional growth chamber, with 5 effusion cells per section (see Fig. 5.5). Thus, the entire system volume is approximately 300% that of a conventional MBE growth chamber. Solid sources are used for all elements, and slotted stainless steel dividers are used to separate growth positions to prevent cross-contamination. For further cost reductions, the chamber walls are cooled using a closed loop polymer chiller. Previously, it has been found that there is no significant difference in the quality of GaAs grown using a chiller than a more costly liquid nitrogen-cooled chamber.[21] Maintenance

and calibration costs are estimated to be twice that of a conventional MBE system, considering the increase in chamber size and number of effusion cells. Total machine costs are estimated based on conventional parts costs assuming bulk purchasing required for production equipment (see Table 5.2).

Table 5.2 : Cost estimation based on machine parts

Part	Unit cost	# of units	Total cost
End chambers	$200K	2	$400K
Chamber sections-emitter	$200K	1	$200K
Chamber sections-base	$120K	5	$600K
Linear transfer system	$50K	1	$50K
Transfer arm for loading / unloading	$50K	2	$100K
Loading / buffer chamber	$100K	2	$200K
Main chamber pump	$30K	3	$90K
Buffer chamber pump	$15K	2	$60K
K-cell with controller, power supply	$100K	30	$3.0M
Electronics, measurement tools	$200K	-	$200K
Cost	-	-	$4.9 MM
Price (Total + 40% margin)	-	-	$6.9 MM

The cost of ownership is calculated based on previous studies of large-scale, production MBE systems.[17] For conventional MBE, 0.25 unskilled and 0.09 skilled labor is required per tool.[17] For linear MBE, the same amount of skilled labor is assumed since the growth sequence can be automated. Unskilled labor is assumed to be doubled, considering the increased throughput,

maintenance and number of platens that require handling. Wages for unskilled and skilled labor of $12.05/hr and $17.56/hr with 55% benefits, and maintenance and calibration costs of $200K/year are based on a similar analysis for conventional MBE.[17] Power consumption of 135kW/h is inferred from a previous analysis.[17] This results in $75K/year by assuming an industrial electricity rate of $0.07/kWh.[22] Power supplied to chiller costs $25K/year, which compares favorably to liquid nitrogen coolant use at $60K/year.[17]

Table 5.3 : Assumptions for MBE cost of ownership estimation

MBE Cost	Unit	Conventional MBE	Linear MBE
Thickest section thickness	μm	3.574	0.47
Substrates / platen	/MBE	7	
Unskilled labor	/MBE	0.25	0.5
Skilled labor	/MBE	0.09	0.09
Unskilled wage	$/MBE/year	39200	75100
Skilled wage	$/MBE/year	20600	19700
Cycled chiller + Electricity	$/MBE/year	100000	300000
Materials utilization		60%	80%
Maintenance + Calibration	$/MBE/year	200000	600000
Depreciation	$/MBE/year	450000	690000
Campaign Length	Month	11.5	11
Maintenance Time	Month	0.5	1

For the linear system, electricity plus chiller and maintenance costs are tripled since the number of pumps and effusion cells are increased by that amount. A total growth campaign length of 11.5 months and 11 months per year is assumed for conventional and linear MBE systems, respectively. Machine depreciation is assumed to follow a 10 year linear model. The machine cost

for a conventional MBE system of $6 MM is inferred from a previous analysis.[17] A 25% discount is then applied for production-level bulk purchasing, leading to a total cost of $4.5 MM per conventional MBE tool. This was set higher than a typical bulk purchase discount of 10% to 15% for the MBE machine, since production-level MBE tools are only needed in modest numbers to satisfy the production needs of the microelectronics and communications industries. The assumptions are summarized in Table 5.3. Additional costs incurred for taxes, insurance, wages other than manufacturing labor, etc. are not included in this analysis, and hence this should be considered to be an estimate at the low end of actual manufacturing costs.

5.6 Cost analysis of single junction GaAs photovoltaic cell via LMBE

Previous cost estimates of solar-to-electricity energy conversion using GaAs thin film photovoltaic cells grown via MOCVD[7] and D-HVPE[6] are used to estimate total cell production costs. The manufacturing process is divided into 3 principal steps. (i) Epitaxial growth, (ii) epitaxial lift-off, and (iii) device fabrication. Each consists of multiple process steps, where the cost per step is estimated from the sum of equipment, utilities, labor and materials costs. We assume LMBE an epitaxial growth rate of 3 μm/hr, 6 min transfer time between each growth position with minimum cooling of the substrate during transfer to avoid epitaxial surface degradation, and 80% material utilization efficiency which is comparable to upside scenario for MOCVD growth.[7] Since conventional MBE requires heating effusion cells even between growths, 60% material utilization efficiency is assumed in that case.

Materials costs are calculated by multiplying the required materials cost per single platen by the number of platens produced per year. A 6 inch GaAs wafer cost with volume purchase varies from $90 - $150/wafer, depending on supplier.[6,7] For the conservative, or “base case”, we assume a 1μm/hr growth rate, $150/wafer substrate cost[7], 20 X substrate reuse with $10/reuse ND-

ELO processing cost, along with 70% yield and 25% power conversion efficiency. The more aggressive upside case assumes a 3 μm/hr growth rate, $90/wafer substrate cost[6], an upper realistic limit of 50 X substrate reuse, with $1/reuse ND-ELO processing cost along with 95% yield and 29% power conversion efficiency. Cost estimations for cell fabrication following epitaxial growth are obtained from Woodhouse, et al.[7], since the fabrication process is unaffected by the particular growth technology employed. Cost estimates for module production based on conventional and linear MBE systems are summarized in Table 5.4. Epitaxial growth costs are calculated based on the tool capital expense, material utilization factor and the cost of each layer in the structure[7]. Equipment cost is the sum of machine depreciation and maintenance cost. The cost contribution for each part of the process is converted from $/MBE/year to $/Wp by dividing the cost of ownership by the total solar cell power produced per tool per year. The total estimated cost including substrate cost for conventional MBE with base case assumptions, and for LMBE with both base and upside case assumptions are given in Fig. 5.6. The base case costs are reduced from $24.82 to $13.63 by switching from MBE to LMBE. Upside case assumptions with optimized processes, improved cell efficiency, and lower substrate cost results in a cost of $3.67/Wp.

Table 5.4 : Cost estimation based on conventional and linear MBE

Step	Equipment ($/Wp)	Utilities ($/Wp)	Labor ($/Wp)	Materials ($/Wp)	Substrate ($/Wp)
Epitaxial growth (Conventional MBE)	13.17	1.01	1.21	0.06	7.52
Epitaxial growth (Linear MBE)	3.99	0.46	0.29	0.06	7.52
Epitaxial growth (Linear MBE, upside)	1.55	0.18	0.11	0.04	0.76
Anode metallization + Bond to flexible substrate	0.02	0.005	0.01	0.225	
Dissolve sacrificial layer + lift-off cell	0.018	0.001	0.008	0.02	
Prep substrate (plasma clean)	0.015	0.0005	0.0005	0.006	
Prep substrate (etch protection layer)	0.018	0.001	0.008	0.02	
Etch front side	0.018	0.001	0.008	0.02	
Cathode metallization	0.024	0.001	0.006	0.046	
VTE ARC	0.015	0.0005	0.0005	0.006	
Test + sort	0	0	0.05	0	
Build module	0.05	0.06	0.06	0.1	
Total (Conventional MBE)	13.34	1.08	1.36	0.5	7.52
Total (Linear MBE, base case)	4.17	0.53	0.44	0.5	7.52
Total (Linear MBE, upside case)	1.73	0.25	0.26	0.48	0.76

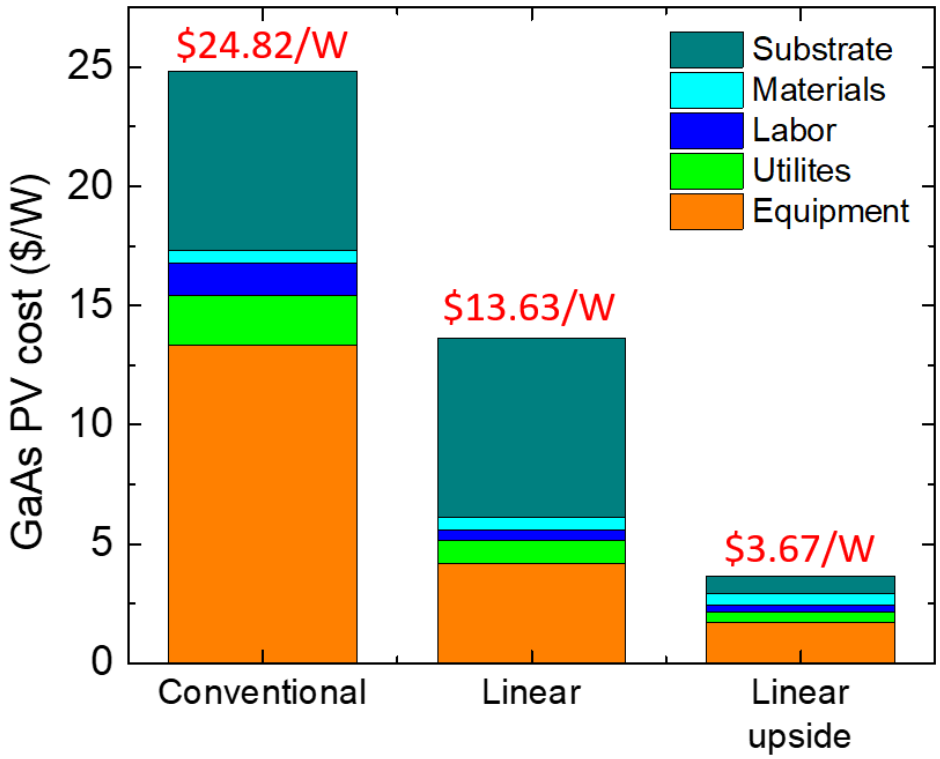

Figure 5.6 : GaAs photovoltaic cell cost estimation for three cases
Growth via conventional MBE, linear MBE with base case assumptions, and linear MBE with upside case assumptions.

5.7 Comparison between relevant technologies

The foregoing discussion principally focuses on scaling conventional MBE into a continuous growth platform, allowing us to avoid uncertainties related to proposing an entirely new growth concept. Indeed, the only new (and as yet untested) component is the linear transfer mechanism in the main chamber. Given an acceptable level of market pull, we expect relatively quick development of the proposed concept after calculating the optimum distance between growth sections that can prevent cross-contamination of the epitaxial layers.

Our analysis shows that the solar-to-electricity conversion cost of GaAs PV cells can be cut by nearly 50% when a conventional MBE system is replaced with the proposed LMBE system. This primarily results from the substantial savings in capital expense and increased throughput.

Labor cost in $/Wp is also reduced for LMBE due to its higher throughput. For conventional MBE with base case assumptions, most of the cell cost is determined by substrate and equipment costs. With LMBE, the equipment cost is reduced from $13.34/Wp to $4.17/Wp. Expanding the growth chamber into multiple sections reduces the components count compared to conventional MBE systems. Thus, the equipment cost and depreciation scales more slowly compared to simply multiplying the number of MBE cluster tools. Yet the substrate cost of $7.52/Wp remains unchanged regardless of growth technology employed. With upside case assumptions, the cell cost is further reduced to $3.67/Wp, which is a nearly 85% reduction compared to the estimated cost based on conventional MBE systems.

A comparison between cell costs achieved using linear MBE, MOCVD[7] or D-HVPE[6], is provided in table 5.5. To make this comparison, we have relied on and modified previous estimates that are not always directly comparable, and that often made unsupported assumptions. Where possible, we have attempted to make these previous estimates consistent with our current analysis, especially for substrate costs that depend on the number of reuses via ND-ELO or CMP. Our analysis assumes 50 X reuse with a cost of $1/reuse and a 29% cell efficiency, which results in $0.76/Wp substrate cost. Woodhouse, et al[7] predicts $4.6/Wp upside case cell cost grown via MOCVD, with 500 X substrate reuse and 20 μm/hr growth rate. Since current status of MOCVD can achieve a GaAs growth rate of 60 μm/hr[23], we estimate a $3.5 – 4.5/Wp considering cost reductions via this faster growth and an adjusted more realistic substrate reuse of 50X.

Analyses based on D-HVPE[6] assumed the growth of a dual junction GaInP/GaAs photovoltaic cell, making a direct comparison with the current work problematic. Furthermore, steps used that lead to bottom line estimates for D-HVPE were not provided. Nevertheless, we can draw some conclusions from those earlier estimates. Horowitz, et al. [6] estimate a $2.0/Wp cell

cost of 30% efficiency, low cost Ni/Ag contacts, $90/substrate with 25 reuses and $10/CMP after every 5 reuses. However, this underestimates substrate cost, which is a major determinant of the cell cost. Including more realistic estimates, we find an upside cost of $2.50 - 3.00/Wp.

Indeed, for all the cases, the two major contributions to the cost are substrate cost and growth tool depreciation (see Table 5.5). Cost reductions in machine depreciation are achieved by improved material utilization efficiency, faster growth rates, and optimized photovoltaic cell structure. However, by employing LMBE, the cost of epitaxial growth by all technologies are, to within the unavoidable uncertainties inherent in such analyses, equal and is no longer the primary factor governing the cost of GaAs cell manufacture.

Table 5.5 : Comparison between MBE, LMBE, MOCVD and D-HVPE

	Max. growth rate (μm/hr)	wafers / hr	Material utilization efficiency	Technology status	Precursor required	Solar cell cost (upside case)	Ref.
MBE	3	7	60 - 80%	used in industry	elemental	$8.8/Wp	17
LMBE	3	27	60 - 80%	proposed	elemental	$3.67/Wp	This work
MOCVD	50-60	100 - 120	30 - 50%	used in industry	metalorganic	$3.50 - 4.50/Wp	7
D-HVPE	200	200 - 300	60 - 80%	lab scale demo.	elemental	$2.50 - 3.00/Wp	6

5.8 Conclusion

In summary, we propose a linear MBE system configuration that has the potential to increase the wafer throughput compared to conventional MBE. This approach potentially increases the material utilization efficiency, requires fewer components compared to a conventional MBE

system, while significantly increasing throughput. We estimate a nearly 55% cost reduction in the production of GaAs thin-film photovoltaic cells using LMBE compared to conventional MBE, and further reduction to 85% for optimized processes. With high volume manufacturing reaching to hundreds of MW to GW production demands, substrate and equipment costs can be further reduced compared to the estimates provided here.

Even with these optimistic assumptions, cost of materials, utilities and maintenance still remain above $3.00/Wp, regardless of the growth technology employed. Major cost impacts arise from high substrate cost that can only be reduced by improved substrate recycling techniques, rather than by increased growth rate or optimized processing. Thus, it is unlikely that MW to GW scale production demands will emerge for GaAs photovoltaics. Moreover, considering that the analyses presented here do not include taxes, insurance, labor beyond manufacturing, marketing, rent, etc., we can expect the final cost will be higher than this estimation. This makes the high demand on GaAs solar energy conversion even more difficult to compete with other incumbent technologies such as Si. Nevertheless, for applications where light weight, very high efficiency, or cell flexibility are essential (e.g. for area-constrained or aerospace applications), GaAs photovoltaics will continue to fill a niche that is inaccessible to low cost, commodity Si solar cells. In that case, LMBE provides an opportunity for cost reductions that have not been possible using conventional growth technologies.

Chapter 5

Bibilography

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Chapter 6

A Retina-Like Hemispherical Focal Plane Array

The work presented in this chapter is done in a collaborative manner with our group alumni, Dr. Dejiu Fan. I contributed to fabrication process development, raytracing simulations and measurement setup using 3D printing.

Another benefit of thin-film structures is that they allow fabrication of three-dimensional (3D) shapes where conventional substrate devices are limited to two-dimensional (2D) structures based on standard photolithography patterning process. A light detecting focal plane array (FPA) used in imagers is one example of a system that can benefit from fabrication on curved surfaces. By mimicking the hemispherical shape of the retina in the human eye, a hemispherical FPA provides a low-aberration image with wide field of view. In this chapter, we report a general approach for fabricating electronic circuits and optoelectronic devices on non-developable surfaces by introducing shear-slip of thin-film circuit components relative to the distorting substrate. In particular, we demonstrate retina-like imagers that allow for a topological transformation from a plane to a hemisphere without changing the relative positions of the pixels from that initially laid out on a planar surface. As a result, the resolution of the imager, particularly in the foveal region, is not compromised by stretching or creasing that inevitably results in transforming a 2D plane into a 3D geometry. The demonstration provides a general strategy for realizing high density integrated circuits on randomly shaped, non-developable surfaces.

6.1 Introduction

One extensively studied system that benefits from being shaped into a non-developable hemispherical architecture is the image sensing focal plane array (FPA). It offers significant benefits if a retinal shape can be achieved without changing the interpixel spacing that results in loss of image resolution or image distortion. The retina is the nearly hemispherical light sensitive three-layer structure on the back of human eye on which an image is focused by the lens[1]. In contrast to the shape and size of the retina, high performance photodetector FPAs employed in modern cameras are flat due to limitations of conventional photolithographic fabrication. The imperfect match between planar FPAs and image planes using only a single element convex lens such as that in the human eye results in a degraded image with a limited range of focus, a narrow field of view (FOV), and off-axis optical aberrations[2–5]. Consequently, additional optical elements are required to correct these aberrations that increase the complexity, weight and cost, while often decreasing the functionality of the imaging system.

Many efforts, therefore, have been made to shape the FPA into a hemisphere[6–15]. Fabricating arrays on retina-like hemispherical surfaces[10,11,16,17], however, introduces significant challenges. For example, thinning and deforming commercial CMOS imagers[9,17] (with integrated addressing circuits) provides a high pixel count, although the curvature must remain small to avoid the significant mechanical strain, or distortions such as creasing or folding. Changes in pixel separation that must be corrected to avoid image artifacts, and resolution loss associated with strain are also unavoidable. Larger deformations from a plane to a hemisphere have been achieved by placing bendable and stretchable metal interconnection “bridges” between pixels that relieve strain to create both concave[11] and convex[18] imagers. However, the gaps between pixels reserved for the bridges result in a loss of resolution, particularly near the central “fovea” at the point of maximum

strain. Recently, Origami-inspired hemispherical FPAs were reported[12,13,19] with high deformability and pixel counts that were achieved by cutting, folding and mating sections to form an approximately hemispherical shape. This process does not result in a perfect conformation to a hemisphere, leading to undesirable optical aberrations and image stitching errors.

In this work, we overcome these deficiencies by employing well-established optoelectronics processing techniques to form a thin-film, GaAs FPA on planar, flexible plastic foils. The hemispherical FPA (HFPA) is then achieved by transferring to an elastomeric handle, and then allowing the circuits to shear and slip along the elastomeric surface during distortion; a method first introduced in making organic thin-films detector arrays[10]. Specifically, a 15×15 thin-film GaAs photodiode FPA was fabricated on a flexible Kapton® foil via cold-weld bonding[20], and subsequently non-destructively epitaxially lifted off (ND-ELO)[21,22] from its parent (growth) substrate. The flexible FPA, attached to an elastomeric transfer handle with rows of detectors separated by plasma etching, is then deformed into a hemispherical shape that allows for shear slippage between the elastomer and the array surface and then is transferred to a mating concave hemispherical substrate to achieve the HFPA. The HFPA shows nearly perfect fabrication yield (~99%) and an external quantum efficiency *EQE* > 80% between wavelengths of 650 and 900 nm. Moreover, the noise performance and detectivity are both comparable to commercially available charge coupled detector (CCD) imagers[23]. Note that the fabrication strategy is independent of the semiconductor materials choice and can achieve the same high pixel density on almost any arbitrarily shaped surface as on a planar surface with a continuous first and second derivative.

6.2 Hemispherical Focal Plane Array (HFPA) Fabrication

A GaAs *p-n* junction photodiode array is first fabricated on a flexible, 25 μm thick E-type Kapton® substrate. Details of the array fabrication process are as follows. The photodiode array

employs a 200 nm undoped GaAs buffer layer, 25 nm undoped AlAs sacrificial layer, 25 nm Si-doped (5×10^{18} cm^{-3}) GaAs contact layer, 25 nm Si-doped (1×10^{18} cm^{-3}) $In_{0.49}Ga_{0.51}P$ window layer, 150 nm Si-doped (1×10^{18} cm^{-3}) GaAs emitter layer, 2.5 μm Zn-doped (2×10^{17} cm^{-3}) GaAs base layer, 100 nm Zn-doped (6×10^{17} cm^{-3}) $Al_{0.26}Ga_{0.74}As$ back surface field layer, and 200 nm C-doped (5×10^{18} cm^{-3}) GaAs contact layer that are consecutively grown on an undoped (100) GaAs substrate using molecular beam epitaxy.

Following growth, the surface native oxide is removed in buffered HF for 90 s and rinsed in de-ionized (DI) water for 10 s. A 200 nm Au layer is deposited using e-beam evaporation on the epitaxial surface, and 5 nm Ir and 200 nm Au layers are sputtered onto a 25 μm E-type Kapton® foil. The GaAs sample with epitaxial layer is bonded to Kapton® foil by applying heat (200°C) and pressure (2 MPa) for 5 min under vacuum (10^{-4} mTorr) using an EVG 510 wafer bonder (EV Group Inc., NY, 12203). The bonded sample is then immersed in 17% HF solution maintained at 60°C with 400 rpm agitation for 3 hrs to remove the AlAs sacrificial layer, thereby separating the epitaxial layers from the parent GaAs wafer using non-destructive epitaxial lift-off (ND-ELO)[22].

The Kapton® substrate is fixed to a rigid Si handle to eliminate curling. All layers are photolithographically patterned using LOR 3A (MicroChem Corp., MA, 01581) and SPR 220 3.0 ((MicroChem Corp., MA, 01581) bilayer photoresist. Photodiode mesas (150 μm diameter, 300 μm pixel pitch) are patterned using inductively coupled plasma (ICP) reactive-ion etching (RIE; Cl_2:Ar_2:BCl_3 = 2:5:10 sccm, 5 mTorr pressure, 500 W ICP power, 100 W forward power, 0°C stage temperature for 7 min). The back contact lines (50 μm wide) are wet etched using TFA Au etchant (Transene Company Inc., MA, 01923) to pattern photodiode rows. A 1.2 μm thick polyimide (PI2610, HD Microsystem, NJ, 08859) insulation layer is spin-cast and cured at 250°C for 5 hrs. The polyimide layer is patterned to expose the light detection area and back contact pads

using O_2 plasma (O_2 = 80 sccm, 800 W ICP power, 300 mTorr pressure, 150°C stage temperature for 10 min). Next, the Ti (10 nm) / Au (500 nm) top contact ring is deposited onto the photodiode mesas. A TiO_2 (49 nm) / MgF_2 (81 nm) anti-reflection coating is then patterned on the light detection area. A Ti (10 nm)/ Al (200 nm) etch mask is deposited onto the reverse side of the Kapton® substrate with a pattern that matches the photodiode rows and contact lines on the front substrate surface. Photodiode mesas on the array are connected only in rows, whereas the column connections are not patterned at this point (see Fig. 6.1).

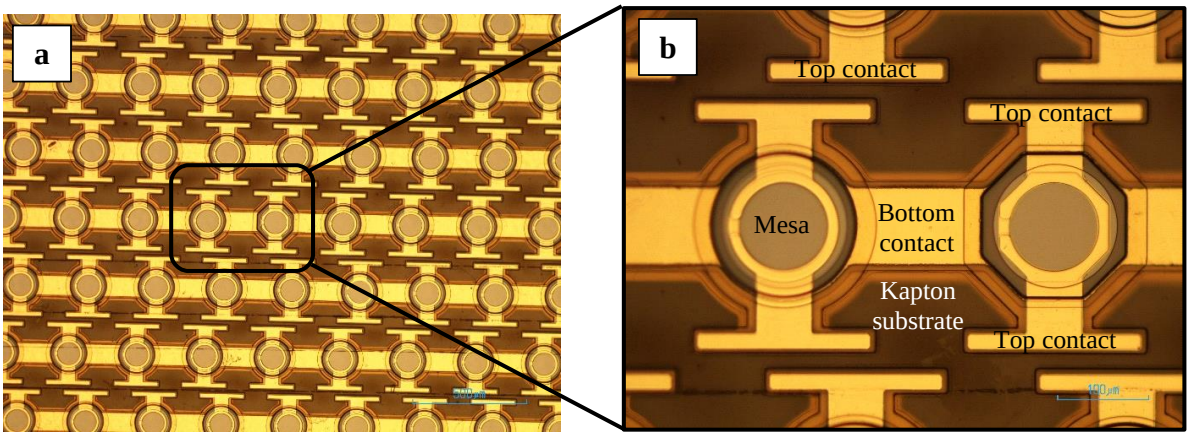

Figure 6.1: Microscopic image of photodiodes array connected in rows.
(a) Microscopic image of photodiodes array connected in rows patterned on 25 μm Kapton substrate. (b) Exploded view of individual photodiode layout. Electrical connections have not been patterned to connect rows of photodiodes.

Separately, a 100 μm PDMS (Sylgard 184, base to curing agent weight ratio = 10 : 1) membrane is spun (800 rpm) on a Si handle pre-treated with a release agent (tridecafluoro-1,1,2,2-tetrahydrooctyl trichlorosilane), and cured at 100°C for 3 hrs. The Kapton® substrate with the detectors facing the membrane is then attached to the PDMS[24,25] as shown in Fig. 6.2 (a). The Kapton® area not covered by the Al mask is removed to separate photodiode rows using O_2 plasma (O_2 = 20 sccm, 6 mTorr pressure, 500 W ICP power, 100 W forward power, 0°C stage temperature for 25 min). The Al mask is then removed using Cl_2 plasma (H_2:Cl_2:Ar = 12:9:5 sccm, 10 mTorr

pressure, 500 W ICP power, 100 W forward power, 0°C stage temperature for 2 min) as shown in Fig. 6.2 (b). This step removes the Kapton® substrate between the rows of detectors, i.e. separates a two-dimensional array plane into individual one-dimensional lines of detectors.

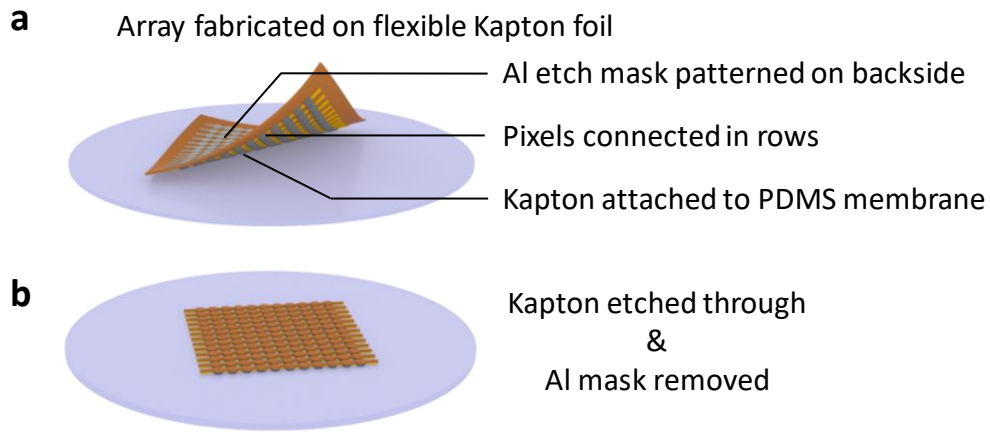

Figure 6.2: Schematic illustration of the key steps of fabricating a hemispherical photodiode array. (a) GaAs *p-n* junction photodiodes array connected in rows fabricated on flexible Kapton® substrate (brown) with Al etch mask (light gray) patterned on the backside is laid flat onto a poly(dimethylsiloxane) (PDMS) membrane (purple). (b) The Kapton® substrate is etched through to the PDMS surface using O_2 plasma. Al etch mask is removed using Cl_2 plasma.

Then, a thin layer of NOA 84 optical adhesive (4000 rpm, Norland Products) is spin-coated, and pre-cured using UV light (0.15 W/cm^2, 1 cm from the sample surface, 2 min) to partially harden the adhesive. The PDMS membrane is peeled from the Si handle, and attached to the bottom of a 3D printed holder (0.5 mm thick, 4 cm × 4 cm square shape with a 2 cm diameter clear aperture in the center for device transfer). The same uncured PDMS is also poured into a plano-concave lens (Thorlabs, LC4942, 12.7 mm diameter, 9.2 mm surface curvature, 4.4 mm edge thickness, 2.0 mm center thickness), and cured at 100°C for 3 hr to form a hemispherical transfer punch. The membrane is then deformed by the centered PDMS punch as shown in Fig. 6.4 (a). The PDMS membrane thus undergoes a topological stretching into a non-developable surface[26] in spite of significant strain (~7% in the center, and ~20% towards the edge, see Fig. 6.3).

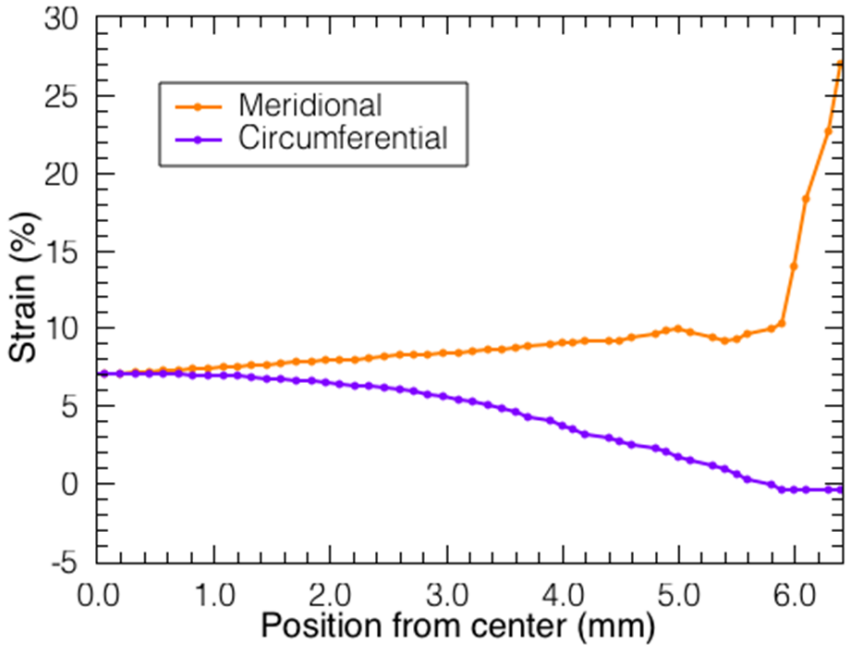

Figure 6.3: Simulated meridional and circumferential strain.
Simulated meridional and circumferential strain in the poly(dimethylsiloxane) (PDMS) membrane upon deformation to the final hemispherical shape using Ansys. The meridional strain in the center is ~7% and it increases dramatically to over 20% towards the edge of the hemisphere.

The pixels, however, do not change their spacing during stretching. The inset of Fig. 6.4 (a) shows cross-sectional views of the array and PDMS membrane in XZ and YZ-planes. In the XZ-plane, detectors (gray) together with in-row connections (yellow) and the etched Kapton® (brown) move freely along the X-direction without longitudinal strain when the PDMS membrane (blue) is stretched. In the YZ-direction, however, the detectors and connections are constrained by the Kapton® film, and hence they shear along the PDMS stretched in the Y-direction. The shear along the membrane surface is allowed without strain due to the weak adhesion at the detector/PDMS interface (see Fig. 6.5)[10].

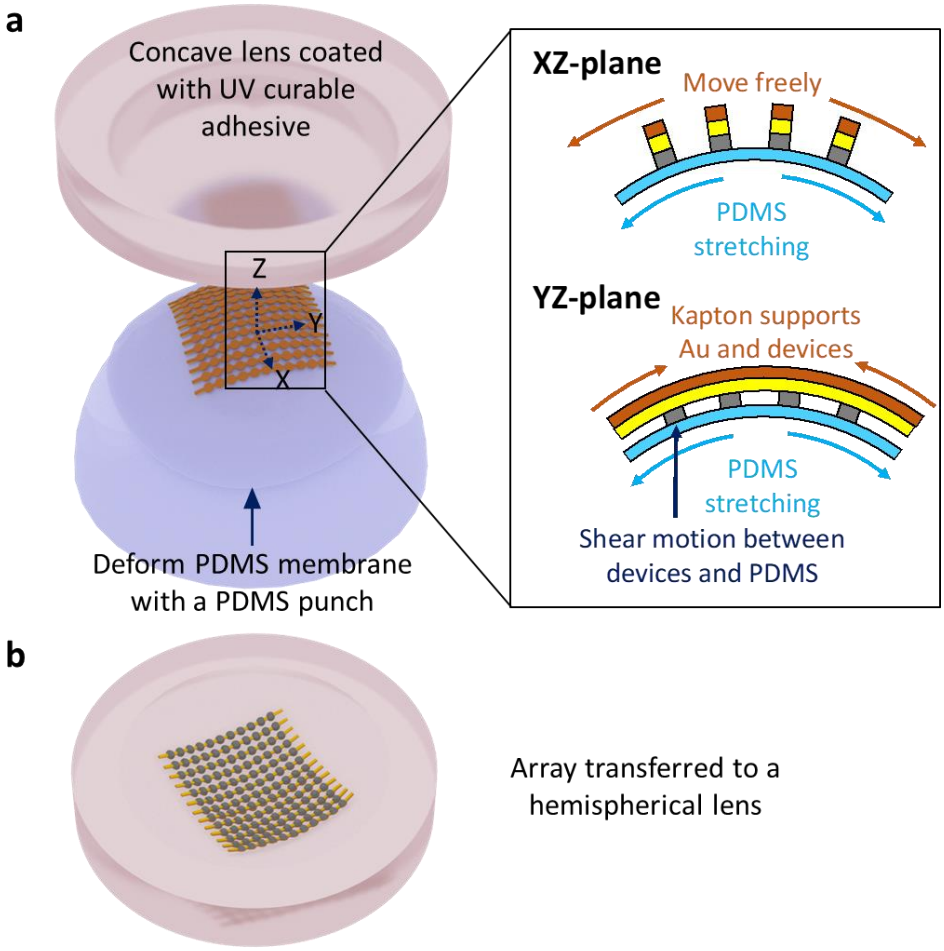

Figure 6.4: Schematic illustration of the key steps of deformation.
(a) The PDMS membrane that supports the array is fixed on its edges and deformed by a centered PDMS hemispherical punch. The array is transferred to a matching hemispherical concave glass lens coated with UV curable adhesive. Inset: Cross-section views from XZ-plane and XY-plane during the deformation process. Kapton® substrate (brown) supports Au connection lines (yellow) and photodiodes mesas (gray) when PDMS membrane (blue) is stretched. Rows of pixels are free to move in X-direction and have shear motion with PDMS membrane in Y-direction. (b) Array (connected in rows) transferred to the concave glass lens.

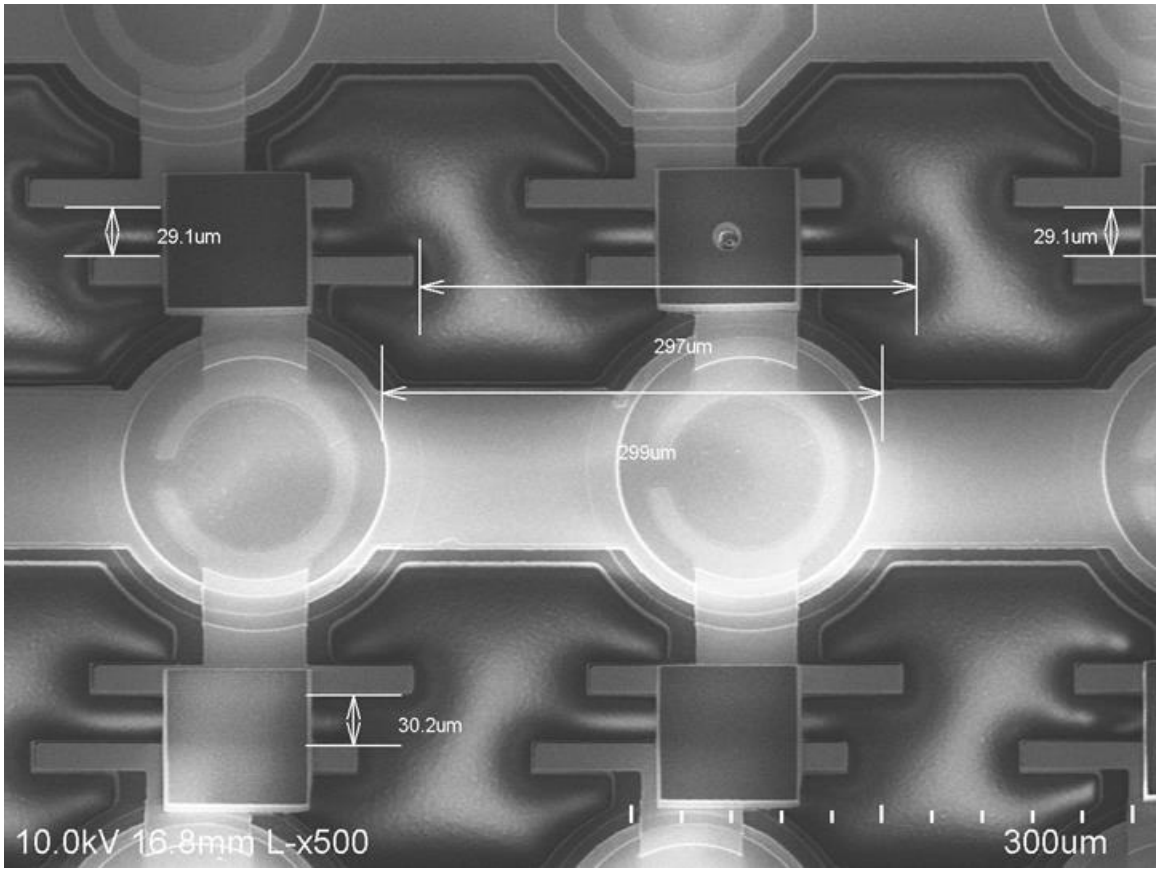

Figure 6.5: SEM image of individual pixels around the center of a fully fabricated (dummy) hemispherical focal plane array.
The designed distance between pixels is 300 μm. The measured distance between pixels in the horizontal direction in this figure (Y-direction in the inset of Figure 6.4 (a)) is approximately 300 μm. This result demonstrates that the photodiodes rows supported by Kapton substrate have no elongation in the horizontal direction during the stretching of PDMS membrane and transferring of the array. The designed gap between rows is 10 μm. The measured distance between pixels in the vertical direction in this figure (X-direction in in the inset of Figure 6.4 (a)) is approximately 30 μm. This result demonstrates that the photodiodes rows supported by Kapton® substrate have ~6.7% additional separation (30 μm = 10 μm gap + 300 μm pitch size × 6.7%) in the vertical direction during the stretching of PDMS membrane and transferring of the array. This result agrees with our simulated value (7%) in Figure 6.3 within measurement variation.

Shear-slip motion on PDMS has previously been observed and characterized in both organic[10] and inorganic[27] semiconductor systems. The governing factor that enables the slip is that the strain energy release rate must exceed the interface bonding energy between the surfaces. For typical inorganic semiconductor/PDMS interfaces, the slip can occur for shear strains is > 7%[27]. In addition, due to the high Young's modulus of the 25 μm thick Kapton® film (~10^3 times higher than PDMS), the stress along the detector rows induced by PDMS stretching is well below the

yield strength, and the strain in the thin film can thus be ignored. Generally, shear-slip motion and non-developable deformation is applicable to any circuit structure as long as the shear-induced energy release rate exceeds the interface binding between the circuit and the substrate transfer stamp, and the stress induced by PDMS stretching does not exceed the material yield strength of the circuit materials. It is worth mentioning that the relative positions of the top (light absorbing) surfaces of detectors on a row do suffer minor shrinkage due to the bending of the Kapton® film. More controllable geometries can be achieved by employing pre-distortion offsets of the pixel spacings during fabrication on the planar surface to achieve the target pixel spacings after transfer.

Next, the deformed array is brought into intimate contact with a hemispherical concave lens (Thorlabs, LC4942) coated with the same NOA 84 optical adhesive. The adhesive is fully cured (0.15 W/cm^2, 1 cm from the sample surface, 5 min), after which the lens and PDMS membrane are separated to complete the transfer (Fig. 6.4 and Fig. 6.2 (b)). The residual adhesive is removed from the concave lens surface using O_2 plasma (O_2 = 80 sccm, 800 W ICP power, 300 mTorr pressure, 150°C stage temperature for 40 min).

The approach described in Fig. 6.2 and Fig. 6.4 transforms the two-dimensional tensile strain introduced during deformation to a simple separation and one-dimensional bending process. It maintains the pixel spacing before and after deformation in the Y-direction. In the X-direction, a second layer of detector rows can be applied in the same manner to fill in the gaps that arise during application of the first layer during stretching as shown in Fig. 6.6.

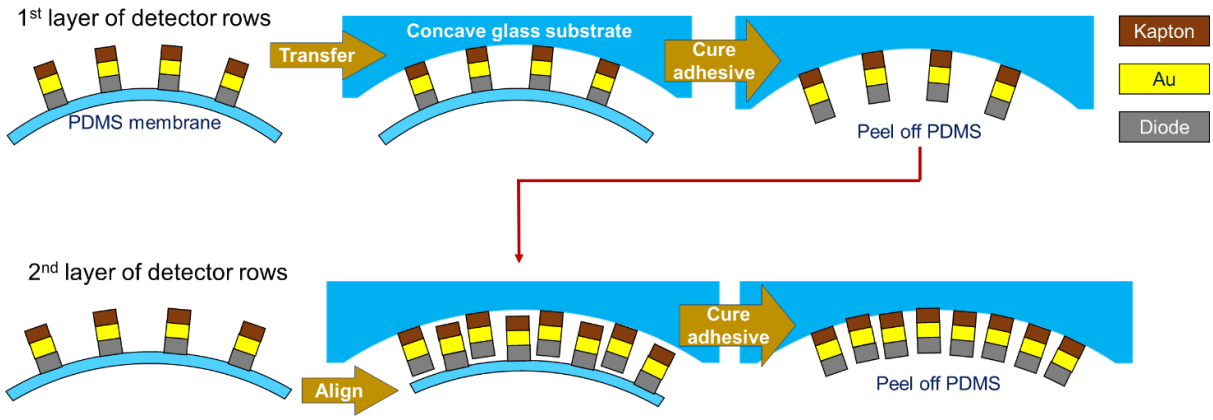

Figure 6.6: Schematic illustration of transferring a second layer of detector rows.
A second layer of detector rows can be applied in the same way as the first layer to fill the gaps that arise during application of the first layer during stretching. During the application, the second layer of detector rows is attached to the PDMS membrane and deformed by a PDMS punch. It is fixed on a 6-axis manual transfer stage that has X,Y, and Z axes translation and X,Y, and Z axes tilt. The top concave substrate with the first layer of detector rows transferred is fixed above the transfer stage. A stereo-microscope is used to observe from the top to align the concave substrate and the 2nd layer of detector rows. This step can be executed the same way as the application of metalized pads that connect rows of detectors. The result of such aligned transfer process on two hemispherical surfaces is demonstrated in both Figure 6.5 and Figure 6.7.

Finally, an array of metalized Kapton® pads is patterned and transferred to the concave substrate to connect rows of detectors and form the column connections (Fig. 6.7). The approach described here is compatible with batch fabrication of imagers (Fig. 6.8) with many high performance materials including, but not limited to Si, GaAs, InGaAs, and etc.

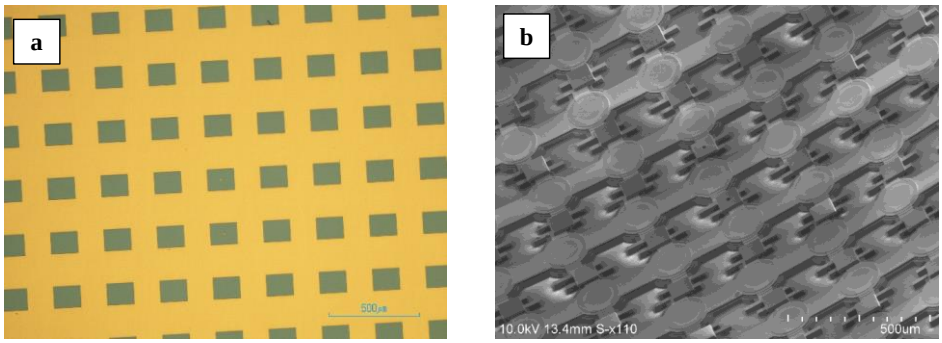

Figure 6.7: Metalized Kapton® pads for column connections.
(a) Microscopic image of photolithography mask of column connection pads. (b) SEM image of column connection pads transferred to the hemispherical concave substrate on top of the transferred rows of photodiodes. They are aligned between rows of photodiodes and enable column electrical connections.

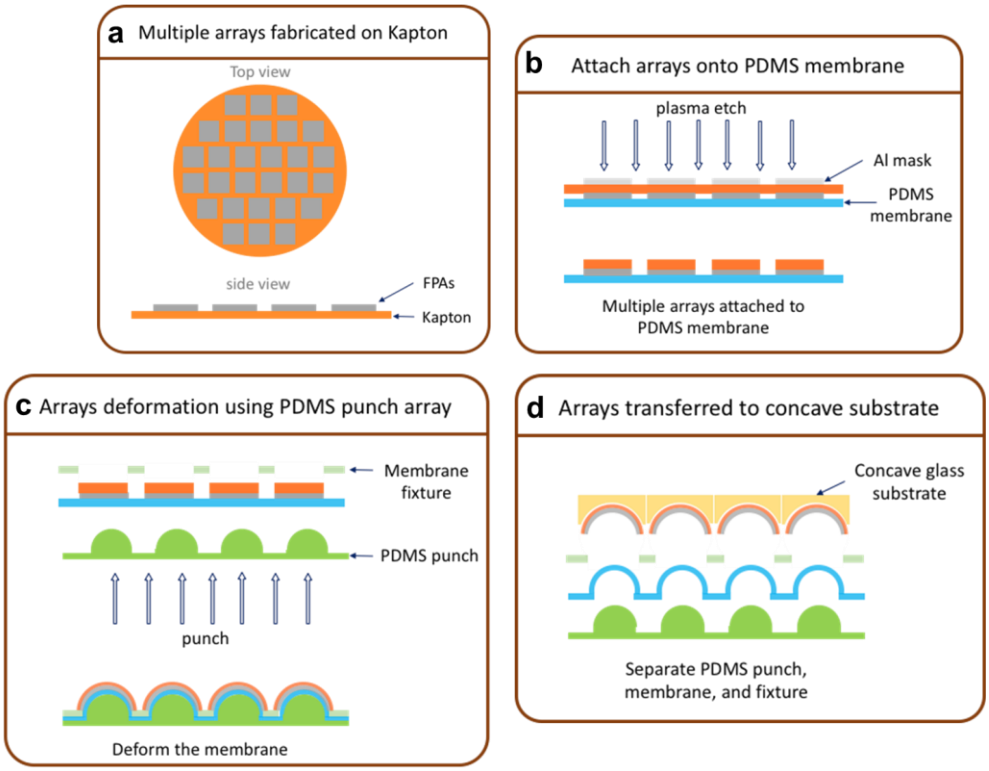

Figure 6.8: Schematics of the batch fabrication of multiple hemispherical focal plane arrays (FPAs). (a) Multiple FPAs (gray) fabricated on Kapton® film (red). (b) Attach the Kapton® film onto PDMS membrane and etch Kapton® to separate FPAs using plasma. (c) Attach the membrane using a fixture with apertures centered to FPAs and deform the membrane with a PDMS punch array centered to FPAs. (d) Transfer multiple FPAs simultaneously to concave glass substrates, separate PDMS punch, membrane, and fixture. Batch fabrication of multiple hemispherical FPAs can be achieved.

6.3 Device characterization

Fig. 6.9 (a) shows a GaAs *p-n* photodiode HFPA fabricated on a truncated concave hemispherical glass substrate with a radius of curvature = 9.2 mm, depth = 2.5 mm, and opening diameter = 12.7 mm. The 15×15 pixel array is centered within the substrate depression, providing high resolution foveal imaging capability. A secondary, 4×2 pixel array is located along the lip of the depression that is transferred at the same time as the central array. It provides peripheral, but low-resolution vision similar to that sensed by the human eye. Furthermore, its application demonstrates the ability to transfer devices at angles > 43° to provide a very large FOV[28].

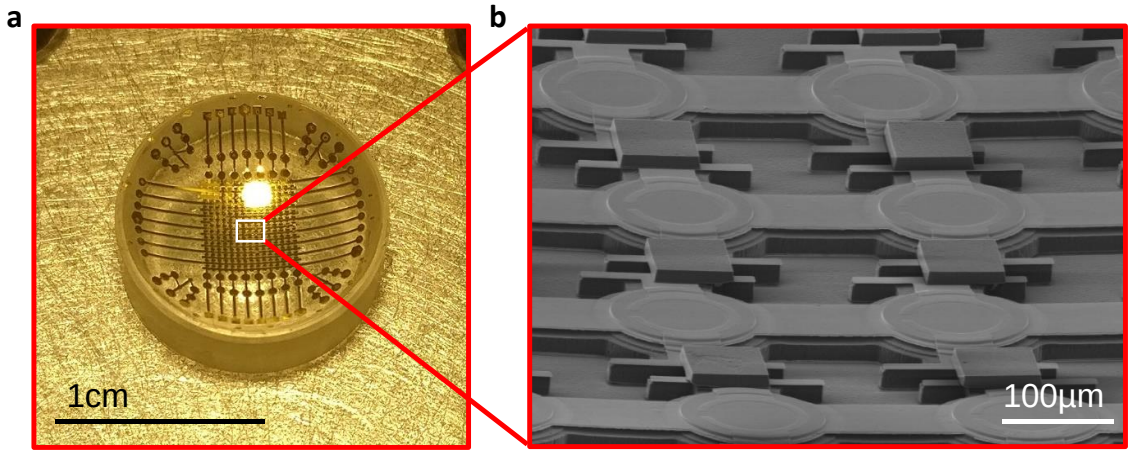

Figure 6.9: Images of a 15×15 pixel GaAs *p-n* junction FPA fabricated on a concave hemispherical surface. (a) Photograph. Additional 4×2 peripheral pixels that allow for motion detection at wide angles of view are also shown. (b) Scanning electron microscopic image of a portion of the photodiode array.

The scanning electron microscopic image in Fig. 6.9 (b) provides a detailed view of the pixels shown in Fig. 6.9 (a). No metal or semiconductor cracks are observed as typically encountered for free-standing metal films subjected to similarly substantial strain[10,29,30]. Metalized Kapton® pads between the pixels form top electrical connections that enable the column readout of the HFPA. Lateral misalignment between rows is due to the asymmetric shear slippage during deformation and transfer. This issue can be solved by designing the array with a compensating offset between rows during fabrication prior to deformation.

Figure 6.10 is a schematic illustration of the photodiode pixel in the array. Each 150 μm diameter photodiode is connected in rows with adjacent pixels (300 μm center-to-center spacing) through the 50 μm wide bottom contact lines supported by the 60 μm wide Kapton® foil strips. Top contact rings are extended out of the photodetection area with 150 μm × 20 μm contact pads, and connected to adjacent units through a separately transferred layer of 80 μm × 60 μm column connection pads. An anti-reflection coating (ARC) is deposited on the top to enhance the optical absorption in visible spectrum.

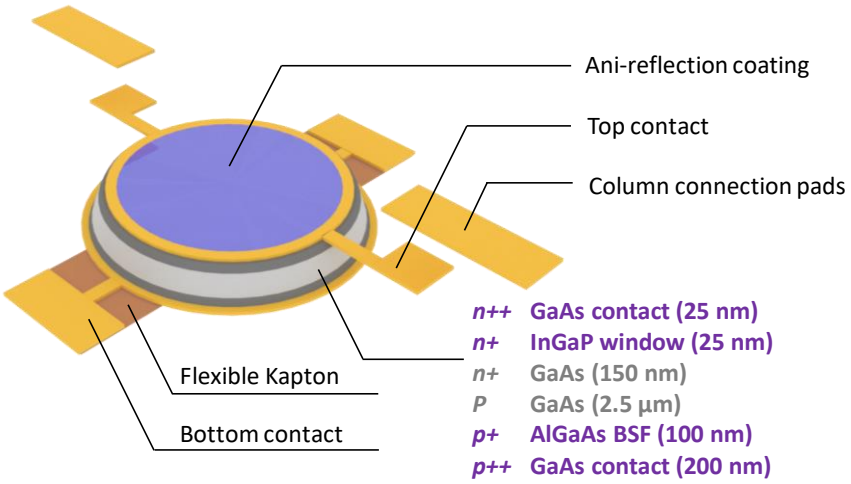

Figure 6.10: Schematic of a single pixel in the array.

The current-voltage (*I-V*) characteristics of a photodiode under dark and 64 nW illumination at a wavelength of λ = 530 nm are shown in Fig. 6.11 inset. The *I-V* characteristics are measured using a Keithley 2400 Source Measuring Unit (SMU). The dark current is 1.3 ± 0.4 nA (corresponding to 7.4 ± 2.1 µA/cm^2) at -1 V for individual detector. The current under illumination is 18.5 nA at 0 V and 23.3 nA at -1 V.

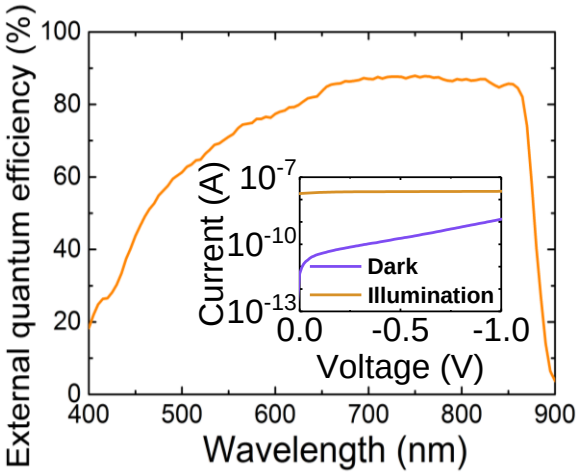

Figure 6.11: *EQE* and *I-V* characteristics.
External quantum efficiency (*EQE*) spectra of the photodiode in the wavelength range from 400 to 900 nm. Inset: Current-Voltage (*I-V*) characteristics of the photodiode in the dark (blue line) and under 64 nW, 530 nm light emitting diode (LED) illumination (orange line).

Figure 6.11 presents the external quantum efficiency, *EQE*, spectrum of a photodiode. *EQE* is measured using monochromatic illumination chopped at 200 Hz and coupled into a FG050LGA optical fiber oriented normal to the photodiode using a Lightwave Probe (Cascade Microtech, CA, 94551). The output signal is collected by a SR830 lock-in amplifier. The light illumination power is calibrated using a reference 818-UV/DB Si detector (Newport, CA, 92606). We observe *EQE* > 80% at λ > 650 nm, which to our knowledge is the highest reported for other hemispherical imagers[10–13,19]. The photodetector noise equivalent power is $NEP = \sqrt{2qI_D}/R(\lambda)$ under shot-noise-limited detection at -1 V, where q is the electron charge, I_D is the dark current, and $R(\lambda)$ is the responsivity at a given wavelength λ. With *EQE* = 67.7% at λ = 530 nm, then $R(\lambda) = 0.29\ A/W$, and $NEP = 7.03 \times 10^{-14}\ W/Hz^{1/2}$. The specific detectivity of the detector is $D^* = \sqrt{A\Delta f}/NEP$, where A is its area, and Δf is the bandwidth, giving $D^* = 1.89 \times 10^{11}\ cm \cdot Hz^{1/2} \cdot W^{-1}$ in a 1 Hz bandwidth. The NEP and D^* are at the same order of magnitude as that of commercially available CCD imagers[23].

The normalized dark current map and the histogram in Fig. 6.12, indicate the yield of the 15×15 photodiode array is > 99% (223/225 photodiodes have a leakage current < 40 nA at -1 V. The dark current of the detectors on the array is 9.1 ± 7.9 nA at -1 V, which is approximately 7 times greater than for individual detectors due to sneak reverse currents from adjacent detectors. This can be eliminated by using a passive pixel sensor address transistor[31] at each pixel that can be transferred simultaneously with the detectors without change or complication to the existing process.

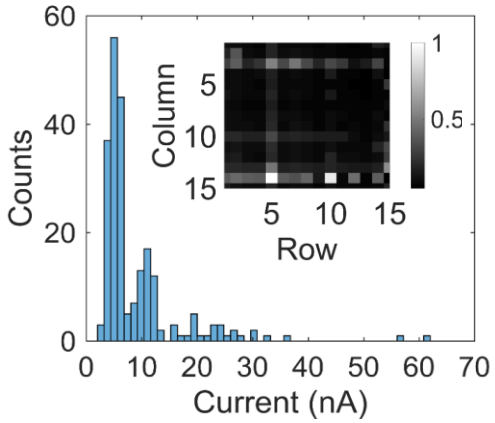

Figure 6.12: Dark current mapping.
Histogram of dark current of photodiodes on the 15×15 FPA. Inset: Normalized dark current maps of the 15×15 GaAs focal plane array (FPA) on hemispherical surface.

As shown in Fig. 6.13, the detector dynamic range is determined from the detector photocurrent (black square) at λ = 850 nm vs. incident optical power. A photocurrent compression of 1 dB from linear response (red line) sets the maximum intensity, P_1, whereas P_0 is the lowest detectable optical power (root-mean-square noise power). The dynamic range is $DR = 10\log(P_1/P_0)$. At 0 V, P_0 = 10^{-4} W/cm^2, P_1 = 10^{-1} W/cm^2, giving DR = 30 dB, corresponding to a 10-bit gray-scale resolution.

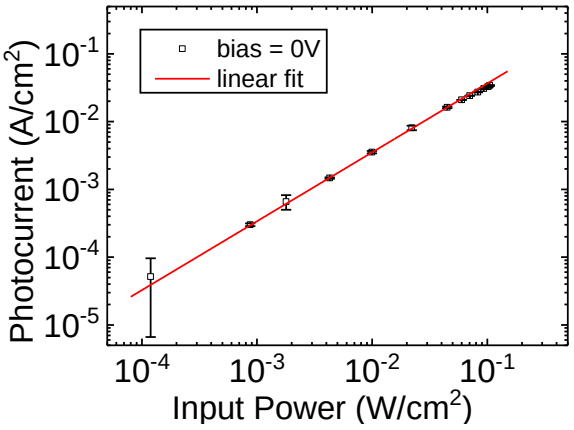

Figure 6.13: Photocurrent vs. input optical power of a single photodetector.
Red line shows a linear fit to the photocurrent at low input optical power. The minimum detectable power is about 10^{-4} W/cm^2, and the 1 dB compression point is at 0.1 W/cm^2, giving a 30 dB dynamic range and a 10-bit gray-scale resolution.

6.4Imaging with HFPA

A conventional imaging system based on a planar FPA has a mismatch with the image plane of a single element lens. Producing a high resolution image thus necessitates additional optical elements that increase the complexity, weight and cost of the system, while restricting the FOV. Using an HFPA, however, provides the possibility of using a single plano-convex lens, whose optical field curvature is matched with that of the curvature of the FPA to produce high quality images[2,3,5].

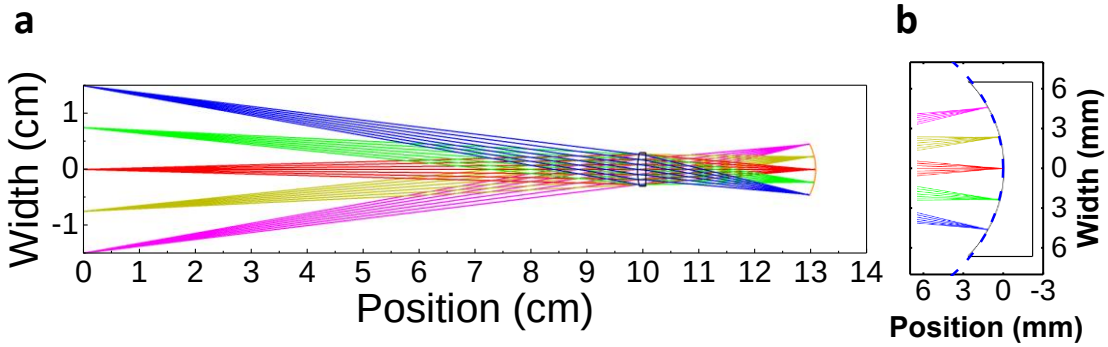

Figure 6.14: Ray tracing simulation.
(a) Ray tracing simulation result of an object (3 cm wide) located 10 cm from a plano-convex lens (black contour). Rays from the object are focused by the lens onto the FPA surface (orange curve, 3.0 cm from the lens). (b) Magnified view around the hemispherical imager (black contour). The simulated lens focal surface (blue dashed line) has good overlap with the concave FPA surface (front curve of the black contour).

As shown in Fig. 6.14 (a), multiple rays illuminated from five point-sources (3 cm wide) positioned at the origin can be focused onto the curved plane of the HFPA centered at 3.0 cm from the lens at a distance of 10 cm. This image plane has a radius of curvature of R = 9.2 mm in the center, and gradually increases to 10.1 mm towards the edge as shown by the blue dashed line in Fig. 6.14 (b). An HFPA (black contour in Fig. 6.14 (b)) with R = 9.2 mm is positioned coaxially with the lens. The simulated results in Fig. 6.15 show a spot size of 13.4 μm and 38.3 μm for the images of point sources in the center and on the edge, respectively, corresponding to a 1.8 times

edge defocusing. In comparison, when a planar FPA is located at the same position as the HFPA, the simulated spot sizes are 13.4 μm and 73.9 μm, corresponding to a 4.5 times edge defocusing.

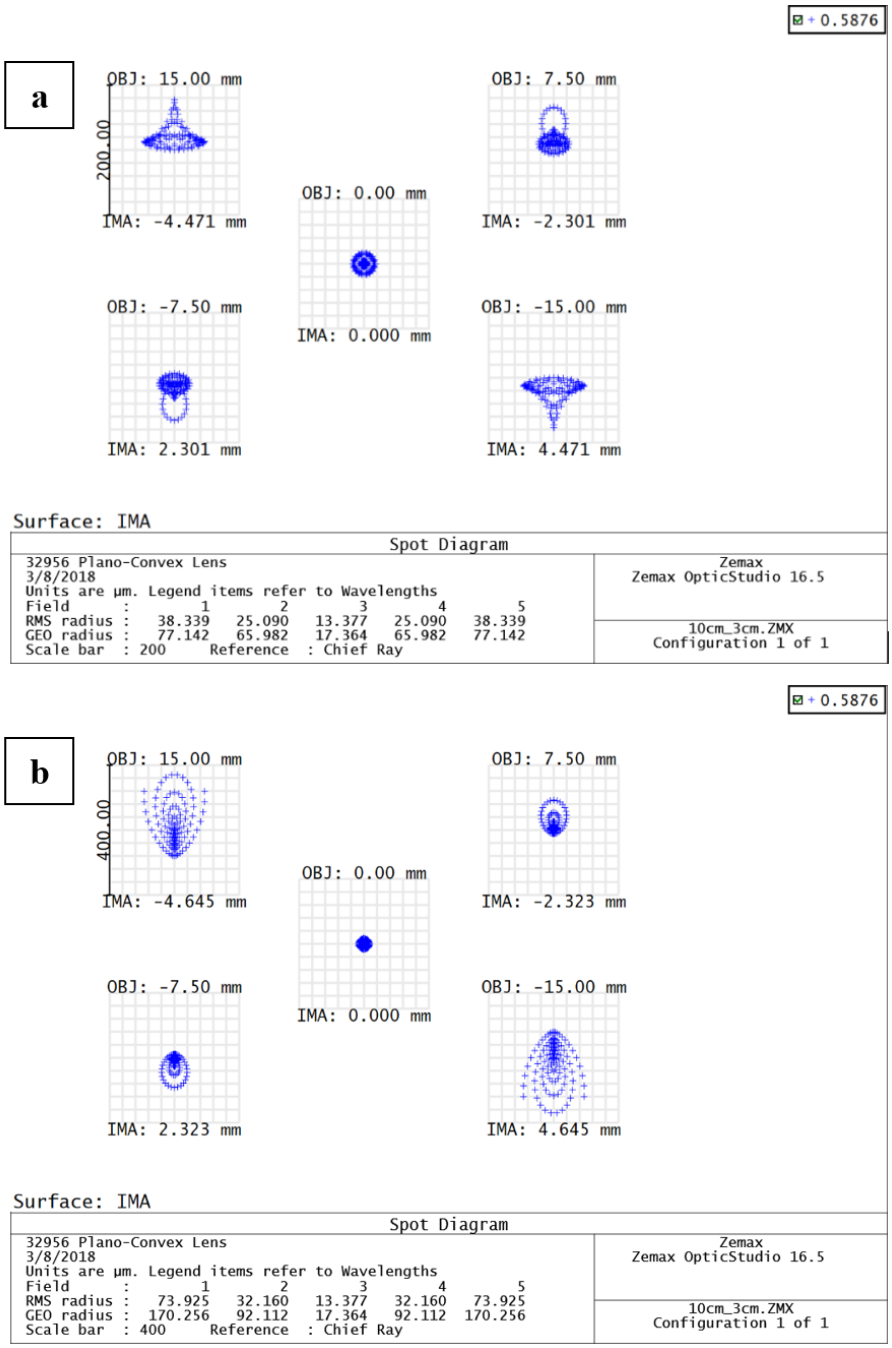

Figure 6.15: Ray tracing simulation spot diagram of a curved image surface using ZeMax.
(a) Each group of spots correspond to the focusing rays on the curved image surface shown in Figure 6.14 (b). Center ray has a spot radius of 13.4 μm, while the ray on the edge has a spot radius of 38.3 μm, showing 1.8 times edge defocusing. (b) Spot diagram of the same light sources focused on a planar image surface. Center ray has a spot radius of 13.4 μm, while the ray on the edge has a spot radius of 73.9 μm, showing 4.5 times edge defocusing.

A single-lens imaging system using the fabricated HFPA is shown in Fig. 6.16. Object imaging is measured using a 48-channel probe card (AccuProbe, MA, 01970) interfaced with a Keithley 2400 SMU and a Keithley 2700 + Keithley 7705 switching unit. A customized LabView graphic user interface is programmed to collect output signals. A schematic of the signal collection mechanism is shown in Fig. 6.16 and Fig. 6.17. The HFPA was mounted on a 3D printed substrate holder. Row and column electrical contacts are extended to the edge of the substrate holder and connected to a 48-channel probe card that is interfaced to the read-out electronics. The plano-convex lens (diameter = 6 mm, focal length = 24 mm) is mounted on a 3D printed lens holder and plugged into the substrate holder. The resulting system is mounted on a six-axis optical stage to capture images as shown in Fig. 6.16 (b).

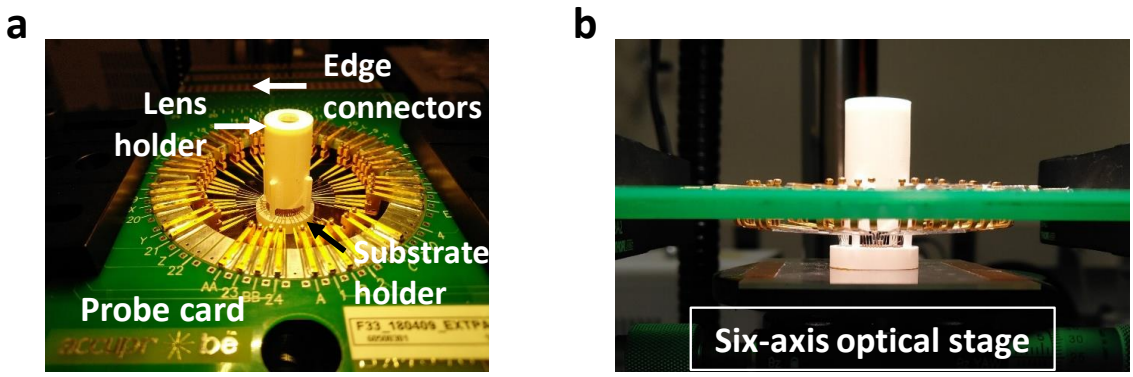

Figure 6.16: Photograph of the HFPA mounted on testing stage.
(a) HFPA mounted on a 3D printed substrate holder integrated with a 3D printed lens holder. Also presented is a 48-channel probe card used to read currents generated by all pixels on the hemispherical FPA simultaneously. (b) Side view of the experimental setup for imaging acquisition.

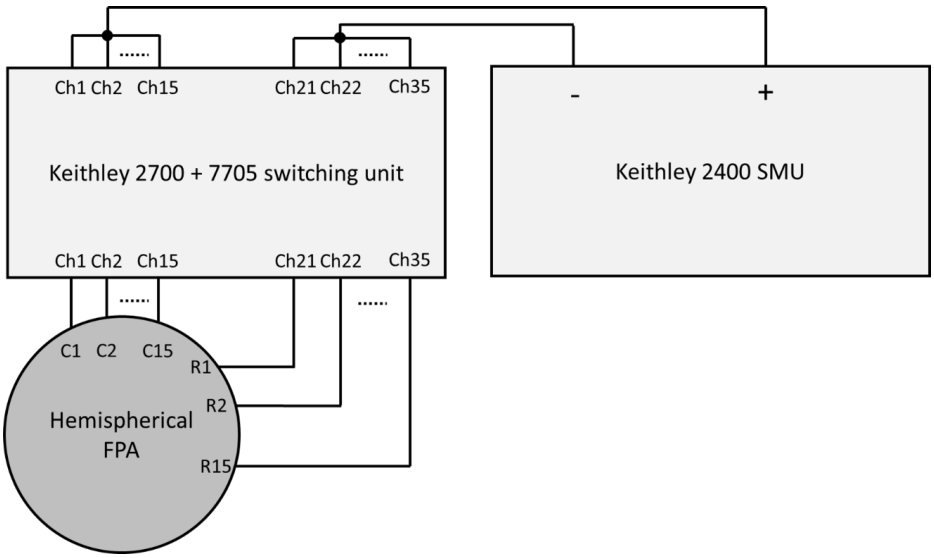

Figure 6.17: Schematics of the image acquisition mechanism.
15 rows and 15 columns of the hemispherical FPA are electrically contacted simultaneously using a probe card. Assign columns to the input channels 1 to 15 on a switching unit, and assign rows to the input channels 21 to 35. The output channels 1 to 15 are wired together and connected to the driving voltage port of an SMU. The output channels 21 to 35 are wired and connected to the SMU ground. The current generated by a specific pixel, for example row 1 and column 1, can be addressed by switching on channels 1 and 21 while leaving all other channels off, and running SMU to collect signal.

The diffuse emission from a λ = 525 nm LED illuminates an image formed by a glass slide patterned with 1 cm wide “O”, “C”, and “M” apertures. Applying a leakage (sneak) current threshold of 15.8 nA, the images of these letters are acquired as shown in Fig. 6.18. The lens provides the HFPA with a calculated array angular coverage of ~15°, and a field of view of approximately 112°. This is demonstrated by focusing the LED source (3 mm diameter) to ~60° from the optical axis of the lens. The edge detectors on the HFPA generate a photocurrent two orders of magnitude larger than in the absence of the light source with a power of 23.2 nW. This demonstrates the object detection ability of the HFPA at a large viewing angle.

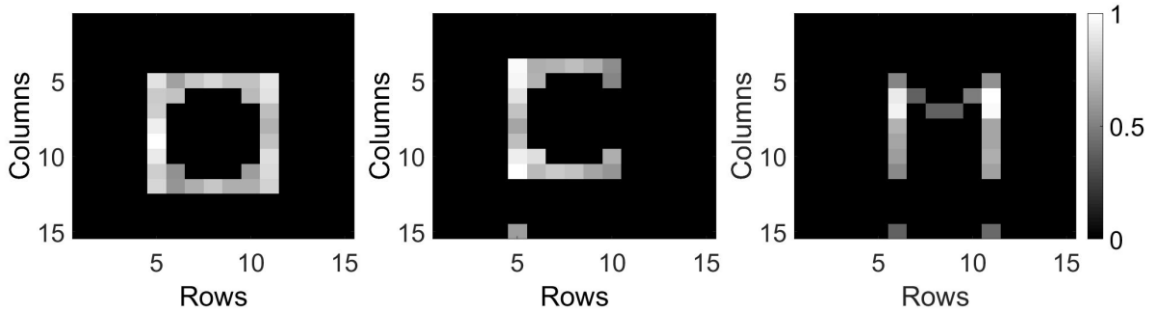

Figure 6.18: Normalized photocurrent map.
Normalized photocurrent map on the 15×15 FPA showing images of letter "O", "C", and "M". A leakage current threshold of 15.8 nA is applied to minimize obscuration of the images by the background sneak currents.

6.5 Conclusion

We demonstrate a general strategy to achieve topological transformations of optoelectronic devices from a 2D plane into a 3D surface by exploiting slippage of the circuits during deformation. We use this process to demonstrate retina-like hemispherical imagers by starting on a planar substrate, and then transferring the array onto a hemispherical surface without loss of array resolution. This process results in defect-free metal interconnections and a fixed pixel spacing. The HFPA has an individual detector performance comparable to that found in conventional planar CCD imagers. The hemispherical shape enables simplified optical designs with reduced aberrations along with a large FOV. Pixel density and counts similar to those in commercial CMOS imagers can be achieved with high precision optics and the integration of access transistors in each cell. The combination features and fabrication strategies demonstrated in this work introduce processing techniques and performance advantages that may lead to new capabilities of next generation conformable and foldable optoelectronic devices.

Chapter 6

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Chapter 7

Near-Field Thermophotovoltaics for Efficient Heat to Electricity Conversion at High Power Density

The work presented in this chapter is done in a collaborative manner with Dr. Rohith Mittapally from Professor Pramod Reddy and Professor Edgar Meyhofer's group in mechanical engineering department at the University of Michigan. My contributions in this work are the epitaxial growth of InGaAs near-field themophotovoltaic cell using molecular beam epitaxy, device design, fabrication and characterization. Detailed information regarding the Si emitter fabrication and measurement setup can be found in : (https://doi.org/10.1038/s41467-021-24587-7).

Thermophotovoltaic approaches that take advantage of near-field evanescent modes are being actively explored due to their potential for high-power density and high-efficiency energy conversion. However, progress towards functional near-field thermophotovoltaic devices has been limited by challenges in creating thermally robust planar emitters and photovoltaic cells designed for near-field thermal radiation. Here, we demonstrate record power densities of ~5 kW/m^2 at an efficiency of 7.3 %, where the efficiency of the system is defined as the ratio of the electrical power output of the PV cell to the radiative heat transfer from the emitter to the PV cell. This was accomplished by developing novel emitter devices that can sustain temperatures as high as 1270 K and positioning them into the near-field (<100 nm) of custom-fabricated InGaAs-based thin film photovoltaic cells. In addition to demonstrating efficient heat-to-electricity conversion at high power density, we report the performance of thermophotovoltaic devices across a range of emitter

temperatures (~800 K – 1270 K) and gap sizes (70 nm – 7 μm). The methods and insights achieved in this work represent a critical step towards understanding the fundamental principles of harvesting thermal energy in the near-field.

7.1 Introduction

Direct conversion of heat to electricity is expected to play a critical role in developing novel thermal energy storage and conversion[1] technologies. Thermophotovoltaic (TPV) devices that are composed of a hot thermal emitter and a photovoltaic (PV) cell are currently being actively explored for such energy conversion applications. In TPV devices electromagnetic radiation emitted by a hot body, when incident on a PV cell, generates electrical power via the photovoltaic effect (see reviews[2,3]). The performance of a TPV system is characterized by two metrics: efficiency, which is defined as the ratio of electrical power output to the total radiative heat transfer from the hot emitter to the PV cell at room (or ambient) temperature, and the power density that is the electrical power output per unit area. Recently, efficiencies of up to 30% in the far-field have been reported[4,5], where the emitter (at ~1450 K) and the PV cell are separated by distances larger than the characteristic thermal wavelength. However, the power densities of far-field TPV systems are constrained by the Stefan-Boltzmann limit, since only propagating modes contribute to energy transfer. This limit can be overcome by placing the hot emitter in close proximity (nanoscale gaps) to the PV cell, where, in addition to the propagating modes, evanescent modes also contribute and dominate the energy transfer. The enhancements in heat transfer via near-field (NF) effects have long been predicted[6–8] and directly demonstrated in recent work[9–13], paving the way for TPV applications. In fact, several computational studies[14,15,24–27,16–23] have suggested that it is possible to achieve high-power, high-efficiency TPV energy conversion via NF effects.

In spite of these predictions, few experiments have probed NFTPV energy conversion. This limited progress is due to multiple challenges associated with creating thermal emitters that are robust at high temperatures, creating high-quality PV cells for selectively absorbing above-band gap NF thermal radiation and maintaining parallelization while precisely controlling the gap between the heated emitter and the PV cell. Recently, a NFTPV system developed by some of us (using a Si emitter and an InAs cell) demonstrated significant enhancements in power output compared to the far-field[28] but featured very low efficiencies (<0.1 %) and low power output (~6 W/m^2). Further, two other experiments also reported large enhancements in power output compared to the far-field by employing different experimental platforms[29,30]. Nevertheless, all of these demonstrations show limited efficiency and power density, with the best-reported device[29] (using a Si emitter and an InGaAs cell) featuring a maximum efficiency of ~0.98% at a power density of ~120 W/m^2 when operated at a maximum temperature of 1040 K. More recently, another work[31] probed the principles of NFTPV energy conversion in a sphere-plane geometry using a spherical graphite emitter and InSb PV cells that were cryogenically cooled. However, given the significant energy expenditure in cooling such devices, the overall efficiency is expected to be comparable to, or lower than those previously reported. Thus, high performance NFTPV demonstrations were limited due to emitters operating at relatively low temperatures and PV cells with poor performance.

7.2 Fabrication of the InGaAs near-field TPV devices

A schematic diagram of the fabrication process for the PV cell is shown in Fig. 7.1. (Step 1) The PV cell fabrication starts with the epitaxial growth of a lattice-matched, inverted *P-n-N* heterostructure on a 2 inch, 350 μm thick, single-side polished, Zn-doped, (100) InP substrate using a GENxplore Molecular Beam Epitaxy system (Veeco Corp.). The structure comprises of a

200 nm undoped InP buffer layer, 200 nm Be-doped (1×10^{18} cm^{-3}) $In_{0.53}Ga_{0.47}As$ (InGaAs) top contact layer, 200 nm Be-doped (1×10^{18} cm^{-3}) InP front window layer, 1 μm Si-doped (1×10^{17} cm^{-3}) InGaAs absorption layer, 100 nm Si-doped (1×10^{18} cm^{-3}) InP back window layer and 100 nm Si-doped (1×10^{18} cm^{-3}) InGaAs bottom contact layer. (Step 2) The PV structure is rinsed in buffered HF (BHF) for 90 s, followed by deposition of an Au/Parylene-C (400/1000 nm) bottom contact and bonding layer via sputtering and physical vapor deposition. Subsequently, the wafer is bonded, via thermal compression bonding (150˚ C, 500 kPa, 5 min) onto a 500 μm Si handle coated with 1 μm Parylene-C. (Step 3) The Si/Parylene/Au/PV/InP stack is submerged in HCl: H_2O (1:1) solution with Si handle facing down for 24 hrs, to remove InP substrate. After removal of the InP substrate, the top surface of the PV device was immediately cleaned using NH_4OH brushing and megasonic cleaning. (Step 4) The PV mesa is defined using standard photolithography and wet etching. Citric acid: H_2O_2 (4:1) and HCl: H2O (1:1) solutions are used for etching the InGaAs and InP layers, respectively. (Step 5) The Ti/Pt/Au (10/30/1000 nm) top contact layer is patterned via standard photolithography and electron beam deposition. (Step 6) A polyimide insulating layer (PI-2555) was spin-coated and annealed at 200°C for an hour, and then patterned via standard lithography and RIE plasma etching to define the device active area and bottom contact pad openings. (Step 7) The Ti/Au (5/1000 nm) top contact pad is patterned via standard photolithography and electron beam deposition. Finally, the top InGaAs contact layer is etched using a citric acid: H_2O_2 (4:1) solution to expose the active area of the PV cell and prevent parasitic absorption.

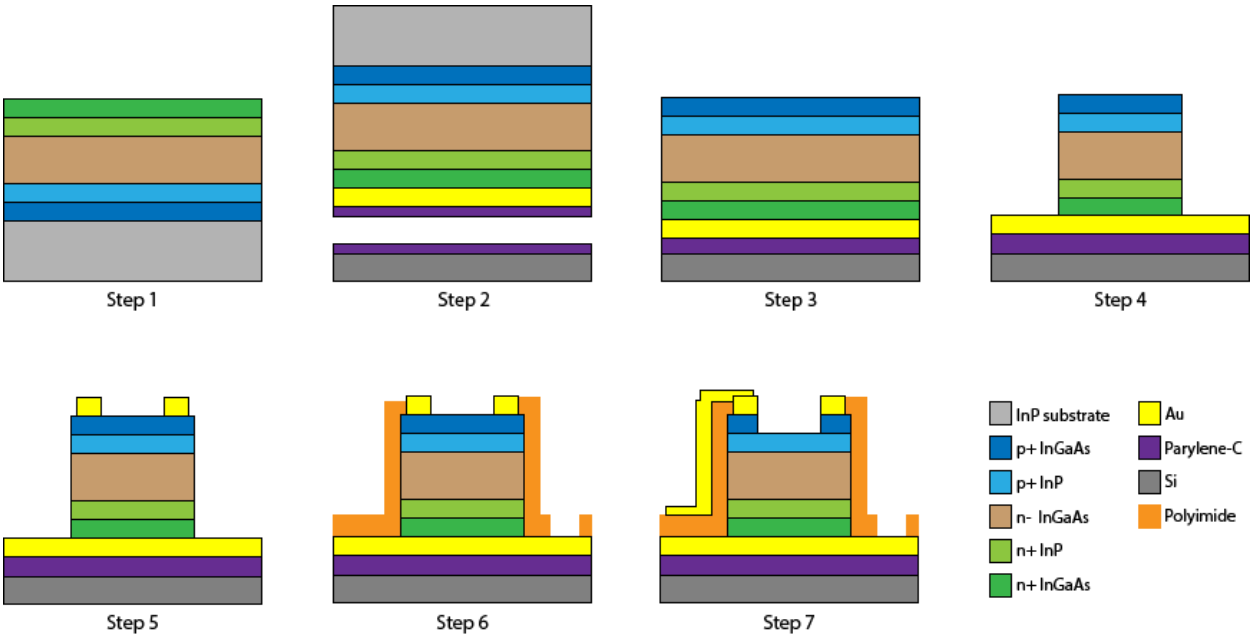

Figure 7.1 : Fabrication process for the InGaAs PV cell

7.3 Devices and experimental setup

To explore the principles of high efficiency NFTPV energy conversion from planar surfaces and PV cells operating at room temperature, we developed microdevices capable of being heated to temperatures as high as 1270 K, along with matching thin film PV cells (Fig. 7.2 (a)) with a spectral response that is capable of absorbing above-band gap (ABG) thermal radiation while minimizing absorption of sub-band gap (SBG) photons[19,21,22]. To elaborate, the emitter features a monolithic, doped silicon cantilever with a circular mesa (see Fig. 7.2 (b) for details) connected to a substrate at room temperature by two stiff beams (Figs. 7.2 (a) & (d)). The two beams form an electrical resistor (R_{emitter}) that can be employed to elevate the temperature of the mesa (T_{emitter}) by distributed Joule heating ($j^2\rho$), where j and ρ are the local current density and resistivity, respectively. Also, a 10 nm-thick layer of AlN (Fig. 7.2 (b)) was conformally deposited over the emitter to form both an electrically insulating layer and a diffusion barrier to protect the emitter surface from degrading at high temperatures[32].

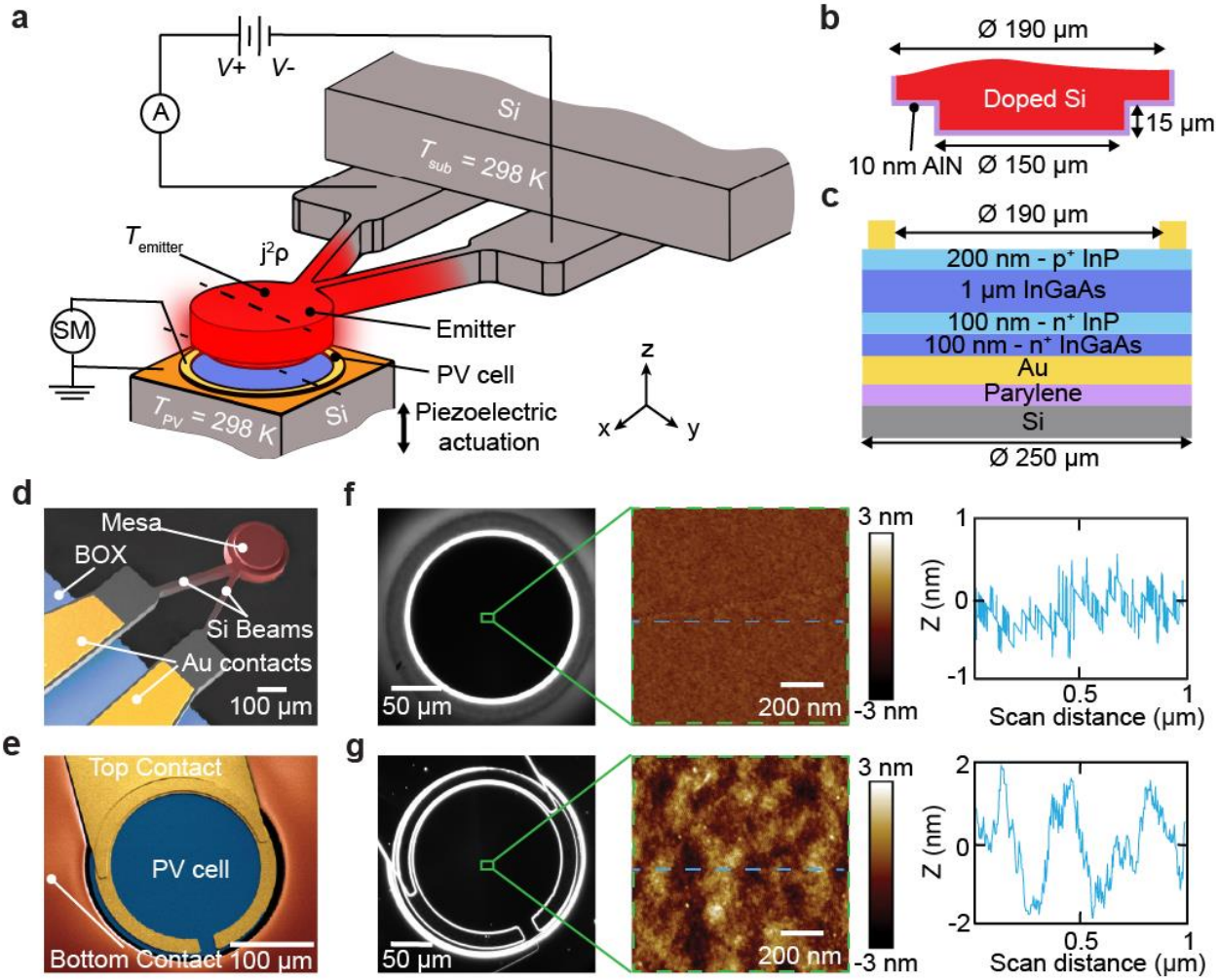

Figure 7.2 : Devices and experimental setup

(a) Schematic depiction of the experimental setup employed for near-field thermophotovoltaic measurements. The custom-fabricated Si emitter features a suspended mesa (see panel d) that is Joule heated (heat dissipation quantified with an ammeter 'A') up to1270 K by applying a bipolar voltage (*V*+, *V*-) to the two beams. The epitaxially-grown InGaAs photovoltaic (PV) cell is moved towards the emitter via a piezoelectric actuator to systematically control the gap size while the electrical power generated is quantified with a source meter (SM). The emitter substrate and the PV cell are at a temperature of ~298 K. (b), (c) Cross-sectional profiles of the emitter and the PV cell at the sections along the black dashed lines in Fig. 7.2 (a). (d) False-colored scanning electron micrograph (SEM) of the emitter with mesa, showing the buried oxide layer (BOX) and the gold contacts on the Si beams. The Si beams featuring a temperature gradient are depicted in red e, False-colored SEM of the PV cell showing the central active layer of the PV cell (blue) as well as top (yellow) and bottom (orange) Au contacts. (f), (g) Dark-field microscope (left panels), atomic-force microscopy (AFM) images (middle panels) and surface roughness profiles (corresponding to the blue dashed lines in the AFM images) of the mesa (f) and the PV cell (g) are shown in the right panels. The peak-peak roughness of the mesa is ~1 nm, while that of the PV cell's active surface is ~4 nm.

The PV cell has a circular active area of diameter 190 µm (Fig. 7.2 (c)) to closely match the dimensions of the emitter, and features a thin film $In_{0.53}Ga_{0.47}As$ (InGaAs) layer epitaxially grown by solid source molecular beam epitaxy on an InP wafer, and transferred to a silicon substrate. The top and bottom Au layers serve as electrical contacts (Fig. 7.2 (e)). The bottom

contact also acts as a back surface reflector (BSR) for recycling SBG photons back to the emitter[4,5]. The emitter and the PV cell, as verified by dark-field optical microscopy[33] and AFM scans of the mesa (Fig. 7.2 (f)) and active area (Fig. 7.2 (g)), are extremely flat and free of particles and other contamination that would interfere with the NF operation of the TPV system.

To parallelize the emitter and the PV cell, we employed a nanopositioning platform[12,28,33,34] in a high vacuum environment (~1 μTorr), and varied the gap size between the emitter and the PV cell from micrometers to nanometers even while the emitter was heated to high temperatures (Fig. 7.2 (a)). This was accomplished by applying a bipolar voltage across the two terminals of the emitter and maintaining the voltage of the mesa close to the ground potential, thus reducing electrostatic interactions with the PV cell, and enabling creation of small gap sizes. Further, no additional active thermal management (i.e. refrigeration) was applied to the PV cell, as the heat transfer is primarily localized to the mesa region of the emitter interacting with the PV cell.

7.4 Experimental scheme for probing NFTPV energy conversion

Here we describe the experimental strategy for heating the emitter, controlling the gap between the parallelized devices, and measuring the power output at each gap size. We began our experiments by passing a current of ~70 mA through the two terminals of the emitter (Fig. 7.2 (a)). This results in a power dissipation of P_{Joule} = 411.8 mW within the beams of the emitter and heats the mesa to a temperature, T_{emitter} = 930 K, as determined by a scanning thermal probe-based method.[35] The heated emitter and PV cell were placed at an initial separation of ~7 μm using a coarse-positioning stepper motor that controls the position of the PV cell. The PV cell was then stepped closer to the emitter using a feedback controlled piezoelectric actuator. The data corresponding to this process are shown in Fig. 7.3 (a), where the top panel shows that large steps of ~800 nm are taken initially followed by finer steps of ~2 nm before contact. The electrical

resistance ($R_{emitter}$) of the emitter (third panel, Fig. 7.3 (a)) and the short-circuit current (I_{sc} at V = 0) measured across the PV cell (schematic, fourth panel Fig. 7.3 (a)) at each gap size do not change significantly during the initial steps, but a large variation is seen over the last hundreds of nanometers due to NF enhancement. A sudden jump in the optical signal that monitors deflection of the emitter, which is accompanied by a simultaneous change of $R_{emitter}$ and I_{sc}, at the end of the approach clearly indicates contact between the devices. At this point the PV cell is quickly withdrawn, to separate the devices back to the initial gap of 7 μm.

To measure the electrical power output of the PV cell, its current-voltage (*I-V*) characteristics are measured at each gap size. Typical curves are shown for gaps of 7 μm, 200 nm and 100 nm in Fig. 7.3 (b), where a clear upward shift of the *I-V* curve to larger short circuit currents (I_{sc}) and moderately increased open-circuit voltage (V_{oc}) is seen with decreasing gap size. The increase in I_{sc} from 9.8 μA at 7 μm, to 56 μA at 100 nm can be attributed to the increased above band-gap (ABG) photon flux from evanescent modes coupled at sub-wavelength gaps (see below). The electrical power output at the maximum power point (P_{MPP}, Fig. 7.3 (c)) of the *I-V* curve is $P_{MPP} = FF \times V_{oc} \times I_{sc,}$ where *FF* is the fill factor (at 100 nm, *FF* = 0.73). The variation of P_{MPP} with gap size is plotted in Fig. 7.3 (d) (violet squares, left axis), where the PV cell power output remains around 2 μW for gaps from 7 μm to 600 nm. Below 600 nm, the power output increases substantially to 14.8 μW at the smallest gap of 70 ± 2 nm, indicating an ~8-fold power enhancement in the NF when compared to the far-field. To interpret this NF enhancement, all the surfaces of the emitter that contribute radiative energy fluxes to the PV cell must be considered. The surfaces of the emitter are labeled ‘mesa’ and ‘rec’ (see schematic Fig. 7.3 (d)), where ‘mesa’ refers to the central region ($A_{mesa} = 7.07 \times 10^{-8}$ m^2) and ‘rec’ signifies the recessed ring ($A_{rec} = 4.2 \times 10^{-8}$ m^2) surrounding the mesa. When considering only the contribution from the A_{mesa}, the NF

power enhancement is 11-fold relative to power generation in the far-field, whereas a smaller 8-fold enhancement is observed when contributions from A_{rec} are included in the power transfer as seen in the experimental data of Fig. 7.3 (d). This is because only the mesa enters the NF of the PV cell, while A_{rec} always remains in the far-field. Thus, the actual enhancement can be larger if all surfaces are brought into the NF.

To understand the physical mechanisms behind the enhancement, we developed a model based on the formalism of fluctuational electrodynamics[7]. Specifically, we employed our model to estimate the power output P_{MPP} and the total radiative heat transfer Q_{RHT} as functions of $T_{emitter}$ and gap size for the geometries (including A_{mesa} and A_{rec}) and materials that correspond to those employed in this work. The estimated P_{MPP} is plotted as a purple line in Fig. 7.3 (d), which agrees with the experimentally measured P_{MPP}. Further, the calculated Q_{RHT} is observed to continuously increase from ~72 μW at 7 μm, to ~1 mW at 70 nm.

7.4.1 Detecting contact between the emitter and the PV cell

To detect mechanical contact between the emitter and the PV cell, we employ a scheme similar to the optical scheme used in atomic force microscopes. Specifically, we focus a laser onto the backside of the emitter and collect the reflected laser beam (schematic in panel 2 of Fig. 7.3 (a)) on a segmented photodiode with two independent detectors. Further, a small AC signal V_{AC} is applied to the piezoactuator which modulates the gap size between the emitter and the PV cell at an amplitude of ~2 nm at 4 kHz. The 4 kHz component of the difference signal of the two segments in the photodiode (Opt_{AC}) is continuously measured in a lock-in amplifier (SRS 830). When the PV cell makes physical contact with the emitter, a change in this signal can be noticed indicating contact (see panel 2 of Fig. 7.3 (a)). In addition, sudden changes in the simultaneously measured

$R_{emitter}$ due to rapid cooling through heat conduction to the PV cell enables us to independently detect contact (Fig. 7.3 (a)).

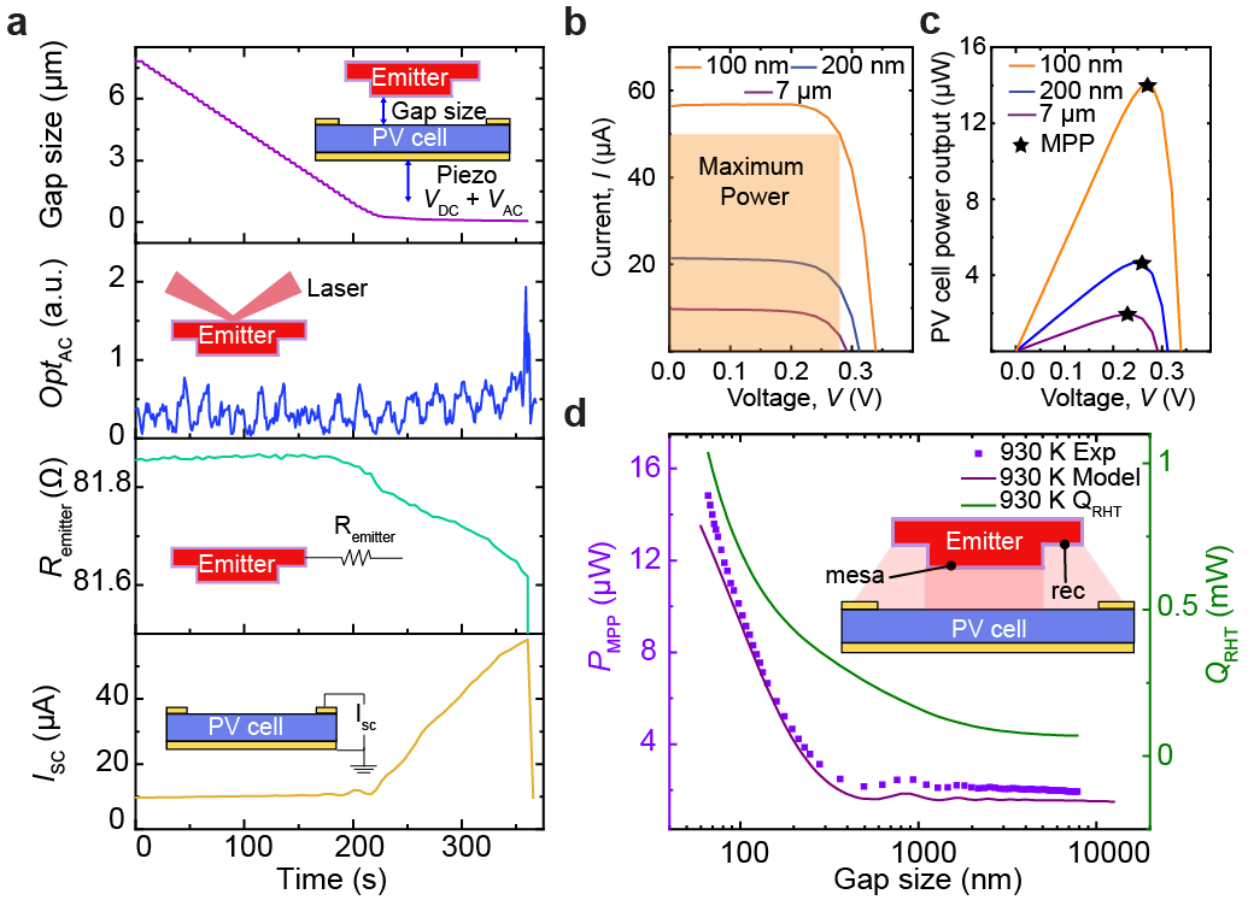

Figure 7.3 : Experimental data with an heated emitter and the PV cell at room temperature
(a) Data obtained as the gap size between the emitter and the photovoltaic (PV) cell is reduced from ~7 μm to contact. The top panel shows the gap size as a function of time. The inset shows how the PV cell mounted on a piezoelectric actuator is displaced (V_{DC} is the DC voltage applied to the feedback-controlled piezo and V_{AC} is a superimposed small AC modulating signal at 4 kHz). The second panel shows the variation of the AC optical signal (Opt_{AC}), while the third and fourth panels show the changes in the resistance of the emitter ($R_{emitter}$) and short-circuit current (I_{sc}) in the PV cell. The simultaneous jumps in Opt_{AC}, $R_{emitter}$ and I_{sc} indicate contact. (b) Data from current-voltage *(I-V)* characterization performed for gaps of 7 μm, 200 nm and 100 nm. The orange shaded region represents the maximum power extractable from the PV cell for a gap size of 100 nm. (c) The power output of the PV cell as a function of the voltage showing the maximum power points (MPP). (d) The power output at the maximum power point (P_{MPP}) at different gaps. Violet squares indicate the measured data, the purple solid line represents the theoretically estimated P_{MPP} and the green line shows the total radiative heat transfer (Q_{RHT}) between the emitter and the PV cell as a function of gap size. The inset (not to scale) indicates that both the 'mesa' (near-field contribution from the circular region in the center) and 'rec' (far-field contribution from the 15 μm-recessed circular ring) surfaces contribute to the total P_{MPP} and Q_{RHT}.

7.4.2 Modeling approach for calculating NF radiative energy transfer

To model the power output and calculate the total radiative energy transfer between the emitter and the PV cell, we first approximate our devices as infinitely extended in the lateral *x*, *y* dimensions and multi-layered along the *z* direction (see Fig. 7.2 (a) for directions). The thermal emission from each layer is generated by fluctuational currents within that material. The correlations of these fluctuational currents are described by fluctuation-dissipation theorem[36,37] and the resulting energy flux in any layer of the structure is calculated using a numerically-stable scattering matrix formulation[38]. Using this method, we calculate Q_{RHT} from different layers of the emitter to the PV cell. To estimate the P_{MPP}, we first calculate the spectral photon flux from the emitter to the active layer of the PV cell. The photocurrent generated from this photon flux is incorporated in an equation describing the PV cell and the maximum power P_{MPP} is obtained from the corresponding *I-V* characteristics.

7.5 NFTPV performance at temperatures above 1000 K

7.5.1 *I-V*, power output of the NFTPV system

To understand the temperature-dependent performance of the TPV system, we systematically increased $T_{emitter}$ in steps of ~100 K and performed experiments as described above. When the emitter temperature increases, the characteristic wavelength of the radiated spectrum decreases, increasing the fraction of energy in the ABG region, and correspondingly the photocurrent (I_{sc}). As the emitter temperature is raised from 1050 K to 1270 K, in Fig. 7.4 (a) we observe that I_{sc} increases from 30 μA to 150 μA. Importantly, a large shift in I_{sc} is seen as the gap size is reduced from 7 μm to ~100 nm; for example, at the highest temperature of 1270 K, a ~5-fold increase in I_{sc} is measured (purple solid and dashed lines in Fig. 7.4 (a)). We note that the *I-V*

curve at 1050 K and a gap size of 100 nm is similar in shape to that of one obtained at 1270 K in the far-field, highlighting that NFTPVs can achieve similar or higher power outputs at significantly lower temperatures when contrasted to a comparable far-field TPV device. Further, in Fig. 7.4 (b), we plot V_{oc} as a function of I_{sc} for the different temperatures and gap sizes (the direction of the arrows signifies decreasing gap size), which indicates a logarithmic dependence of V_{oc} on I_{sc}, characteristic of PV cells. Thus, V_{oc}, I_{sc} and P_{MPP} increase with decreasing gap size and increasing temperature. Further, the calculated V_{oc} and I_{sc} (solid lines in Fig. 7.4 (b)) agree with the experimental data over the broad range of temperatures and gap sizes explored.

The measured P_{MPP} as a function of gap size is plotted in Fig. 7.4 (c) at different temperatures between 810 and 1270 K. At all temperatures, P_{MPP} increases when the gap size is decreased sufficiently; for example, at 1050 K the power output increased from ~7 μW at 7 μm, to 41 μW at a 90 nm gap, a six-fold increase due to NF enhancement. The measured (various symbols) P_{MPP} agree well with that estimated from our model (color bands corresponding to $T_{emitter} \pm \Delta T$, where ΔT = 27 K when $T_{emitter}$ = 1270 K and ΔT = 10 K for other temperatures, as 10 K is the upper bound to uncertainty in that temperature range). Non-monotonic changes in the experimental power outputs are seen for gap sizes between 500 nm and 7 μm at all temperatures due to interference effects, highlighting the capability of our platform to resolve such effects in agreement with the model.

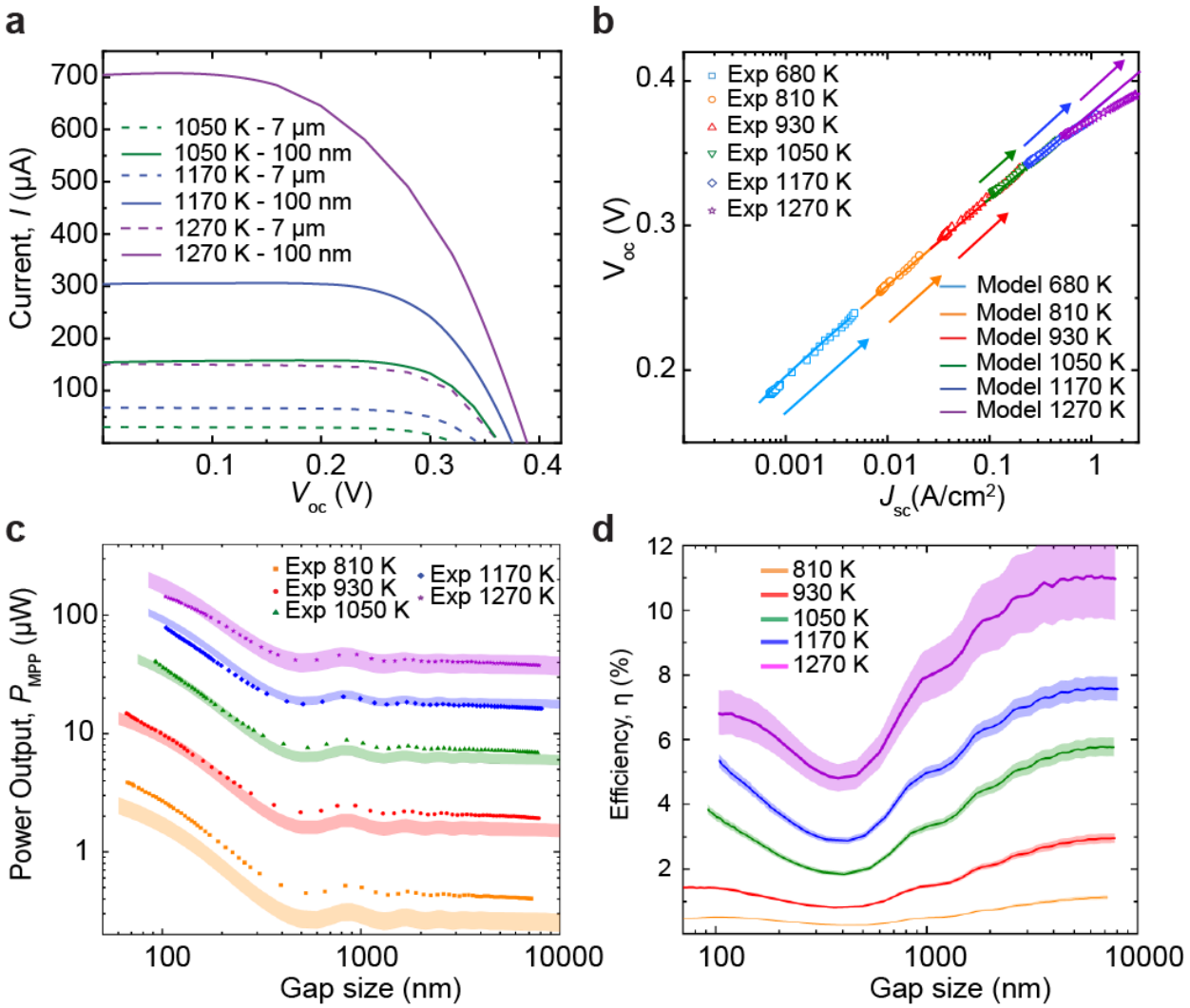

Figure 7.4 : Performance of the TPV system as a function of temperature and gap size
(a) Current-voltage *(I-V)* curves obtained at three emitter temperatures and two gap sizes, indicating an upward shift with increasing temperature and reduced gap size. Dashed lines and solid lines correspond to 7 μm and 100 nm gap sizes respectively. (b) V_{oc} (open-circuit voltage) as a function of J_{sc} (defined as short-circuit current (I_{sc}) per unit area of the PV cell) obtained from experimental data (various symbols) and calculations (solid lines) at all temperatures. The arrow direction indicates decreasing gap size. At high temperatures there is some overlap in the data sets. (c) The experimentally measured power output (P_{MPP}) at different temperatures as a function of gap size, indicating power enhancements as the gap size is reduced from 7 μm to 100 nm. The shaded regions indicate the theoretical power output (P_{MPP}) based on our model in a temperature range of $T_{emitter} \pm \Delta T$, ΔT = 27 K for $T_{emitter}$ = 1270 K and 10 K otherwise. (d) The efficiency (η) defined as ratio of P_{MPP} to the calculated total radiative heat transfer (Q_{RHT}) at different temperatures of the emitter as a function of gap size. The solid lines correspond to the efficiencies obtained by calculating Q_{RHT} at $T_{emitter}$, while the shaded regions correspond to the efficiencies due to the uncertainty (ΔT) in the measurement of $T_{emitter}$

The NFTPV energy conversion efficiency (η), defined as the ratio of the measured power output P_{MPP} to the calculated total radiative heat transfer Q_{RHT} to the PV cell ($\eta = (\frac{P_{MPP}}{Q_{RHT}}) \times 100$) is plotted in Fig. 7.4 (d) as a function of gap size and temperature (color bands correspond to efficiencies obtained by calculating Q_{RHT} in a temperature interval of $T_{emitter} \pm \Delta T$, where ΔT = 27 K for $T_{emitter}$ = 1270 K and 10 K for other temperatures, as described above). Here, η increases with temperature, independent of gap size. For example, at 100 nm gaps, an increase in efficiency from 0.5% to 7.3 % is observed as the emitter is heated from 810 K to 1270 K. We note that at temperatures >930 K, the efficiency is greater than the highest efficiencies reported in the literature[28–30]. At a given temperature, the efficiency initially decreases with gap size for the smallest gaps, then starts to increase, as predicted by our model (see below).

7.5.2 Spectral characteristics

To understand the detailed spectral characteristics of NF energy transfer, we calculate the spectral energy transfer (Fig. 7.5 (a)) from the emitter at 1270 K to the PV cell at 300 K for a range of gap sizes. For example, at a gap size of 100 nm, significant enhancement over the blackbody limit (black dashed line) can be seen in the ABG energy transfer, while considerable suppression of SBG energy transfer below the blackbody limit is observed, due to the incorporation of a thin-film back reflector. The residual SBG energy transfer has contributions from surface phonon-polaritons in the low frequency range (~14% of Q_{RHT} in 0.0124 - 0.073 eV range) while the rest of the absorption primarily occurs in the Au BSR (~55% of Q_{RHT} in 0.074 - 0.74 eV range). The power generating component of the ABG spectrum absorbed in the active layer (P_{AL}) is shaded in

orange (~26% of Q_{RHT}). Approximately 32% of P_{AL} is extracted as electrical power, while the rest is lost due to thermalization, non-radiative recombination and ohmic losses.

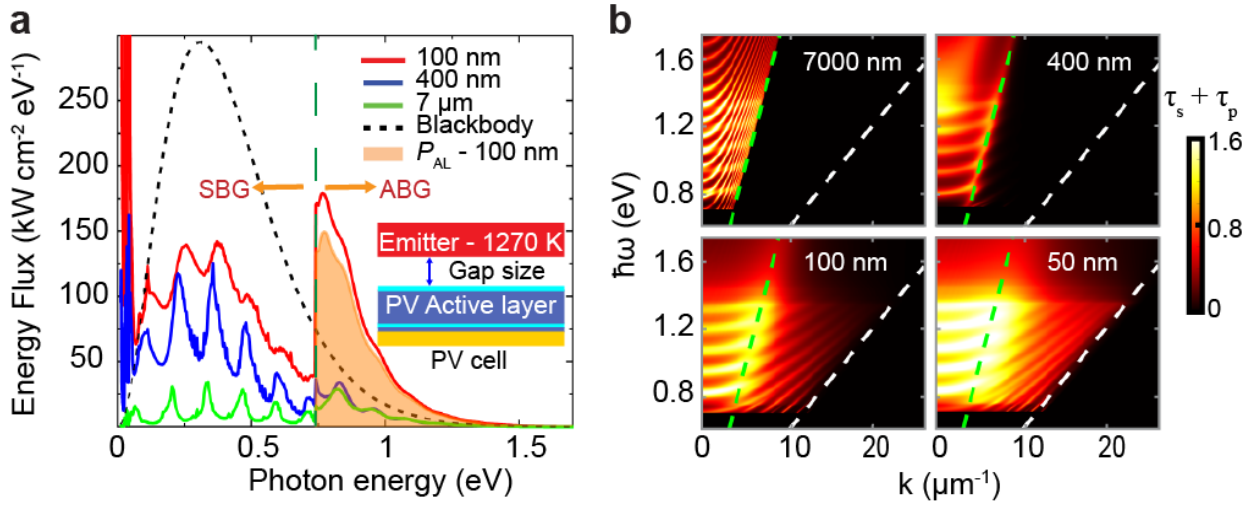

Figure 7.5 : Physical mechanism of NF enhancement
(a) The spectral energy transfer from a hot thermal emitter at 1270 K to a photovoltaic (PV) cell at 300 K is plotted as a function of photon energy for three gap sizes. The black dashed line represents the blackbody radiative limit between two semi-infinite plates at 1270 K and 300 K. Enhancement in above-band gap (ABG) transfer is seen as the gap size is reduced down to 100 nm. The orange shaded region represents the radiative energy transfer (P_{AL}) from the emitter to the InGaAs active layer, which drives the generation of charge carriers. Green dashed line represents the band gap of the PV cell while SBG represents the sub-band gap region. Note that the energy flux for the 100 nm gap size at low energies (<0.1 eV) extend beyond the y-axis range. (b) The total transmission function of different modes from the emitter to the active layer, as a function of photon energy and parallel wavevector at four gap sizes. The green dashed line represents the light line in vacuum, while the white line represents the dispersion relation in the top InP layer.

Next, the efficiency trend as a function of gap size can be understood by comparing the spectral energy transfer at three gap sizes of 7 μm (far-field), 400 nm and 100 nm. In the far-field (green line), a large suppression of SBG energy transfer is observed that is related to the thin-film BSR[4,5]. Even when we reduce the gap size, the SBG energy transfer remains below the blackbody limit. Moreover, as the gap size is reduced from 7 μm to 400 nm, SBG energy transfer is observed to increase more rapidly than ABG energy transfer. These differences in the rates of change of SBG and ABG energy transfer cause an initial drop in the efficiency in Fig. 7.4 (d) at intermediate gaps around 500 nm. As the gap size is further reduced to 100 nm, ABG energy transfer exceeds

the blackbody limit, whereas a comparatively smaller rise in SBG energy transfer results in the efficiency increase at smaller gaps.

To further elucidate the contribution of different modes to the observed NF enhancement in P_{AL}, we evaluate the transmission coefficients of *s* and *p*-polarization modes ($\tau_s+\tau_p$) as a function of photon energy ($\hbar\omega$ > 0.74 eV) and parallel wavevector (*k*) (Fig. 7.5 (b)). In the far-field at a gap of 7 μm, only propagating modes above the light line in vacuum contribute to ABG energy transfer, whereas in the NF at 100 nm, evanescent modes between the light line in vacuum (green dashed lines in Fig. 7.5 (b)) and in the top substrate of the PV cell (white dashed lines) also contribute, leading to a broadband enhancement in ABG energy transfer.

7.5.3 Near-field improvement

The performance of a PV cell under illumination is generally determined by the short-circuit current (I_{sc}), open-circuit voltage (V_{oc}) and the fill factor (*FF*). While I_{sc} depends on the incident photon flux, the internal quantum efficiency and series resistance (weak dependency due to low series resistance) of the PV cell, V_{oc} and *FF* depend on various factors such as the non-radiative recombination, series and the shunt resistances of the PV cell. In our experiments, I_{sc} (Fig. 7.6 (a)) is observed to increase with more-than-linear dependency on temperature at both gap sizes of 100 nm (NF, green circles) and 7 μm (far-field, violet squares). Similarly, the variation of V_{oc} with temperature is plotted in Fig. 7.6 (b) along with the theoretical calculations. The experimental data agree quite well with the theoretical calculations. Specifically, the agreement in V_{oc} with our model which does not include temperature dependency of the PV cell, indicates that the cell remained close to room temperature during our measurements.

Finally, the power density and efficiency in the far-field (7 μm) and NF (100 nm), respectively, as functions of temperature are shown in Fig. 7.6 (c) and (d). A clear enhancement

in power density is observed at all temperatures (~7× at 810 K and ~4× at 1270 K). The estimated efficiency from our calculations of P_{MPP} and Q_{RHT} is $\eta = (\frac{P_{MPP}}{Q_{RHT}}) \times 100$ ~8.3% (green dashed line), which is slightly higher than the efficiency estimated from the experimental power output (~7.3 %). This ~18% disagreement at the highest temperature with the theoretically predicted value may be attributed to uncertainty in temperature measurement of the emitter, modelling parameters, such as the dielectric properties of the emitter as a function of temperature and the PV cell's series and shunt resistances or a small increase in the temperature of the PV cell. The efficiencies in the NF are slightly smaller than in the far-field, owing to absorption in the Au film reflector, which can be mitigated by engineering the devices to further suppress SBG energy transfer. This can be achieved by employing an air-gap PV cell which has recently been shown to support very efficient SBG suppression[4]. Such devices must be engineered to address a host of technical requirements (smooth surfaces, planarity, temperature compatibility) before they can be adapted for NFTPV studies.

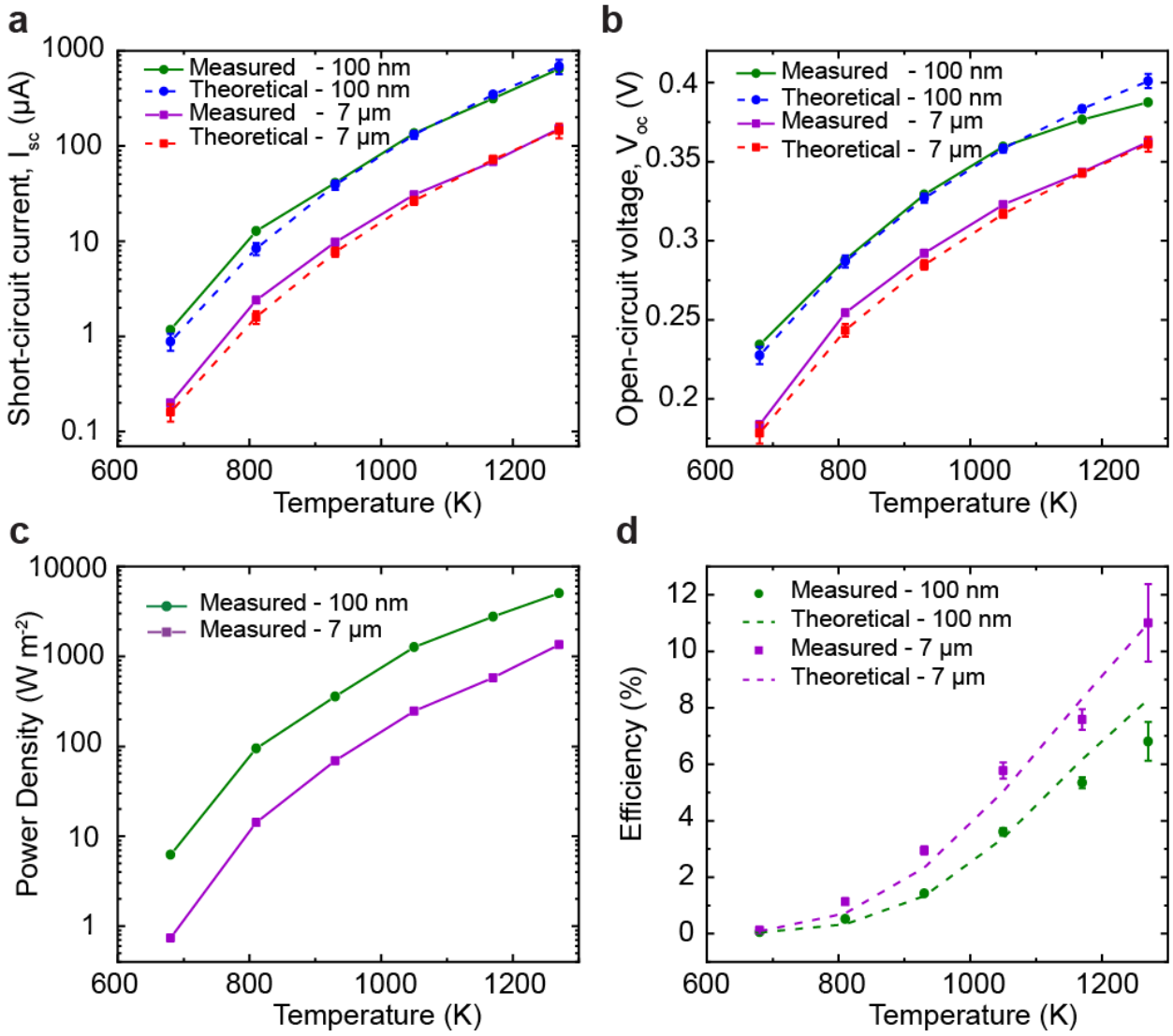

Figure 7.6 : Performance of NFTPV system

(a),(b) Measured and calculated short-circuit current (I_{sc}) and open-circuit voltage (V_{oc}) as a function of temperature. Green circles and violet squares represent the experimental data points, while blue circles and red squares represent the calculated data points with the corresponding uncertainties, at gap sizes of 100 nm and 7 μm respectively. Solid and dashed lines added as a guide to the eye. (c) The measured power density (P_{MPP} per unit area of the PV cell) is plotted as a function of temperature at two gap sizes, one in the far-field (violet squares) and other in the near-field (green circles, solid lines plotted as visual guide). (d) Efficiency of NFTPV system at different temperatures for two gap sizes, defined as the ratio of the measured power output (P_{MPP}) and theoretical radiative heat transfer (Q_{RHT}), calculated at $T_{emitter}$ with an uncertainty of $\pm \Delta T$, where ΔT = 27 K for $T_{emitter}$ = 1270 K and 10 K otherwise. The dashed lines represent theoretical estimates of the efficiency based on our model.

7.6 Conclusion

We demonstrated efficient (~7.3 %, excluding the heat losses through conduction and radiation from surfaces not facing the photovoltaic cell) thermophotovoltaic power generation in

the NF (<100 nm gaps) at an unprecedented power density of ~5 kW/m^2 when the emitter is heated to 1270 K and the PV cell is at room temperature. This power density is more than an order of magnitude higher than for the best-reported TPV systems in the NF, while also operating at 6-times higher efficiency[29]. By employing a heavily-doped silicon, we could successfully operate the emitter in the temperature range of 300 – 1270 K by Joule heating. Further, the emitters presented here, capable of operation at high temperatures (up to 1270 K), present a platform for future work aiming to experimentally explore novel strategies to improve NFTPV performance by engineering thermal emitters[39–43] or PV cells[4,44]. These advances are expected to help establish the principles necessary for the exploitation of a range of NF based TPV nanotechnologies. Future studies on the long-term stability of the emitters at high temperatures with various protective coatings, under a range of pressures could enable realization of practical devices.

Chapter 7

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Chapter 8

Air-bridge Si thermophovotoltaic cell with high photon utilization

The work presented in this chapter is done in a collaborative manner with Tobias Burger from Professor Andrej Lenert's group in Chemistry department at the University of Michigan. I mainly contributed to the Si thermophotovoltaic cell development, fabrication and characterization.

Thermophotovoltaic (TPV) cells convert thermal radiation energy into electricity. Unlike solar cells, TPV cells can be placed in close proximity to the heat source. This allows emitted or reflected photons from the cell to be re-absorbed at the heat source, and have a chance to be emitted back with higher energy. Therefore, minimizing the parasitic absorption of the out-of-band (OOB) photons can drastically improve the photon utilization and efficiency of TPV cells. As the OOB reflectance approaches unity, spectral efficiency of the TPV system becomes less sensitive to the bandgap of the cell and temperature of the source. This suggests that low-cost semiconductors like Si which was considered impractical due to relatively high bandgap, can potentially be exploited in TPV applications. In this chapter, we introduce preliminary results regarding air-bridge Si TPV cell fabrication. With lateral *p-n* junction structure formed on the front surface of the 300 μm thick Si wafer, the TPV cell with air-bridge reflector shows extremely low series resistance of ~50 $m\Omega \cdot cm^2$ and OOB reflectance of ~97%. We also demonstrate a dummy air bridge structure of 6 cm × 6 cm area bare Si bonded onto 4" Si wafer, showing the scalability of such structure. With improved OOB reflectance, low series resistance and potential scalability, we expect the use of low-cost Si can expedite the widespread use of TPV system in diverse energy solutions.

8.1 Motivation

The work described in this subsection motivated the development of devices described later in this chapter. While Dejiu Fan and Tobias burger mainly lead the project, I participated in material growths and development of the bonding process for device fabrication. Detailed information can be found in the our publication.[1]

8.1.1 Photon utilization in TPVs

OOB thermal radiation in a TPV can be recycled back to the closely positioned emitter using spectral control, enabling recovery of the unconverted energy[2]. Up to date, selective reflectors including metallic back-surface reflectors[3–5], Bragg/plasma filters[6], and photonic crystals[7], have yet to exceed 95% OOB reflectance. At this level, the largest losses relative to theoretical limits are due to spectral inefficiencies. 5% OOB reflectance loss, although seemingly small, lowers TPV efficiency by ~10% absolute[8] due to the importance of low-energy photons. We demonstrate an alternative approach where the dielectric spacer within the thin-film cell is replaced with air.[1] The air-bridge InGaAs TPV cell absorbs most of the IB radiation to generate electricity while serving as a nearly perfect mirror with ~99% OOB reflectance.

The benefits of an air-bridge architecture are apparent from a theoretical comparison of energy flows and losses in a TPV utilizing a conventional thin-film and an air-bridge cell. In Fig. 8.1(a), a hot thermal source radiates photons with a broad, blackbody spectrum. Photons with energy (E) greater than the TPV semiconductor bandgap (E_g) are absorbed and generate current, while photons with $E < E_g$ travel through the TPV, are reflected by the BSR, and re-absorbed by the emitter.

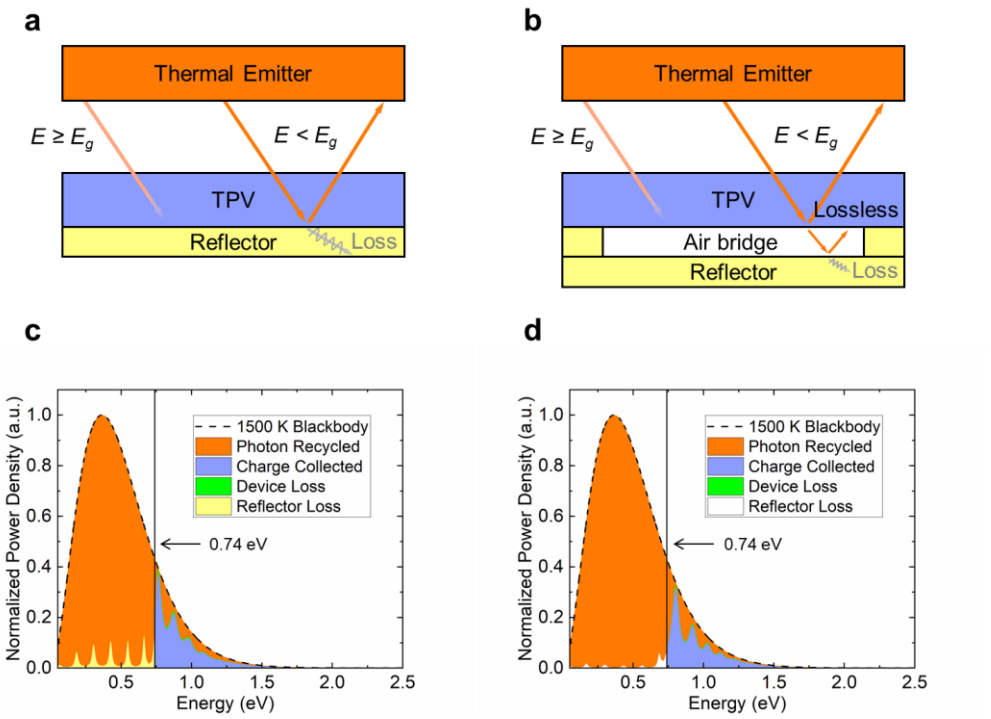

Figure 8.1 : Photon utilization in air-bridge thermophotovoltaics (TPVs).
Conceptual schematics of energy flow in (a) a conventional thin-film TPV with Au versus (b) a thin-film TPV with air-bridge reflector. (c) Power distribution of a conventional thin-film InGaAs cell (E_g = 0.74 eV) with a Au BSR operated with a 1500 K blackbody source (structure given in Extended Data Fig. 1). The dashed line shows the normalized power density of the blackbody, and the cell absorption spectrum is calculated using transfer matrix methods[38]. (d) Power distribution of the air-bridge TPV shown in (b) operated using a 1500 K blackbody emitter.

Conventional reflectors such as Au introduce a loss of ~5% at the semiconductor/Au interface. In contrast, when an air cavity is integrated within the cell (Fig. 8.1 (b)), photons with $E < E_g$ experience lossless Fresnel reflection at the TPV/air interface. Photons that transmit through this interface are then reflected by the Au with < 2% reflectance loss at the air/Au interface. When integrated over the emitter spectrum, OOB absorption by the conventional thin-film cell is 4.7%, representing the primary source of loss (Fig. 8.1 (c)). Other loss pathways include carrier collection (~2.5%). The absorption oscillations are Fabry-Perot modes formed in the cavity between the reflector and the TPV. In comparison, the air-bridge cell loses only 1.1% of power to OOB absorption (Fig. 8.1 (d)). Both cells have a similar energy transfer efficiency in the in-band region (61.1% for conventional vs. 61.8% for air-bridge), whereas the air-bridge structure effectively reduces the OOB losses by more than 4 times compared to the conventional cell.

8.1.2 Spectral properties of the air-bridge InGaAs TPV

The spectral properties of the Au reflector and air-bridge cells were characterized using Fourier transform infrared (FTIR) spectroscopy (Spectrum GX FTIR microscope, Perkin-Elmer, MA, 02451). The measurements were done in the near-IR spectral region (12000 cm^{-1} to 1800 cm^{-1}) with a 0.3 mm × 0.3 mm aperture using a CaF_2 beam splitter and a liquid nitrogen cooled InSb detector. Figure 8.2 (a) and (b) shows measurement results for Au reflector and air-bridge cells, respectively. As weighted by the 1500 K blackbody emission spectrum, the average OOB power reflectance is 95.3% for the Au reflector cell, and 98.5% for the air-bridge cell. The average IB power absorption is 63.6% and 61.2% for the Au reflector and the air-bridge cells, respectively.

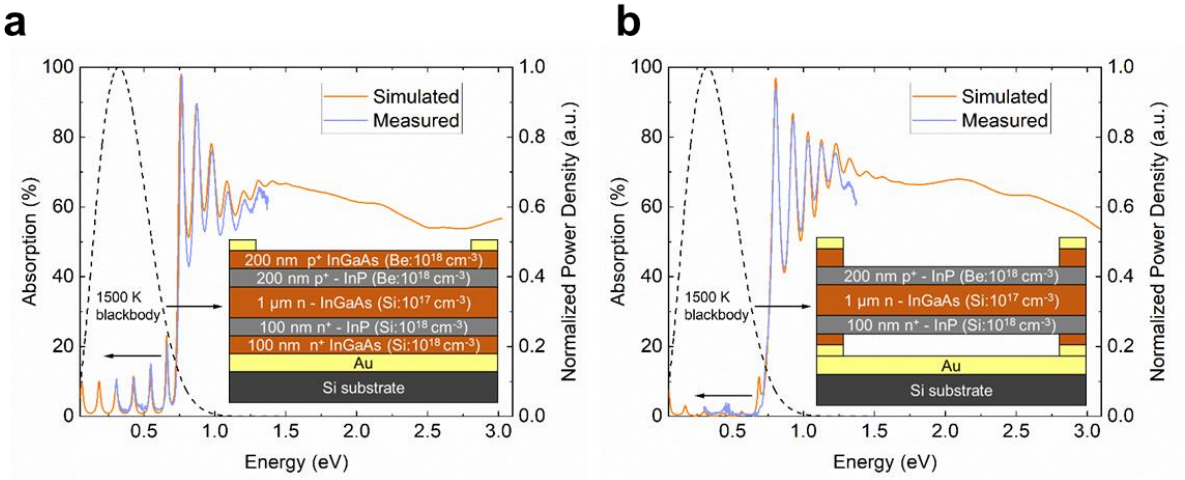

Figure 8.2 : Absorption spectra of Au reflector and air-bridge TPV.
(a) Simulated (orange) and measured (blue) absorption spectra of the Au reflector TPV (structure in inset) using Fourier-transform infrared (FT-IR) spectroscopy. The optical cavity formed by the Au reflector and the TPV thin films leads to increased absorption by the Au reflector by creating several interference peaks. (b) Simulated (orange) and measured (blue) absorption spectra of the air-bridge TPV (structure in inset) using FT-IR. The air-bridge TPV features a lossless reflective semiconductor/air interface, effectively eliminating most parasitic out-of-band absorption.

The spectral enhancements of the air-bridge architecture are accurately described by the spectral efficiency, *SE*, which captures the combined effects of the enhancement of IB and suppression of OOB radiative transport [9]. $SE = \frac{E_g \cdot \int_{E_g}^{\infty} \varepsilon_{eff}(E) \cdot b(E,T_h)\, dE}{\int_0^{\infty} \varepsilon_{eff}(E) \cdot E \cdot b(E,T_h)\, dE}$ where $b(E,T_h)$ is the spectral photon flux of the emitter, and $\varepsilon_{eff}(E) = \frac{\varepsilon_e \varepsilon_c}{\varepsilon_e + \varepsilon_c - \varepsilon_e \varepsilon_c}$ is the effective emissivity, where

ε_e is the emissivity of the emitter, and ε_c is the emissivity/absorptivity of the cell. *SE* captures the dependence of the performance metric on the spectral properties of both the emitter and the cell and corrects for multiple reflections across the emitter/cell cavity. We also define average in-band absorption as $A_{in} = \frac{\int_{E_g}^{\infty} \varepsilon_c(E) \cdot E \cdot b(E,T_h)\, dE}{\int_{E_g}^{\infty} E \cdot b(E,T_h)\, dE}$, and average out-of-band reflectance as $R_{out} = \frac{\int_0^{E_g} (1-\varepsilon_c(E)) \cdot E \cdot b(E,T_h)\, dE}{\int_0^{E_g} E \cdot b(E,T_h)\, dE}$. We find *SE* = 58.1% and 72.9% for the Au reflector and the air-bridge TPV cells, respectively (Fig. 8.3, denoted by stars). Within the common range of source temperatures, OOB loss dominates with increasing bandgap. **However, when R_{out} > 0.99 (orange region), this dependence vanishes, suggesting that the cell design becomes insensitive to E_g and emitter temperature. Thus, the nearly perfect reflectance of the air-bridge design may allow low cost materials like Si to be used as TPV cells while maintaining a high *SE* at relatively low emitter temperatures (~ 1500 K).**

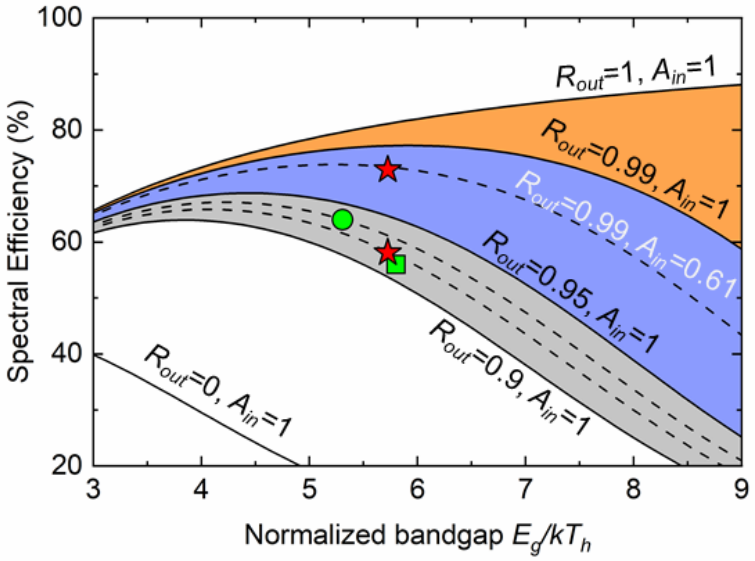

Figure 8.3 : Spectral efficiency.
Measured spectral efficiency of the Au reflector and air-bridge TPVs (stars). Also shown are previous results (circle[39] and square[4]). The simulated spectral efficiencies are calculated for with various OOB reflectance (R_{out}) and IB absorptions (A_{in}) shown by lines.

8.1.3 Power conversion efficiency

The power conversion efficiency (*PCE*) is defined by:

$$PCE = \frac{P_{electrical}}{P_{incident} - P_{reflected}} \tag{8.1}$$

where $P_{electrical}$ is the electrical power generated, $P_{incident}$ is the incident power, and $P_{reflected}$ is the power reflected by the cell.[4,5] Here, $P_{electrical} = V_{oc} \cdot I_{sc} \cdot FF$, where V_{oc} is the open-circuit voltage, I_{sc} is short-circuit current, and FF is the fill factor. The electrical power generated under illumination can be obtained directly from the cell current-voltage (*I-V*) characteristics while the incident and reflected power can be calculated from the spectral emissivity of the cell and emitter.

The *PCE* of each cell under various illumination conditions is shown in Fig. 8.4. The peak *PCE* of the air-bridge cell is 8% greater than a comparable cell fabricated on the Au BSR at a similar photocurrent. Given that these two cells have similar in-band absorption (about 60%), this improvement is primarily (about 6.5%) attributed to the improved OOB reflectance.

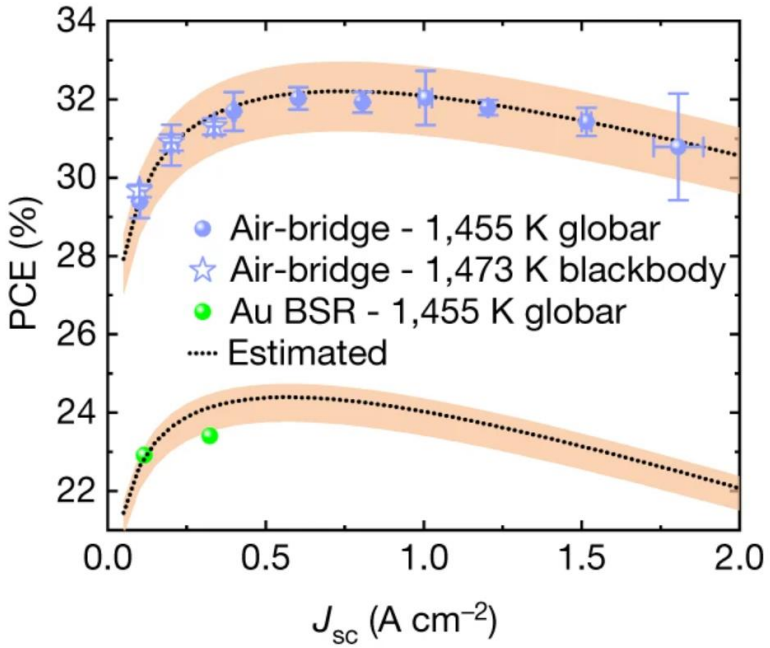

Figure 8.4 : *PCE* of the Au BSR and the air-bridge cell versus short-circuit current density (J_{sc})
Au BSR cells were measured under 1,455-K SiC globar illumination and air-bridge cells were measured under 1,455K globar and 1,473-K true blackbody illumination. Also shown are the simulated *PCE*–J_{sc} curves based on the diode equation (dotted lines) and estimates (shaded) that treat the emitter as a collimated or diffused source, setting the upper and lower bounds, respectively.

8.2 Introduction

Conversion of heat to electricity plays an important role in various energy applications including waste heat scavenging[10], distributed generation[11–13], thermal energy storage[14,15] or direct solar energy conversion.[16–20] TPV cells are widely used in such applications by absorbing radiated photons from high temperature sources and generating electricity via the photovoltaic effect. As the emitter and cell can be closely placed, there exists a radiative exchange between the emitter and the cell. Thus, efficiency of the TPV cell can be enhanced by both emissive and absorptive spectral control.[21] Controlling the absorption can be done by use of front surface filter (FSF), back surface reflector (BSR), or both. Such methods can potentially be generally used for broad-band thermal emitters, as they require engineering of the TPV cell, rather than the emitter.

Achieving high OOB reflectance has a huge impact on cell efficiency due to the high spectral density of low-energy photons.[8] While OOB reflectance of diverse selective reflectors including metal BSR[4,5,22], photonic crystals (PhC)[7] and Bragg/plasma filters[6] remain below 95%, we recently demonstrated an $In_{0.53}Ga_{0.47}As$ (InGaAs) on dielectric/metal structure with OOB reflectance of 96%.[8] and an InGaAs air-bridge TPV cell with OOB reflectance of ~99%, which showed ~8% absolute increase in efficiency compared to the same device with conventional Au BSR.[1] Our estimates show that with OOB reflectance of > 99%, spectral efficiency of the TPV system becomes virtually insensitive to the emitter temperature or cell bandgap. With sufficiently high OOB reflectance, TPV cell based on low-cost, higher bandgap semiconductors such as Si can potentially be paired with relatively low temperature emitters (1000-1500K).

Application of Si PV cells in TPV systems has been proposed in the past for several times. Swanson reported[22] a Si TPV cell with 95% OOB reflectance using Ag BSR, and power conversion efficiency of 29% under a 2300 K broadband emitter. Yeng et al. [23] reported a power conversion

efficiency of 6.4% using conventional Si PV cell enhanced with PhC selective filter under 1660K PhC emitter. Most of the other works focus on the thermal management, system arrangement or cost estimate of the overall system with conventional Si solar cells[24–28], rather than the development of the Si cells specified for TPV applications.

In this chapter, we demonstrate a Si TPV cell with an air-bridge BSR. A planar *p-n* junction structure used in conventional Si PV cells is not practical for TPV applications, due to free carrier absorption at the heavily doped emitter layer.[29] Such parasitic loss is negligible for conventional PV, as the peak absorption wavelength stays within the visible wavelength range. (400~900nm). However, this could be detrimental to TPV applications as the emission peak sit within the near-IR (NIR) to mid-IR band, as free carrier absorption is proportional to the fourth power of wavelength.[29] We use a point lateral *p-n* junction structure formed on top of a Si wafer, with heavily doped Si area covered by Au contacts that can reflect the OOB photons. To minimize series resistance loss, different spacings between p+ and n+ contact were tested, achieving R_s ~50 $m\Omega \cdot cm^2$.Combined with air-bridge BSR using cold weld bonding, we obtain ~97% OOB reflectance, which is an unprecedented value with Si. With external quantum efficiency (EQE) normalized to device active area reaching ~70%, we expect the Si TPV can potentially be applied for lower temperature heat-to-electricity conversion, expediting the widespread use of thermophotovoltaic energy conversion.

8.3 Device fabrication

For optimal absorption of in-band photons and minimum free carrier absorption of OOB photons at the base layer, 100-200um thick Si layer is required. A Thicker base layer is not ideal as free carrier absorption increases from background doping, with negligible gain in the in-band absorption. However, as Si is fragile and even flexible at such thicknesses, handling and processing

becomes extremely tricky and wafer yield is severely reduced. As a compromise, a 300um thick wafer with resistivity of 10-100 Ω·cm was chosen for proof-of-concept processing, and a lateral *p*-*n* junction was formed on the top, so that the Si wafer can potentially be thinned from the bottom to its optimum thickness using etching or chemo-mechanical polishing (CMP).

Figure 8.5 shows a schematic diagram the of Si TPV cell fabrication. 500nm thick, masking thermal oxide was grown via wet oxidation under 1000°C. Standard photolithography and deep reactive ion etching (DRIE) used to pattern the masking oxide, followed by solvent cleaning, piranha and RCA cleaning[30] before dopant diffusion. *p*+ pockets were formed using boron diffusion furnace under 1050°C for 2 hours using Techneglas GS139 boron sources. The masking oxide was then etched under 1:1 hydrofluoric acid (HF) and de-ionized water (DI) solution to remove borosilicate glass (BSG) and residual boron formed on top of the masking oxide. A 500 nm second masking oxide was grown via low-pressure chemical vapor deposition (LPCVD) under 900°C for 2.5 hours to minimize the boron drive-in during the oxidation[31], and avoid top Si surface consumption during thermal oxidation[32]. Oxide patterning and photoresist cleaning was done identical to the first masking oxide layer. The *n*+ pockets were formed using phosphorus diffusion furnace under 950°C for 30 min. using $POCl_3$ sources, followed by 5 min. drive-in. The second masking oxide layer was then removed using 10:1 (DI:HF) solution for cleaning of residual phosphorus deposited on the masking oxide during the diffusion. To passivate the surface without dopant migration, 50 nm low-temperature oxide was deposited under 400°C. Contact openings are patterned via photolithography and wet etching, and Ti/Pt/Al/Pt/Au (5/30/1500/30/200 nm) contact layer was deposited via e-beam evaporation and patterned using metal lift-off. For air-gap formation, a Ti/Au (5/500 nm) support grid was deposited on the back of the device and bonded onto Au/Si handle via cold welding.

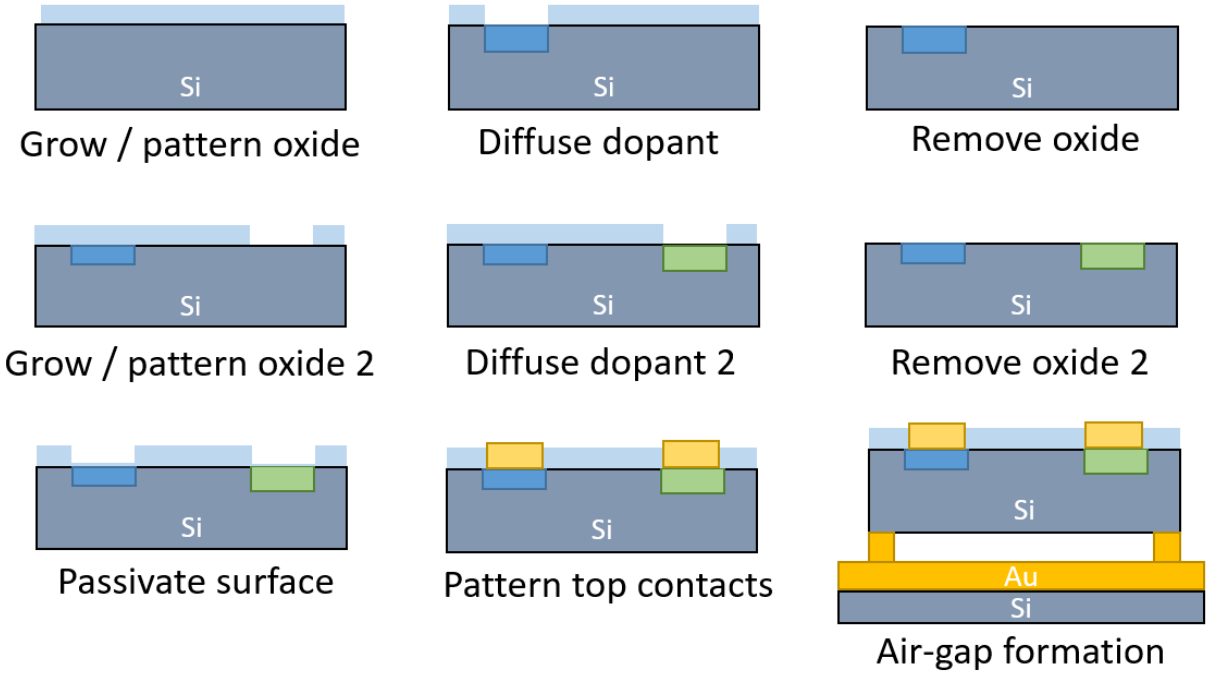

Figure 8.5 : Si TPV fabrication process steps

8.4 Si TPV dark J-V measurements

Due to the high current density that TPV cells usually operate at (e.g. ~1 A/cm^2), resistance loss can be significant. Several different top grid designs with different open area ratio were tested using 5 mm x 5 mm mesa cells. Figure 8.6 (a) shows a lateral view of grid spacing, *d* and width, *w* (µm). For conventional photovoltaic cells, it is optimal to keep the ratio *w*/*d* as small as possible, as area covered with the metal contacts reflect light back cannot absorb any photons. However, for TPV applications, photons reflected back from the top contacts can be considered similar to OOB photons reflected back from the BSR. Therefore, a high *w*/*d* ratio may potentially achieve similar *PCE* with reduced series resistance and improved OOB reflectance, even with relatively low short circuit current (J_{sc}) under illumination. An illustration of the top view of a Si TPV cell is shown in Fig. 8.6 (b). Cathode and anode layers cover the *n*+ and *p*+ Si layers, respectively. To ensure the isolation of the contacts from the *p*- Si bulk, a high doped Si area is designed 4µm wider than the

metal contacts to allow alignment tolerance. There is a potential issue of OOB photon loss at the exposed high-doped Si layer by free carrier absorption, and this can be alleviated by etching the passivation oxide narrower than the high-doped Si layer, and depositing wider top metal contacts.

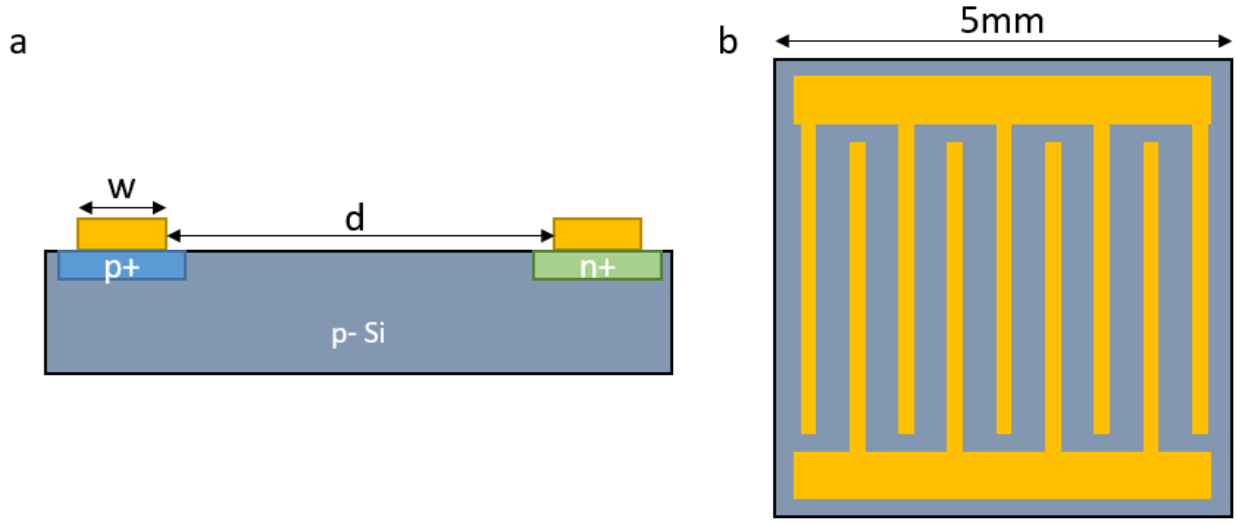

Figure 8.6 : Si TPV structure
A schematic illustration of (a) sideview of p-n junction and grid dimension (b) top view of Si TPV cell with metal contacts

Different grid width and spacing is labeled as $w \times d$ hereafter. An initial design of 7×90 was chosen, as it is similar to a conventional PV cell dimension, while keeping the spacing d smaller than the minority carrier diffusion length of ~100μm. Then, two different grid widths of 20 and 40 μm, and three different grid spacings of 20, 40 and 60 μm were chosen. Each device was measured via four-probes in the dark for evaluation of series resistance. *J-V* characteristics with different grid dimensions are shown in Fig. 8.7 (a). The 7×90 device clearly experiences resistive loss at lower current density of ~100 mA/cm^2 compared to the other devices. Extracted R_s values and geometric active area ratios defined as $d/(d+w)$ are summarized in Table 8.1. Interestingly, 20 μm wide contact devices show smaller R_s compared to 40 μm devices with the same spacing. This suggests that the resistance from the metal contact itself has a minimal effect, as wider devices with the same spacing have fewer grid lines that can conduct current. We chose to use 20 μm width

devices for further analysis of quantum efficiencies and illumination measurements, as they have lower R_s compared to 40 µm devices even with higher open area ratio, which results in higher J_{sc} and less resistive loss. A zoomed-in view of *J-V* characteristics in the region where resistive loss in 20um wide devices and a conventional 7×90 device is shown in Fig. 8.7(b). *J-V* measurements are done before and after the air-gap formation multiple times, and bonding does not affect the *J-V* characteristics.

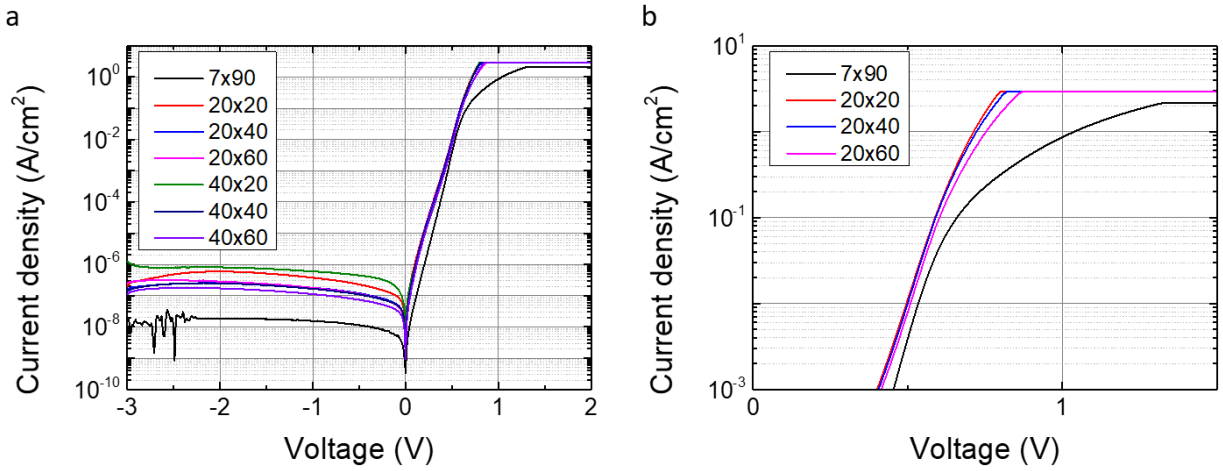

Figure 8.7 Si TPV *J-V* measurement under dark
(a) J-V measurements of all the devices tested for Rs measurement. (b) Zoomed-in view of where Rs loss starts to dominate

Table 8.1 : Summarized open area ratio and *Rs* for different grid dimensions

w \ *d*	20 µm	40 µm	60 µm	90 µm
7 µm	·	·	·	92.8%, 250mΩ·cm²
20 µm	50%, 43 mΩ·cm²	60%, 59 mΩ·cm²	75%, 95 mΩ·cm²	·
40 µm	33%, 54 mΩ·cm²	50%, 64 mΩ·cm²	60%, 97 mΩ·cm²	·

8.5 Surface passivation and EQE measurements

In a lateral p-n junction structure, surface recombination can be detrimental to the device performance as excited charges have higher chances to conduct near the surface compared to vertical *p-n* junction structure, where most of the charges conduct through the bulk base layer. Due to dopant migration at temperatures above ~850°C[31], PECVD or low-temperature CVD oxide deposition are suitable for our device structure. There exists a tradeoff between oxide thickness and parasitic absorption of OOB photons from the oxide layer. 20×60 Si TPV devices with no SiO_2 passivation layer, 20, 50 and 100nm PECVD and 50nm low temperature oxide (LTO) were tested to check the passivation effect. For EQE measurement, TPV cells were placed under monochromatic illumination chopped at 200Hz, coupled into a multimode SubMiniature version A (SMA) to bare fiber optic cable patch. The light illumination power is calibrated using a reference 818-UV/DB Si detector (Newport) from 400 to 900nm, and the output signal from the TPV cell is measured by SR830 lock-in amplifier. Measured EQEs of 20×60 devices with different passivation layers are shown in Fig. 8.8.

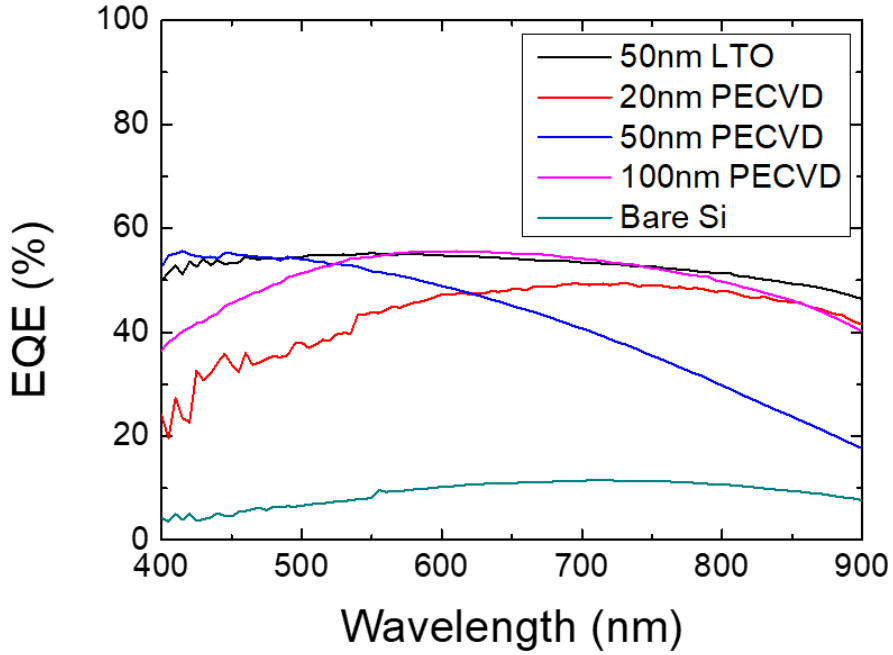

Figure 8.8 : EQE measurements with different passivation oxides

Devices with 20nm PECVD oxide showed sample to sample variation, yet we show the highest measured value for comparison. PECVD oxide showed a varying EQE profile as the thickness changed, and device with 50nm LTO showed the best passivation, showing high EQE over broad wavelength range. Relatively low peak EQE compared to c-Si PV cells (~90% peak EQE[33]) is mainly due to high area fill factor of Au contacts, as well as missing surface texture[34,35] and a proper anti-reflective coating (ARC), [36] while SiO_2 is serving as a single-layer ARC. Measured EQE of 20×20, 20×40 and 20×60 devices with 50nm LTO passivation layer is shown in Fig. 8.9 (a). The effect of active area ratio clearly appears on EQE value, but light absorption at the emitter for TPV applications is not considered. For accurate comparison, measured EQE values need to be normalized to the ratio of actual area that contributes to the light absorption. Here, geometric active area ratios are inaccurate since there exists a 2 μm alignment tolerance in heavily doped Si area, which does not contribute to the photocurrent. Therefore, device active area ratio including the alignment tolerance defined as $(d\text{-}4)/(d+w)$ considering the alignment tolerance is used. Normalized EQE is shown in Fig. 8.9(b), showing well aligned values between different grid dimension devices. All the EQE measurements were done before the air-gap formation, and the effect of bonding on the EQE needs to be verified.

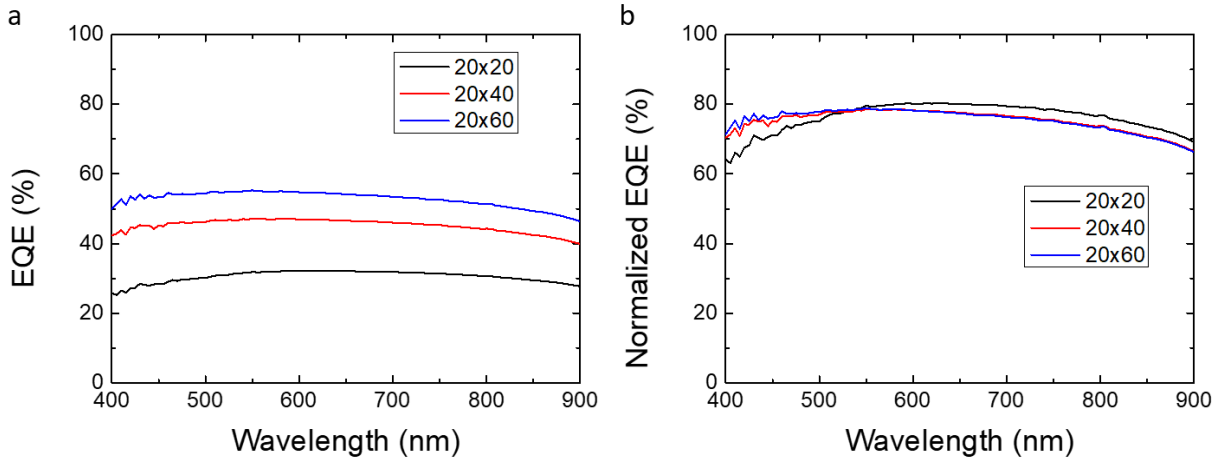

Figure 8.9 : Si TPV EQE measurements on different grid dimensions
Measured EQE of Si TPV devices with 50nm LTO passivation layer and different grid dimensions. (a) Absolute value and (b) Normalized to active area ratio

8.6 OOB reflectance

To validate the feasibility of the air-bridge reflector on Si, absorption spectra of a Si TPV with air-bridge reflector and a conventional Au BSR cell was simulated using the transfer matrix method[37] for comparison. Figure 8.10 (a) and (b) shows calculated absorption spectrum of 50nm SiO_2, 300μm undoped Si layer with 500nm thick air-bridge reflector and Au BSR, respectively. Missing data points below 0.1 eV are due to lack of *n,k* values at wavelengths longer than 24 μm. OOB reflectance is calculated by integrating the reflected energy density over the below-bandgap energy range. The Au BSR and air-bridge reflector cell shows 96.3% and 99.1% OOB reflectance, respectively.

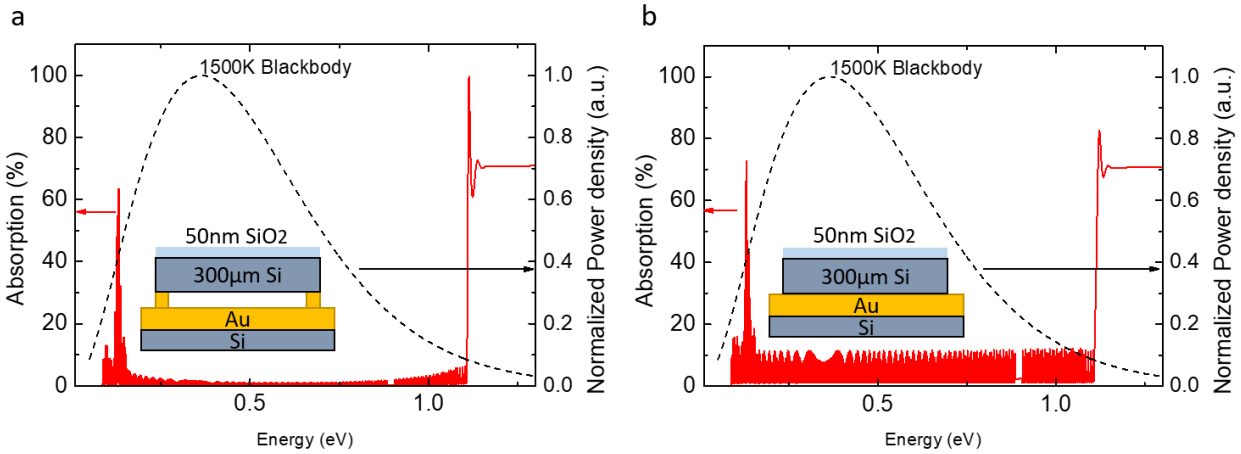

Figure 8.10 : OOB reflectance of Si TPV cell
Simulated (red) absorption spectra of the Si TPV with (a) air-bridge reflector and (b) Au BSR, overlaid with normalized power density of 1500K blackbody radiation spectrum (black dashed line).

Preliminary Fourier-transform infrared (FTIR) spectroscopy results of air-bridge Si TPV structure using 90 μm Si are shown in Fig. 8.11, with estimated OOB reflectance of 96.8% under 2300K blackbody spectrum. Discrepancy between the measurement and simulation is potentially due to free-carrier absorption from the bulk Si and eavily doped Si areas needed for alignment tolerance, as the reflectance drop tends to increase at longer wavelength.[29] Such loss can be potentially alleviated by using metal top contacts wider than the bottom heavily doped layer, while

keeping the oxide etch area narrower than the doped Si area. For more clear comparison, A 300 µm thick Si TPV with air-bridge and Au BSR need to be measured.

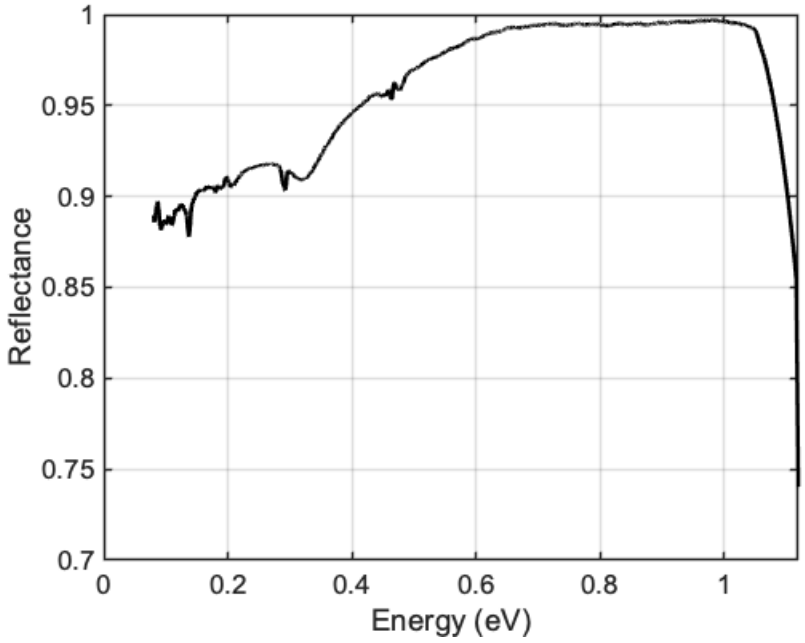

Figure 8.11 : FTIR spectroscopy for air-bridge Si TPV

8.7 Large-area air-bridge structure

Another well-known benefit of Si is better scalability compared to compound semiconductors, as it does not require epitaxial growth for device fabrication. Even if Si is widely used in terrestrial solar energy harvesting where the top cell fabrication steps can be similar to TPV cells, employing high OOB reflectance in large scale is crucial for widespread use of Si in TPV applications. For demonstration, we demonstrate 6cm × 6cm air-bridge structure filled with 7 um wide support grids with 100 µm spacing. Top contact grid patterns were initially formed on top of a 300 µm thick Si wafer using standard photolithography. The wafer was then thinned to 60 µm, using HF-nitric etch from the back surface while front side is covered with photoresist SPR220 (3.0) and mounted on a Teflon® carrier (Fig. 8.12 (a)). After thinning, a 500 nm Au bottom grid for air-gap support was patterned on the back of the wafer, and the wafer is cleaved into a 6 cm ×

6 cm square for easier air-gap formation. The square piece was then bonded onto a 4” Si handle wafer coated with Au using cold-welding, under 150°C and 2MPa, for 3 min. The sample after the bonding is shown in Fig. 8.12 (b). Initial profilometry measurement show a flat surface over the whole sample, while part of the measurement is shown in Fig. 8.12 (c). Further investigation including FTIR measurement and scanning electron microscopy (SEM) of the sample cross section is required to ensure the air-bridge formation.

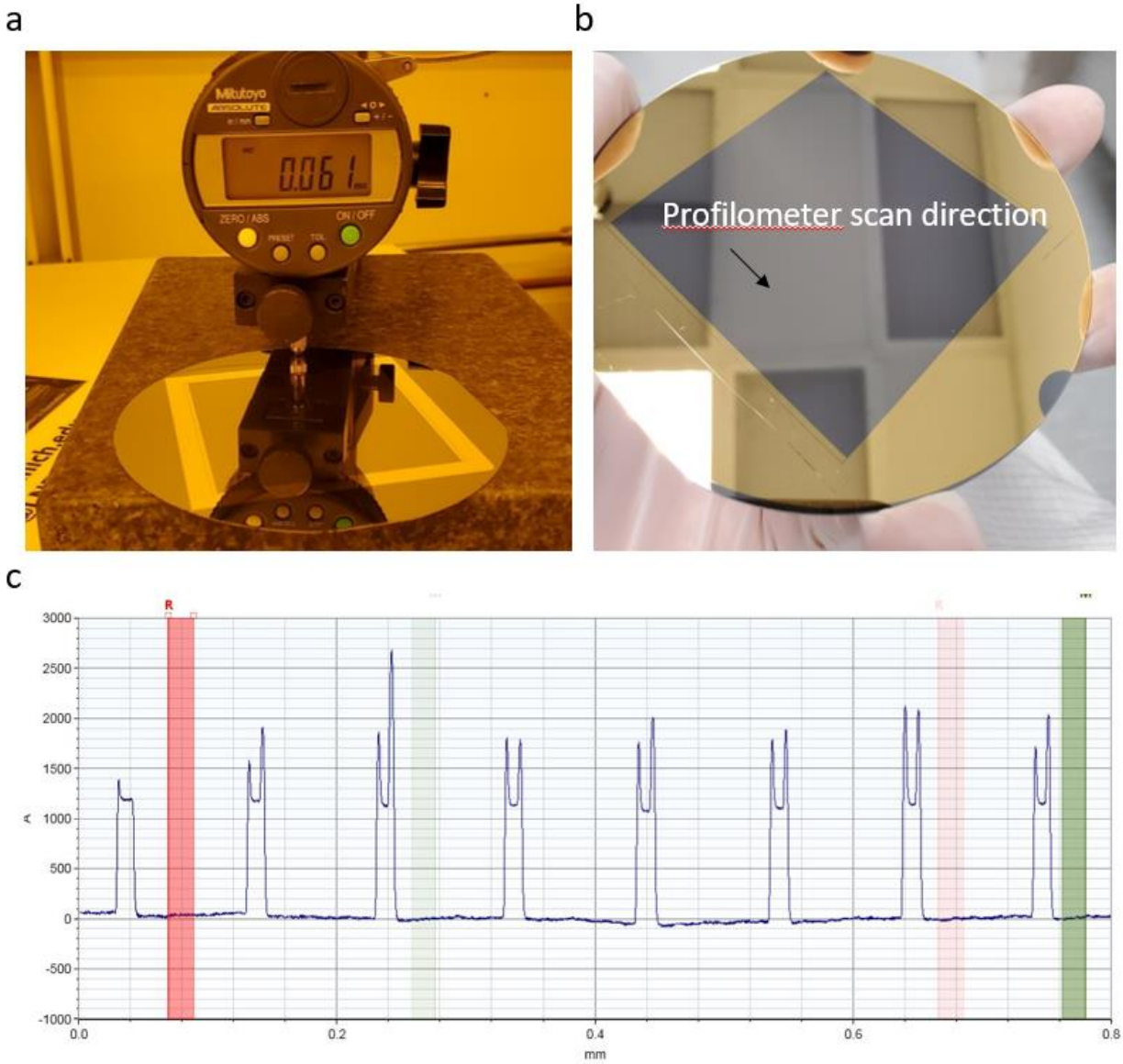

Figure 8.12 : Large-area Si air-bridge formation
Photograph of (a) 4” Si wafer thinned down to 60µm. (b) 6cm × 6cm square sample bonded onto 4” Si handle wafer, forming air-bridge structure. (c) Profilometry measurement of top surface after the bonding.

8.8 Illumination measurement setup and simulation

Figure 8.13 (a) shows a schematic illustration of illumination setup. The cell is mounted to a water-cooled copper stage. A closed-loop chiller keeps the stage temperature at 20°C. Sufficient thermal contact between the cell and stage is achieved by application of a Ga-In eutectic paste at the interface. A SiC globar emitter is positioned above the cell using a three-axis translational stage. The globar is heated to incandescence via Joule heating to simulate the illumination conditions of a thermophotovoltaic generator. Emitter temperature is varied between 1500°C and 1850°C using a variable AC transformer to regulate input power. The view factor, and therefore illumination intensity, may be tuned by varying the position of the emitter relative to the cell. Current-voltage characteristics are measured in the dark and under various illumination conditions using a Keithley 2401 source meter operated in 4 wire sensing mode.

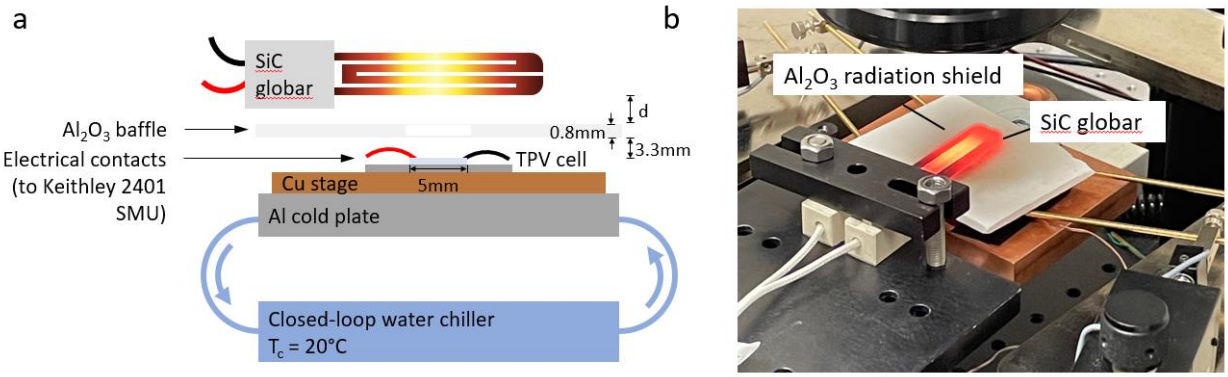

Figure 8.13 : Illumination setup for Si TPV
(a) A schematic illustration of the setup. Cell is mounted on a Cu stage connected to a closed-loop water chiller. Al2O3 baffle with an opening is used to keep the outer area from being heated by the illumination. (b) Picture of the illumination setup.

Emitter characteristics (temperature and emissivity) are measured directly by collimating and redirecting emission into the external port of a Nicolet iS50 FTIR spectrometer. Raw emission spectra are compared to that of a cavity blackbody source (IR-564, Infrared Systems Development Corp.) to normalize for the FTIR system response and optical absorption in the beam path.

SiC experiences thermal decomposition at temperatures exceeding 1710°C, the melting point of the globar's protective SiO_2 coating. To prevent accumulation of decomposed material on the cell, a sacrificial glass deposition shield is positioned over the aperture for emitter temperatures between 1710°C and 1850°C.

Simulated efficiency of air-bridge TPV cell with different emitter temperature is shown in Fig. 8.14. *PCE* was estimated using a similar method in reference 1. There is a monotonic increase in efficiency as a function of emitter temperature due to increased IB absorption from Si. Even at 1500 – 1800 K where Si is considered impractical, we expect 5 – 15% *PCE*. Efficiency roll-off at high current density under 2300 K emitter temperature is due to resistive loss from series resistance.

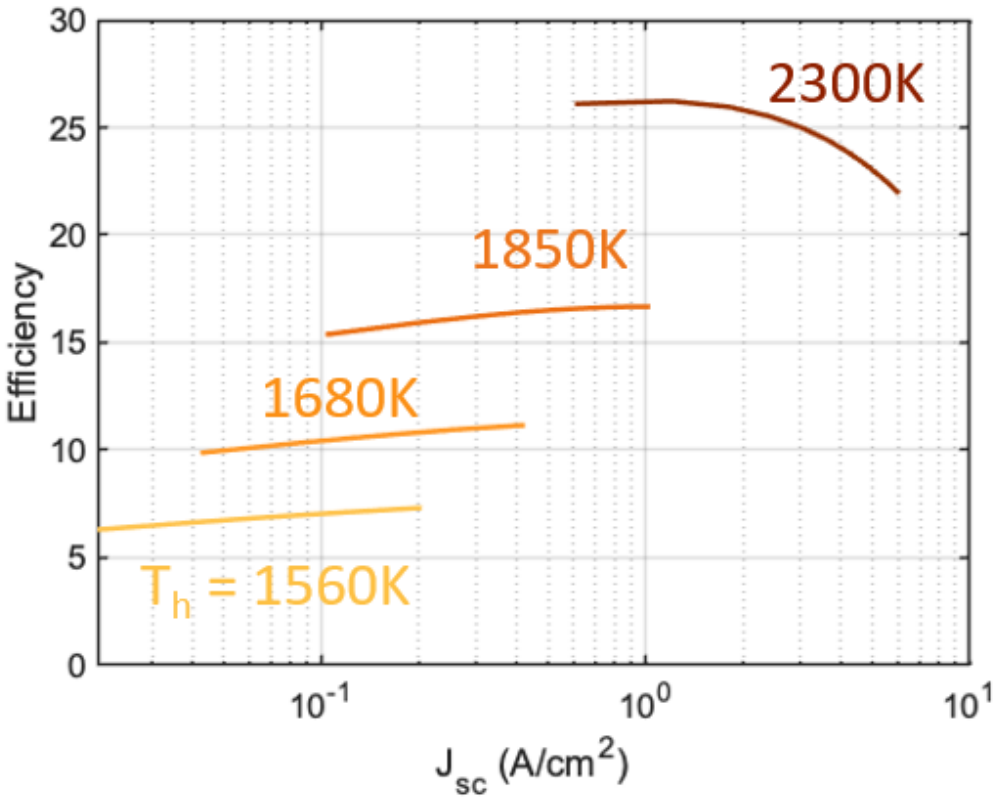

Figure 8.14 : Simulated *PCE* of an air-bridge Si TPV cell

8.9 Conclusion

In this chapter, we describe fabrication of Si TPV devices with air-bridge reflectors. Implementing a lateral *p-n* junction structure formed on top of the Si wafer and varying grid dimensions, we successfully achieve a low-series resistance Si TPV device. Relatively low EQE compared to Si PVs are due to high metal contact area fill factor. However, the top contacts can work as reflectors in TPV applications. Normalized EQE ~70% are found for broad wavelengths with different grid dimensions. Our 90 μm Si TPV cell with 500 nm air-bridge structure achieves ~97% OOB reflectance under 2300K blackbody spectrum, while some of the OOB loss is potentially due to free carrier absorption from the bulk and heavily doped Si layer. While some of the FTIR and SEM measurements are ongoing, with efficiency measurements under heated SiC light source under preparation as well. Once we finish collecting all the data, we expect the work can provide guidelines for expediting the widespread use of TPV applications via implementing low-cost, high-scalability Si.

Chapter 8

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Chapter 9

Conclusion and Future Work

9.1 Thesis summary

III-V compound semiconductors are preferred over elemental semiconductors in high performance optoelectronic applications due to their strong light absorption, bandgap tunability and high carrier mobility. However, their cost due to relatively low throughput growth process and high substrate prices often hinders their deployment in a variety of applications. In this thesis, we demonstrated a pathway to cost reduction of III-V semiconductors using epitaxial lift-off and substrate recycling. Separation of the epitaxial active layer from its growth substrate allows for both the fabrication of high-performance optoelectronic devices and potential cost reduction via substrate recycling. Cost of solar cells can be further reduced by using concentrated PV systems to replace the costly semiconductor materials with low-cost reflective concentrators. Furthermore, we estimate GaAs single junction photovoltaic cell manufacturing cost, with potential methods to improve the throughput of molecular beam epitaxy (MBE) growth. We conclude that the throughput is not a major bottleneck in lowering the cost of III-V semiconductor devices, which is a misperception among the community. As a light detection application, weo demonstrated a hemispherical focal plane array of GaAs detectors, showing how a thin-film structure can benefit the devices in terms of achieving fabrication on unconventional surfaces. Another energy harvesting application is thermophotovoltaics (TPV), where radiated photons from high

temperature sources are converted into electricity. We use an InGaAs thin-film cell with Au back reflector for near-field TPV (NF-TPV), which improves energy transfer via near-field radiative heat transfer. We finally demonstrated an air-bridge Si TPV cell with high out-of-band (OOB) reflectance that can potentially operate in conjunction with relatively low temperature sources. In this chapter, we briefly cover opportunities of future work regarding non-distructive epitaxial lift-off (ND-ELO) and Si TPV.

9.2 Future work: Improving ND-ELO

Despite its high cost, thin-film GaAs photovoltaics can still be favored over Si in certain applications due to its light weight, flexibility and high-efficiency. Applications such as space solar or small-scale energy harvesting including wireless sensor nodes (WSN) or microbots are good examples where GaAs thin-film PVs can outperform Si. Our analysis in chapter 7 expect that the dominant factor in GaAs PV cost is the substrate, rather than the throughput of the growth system. And substrate recycling is probably the most efficient way to reduce the substrate cost in manufacturing processes. ND-ELO has a potential for substrate recycling of III-V compound semiconductors due to its simplicity of protection layer structures. It can also be applied to virtually any type of substrate, as far as selective etching of alternating layer can be achieved. Yet in our work in chapter 3, we demonstrated that there is potential of particle generation during the process, especially in large scale wafers. This can ultimately limit the number of growth cycles and thus the final substrate cost.

9.2.1 Megasonic cleaning and sol-gel brushing

One potential method to reduce the particle density during the ND-ELO process to use sol-gel brushing and megasonic cleaning. Fabrication of the NF-TPV cell described in chapter 6 requires particle-free, flat surface on the top of the cell to achieve near field approach with the

emitter. Particle generation on the surface during the fabrication and InP substrate etch was always a problem, and introducing sol-gel brushing and megasonic cleaning step helped increasing the yield of devices to 95%. A device mesa structure before and after cleaning during the NF-TPV fabrication is shown in Fig. 9.1 (a) and (b), respectively. Any type of particle generated during the wet etching process has been successfully removed. Such a cleaning method can potentially be applied to ND-ELO process in terms of macroscopic particle control, as the biggest hurdle we experienced during scaling up was particle generation, rather than the microscopic surface

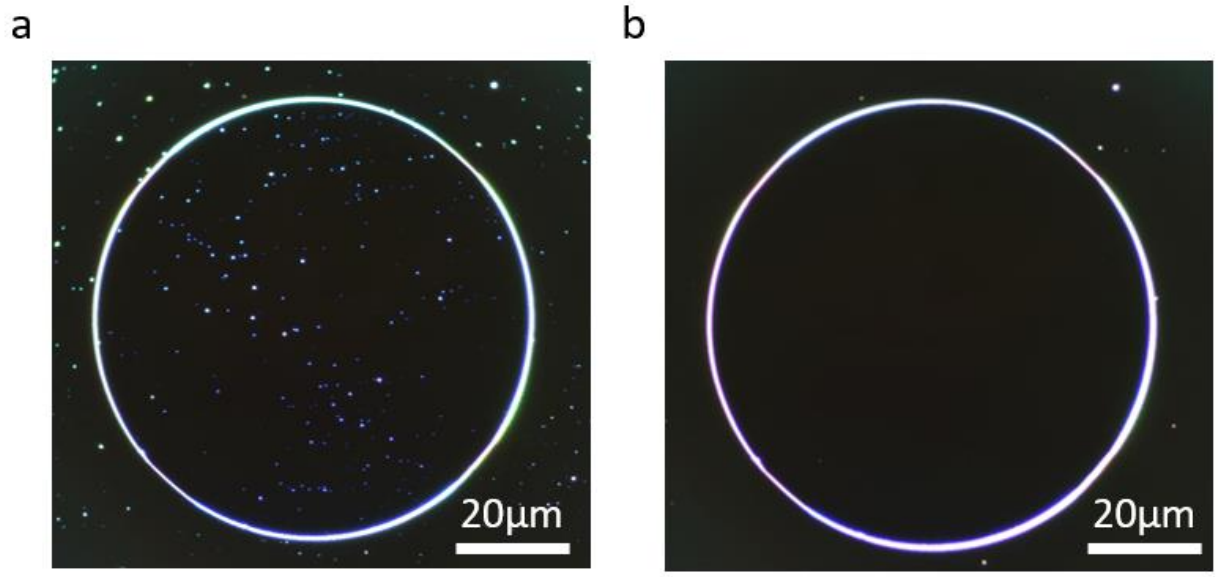

Figure 9.1 : Effect of megasonic cleaning and sol-gel brushing
Dark-field microscopy of NF-TPV cell (a) right after the InP etch, and (b) after sol-gel brushing and megasonic cleaning.

recovery of GaAs.

9.2.2 Particle accumulation on the edge and bonding

Another potential issue in ND-ELO is the bonding process. Using Au-Au cold welding often results in particle accumulation on the edge due to imperfect growth and bonding. Any type of metal particle on the surface can severely impact the regrowth. The bonding layer for ND-ELO needs to be stable in ~24 hours exposure to HF and the following fabrication processes including

wet etching of III-V compound semiconductors and standard lithography process. Finding an alternate bonding material is key to solving the edge metal particle accumulation problem. Parylene-C can be a potential candidate, as it is widely used for surface passivation or insulation layers, and has been proven to be stable in HF vapor.[1] Effects of long-term exposure to HF solution still needs to be tested. As parylene can be etched using oxygen plasma, any particle generated during parylene deposition or bonding can be removed with plasma cleaning. Au particles are much more difficult to remove since the Au etchant also attacks the III-V compound semiconductors. Another potential benefit of parylene-C is that the bonding can be achieved at much lower temperature and pressure compared to Au-Au cold-welding, and thus introduce less strain across the sample during the bonding. This can potentially impact the fabrication of the mechanically sensitive thin-film structure.

9.3 Future work: Si TPV

For operation of TPV cells under the heat sources with emission peak energy much lower than the bandgap energy, improving out-of-band (OOB) reflectance is critical.[2] Even though we achieved ~97% OOB reflectance with the Si TPV, gaining the remaining 3% OOB reflectance can drastically improve the power conversion efficiency. In this section, we introduce a few potential pathways to minimizing the parasitic absorption of OOB photons.

9.3.1 Improved metal top contacts

Free-carrier absorption increases as the fourth power of wavelength,[3] and can be detrimental to OOB reflectance as discussed in chapter 8. One potential loss of OOB reflectance in our current Si TPV design is the exposed heavily doped layer underneath the top contact grid. A microscope image of current Si TPV grid is shown in Fig. 9.2 (a). Metal grids were initially designed narrower than the heavily doped Si area to ensure the isolation of contact and bulk Si. With insulation of the

oxide layer, metal contacts wider than the heavily doped Si area can still be deposited without shunting the device. However, as the oxide thickness is less than ~100 nm, patterning the contact opening can be tricky, especially with wet etching where lateral etching of the oxide can result in the device leakage path. An illustration of current contact grid design and proposed design is shown in Fig. 9.2 (b).

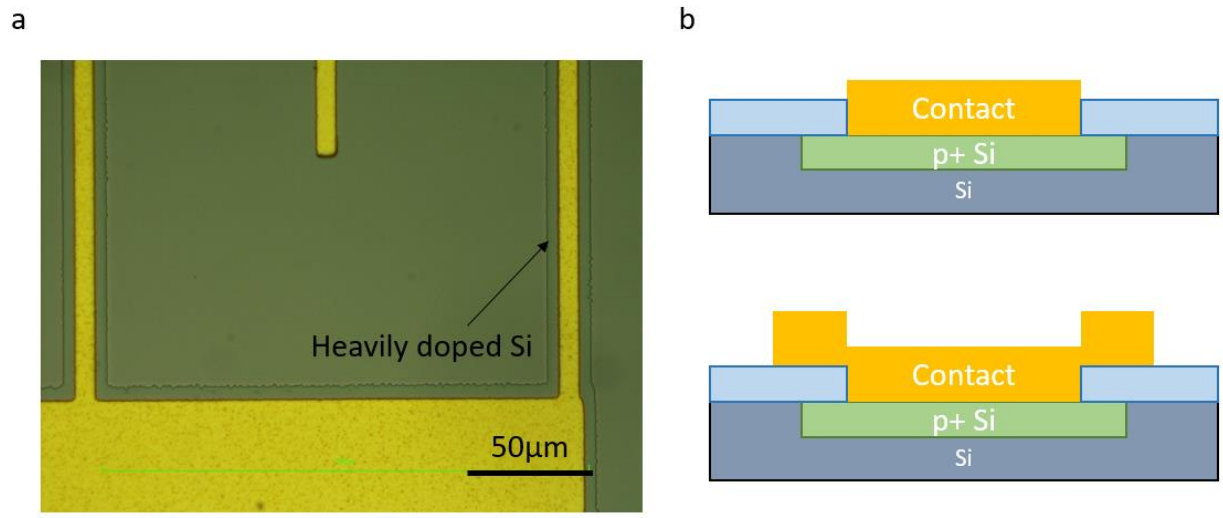

Figure 9.2 : Si TPV grid design and improvement plan
(a) Microscope image of current Si-TPV grid design, showing exposed heavily doped Si area. (b) Schematic illustration of (Top) current Si TPV grid design, (Bottom) improved grid design to minimize parasitic absorption.

9.3.2 Absorption from the bulk Si

Parasitic absorption from the bulk is another OOB loss mechanism. Even if the background doping is $10^{15} \sim 10^{16}$ cm^{-3} which can be as low as Czochralski Si wafers can achieve, absorption from 300 µm thick Si can still become an obstacle for achieving near-unity OOB reflectance. Using near-intrinsic float-zone Si wafers can potentially minimize bulk absorption. Another way is to use a thin Si layer (30 – 50 µm), but precisely controlling the thickness by thinning the back is difficult. Using silicon-on-insulator (SOI) wafers and laterally etching the SiO_2 layer allows precise control of thin-film Si thickness, but can potentially limit the scalability or fabrication throughput due to slow lateral etching of SiO_2.[4] Figure 9.3 shows our preliminary measurement of 30 µm thick Si on

500 nm air-bridge structure, using SOI wafer process. Measured absorption shows good agreement with simulation using transfer matrix methods[5] in the OOB range, with ~99.5% OOB reflectance.

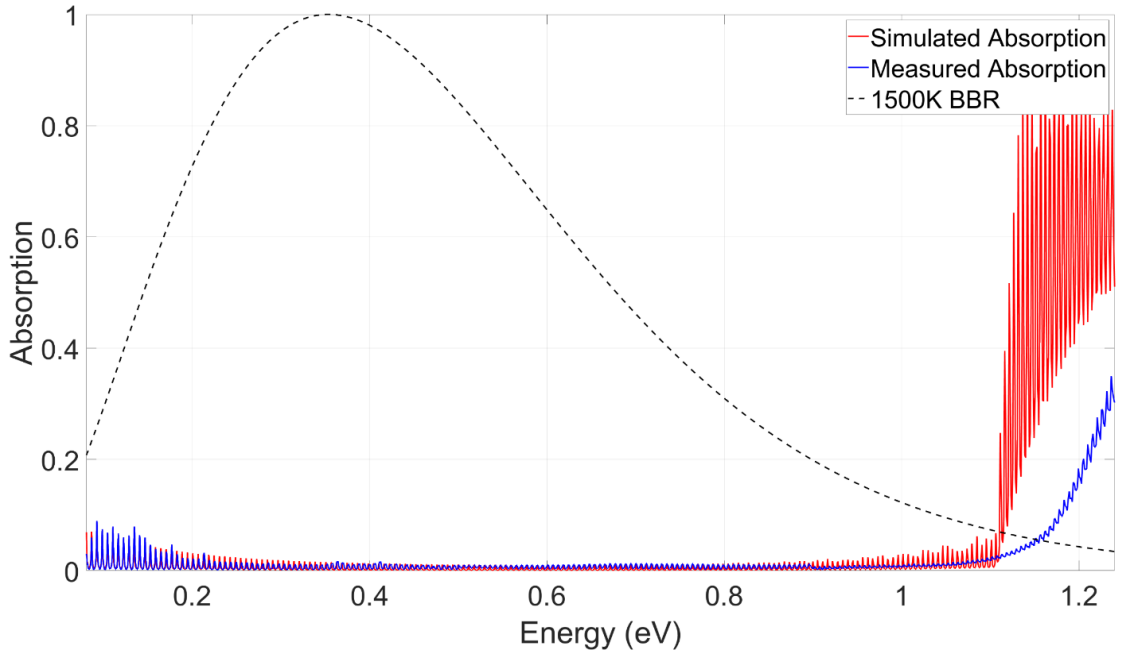

Figure 9.3 : Simulated and measured absorption spectrum of 30µm thick Si with air-bridge reflector

Several potential challenges exist with SOI processing and thin film Si TPV. First, prolonged exposure to HF can increase the surface recombination velocity, and passivation of thin-film Si can be difficult due to handling. Second, general handling of thin-film Si after separation can be extremely tricky, especially with increasing sample size. Finally, spectral efficiency is also affected by in-band (IB) absorption, and there exists a trade-off between IB absorption and OOB reflectance as the wafer is thinned to 30-50 µm. With all the challenges, thinning the Si wafer down to ~90 µm before air-bridge formation can be a less effective, but is a realistic solution to reducing the bulk parasitic absorption.

9.3.3 Alternative back surface reflector

A new type of back surface reflector (BSR) that can outperform the air-bridge reflector may lead to improved OOB reflectance. Even though the air-bridge reflector enhanced OOB reflectance

to nearly ~99% for InGaAs, there still exists a loss channel at the air and gold interfaces. Although challenging, achieving completely lossless reflection and thus near-unity OOB can enhance the TPV efficiency up to ~50% assuming no resistive losses.[2,6] Pyramid structures commonly used for light trapping in Si PV cells[7,8] can potentially be an alternate BSR if formed at the back surface of the TPV cell. Figure 9.4 (a) shows a conceptual illustration of the proposed pyramid structure. Total internal reflection (TIR) at the facets of the pyramids allows lossless reflection at the interface. A preliminary result of simulated transmittance, reflectance and absorption is plotted in Fig. 9.4 (b), with calculated reflectance of 99.93% for energy < 0.95 eV. Due to the lengthy runtime of the simulation, the initial number of data points is limited and may affect its accuracy.

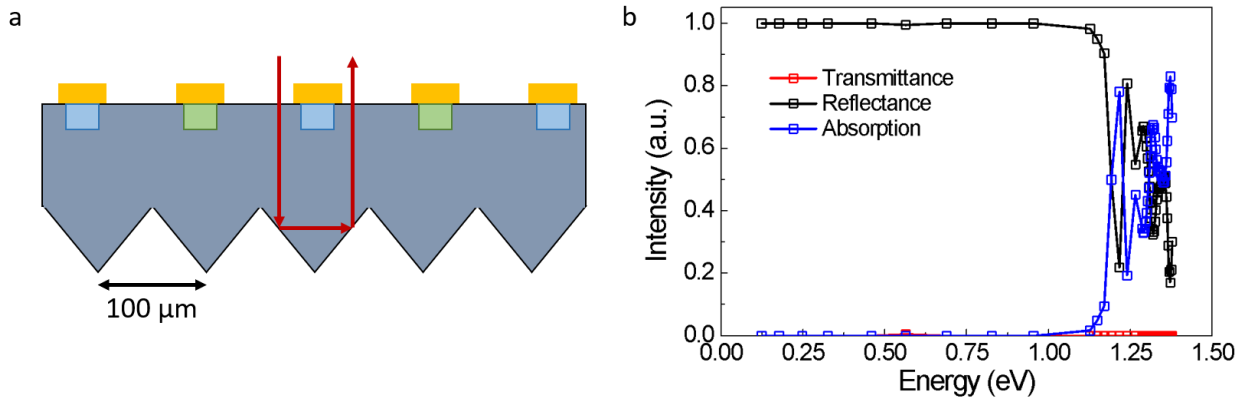

Figure 9.4 : Pyramid structure back surface reflector
(a) A schematic illustration of proposed pyramid BSR structure integrated at the back surface of Si TPV cell. (b) Simulated transmittance, reflectance and absorption of proposed structure.

Several challenges regarding implementing the structure can be expected. First, handling the wafer after pyramid formation may be tricky as the structure is formed on the bottom surface of the substrate. Second, careful alignment between the pyramid structure and top contact grid is needed, as some of the reflected light from TIR can be absorbed at the heavily doped Si layer, if the contact grids are not aligned properly. Lastly, installation into the TPV system might be difficult due to the bottom surface roughness.

9.4 Conclusions

We summarized our efforts on cost reduction of III-V semiconductors via substrate recycling, concentrated PV and increasing the throughput with a conceptual, new growth system. We also demonstrated thin-film optoelectronic devices including a hemispherical GaAs photodetector array, InGaAs NF-TPV cells and Si TPV cells with air-bridge back surface reflectors. Our results show how thin-film structures can be applied to optoelectronic devices for cost reduction and performance enhancement. With potential room for improvements described in future work, we expect thin-film structures will keep playing an important role in high-performance, cost-effective optoelectronic devices. Additional works related to organic photovoltaics will be covered in appendices.

Chapter 9

Bibilography

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Appendix A

Cost Estimates of Production Scale Semitransparent Organic Photovoltaic Modules for Building Integrated Photovoltaics

Building integrated photovoltaics (BIPVs) are attached to commercial and residential structures to enable solar energy harvesting. While conventional Si photovoltaics (PVs) are dominant in the current market, second and third generation thin film solar cells based on amorphous Si, CdTe, CIGS, perovskites or organic photovoltaics (OPVs) are often considered as an alternative for BIPV applications since they may offer reduced costs compared to Si PVs. Indeed, recent advances in performance suggest that lightweight, flexible and visibly transparent OPVs can potentially be integrated into windows or other applications to which Si PVs are less well suited. Here, we estimate the cost of high efficiency, semitransparent OPVs (ST-OPVs) based on solution processing in a roll-to-roll (R2R) manufacturing line. Assuming modules with 10% power conversion efficiency (*PCE*), a 70% geometric fill factor (*GFF*), and 95% inverter efficiency, we anticipate a \$1.6/W_p module manufacturing cost that includes the cost of the microinverter to condition the OPV dc output to be compatible with the ac line voltage of the building. The materials and inverter cost comprise ~90% of the total module cost. Hence, with simplified material synthesis and a lower inverter cost, including marginally improved *PCE* and *GFF*, we expect the cost can be as low as \$0.47/$W_{p.}$ While the module costs ~60% of the average (uninstalled) double-pane window, we expect the payback period can be as short as 2 to 6 years, suggesting that OPVs can be an economic and attractive candidate for BIPV applications.

A.1 Introduction

Building integrated photovoltaics (BIPVs) are a space-efficient means for harvesting solar energy by replacing or covering a part of a building (e.g. rooftop, façade or windows) with photovoltaic modules.[1–4] More than 80% of the current BIPV market is based on rooftop installed crystalline Si (c-Si) modules, with the remaining 20% installed mostly on façades.[4,5] Integration of c-Si photovoltaics onto windows, however, has the disadvantage of visible opacity,[6,7] requiring that the cells be perforated with holes, or applied in strips. Both strategies result in a reduction in their geometric fill factor (*GFF*, is the ratio of active cell to total module area), and hence limit the power that can be produced. An alternative approach is to employ visibly semitransparent photovoltaics based on organic semiconductors, quantum dots and perovskites integrated onto windows.[1–3,8–10] However, besides organic semiconductors, application of such materials in BIPV systems has not been reported due to inadequate device performance and reliability, limited scalability, toxicity of materials, or high manufacturing cost compared to c-Si photovoltaics.[1,2] Despite the scalability and successful demonstration of display manufacturing on an enormous scale, organic semiconductors are often considered to be an immature alternative to c-Si PVs within the BIPV industry.[1,2] Recently, organic photovoltaic cells (OPVs) based on DBP:C_{70} with accelerated intrinsic lifetimes extending to T_{80} = 27000 yr have been reported,[11] where T_{80} is a time of operation for the *PCE* to drop to 80% of its initial value. Furthermore, OPVs with cell *PCE* > 17% ,[12] module *PCE* > 14%[13] and neutral density, semi-transparent OPVs (ST-OPVs) with *PCE* > 10% have been reported. [14]

The visible transmittance of the ST-OPV cell is another important metric determining how well the technology is suited for use in power generating windows. To define transparency of the

device, the average visible transmittance (*AVT*) which is the arithmetic mean of transmittance of the cell from 400 to 650 nm is often used. However, a more apt comparison that quantifies the *appearance* of the sunlight entering an interior space is provided by average photopic transmittance (*APT*), which is the transmittance of the cell weighted by the spectral response of human eye to a window illuminated by an AM 1.5G reference spectrum. Then, the light utilization efficiency (*LUE*), which is the product of *PCE* and *APT*, combines these factors into a ST-OPV figure of merit.[15,16] A compilation of the *LUE* vs. *APT* for a range of thin film technologies (including amorphous Si – a-Si – perovskites, and OPVs) originally summarized by Lunt *et al*.[16] and updated by Li *et al*. [15] is provided in Fig. A.1, and device performance of highlighted results are shown in Table A.1. Apparently, ST-OPVs have the highest combination of transparency and efficiency, with a maximum *LUE* = 5%, compared with other thin film solar cell technologies. Given the scalability of OPVs using printing or other roll-to-roll (R2R) manufacturing processes, [17–19] and their possibility for exceptionally long operational lifetimes,[11] these advances point to their particular suitability for BIPV applications, especially for semi-transparent power generating windows.

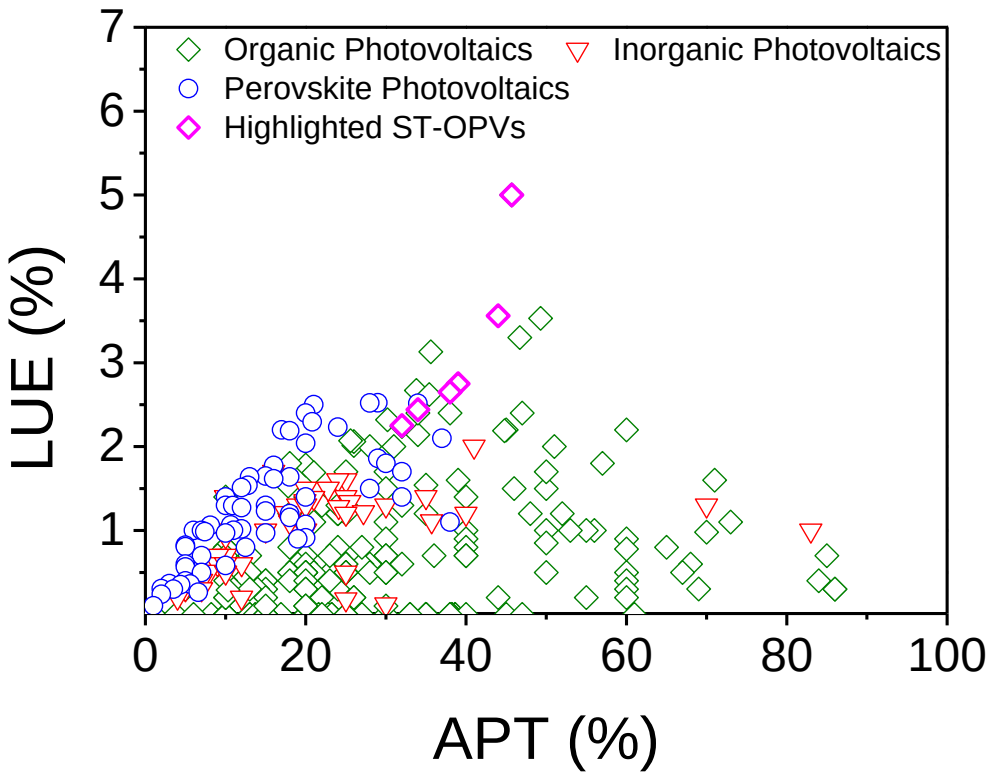

Figure A.1 : Compilation of LUE vs APT of semitransparent photovoltaic cells with different technologies. Data adapted from Refs. [15,16]. APT is recalculated from literature when possible, otherwise the reported average visible transmittance (AVT) is used.

Table A.1 : Recent advances in semitransparent OPV performance

Active layer	J_{sc} (mA/cm^2)	V_{oc} (V)	FF	PCE (%)	APT* (%)	LUE (%)	Reference
PTB7-Th : IEICO-4Cl	17.6	0.714	0.554	6.97	38	2.65	[20]
PTB7-Th : BT-CIC	15.8	0.68	0.662	7.10	39	2.75	[21]
PTB7-Th : IEICS-4F	16.97	0.72	0.58	7.20	34	2.44	[22]
PTB7-Th : ATT-2	17.23	0.71	0.57	7.02	32	2.25	[23]
PTB7-Th : BT-CIC : TTFIC	16.6	0.68	0.72	8.00	44	3.56	[15]
PTB7-Th : A078	20.4	0.75	0.70	10.8	45.7	5.0	[14]

*APT recalculated from the literature if possible, otherwise AVT was used.

Beyond these promising studies of laboratory cell performance, the acceptability of a PV technology ultimately hinges on the cost to produce large scale modules at high volume. Several different estimates of OPV module cost have varied from \$0.2 to \$1.2/W_p based on differing assumptions of materials sets employed, and on module efficiencies that range from 5-10%.[24–28] Up until now, however, most cost analyses are based on opaque cells while also omitting the costs of inverters, and miscellaneous costs such as sales, administrative, marketing, and R&D. Furthermore, they do not consider recent significant advances in OPV technology that have

occurred over the last few years. In this work, we estimate manufacturing cost of *semitransparent* OPV modules based on assumptions and accuracy corresponding to Class 4 of the Cost Engineering Classification System.[29] Starting with estimations of high throughput R2R equipment costs needed for realizing a high efficiency single junction ST-OPV structure, we estimate the maintenance, utility, labor and materials costs. We further estimate costs due to the inclusion of a microinverter for making the solar output compatible with most in-building ac electrical systems. Inclusion of the inverter significantly simplifies power window installation,[30] but is counterbalanced by the added cost of the inverter. Assuming the PV modules are integrated within double-pane windows to simplify encapsulation, we expect a manufacturing cost of \$106.16/m^2. This places a premium on the average double-pane window cost in U.S. of \$106.80/m^2[31–33] including the sealant, frame and assembly costs, based on market data and assuming a 30% margin. We estimate the cost can be as low as \$57.24/m^2, provided that the materials and inverter costs can be incrementally reduced. We assume a base case semitransparent module *PCE* = 10%, which compares with current non-transparent module *PCE* > 14%.[13] With *GFF* = 70%, and an inverter efficiency of η_{inv} = 95%, the estimated module cost without the inverter is \$0.68/W_p, at ~160MW annual production volume. We estimate a microinverter cost of \$0.78/W_p based on market data, which is similar to the household scale Si PV microinverter cost of \$0.45/W_p[34] considering the efficiency differences between the two PV technologies. Assuming modest cost reductions in microinverters, OPV materials, contacts and optical coatings, we estimate the total system cost including miscellaneous costs can be further reduced from \$1.6/W_p to \$0.47/W_p in the foreseeable the future. This suggests an energy payback period of 2 to 6 years depending on the window orientation, local cost of electricity, and location of installation.

A.2 Cost estimate assumptions

We divide the manufacturing cost into four categories – capital equipment, labor, utilities and materials. Additional miscellaneous costs including marketing, general and administrative (G&A), research and development (R&D) are assumed to be 10% of total manufacturing cost based on recent 3-year average of PV manufacturing industry standards.[35] Then, the desired OPV module structure for cost analysis is chosen and performance assumptions are established. For this analysis, we assume a 1 m wide R2R manufacturing web for PV module fabrication. Figure A.2(a) shows a schematic of an archetype semitransparent OPV cell structure. Starting from flexible barrier substrate, the first deposited layer is the transparent cathode, followed by the cathode buffer/exciton blocking layer, active layer, anode buffer, and transparent anode. The layers are encapsulated by a second barrier substrate. For transparency, a mixture of non-fullerene acceptors and energy-level-matched donors that selectively absorb near-infrared (IR) photons are used as the active layer.[20–23,36] Optical layers for outcoupling the visible and reflecting the IR photons are included to increase efficiency and transparency.[15]

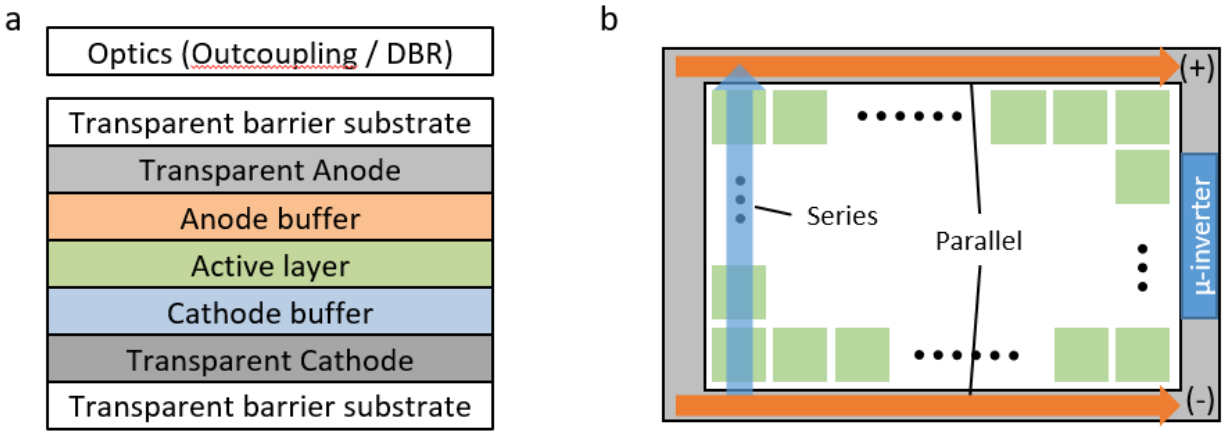

Figure A.2 : Schematic illustrations of ST-OPV cell and module prototype
(a) archetype semitransparent OPV device structure, and (b) proposed PV module layout for window integration. The microinverter (μ-inverter) is positioned outside of the viewing area, and individual cells are laid out in a series-parallel array configuration.

A conceptual, schematic top view of a ST-OPV module integrated into a 1 m × 2 m window used in our cost estimates is shown in Fig. A.2(b). An array of 2 cm × 2 cm ST-OPV cells are connected in a series-parallel circuit within the window module. Electrical interconnects and a microinverter for each module are integrated outside the viewing space of the window. The transparent PV cell foils can be directly attached onto a single-pane window surface without additional encapsulation,[4,37] or they can be inserted into the pocket of a double-pane window[38] as shown in Fig. A.3. In this analysis, we use the latter configuration since it allows for simplified OPV encapsulation with inert gas commonly used within the gap between the panes. The optical coupling layers can be separately deposited onto the inner surfaces of the opposite panes. Integration of the optical coupling layers with the PV module itself is simplified compared to the direct attachment onto a single-pane window, which requires deposition of all layers onto the substrate film, or integration with the encapsulating lid.

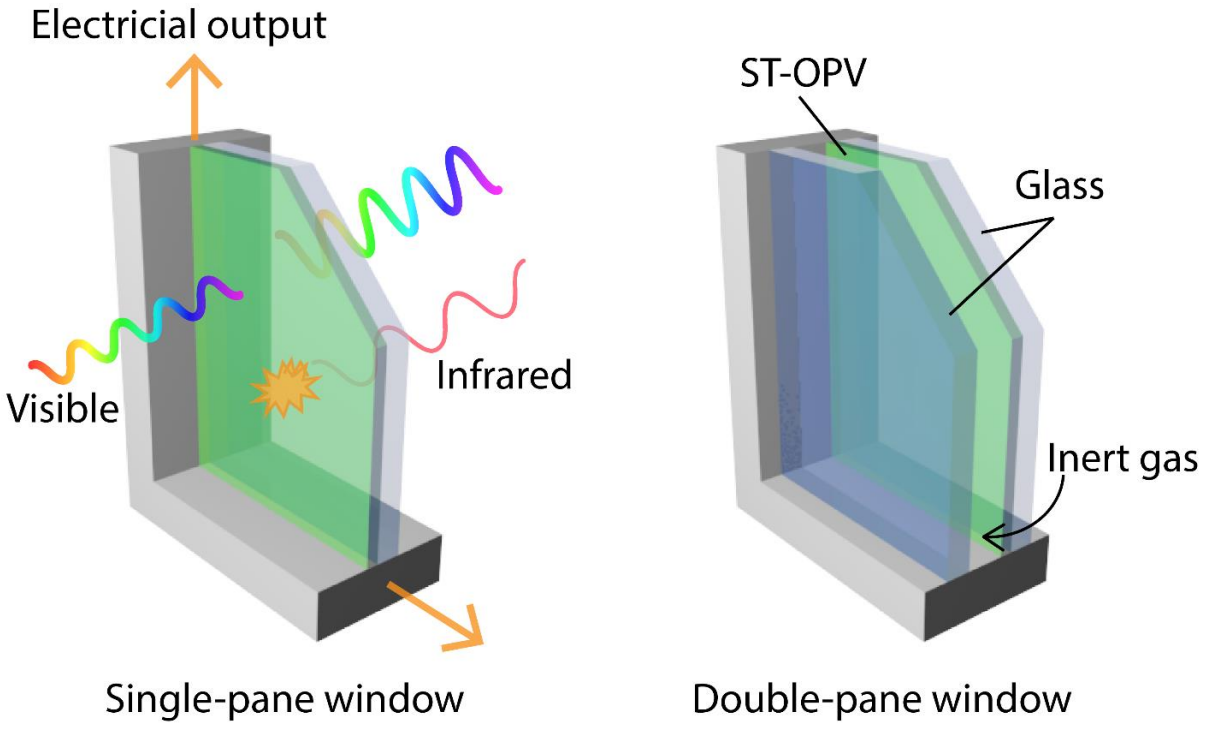

Figure A.3 : Illustration of ST-OPV integrated onto windows
(Left) The PV module is laminated onto a single pane, and (right) into the pocket between a double pane, thermally insulating window. Typically, inert gas fills the gap between the panes.

Figure A.4 shows materials choices and manufacturing processes used in the study. Starting from an ITO-coated transparent PET substrate, the bottom contact is patterned by laser scribing. The ZnO cathode buffer/exciton blocking layer, PTB7-Th:BT-CIC active layer, and MoO_3 anode buffer are consecutively applied via slot-die coating. Each solution process is followed by solvent annealing in an oven integrated within the R2R tool. Before top contact deposition, the active layer is patterned for interconnect attachment using laser scribing. Contact layers are patterned during printing and sputtering and do not require additional scribing. The roll is transferred into a vacuum chamber for thin Ag transparent top contact[15] R2R sputter deposition. After contact patterning, the roll is encapsulated by attachment of a second barrier substrate, spliced into the desired size, laminated onto a glass pane, and assembled into the double pane window.

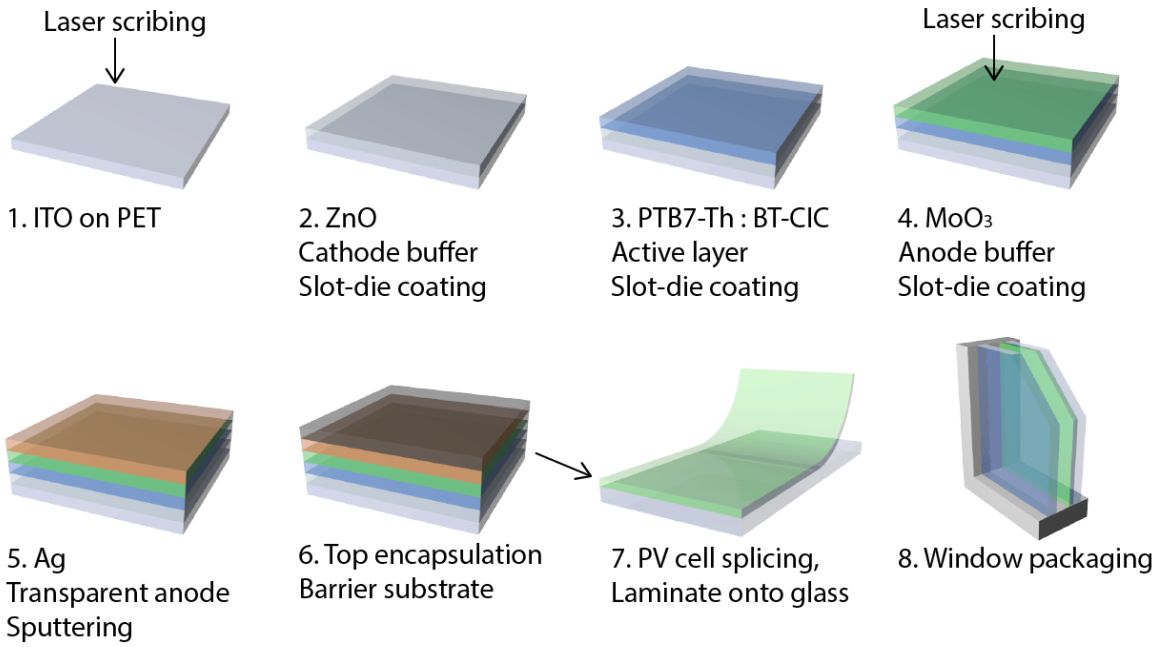

Figure A.4 : ST-OPV module window manufacturing process sequence

A list of required manufacturing equipment and their annual costs assuming 10 year linear depreciation is summarized in Table A.2. Here, we assume a 10 year equipment lifetime, although

depreciation rates of 5 to 7 years are often used to maximize financial efficiency (i.e. to reduce soft costs due to tax adjustments, etc.).[39,40] An accurate plant cost estimate depends on location and total area. For our estimate, therefore, we simply assume a plant cost of four times the total equipment cost, with an additional 10% contingency for waste handling.[26,41] The machine platform comprises a skeletal support structure and R2R web manipulation components including rollers, tensioning systems, motors, etc. Printing and slot-die coating stations include baking ovens for thermal annealing the films after coating. Scribing and test/sort equipment costs were estimated by proportionally scaling the lamination station cost.[27]

Table A.2 : Equipment and plant cost estimation for manufacturing

Item	Required quantity	Depreciation ($/year)	Reference
Machine platform	1	183K	[40]
Slot-die coating station	3	209K	[40]
Sputtering station	1	178K	[39]
Splice table	1	10K	[40]
Laminating station	2	25K	[40]
Laser scribing	2	75K	[40], [27]
Test / sort equipment	1	25K	[40],[27]
Plant cost	-	5.1MM	[22,40]

Plant cost is assumed to be 4 times the total equipment cost, with additional 10% for waste handling.

Assumptions for labor, utilities cost and production parameters are provided in Table A.3. A 5 m/min roll translation speed during deposition ensures stable thickness and quality control of each layer.[27,39,40] Considering a 1 m web width and 5% roll preparation time during the manufacturing cycle, the annual PV module production area is 2.25×10^6 m^2, assuming 11 month/yr and 24 h/day utilization. This production rate corresponds to ~160MW/year production, assuming a base case module performance of *GFF* = 70%, η_{inv} = 95% and *PCE* = 10%, which is

consistent with recent advances in ST-OPV efficiency of nearly 11%[14] and a reported opaque OPV module efficiency of 14%.[13] Here, *GFF* = 70% is a conservative estimate that allows room for inter-cell contacts, and window structures outside of the viewing area. We also assume one unskilled personnel per each lamination, splicing and scribing station, and one skilled personnel per each coating and printing station, resulting in a total of 6 unskilled labor and 5 skilled labor per production line. With 55% employee benefits, $15/h and $20/h unskilled and skilled wages, the annual labor costs are $1.2MM and $1.3MM, respectively. As our estimate is not at a stage to confirm detailed manpower cost such as marketing, human resources, legal or financial cost, the marketing and selling costs are included in the 10% miscellaneous cost. Additional labor might be required when detailed manpower structures are confirmed. We include electricity costs of $83K/year for sputtering and $44K/year for coating and printing utilities support based on estimated power consumption and an industrial electricity costs of $0.07/kWh.[42] Lamination, splicing and testing/sorting stations are assumed to use half the power of the coating and printing stations. Additional utilities costs such as process chilled water are $100K/system/year. Maintenance of $10K/year is assumed for each station.

Table A.3 : Cost of ownership assumptions

Item	Unit	Value
Roll moving speed	m/hr	300
Roll preparation and loading time	hr/hr	0.05
Substrate width	m	1
Production area per system	m^2/year/system	2.25MM
Unskilled labor	/system	6
Skilled labor	/system	5
Unskilled wage	$/system/year	$1.2MM
Skilled wage	$/system/year	$1.3MM
Electricity – Sputter[(a)]	$/equipment/year	$83K
Electricity – Coating / Printing station[(b)]	$/equipment/year	$44K
Utilities – Process chilled water, etc.	$/system/year	$100k
Maintenance	$/equipment/year	$10K
Maintenance time	month/year	1

(a) From refs. [38,40]

(b) From refs. [39,40]

A.3 Cost estimate results

With these assumptions, the manufacturing cost is calculated by dividing the total cost for annual production by the area produced, as listed in Table A.4. Materials costs for each layer is the product of the amount of material required, and the source material cost based on weight, We assume 80% material utilization efficiency for solution processed layers, and 25% for sputtered layers.[39,40] Since active layer materials costs are unavailable in volume quantities, we estimate the bulk organic semiconductor cost based on $31/g/synthesis step, times number of steps required.[43] A three-step synthesis of PTB7-Th,[44] five-step synthesis of BT-CIC[21,36] for a PTB7-Th:BT-CIC 1:1.5 mixture results in $130.2/g. Using the density of the mixture after annealing, an active layer thickness of 160 nm, we obtain $29.67/$m^2$ for the active layer materials. Materials cost estimates for ITO on PET, barrier substrates, ZnO, MoO_3, and Ag are provided in Table A.5.

Table A.4 : Itemized manufacturing cost estimate ($/m^2)

Layer	Equipment/plant	Utilities	Labor	Materials	Inverter	Total
Plant cost	2.24	0	0	0	0	2.24
Machine platform	0.08	0.02	0.09	0	0	0.19
ITO on PET substrate	0	0	0	5.00	0	5.00
ZnO Cathode buffer	0.09	0.02	0.12	0.02	0	0.25
PTB7-Th : BT-CIC Active layer	0.09	0.02	0.12	29.67	0	29.89
MoO_3 Anode buffer	0.09	0.02	0.12	0.03	0	0.26
Ag Top contact	0.08	0.04	0.12	0.13	0	0.37
Top barrier substrate	0	0	0	1.5	0	1.5
Lamination	0.02	0.03	0.17	0.09	0	0.31
Splicing / Scribing	0.09	0.04	0.26	0	0	0.39
Testing / sorting	0.01	0.01	0.09	0	0	0.11
Optics	0	0	0	4	0	4.00
Inverter	0	0	0	0	52	52.00
Total[(a)]	2.78	0.2	1.07	40.43	52	96.51

(a) Values shown in the table are before additional 10% miscellaneous cost is added

Table A.5 : Materials cost estimate

Layer	Supplier	Layer thickness	Density (g/cm^3)	Usage (mg/m^2)	Cost ($/g)	Cost ($/$m^2$)	References
ZnO	Sigma aldrich	20 nm	5.6	7	3.9	0.02	[45]
MoO3	US research nanomaterials	20 nm	4.7	6	4.8	0.03	[46]
Ag	Kurt J. Lesker	15 nm	10.5	63	2	0.13	[47]
ITO on PET	Li Da tech.	-	-	-	-	5.0	[48]
Barrier substrate	Amcor	-	-	-	-	1.5	[27]

80% utilization factor for solution processing and 25% utilization for vacuum processing was assumed.
ZnO and MoO3 nanoparticles dispersed in H_2O with 20 wt. % was used for cost estimation.
Order scale of 100~500g was assumed for ZnO and MoO3, as monthly usage of 1500g is expected with production rate and materials usage.
Ag sputter target with highest volume available from the vendor was used for estimation.
Barrier substrate cost was cross referenced from a recent publication as the market cost was not readily available

The optical coating structure depends on the location and orientation of the installation. We estimate the cost of the coating by subtracting the cost of glass without coating ($3/$m^2$), from the cost of glass with an anti-reflective coating ($7/$m^2$).[49] A microinverter is required to combine the outputs of several photovoltaic modules into the ac power line of the building to compensate for non-uniform solar illumination on each module[30]. For a 2 m × 1 m module comprising an array of series and parallel connected 2 cm × 2 cm cells, each with an open circuit voltage of 0.7 V and short circuit current of 16 mA/cm^2 for APT = 50%,[15] we estimate a 16 Adc and 34 Vdc maximum module output. We use an inverter price of $52/$m^2$ estimated by applying a 20% bulk purchase discount from commercial price.[50] With an additional 10% miscellaneous cost premium, we arrive

at a total module cost estimate of $\$48.96/m^2$ and $\$106.16/m^2$ without and with the inverter, respectively.

Although our materials cost estimates are as realistic as possible at this time, we nevertheless expect a ±30% error for active layer and optical layer coatings, considering the lack of information on bulk-production active layer materials cost, and location and orientation dependence of the window. We expect a potential ±20% error for other PV layers due to cost variations between different vendors, and the expected purchase volume. A sensitivity chart according to the estimated errors is shown in Fig. A.5.

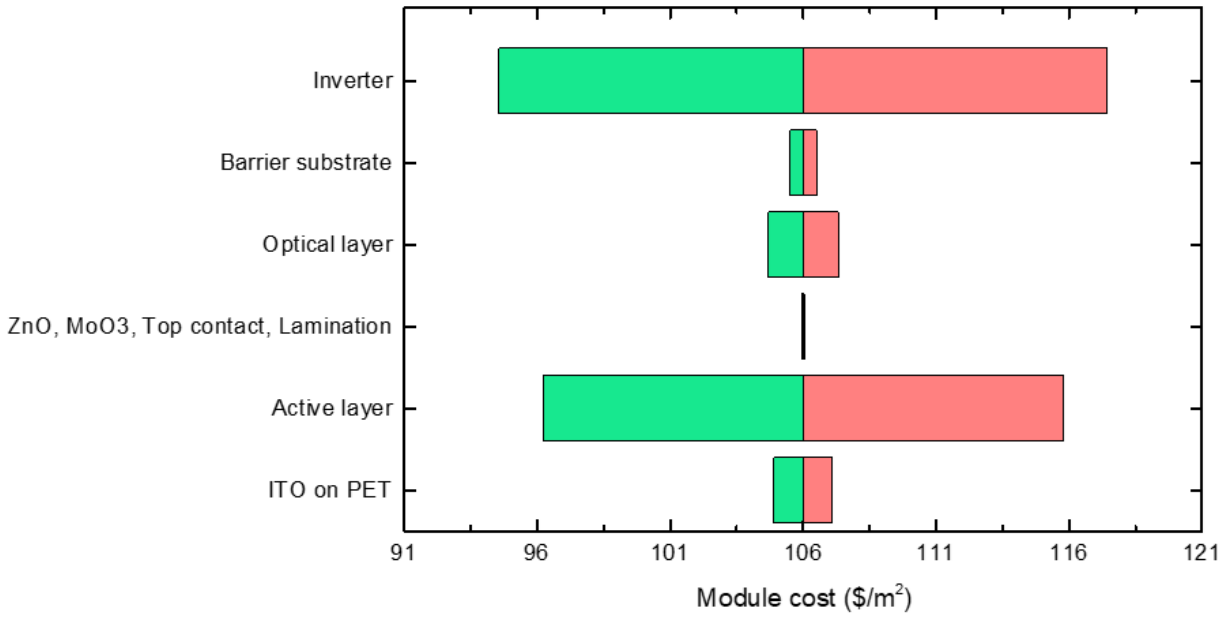

Figure A.5 : Cost sensitivity for different materials
Active layer and optical layer errors were estimated to be ± 30%, considering the limited data of bulk cost for active layer and orientation / installation dependence of optical layer. Errors for other items are estimated as ± 20%

A.4 Potential cost reduction scenarios

Our analysis indicates that materials cost comprises ~90% of total PV module manufacturing cost. This result agrees with previous analyses normalized to our production levels that indicate the material costs are dominant, accounting for 90-98% of total module cost [24–28].

Due to high R2R system throughput, the fixed costs scale inversely, whereas material and microinverter costs scale linearly with the area produced. Indeed, this conclusion is consistent with other volume-manufactured PV technologies where materials are found to consume a large fraction of the total system cost.[34,49,51,52] The production of 160 MW/year can lead to additional costs for handling and warehousing; considerations needed to refine future cost estimates.

Figure A.6(a) shows a potential scenario in materials cost reduction without including the 10% miscellaneous cost contribution. The most expensive device component is its active layer due to its thickness, and the several steps used in materials synthesis. If the materials require only a 2-step synthesis, the materials cost can be reduced by 38%. The ITO on PET anode and the optical coating are the next most expensive contributions. This suggests that development of cost-effective, flexible and transparent contacts is an important challenge to be met for reducing ST-OPV costs. With the assumption of 50% future reduction in the bottom contact, optics and barrier substrate costs, the total materials cost is reduced by additional 11%. PV glass cost including the module, inverter and miscellaneous costs compared with double-pane windows[31–33] is shown in Fig. A.6(b). Initial estimates suggest that PV glass is approximately twice as expensive as an average double-pane window. With modestly improved cost efficiencies, the additional cost from PV module integration can be only ~60% of average, uninstalled windows cost. Another important factor to consider is that double-pane windows are priced between \$50/m^2 – \$200/m^2, from low-end to high-end models.[31–33] Considering that power generating windows will be positioned as high-end products, the PV module cost can range from 33% to as low as 25% of the total installed power generating window cost.

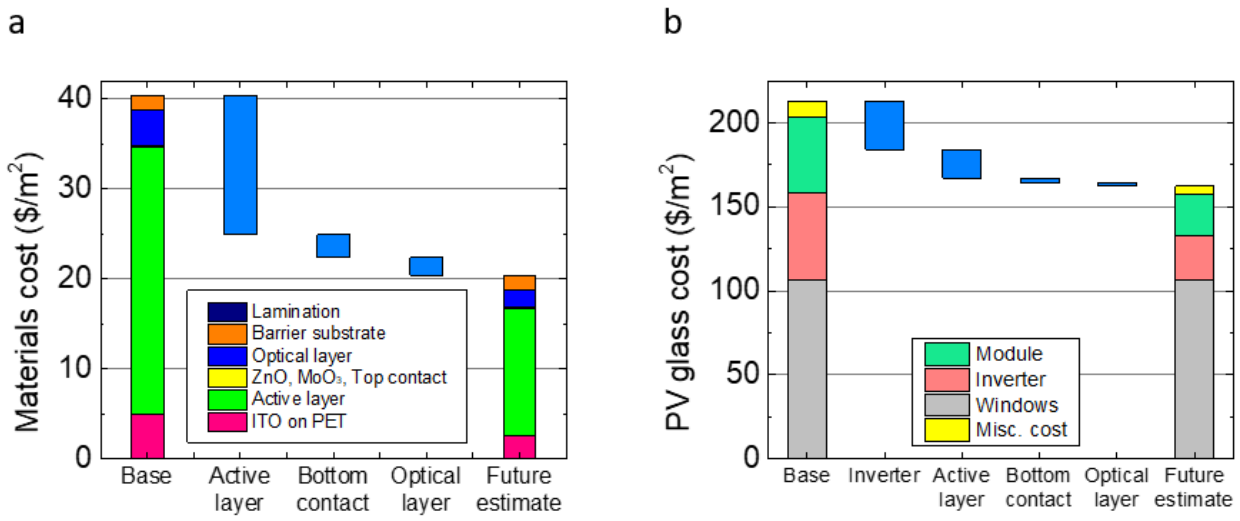

Figure A.6 : ST-OPV cost reduction scenarios
(a) materials cost in manufacturing ST-OPV modules with the impacts of several cost reduction scenarios, and (b) total PV glass cost including the window panes and the impacts of several cost reduction scenarios.

The module cost including the microinverter is shown in Fig. A.7. Additional simplifications in materials synthesis and a 50% reduction in microinverter costs changes the module cost from a base case of \$1.6/W_p, to \$1.16/W_p. Provided that ST-OPV lab efficiency is increased to yield a module *PCE* = 15% and *GFF* = 90%, the cost further reduces to \$0.47/W_p. These realistic improvements in performance in the near future suggest that the production cost of ST-OPVs can be on par with Si photovoltaics.[34]

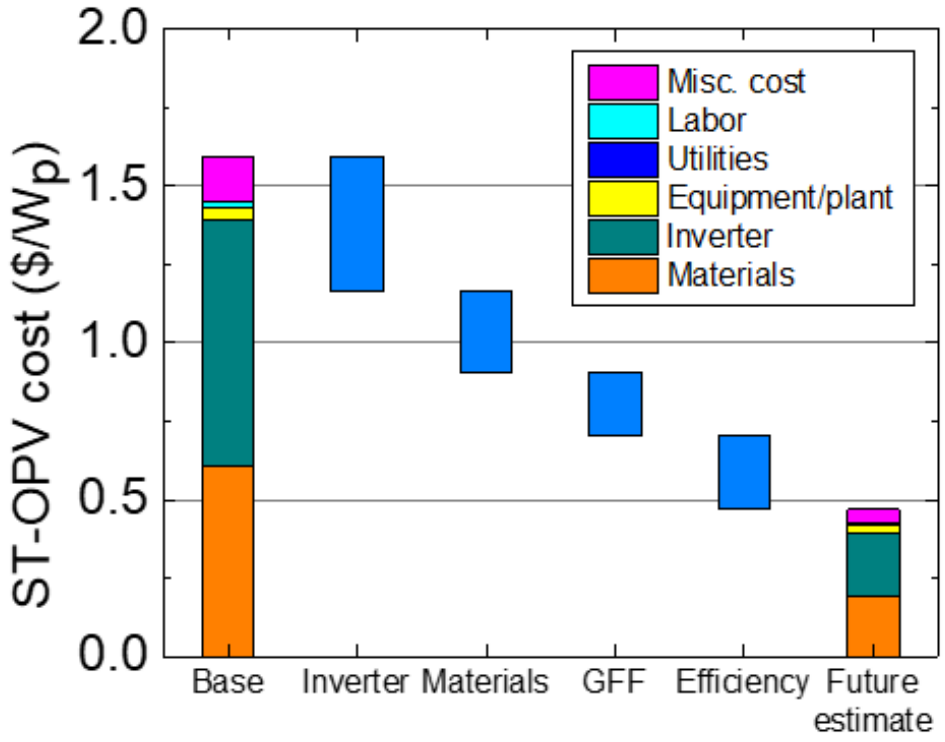

Figure A.7 : ST-OPV module cost reduction scenarios
Waterfall diagram showing module and inverter cost in $/$W_p$ and the impacts of several cost reduction scenarios based on projected modest device performance improvements described in text

A.5 Payback period estimation

To estimate the economic feasibility of ST-OPV windows, we simulate annual power generation from a BIPV module with *PCE*=15%, *GFF*=90% using the PV-GIS tool[53] in multiple regions across the U.S., from latitudes 27° to 48°. For comparison, a calculation based on the annual solar path assuming uniform, AM 1.5G solar irradiance of 800W/m^2 is also provided to show the latitude dependence without effects of weather or altitude of different locations.[51]

Five different configurations were modelled: east and south facing windows, east and south facing 45° tilted surfaces, and the optimal orientation determined by the PV-GIS tool. The data

points in Fig. A.8 show the estimate based on annual solar irradiance data, whereas dashed lines show calculation based on uniform irradiance throughout the year. Bars centered at each data point allow for variants in altitude differences within the regions at the same latitude.

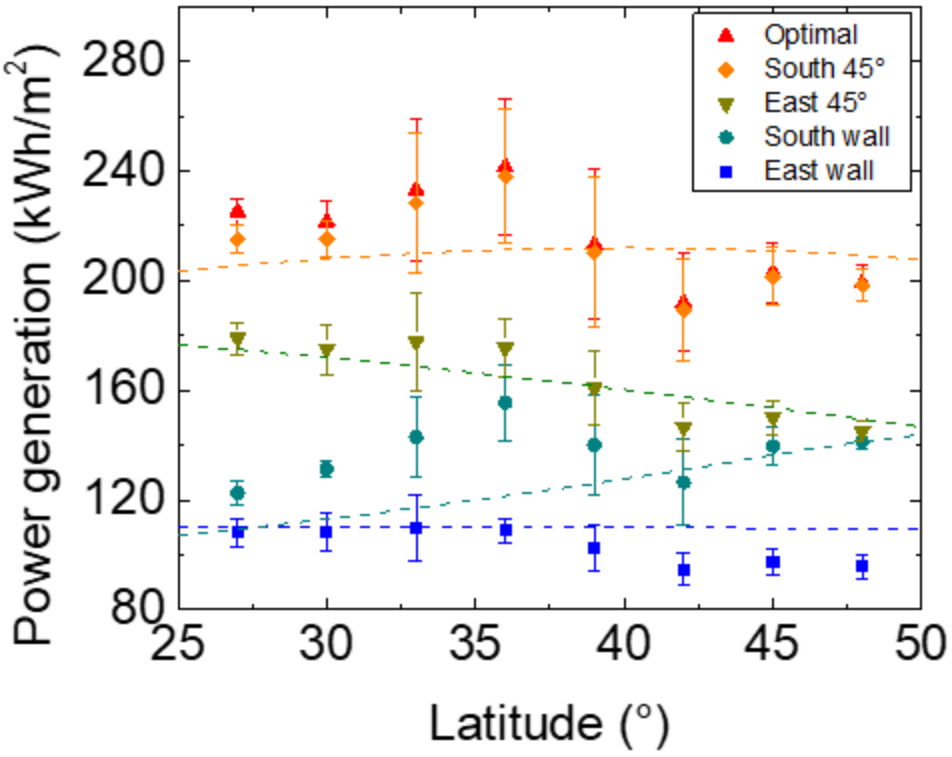

Figure A.8 : Annual power generation from ST-OPV window
Simulated annual power generation from ST-OPV windows vs. latitude. The calculations are shown for different module orientations, and are based on annual solar irradiance from the PV-GIS tool (data points), and based on uniform, AM1.5G, 800 W/m^2 (peak) solar irradiance (dashed lines). The vertical bars for each data point account for variations in average cloud cover and altitudes at different locations within a given latitude.

There is only a small dependence of annual power generation on latitude for south facing, 45° tilted surfaces, and east facing windows. East facing 45° tilted surfaces show a monotonic decrease, and south facing windows show an increase of power generation with increasing latitude. With the module cost estimate of \$55.52/m^2, and a typical residential electricity cost of \$0.13/kWh,[42] the payback period of the ST-OPV window module ranges from 2 to 6 years, depending on the location and orientation of the installation.

A.6 Conclusion

Our study of the manufacturing cost for ST-OPV modules used in power generating windows suggests that high throughput R2R manufacturing can potentially enable large scale production of economically feasible and visually attractive building applied solar harvesting appliances. A principal conclusion of our analysis is that materials and microinverter costs are the dominant contributors to total module cost, significantly overtaking the costs of equipment and other miscellaneous operational costs. Starting from $\$1.6/W_p$ estimate based on current ST-OPV performance, we expect the cost could be as low as $\$0.47/W_p$ with modest future improvements in module performance and production cost reductions. When used in high end, double-pane thermally insulating windows, we anticipate an average energy payback period of 2 to 6 years, depending on the location, window orientation and local electricity cost of the installation.

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Appendix B

Surface Passivation of InP Using an Organic Thin Film

We demonstrate the surface passivation of InP using thin layers of a perylenetetracarboxylic diimide derivative (PTCDI-C_9) applied via organic vapor phase deposition (OVPD). The organic layer forms a conformal crystalline film on the InP surface, which is confirmed by atomic force microscope and X-ray diffraction. Area-dependent photoluminescence measurements indicate that the coating reduces surface recombination. The organic thin film deposited by OVPD exhibits improved photoconductivity compared to an unpassivated InP sample, and to a layer deposited via vacuum thermal evaporation. Our results suggest that semiconductor surface passivation using organic thin films deposited by OVPD has applications to a variety of optoelectronic devices, particularly with structures requiring sidewall or conformal coatings.

B.1 Introduction

Compound semiconductors suffer from significant surface recombination of minority carriers due to a high surface state density.[1] In this context, passivation of semiconductor surfaces can minimize surface recombination, and hence improve the performance and stability of a variety of compound semiconductor-based optoelectronic devices including photodetectors, photovoltaics and light emitting diodes.[2] Efforts have generally focused on reducing the semiconductor surface recombination velocity using various treatments with sulfides and thiols.[3] Among the many

methods, a promising approach is to coat the surface with a stable, thin-film organic layer[4,5,6] such as 3,4,9,10 perylenetetracarboxylic dianhydride (PTCDA), regioregular poly(3-hexylthiophene-2,5-diyl) (P3HT), etc. [6,7] In this work, we show that the addition of a thin layer of N,N'-dinonyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C_9) via organic vapor phase deposition (OVPD) on the surface of InP can act as a conformal, and effective passivation layer. We choose to deposit PTCDI-C_9 due to its superior surface coverage compared to many other organic molecules, along with its stability and ease of vapor phase deposition.[8,9]

B.2 OVPD growth of PTCDI-C_9 film

The OVPD process entails the volatilization of source organic materials by a hot, inert carrier gas in a hot-walled reactor. The organic is transported by the carrier to a cold substrate where the source material is physisorbed.[10] Transport within the gas-flow boundary layer near the substrate surface is diffusive, resulting in near equilibrium growth as opposed to the kinetically driven growth characteristic of vacuum thermal evaporation (VTE). As a consequence, the OVPD grown film exhibits improved crystalline order compared to films grown by VTE. Furthermore, OVPD enables the conformal coating of 3D surfaces. Provided that an appropriate passivating organic is used, this process can result in protective side-wall coverage.

Figure B.1(a) shows the molecular structural formula of PTCDI-C_9, which is synthesized according to previous procedures[11] and purified three times using gradient thermal sublimation in vacuum.[12] The PTCDI-C_9 film is grown by either OVPD or VTE. OVPD growth employed 45 sccm (standard cubic centimeters per minute) of N_2 injected into a source barrel, and 50 sccm dilution flow in the main reactor.[8] The chamber pressure during growth was 0.61 torr, and the organic source temperatures were between 280 and 290 ℃ to maintain a deposition rate of 0.2 Å/s. The VTE growth at 0.2 Å/s was performed in a chamber with a base pressure of 2×10^{-7} torr. The

substrate temperatures of 55°C and room temperature were used during OVPD and VTE growth, respectively. These temperatures were chosen to achieve deposition of extended organic crystals on the semiconductor surface. The organic films have a grain size of a few hundred nanometers when deposited by OVPD, which is at least ten times of that when grown by VTE, as shown in Fig. B.1(b). Both growth methods show a Stransky-Krastanov growth mode that forms a monolayer thick wetting layer topped by islands a few monolayers thick.[13] Both the wetting layer and islands show a total height of 2.2 ± 0.1 nm. Figure B.1(c) shows the morphologies of 1 nm, 2 nm 3 nm and 4 nm thick PTCDI-C_9 films grown by OVPD that shows a large grain size. Also apparent is the smaller grain size of VTE grown films. These images also indicate the coating is only a few monolayer thick with nearly complete surface coverage via the wetting layer.

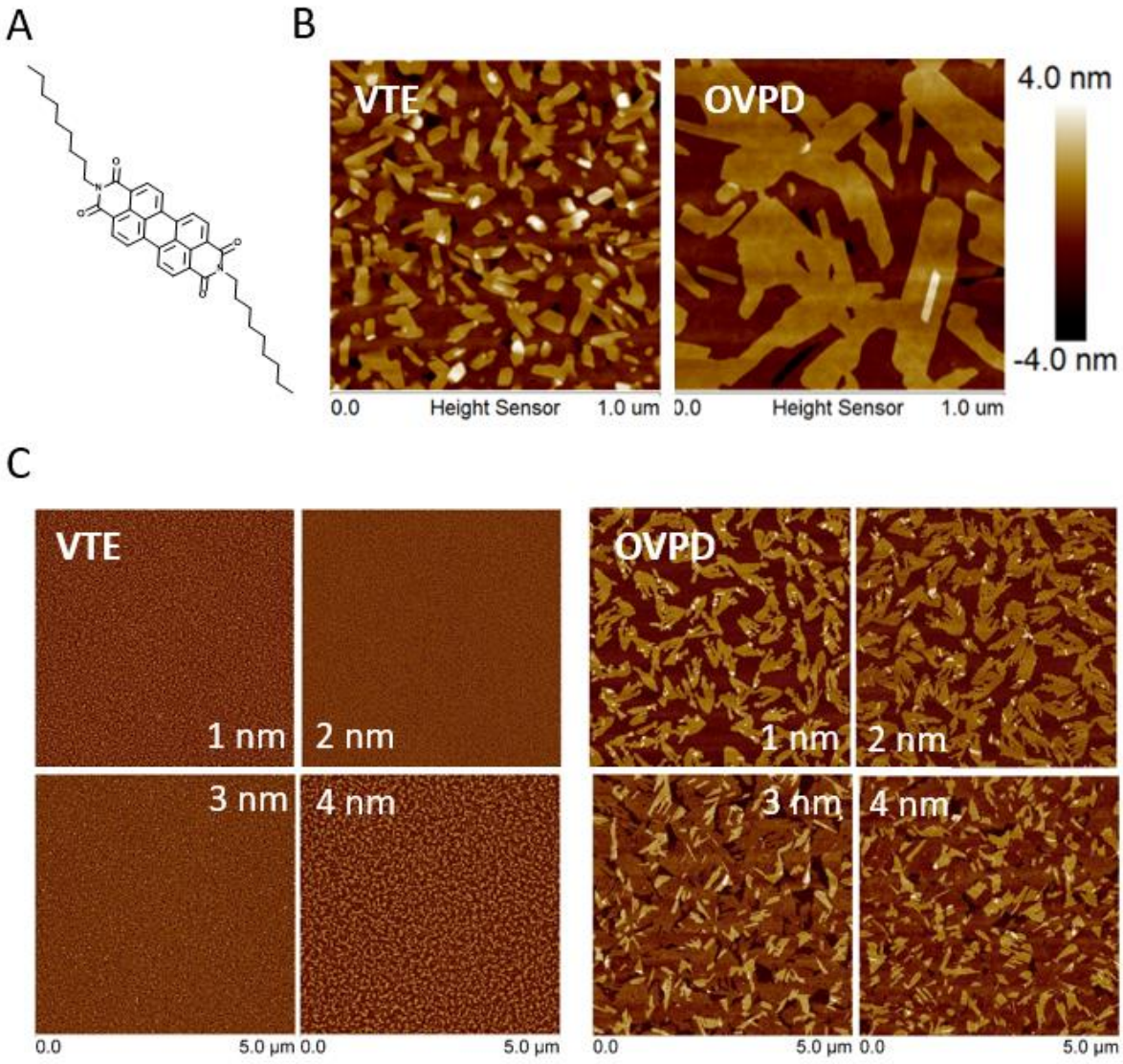

Figure B.1 : OVPD growth of PTCDI-C_9
(a) Molecular structural formula and (b) atomic force microscope image of PTCDI-C_9 film grown by (right) organic vapor phase deposition (OVPD) and (left) vacuum thermal evaporation (VTE). (c) Thickness dependent morphology of PTCDI-C_9 films grown by (right) OVPD and (left) VTE.

X-ray diffraction (XRD) patterns of 100nm OVPD or VTE grown layers on sapphire substrates are shown in Fig. B.2. Ex-situ variable angle spectroscopic ellipsometry was used to determine the layer thicknesses. In Fig. B.2, we find the PTCDI-C_9 film grown by VTE shows single diffraction peak at $2\theta = 4.20 \pm 0.03°$, corresponding to an interlayer spacing of molecules that stand upright on the surface of 20.8 ± 0.1 Å.[14] In contrast, OVPD grown films exhibits significantly enhanced (001) peak intensity and an additional (002) peak at 8.4 ± 0.03^{o}, showing an

improved crystallinity. The low intensity of the (001) peak of VTE grown films is consistent with the AFM measurement images that show a smaller grain size, which can potentially lead to higher disorder. Moreover, the full width half maxima (FWHM) of the (001) peak is larger for the VTE-grown sample (FWHM =0.35±0.02°) than the OVPD-grown sample (FWHM = 0.30±0.02°). Using Scherrer analysis, the difference in FWHM indicates that the OVPD-grown samples have slightly larger out of plane domain size[15] of 26±2 nm, compared to 22±1 nm for VTE-grown samples.

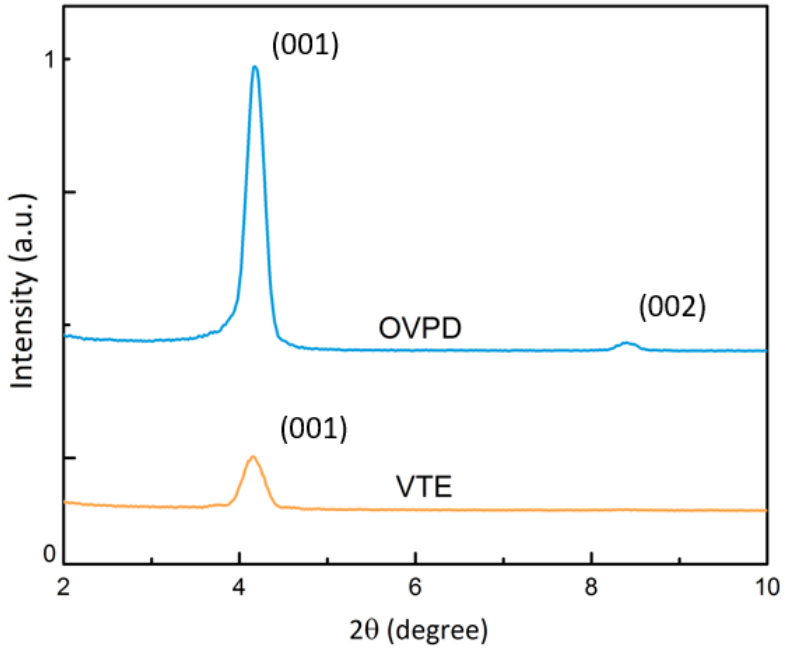

Figure B.2 : X-ray diffraction patterns of PTCDI-C_9 films

B.3 Photoluminescence of PTCDI-C_9 passivated InP

A PTCDI-C_9 film was grown on an InP epitaxial layer by OVPD or VTE to further investigate its passivating characteristics. A 2 μm thick, 3×10^{16} cm^3 Be-doped InP epitaxial layer is grown at 480°C by gas source molecular beam epitaxy (GSMBE) on a (100) S-doped InP substrate. Following growth, the native InP surface oxide layer is removed by immersion in

buffered hydrofluoric acid (BHF) for 1 min. A 4 nm thick PTCDI-C_9 layer is then grown on the surface. Figure B.3(a) shows measured photoluminescence (PL) spectra of samples excited with emission from a 633 nm wavelength diode laser. The emission at the band edge of InP at 925 nm shows increased PL intensity due to reduced non-radiative recombination for surfaces covered by the organic layer, possibly a result of holes injected from the PTCDI-C_9 film filling the surface and near-surface traps.[6] Furthermore, InP with PTCDI-C_9 grown by OVPD provides 1.5 and 3-fold increased PL emission over InP with a bare surface, and with PTCDI-C_9 deposited by VTE, respectively. To determine the stability of the passivated surface, PL measurement of the InP with an OVPD deposited film was taken every 3 days after the deposition, for a total of 15 days. The sample was kept under low pressure of 10^{-2} torr to simulate conditions of low oxygen and moisture contact. Figure B.3(b) shows the integrated PL intensity, which is proportional the surface recombination velocity, normalized to the first day of measurement. No physical delamination of the film or degradation in PL intensity was observed, indicating a stabilized surface. We expect

the passivated surface to be air stable via overcoating the organic/InP surface with a barrier such as parylene.[16]

B.4 Effect of conformal coating of OVPD growth on passivation

Coating by OVPD is conformal, thereby permitting side-wall coverage in devices with 3D surfaces. Recombination at exposed (011) surfaces is considerable. To determine if such surfaces can be passivated by an organic coating, therefore, the dependence of the PL intensity on InP mesas with sizes ranging from 400 μm × 400 μm to 1 mm × 1 mm, was measured. The mesas, employing the same epitaxial structure as above, were patterned using photolithography and wet etching ($HCl:H_3PO_4$, 3:1 ratio). The PL intensities of the InP mesas coated with PTCDI-C_9 by VTE shows a 49% reduction in PL intensity from 1 mm^2 to 0.16 mm^2 mesas (see Fig. B.4). On the

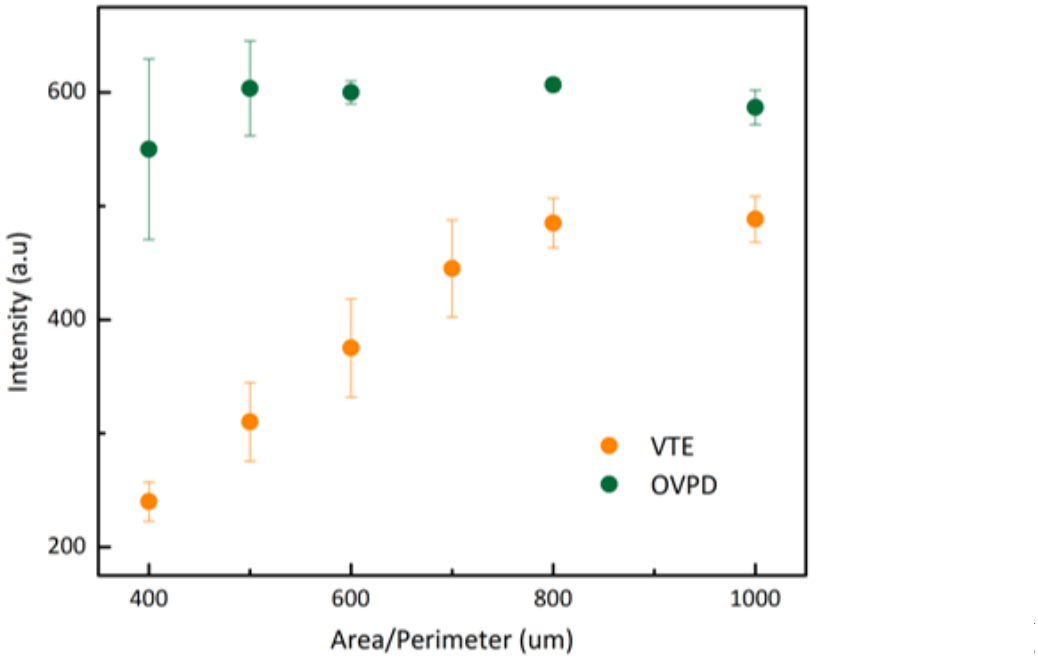

Figure B.4 : Dependence of the PL intensity on the area/perimeter ratio of mesas on p-InP epitaxial layer coated with PTCDI-C_9 film grown by VTE and OVPD.

other hand, the same structure coated using OVPD exhibits a nearly constant PL intensity with area. From these results, we infer that the surface recombination for OVPD coated InP surfaces is reduced compared to those sidewall surfaces coated by VTE.

B.5 InP photoconductor with PTCDI-C_9 passivation

Finally, the organic coating is applied onto the surface of an Fe-doped (semi-insulating) InP photoconductor.[17] The as-received (100) Fe doped InP substrate (AXT, Inc., CA 94538) was immersed in BHF for 1 min to remove the residual surface oxide. Then, a 5 nm thick Ti/300nm Au contact layer was deposited by e-beam evaporation, and patterned using photolithography. After the patterning, ohmic contacts were formed by rapid thermal annealing at 350 ℃ for 1 min in air. The channel width and length of photoconductor is 100 um and 7000 um, respectively (see inset, Fig. B.5). The surface oxide was once more removed by BHF, and a 4 nm thick PTCDI-C_9 layer was deposited on InP via VTE or OVPD. The current–voltage characteristics of bare InP, VTE-passivated, and OVPD-passivated InP photoconductors were measured in the dark and under 100 mW/cm^2 intensity illumination from a halogen lamp. Table B.1 shows the measured dark current at 1 V, and the photoconductivity for the three different surface preparations. The photoconductor coated by the organic layer shows a slight or no increase in dark current (I_D) at 1 V compared to bare InP-based photoconductor, with I_D = 19.5 ± 0.5 nA, for all three samples. In contrast, the photoconductivity increased from 6.81 ± 0.05 $\times 10^{-6}$ S for the bare InP photoconductor to 7.35 ± 0.02 $\times 10^{-6}$ S and 1.05 ± 0.03 $\times 10^{-5}$ S for VTE and OVPD deposited samples, respectively. Figure B.5 shows the photocurrent of the Fe-doped InP photoconductor with and without the organic coating. This observation confirms the improved surface passivation of the InP surface using films grown by OVPD compared with VTE.

Table B.1 : Electrical characteristics of InP photoconductors

Passivation	Dark current at 1V (nA)	Photoconductivity (x10^5 S)
Bare InP	19 ± 0.4	0.68 ± 0.01
VTE	19 ± 0.6	0.74 ± 0.05
OVPD	20 ± 0.5	1.05 ± 0.03

with and without passivation, in the dark and under 100 mW/cm^2 white light illumination.

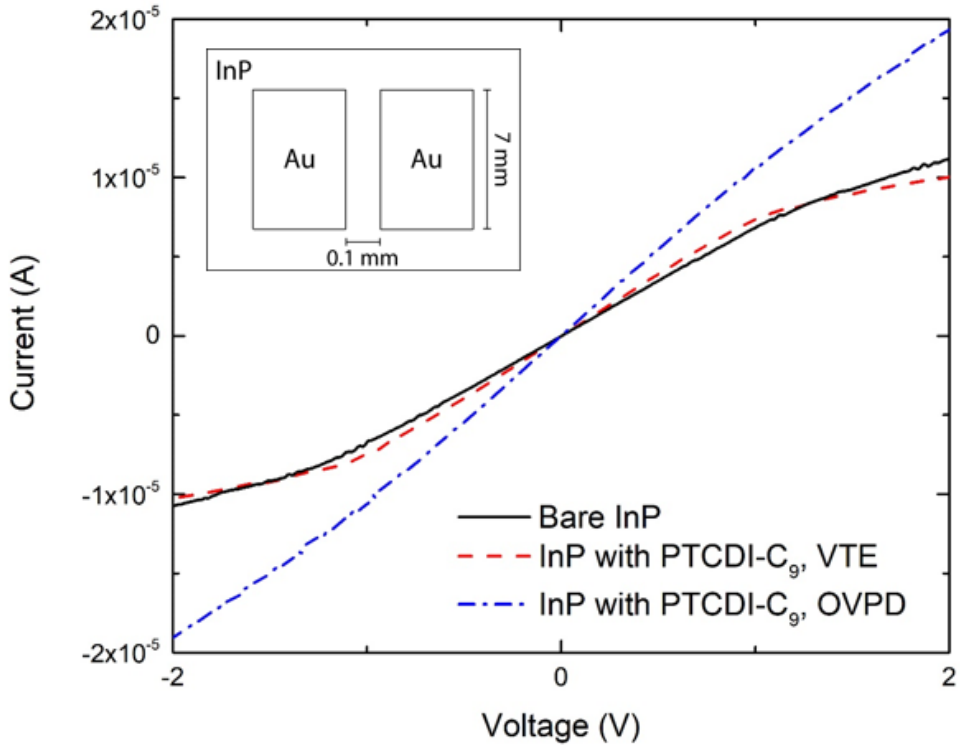

Figure B.5 : Current-voltage characteristic of Fe-doped InP photoconductors
Without passivation, and coated with PTCDI-C_9 using VTE or OVPD. The device was tested under illumination from a 100 mW/cm^2 halogen lamp. *Inset*: Plan view of the InP photoconductor.

B.6 Conclusion

In summary, we demonstrate an effective method for passivating III-V semiconductor surfaces by growing monolayer thick organic films via OVPD. We found that 4 nm thick PTCDI-C_9 give full InP surface coverage, even on 3D structured surfaces. AFM and XRD measurements

indicate that the morphology and crystallinity of OVPD grown organic films is improved compared to those deposited by VTE. The larger PL intensity indicates the reduced surface recombination when the InP surface is coated by the organic layer. Finally, organic passivation is applied to the surface of an InP photoconductor, improving its photoresponse. This is also attributed to a reduced surface recombination compared with untreated surfaces. Our results demonstrate a means for conformal coating of inorganic surfaces by OVPD as an effective method for improving the surfaces of InP and potentially other III-V semiconductor surfaces. This technology has potential for various optoelectronic devices such as light emitting diodes, photodiodes and transistors.

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