# W-BAND THREE-DIMENSIONAL INTEGRATED CIRCUITS UTILIZING SILICON MICROMACHINING

by

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To my father,

Donald F. Herrick

and my mother,

Sandra K. Blair

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# PREFACE

This thesis presents several low-loss micromachined W-band circuit components suitable for integration in a multi-layer silicon environment. Some of these components are micromachined finite ground coplanar waveguides, micromachined circuit combining networks, through-wafer vertical interconnects, and wafer-to-wafer vertical interconnects. In addition, this thesis also includes implementation of these novel architectures into the first 94 GHz micromachined silicon multi-layer transmit module. This transmit module is not only a high-density multi-layer circuit, but an integrated conformal package utilizing thermocompression bonding. The multi-layer silicon environment, with appropriate design and packaging, can provide a solution to the low power problems of conventional monolithic microwave integrated circuits (MMICs) by providing more power per unit area. Although this research effort includes a large fabrication effort, the work is presented with equal weighting on design, simulation, fabrication, and measurement. The strong technology base established through this project forms a legacy for future technology maturation and may also be applied at lower frequencies.

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# CHAPTER 1

# INTRODUCTION

## 1.1 Motivation

### 1.1.1 Current Integrated Circuit Applications

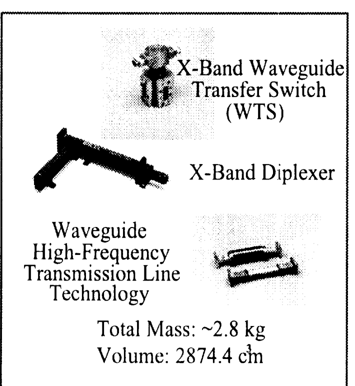



Figure 1.1: Traditional waveguide components for satellite communications at X-band (8-12 GHz).

Today's microwave and millimeter-wave markets are driving three important metrics: low cost, high performance, and small size. This, in turn, dictates the replacement of traditional waveguide components, which are massive and costly but extremely low loss, with smaller semiconductor products. Figure 1.1 shows traditional waveguide components for an X-band satellite communications application. Solid state device technology has driven the development of planar Monolithic Microwave Integrated Circuits (MMICs) that dominate todays communications systems. This technology has allowed for the design of small radio

frequency (RF) circuits that combine many functions on a single circuit while providing high performance and low cost. Spacecraft communications systems have benefited from these advances as applied to microelectronics and VLSI (Very Large Scale Integration), and have experienced steady decreases in both cost and weight. During the past two decades, the level of integration, available materials, batch-production yields, reliability, and raw performance of high-frequency and high-speed components have steadily increased. Consequently, many frequency and speed requirements previously met with large volume and/or weight components are now achievable with miniature, lightweight, and highly reliable devices.

The semiconductor industry has been providing integrated circuits (ICs) in standard packages for more than twenty-five years. However, it has become clear that the performance advantages inherent in VLSI semiconductor devices will not be realized at the system level with conventional packaging [32]. Consequently, many new packaging technologies have evolved at the chip-level, such as ball grid arrays which combine a dense areas of contacts with a chip surface mount, and multi-chip modules (MCMs), which integrate chip packaging. Originally, multichip modules allowed bare chip attachment to a printed circuit board substrate using wire bonding, tape automated bonding (TAB), or flip chip, and eliminated individual packaging and the associated parasitics. Today a MCM substrate may be ceramic, thin films over silicon (also known as high-density integration (HDI)), or printed wiring board and may include interconnects as well a multiple chips. An example of this is the Deutche Aerospace T/R MCM radar module shown in Figure 1.2 [32]. This 20 GHz radar module has been fabricated on ceramic substrates using thin film technology for the fabrication of microstrip planar transmission lines.

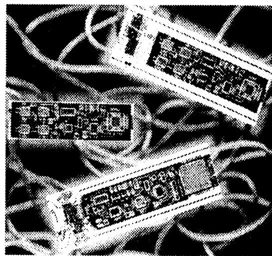


Figure 1.2: Deutche Aerospace T/R MCM radar module [81, 32].

Despite these advances, the development of MCM technology has clearly demonstrated the difficulty in realizing high power systems in monolithic form. The main reasons for this power limitation are low power MMIC devices, high-loss interconnects and passive components, low-efficiency planar antennas, and limited integration capability. The need to develop microwave monolithic circuits with high-power and low-cost leads to the following requirements for optimum high-frequency performance: lightweight hardware, high-density interconnect technology, high reliability, and advanced packaging. The development of high-power microwave circuits with both small size and low cost poses serious challenges. The response to this challenge is to use novel concepts in circuit design, fabrication, and implementation to establish significant new benchmarks in power output.

### 1.1.2 Future Integrated Circuit Applications

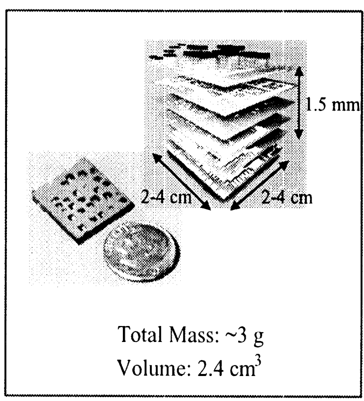



Figure 1.3: Silicon multi-layer future technology.

The next step beyond the current state-of-the art for the presently used multichip module (MCM) is the development of a technology which can provide monolithic integration of Si (or SiGe) circuits, advanced micro-electromechanical (MEMS) devices, micromachined analog components (e.g. filter/multiplexers), and digital CMOS based processing circuits into one wafer or multi-wafer stack. Additionally, if tens of watts of radiated power can be economically produced, applications such as moderate range adverse weather radars, weapon seakers, and tactical data links can be greatly enhanced in effectiveness and capability.

One way to meet the required metrics for both the microwave market and the semiconductor industry is a multi-layer approach as shown in Figure 1.3. By replacing single chips, MCMs, and/or wafers with three-dimensional integration, substantial size and weight reductions may be achieved [3]. For example, a four chip stack requires less printed circuit board real estate as compared to four adjacent chips, improving substrate efficiency. With regard to power, a multi-wafer stack can provide more power per unit area than a single wafer in which sources and interconnects are on the same lateral plane. Additionally, delay refers to the amount of time required for a signal to travel between functional blocks on a circuit, and is directly linked to interconnect length. Reducing the interconnect length through three-dimensional integration also improves performance. The magnitude of these various benefits depends on the vertical interconnect and three-dimensional packaging.

When conventional planar transmission lines such as microstrip and coplanar waveguide are tested in a three-dimensional environment, their performance may be degraded at higher frequencies due to parasitic radiation and coupling, as well as parasitics from metallized packages or carriers. To avoid these parasitic mechanisms, novel low-loss transmission line designs are required. Thus there is a need for innovative transmission lines on high-resistivity silicon appropriate for RF applications operating at frequencies increasing toward the millimeter-wave regime. Furthermore, investigation and development of packaging and low-loss vertical interconnects is needed for use in three-dimensional vertically integrated circuits. The development of a multi-layer silicon module using these novel transmission lines and interconnects will provide more power per unit area thus increasing the overall power capability of future MMICs, while decreasing volume and cost.

## 1.2 Subject Overview

The work presented in this thesis has been performed iteratively with four stages: design, simulation, fabrication, and measurement. This brief overview is meant to explain the ubiquitous characteristics of each stage. For example, the design stage involves the choice of substrate, frequency, and numerical simulator. The fabrication stage involves silicon micromachining and integrated circuit processing, while the measurement stage involves the

choice of calibration and equipment. Although more rigorous explanations can be found in the literature [50, 90, 65], the following subsections provide background to the fundamental choices made in this research effort.

### 1.2.1 High Frequencies

Modern millimeter-wave communication systems use both MMIC and waveguide components in a hybrid form for optimal performance. However, when appropriate, MMICs are widely used in communication and radar systems due to their many advantages over other conventional waveguide technologies. Some of these advantages include small size and weight, improved reliability and reproducibility, low fabrication cost, and broadband operation. Reduced size and weight are particularly important, as they translate to reduced overall cost. Wavelength dictates the size of MMIC circuits, consequently higher and higher operating frequencies are required for minimal circuit size.

Although higher frequencies have historically been used for military systems and space applications, many commercial applications have emerged. Some of these include, but are not limited to, collision avoidance radar [71, 95, 14], wireless local-area networks (LANs) [106], radio astronomy [36], and microwave sensor systems.

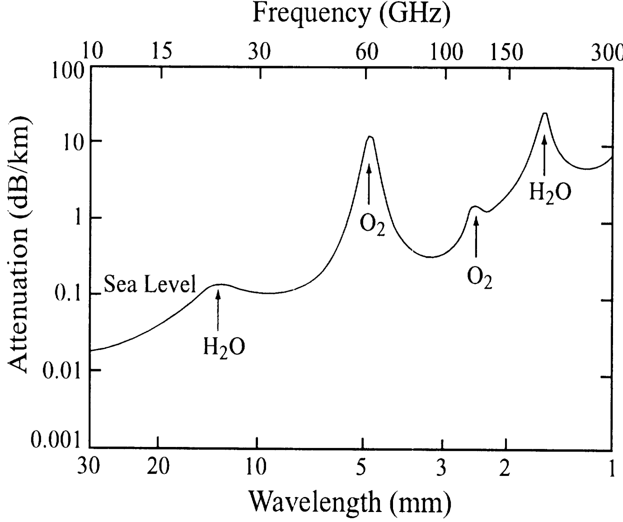



Figure 1.4: Average atmospheric absorption as a function of frequency and wavelength [7].

For communication applications designed to transmit signals through the earths at-

mosphere, atmospheric absorption is a significant factor in determining the appropriate frequency range of operation. Microwaves and millimeter-waves can penetrate many atmospheric conditions such as dust, smoke, and fog, that reduce visibility conditions. Atmospheric microwave energy absorption increases with frequency, and there are several absorption peaks due to water vapor and gaseous oxygen that should be avoided [7]. However, local minima in the absorption spectrum at approximately 35 GHz, 94 GHz, 140 GHz, and 220 GHz as shown in Figure 1.4 make these frequencies an appropriate choice for secure, short-range communications. The work presented in this thesis concentrates on frequencies between 2-110 GHz, with an emphasis in the later work on 94 GHz.

### 1.2.2 Numerical Simulations

Separation of variables, series expansion, conformal mapping, and integral methods are analytical (exact) methods commonly used to solve electromagnetic problems. At low frequencies, analytic methods are well-suited for characterizing the electrical behavior of lumped element circuits and models, although they may be used as a design tool at any frequency range. As frequency increases into the microwave and millimeter-wave range, and circuit dimensions become large compared to a wavelength, distributive effects make quasi-static and full-wave analysis better suited to analyze and design microwave circuits. It is important to note that quasi-static methods assume only a single mode and do not take into account any hybrid or parasitic modes that may be associated with a quasi-TEM line. For this reason, full-wave techniques may be used to address the dispersive nature of circuits at high frequencies in addition to coupling and parasitic effects. Some popular full-wave numerical methods are finite-difference time-domain (FDTD), method of moments (MoM), finite element method (FEM), and transmission line matrix (TLM).

Numerical solutions of electromagnetic problems have developed into many successful commercial packages with the advance of computer technology and computational speed. One commonality between the techniques is the discretization of the problem space into elements, or a mesh. This is done in either time or frequency domain. Time-domain methods use an impulse stimulus, such as a Gaussian pulse, to calculate waveform evolution

Table 1.1: Examples of High Frequency Electromagnetic Simulation Software

| Software | Vendor | Type | Used in Dissertation |
|---|---|---|---|
| HFSS | Ansoft[4] | FEM | yes |
| HFSS | HP[21] | FEM | yes |
| Maxwell (2-D) | HP[5] | FEM | yes |
| FullWave | Infolytica[53] | FEM | no |
| Opera/Soprano | VectorFields[112] | FEM | no |
| IE3D(2.5-D) | Zeland[132] | MoM | yes |
| NEC-Win | Nittany[80] | MoM | no |
| Fidelity | Zeland[132] | FDTD | no |
| XFDTD | Remcom[91] | FDTD | no |
| Micros-Stripes | Sonnet[102] | TLM | no |
| Simian(2-D) | [108, 62] | Ribbon Method | yes |

by stepping in time. Frequency-domain methods, such as Finite Element (FE), iteratively solve for a single frequency point through matrix inversion and may then be swept over a frequency range. Experience has shown that the type of simulator chosen highly depends on the specific problem to be solved. There is also a compromise between accuracy and mesh size, since it is desirable to use a mesh which is fine enough to obtain an accurate field solution but not so fine that it overwhelms computational memory and/or processing power. Most simulators are based on solving Maxwell's equations in differential or integral form to obtain the electric and magnetic fields, from which S-parameters, impedance, capacitances, etc., can be calculated. Table 1.1 gives examples of some of the current high frequency electromagnetic simulators commercial available. Additional information may be obtained from [97, 113]. The predominant solvers used in this research effort are HFSS [4], IE3D [132], Maxwell2D [5], and Simian [62, 108].

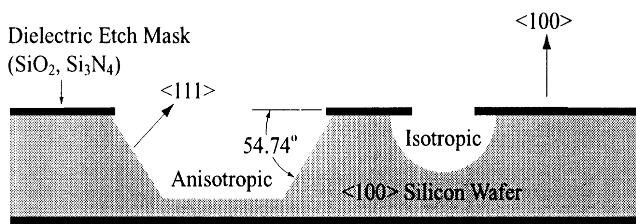



Figure 1.5: Cross-section of micromachined Si wafer.

### 1.2.3 Silicon as a Substrate

Early transistors were made of germanium (Ge), but today most circuits are made out of Silicon (Si), Indium Phosphide (InP), and Gallium Arsenide (GaAs). Although GaAs has a higher electron mobility than Si, it also has severe limitations including low hole mobility, less stability during thermal processing, a poor thermal oxide, much higher defect densities, and high cost. Si has therefore become the substrate of choice for highly integrated circuits, and GaAs is reserved for circuits that operate at very high speeds but with low to moderate levels of integration.

One salient feature of silicon, highly utilized in this work, is its ability to be micromachined, or chemically sculpted [65]. Micromachining techniques originated in the 1960's with the first Si piezoresistive diaphrams developed by Tuft *et al.* at Honeywell in 1962. In 1972, Sensym/National Semiconductor was the first to make independent Si sensor products. Other micromachined mechanical and electrical structures were explored throughout the 1970's and 1980's including thermal print heads (Texas Instruments 1977), thermally isolated diode detectors (Hewlett Packard 1980), and ink jet nozzle arrays (IBM 1977).

Wet bulk micromachining is the most popular and best-characterized micromachining method today. It can be defined as the wet etching of three-dimensional features into the bulk of crystalline or noncrystalline materials. This is in contrast to surface micromachined features, which are built up on the surface of a substrate. This sculpting, as applied to single crystal Si, can be made by using either orientation-dependent (anisotropic) or orientation-independent (isotropic) etchants, as shown in Figure 1.5. Table 1.2 shows characteristics of three commonly used anisotropic wet etchants: ethylenediamine pyrocatechol (EDP), potassium hydroxide (KOH), and tetramethyl ammonium hydroxide (TMAH) [85, 104,

Table 1.2: Wet etchants for Si bulk micromachining.

| Etchant | Composition | Temp (°C) | Si Etch Rate (μm/hr) | Selectivity <100>/<111> | Masking films (etch rate (Angstroms/min)) | Safety |
|---|---|---|---|---|---|---|
| EDP | Ethylene Diamene 150ml<br>Pyrazine 0.9g<br>Catechol 48g<br>DI water 48ml | 110 | 80 | 35 | $SiO_2$ (2-5)<br>$Si_3N_4$ (1) | Toxic |
| KOH | KOH pellets, 300g<br>DI water, 600 ml | 65 | 30 | 400 | $SiO_2$ (14-24)<br>$Si_3N_4$ (not attacked) | Safe |
| TMAH | TMAH, 25 wt. % | 85 | 35 | 12.5 | $SiO_2$ (5)<br>$Si_3N_4$ (1) | Safe |

105, 130, 1, 65]. Note that selectivity is a measure of lateral undercut, with KOH providing the least amount of undercut and TMAH providing the most. Etchant age, composition, and temperature can alter etch rates and data in the table represent typical experimentally observed values. Note plasma assisted techniques, like reactive ion etching, may also be used for dry micromachining.

Silicon micromachining has been applied to microwave and millimeter wave circuits in many ways since its introduction in the late 1980's. Silicon micromachined, dielectric membrane supported structures such as antennas, transmission lines, and filters, have shown improved performance and have extended the operating range of planar circuits to W-band frequencies and beyond [20, 58, 65, 122, 31]. New concepts in integrated conformal packaging have been introduced, leading the way for micromachining to impact planar microwave circuits beyond the component level and into the system integration area. Micromachining now has the potential to revolutionize the microwave field by offering new techniques that can be used to integrate entire systems onto a single integrated circuit (IC). This work examines Si wet bulk micromachining as applied to lower loss planar transmission lines and multi-layer system integration techniques for ICs.

### 1.2.4 Integrated Circuit Processing

In addition to Si micromachining, there are many basic steps to building an IC, including thin film deposition, wet and dry etching, and photolithography. Although there are

many excellent sources of information on IC fabrication, the heavy level of processing to be presented benefits from a general overview of the basic processes utilized herein. Specific fabrication processes for this work are included in the Appendix C.

Thin film deposition includes deposition of metals and insulators, with the three main methods being physical vapor deposition, electro-plating, and chemical vapor deposition. Under the category of physical vapor deposition, thermal evaporation and sputtering are used in this work. Thermal evaporation is the sublimation of a heated material (Cr, Au, Ti, Al, Ni, etc.) onto a substrate under vacuum. During sputtering, a material (Ta, Au, Ni etc.) at a high negative potential is bombarded with positive argon ions created in a plasma. This material is sputtered away and ejected surface atoms are deposited onto the substrate, allowing for more conformal sample coverage than may be achieved with thermal evaporation. For example, $Ta_2N$, used for thin film resistors, is formed by reactively sputtering Ta in an argon (90%) nitrogen (10%) plasma. Electro-plating is the electrodeposition of metal (Au) onto a surface via chemical changes by the passage of current through an electrolytic solution. This process is used to form thicker conductive layers, as the limiting thickness of evaporated metallic films is on the order of 1 $\mu$m.

Chemical vapor deposition (CVD) is used to deposit thin films, such as $SiO_2$ and $Si_3N_4$, onto wafer surfaces through the reaction of vapor phase chemicals that contain the required thin film constituents. In plasma-enhanced CVD (PECVD), a glow discharge (or plasma) is generated by applying an RF field to a low pressure gas, creating free electrons in the discharge region. Having gained sufficient energy from the electric field, the electrons collide with gas molecules initiating gas-phase dissociation and ionization of the reactant gases. Although LPCVD (800-1250 °C) $SiO_2$ and $Si_3N_4$ are typically of better quality, PECVD has two advantages: the lower deposition temperatures (300 °C) and the ability to deposit $SiO_2$ and $Si_3N_4$ over metals.

Etching of thin films can be done using wet or dry etching techniques. Dry etching techniques involve plasma and may be conducted in either pure plasma or reactive ion etching (RIE) mode. In pure plasma mode, the ions and free radicals produced by the plasma diffuse to the electrode and wafer surfaces without biasing. In contrast, RIE uses a negative self-bias DC voltage between the plasma and wafer electrode to accelerate ions

from the plasma to the wafers. In this mode, most of the etching is accomplished with ion acceleration towards the wafer surface. This ion etching is part chemical and part physical as the ions hit the wafer surface and in doing so remove additional material. While pure plasma mode is used for wafer descumming (resist removal) and blanket removal of dielectric films ($SiO_2$,$Si_3N_4$), RIE is typically used for dielectric film patterning ($Ta_2N$, $SiO_2$, $Si_3N_4$).

Wet etching involves placing a wafer in a beaker of acidic or basic solution depending on the process at a given temperature and then rinsing in deionized (DI) water. Metallic thin films may be etched in this manner, as well as dielectric thin films, each with its specific etchant. For example, Ti and $SiO_2$ may be etched with hydrofluoric acid and DI water, while Au may be etched in Gold Etchant. As previously discussed, silicon may be wet-etched, or micromachined, using EDP, KOH, or TMAH.

Pattern transfer from masks onto thin films is accomplished through lithographic means. Standard ultraviolet (UV) photolithography is used in this work although other methods include but are not limited to X-ray, electron-beam, ion-beam, and deep UV photolithography. With standard UV photolithography, a photomask, a glass plate with a chromium absorber pattern, is placed in direct contact with a photoresist coated wafer surface, which is then exposed to UV radiation and developed in an alkaline solution. The photoresist is of liquid form and spun onto a wafer at speeds of 1-3.5 krpm resulting in micron order thicknesses. Photoresists are extremely vulnerable to environmental changes, such as humidity and temperature, and are often the source of processing problems. Thus the resolution of a photolithographic development can be limited by many parameters, including mask accuracy, UV diffraction, mechanical system stability, environmental conditions, and resist stability.

### 1.2.5 Measurement and Calibration

All circuit measurements are taken on an HP 8510C Vector Network Analyzer[1], which can be configured to measure scattering parameters from 2-110 GHz using three separate test sets. For measurements from 2-40 GHz, an 8516A S-Parameter Test Set connected

[1]Hewlett-Packard, Santa Clara, CA.

to Model 40A Picoprobes[2] via 3.5 mm coaxial cables is used for on-wafer measurements. Measurements above 40 GHz require an 85105A Millimeter Wave Controller with an additional test set. U-Band measurements, for example, allow measurements from 40-60 GHz with an 83556A Mm-Wave Source Module in addition to directional couplers and harmonic mixers to convert the measured signals to the 1.2 MHz baseband of the 85105A. On-wafer measurements with the U-band test set also require Model 67A Picoprobes connected to 1.89 mm coaxial cables, WR-19 to 1.89 mm coax adaptors, and finally to the WR-19 output of the U-band test set. The W-band (75-110 GHz) set-up is simpler with the W85104A test set modules supplying signals through WR-10 waveguide and Model 120A-BT picoprobes for on-wafer measurements. Figure 1.6 shows a photograph of the W-band set-up. In all measurement configurations, the ground-signal-ground probe pitch is 150 $\mu$m, and is well suited to launching and receiving coplanar waveguide (CPW) type modes.

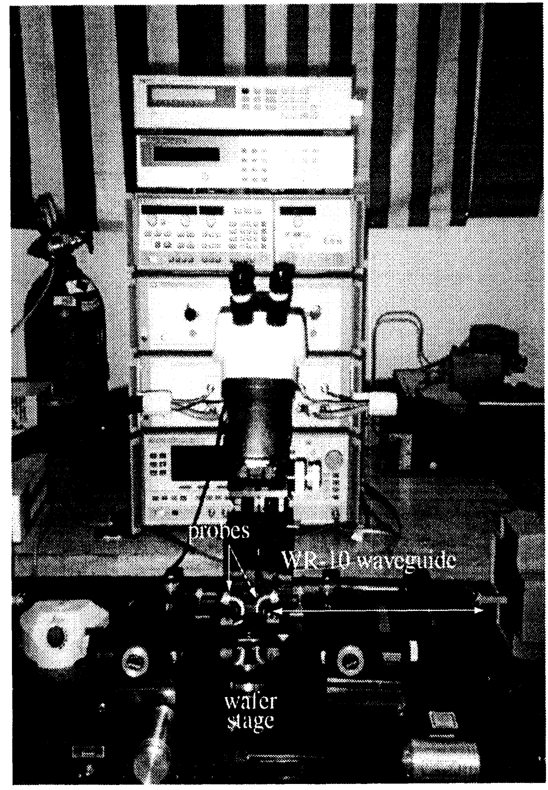
The Through-Reflect-Line (TRL) calibration has been used for all calibrations since it provides an on-wafer reference plane and uses calibration standards fabricated in conjunction with the circuits to be tested. In this way, all discontinuities and unwanted effects from the waveguides, probes, and even the transmission line itself may be de-embedded from the measurements, yielding accurate loss measurements.

TRL calibration sets for CPW lines consist of three primary lines along with longer additional lines for improved calibration. The primary basic line is the Through, whose length is not specific but should be less than a quarter wavelength. The Reflect line is typically a short for CPW and is half the length of the Through. The Line is a delay line whose length is chosen such that the phase difference between it and the Through line is between 50 and 140 degrees. An optimal length of Line is 90 degrees of insertion phase in the middle of the desired frequency span. Multiple delay lines are typically used to provide complete frequency coverage.

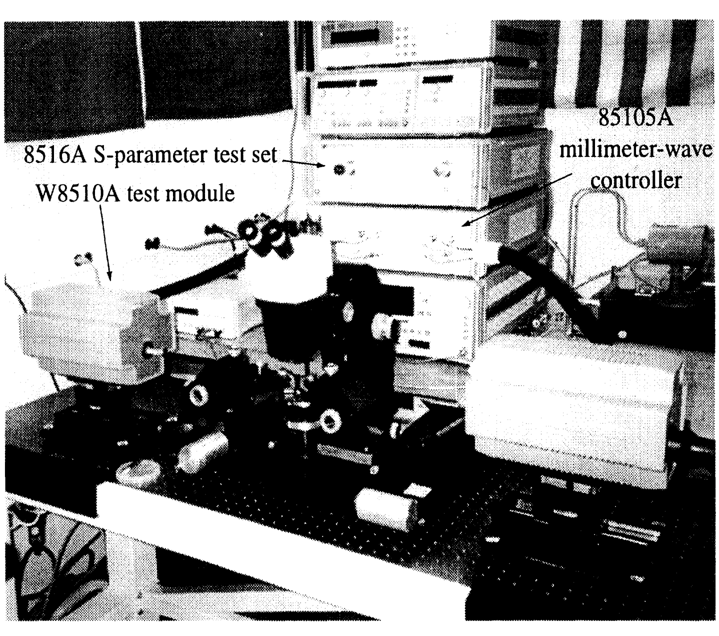
Multical, developed by NIST [70, 69, 67], is used to implement the TRL calibration by generating the best set of calibration coefficients for the network analyzer by analyzing the calibration standard measurements. Multical is also able to generate information on attenuation and relative effective permittivity.

[2]GGB Industries, Naples, FL.

Note that there are many factors that may contribute to the error margin of a particular measurement. Circuits are typically designed for a specific frequency and bandwidth. As discussed in the following section, ohmic loss varies as the $\sqrt{f}$, thus it is not appropriate to average loss values over a particular frequency range unless the insertion loss measured is quite small and broadband. Instead it is appropriate to examine the insertion loss at the design frequency and determine error from the ripple in the measurement around that frequency point or measure the same circuit repeatedly and observe the variation between measurements at the design frequency. Other factors that contribute to measurement variation are fabrication inconsistencies, such as uniform metal thickness, air bridge integrity, and thin film resistor thickness.




(a)




(b)

Figure 1.6: W-band measurement set-up.

### 1.2.6 Planar Transmission Lines: Coplanar Versus Microstrip

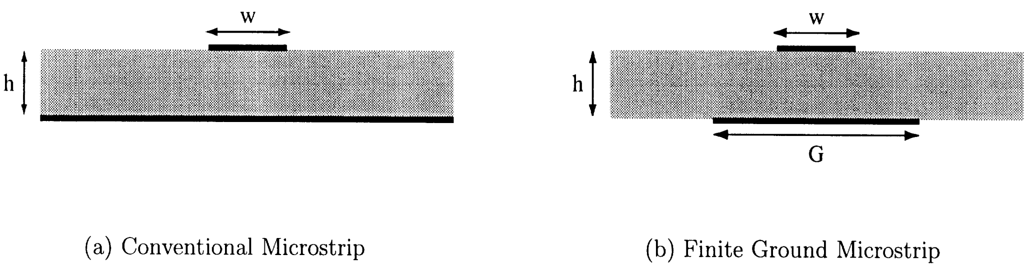
Before continuing, discussion of planar transmission line characteristics and the rational for choosing finite ground coplanar (FGC) transmission lines as the primary line architecture in this dissertation is warranted. There are several reasons for the attenuation of signals traveling through a transmission line. Of those, conductor, dielectric, and radiation losses are the most prevailing form of loss in a planar transmission structure. Conductor losses are caused by the resistive nature of the conductors that force the signal to penetrate through the conductor material. At microwave and millimeter wave frequencies current density is maximum at the surface of the conductor and decreases exponentially with depth into the conductor resulting in heat generation and power loss known as ohmic loss. The penetration depth of the current is defined as the skin depth of the line, and is a function of frequency f and the resistivity $\rho$ of the conducting material, as given by the following relationship: $\delta = \frac{1}{2\pi}\sqrt{\frac{\rho}{f\mu}}$. In the case of lossy conductors it can be shown that signal attenuation measured in dB/cm is inversely proportional to skin depth. As a result, a line of fixed physical length exhibits an ohmic loss that varies with frequency as $\sqrt{f}$. For microwave and millimeter-wave applications where physical lengths scale with frequency, ohmic loss is measured in dB per guided wavelength (dB/$\lambda_g$) and exhibits a frequency variation proportional to $\frac{1}{\sqrt{f}}$ .

In planar transmission lines, dielectric loss is introduced whenever the excited field is partially or entirely distributed inside a substrate. This is because the medium will absorb part of the transmitted energy due to the presence of polarization charges and their inability to instantaneously follow the changes in the induced electric field. The resulting loss, known as dielectric loss, if measured in dB/$\lambda_g$, shows a constant behavior independent of operating frequency. In addition to ohmic and dielectric loss, planar transmission lines operating in an open or semi-open environment may suffer from parasitic radiation that may happen either in a distributed way along the length of the line or it may be localized at discontinuities.

There are two transmission line geometries best suited for vertically-integrated interconnect networks: microstrip and coplanar waveguide. Both are popular transmission lines, primarily because they can be fabricated with photolithographic processes and can be eas-

ily integrated with other active and passive devices. Each geometry can be modified using micromachining [58, 65] to provide equivalent structures that exhibit improved electrical performance at the cost of higher fabrication complexity. In the following, advantages and disadvantages of each line are discussed, particularly with respect to signal attenuation, line size, and multilayer applications.

### Microstrip Line




(a) Conventional Microstrip

(b) Finite Ground Microstrip

Figure 1.7: Microstrip

A microstrip line is a planar waveguiding structure characterized by two conductors facing opposite sides of the dielectric substrate (see Figure 1.7(a)). In all monolithic applications the utilized microstrip geometry has a semi-infinitely large ground in order to reduce ohmic losses to a minimum. In these circuits the line characteristics are determined by the substrate thickness, the line width, and the dielectric characteristics of the substrate. While semi-infinite ground planes minimize the line loss for a given line width, they introduce new problems in packaging and circuit integration. Specifically, it has been extensively observed that lines that share the same ground experience higher coupling and require wider separations to achieve desired isolations. Also, large ground planes make vertical line integration difficult. To design lines that can transition vertically into higher or lower planes in a three-dimensional circuit, the ground has to be finite (Figure 1.7(b)) and also transition vertically with the line in a way that preserves field confinement and line characteristics. To leave the microstrip mode uninterrupted, the ground must extend approximately two substrate thicknesses to either side of the microstrip conductor edges (G = W + 4h). However, in many designs narrower ground conductor widths may be desirable in an effort to achieve

Table 1.3: 50 Ω Microstrip losses at 30 GHz. [88, 40]

| Substrate Thickness($\mu$m) | Line Width($\mu$m) | Metal Thickness($\mu$m) | Loss(dB/mm) |
|---|---|---|---|
| 2.5 (polymide) | 5 | 3 | 0.5 |
| 7 (polymide) | 34 | 3 | 0.25 |
| 500 (300 Ω-cm Si) | 420 | 8 | 0.05 |

higher line impedances. In the case of thin substrates, the center conductor of a 50 Ω line becomes very narrow and introduces additional losses as observed in MCMs and circuits that use the high-density integration (HDI) approach shown in Figure 1.8[22, 88].

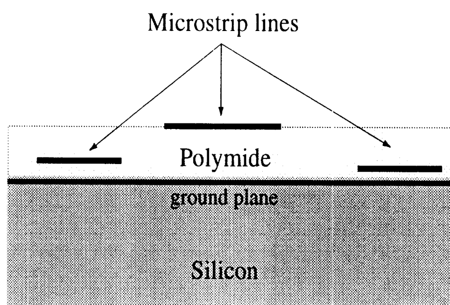



Figure 1.8: Schematic of high-density integration(HDI) as applied to microstrip.

As demonstrated by an extensive study presented in the literature [22, 88], conductor loss in microstrip lines varies inversely with the width of the line and is the dominant component when the substrate thickness becomes electrically small. This is a direct consequence of the frequency variation of each loss component and the increased current density. Table 1.3 shows the measured loss of 50 Ω microstrip lines printed on a variety of substrates operating at 30 GHz. These measured results indicate that lines suffer substantial loss when the line width reduces to a few microns.

In microstrip circuits, dielectric and radiation losses may be reduced by decreasing the substrate thickness. As mentioned earlier, the presence of the substrate increases parasitic capacitance and radiation resistance at junctions and transitions, and makes the line susceptible to radiation from these discontinuities. To reduce this radiation the line capacitance can be increased by locally reducing the substrate thickness as shown in Figure 1.9 where

lines have been printed on high-resistivity micromachined Si substrates. In Figure 1.9(a), the substrate has been removed underneath the line using anisotropic wet etching (KOH or EDP) [58, 65] to reduce the effective dielectric constant and improve TEM propagation. In Figure 1.9(b) the substrate has been removed and the etched cavity has been metallized to improve propagation efficiency. In addition to fabrication difficulties, thinner Si or GaAs substrates for the arrangement of Figure 1.9 are not recommended due to the required narrow line widths and the subsequent increase in conductor loss.

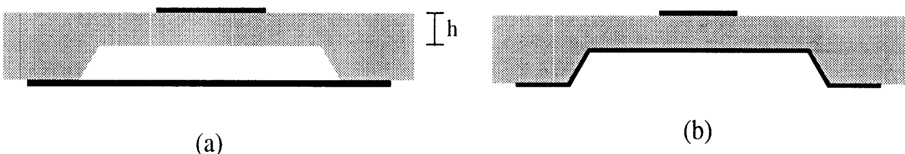



Figure 1.9: Alternative microstrip geometries ($h >= 30\mu$m)

### Membrane Microstrip

To reduce dielectric loss and parasitic capacitance, a micromachined version of the microstrip has been developed (see Figure 1.10) and extensively used in high-frequency applications including Ka-, V-, and W-band filters and broadband couplers [11, 12, 8, 20, 93]. Due to the fact that the substrate material has been removed, the exhibited loss is only of conductor type and is considerably lower than any other microstrip line. The total width of this line $W_T$ is given by the following equation [92]:

$$W_T = 5h_m + 2h_s tan(54.7) \quad (1.1)$$

where $h_m$ is the distance of the microstrip from the ground plane and $h_s$ is the lower substrate thickness as shown in the figure. In Equation 1.1, 54.7 ° is the angle of the sidewalls produced by the wet etchant as it etches selectively along the $< 111 >$ silicon crystal planes. The loss of this line has been measured up to W-band and has been found to be the lowest exhibited by a planar line in that frequency range. This loss is equal to approximately 0.05 dB/mm, or 0.5 dB/cm, at 94 GHz, which is approximately only twice

the loss exhibited by a metallic waveguide operating in the same frequency range [92].

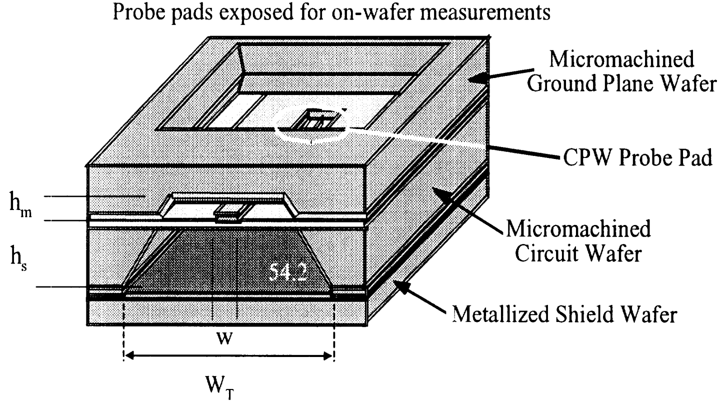



Figure 1.10: Membrane microstrip [92].

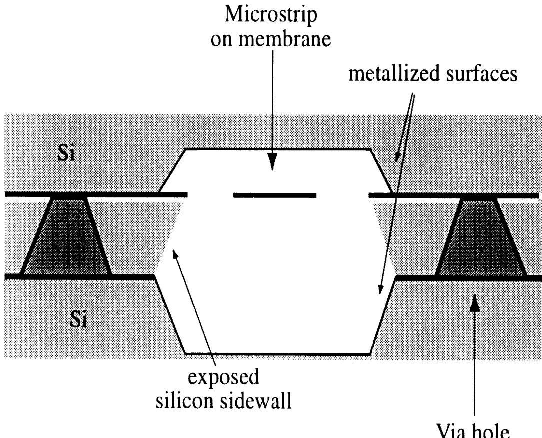
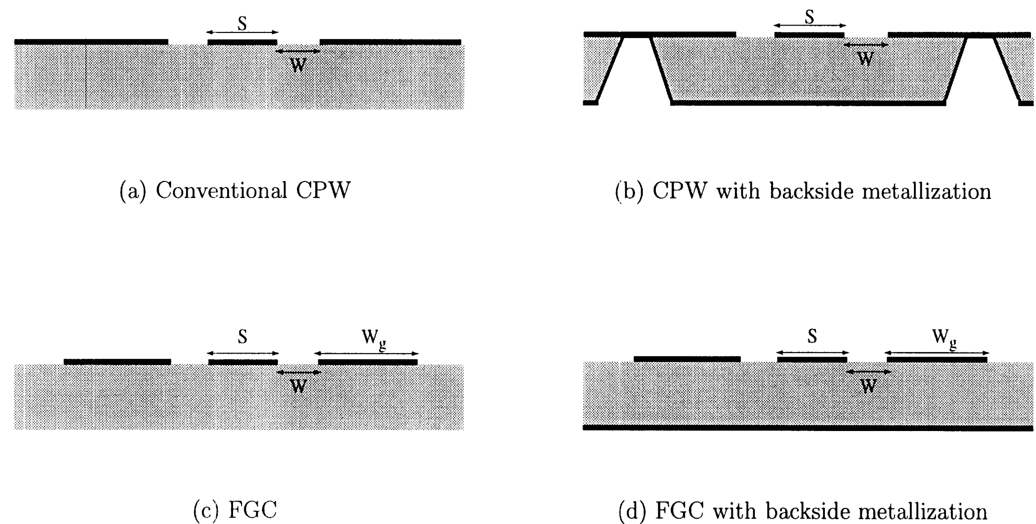



Figure 1.11: Alternative version of membrane microstrip [11].

### Finite Ground Coplanar Waveguide




(a) Conventional CPW

(b) CPW with backside metallization

(c) FGC

(d) FGC with backside metallization

Figure 1.12: Coplanar waveguide geometries.

Finite ground coplanar (FGC) waveguide (see Figure 1.12(c),1.12(d)) is a uniplanar line that exhibits favorable characteristics compared to other types of coplanar lines shown in Figures 1.12(a) and 1.12(b). The geometrical parameters important in determining characteristic impedance, dielectric constant, and losses are the ground conductor width $W_g$, aperture width W, center conductor width S, and effective dielectric constant $\epsilon_{eff}$. Design curves derived by use of a combination of static analysis and conformal mapping [89, 46] for the lines characteristic impedance and dielectric constant are shown in Figure 1.13 as a function of the aspect ratio (AR = (S/(S+2W)).

The major advantage of the FGC line (Figure 1.12(c)) is the flexibility in design, the independence from substrate thickness, and the localized field distribution. As a result, it does not require vias for ground equalization, since its propagation characteristics are not sensitive to the substrate thickness. The line also preserves its performance in the presence of back side metallization when the separation between the line and the added conductor is greater than 500 microns (see Figure 1.12(d)). The line geometry allows for control over the cut-off frequency of the higher order modes through the relation:

$$2(W_g + W) + S \leq \lambda_g/2 \tag{1.2}$$

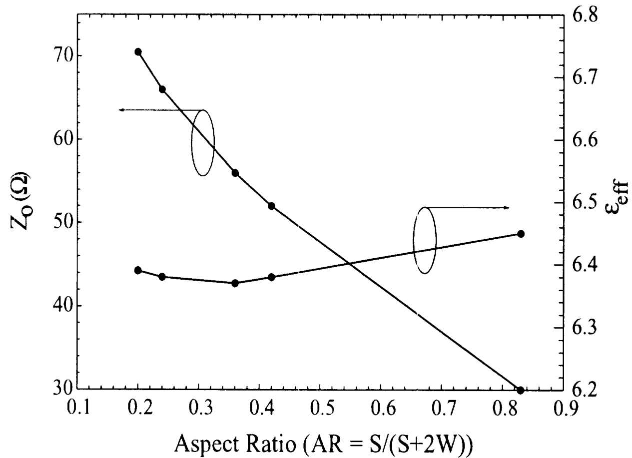



Figure 1.13: $Z_o$ and $\epsilon_{eff}$ for various FGC aspect ratios where S is the center conductor width and W is the aperture width.

When the line is designed so that it operates in the coplanar waveguide mode regime, the line attenuation as a function of frequency is mostly attributed to conductor loss. Extensive measurements performed between 10 and 110 GHz show a loss factor which in $dB/\lambda_g$ varies as $\frac{1}{\sqrt{f}}$ as shown in Figure 1.14(a) and is practically independent of the GaAs and Si substrates [9]. When the width of the ground plane becomes smaller, the loss factor starts increasing and becomes noticeable when the ground conductor width becomes less than 1.5 times the width of the center conductor. Figure 1.14(b) shows theoretical and experimental results for the loss of the FGC line for various ground plane widths [89].

The loss of the finite ground coplanar line varies inversely with the product of the aperture width and the separation. As a result, lower losses require larger line widths and lower cut-off frequencies. Figure 1.15 shows data from measurements performed on lines of different characteristic impedances using TRL calibration. These data clearly indicate a monotonic decrease of the loss with increasing product S×W. This curve by itself is not very helpful in design unless the dependency of the size of the line or of the cut-off frequency for the same product is known. The two plots in Figure 1.15 show experimentally obtained line loss at 40 GHz, line-width, and cut-off frequency versus S×W. These trends hold true for lines printed on different substrates, having different S and W, but the same S×W product.

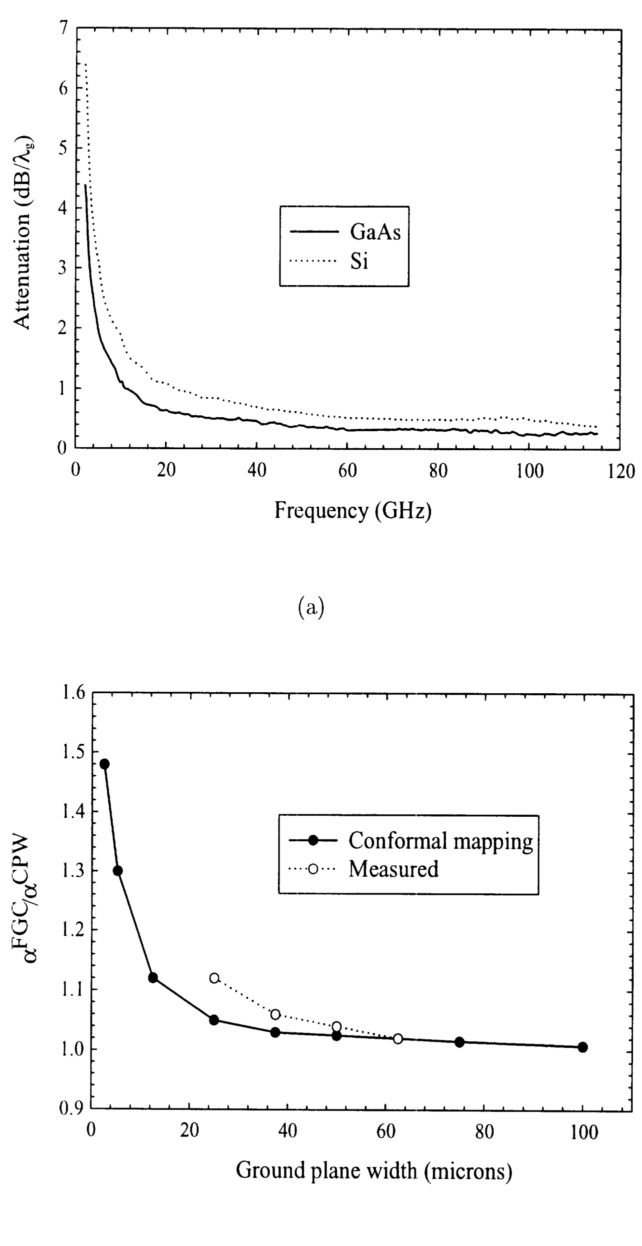



Figure 1.14: (a) Attenuation versus frequency for 50 $\Omega$ FGC line on Si and GaAs. (b) Attenuation of FGC lines with S=W=25 $\mu$m normalized to the attenuation of conventional CPW of the same dimensions versus ground plane width [89, 9].

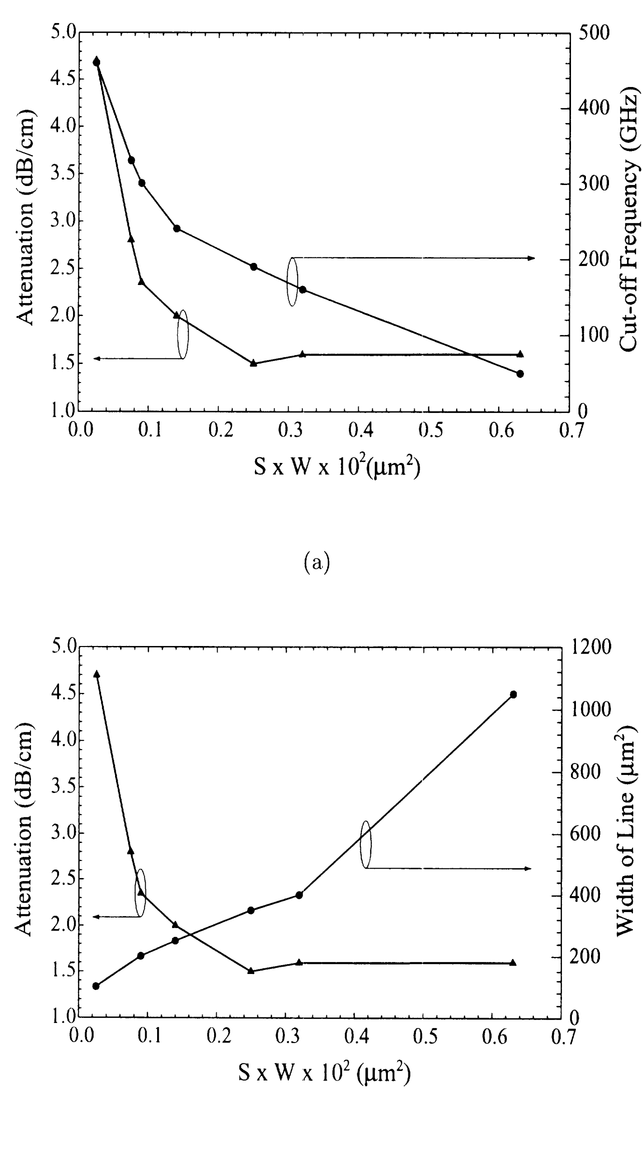



Figure 1.15: Attenuation at 40 GHz, (a) cut-off frequency, and (b) line width versus S×W. All measurements performed on silicon substrates of various thicknesses.

### Microshield FGC Lines

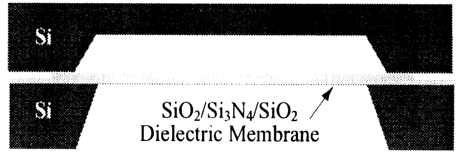



Figure 1.16: Microshield line.

Membrane-supported coplanar waveguide (Figure 1.16) has been demonstrated at frequencies from K-Band to 250 GHz, as shown by Weller [125] and Robertson [92]. The primary strengths of these structures derive from the homogeneous air dielectric, and includes broad TEM bandwidth, minimal dispersion, and zero dielectric loss.

Although this membrane line offers extremely low-loss performance, it presents some potential problems with regard to component design. The primary challenge is achieving low characteristic impedance and realizing physically compact geometries. Since the effective dielectric constant is close to one, membrane line lengths are approximately 2.5 times longer that equivalent lines on Si and GaAs. Thus distributed circuits, such as filters, require larger surface area. Additionally, large areas of micromachined silicon may affect the integrity of the wafer.

To address these issues, a new architecture for reduced size mm-wave low-pass and bandpass filters has been designed by Weller *et al.* [120], utilizing a combination of series short-end stubs and integrated metal-insular-metal (MIM) overlay capacitors. Photos and measurements of fabricated circuits can be found in Appendix D. This architecture demonstrates broad band performance and smaller size with membrane lines.

### Packaging

When microstrip and coplanar lines are printed in high-density configurations, minimizing interactions between adjacent circuits becomes extremely important. This interaction, known as crosstalk, may be due to substrate modes or parasitic coupling capacitances and results in degraded electrical performance. In high density circuits, on-wafer packaging becomes an important means of isolating circuits while preserving the integrity of perfor-

mance and the monolithic character of the circuit. With multi-layered configurations, the vertical stacking of substrates necessitates packaging and requires different designs intended for microstrip or coplanar waveguide circuits with the requirement that all conductors be of finite size. On-wafer packaging of a microstrip is more difficult to perform than that of coplanar structures simply due to the possible distances that can be achieved between the line conductors. In microstrip, the distance between the two conductors is determined by the substrate thickness, but in the coplanar waveguide the same distance is determined independently of substrate thickness, and is based on loss or line impedance requirements. To ensure package noninvasiveness, it is important to minimize the distance between the line conductors (slot apertures) and improve field confinement.

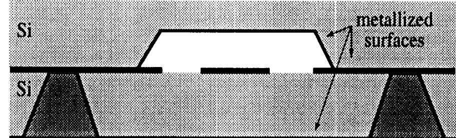



Figure 1.17: Packaged microstrip line.

If the packaging cavity is to provide electromagnetic shielding in addition to physical protection for a microstrip line, cavity surfaces must be coated with a conductive layer. In order to keep the potential of the conducting layer of the package from floating away from that of the ground conductor, resulting in additional parasitic capacitances, the ground conductors of the package should be brought to the same potential with the microstrip ground. This requires a shielding configuration in which the conducting surfaces of the cavity and the microstrip ground meet each other half-way at same level with, but on either side of, the center conductor (Figure 1.17). For high isolation requirements, silicon micromachining of the circuit can provide on-wafer packaging of a microstrip circuit that reduces electromagnetic coupling between adjacent lines to significantly low levels. Lower loss versions of the line may be accomplished by thinning the middle portion of the lower substrate or removing it completely as done for the membrane microstrip line. However, when these packaging options are considered, circuit structural integrity becomes an issue.

Packaging for finite ground coplanar (FGC) lines is easier because the ground planes and

center conductor are on the same planar surface. As a result ground equalization is achieved along the sides of the package where it interfaces with the FGC ground planes. Packaging in FGC is important for three reasons: to create an air region above the apertures and keep dielectric loss minimized, to provide a cavity for air-bridge protection, and to provide electromagnetic shielding and further reduce coupling. Adjacent FGC lines naturally have high isolation due to very good confinement in the aperture regions. It is for these reasons that the FGC line architecture is chosen for multi-layer high-density applications discussed in this dissertation.

## 1.3 Thesis Overview

This thesis presents several low-loss micromachined W-band circuit components suitable for integration in a multi-layer Si environment. Chapter 2 introduces a micromachined finite ground coplanar waveguide (FGC) design which provides up to 40% lower attenuation in W-band as compared to a conventional FGC line. Multi-layer environments require vertical interconnects thus the focus of Chapters 3 and 4 is on intrawafer and wafer-to-wafer interconnects, respectively. At 94 GHz, the loss of a micromachined 3-via intrawafer interconnect is 0.5-0.6 dB and that of a wafer-to-wafer interconnect 0.1 dB. In Chapter 5, MFGC lines are applied to circuit combining networks, showing the ability of impedance-matched interconnects to reduce loss. Lastly, in Chapter 6, the components are integrated into a 94 GHz transmit module, demonstrating successful implementation of these novel architectures as low-loss multi-layer candidates. The packaging and bonding issues associated with this multi-layer architecture are also addressed.

# CHAPTER 2

# SILICON MICROMACHINED COPLANAR WAVEGUIDES

## 2.1 Introduction

In this chapter, a new class of silicon micromachined lines and circuit components is presented for operation between 2-110 GHz. In these lines, which are of finite ground coplanar (FGC) waveguide type, silicon micromachining is used to remove the dielectric material from the aperture regions in an effort to reduce dispersion and minimize propagation loss. Measured results show significant loss reduction to levels comparing favorably with those of microshield membrane-supported lines. As a demonstration, this technology is applied to a low pass filter. Lastly, a modeling method is offered which allows design of these novel micromachined finite ground coplanar (MFGC) waveguides.

## 2.2 Motivation

As shown recently, the Finite Ground Coplanar (FGC) line, shown in Figure 2.1a, provides an alternative to conventional microstrip or coplanar waveguide for millimeter- and submillimeter-wave applications [89, 25, 127]. This line is printed on high-resistivity silicon (Si) with a thin layer of thermally grown dielectric, such as $SiO_2$ or $Si_3N_4$. After metal deposition, the $SiO_2$ or $Si_3N_4$ is removed from the line apertures to avoid dielectric losses from thin film processing contaminates. When well designed, these lines exhibit very low

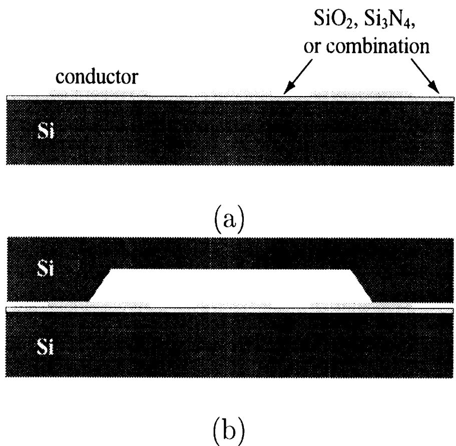



Figure 2.1: Finite Ground Coplanar Waveguide: (a) FGC on high-resistivity Si. (b) Packaged FGC.

insertion loss characteristics, but this loss depends heavily on the cross-sectional line dimensions. Fortunately, the many design parameters of coplanar waveguide allow for easier optimization of line characteristics, such as loss, and is one of the main advantages of FGC lines. They also have the ability to operate on a variety of substrates with or without backside metallization and without requiring vias for ground equalization. These characteristics have made them viable candidates for high-frequency, low-cost, high-performance circuits. Furthermore, quasi-TEM operation allows for a quasi-static modeling as already demonstrated by the agreement between measured data and LIBRAs quasi-static analysis for frequencies up to 110 GHz [103]. The exhibited low loss is responsible for the high performance exhibited by a variety of stubs and filters, designed for operation at W-band [93, 119]. Additionally, the use of FGC lines in W-band detectors has demonstrated bandwidths in excess of 30% with sensitivities as high as 3100 V/W. Furthermore, multiplier circuits based on this type of line have demonstrated increased power levels at frequencies exceeding 77 GHz [10, 9]. Despite these successes, a poorly designed FGC line may trigger leaky modes, which must be avoided by thoroughly understanding the loss mechanisms present in the FGC line and developing proper design rules [115, 99, 78, 79].

The study of FGC lines on high dielectric constant substrates, such as silicon, has demonstrated that line loss, in dB/$\lambda_g$, is dominated by frequency-dependent ohmic loss

| Structure | Measured Freq Range Attenuation | Advantages | Disadvantages |
|---|---|---|---|
| Si SiO$_2$/ Si$_3$N$_4$/SiO$_2$ Dielectric Membrane<br>Microshield<br>T.M. Weller et. al., 1993 IEEE MTT-S<br>(a) | Measured 0-110 GHz<br>Etched<br>0.4 dB/cm @ 20 GHz<br>Unetched<br>1.0 dB/cm @ 20 GHz | Extremely low loss | Backside processing<br>Requires larger circuit area<br>Complicates circuit layout |
| 2.6 μm GaAs<br>CPW with elevated 150 μm long air-bridge center conductor<br>F. Schnieder et. al., 1996 IEEE Guided Wave Letters<br>(b) | Measured 0-40 GHz<br>Airbridge CPW<br>1.4 dB/cm @ 20 GHz<br>Conventional<br>2.5 dB/cm @ 20 GHz | No wet-etching<br>Frontsided processing | Airbridge processing<br>Possible mechanical instability<br>More difficult to design |
| Glass low-ρ Si<br>Micromachined CPW for CMOS<br>V. Milanovic et. al., 1997 IEEE MTT Journal<br>(c) | Measured 0-40 GHz<br>Etched<br>3 dB/cm @ 20 GHz<br>Unetched<br>25 dB/cm @ 20 GHz | CMOS compatible<br>Frontsided processing | Complex Fabrication<br>(glass cuts and 2 wet-etching steps)<br>Metal layers fully encapsulated in glass<br>Substrate thickness limited |
| CF$_4$ Plasma RIE Aluminum 1000 Ω/cm Si<br>Trenched CPW<br>Z.R. Hu et. al., 1997 IEEE MTT-S<br>(d) | Measured 0-40 GHz<br>Etched<br>3 dB/cm @ 20 GHz<br>Unetched<br>3.6 dB/cm @ 20 GHz | Simple fabrication<br>Frontsided processing<br>Structural integrity uncompromised | Shallow trench (13 μm deep)<br>Slow etch time (1.5 μm/hr)<br>Only vertical sidewalls<br>Difficult to etch under conductor |
| Gold hi-ρ Si<br>Micromachined Finite Ground Coplanar Waveguide<br>K.J. Herrick et. al., 1997 IEEE MTT-S<br>(e) | Measured 0-110 GHz<br>Etched<br>1.0 dB/cm @ 20 GHz<br>Unetched<br>1.7 dB/cm @ 20 GHz | Simple fabrication<br>Frontsided processing<br>Structural integrity uncompromised<br>Able to adjust undercut<br>Faster etch time (35-70 μm/hr) | Wet-etching |

Figure 2.2: State of the Art Low-loss FGC lines (a) Microshield [125, 122, 121] (b) Air-bridge CPW [98] (c) Micromachined CPW for CMOS [73] (d) Trenched CPW [52] (e) Micromachined FGC presented in this chapter [45, 46].

in the metallic conductors and frequency-independent dielectric loss in the substrate. The substrate material itself influences the propagation characteristics by increasing the value of the effective dielectric constant from 1, for an air-suspended coplanar line, to approximately 6, for the finite ground coplanar waveguide printed on a high-resistivity (3000 Ω-cm) silicon wafer (see Figure 2.1(a),(b)) independent of frequency. Given particular ohmic and dielectric losses for the metal and substrate used, line loss may be further influenced by the current density, which can be controlled by the aspect ratio and characteristic impedance.

Figure 2.2 shows the predominant modifications of the FGC line as reported in the

literature, and represents the current state-of-the-art low loss designs. Loss values are given as reported for both conventional and modified FGC lines of same dimensions. The microshield line, labeled 2.2(a), involves wet etching the silicon material underneath the FGC line supporting it with only a 1.5 $\mu$m dielectric membrane [125, 122, 121]. While the use of membranes has demonstrated the lowest loss by a planar interconnect, they are limited by the need for backside processing, complexity of the layout, and size of the required membrane. The air-bridge CPW line, 2.2(b), is a modified FGC in which the center conductor is realized with periodic air bridge sections, 150 $\mu$m in length, and connected to the substrate with 70 $\mu$m x 70 $\mu$m posts. These elevated center conductor sections may be difficult to design [98]. A micromachined FGC for CMOS has been developed, 2.2(c), in which the glass-enclosed metal conductors are suspended in air using a two-step wet etch [73]. However, the fabrication for this line is rather complex and may limit the thickness of the substrate. The trenched FGC line, 2.2(d), involves simply removing material from the apertures of the line using reactive ion etching (RIE) [52]. In this process, it is difficult to remove material from underneath the lines to obtain undercut since vertical side walls are achieved. The slower etch rate also reduces the amount of depth obtained, however the fabrication method is simple.

Herein, another low-loss approach is presented which effectively removes material underneath the line without requiring suspension of the center conductor in free space or back-sided processing. It will be shown that the micromachined FGC or MFGC line, Figure 2.2(e), is a preferable candidate for multi-layer thin-silicon integrated circuits [45, 46] due to the significant reduction in loss and ease in design. As a parametric study, line geometry is kept constant and micromachining is applied to the aperture regions to the extent that the silicon begins to etch laterally under the lines. The effect of lateral etching, or undercut, is examined for four different aspect ratios. A second parametric study investigates the ability to maintain a particular characteristic impedance while reducing loss through micromachining. Lastly, the MFGC lines are applied to a low pass filter to demonstrate performance ability.

## 2.3 Micromachined Coplanar Waveguide

The characteristic impedance of a FGC line strongly depends on its geometrical parameters including the center conductor width, ground width, and conductor separation. An increase of the characteristic impedance to values above 75 Ω requires either a narrow signal conductor leading to current crowding, or wider aperture dimensions, leading to multimoding or a single leaky mode [79, 78, 99, 115]. Another characteristic of FGC lines is the tight field concentration in the apertures between the conductors. When material in this area is removed, the line capacitance is reduced and leads to less current density in the conductors. As a result, the line exhibits lower loss and lower parasitic capacitance. Therefore, one method of increasing the line impedance without encountering the above problems due to geometry modifications is to remove material from the apertures with mechanical or chemical processes. Likewise, a particular impedance may be maintained and loss may be reduced by modifying the line geometry and removing dielectric material to modify the current distribution.

Figure 2.3 shows apertures of a micromachined coplanar waveguide in which material is removed from the aperture regions by wet etching using ethylenediamene pyrocatechol (EDP) [65]. This anisotropic etching is in contrast to the isotropic method shown in Figure 2.4 using a combination of hydrofluoric and nitric acids. These micromachined lines can be fabricated on full thickness substrates with no wafer thinning or via holes for ground equalization. Corner compensations have been developed to aid in micromachining bends and other discontinuities [65]. Alternatively, circuit sections with complex bends may be left conventional while the adjacent sections are micromachined. The micromachined lines propagate a near TEM mode with very little dispersion, and the effective dielectric constant of the micromachined finite ground coplanar waveguide lines is constant within $\pm$ 1% from 4 to 110 GHz, while junction parasitics are very weak. These properties simplify the design of millimeter-wave components and provide improved electrical performance. The design, fabrication, and measurement of interconnects and filters based on this micromachined line technology is discussed in detail below.

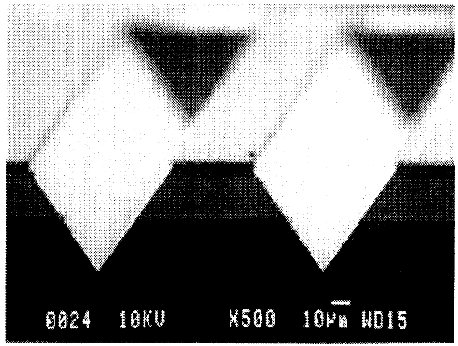



Figure 2.3: Anisotropically etched Si.

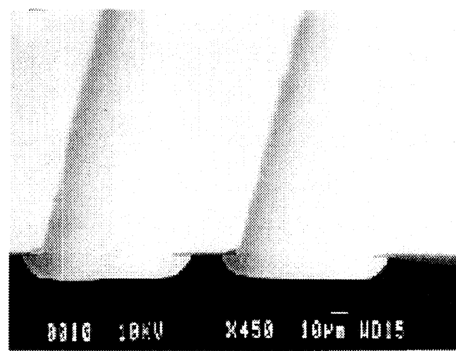



Figure 2.4: Isotropically etched Si.

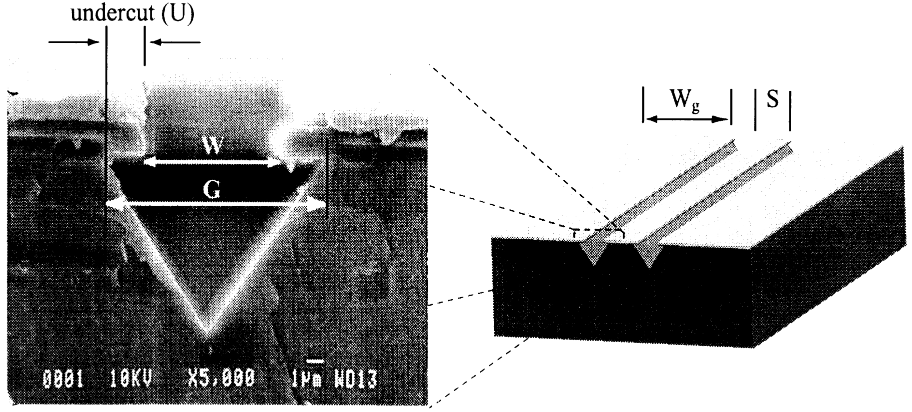



Figure 2.5: Cross-section of Micromachined Finite Ground Coplanar (MFGC) line.

### 2.3.1 Line Architecture

Micromachined Finite Ground Coplanar (MFGC) lines (see Figure 2.5) have a geometry similar to conventional FGC lines, except that the material underneath the line apertures has been removed, as discussed previously. The shape of the groove created by the etchant strongly depends on the solution and the time of the etch. The resulting micromachined FGC line has all the advantages of conventional CPW including balanced propagation, coplanar configuration, and the capability of front-side wafer processing. The width of the line and the depth of the grooves provide direct control over the cut-off frequency of the next higher order mode and the range of single mode propagation. In this research, focus is

placed on EDP-etched MFGCs because of the ease in fabrication and the better control over the undercut and realized shapes. The groove size, G, can be defined as the aperture width (W) plus the lateral undercut (U). By appropriately choosing the ground-strip width ($W_g$), the signal-strip width (S), and the groove size (G), the cut-off frequency can be pushed beyond the highest operating frequency. The result is the elimination of parasitic parallel plate/microstrip modes and the reduction of undesired loss. The design equation for this line is given below,

$$2(Wg + W) + S < F_G \lambda/2$$

where $F_G = \frac{1}{\sqrt{\epsilon_{eff}}}$, is a factor directly dependent on the amount of removed material. The electrical parameter $F_G$ is very important to the design of lines that operate in the single-mode regime. As it will be discussed later, $F_G$ is inversely related to the effective dielectric constant, and as a result strongly depends on the aspect ratio, $AR = \frac{S}{S+2W}$, and dielectric constant, $\epsilon_r$, of the substrate. Measurements performed on a variety of lines and for a variety of undercuts, U, reveal that in a MFGC line, the coefficient $F_G$ exhibits a strong dependence on the center conductor width, S, and undercut, U, and shows to be less critically dependent on the aperture, W. A plot of $F_G$ versus undercut for five different aspect ratios is shown in Figure 2.6. Note that for each aperture width, the depth of the center of the V-shaped groove is dictated by the 54.7° angle of the $< 111 >$ Si crystal planes. Therefore the 25 $\mu$m aperture yields a center depth of 17 $\mu$m, whereas that of the 80 $\mu$m aperture is 56 $\mu$m. In the limit of total dielectric removal, $F_G$ goes to 1. As seen in Figure 2.6, the two parameters highly influencing $F_G$ are the aspect ratio, AR, of the line and the undercut, U. This indicates that the electric field between the line conductors confines mostly in the aperture region and very little field is penetrating into the substrate. Due to the capability of the line to effectively confine the fields on one side of the wafer, wafer thickness and back side metallization are not critical to performance. As a result, wafer thinning is not required unless dictated by other circuit layout and size restrictions.

Several micromachined FGC lines and filter circuits have been fabricated on 500 $\mu$m thick Si substrates. The total width of the line, 2(Wg+W)+S, has been chosen for all designs to push the cut-off frequency of the first higher order mode to 120 GHz. The back side of the

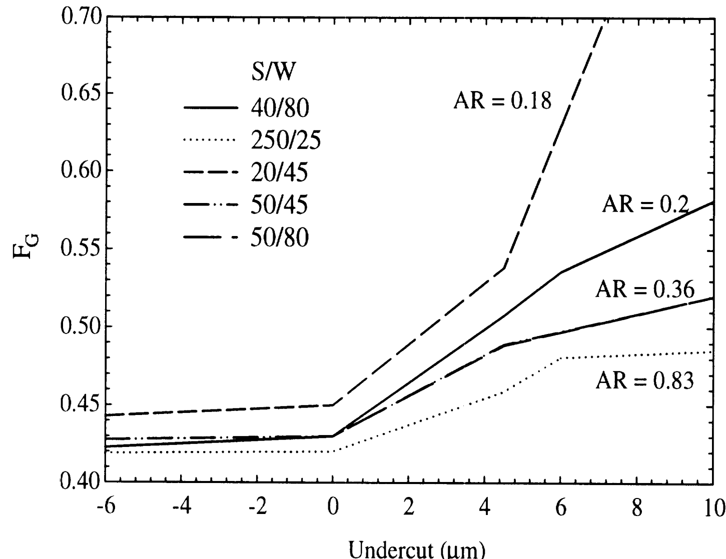



Figure 2.6: $F_G$ versus Undercut($\mu$m) for five different aspect ratios(AR=S/(S+2W)), where S is the center conductor width and W is the aperture width.

wafer is not metallized, but is in contact with a metal chuck during measurements. Since the realized geometries are symmetric, air bridges for ground equalization are not needed in the circuit.

### 2.3.2 Fabrication

As shown in Figure 2.7, all the micromachined FGC lines studied herein are fabricated on 500 $\mu$m thick Si substrates with a 1.5 $\mu$m $SiO_2/Si_3N_4/SiO_2$ protective layer. Circuit metallization is obtained via electro-plating 1.7-2 $\mu$m of Chrome/Gold (Cr/Au). Si apertures are opened and anisotropically etched using ethylenediamine pyrocatechol (EDP). Although both isotropic and anisotropic etchants have been investigated [65], anisotropic etching with EDP has been the most reliable. Since this selective etchant stops along the $< 111 >$ crystal planes, this method of micromachining is relatively easy to control. Undercut at a rate of 2 to 3 $\mu$m per hour has been characterized. In the following, lines with 2-12 $\mu$m undercut have been designed, fabricated, and measured to understand the trends of line performance versus undercut for various aspect ratios.

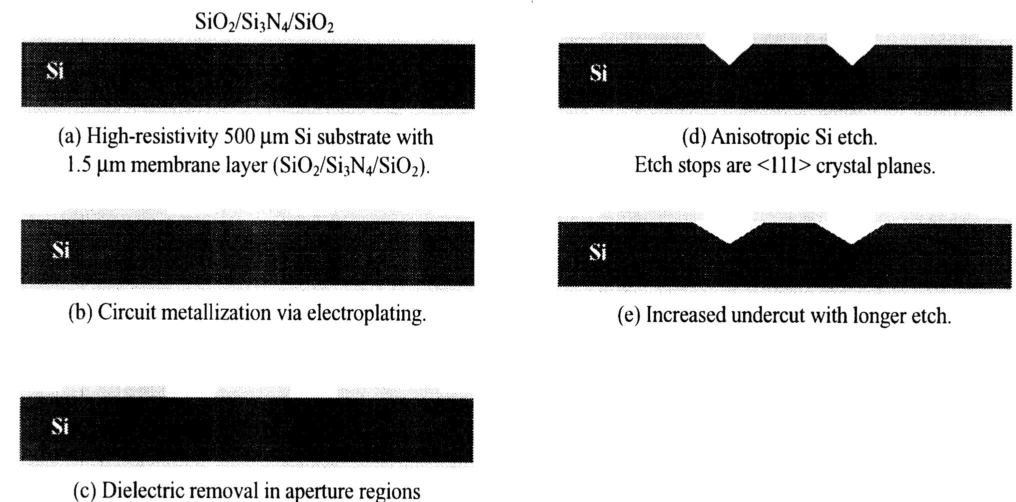



Figure 2.7: MFGC process flow.

## 2.4 Measurements

Following fabrication, S-parameters are measured using a Through-Reflect-Line (TRL) calibration. On-wafer calibration standards, consisting of micromachined FGC lines are used with NIST MultiCal software [70, 67, 68]. All measurements are made on an Alessi probe station using picoprobes[1] from 2 to 110 GHz, with a gap from 60 to 75 GHz, and several test sets for calibration to cover the desired frequency range. The resulting S-parameter data from the through and delay lines are then processed using MultiCal to compute the effective dielectric constant, $\epsilon_{eff}$, and attenuation constant, $\alpha$.

### 2.4.1 Effect of Micromachining and Lateral Undercut

Lines of various aspect ratios and groove sizes are fabricated and their loss and effective dielectric constants are measured for frequencies varying from 2 GHz to 110 GHz. Measured results show that the loss and $\epsilon_{eff}$ strongly depend on the aspect ratio of the line and the amount of material removed. As seen from the measurements, $\epsilon_{eff}$ is independent to the operating frequency indicating that the line has almost zero dispersion. Specifically, Figure 2.8 shows measured values of the effective dielectric constant as a function of frequency, with W-S-W equal to 80-40-80 $\mu$m, for the conventional FGC and micromachined FGC lines with

[1]GGB Industries, Naples, FL.

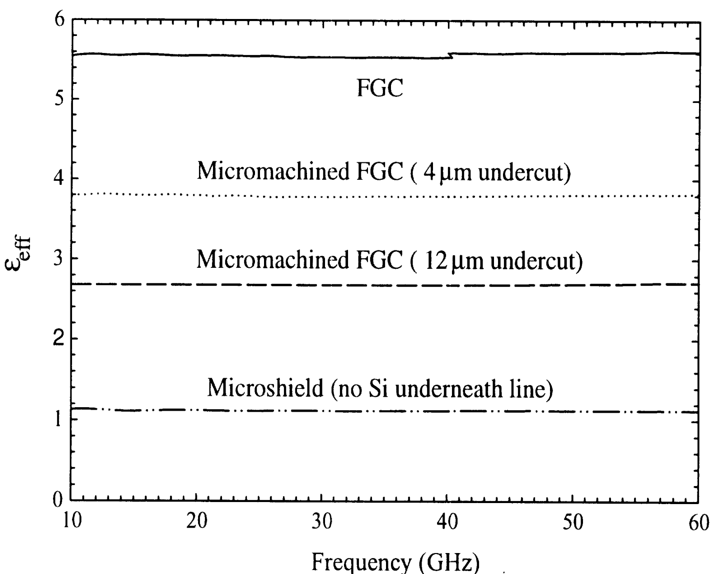
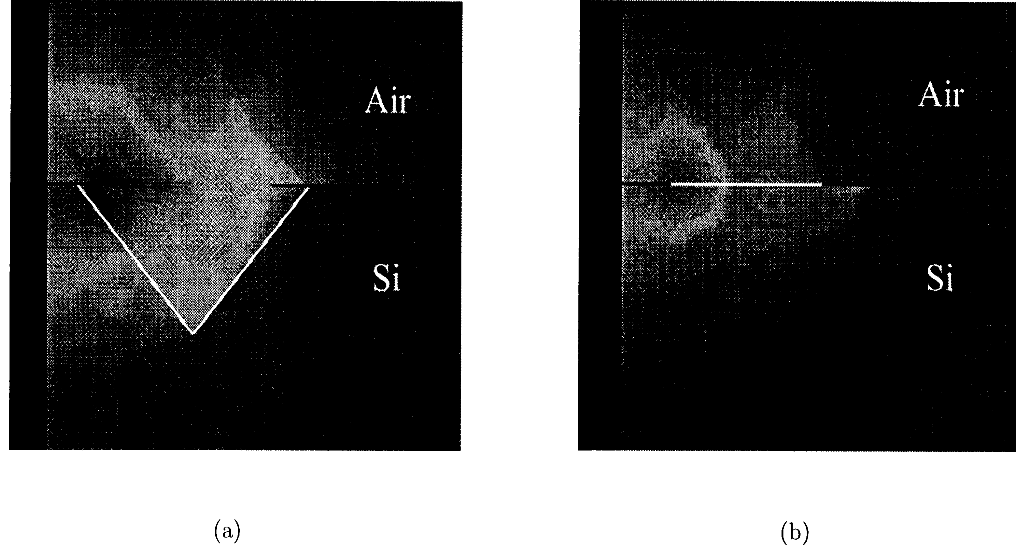



Figure 2.8: $\epsilon_{eff}$ vs. frequency for a 80-40-80 $\mu$m MFGC with 4 and 12 $\mu$m undercut. Comparison with conventional FGC of same dimensions and 75 $\Omega$ microshield with S/W of 250/25 $\mu$m.

4 and 12 $\mu$m undercut. Note, although the silicon is unetched for the conventional case, the membrane $SiO_2/Si_3N_4/SiO_2$ is removed in the aperture regions. These measurements are compared to a membrane coplanar waveguide (microshield [125, 122]), which has an effective dielectric constant close to 1 independent of aspect ratio as all silicon material is removed from the line. This particular microshield line is 75 $\Omega$ with S/W of 250/25 $\mu$m. These results confirm that the removal of the material results in reduction of the effective dielectric constant from the initial value of 5.6 to 2.72 for this particular geometry due to considerable reduction of the line capacitance. The effective dielectric constant of any FGC line will be reduced through micromachining the aperture regions, and the magnitude of the change is dependent on the width of the aperture and the amount of material removed.

To confirm the measurements, a full-wave finite element method [4, 21] is used to plot the electric field distribution in micromachined FGC lines with 8 $\mu$m undercut (see Figure 2.9(a)) and compared to the field distribution in non-micromachined FGC lines (see Figure 2.9(b)). From the two figures it is shown that the field concentrates in the air region where the material is etched away, resulting in a much lower effective dielectric constant, higher line




(a) (b)

Figure 2.9: Simulated electric field distribution of (a) MFGC line (b) conventional FGC.

impedance and reduced ohmic loss. Loss reduction is evident from the measured data shown in Figure 2.10 where loss in dB/cm is plotted versus frequency for W-S-W lines of 45-20-45 $\mu$m for both conventional FGC and micromachined FGC with 4 $\mu$m undercut. Note both lines are on the same wafer, and the conventional FGC line has bare silicon in the aperture regions with no 1.5 $\mu$m $SiO_2/Si_3N_4/SiO_2$ membrane. The loss in the micromachined line is approximately 40% less than that of FGC, with a 1 dB/cm improvement approaching 2.5 dB/cm at 94 GHz. The loss also exhibits a square-root frequency dependence indicating dominance of conductor loss.

Figure 2.11 shows the loss factor in dB/cm for a 80-40-80 $\mu$m micromachined line measured from 10 GHz to 60 GHz. The loss in this line has been reduced from 1.7 dB/cm to 1.0 dB/cm, or 0.1 dB/mm, for the 12 $\mu$m undercut MFGC line at 60 GHz. The lines also exhibit the same square root frequency dependence seen in Figure 2.10. To illustrate this, the measured data are approximated by simple functions that vary proportionally to $\sqrt(f)$. Since this loss is predominantly ohmic and has a known frequency dependence, 1.5 dB/cm, or 0.15 dB/mm, attenuation is expected for the 12 $\mu$m MFGC line at 94 GHz. Similarly, Figure 2.12 shows loss in dB/cm for FGC and micromachined FGC lines with W-S-W equal to 45-50-45 $\mu$m and indicates substantial reduction in loss, from 1.7 dB/cm to 0.9 dB/cm, with increasing undercut up to 6 $\mu$m.

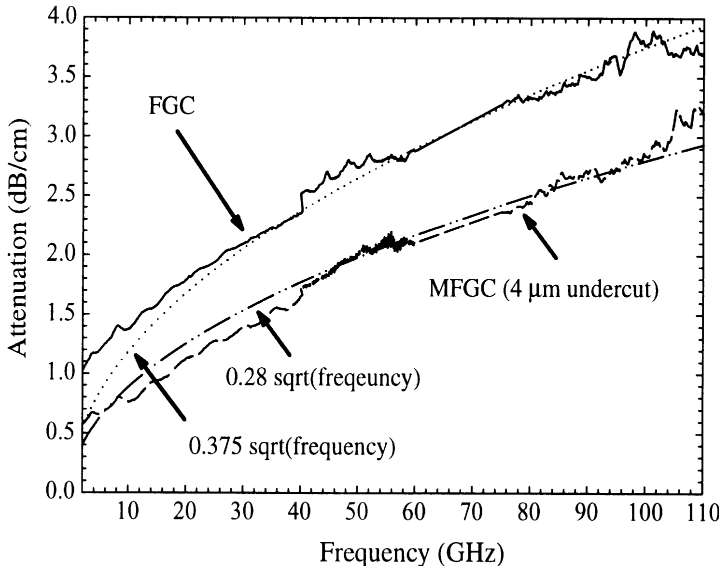



Figure 2.10: Attenuation vs. Frequency for FGC line with 20 $\mu$m center conductor and 45 $\mu$m apertures compared with micromachined line of same geometry.

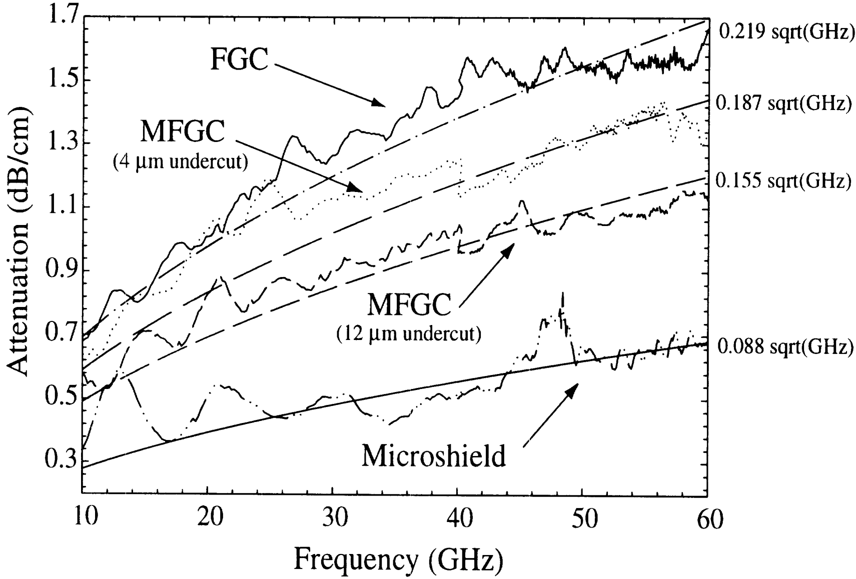



Figure 2.11: Attenuation vs. Frequency. All FGC lines have W=80 $\mu$m, S=40 $\mu$m. The micromachined lines have undercut of 4 and 12 $\mu$m, and the microshield line has a 75 $\Omega$ characteristic impedance with 250 $\mu$m center conductor and 25 $\mu$m apertures.

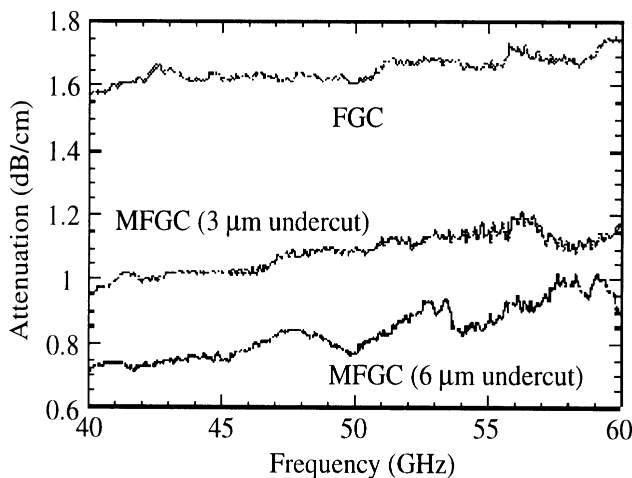



Figure 2.12: Loss in dB/cm in FGC and MFGC lines with S=50 and W=45 $\mu$m at U-band.

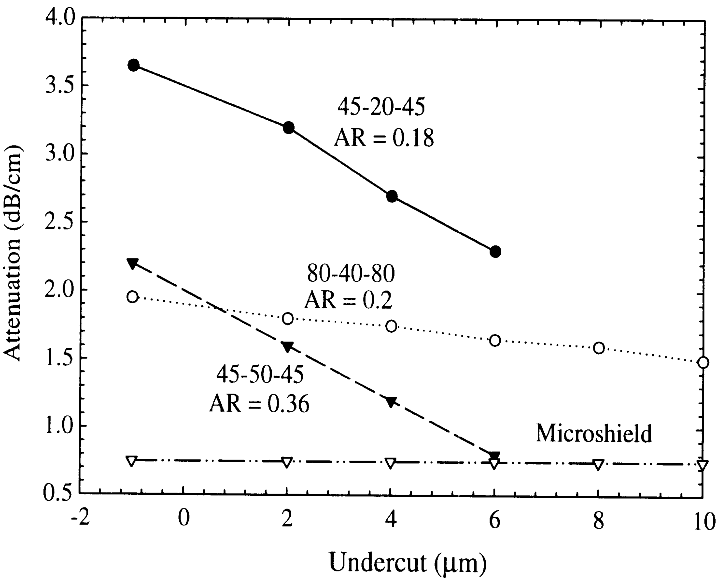



Figure 2.13: Measured loss versus undercut at 94 GHz.

For micromachined FGC lines with the aspect ratios discussed herein, measurements up to W-band have confirmed the predominantly ohmic loss behavior versus frequency. Based on this, the $\sqrt(f)$ dependency can be used to predict losses at 94 GHz. Figure 2.13 shows loss in dB/cm at 94 GHz for various lines, as a function of undercut. Comparison of this loss to that of a 75 $\Omega$ microshield line with S/W of 250/25 $\mu$m indicates the capability of the micromachined FGC to provide competitive performance to that of membrane lines, the loss of which approaches 0.075 dB/cm in W-band [117, 92]. Although microshield FGC lines yield the lowest attenuation to date, two trade-offs are the complex fabrication and longer wavelength due to the air dielectric. Figure 2.14 shows measured effective dielectric constant versus undercut for a micromachined FGC line with S/W of 40/80 $\mu$m. The monotonic decrease of the effective dielectric constant with undercut, indicates that the loss exhibited by the micromachined line in dB/$\lambda_g$ will not vary with the undercut as dramatically as it has been observed when the same loss is measured in dB/cm. This implies that use of these lines is unquestionably beneficial in circuits where physical lengths remain fixed, such as antenna feed networks. However, in circuits where electric lengths remain unchanged, micromachined lines will tend to provide less loss and reduced junction parasitics but will result in longer circuit physical dimensions, although not as long as those required from microshield. In this case, the use of micromachined lines clearly depends on the trade off allowed by the circuits specifications and the objectives of the circuit designer.

From the measured micromachined FGC lines, design guidelines based on measured data have been developed. Although there are different ways to present such data, tabular format has been used here as seen in Table 2.4.1. This table shows the effect of removing material from the aperture regions with increasing lateral undercut, as compared to that of a conventional FGC line [59]. The general trend with increasing undercut is decreasing $\epsilon_{eff}$, decreasing attenuation, and increasing characteristic impedance. These aspect ratios where chosen to ensure balanced, single-mode propagation, and lines with similar aspect ratios will behave accordingly.

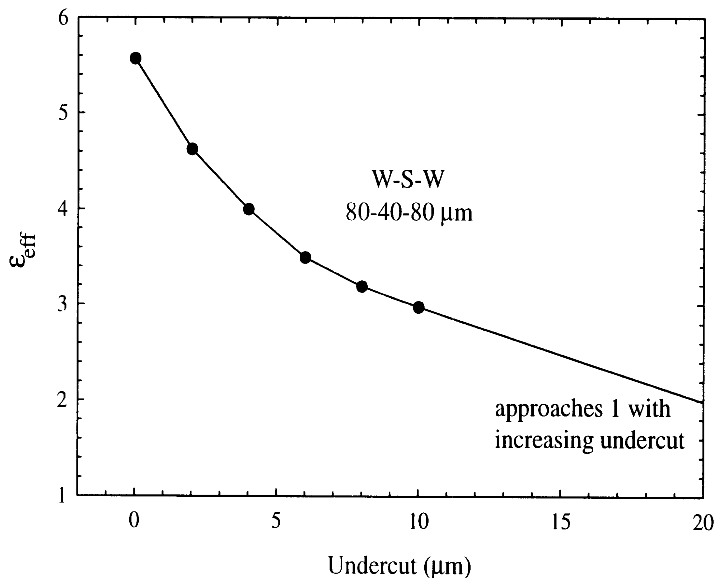



Figure 2.14: Effective dielectric constant versus. undercut for MFGC with W-S-W equal to 80-40-80 $\mu$m.

| AR | | FGC (no undercut) | 2$\mu$m | 4$\mu$m | 6$\mu$m | 8$\mu$m | 10$\mu$m |
|---|---|---|---|---|---|---|---|
| 0.18 | $\epsilon_{eff}$ | 4.938 | 4.165 | 3.56 | 2.52 | n/a | n/a |
| 0.18 | $\alpha$ (dB/cm) | 3.65 | 3.2 | 2.7 | 2.3 | n/a | n/a |
| 0.18 | $Z_o$ ($\omega$) | 71 | 77.31 | 83.62 | 99.39 | n/a | n/a |
| 0.2 | $\epsilon_{eff}$ | 5.57 | 4.625 | 4.0 | 3.494 | 3.189 | 2.973 |
| 0.2 | $\alpha$ (dB/cm) | 1.95 | 1.8 | 1.75 | 1.65 | 1.6 | 1.5 |
| 0.2 | $Z_o$ ($\omega$) | 64 | 70.2 | 75.5 | 80.8 | 84.58 | 87.59 |
| 0.36 | $\epsilon_{eff}$ | 5.408 | 4.83 | 4.34 | 4.081 | 3.845 | 3.698 |
| 0.36 | $\alpha$ (dB/cm) | 2.2 | 1.6 | 1.2 | 0.8 | n/a | n/a |
| 0.36 | $Z_o$ ($\omega$) | 57 | 60.31 | 63.53 | 65.62 | 67.60 | 68.93 |

Table 2.1: Decreasing $\epsilon_{eff}$, decreasing attenuation (at 94 GHz), and increasing characteristic impedance for three different aspect ratios (AR), with increasing undercut.

### 2.4.2 Maintaining Characteristic Impedance.

Given a particular aspect ratio, micromachining the aperture regions has been shown to increase the characteristic impedance in addition to reduce loss. Although the reduction in

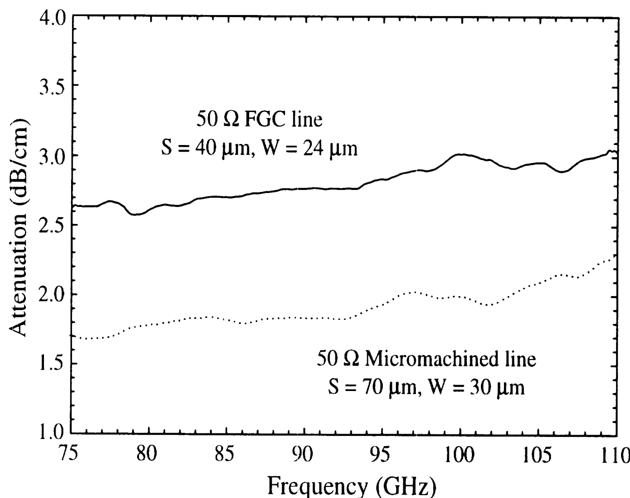



Figure 2.15: Measured attenuation versus frequency for 50 and 70 Ω lines in FGC and MFGC versions showing lower loss in micromachined line.

loss is a desired effect, higher impedance may not be. Using 2-D static solvers to determine the capacitance of the cross section of an MFGC line, a particular impedance may be obtained by modifying the aspect ratio [5]. In this way, impedance is maintained and loss is reduced as shown through the measured results of Figure 2.15. A 50 Ω FGC line with S/W of 40/24 $\mu$m has loss of 2.6 dB/cm at 75 GHz, while the micromachined version has loss of only 1.7 dB/cm while maintaining the same 50 Ω impedance by modifying S/W to 70/30 $\mu$m. The increased width of the line does not increase radiation loss as long as S+2W is close to $\lambda_g/10$ [96]. This method of maintained impedance with reduced loss is applied to combining networks in Chapter 5.

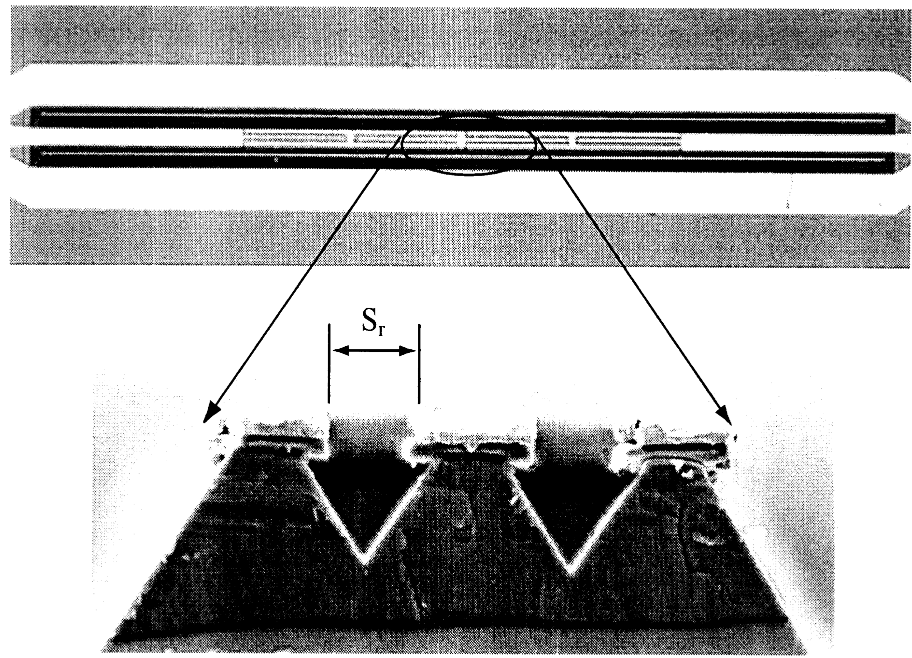



Figure 2.16: Micromachined four resonator band-pass filter with W = 45 $\mu$m, S = 50 $\mu$m, and 4 $\mu$m undercut.

### 2.4.3 Micromachined Low pass FGC Filter

The micromachined finite ground coplanar waveguides described above have been applied to a four-resonator low pass filter as shown in Figure 2.16. The Si substrate has been etched away from the main lines (45-50-45 $\mu$m) and the resonator apertures ($S_r$ = 20 $\mu$m) to allow for reduced loss and reduced parasitics. The filters were etched for two hours in EDP to introduce a 4 $\mu$m undercut. This filter design was taken from Weller, Herrick, *et al.* as it was originally applied to micromachined filters with thin film MIM capacitors (see Appendix D) [120]. Here the same metallization is used, no MIM capacitors are used, and micromachining is applied only to the aperture regions. Measured performance is shown in Figure 2.17, with a gap in data points from 60-75 GHz due to lack of appropriate measurement equipment. The measured results for the low pass filter show a cut-off frequency close to 55 GHz, show pass-band insertion loss of 0.8 dB up to 35 GHz, and demonstrate the ability to apply MFGC lines to a range of applications.

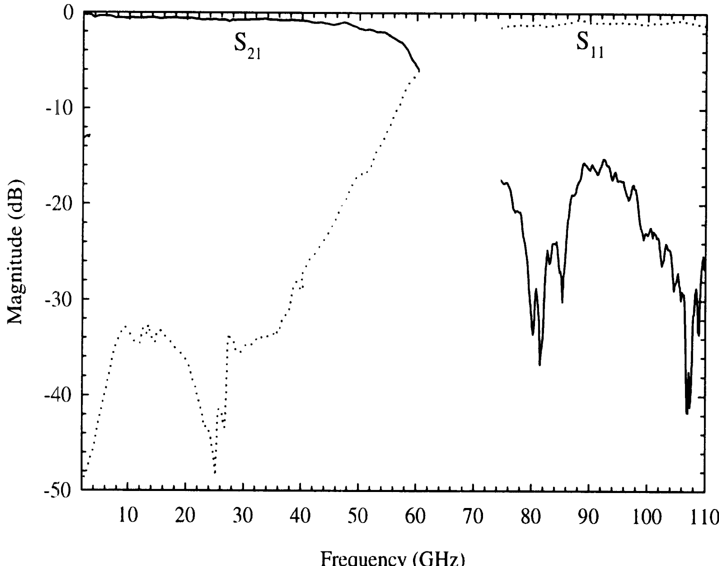



Figure 2.17: Measured scattering parameters for the micromachined low pass filter of Figure 2.16.

## 2.5 Modeling of Micromachined Coplanar Waveguide

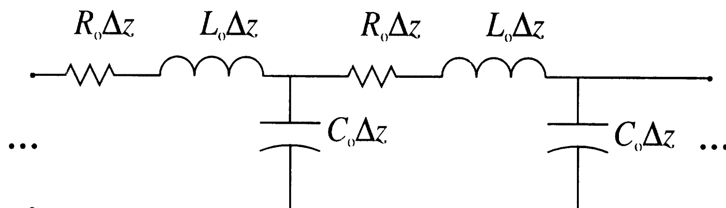



Figure 2.18: Lumped-element equivalent circuit for an incremental length of transmission line.

Quasi-TEM propagation is assumed to be the dominant mode for modeling of the MFGC line. In addition, it is assumed that ohmic losses dominate and dielectric losses are negligible. These assumptions allow the MFGC waveguide to be modeled as a transmission line with per-unit-length series inductance, series resistance, and shunt capacitance as shown in Figure 2.18. The series inductance and resistance are found using SIMIAN, a two-dimensional frequency-dependent series impedance extraction tool [108, 62]. The shunt capacitance is found using a two-dimensional FEM program [5]. The impedance and effective dielectric

constant can be found from the capacitances with and without substrates with the following equations.

$$\epsilon_{eff} = \frac{C_{sub}}{C_{air}}$$

$$Z_o = \frac{1}{v_o \sqrt{\epsilon_{eff}} C_{air}}$$

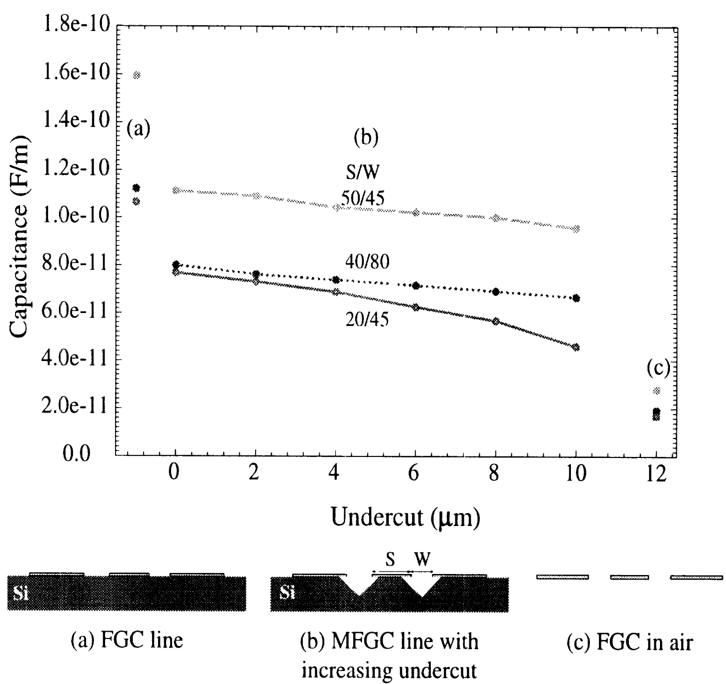



Figure 2.19: Capacitance versus undercut for three FGC lines with values for (a) a conventional FGC line (b) a micromachined FGC line with increasing lateral undercut (c) a FGC in air.

Capacitance values as calculated from Maxwell-2D [5] are shown in Figure 2.19. The values shown are categorized in three groups. Group (a) represents the typical values of a conventional FGC line on silicon with the 50/45 line having the highest capacitive value of $1.6\times10^{-10}$ F/m and the other two lines (40/80 and 20/45) with values close to 1.1 $\times10^{-10}$ F/m. Group (b) represents values for a micromachined line that is first etched without undercut (0 $\mu$m undercut) and then progressively etched with increasing undercut up to 10 $\mu$m. All three lines show decreasing capacitance in response to increasing undercut with the most pronounced slope for that of the 20/45 line. For this line, a 10 $\mu$m undercut would

have the center conductor floating on air which is unrealizable. However the effect is shown. Group (c) represents the capacitance of the lines on air.

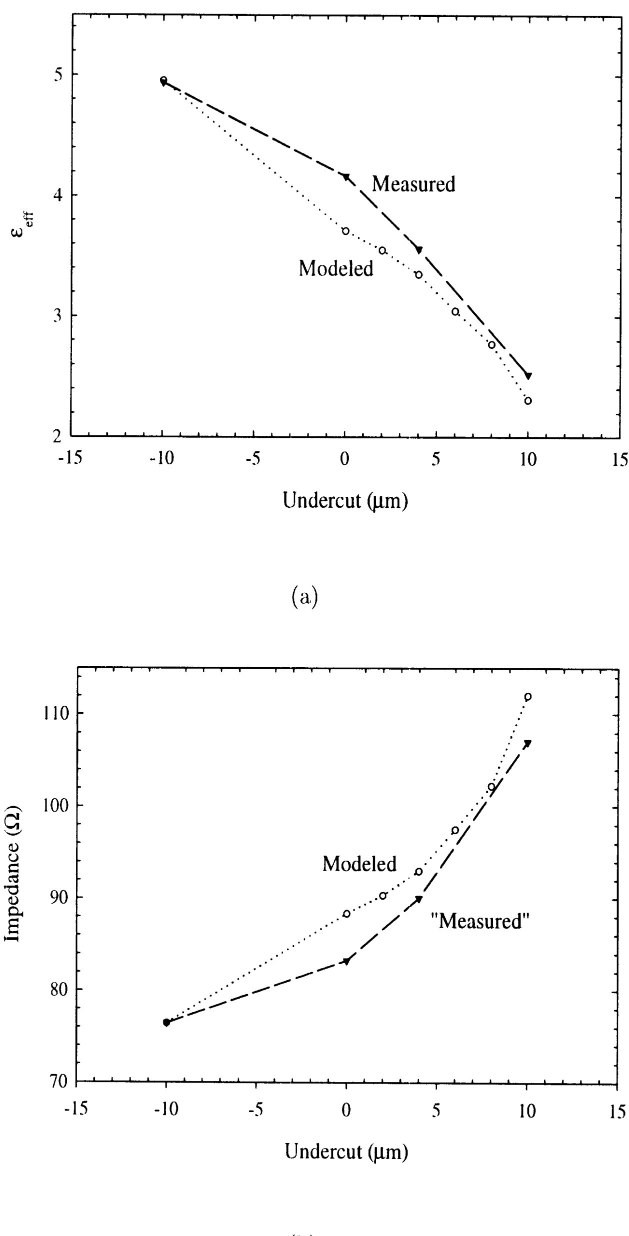



Figure 2.20: (a) Effective dielectric constant vs. undercut for FGC and MFGC with W-S-W equal to 45-20-45 $\mu$m. (b) Characteristic impedance vs. undercut for FGC and MFGC with W-S-W equal to 45-20-45 $\mu$m.

Maxwell-2D is used to model the W-S-W 45-20-45 $\mu$m line of Cr/Au (500 Å/2000 Å) on a 1.5 $\mu$m tri-dielectric layer with a 500 $\mu$m Si substrate as shown in Figure 2.19b. A plot of

$\epsilon_{eff}$ versus undercut for the measured and modeled geometry show agreement of the FGC, or unetched line (Figure 2.20(a)). Comparison of the effect of micromachining show similar slopes and close values. Figure 2.20(b) shows the corresponding characteristic impedance values, which are also quite similar. The offset between the measured MFGC data points may be attributed to many factors, including the difficulty of determining undercut within $\pm$ 2 $\mu$m, particularly with regard to uniform etching along the length of the line. Additional factors include differences in the dielectric constant of the Si, $SiO_2$, $Si_3N_4$ and thicknesses of any of the materials. Small changes in any of these parameters can greatly affect the results. However, this simple modeling can provide valuable information about the general effect of micromachining and the approximate impedance and effective dielectric values that may be obtained.

Figure 2.21 shows the resistance and inductance per unit length versus frequency as calculated from Simian for four different FGC lines. Note in Figure 2.21(a) the increase in resistivity with increasing frequency for all four aspect ratios, with the 20 $\mu$m center conductor line showing the highest resistivity of 5000 $\Omega$/m at 110 GHz and the 50 $\mu$m line showing the least resistivity of 2500 $\Omega$/m at 110 GHz. The inductance per unit length as shown in Figure 2.21(b) is constant over frequency with the widest aperture dimension of 80 $\mu$m giving the highest in inductance while the lowest inductive value of $4.2\times10^{-7}$ H/m is calculated for the narrowest aperture dimension of 24 $\mu$m.

The attenuation can be calculated using the following formula:

$$\alpha = Re\sqrt{(R + jwL)(jwC_{sub})}$$

Attenuation versus frequency for the 45-20-45 line is shown in Figure 2.22. Recall the line is 71 $\Omega$ conventionally and becomes 84 $\Omega$ with micromachining and 4 $\mu$m of undercut. The modeled data is fit to the measured FGC case by modifying the conductivity used to compute the series resistance and inductance of the conductors. Although this does not affect the slope of the attenuation curve, it takes into account any frequency independent dielectric or radiation losses previously unaccounted for, and shifts the curve up or down. Once the FGC line modeling is fit to the measured data, the attenuation is calculated for the MFGC line by simply replacing the shunt capacitance with that for the micromachined

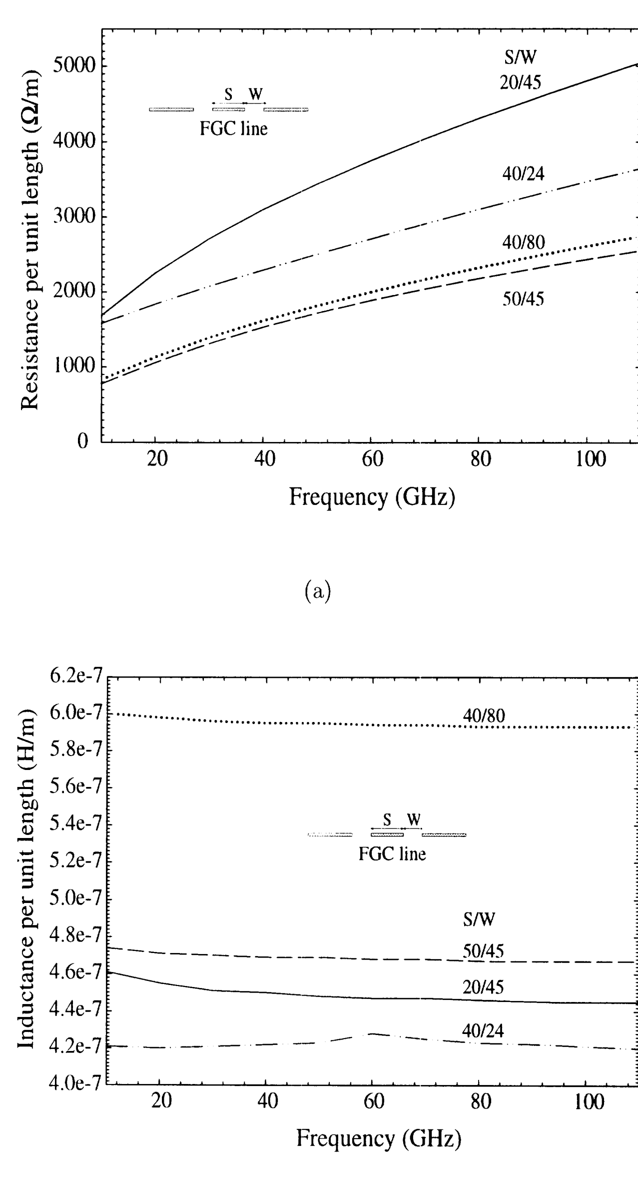



Figure 2.21: (a) Resistance per unit length versus frequency for four FGC lines as found using Simian. (b) Inductance per unit length versus frequency for four FGC lines as found using Simian.

line. Using this method good agreement is obtained between measured, and modeled, micromachined and conventional lines.

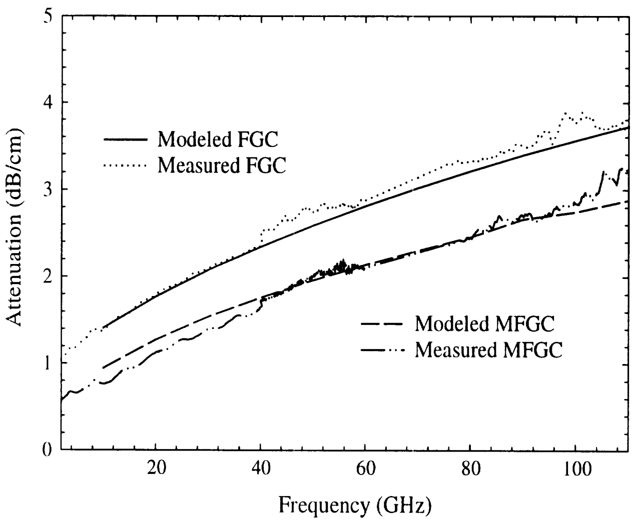



Figure 2.22: Attenuation vs. frequency for 45-20-45 $\mu$m line comparing measured and modeled data.

## 2.6 Conclusions

A new class of Si micromachined lines has demonstrated significantly lower-loss performance as compared with conventional CPW from 2-110 GHz. This is due to the capability of the lines to excite a quasi-TEM mode, operate free of parasitic parallel plate modes, and operate without vias, resulting in single side wafer processing. These lines have been studied extensively and have shown the potential to compete with membrane lines in terms of performance, with the advantage of simpler fabrication and compact line geometry. Increasing lateral undercut decreases the effective dielectric constant, decreases attenuation, and increases characteristic impedance. By modifying the line geometry, a particular characteristic impedance can be maintained while loss is reduced. In addition, the MFGC line has been used in the development of a four-resonator low pass filter, demonstrating one of many circuit applications. Finally, modeling techniques have been given for design assistance of these low loss lines.

# CHAPTER 3

# SINGLE-LAYER SILICON MICROMACHINED VERTICAL INTERCONNECTS

## 3.1 Introduction

This chapter addresses vertical system integration by developing a micromachined 3-via interconnect which allows low loss transfer of millimeter-wave signals through a silicon wafer. More specifically, a novel vertical interconnection utilizing finite ground coplanar (FGC) waveguide and silicon micromachining is developed for W-band. This transition uses standard processing techniques, and is a compact 520 $\mu$m x 520 $\mu$m design with measured results indicating 0.5-0.6 dB insertion loss at 94 GHz. This chapter introduces the interconnect concept and describes the matching method used for loss minimization. In addition, the novel interconnect micromachining fabrication technology is explained. Finally, W-band measurements are compared to simulated results to show the ability and accuracy of the fabrication process, as well as the applicability of this technology to high frequency applications.

## 3.2 Motivation

The challenge in today's market is to meet three criteria: low cost, high performance, and small size. The drive behind highly-integrated multi-chip modules (MCMs) comes from different segments in the market. At one end, electronic data processing and networking

markets below 1 GHz are driving increasing chip lead counts and improved electrical performance, as they move toward greater computational capabilities. On the other end, package size reduction and cost are being driven by automotive, radar, and mobile communication markets, moving to replace waveguide components with smaller products. One method of meeting the required metrics for both markets is a multi-layer approach.

When referring to multi-layer IC structures, there are four basic three-dimensional stacking approaches: bare die (chips), packaged chips, multichip modules (MCMs), and wafers. By replacing single chips or MCMs with three-dimensional integrated circuits, substantial size and weight reductions are achieved [3]. Also, a four chip stack requires less printed circuit board real estate as compared to four adjacent chips, improving substrate efficiency. Reducing the interconnect length through three-dimensional integration also improves performance by minimizing signal delay. The magnitude of these various benefits depends on the vertical interconnections and three-dimensional packaging, regardless of the stacking approach.

Table 3.1: Multichip Module (MCM) assembly techniques for X-band frequencies (current state-of-the art)[32, 63].

| Substrate | Vertical Interconnect | Chip Interconnect | Company |
|---|---|---|---|
| Cofired Ceramic | Fuzz Button | Wire Bond | Raytheon (E-Systems) |
| Low $\epsilon$ polymer on Si | HDI thin film | HDI-chips first | General Electric, Lockheed |
| Cofired ceramic | Solder-filled vias | flip chip | Micron |

At lower frequencies, such as X-band, bare dice are mounted on a multi-chip module substrate and interconnected using wire bonding, tape automated bonding (TAB), flip-chip, or thin film metallization. The multi-chip modules are then stacked vertically using various integration techniques. Table 3.1 shows some of these state-of-the-art techniques and the companies credited for them [3, 32]. Ceramic MCMs using fuzz buttons in plastic spacers and filled vias in substrates by Raytheon (E-Systems) are prevalent. Another example is General Electric and Lockheed's high-density interconnect (HDI) approach for thin film

interconnects. Note that MCM substrates may be cofired ceramic, printed wiring board, or a combination of thin film metals and dielectric materials over substrates such as silicon, diamond, and metal. Thus, at X-band and lower frequencies, there are many commercially available vertical interconnects for various multilayer schemes on various substrates.

In W-band, this is not the case, and the examination of multi-layer approaches necessitates development of vertical interconnects. At microwave and millimeter-wave frequencies in particular, the added discontinuities of a vertical transition make low loss and wide bandwidth more challenging goals, and the transition may be coupled through a substrate electromagnetically or with direct contact. In this research effort, a compact, direct contact vertical interconnect is developed using silicon and finite ground coplanar transmission line technology at 94 GHz.

## 3.3 Vertical Interconnect Concept

Silicon micromachining has been applied to microwave and millimeter wave circuits in many ways since its introduction. Membrane supported structures such as antennas, transmission lines, and filters have shown improved performance and have extended the operating range of planar circuits to W-Band frequencies and beyond [31, 120, 46, 84, 33]. New concepts in integrated conformal packaging have been introduced, leading the way for micromachining to impact planar microwave circuits beyond the component level and into the system integration area [58, 40, 65]. One scenario for total system integration calls for the use of multiple layers to accomplish various system functions such as amplification, signal reception, down conversion, and filtering. Micromachining offers the possibility to vertically connect multiple silicon layers to achieve new levels of high density integration.

A conceptual schematic of the three-via vertical interconnect appears in Figure 3.1. The pyramidal shaped vias form a three conductor transmission line through a silicon (Si) substrate, and are expected to create very little radiation into the substrate. The two ground vias open from the front side of the wafer, while the center conductor via opens from the opposite side. This allows flexibility in choosing the via separation, minimizes circuit size, and reduces radiation by forcing the current to flow along the parallel inner

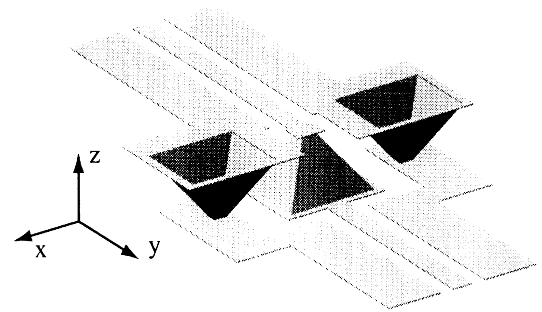



Figure 3.1: A vertical interconnect employing three micromachined pyramidal via holes. The vias permeate the Si substrate (not shown) to connect the upper and lower finite ground coplanar (FGC) transmission lines.

sidewalls.

## 3.4 Preliminary Design and Simulation

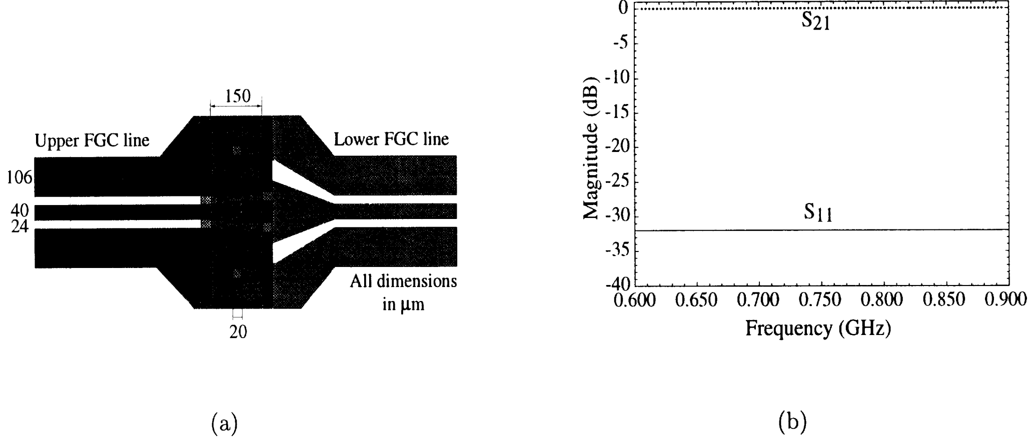
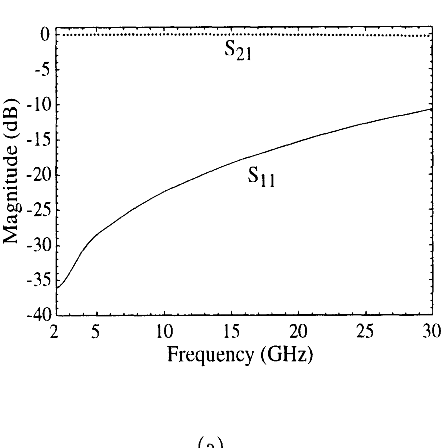
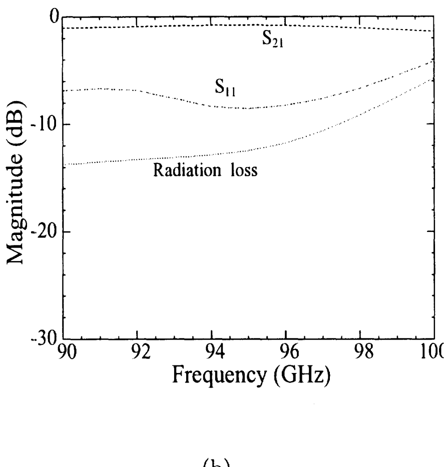



Figure 3.2: (a) Schematic. (b) Simulated S-parameters for a single 3-via interconnect from 600-900 MHz.

The preliminary design is shown in Figure 3.2(a) as simulated on a 100 $\mu$m high-resistivity Si substrate with 50 $\Omega$ FGC lines. Both upper and lower FGC lines have 40 $\mu$m center conductors and 24 $\mu$m apertures. The total width of the line is 300 $\mu$m, which is much less than $\lambda_g/2$ (650 $\mu$m) at 94 GHz. Although the silicon dielectric is not shown




(a)




(b)

Figure 3.3: Simulated S-parameters for single three-via interconnect: (a) 2-30 GHz (b) 90-105 GHz.

in Figure 3.2(a), the pyramidal-shaped vias are completely embedded in the dielectric with 150 x 150 $\mu$m apertures narrowing to 20 x 20 $\mu$m at the via bases. Figure 3.2(b) shows the simulated S-parameters from IE3D [132] ranging from 600-900 MHz. The response is quite flat with insertion and return loss values of 0.0027 dB and 32 dB, respectively, without inclusion of conductor loss. Thus this transition works well at lower frequencies.

Figure 3.3 shows the effect of increasing frequency on the three-via structure. At 2 GHz, the transition is quite effective with insertion and return losses of 0.0009 dB and 36 dB, respectively. As frequencies increase to 30 GHz, however, the performance decreases to insertion and return losses of 0.34 dB and 10.7 dB, respectively. Simulations from 90-100 GHz show further deterioration at high frequencies as shown in Figure 3.3(b). The best reflection and insertion loss achieved in this case are 8 and 1 dB at 90 GHz, respectively. Radiation loss has been defined here as $10 \cdot log(1 - |S_{11}|^2 - |S_{21}|^2)$, since in this simulation no conductor or dielectric losses have been defined. By observing the computed values, we can conclude that the high insertion loss is mostly attributed to radiation loss which varies from 14 dB at 90 GHz to 6 dB at 100 GHz.

The field in the vias is well confined as shown in Figure 3.4 and therefore does not contribute to the radiation loss. The calculations of these field distributions has been

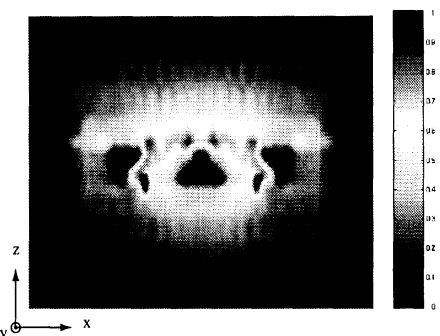
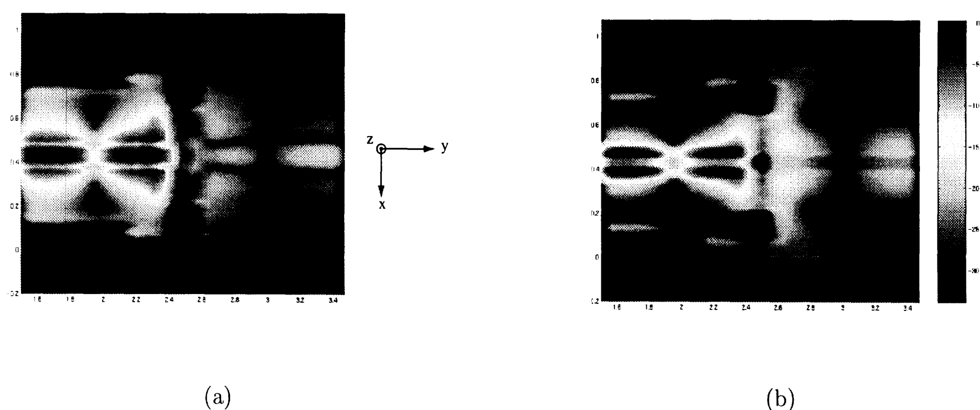



Figure 3.4: Electric field distribution for yz-plane of 3.2(a)

performed using FEM[1] with the feedlines terminated as open circuits and excited with ideal current sources. Note the fields on the two lines exhibit strong standing waves, which are denoted by dark and light periodic sections as shown in Figure 3.5. The radiation loss exhibited by this transition is due to the electric field excited at the terminating edge of the input line. This field launches a horizontally-polarized substrate mode as shown in Figures 3.5(a) and 3.5(b).



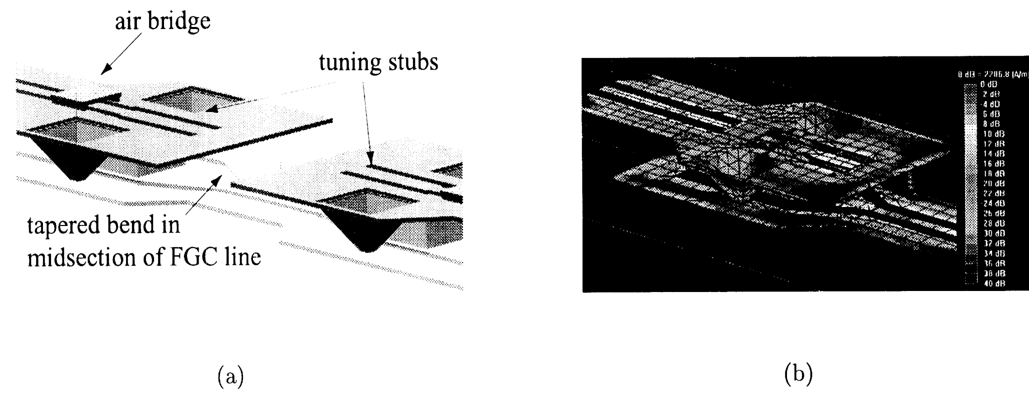

(a) (b)

Figure 3.5: (a) Z-component of the electric field vector for the transition of Figure 3.2(a). (b) Total electric field distribution for the transition of Figure 3.2(a) showing launched horizontal electric field component.

[1]FEM code developed by Dr. Jong-Gwan Yook at The University of Michigan

## 3.5 Improved Design and Simulation

To resolve the radiation problem at high frequencies, the transition from the feed FGC line to the vertical via structure has been modified as shown in Figure 3.6(a) [2]. The two finite grounds from the upper line have been connected at the end of the line to short circuit any undesired horizontally polarized substrate modes that would tend to launch a parasitic wave from the end of the line. The presence of the short requires a quarter-wave FGC stub to provide a radio-frequency (RF) open to fields which would tend to propagate horizontally passed the via structure [43, 47]. Furthermore, compensation is required to adjust for the capacitance introduced by the vias themselves and the inductance produced by the sharp bends in the lines. The matching network used to remedy this consists of tapered bends to smooth the transition and air bridges for capacitive matching.




(a) (b)

Figure 3.6: (a) Schematic of improved design with tuning stub, air bridge, and tapered bend. (b) IE3D plot of current distribution for 3-via interconnect.

Figure 3.6(a) shows the transition in a back-to-back configuration as has been measured, while Figure 3.6(b) shows the current distribution at 94 GHz. This transition has been modeled numerically using IE3D [132] showing 40 dB return loss and 0.2 dB insertion loss at 94 GHz (Figure 3.7).

A schematic of the entire back-to-back configuration is given in Figure 3.8. The calibration reference planes are shown as well as the placement of the air bridges, which vary in

[2]Patent pending. Co-inventors are Cheng P. Wen, Linda P.B. Katehi, Stephen Robertson, Katherine Herrick, Thomas Ellis, and Gabriel Rebeiz.

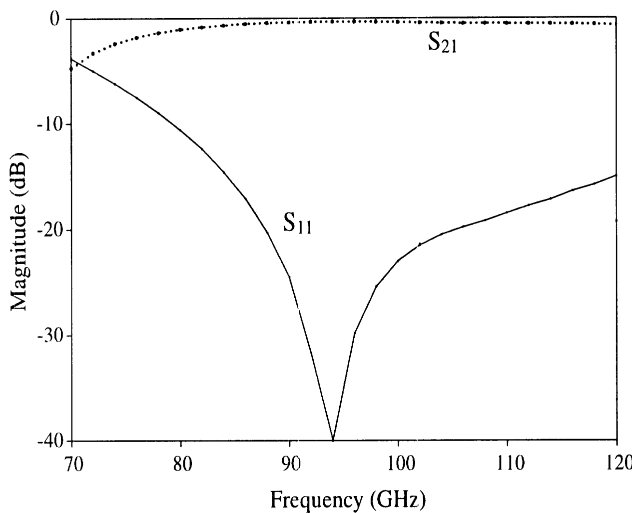
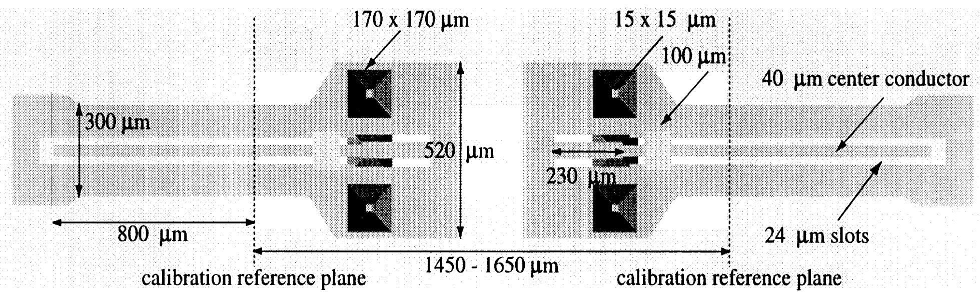
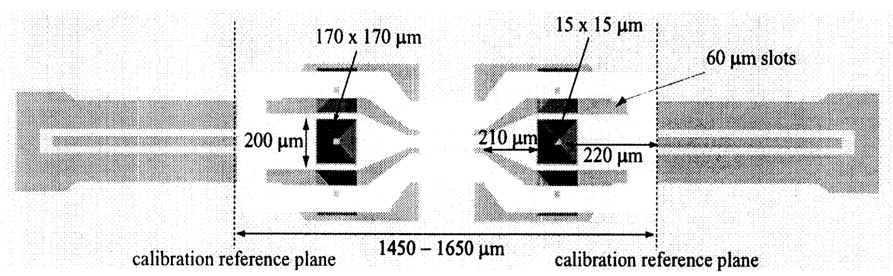



Figure 3.7: Simulated S-parameters for 3-via vertical interconnect.

width from 70-130 $\mu$m depending on the design. The FGC line has center conductor, ground plane, and separation widths of 40, 106, and 24 $\mu$m, respectively. The via dimensions are 170 x 170 $\mu$m at the large aperture and approximately 15 x 15 $\mu$m at the bottom.




(a)




(b)

Figure 3.8: Schematic of back-to-back vertical interconnect transition.

## 3.6 Fabrication Technique

The marriage of deep silicon micromachining and precision thin film lithography is complex because either electrical conductors and thin film microstructures must be protected from etch damage or a method of patterning over etched structures must be obtained. Fabrication of the vertical interconnect requires metallization of the planar silicon surfaces as well as in the vias themselves. Spinning photoresist over a micromachined silicon wafer yields a nonuniform photoresist layer, since the resist in the vias, or etched regions, spins outward forming a thick lip around the via opening, which then waves radially outward. Coverage becomes a problem because the liquid photoresist film withdraws itself from the edges due to surface tension. Additionally, the photoresist in the bottom of the via is difficult to develop. Ideally, a photoresist yielding conformal coating of three-dimensional silicon structures, such as an electrodepositable resist rather than a spun resist, seems well-suited to this type of project. Quite recently, the new negative electrodepositable photoresist made by Shipley (2100 ED), has shown great promise [72, 48, 61]. However, Fresnel diffraction and sidewall reflections make precision thin films more difficult to define. Other planarization methods for direct contact interconnects, such as a perforated silicon nitride membrane [114] are currently under development but have not been applied to measurable circuits thus far. For this project, standard fabrication and photolithographic techniques are used in a novel way.

The initial fabrication method involves metallizing the planar surfaces and vias separately. The circuit metal is evaporated, the vias are etched, and then silicon shadow masks are used to evaporate gold into the via regions (Figure 3.9). There are many problems associated with this method which are illustrated in Figure 3.10 and can be summarized as follows. First, it is difficult to achieve proper step coverage between the surface patterns and the via sidewalls. This is because a 0.5 $\mu$m layer of silicon dioxide lay underneath the 2 $\mu$m electro-plated Au surface patterns, necessitating a via sidewall thickness of 2.5 $\mu$m. The maximum allowable evaporated metal thickness is 1 $\mu$m. Second, the thickness of the via metallization worsened surface tension along the floor and sidewalls of the via, causing the metallization to pull up from the silicon base and sidewalls. Third, alignment for the

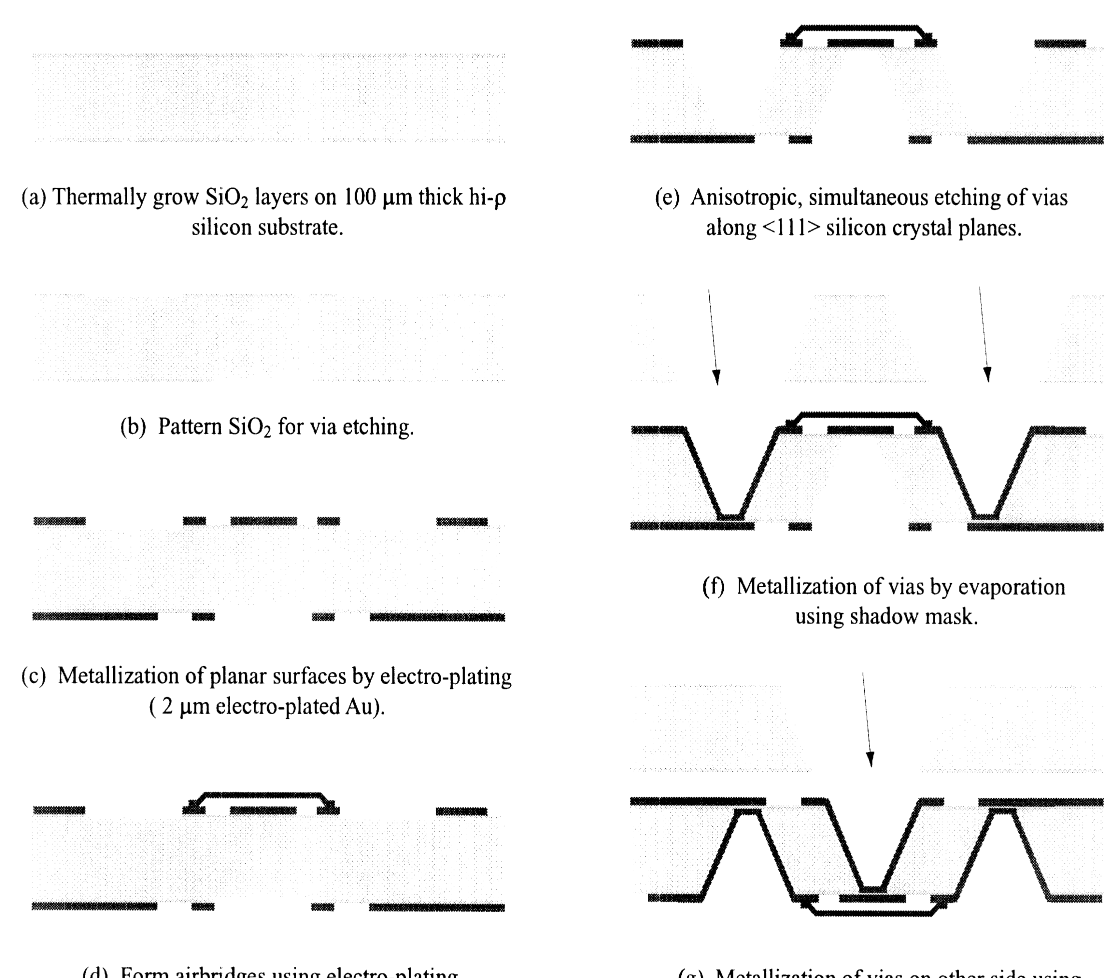



Figure 3.9: Initial fabrication process of vertical interconnects.

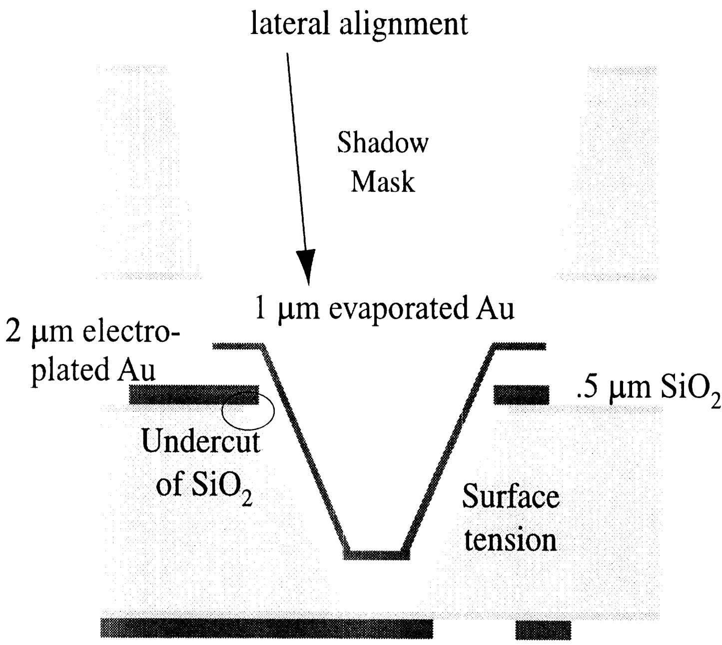
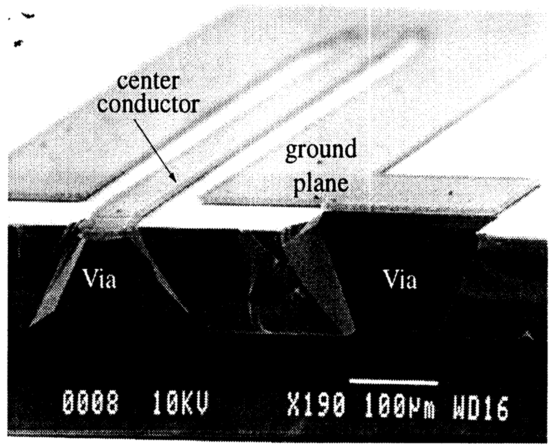



Figure 3.10: Illustration of fabrication problems.

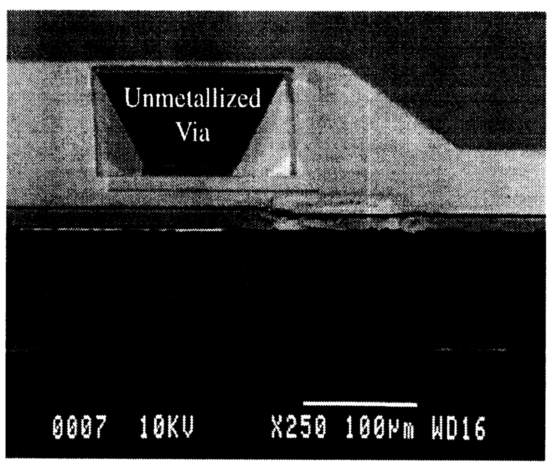
via metallization is attempted using a shadow mask, or another silicon wafer with via-sized apertures. This method proves to be difficult and inconsistent.

Scanning electron microscope (SEM) photos of the initial fabrication attempt are shown in Figures 3.11 and 3.12. Cross-sections both in width and length show the micromachined vias and surface metallization prior to via metallization in Figure 3.11. After via metallization using the shadow mask method, step coverage is insufficient as seen in Figure 3.12.

After many trials, a new method of three-via interconnect fabrication has been developed. This method has proven successful and repeatable compared with the previous process, eliminating the above problems by etching the vias first. After etching, the oxide is removed around the via and in its base. Then, using a modified lift-off technique, simultaneous metallization of surface patterns and vias may be achieved. This ensures both step coverage and sidewall adhesion, since only 1 $\mu$m of metal is required. Additionally, no shadow masks are needed for alignment, and consistent, repeatable photolithographic methods are used in its place. Thus, the new process has circumvented the problems of its predecessor, providing a successful fabrication method for the three-via interconnect.




(a) Cross-section along width of three-via interconnect.




(b) Cross-section along length of three-via interconnect.

Figure 3.11: SEM photographs of three-via cross-sections prior to via metallization.

The improved fabrication process flow is shown in Figure 3.13. First, a 6000 Å thick layer of thermal silicon dioxide ($SiO_2$) is grown on both sides of the 100 $\mu$m thick Si substrate (Figure 3.13(a)), and gold (Au) patches are defined where the via trenches will form (Figure 3.13(b)). The $SiO_2$ is then patterned to expose the Si to the anisotropic etchant (EDP or KOH) as shown in Figures 3.13(c) and 3.13(d). The etchant provides smooth sidewalls along the 54° $< 111 >$ crystal planes, with an undercut of approximately 2-5 $\mu$m. After

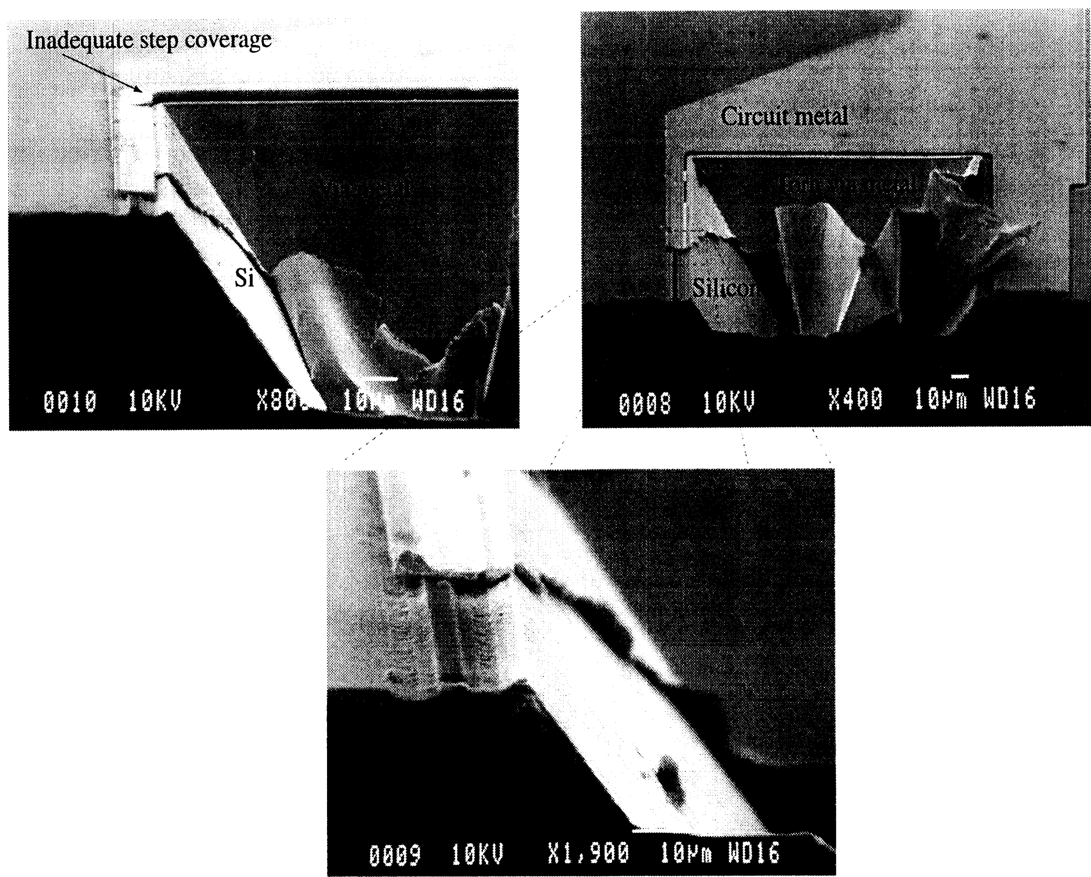



Figure 3.12: SEM photographs illustrating step coverage issues with shadow mask method of via metallization.

micromachining, the remaining $SiO_2$ is removed from the entire circuit, both on the surfaces and at the bottom of the vias (Figure 3.13(e)). At this point the 15 x 15 $\mu$m bottom of the via has only a 5000 Å thick Au layer across it. Simultaneous metallization of surface patterns and via sidewalls is obtained using a slightly modified lift-off technique (Figure 3.13(f)). Lastly, air bridges are added with 2.5 $\mu$m thick electroplated gold (Figure 3.13(g)).

Over seventy-two circuits have been fabricated with ninety percent yield, and a sampling of these circuits is shown in Figure 3.14. Top and bottom views of one back-to-back circuit are shown in Figure 3.15. Sufficient sidewall adhesion has been obtained as seen in Figure 3.16.

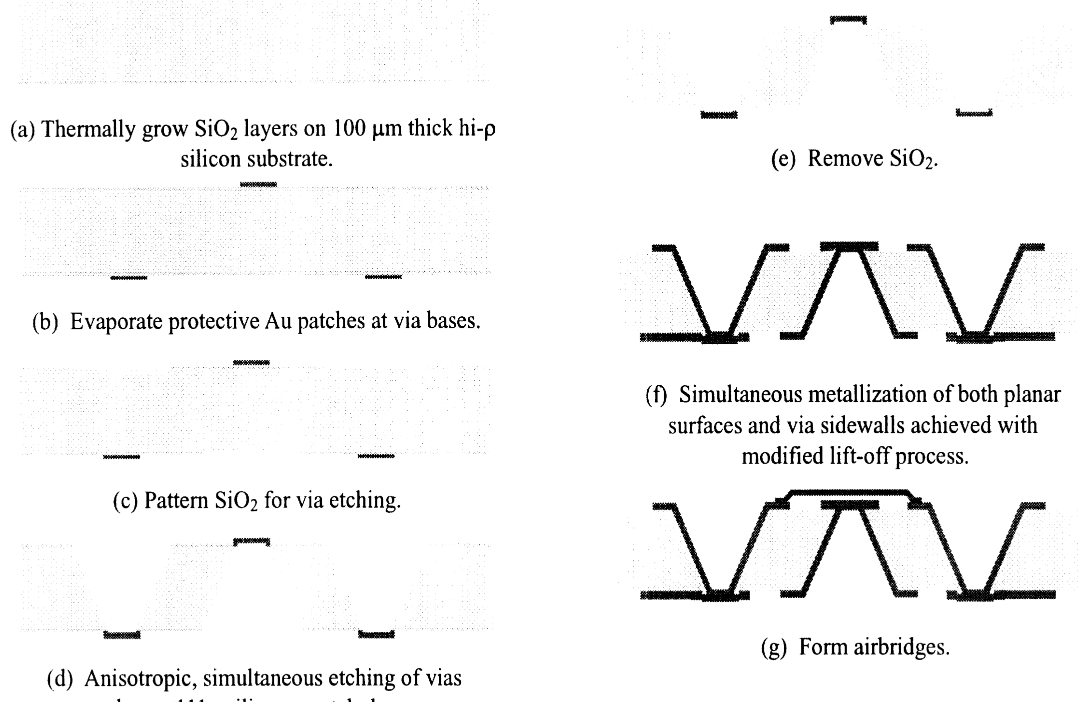



Figure 3.13: Final fabrication process for vertical interconnects.

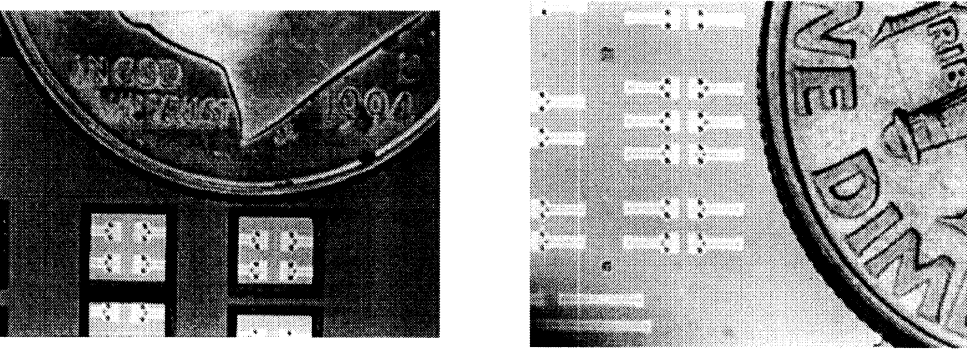
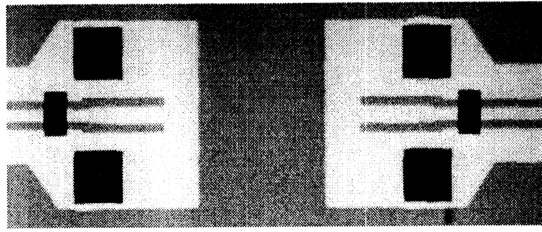
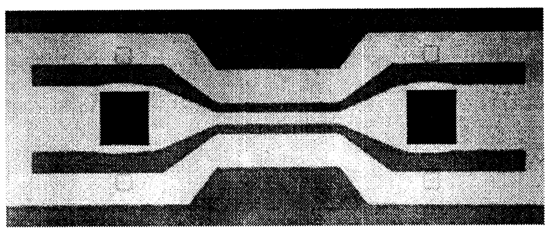


Figure 3.14: Top view of fabricated vertical interconnects as compared to a dime.



(a) Top view.



(b) Bottom view.

Figure 3.15: Photo of top and bottom of three-via back-to-back transition.

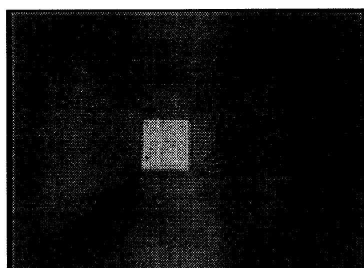


Figure 3.16: Close-up within metallized via.

## 3.7 Measured Results

S-parameters of the vertical interconnects have been measured on an HP 8510C Network Analyzer[3], using 150 $\mu$m pitch picoprobes[4] and the TRL calibration method to de-embed the probe-to-wafer transition and establish the measurement reference planes at the input and output ports of the circuits under test [70]. The interconnects are tested in a back-to-back configuration, with a short section of transmission line connecting them. Note the test circuits are placed on a Si support wafer, with micromachined openings underneath the back side of the transmission line.

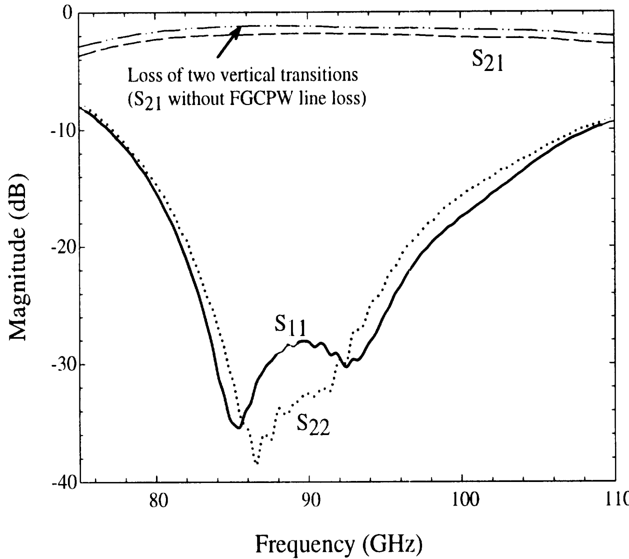



Figure 3.17: Measured S-parameters of back-to-back vertical interconnect transition.

Measured results from one of thirty-six different circuit designs are shown in Figure 3.17 for a back-to-back FGC three-via transition, with 1.72 dB insertion loss and 30 dB return loss at 90 GHz. The midsection length is 734 $\mu$m, the tuning stub is 220 $\mu$m, and the air bridge width is 100 $\mu$m. After accounting for the 0.6 dB loss of the FGC feeding lines, the loss due to each transition is approximately 0.55 dB from which 0.2 dB is attributed to radiation losses and 0.35 dB to ohmic losses. Considering that ohmic loss reduces as $\sqrt{f}$, the same transition designed for 30 GHz operating frequency, by changing the length of the

[3]Hewlett-Packard, Santa Clara, CA.
[4]GGB Industries, Naples, FL.

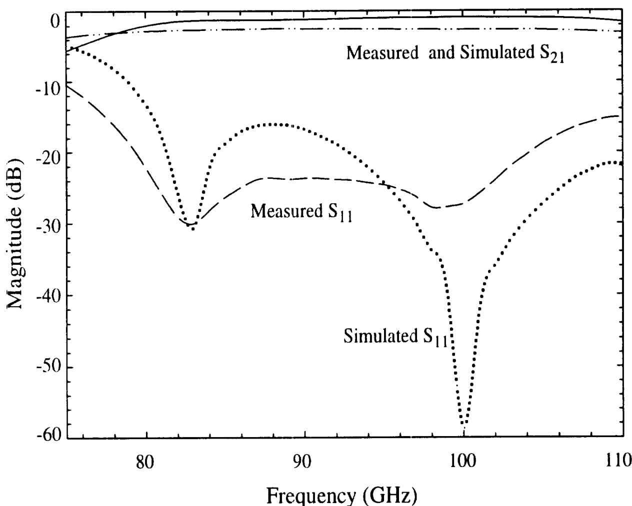


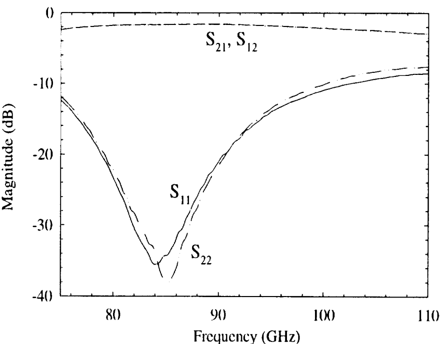

Figure 3.18: Measured S-parameters of back-to-back vertical interconnect transition compared with Libra model.

short circuit stub and the size of the capacitive bridge, would exhibit an insertion loss of less than 0.2 dB.

The double resonance is due to the two vias and the separation between the resonances is due to the midsection of line. Measured results from a different circuit in which the stub and air bridge dimensions are the same and the midsection is 200 $\mu$m longer are given in Figure 3.18, showing further separation of the resonances as expected. These results are compared with a Libra model showing a good match, and the ability to model and tune the resonances. Figures 3.19 and 3.20 show measured results from back-to-back designs with variations in midsection length, stub length, and air bridge width. Almost seventy circuits of similar dimensions were fabricated and tested with very similar and consistent results. Measured insertion loss ranges between 1.7 and 2.2 dB for the individual back-to-back transitions, which corresponds to 0.5 -0.7 dB loss per interconnect.

## 3.8 Design

Modeling of the via structure is very difficult in terms of RLC discrete elements due the intertwining and interrelating of the vias, air bridge, tapered bends, and surrounding transmission lines. In order to explain trends of modifications in the air bridge and stub



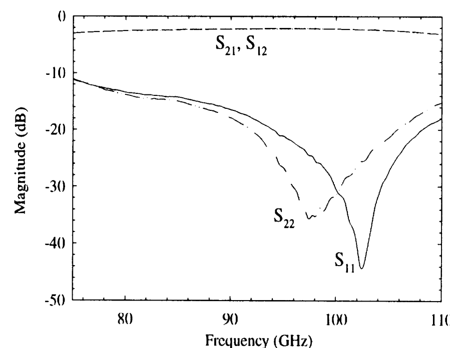
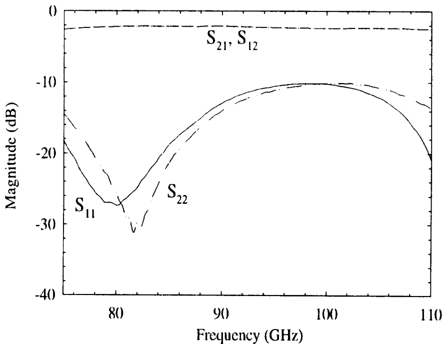




Figure 3.19: Measured S-parameters of back-to-back vertical interconnects: a) 734 $\mu$m midsection, 230 $\mu$m stub, and 100 $\mu$m air bridge. b)934 $\mu$m midsection, 240 $\mu$m stub, and 130 $\mu$m air bridge.



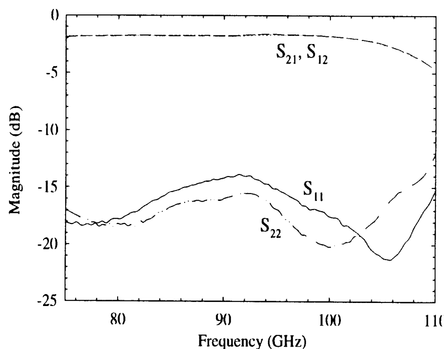




Figure 3.20: Measured S-parameters of back-to-back vertical interconnects: a) 934 $\mu$m midsection, 230 $\mu$m stub, and 100 $\mu$m air bridge. b)734 $\mu$m midsection, 240 $\mu$m stub, and 130 $\mu$m air bridge.

tuning parameters, the via structure is simulated with stubs lengths ranging 220-240 $\mu$m and air bridges ranging 70-130 $\mu$m. The general trend is to decrease the stub length (decrease the series inductance) and increase the air bridge width (increase the shunt capacitance) to achieve higher resonant frequencies. In order to present a set of design rules, tabular information is given concerning capacitance of air bridge, stub length, and micromachined via dimensions.

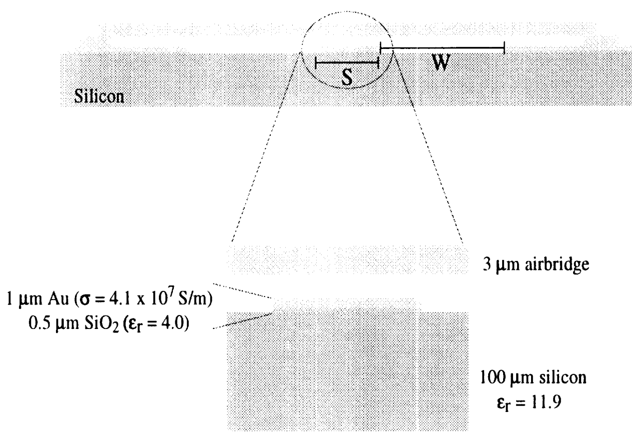



Figure 3.21: Cross section of air bridge over FGC line.

The increased capacitance due to loading by an air bridge is determined using a static solver and the cross section of the geometry as shown in Figure 3.21 [5]. From the capacitance per unit length of the cross-section, the capacitance of the air bridge is determined simply by multiplying by the width of the bridge. This has shown to be a highly effective model due to the static behavior of the fields around the air bridge (See Appendix A). Table 3.2 gives example capacitive values in addition to the effective dielectric constant and impedance of an FGC section of line with and without an air bridge. Thus a 70 $\mu$m bridge over this particular FGC line represents 19.4 fF, while a 130 $\mu$m bridge yields 36 fF.

Table 3.2: Results of air bridge capacitive modeling using 2-D static solver [5].

| FGC dimensions ($\mu$m) | Capacitance (F/m) | $\epsilon_{eff}$ | $Z_o$ ($\Omega$) |
|---|---|---|---|
| 40-24-106 | $1.47\times10^{-10}$ | 6.2 | 53 |
| 40-24-106 with bridge | $3.30\times10^{-10}$ | 1.89 | 13.89 |

To assist in stub tuning, Table 3.3 gives the length of quarter wave stub sections required for tuning frequencies from 30-100 GHz. Note that the reported stub lengths for the 94 GHz transition are about 50 $\mu$m less than a quarter wavelength because it is the length taken from a known point on the via (the edge) to the end of the stub. Since anisotropic etching is used, the size of the via is dictated by the 54° angle of the $< 111 >$ Si crystal planes as well as the thickness of the silicon. Table 3.4 shows the larger via dimensions required for

Table 3.3: Length of quarter wavelength tuning stub for FGC on Silicon with effective dielectric constant of 6 as a function of frequency.

| Frequency (GHz) | Stub length ($\mu$m) |
|---|---|
| 30 | 1020 |
| 40 | 765 |
| 50 | 612 |
| 60 | 510 |
| 70 | 437 |
| 80 | 382 |
| 90 | 340 |
| 100 | 306 |

Table 3.4: Anisotropically micromachined via dimensions for different silicon thicknesses with 10 x 10 $\mu$m via base.

| Substrate thickness ($\mu$m) | Via dimensions ($\mu$m) |
|---|---|
| 50 | 80 x 80 |
| 70 | 110 x 110 |
| 100 | 150 x 150 |
| 200 | 290 x 290 |
| 400 | 576 x 576 |
| 500 | 708 x 708 |

a via base of 10 x 10 $\mu$m as a variation of substrate thickness.

## 3.9 Conclusions

On-wafer S-parameter measurements of W-band vertical interconnects have been demonstrated, confirming that silicon micromachining techniques can be used to create a very compact 3-via interconnect between FGC lines on opposite sides of a Si substrate. These

vertical transitions provide approximately 0.5-0.7 dB of loss, which compares well to simulated results. In addition, the approach is shown to be compatible with MMIC technology which may assist in the utilization of high density multi-level integration schemes.

As multi-layer structures become a desirable means of achieving high-density integrated circuits, vertical interconnects become critical to their success. Criteria upon which to evaluate a vertical interconnect include loss, bandwidth, transmission efficiency, size, and ease of fabrication. Particularly at W-band, the added discontinuities of any vertical transition make low loss and wide bandwidth more challenging goals, and the transition may be coupled through a substrate electromagnetically or with direct contact. Although both electromagnetically (EM)-coupled transitions and direct contact (DC) transitions require double-sided processing, direct contact transitions have the added complexity of a through-hole. Clearly, there is a need for W-band interconnects of either EM-coupled or DC form. While our efforts have concentrated on direct contact interconnect, Gauthier *et al.* have developed and measured both CPW and microstrip overlay em-coupled designs at W-band [34]. Although the EM-coupled designs are comparable in loss and simpler to fabricate, they require over twice the real estate. The smaller size of the 3-via direct contact interconnect presented in this chapter makes it the most viable candidate for high density applications such as the power cube project presented in Chapter 6.

# CHAPTER 4

# TWO-LAYER WAFER-TO-WAFER TRANSITION

## 4.1 Introduction

In addition to vertical transitions through a single silicon (Si) wafer, multilayer designs must provide an avenue for high-frequency signals to flow from wafer to wafer. For this purpose, a two-layer electrical bond is proposed to provide electrical connection between two finite ground coplanar (FGC) waveguides on vertically stacked silicon substrates. Essentially, a FGC line on one wafer connects vertically to another wafer with electroplated gold (Au) pads on its center conductor and ground planes. The FGC line is surrounded and protected with micromachined shielding cavities. Insertion loss of approximately 0.1 dB is measured for this compact transition at W-Band.

## 4.2 Motivation

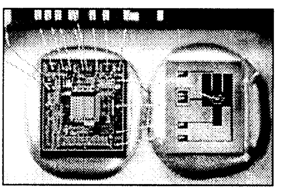
Wafer bonding has been used commercially in applications such as power devices, silicon on insulator (SOI), sensors, die attachments, hermetic sealing, and other MEMS applications [128, 129, 75, 107]. Its use has become prevalent due to the many technical and economic advantages afforded. For example, specialty wafers may be used for some devices while silicon may be used for the main circuitry, and fabrication compatibility issues may be circumvented by processing separate wafers. Commercially, these advantages translate to economic benefits as well, since well-founded processing lines need not be disrupted.

There are three main classes of bonding: anodic, fusion, and intermediate. Anodic

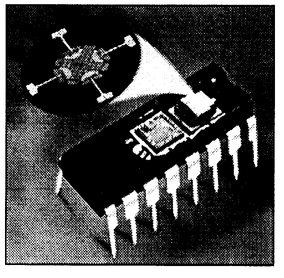
bonding involves glass to silicon bonding at temperatures up to 500 °C and potentials between 100 Volts-1 Kilovolt. A negative potential is applied to the glass wafer which typically has a high content of alkali metals. Under the negative potential, these metals become mobile, ionize, and form a space charge at the wafer interface. This creates a strong electrostatic attraction and holds the wafers in place. Increasing the temperature up to 500 °C increases the alkali metal ion mobility while oxygen, also from the glass, is transported by the applied electric field to the wafer interface. The oxygen reacts with silicon and forms $SiO_2$ creating a permanent bond. An application of this process is shown in Figure 4.1(a), a sensor chip for Ford's MEMS automotive airbag accelerometer.

The second main class of bonding, fusion bonding, is also known as silicon-to-silicon direct wafer bonding (DWB) and requires either hydrophobic or hydrophilic silicon surfaces be brought into contact and annealed at temperatures up to 1000 °C. In the hydrophobic case, a van der Waals force creates the initial pre-bond. However in the hydrophilic case, hydrogen oxide (OH) facilitates the pre-bond. Although the high temperatures required for this bond make it incompatible with microelectronic circuits, it is currently used for multiwafer microstructures like accelerometers and other microstructures, such as the Massachusetts Institute of Technology's (MIT's) micromachined turbine (Figure 4.1(c)). Intermediate bonding, the third class of bonding, involves bonding wafers with an intermediate film be it glass (glass-frit bond example shown in Figure 4.1(b)), polymer-based, or metal. Glass-frit bonding temperatures are generally 400-500 °C and, like all spin-on processes, thickness control is an issue. In intermediate metal-based bonding, various metals have been applied such as Ti, $TiSi_2$, PtSi, and $CoSi_2$ [128] with reported bond temperatures up to 700 °C.

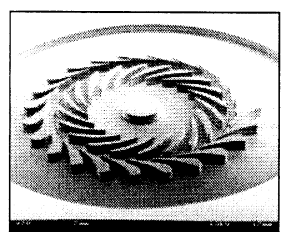
High temperature wafer-to-wafer bonding, such as anodic, fusion and glass-frit bonding mentioned above, may be deleterious to complex circuits by allowing dopant diffusion, reducing conductivity, and/or modifying physical circuit dimensions. Thus there is a need to develop a low-temperature wafer-to-wafer bond that allows mating of micromechanical structures and other complex circuits without compromising electrical performance. Low-temperature wafer bonding has been under study mainly for die attachment and electrical interconnects with the bulk of research centered on the eutectic temperature [129, 128, 107].



(a) Anodic Bonding



(b) Glass-Frit Bonding



(c) Fusion Bonding [64]

Figure 4.1: Three examples of commercial wafer bonding applications a) Sensor Chip for Ford MEMs automotive airbag accelerometer b) Sensor Chip for Motorola micromachined automotive airbag accelerometer c) Micromachined turbine from MIT's Micro gas turbine engine [116].

Of the eutectic-solder based bonding, eutectic gold wafer bonding has been most highly promoted due the low minimum liquidus temperature and widespread use in die bonding. However, these bonding studies, by Wolfenbuttel and Tiensuu for example [129, 128, 107], focus on the bond itself and ascertain bond quality through visual inspection of grain boundaries or load measurements. Measurements including the bond are not performed thus conductivity is not a consideration in these studies. Unlike many previous wafer-to-wafer silicon-gold bond investigations, the goal of this work is not only to develop a low-temperature gold-to-gold wafer bond but to develop an RF electrical connection from one silicon wafer to another at W-band.

## 4.3 Design

Figure 4.2 illustrates the transition concept and measurement method as a back-to-back configuration in which a single FGC line transitions from lower to upper wafer, shifting again to the lower wafer for on-wafer probing. Probe windows are micromachined through the upper 100 $\mu$m wafer, and 40 $\mu$m air cavities are micromachined around the FGC line for protection. The lower (AA') and upper (CC') FGC cross-sections have dimensions of 40-24-106 $\mu$m (S-W-$W_g$) and line thickness of 1 $\mu$m while the transition region (BB') includes

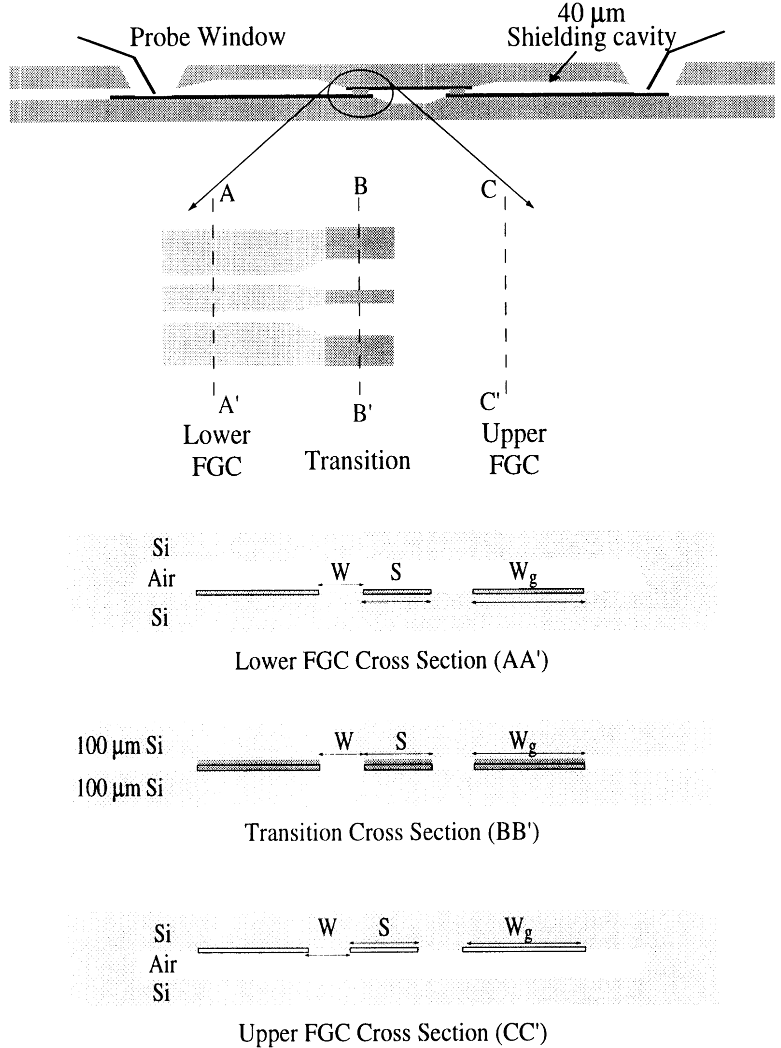



Figure 4.2: Illustration of wafer to wafer transition.

an additional 3 $\mu$m of gold on both sides to ensure wafer-to-wafer contact. Once in contact, the gold of BB' is 8 $\mu$m tall and sandwiched between the silicon wafers, thereby changing the shunt capacitance, effective dielectric constant, and characteristic impedance of the line. To design a transition with good RF performance at W-band, the transition geometry must be modified to preserve the original 50 $\Omega$ characteristic impedance.

Electro-static simulations show that a 50 $\Omega$ line may be achieved in the transition region (BB') by making minor changes to the FGC feed line dimensions [5]. Figure 4.3 illustrates the two dimensional cross-section modeled. The capacitance is computed twice for the FGC mode of interest: once as shown in Figure 4.3, producing $C_{sub}$, and once with all substrates

replaced with air ($C_{air}$). For the FGC mode, a 1 V bias is applied to the center conductor, and 0 V is applied to the ground planes. The effective dielectric constant and characteristic impedance are calculated using Equations 4.1 and 4.2 where $v_o$ is the speed of light. As shown in Table 4.1, line characteristics for the feed and three 50 Ω transition geometries are shown. Note, all transition geometries yield $\epsilon_{eff}$ between 9-10, while that of the feed line is 6.3.

$$\epsilon_{eff} = \frac{C_{sub}}{C_{air}} \tag{4.1}$$

$$Z_o = \frac{\sqrt{\epsilon_{eff}}}{v_o C_{sub}} \tag{4.2}$$

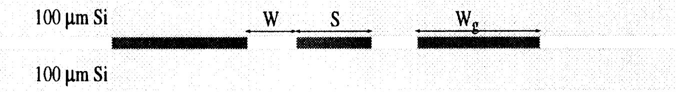


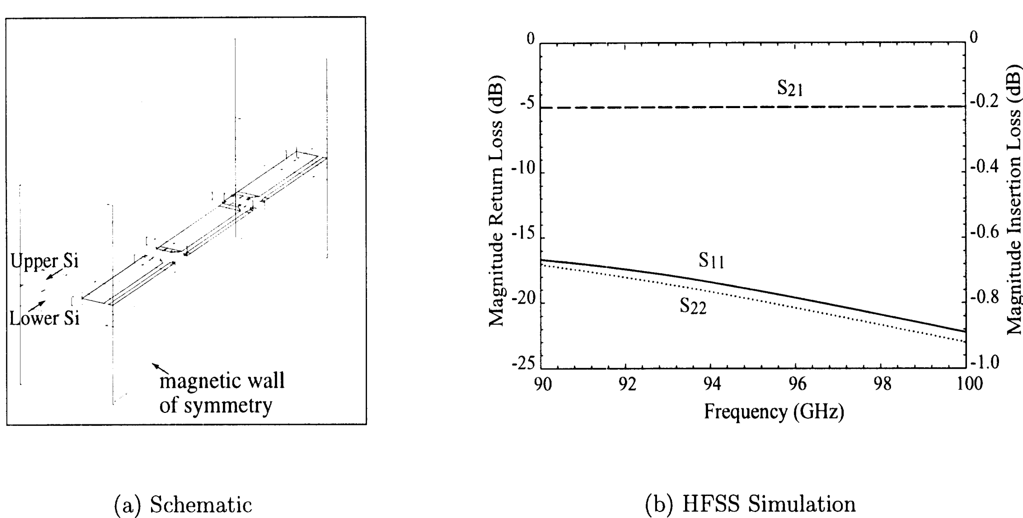

Figure 4.3: Schematic for Maxwell 2D RF interconnect simulation.

Table 4.1: Characteristics of feed line and transition geometries.

| | Feed Line (AA',CC') (40-24-106 μm) | Trans 1 (BB') (20-44-100 μm) | Trans 2 (BB') (30-59-100 μm) | Trans 3 (BB') (40-65-100 μm) |
|---|---|---|---|---|
| Gold (μm) | 1 | 8 | 8 | 8 |
| Upper Si | no | yes | yes | yes |
| $C_{sub}$ (F) | $1.7\times10^{-10}$ | $2.14\times10^{-10}$ | $2.1\times10^{-10}$ | $2.15\times10^{-10}$ |
| $C_{air}$ (F) | $2.7\times10^{-11}$ | $2.22\times10^{-11}$ | $2.12\times10^{-11}$ | $2.15\times10^{-11}$ |
| $\epsilon_{eff}$ | 6.3 | 9.6 | 9.9 | 9.9 |
| $Z_o$ (Ω) | 49.9 | 48.4 | 50 | 48.8 |

Full-wave FEM analysis of the back-to-back transition for the three transition geometries indicates similar insertion and return losses [4]. The total circuit length for all simulations is 1820 μm with two 100 μm long transition sections. For example, the simulation for the 30-59-100 μm transition, using a magnetic wall for symmetry, indicates insertion and

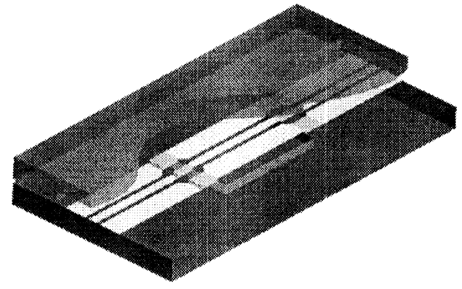
return losses of 0.2 dB and 18 dB, respectively, as shown in Figure 4.4. Since no ohmic loss is included here, the 0.2 dB insertion loss indicates 0.1 dB loss per transition due to mismatch. The full geometry is analyzed considering finite conductivity of $4.1 \times 10^7$ Siemens/meter, and results in insertion and return losses of 0.85 and 20 dB, respectively. The geometry is shown in Figure 4.4(a), with a curved cut-out of the upper silicon wafer for view of the transition. The simulated S-parameters of the 30-59-100 $\mu$m transition are shown in Figure 4.5 in addition to the S-parameters of a through line of the same length. The difference in insertion loss between the back-to-back transition and the through line is 0.166 dB, implying 0.083 dB insertion loss per transition. Simulations for the back-to-back 40-65-100 $\mu$m and 20-44-100 $\mu$m transitions yield similar results of 0.82 dB and 0.77 dB insertion losses with 20.13 dB and 22.55 dB return losses at 94 GHz, respectively, as shown in Figure 4.6. As compared to the through line, the loss of the 40-65-100 $\mu$m transition is 0.068 dB, and the loss of the 20-44-100 $\mu$m transition is 0.043 dB. Table 4.3 summarizes these results, showing estimated loss of each of the three transitions to be <0.1 dB.



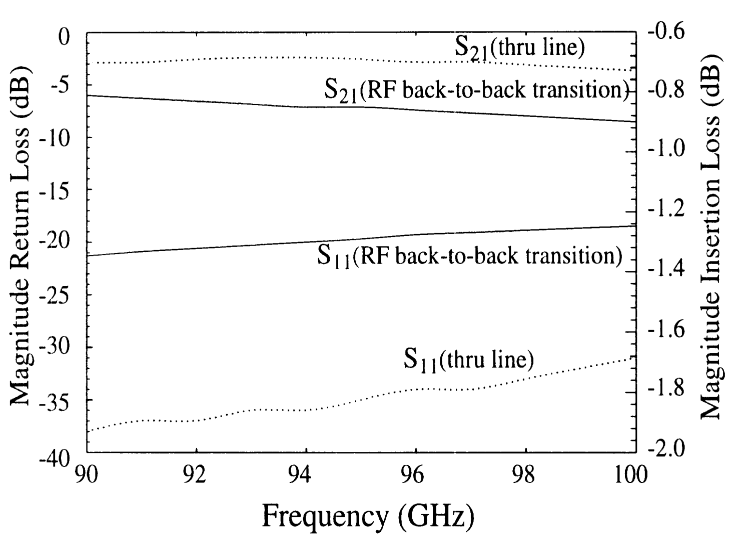

(a) Schematic

(b) HFSS Simulation

Figure 4.4: HFSS simulation results for RF back-to-back interconnect with 30-59-100 $\mu$m transition. The geometry is cut lengthwise through the center conductor and a magnetic wall is used for symmetry. Perfect conductors are used. (a) Schematic (b) Simulated S-parameters

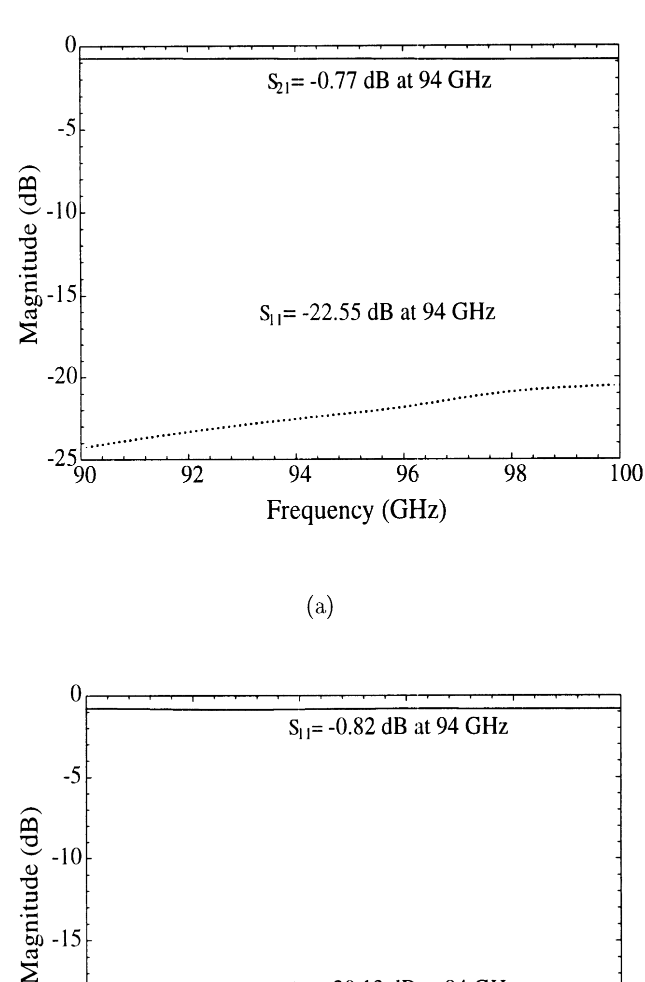


(a) Schematic




(b) HFSS Simulation

Figure 4.5: HFSS simulation results for RF back-to-back interconnect with 30-59-100 $\mu$m transition as compared with through line of same length. Finite conductivity of $4.1 \times 10^7$ Siemens/meter is used. (a) Schematic (b) Simulated S-parameters




(a)



(b)

Figure 4.6: HFSS simulation results for RF back-to-back interconnect with (a) 20-44-100 $\mu$m and (b) 40-65-100 $\mu$m transition.

Table 4.2: Back-to-back RF wafer-to-wafer transition simulation summary.

| Simulation | Figure | Insertion Loss ($S_{21}$) dB | Return Loss ($S_{11}$) dB | Transition Loss dB |
|---|---|---|---|---|
| 30-59-100 | 4.4(b) | 0.2 | 18 | 0.1 |
| Through | 4.5(b) | 0.684 | 36 | n/a |
| 20-44-100 | 4.6(a) | 0.77 | 23 | 0.043 |
| 30-59-100 | 4.5(b) | 0.85 | 20 | 0.083 |
| 40-65-100 | 4.6(b) | 0.82 | 204 | 0.068 |

## 4.4 Fabrication

Fabrication involves two-sided processing, probing windows, finite ground coplanar air cavities, and alignment marks. The fabrication process flow includes fabrication of the upper and lower 100 $\mu$m high-resistivity (3000 $\Omega$-cm) silicon wafers with thermally grown $SiO_2$ on both sides. Although fabrication details are given in the appendices, a fabrication summary is given here.

As shown in the right column of Figure 4.7, the lower wafer fabrication begins with metallization of the frontside alignment marks and circuit metal using lift-off of Chrome/Gold (Cr/Au) (500/9500 Å). Oxide is then patterned for cavities using buffered hydrofluoric acid (BHF) at an etch rate of 1000 Å/min. Electroplating of the RF interconnects commences with patterning a thin photoresist layer, after which a seed layer of Cr/Au/Cr (500/1000/500 Å) is flood evaporated, patterned, and electro-plated in a cyanide based solution to approximately 3 $\mu$m. Removal of the seed layers completes the RF interconnect formation, and the final step is to anisotropically etch the oxide-patterned cavities in Potassium Hydroxide (KOH) to a depth of 40 $\mu$m.

The upper wafer is fabricated in a similar manner and allows for probe windows for measurement as illustrated in the left column of Figure 4.7. After metallization of frontside alignment marks using lift-off of Cr/Au (500/2000 Å), oxide is patterned for the probing windows. These two processes are repeated on the backside of the wafer using infrared (IR) alignment, with protective cavities patterned in addition to probing windows. Electroplating of the RF interconnects is completed using the same method described for the lower wafer, and the oxide-patterned cavities and probe windows are anisotropically etched in KOH. In this case, the probe windows must be etched through the 100 $\mu$m wafer and the cavities need only be etched 40 $\mu$m. For this reason, the choice of KOH becomes useful as it etches oxide at a rate of 14 Å/min or 840 Å/hour, allowing a thin film of oxide to protect the cavity regions from the etchant until 60 $\mu$m is etched in the probe window regions. In this way two different etch depths may be obtained during one etch.

There are two wafer fabrication processes that may affect alignment and bonding of the upper and lower wafers. The first is electroplating and the issue is the ability to uniformly

Upper Wafer

(a) Thermally grow $SiO_2$ layers on 100 μm thick hi-ρ silicon substrate

Front

Back

(b) Metallization of alignment marks

(c) Oxide patterning

(d) Metallization of backside alignment marks

(e) Partial oxide patterning

(f) Circuit metallization

(g) Electroplating of RF interconnects

(h) KOH etch of probe windows and cavities

Lower Wafer

(a) Thermally grow $SiO_2$ layers on 100 μm thick hi-ρ silicon substrate.

Front

Back

(b) Metallization of circuit metal and alignment marks

(c) Oxide patterning for cavity

(d) Electroplating of RF interconnects

(e) KOH etch of cavity

Alignment of top and bottom wafers forms RF interconnects.

Figure 4.7: Fabrication of Upper and Lower 100 $\mu$m silicon wafers for RF interconnects

control the electro-plated bump height. Electroplating solution, current, wafer placement, and cleanliness are all contributing factors. As observed experimentally, the estimated electroplated ripple is $\pm$ 0.3 $\mu$m. The second process is wafer alignment from one side to the other and is achieved using conventional infrared (IR) alignment techniques in which

typical IR alignment error is $\pm$ 5 $\mu$m. Special attention is given to both the electroplating and IR alignment steps to ensure wafer-to-wafer contact and alignment.

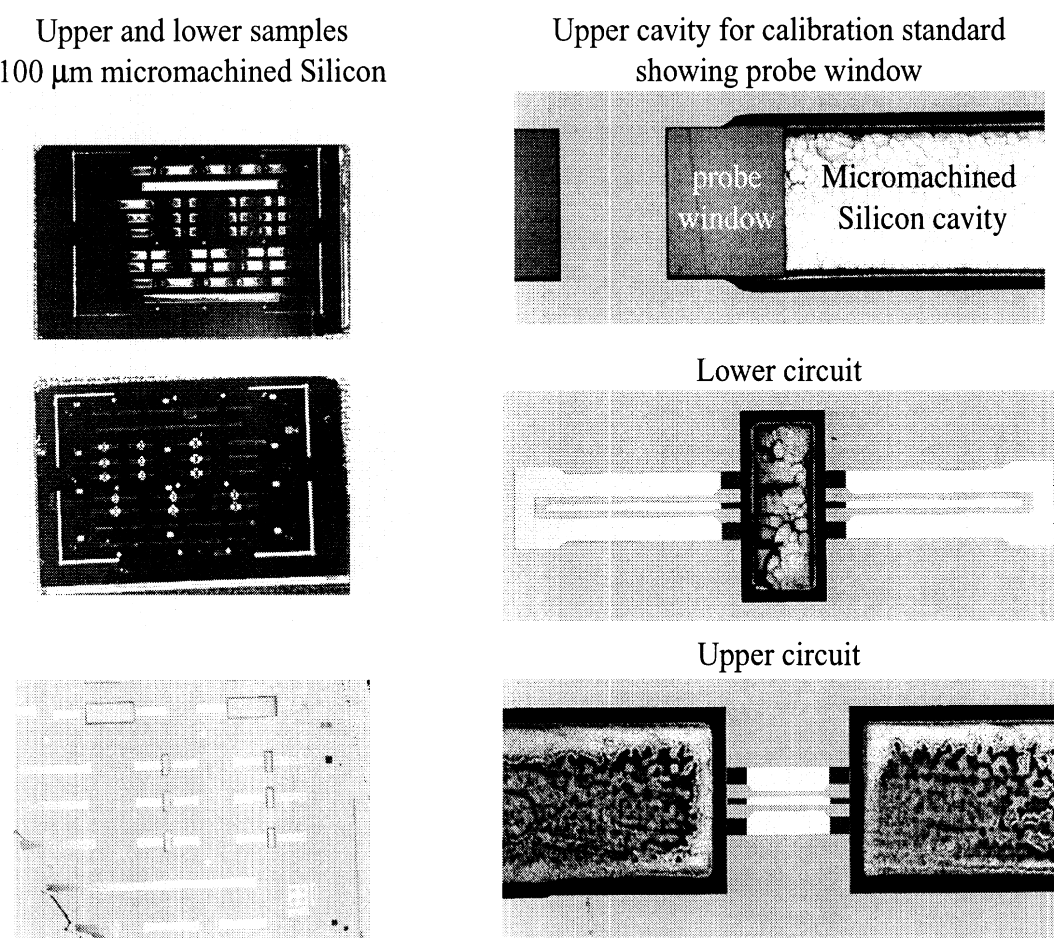



Figure 4.8: Photos of fabricated circuits.

Photographs of fabricated circuits are seen in Figure 4.8. The left column shows the upper and lower 100 $\mu$m silicon samples of dimensions 0.75 by 1.25 inches, as well as a close-up of the lower wafer. The right column of Figure 4.8 displays an upper micromachined air cavity for a calibration through line. The probing window, which allows probing through the 100 $\mu$m upper wafer to the circuit on the lower wafer, is also shown. A close-up of one RF wafer-to-wafer transition is also shown as a combination of the upper and lower wafers.

## 4.5 Wafer Alignment and Thermocompression Bonding

### 4.5.1 Theoretical Considerations

There are essentially three silicon wafer-to-wafer bonding techniques as mentioned in the introduction: anodic, direct, and intermediate-layer bonds. The latter technique includes bonding with polymer glue, soft glass, or metal. The bonding process for all techniques may be summarized as a three-step sequence: surface preparation, contact, and annealing. The first step is important since the quality of the bond has a strong dependence on surface conditions. Intimate contact is made, after proper alignment, using pressure, which is followed by increased temperature. The type of bonding examined here may be categorized as intermediate-layer bonding, with the intermediate layer being gold, and, as reported in the literature [2, 107, 128, 129, 101, 109], has been referred to as thermocompression bonding, solid state welding, diffusion welding, and eutectic brazing. The formation of a solid state bond between joining metals is the common denominator. Hereafter, the bonding discussed and presented will be referred to as thermocompression bonding.

In thermocompression bonding, time, temperature, and pressure coalesce the base metals at temperatures below their melting point or melting range. While in intimate contact at the bonding temperature, atoms in the metal acquire increased energy, and after a specified period of time, the transport of atoms across the original interface results in a solid state bond. As thermocompression bonding involves a range of temperatures, pressures, and deformations, it is difficult to present one comprehensive theory of the process. However, it is worthwhile to list and consider factors that may contribute to the process. In doing so, the reasoning for the temperature, time, and pressure for the wafer-to-wafer transition of interest will be clarified.

#### Forces of Attraction

To obtain adhesion, the two metallic surfaces, both gold in this case, must be close enough together to become mutually attractive. The problem is to determine the nature of these forces. Metals are characterized by their high thermal and electrical conductivities. Neither covalent (shared electron pairs) nor ionic (unlike charges) bonding is realized

because both types localize the valence electrons and preclude conduction. Strong bonding does exist, however, and can be explained by viewing the metal as a periodic structure of positive ions surrounded by a sea of electrons which are free to move unrestricted. The attraction between the positive ions and the free electrons provides the bond. In the case of gold with its face-centered cubic (fcc) structure, the approximate atomic radius is 1.22 Å and approximate ionic radius is 1.37 Å. The attractive force is proportional to the inverse of the square of the distance. For these normal cohesive forces of metals to be utilized in thermocompression bonding, the surfaces must be clean and brought to very intimate contact on the order of 10-30 Å. A longer range force is the van der Waals force of attraction in which an interatomic dipole is created when moving electrons create an excess of electrons on one side of the nucleus and a deficit on the other. Two atoms may be attracted to the other when atomic dipoles are created, however this attractive force falls off as the inverse of the seventh power of the distance. Compared to the adhesion forces in gold, the van der Waals forces are quite small and are probably insignificant contributors to thermocompression bonding. Thus the attractive forces used in thermocompression bonding are mainly those from the normal cohesive forces in metals.

To take advantage of these attractive forces, the metals must be placed in intimate contact, using pressure for example. However, pressure alone, causing both plastic and elastic deformations, is not sufficient for bonding at room temperature. One reason for this may be surface contaminants, to be discussed in a following section. Another means of bringing the atoms in close enough contact is through diffusion. As temperature is increased and the metallic atoms vibrate more energetically, a small fraction of them will relocate in the lattice. In addition to temperature, the fraction of relocating atoms depends also on how tightly the atoms are bound. The amount of energy required for an atom to change position is called the activation energy, Q (cal/mol). $D_o$ and Q are temperature independent, R is the gas constant and T is the absolute temperature. Many experimental studies [13, 109] have shown the complexity in determining a single activation energy value, and of the various diffusion mechanisms that may contribute to thermocompression bonding, volume, grain boundary, and surface diffusion mechanisms have been examined. As an additional complexity, although most data relating to self-diffusion in pure metals can be linked to

a vacancy mechanism [101, 109, 13], an atom may diffuse as an interstitial impurity as well. Thus it is difficult to know apriori the amount of energy required for atomic diffusion. However, it is clear that cohesive metallic forces are needed for strong thermocompression bonding, and that both pressure and temperature are required. What still needs to be determined is the appropriate ranges of each.

### Pressure

As it is known, increasing pressure increases the amount of contact between the gold atoms. However some of the limiting factors are fracture of the silicon substrates and equipment threshold. The silicon wafers used in this research effort have been thinned, from a conventional thickness of 500 $\mu$m, to 100 $\mu$m resulting in a more fragile sample. Also, applying pressure to a plate, as on a bonding machine, that is not perfectly flat may cause that plate to stress fracture. Work at the Massachusetts Institute of Technology (MIT) on thermocompression bonding [6] has been conducted on 4 inch silicon wafers with thin lines of evaporated gold. Their as yet unpublished work focuses on full thickness, 4 inch silicon wafer thermocompression bonding using Electronics Visions bonding equipment [116] and bond strength evaluation. The pressure used by Dr. Ayon [6] is on the order of 5 mbar, and this value is used for reference. The samples for the RF interconnect measurements are only approximately one inch square thus the pressure needs to be scaled down appropriately. However, equipment limitations also play a role in the applied pressure.

### Temperature: The Role of Diffusion

Increasing temperature enhances the diffusion mechanisms present in the gold atoms. However, it is important to consider other materials present, and how they will be affected by increases in temperature. In this case, the main concern is silicon, and its eutectic point is shown in the silicon-gold phase diagram of Figure 4.9, which indicates the lowest melting temperature. The silicon-gold alloy is formed by solid-liquid interdiffusion at the interface, followed by solidification upon cooling. This point is located at 363 °C for gold-silicon and corresponds to a eutectic composition of 2.85 % Si and 97.1 % Au by weight.

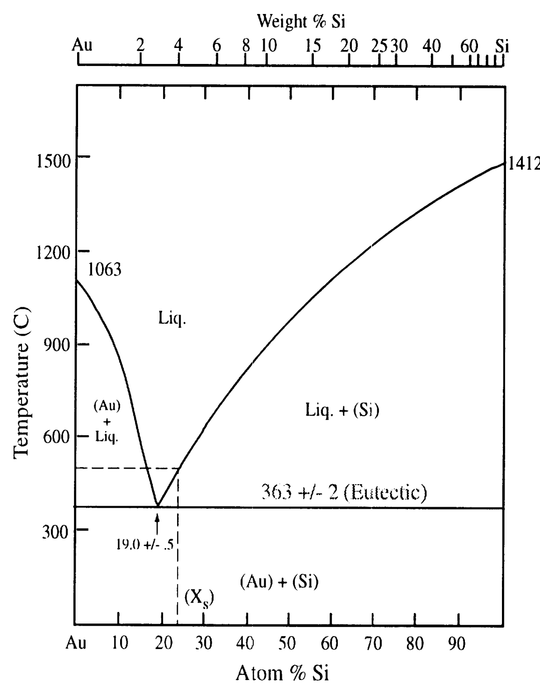



Figure 4.9: Phase diagram for Au-Si [37]

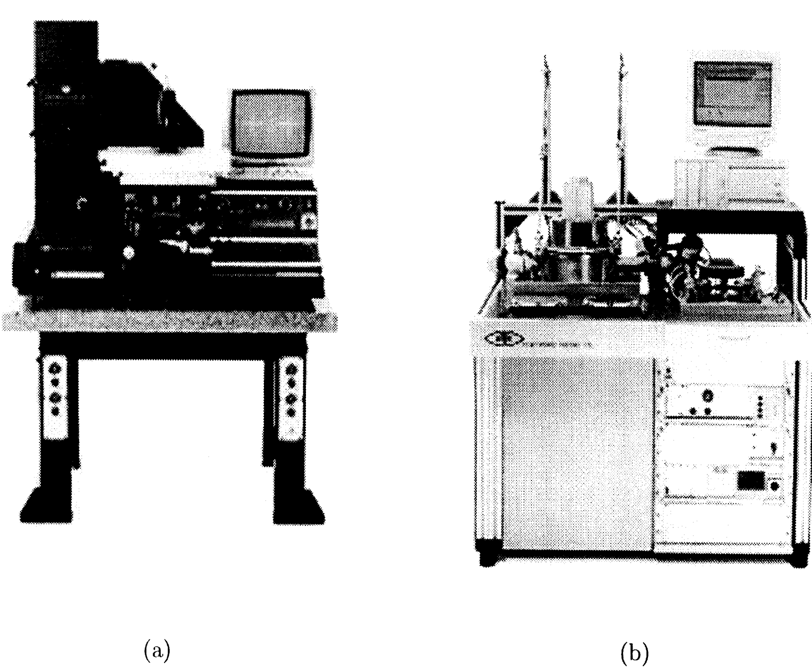
Eutectic bonding is currently used for die bonding and multi-wafer assembly [107, 128, 129] as an alternative to high-temperature bonding. However, to maintain purity and highest conductivity of the gold electrical contacts, which are part of the circuits themselves, it is highly undesirable to allow silicon diffusion into the gold or vice-versa. Additionally, it is important to maintain the dimensions of the gold lines, as they define the characteristic impedance. For this reason, the bonding temperature for the gold-to-gold diffusion is kept to 350 °C, 13 °C below the eutectic.

### Effect of Surface Contaminants

Since it has been experimentally shown that deformation welding generally produces sufficient intimate contact for a metallic bond, it may be concluded that surface films and contaminants are responsible for failed bonding attempts [55, 56]. There are two general groups of surface films: oxide films and adsorbed organic and water vapor films. Oxide films are relatively brittle and hard compared to metals while adsorbed films tend to be more elastic. Both films may be present on a metallic surface.

Most metals react with atmospheric oxygen to form native oxide layers 20-100 Å. Essentially only a few seconds of atmospheric contact is sufficient to produce this oxide layer. However, gold is unique in that it is typically free of oxide. This has been found experimentally [55, 56] and suggests that adsorbed organic films may be the cause of bonding difficulty with regard to gold thermocompression bonding. Jellison [55, 56] examined the effect of surface contamination on thermocompression bonding of gold. On two groups of gold samples, Auger electron spectroscopy indicated carbon as the primary surface impurity. Nitrogen traces were found on one group suggestive of residual photoresist. Exposure to ultraviolet radiation was shown to significantly reduce these surface contaminants and improve bond strength. Additionally, ultraviolet cleaning before bonding reduced the temperature required for thermocompression gold bond formation.

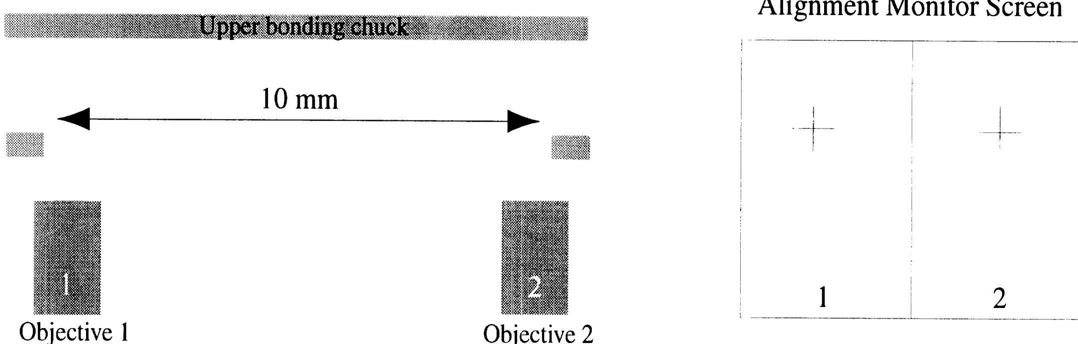
### 4.5.2 Experimental set-up



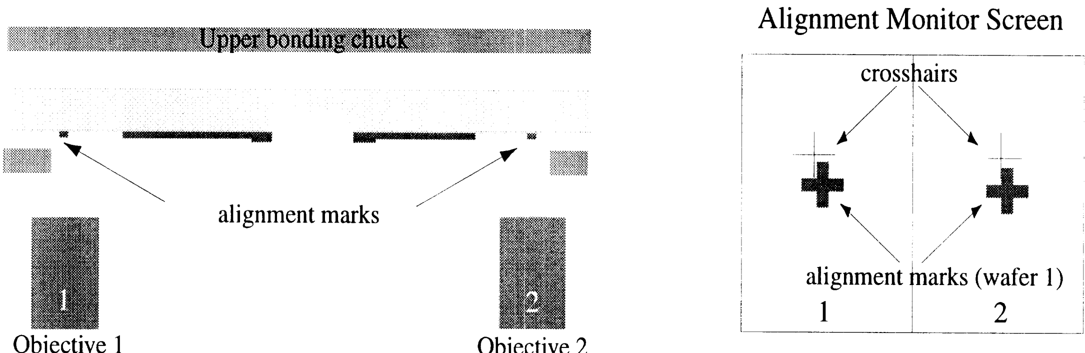
(a) (b)

Figure 4.10: Electronics Visions Align and Bond Equipment [116].

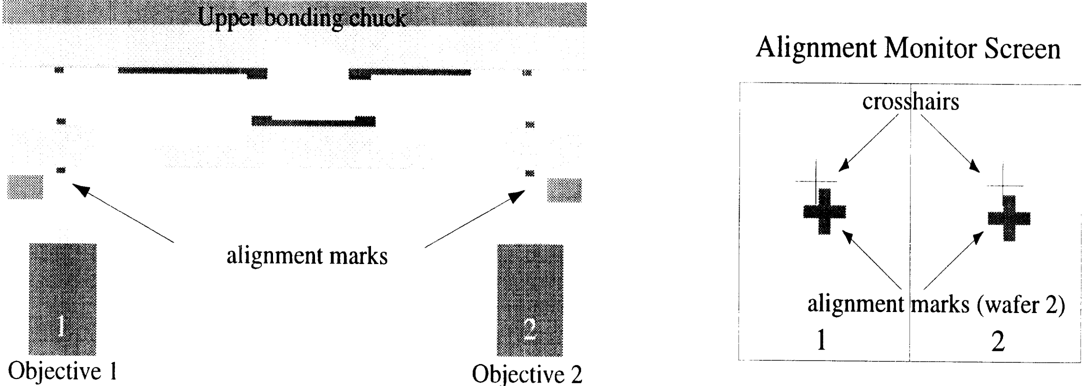
Since high-pressure and uniform heating are required for the bonding process, commercial wafer bonding equipment, shown in Figure 4.10, is used for this effort [116]. The experimental align and bond procedure begins as follows. To prevent surface contamina-




(a) Alignment set-up for Electronics Visions bonding includes two alignment/bonding chucks, two microscope objectives, and a split view monitor screen allowing view of each objective. Lower chuck includes 10 mm diameter viewing hole.

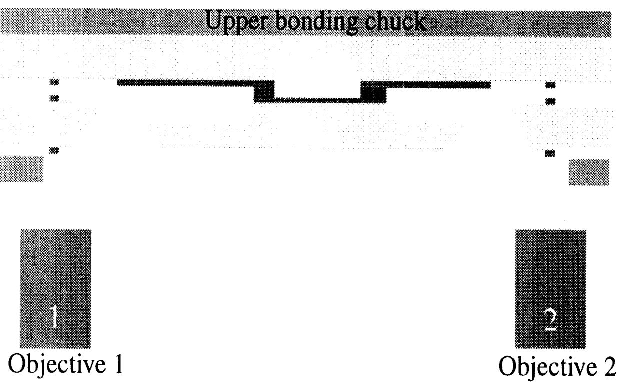



(b) First wafer is loaded onto lower chuck with alignment marks in view. Alignment marks are aligned to crosshairs on monitor screen.

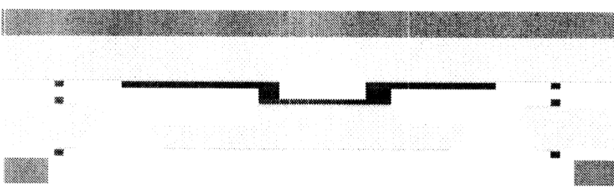



(c) First wafer is vacuum-held onto upper chuck and elevated while second wafer is loaded onto lower chuck and aligned to reference crosshairs.

Figure 4.11: Method of Alignment for Electronics Visions Equipment (a-c).




(d) Upper bonding chuck is lowered to form contact between upper and lower wafers. Alignment is complete.



(e) Entire alignment jig removed from aligner and placed in bonder for application of heat and pressure.

Figure 4.12: Method of Alignment for Electronics Visions Equipment (d-e).

tion, the wafers are cleaned with organic solvents and then ultraviolet (UV) exposed for 30 minutes. Aligned silicon wafer bonding is a two step process utilizing both pieces of Electronics Visions equipment. First the wafers are aligned in the EV420 Manual Aligner (Figure 4.10(a)). With this equipment, aligning begins by loading the first sample and aligning it to cross-hairs on a monitor screen as shown in Figure 4.11. This sample is then vacuum held to an upper plate. The second wafer is then loaded and aligned to the same cross-hairs on the monitor screen. Once aligned the wafers are brought into close proximity and clamped together in the bond fixture. As shown in Figure 4.12, this bond fixture is then loaded into the vacuum bond chamber of the EV 501 Manual Wafer Bonder (Figure 4.10(b)). The following sequence of events occurs. First a nitrogen ambient of $10^{-2}$ bar is achieved in order to maintain a low particulate environment and prevent further oxidation. A small amount of pressure, 50 Newtons (N), is then applied to the samples while the top

and bottom bond plates heat up to 350 °C. Once temperature has stabilized, 200 N are applied for 30 minutes.

## 4.6 Measurements

S-parameters of the RF wafer-to-wafer transitions are measured on an HP 8510C Network Analyzer[1] using 150 $\mu$m pitch Picoprobes[2] and a TRL calibration method to de-embed the probe-to-wafer transition and establish reference planes at the input and output ports of the circuits under test [69, 67]. The interconnects are tested in a back-to-back configuration, with a short section of transmission line connecting them. Figure 4.13 shows a photograph of the RF back-to-back circuit with Transition 2 (30-59-100 $\mu$m) revealing placement of the reference planes just at the onset of the transition, 800 $\mu$m in from each probe. The S-parameter measurements for each RF wafer-to-wafer transition will therefore show the loss of two 100 $\mu$m transitions and a 400 $\mu$m midsection of feed line.

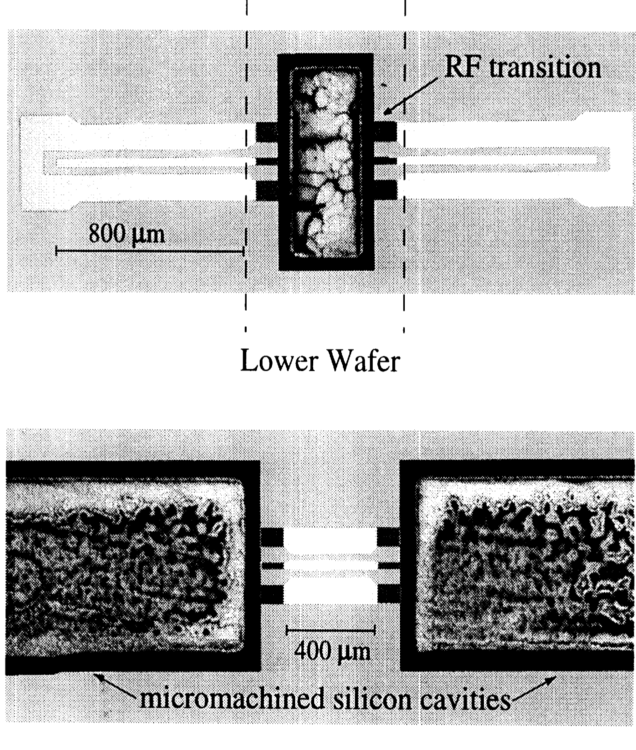



Figure 4.13: Photograph of RF wafer-to-wafer transition showing placement of calibration reference planes.

[1] Hewlett-Packard, Santa Clara, CA.
[2] GGB Industries, Naples, FL.

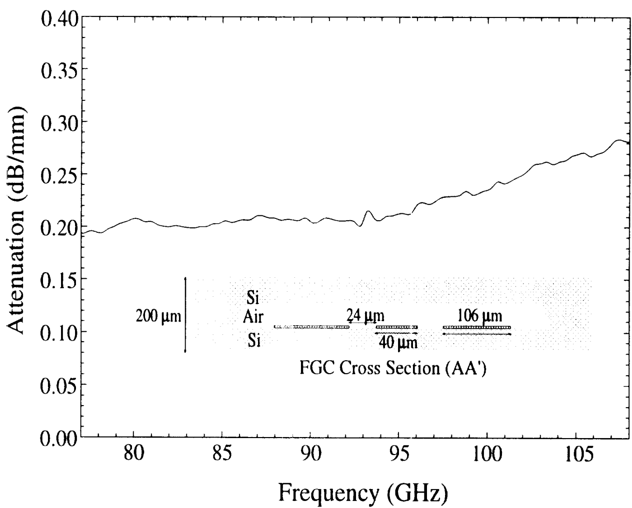


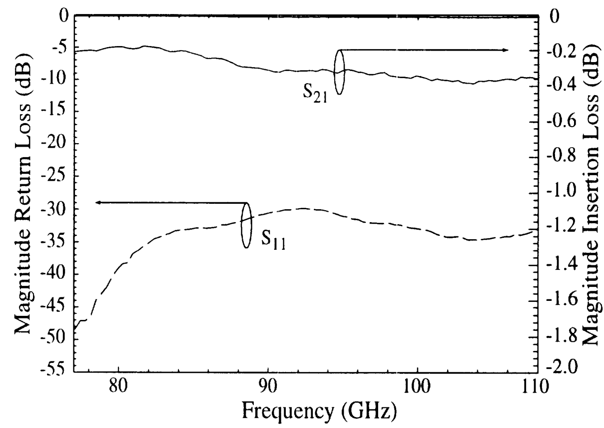

Figure 4.14: Measured Attenuation for FGC line.

At 94 GHz, the attenuation of the 50 Ω feed line, with cross-section AA', is 0.22 ± 0.02 dB/mm as shown in Figure 4.14. Note that this measurement is made after the wafer is cooled from the bonding temperature of 350 °C. Thus the expected loss from the 400 $\mu$m midsection of feed line is approximately 0.09 ± 0.01 dB.

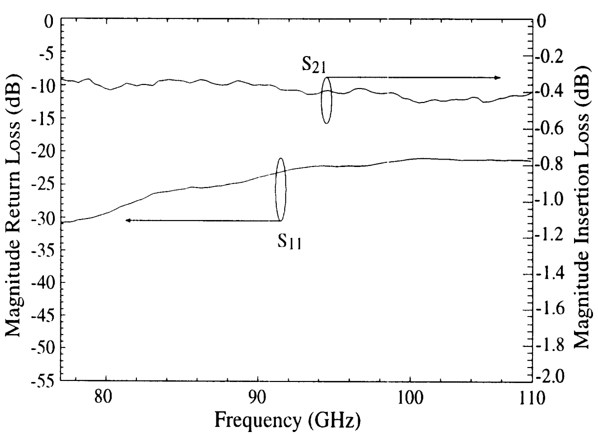
Figure 4.15 reveals back-to-back transition measurements for the three transition geometries, with return loss plotted on the left axis and insertion loss plotted on the right. From 90-98 GHz the insertion loss for transition 1 ranges 0.32 ± 0.02 dB with return loss below 30 dB. Subtracting the line loss of 0.09 dB from the total insertion loss yields 0.23 ± 0.03 dB loss for the two transitions. Thus the loss per transition may be approximated as 0.13 ± 0.02 dB per transition. Table 4.6 summarizes the results from 90-98 GHz with transition loss ranging from 0.07 dB to 0.15 dB with an error of ± 0.02 dB. Loss variation may be due to bond quality and wafer alignment, in addition to measurement error. Nonetheless, the average loss per transition is 0.12 dB.

Table 4.3: Back-to-back wafer-to-wafer interconnect measurement summary from 90-98 GHz.

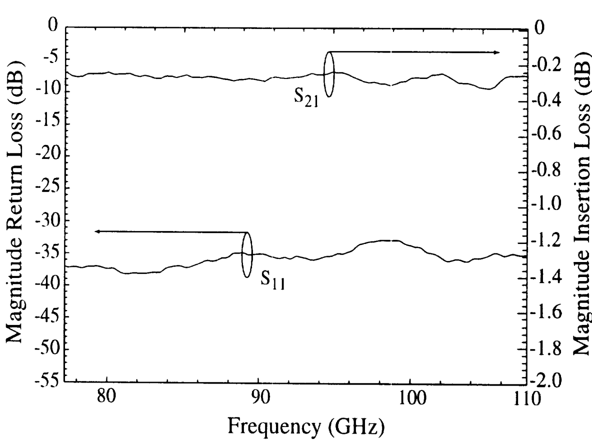
| Geometry | Figure | Insertion Loss ($S_{21}$) dB | Return Loss ($S_{11}$) dB | Transition Loss dB |
|---|---|---|---|---|
| 20-44-100 | 4.15(a) | $0.32 \pm 0.02$ | $\leq 30$ | $0.13 \pm 0.02$ |
| 30-59-100 | 4.15(b) | $0.38 \pm 0.04$ | $\leq 20$ | $0.15 \pm 0.02$ |
| 40-65-100 | 4.15(c) | $0.24 \pm 0.04$ | $\leq 30$ | $0.07 \pm 0.02$ |




(a) Transition 1 (20-44-100 $\mu$m)




(b) Transition 2 (30-59-100 $\mu$m)




(c) Transition 3 (40-65-100 $\mu$m)

Figure 4.15: S-parameters of measured RF wafer-to-wafer transitions.

## 4.7 Bond Evaluation and Analysis

Bond evaluation is obtained through visual inspection, and Figure 4.16 shows photographs of the bonded circuit of Transition 1 after being pulled apart. The gold bond is strong enough to rip the upper gold pads off the upper silicon wafer, taking silicon dioxide and some silicon with it. Misalignment on the order of 2-3 $\mu$m is shown.

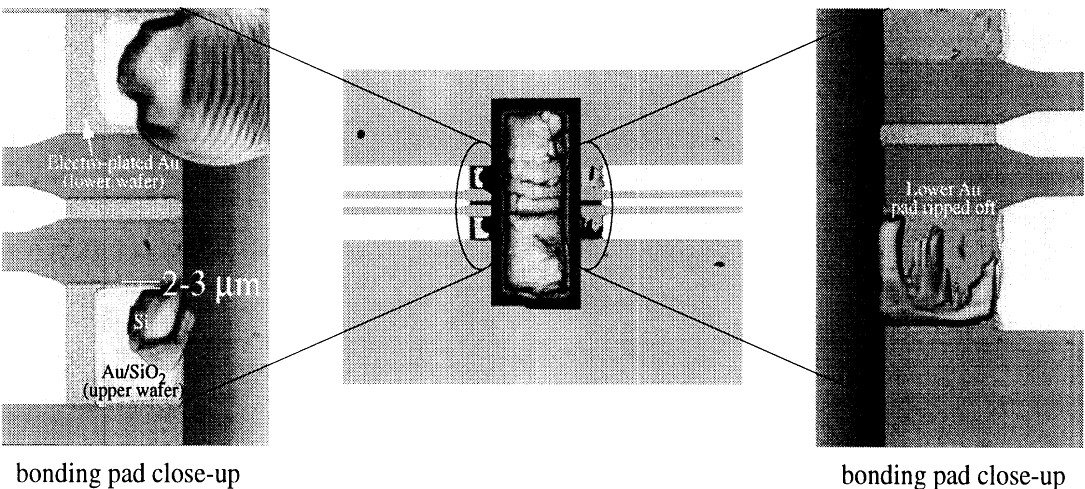



Figure 4.16: Photograph of bonded sample after wafers pulled apart showing bonding and alignment.

### 4.7.1 Misalignment

To determine the importance of lateral alignment, a parametric study is made for two of the three wafer-to-wafer transitions. For each geometry, HFSS simulations are run in which the top wafer is laterally shifted with respect to the lower wafer by increments of 5 microns until the center conductors no longer touch. A lateral misalignment schematic is shown in Figure 4.17. Examining Figure 4.18(a), insertion loss for the 40-65-100 $\mu$m transition varies from 0.85 dB (aligned) to 0.77 dB at 25% misalignment, and 0.76 dB with 75% misalignment. As misalignment varies from 0-100 % from the center conductor, insertion loss varies by 0.13 dB for this transition. Examining the corresponding return loss values, shown in Figure 4.18(b), 25% misalignment (10 microns) yields 29 dB return loss while a 75% misalignment yields 18 dB return loss. With return and insertion losses ranging from

18-35 dB and 0.72-0.84 dB, respectively, it may be concluded that lateral misalignment is not critical to circuit performance but modifies insertion loss by 0.1 dB. A similar result is found from the 30-59-100 $\mu$m transition, with insertion loss values ranging from 0.73 - 0.93 dB.

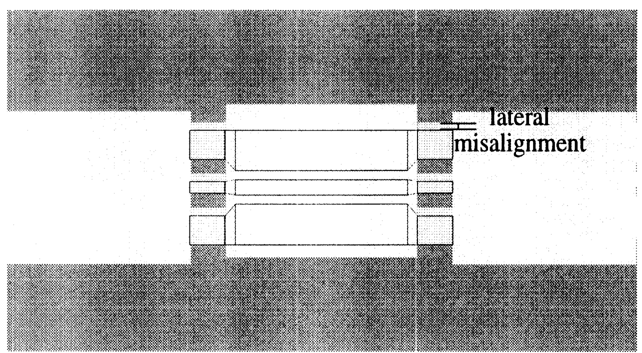
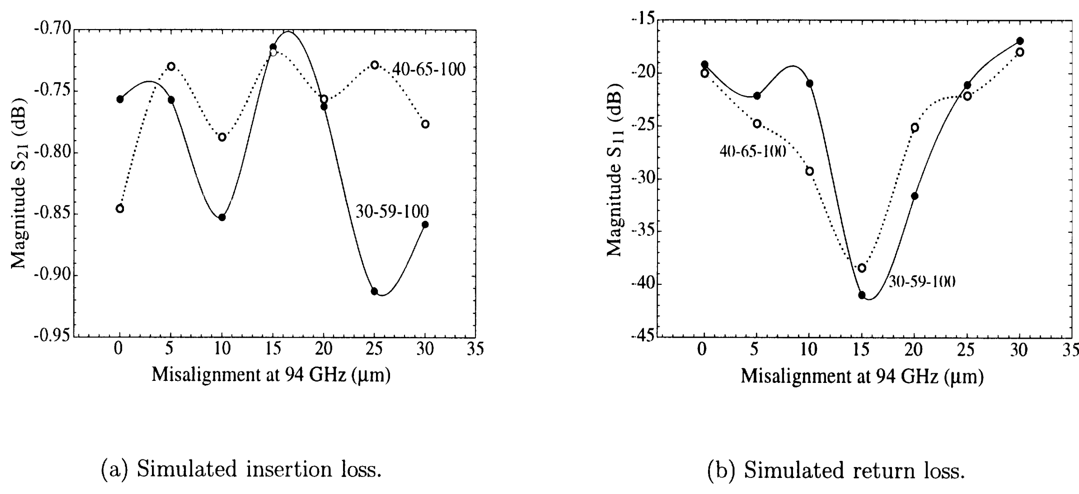



Figure 4.17: Schematic of simulated lateral misalignment.




(a) Simulated insertion loss.

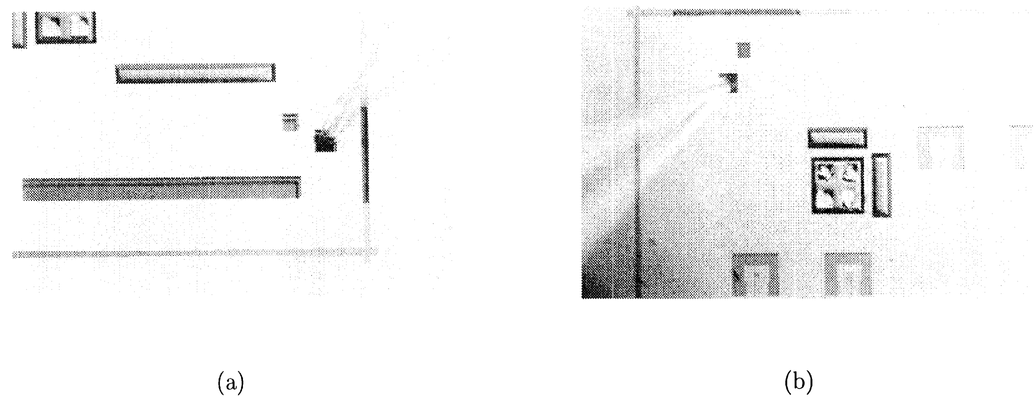
(b) Simulated return loss.

Figure 4.18: Simulated scattering parameters as a function of misalignment at 94 GHz for Transitions 2 and 3 (a) Insertion loss (b) Return loss.

### 4.7.2 Contact

Early in this study, wafer-to-wafer alignment was attempted by anisotropically etching holes through the wafers and then threading them together with flexible fiber optic cable [100]. The fibers are uniformly 215 $\mu$m diameter, making the undercut of the anisotropic

etchant a critical factor. A photo of the fibers threaded through two silicon wafers is shown in Figure 4.19. After being threaded and therefore aligned, silver epoxy was placed along the sides of the two samples and they were then put in an oven at 110 °C with a relatively light weight on top of them for pressure and curing.



(a) (b)

Figure 4.19: Photos of 215 $\mu$m diameter optic fibers threaded through two Si wafers.

Measurements of these circuits were unfavorable although the application of pressure during measurement provided much improvement. Figure 4.20 shows the measurement with the application of pressure from 75-105 GHz, and the deleterious effect of releasing that pressure from 105-110 GHz. This measurement illustrates the importance of strong gold-to-gold wafer bonds as the application of pressure yields 1 dB insertion loss and no pressure yields insufficient RF coupling for signal flow. Simulation of the wafer-to-wafer transition with 2 $\mu$m vertical separation verifies this result as seen in Figure 4.21. From 90-100 GHz, the circuit is essentially open with insertion loss of 15 dB.

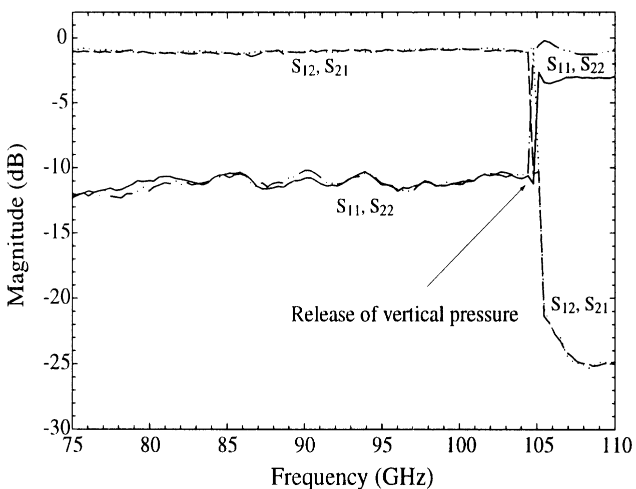



Figure 4.20: S-parameter measurements of unbonded RF wafer-to-wafer transition.

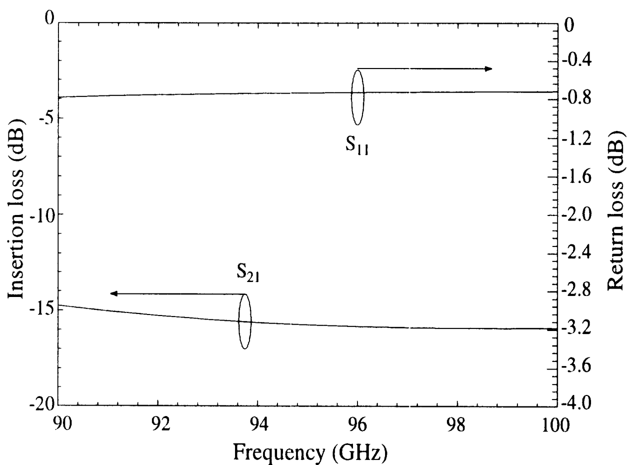



Figure 4.21: S-parameter simulations of RF wafer-to-wafer transition with 2 $\mu$m vertical separation.

## 4.8 Conclusions

On-wafer S-parameter measurements of a W-band RF wafer-to-wafer interconnect are demonstrated with average loss per transition of 0.12 dB. Table 4.8 summarizes the measured and simulated results for each of the three examined transition geometries. All three geometries yield similar measured results ranging from 0.07 to 0.15 dB loss per transition. The 0.07 dB variation may be due to the geometries themselves, the alignment, the bond quality, and error of the measurement.

Table 4.4: Wafer-to-wafer interconnect summary from 90-98 GHz.

| Geometry | Measured Transition Loss dB | Figure | Simulated Transition Loss dB | Figure |
|---|---|---|---|---|
| 20-44-100 | 0.13 | 4.15(a) | 0.04 | 4.6(a) |
| 30-59-100 | 0.15 | 4.15(b) | 0.08 | 4.5(b) |
| 40-65-100 | 0.07 | 4.15(c) | 0.07 | 4.6(b) |

Thus, alignment and bonding are the most important criteria to obtaining repeatable results. Simulations indicate that direct contact is most critical. Misalignment, of the width of the center conductor, affects insertion loss by 0.1-0.2 dB at W-band. Both measured and simulated results show the need for high-pressure low-temperature bonding, and without it RF coupling is insufficient for signal flow.

The thermocompression bond used for the interconnect is not only a strong low-temperature gold-to-gold bond but an excellent RF electrical connection. In addition, the approach is compatible with MMIC technology, and may assist in the utilization of high density multi-level integration schemes.

# CHAPTER 5

# MICROMACHINED CIRCUIT COMBINING NETWORKS

## 5.1 Introduction

In circuit combining networks, low loss interconnecting transmission lines are pivotal in reducing excess loss. Micromachined Finite Ground Coplanar (MFGC) waveguides are used in this study as low loss interconnects showing significant improvements in line loss while maintaining characteristic impedance for both 50 and 70 $\Omega$ designs. Wilkinson power dividers, reactive tee junctions, and right angle bends are combined with micromachined interconnects in 1:2, 1:4, and 1:8 power dividing networks showing loss reduction of 0.2-1.6 dB depending on circuit type and size.

## 5.2 Motivation

With the advancements of high density and multi-layer circuit applications comes the continued emphasis on low-loss, low-cost transmission lines. In power dividing networks, in which power is split from one to four or more signal paths, the transmission line characteristics become significant since longer lines are typically required. This is especially true in a multi-layer environment where each layer may consist of a one to four divider, and the loss of the entire multi-layer network is equal to the number of layers times the loss of each layer. The proper choice of transmission line and aspect ratio reduces parasitics and minimizes the overall circuit loss. In fact, line loss may become the dominant loss mechanism despite the presence of power splitting elements such as Wilkinsons and reactive tee

junctions. Thus choosing a transmission line for the entire network or as an interconnect between components yields flexibility and may influence the circuit loss most significantly.

As shown in Chapter 2, Micromachined Finite Ground Coplanar (MFGC) waveguide has demonstrated significantly lower loss than conventional coplanar waveguide for frequencies up to 110 GHz [45, 46, 47]. By simply micromachining the silicon from the aperture regions of the line, loss improvements can be made without sacrificing the structural integrity, double-sided processing, and modifying the aspect ratio. Arguably, the localization of the fields also makes this line a better multi-layer candidate than microstrip. However, in addition to decreasing the attenuation of the line, micromachining the aperture regions decreases the effective dielectric constant, thereby increasing the characteristic impedance. Thus geometry modifications must be made to match a particular impedance to a micromachined line.

This study focuses on the application of MFGC lines in power combining networks. Rather than redesign components such as Wilkinsons and reactive tee junctions, the intent here is to develop MFGC feed lines that maintain the characteristic impedance of the components as well as provide a significantly lower loss interconnect between these components. The modeling and measurement of the lines themselves are first presented for two characteristic impedances under study: 50 and 70 Ω. These lines are integrated into circuit combining networks to demonstrate the loss improvements obtained through micromachining. Both modeled and measured results show the loss reduction when the lines are micromachined in one to two (1:2), one to four (1:4), and one to eight (1:8) circuit combining networks.

## 5.3 Components

The components used for the circuit combining networks are Wilkinson power dividers, reactive tee junctions, and right angle bends. These individual components were designed by Dr. Tom Weller [118], and have been simulated, fabricated, and measured as an integrated network in this dissertation. A description of the elements is given in this section as well as simulation results. Figure 5.1 shows the equivalent circuit for the Wilkinson, while Figure 5.2 shows the schematics of the 50 and 70 Ω designs. In both cases the power is split equally,

thus 3 dB of nominal loss is expected. For the 50 Ω case, the feed line dimensions are 40 μm center conductor, 24 μm apertures, and 106 μm ground planes. Note the high impedance sections on either side of the air bridges used for compensation, and the thin film 100 Ω resistor. For the 70 Ω case, the feed line dimensions are 18 μm center conductor, 35 μm apertures, and 100 μm ground planes. The 100 Ω mid sections are made using asymmetrical coplanar stripline with an outer strip width of 100 μm, an inner strip width of 25 μm, and a slot width of 50 μm. The thin film resistor is 140 Ω and no air bridge compensation is used in this design.

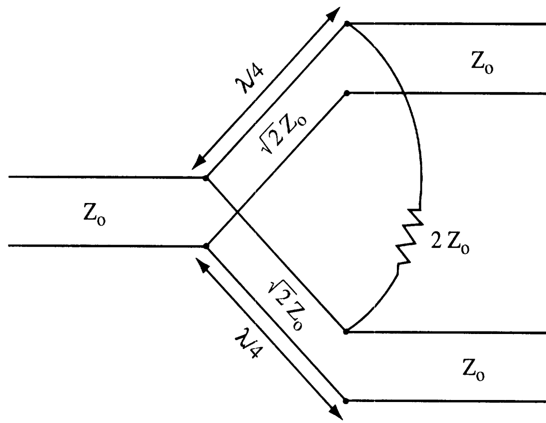
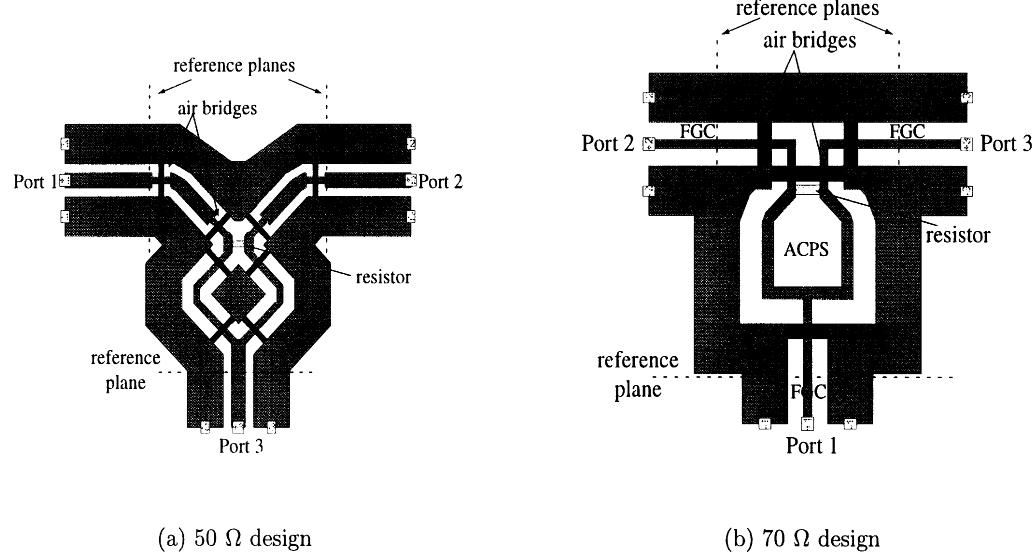



Figure 5.1: Equivalent transmission line circuit for Wilkinson power divider.

Simulated results are based on IE3D which characterizes mismatch but is unable to accurately characterize the loss of the two lines. The proof of this is the inability of IE3D to model a finite thickness conductor. Although 1 μm thickness of metal with conductivity $4.7 \times 10^7$ S/m is used, the 2.5-D code approximates this thickness based on an infinitely thin conductor. Additionally, 50 and 70 Ω through lines were simulated, and based on the insertion loss, the attenuation of the 50 and 70 Ω lines is 0.16 dB/mm and 0.19 dB/mm at 90 GHz, respectively. This loss is less than the 0.28 dB/mm and 0.34 dB/mm losses measured for these 50 and 70 Ω lines at 90 GHz, respectively. Thus the simulations shown here only indicate the mismatch for a given component.

Simulated results for the 50 Ω Wilkinson, shown in Figure 5.3(a), yield insertion loss values ranging 3.2-3.6 dB from 75-100 GHz. Attenuation based on 0.16 dB/mm is used to de-embed the insertion loss to the reference planes indicated in Figure 5.2(a), reducing

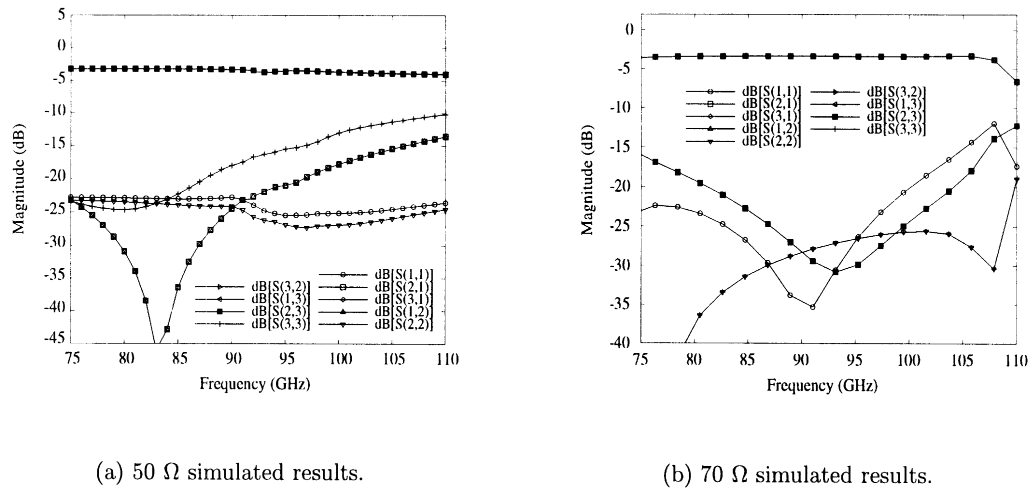



(a) 50 Ω design

(b) 70 Ω design

Figure 5.2: Schematics of Wilkinson power dividers as simulated in IE3D [132]: a) 50 Ω b) 70 Ω.

the excess loss (3 dB nominal) to 0.07-0.47 dB. Simulated results for the 70 Ω Wilkinson, shown in Figure 5.3(b), yield insertion loss values ranging 3.4-3.7 dB from 75-100 GHz. Attenuation based on 0.19 dB/mm is used to de-embed the insertion loss to the reference planes indicated in Figure 5.2(b), reducing the excess loss to 0.3-0.6 dB.




(a) 50 Ω simulated results.

(b) 70 Ω simulated results.

Figure 5.3: S-parameters of Wilkinson power dividers as simulated in IE3D [132]: a) 50 Ω b) 70 Ω.

The schematic for the 50 and 70 Ω reactive tee junctions is shown in Figure 5.4. If the

transmission lines are assumed low loss and the characteristic impedances are assumed real, Equation 5.1 represents the tee junction [90]. For an equal 3 dB split, $Z_1 = Z_2$. Thus for the 50 Ω tee junction, 100 Ω is produced at the output. A quarter wave transformer of 70.7 Ω is used after each output to bring the line back to 50 Ω. For the 70 Ω tee junction, a 50 Ω quarter wave transformer is used at the input, producing 70 Ω output lines.

$$\frac{1}{Z_0} = \frac{1}{Z_1} + \frac{1}{Z_2} \tag{5.1}$$

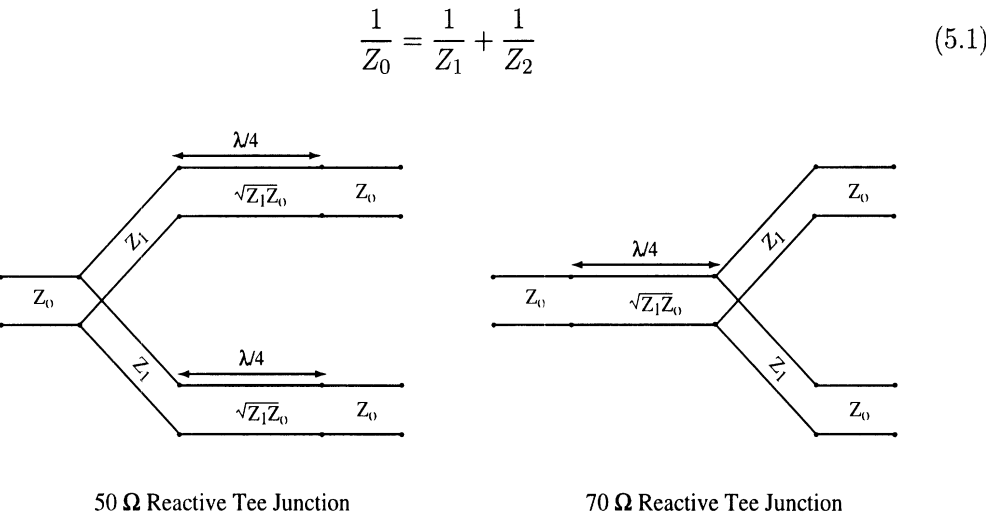
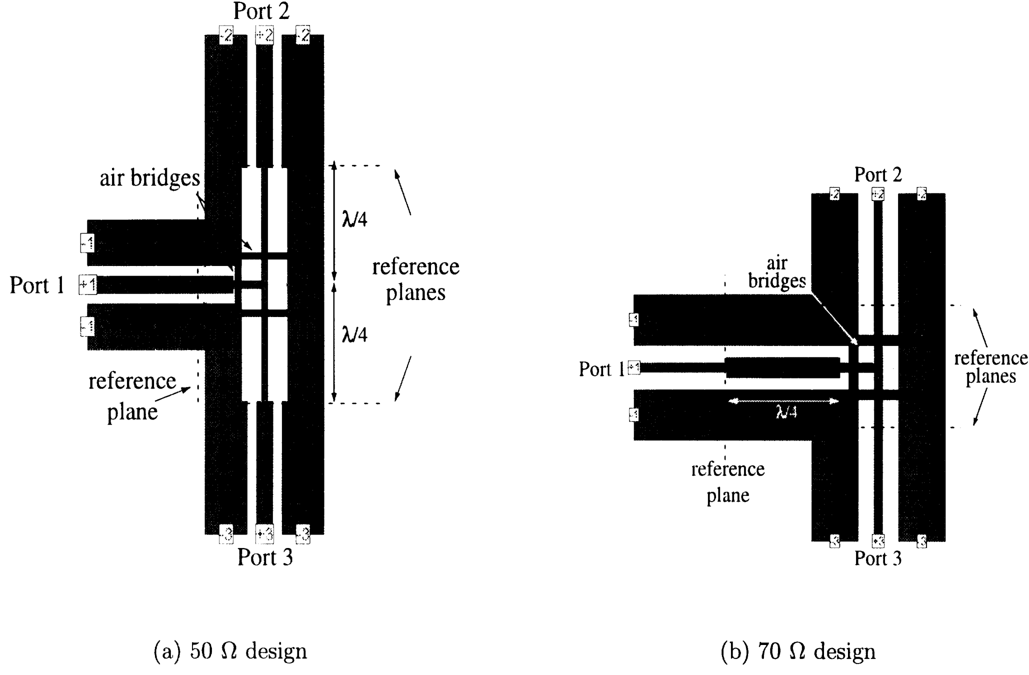



Figure 5.4: Equivalent transmission line circuit for reactive tee junction.

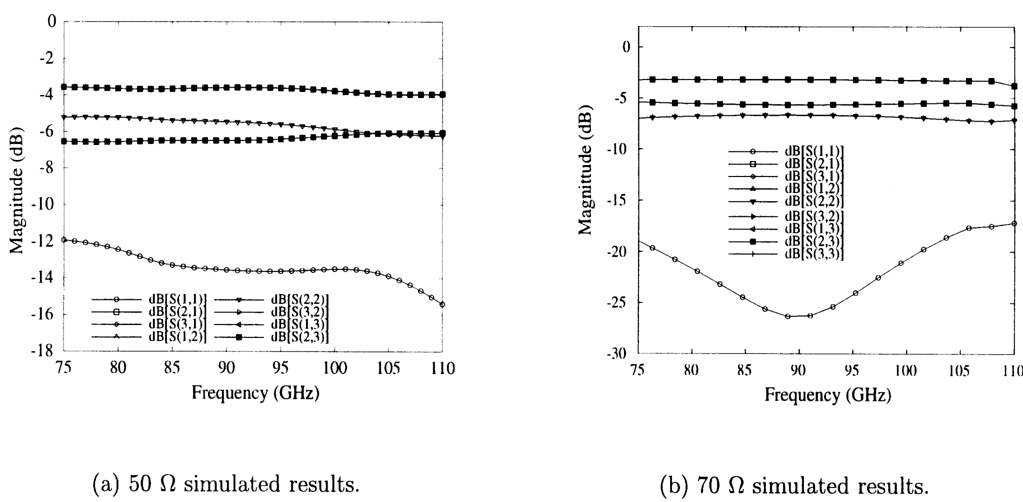
Simulated results for the 50 Ω reactive tee junction, shown in Figure 5.6(a), yield insertion loss values ranging 3.55-3.74 dB from 75-100 GHz. Attenuation based on 0.16 dB/mm is used to de-embed the insertion loss to the reference planes indicated in Figure 5.5(a), reducing the excess loss (3 dB nominal) to 0.43-0.62 dB. Simulated results for the 70 Ω tee junction, shown in Figure 5.6(b), yield insertion loss values ranging 3.2-3.3 dB from 75-100 GHz. Attenuation based on 0.19 dB/mm is used to de-embed the insertion loss to the reference planes indicated in Figure 5.2(b), reducing the excess loss to 0.04-0.1 dB. Differences in estimated insertion loss for the two designs may be explained by the two quarter-wave high impedance sections in the 50 Ω design as opposed to the single 50 Ω quarter-wave impedance section in the 70 Ω design. Thus the additional high impedance line length is attributed to the higher insertion loss for the 50 Ω design. Although both the reactive tee junction and Wilkinson divide power equally, the tee junction has the advantage of simpler fabrication as it has no thin film resistor. However, it only provides approximately 7 dB




(a) 50 Ω design (b) 70 Ω design

Figure 5.5: Schematics of reactive tee junctions as simulated in IE3D [132]: a) 50 Ω b) 70 Ω.

isolation between the two output ports.

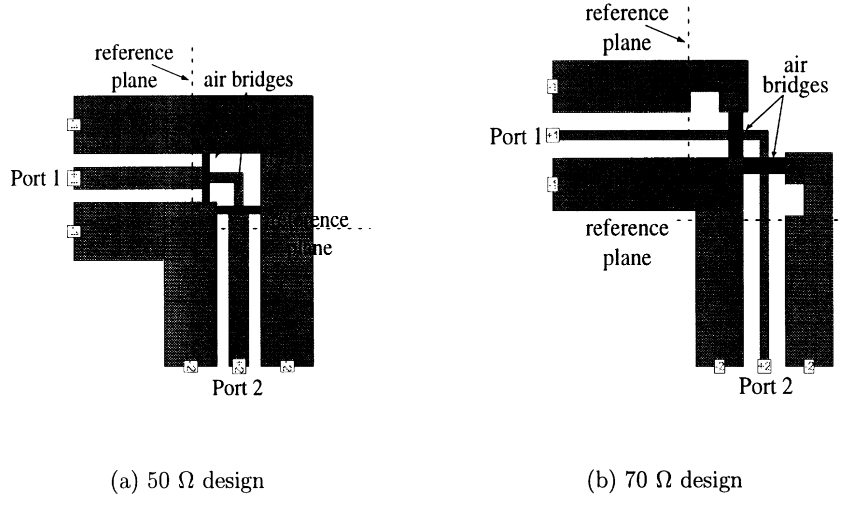



(a) 50 Ω simulated results. (b) 70 Ω simulated results.

Figure 5.6: S-parameters of reactive tee junctions as simulated in IE3D [132]: a) 50 Ω b) 70 Ω.

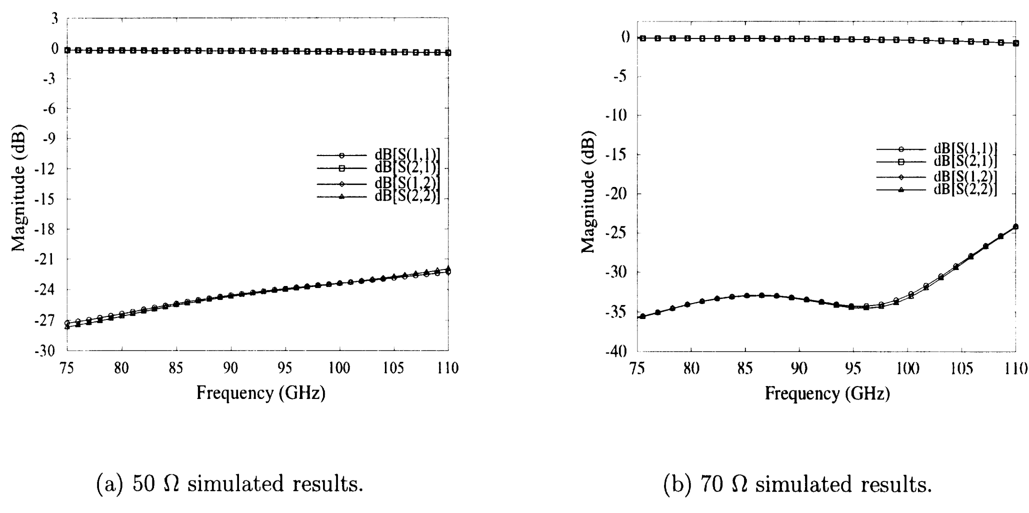
Lastly, schematics for the right angle bend designs is shown in Figure 5.7. Simulated results shown in Figure 5.8(a) shows insertion loss varying 0.2-0.4 dB for the 50 Ω design.

Subtracting the line loss up to the reference planes, reduces the insertion loss to 0.1-0.3 dB. Likewise, the insertion loss for the 70 Ω bend ranges from 0.23-0.43, which reduces to 0.13-0.33 dB after de-embedding.




(a) 50 Ω design (b) 70 Ω design

Figure 5.7: Schematics of right angle bends as simulated in IE3D [132]: a) 50 Ω b) 70 Ω.




(a) 50 Ω simulated results. (b) 70 Ω simulated results.

Figure 5.8: S-parameters of right angle bends as simulated in IE3D [132]: a) 50 Ω b) 70 Ω.

All of the 50 Ω designs incorporate compensations for the effect of air bridges on the line, which consist of high impedance sections on either side of the air bridge [118]. Compensation is not applied to the 70 Ω designs because of the difficulty in realizing a higher impedance. However, the 70 Ω right angle bend includes a compensation in which the center conductor is

narrower in between the air bridges and the outer ground plane is removed. An examination of compensations for single air bridges is presented in Appendix A, in which the air bridge is modeled as a shunt capacitance and it's equivalent low impedance is compensated with high impedance sections. The equivalent circuit is shown in Figure 5.9 and the equivalent impedance is shown in Equation 5.2. Setting $Z_{t2}$ equal to the impedance of the line and solving for $l$ yields two solutions for the high impedance section lengths. As shown in Appendix A, air bridges compensated with two different lengths of high impedance section are fabricated and measured. These measurements are well-matched with a Libra model.

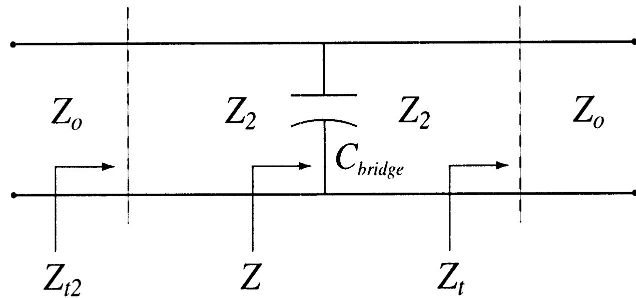



Figure 5.9: Equivalent circuit for air bridge.

$$Z_{t2} = Z_2 \frac{Z + jZ_2 tan(\beta l)}{Z_2 + jZ tan(\beta l)} \tag{5.2}$$

Table 5.1 shows a summary of the simulated component insertion loss after de-embedding up to the reference planes. The loss of the bend is approximated as 0.15 dB for both geometries, while that of the 50 and 70 Ω Wilkinsons are 0.27 and 0.42 dB, respectively. The simulation for the tee junction yields the most variation between the two designs with the 50 Ω design having 0.53 dB loss and the 70 Ω design with only 0.03 dB. These values are used as conservative estimates of component insertion loss.

## 5.4 Interconnects

Design of the micromachined finite ground coplanar (MFGC) waveguide shown in Figure 5.10 begins with electro-static simulations of the cross-section of the line [5]. From the calculated line shunt capacitance, the effective dielectric constant and characteristic

Table 5.1: IE3D estimated loss for 1:2, 1:4, 1:8 circuit networks.

| Component | Sim Atten (dB/mm) | Loss from 75-100 GHz (dB) | Average Loss (dB) |
|---|---|---|---|
| 50 Ω Bend | 0.16 | 0.1-0.3 | 0.15 |
| 70 Ω Bend | 0.19 | 0.13-0.33 | 0.17 |
| 50 Ω Tee | 0.16 | 0.43-0.62 | 0.53 |
| 70 Ω Tee | 0.19 | 0.04-0.1 | 0.05 |
| 50 Ω Wilk | 0.16 | 0.07-0.47 | 0.27 |
| 70 Ω Wilk | 0.19 | 0.3-0.6 | 0.45 |

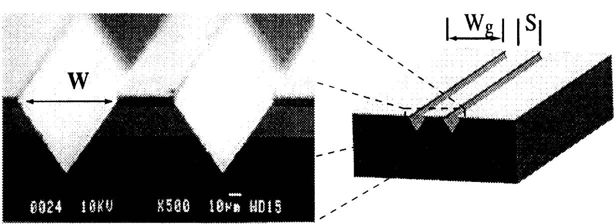



Figure 5.10: MFGC geometry.

impedance are obtained as shown in Table 5.2 for micromachined and conventional 50 and 70 Ω transmission lines. For the 50 Ω line, the center conductor width is increased by 30 $\mu$m to maintain a 50 Ω line when the 30 $\mu$m apertures are etched, while the center conductor width is increased by 22 $\mu$m for the 70 Ω design. Note the wider apertures of the 70 Ω MFGC design are responsible for the lowest effective dielectric constant of 4.3

Table 5.2: Characteristics of micromachined and unmicromachined lines.

| Design | S/W ($\mu$m) | $C_{sub}$ (F/m) | $C_{air}$ (F/m) | $\epsilon_{eff}$ | $Z_o$ (Ω) |
|---|---|---|---|---|---|
| 50 Ω FGC | 40/24 | $1.7\times10^{-10}$ | $2.7\times10^{-11}$ | 6.2 | 54 |
| 50 Ω MFGC | 70/30 | $1.4\times10^{-10}$ | $2.9\times10^{-11}$ | 4.7 | 52 |
| 70 Ω FGC | 18/52 | $1.15\times10^{-10}$ | $1.85\times10^{-11}$ | 6.2 | 72 |
| 70 Ω MFGC | 40/40 | $9.8\times10^{-11}$ | $2.3\times10^{-11}$ | 4.3 | 71 |

Figures 5.11 and 5.12 yield the series resistance and inductance per-unit-length for the four lines as a function of frequency [62, 108]. The conductivity used for all four lines is $3.7\times10^{7}$ S/m. Note the highest resistance and inductance values for the 70 Ω FGC line with the narrowest center conductor. The 50 Ω micromachined line yields the lowest series resistance and inductance values due to its 70 $\mu$m wide center conductor. Figure 5.13 shows the modeled attenuation versus frequency for each line. At 94 GHz, attenuation values are 2.9 and 2.8 dB/cm for the unmicromachined lines, while those for the micromachined lines are reduced to 1.9 and 1.8 dB/cm. Although the 70 Ω line is more lossy than the 50 Ω line, due to the narrow center conductor width (18 $\mu$m), micromachined versions of both lines yield approximately 1 dB/cm loss improvements.

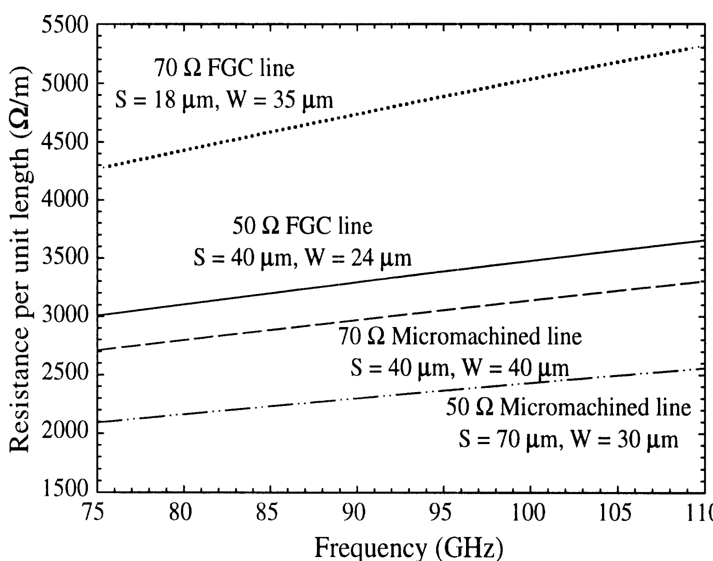



Figure 5.11: Modeled resistance per unit length versus frequency for four aspect ratios.

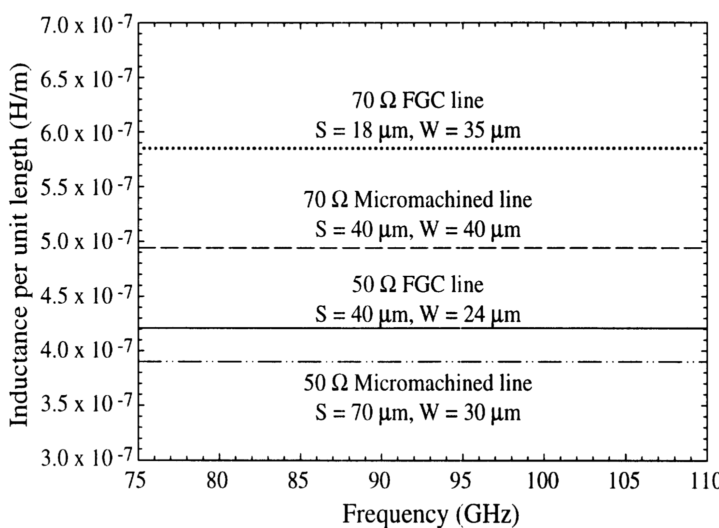



Figure 5.12: Modeled inductance per unit length versus frequency for four aspect ratios.

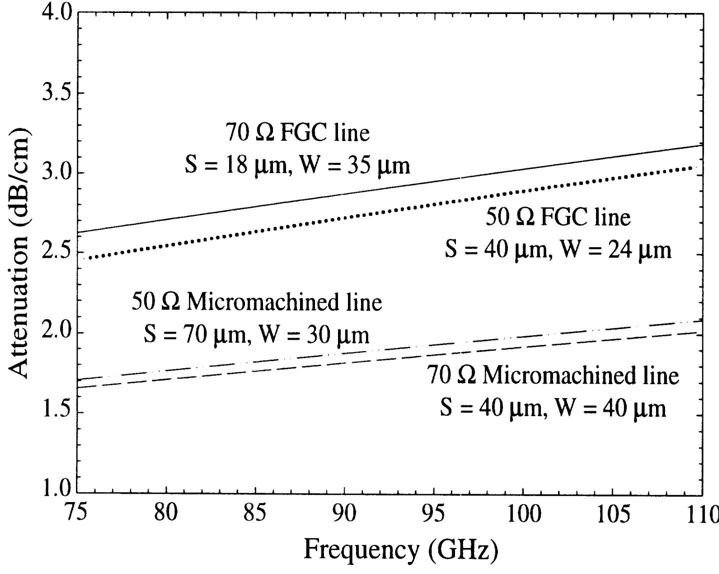



Figure 5.13: Modeled attenuation versus frequency showing expected loss improvement utilizing silicon micromachining.

## 5.5 Fabrication

The circuits are printed on 400 $\mu$m thick high-resistivity double-side polished silicon wafers with 6600 Å$SiO_2$ on both sides. The five main fabrication steps are thin film resistor deposition, circuit metallization, aperture definition, air bridge formation, and anisotropic wet etching of the apertures. Nichrome (NiCr) is used for the thin film resistors as it is not etched in potassium hydroxide (KOH), the anisotropic etchant used to create the micromachined grooves.

For the thin film resistors, 400 Å of NiCr is deposited using a lift-off process. This thickness results in a sheet resistance of 42 $\Omega$/square based on a four point probe measurement. A lift-off process is also used for the circuit metallization of Cr/Au (500/9500 Å), and silicon dioxide is patterned in the aperture regions and etched in buffered hydrofluoric acid (BHF) for 6.6 minutes (1000 Å/min etch rate). Flood evaporation of a seed layer (Cr/Au/Cr (500/1000/500 Å)) initiates air bridge formation. After patterning, the bridges are electro-plated in a cyanide based solution to approximately 3 $\mu$m, and removal of the seed layers completes the air bridge formation. The final step is to anisotropically etch the oxide-patterned apertures in Potassium Hydroxide (KOH) at an etch rate of 30 Å/hour. Note that KOH yields a minimal amount of lateral undercut, although substantial lateral undercut may be achieved using other anisotropic wet etchants such as ethylene diamene pyrocatechol (EDP) and tetramethyl ammonium hydroxide (TMAH) [45, 46, 65].

## 5.6 Measurements

### 5.6.1 Components

Measurement of the individual components requires right angle orientation of the measurement probes. As the W-band set-up requires the probes to be aligned and facing each other, a right angle bend is added to each of the components for measurement purposes. Thus the three circuits measured for component loss extraction are: Wilkinson and bend, reactive tee and bend, and double bend. The measured values at 94 GHz are averaged and assigned a margin of error based on the ripple in the measurement. The attenuation of the

interconnecting lines is de-embedded from the measurement and the remaining insertion loss represents that of the component tested. Table 5.3 shows the measured component loss estimates. The 50 Ω Wilkinson and bend data is taken from back-to-back measurements. Thus the component loss is actually half of the remaining loss as entered into the table. The component loss for the 50 Ω circuits also agrees with and represents those obtained by Dr. Henderson [38].

Table 5.3: Estimated component insertion loss values at 94 GHz as taken from measurement. The error of the measurement for the 50 Ω components is ± 0.03 dB, and the error for the 70 Ω component measurements is ± 0.07 dB

| Design | Total insertion loss | Estimated line loss | Component loss |
|---|---|---|---|
| 50 Ω Wilk and bend | 1.25 dB | 0.26 dB | 0.50 dB |
| 50 Ω tee and bend | 0.5 dB | 0.16 dB | 0.34 dB |
| 50 Ω double bend | 0.49 dB | 0.28 dB | 0.21 dB |
| 70 Ω Wilk and bend | 1.5 dB | 0.18 dB | 1.32 dB |
| 70 Ω tee and bend | 1.13 dB | 0.16 dB | 0.97 dB |
| 70 Ω double bend | 1.07 dB | 0.11 dB | 0.96 dB |

Based on the measured results the insertion loss of 50 Ω bend is approximately 0.11 dB while that of the 70 Ω bend is 0.48 dB. The explanation for the higher loss in the 70 Ω design is the open corners and high density of current on the compensating air bridges and the higher impedance compensating center conductor. Thus the 70 Ω bend is not an optimal design and this further illustrates the inability of IE3D to effectively model loss. The 50 Ω components are therefore preferable. However, all components will be incorporated into 50 and 70 Ω micromachined networks to show the improvement obtained through micromachining.

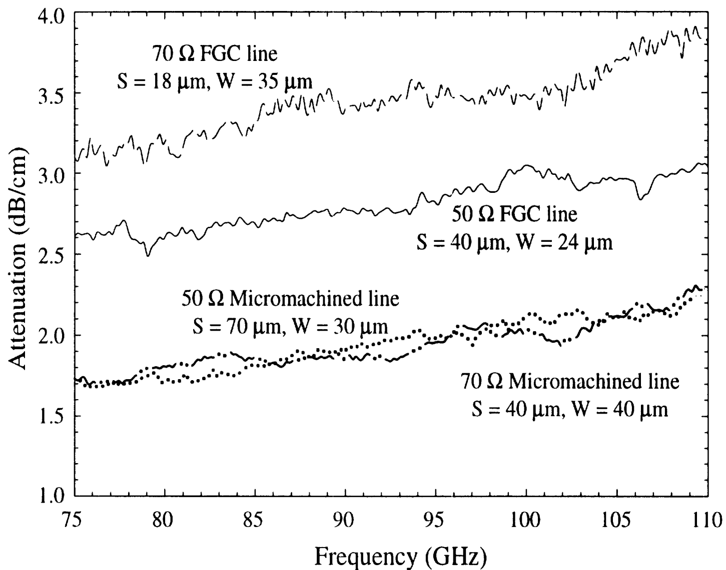
### 5.6.2 Interconnects

S-parameters of the combining networks are measured on an HP 8510C Network Analyzer[1], using 150 $\mu$m pitch Picoprobes[2] and a TRL calibration method to de-embed the probe-to-wafer transition. This method of de-embedding establishes reference planes at the input and output ports of the circuits under test [69, 67]. A separate calibration set is used for each of the four geometries tested (50 $\Omega$ FGC, 50 $\Omega$ MFGC, 70 $\Omega$ FGC, and 70 $\Omega$ MFGC), and the measured attenuation based on each calibration is shown in Figure 5.14. These measured results are compared with modeled in Figure 5.14(b) showing close match of all lines except the 70 $\Omega$ FGC line. This line may be lossy due to contaminants in the aperture regions. The results have been tabulated showing attenuation values for both measured and modeled lines in dB/mm at 94 GHz (see Table 5.4). The attenuation of the 70 $\Omega$ line is 0.34 dB/mm at 94 GHz, while the 50 $\Omega$ line measures 0.27 dB/mm. Both micromachined versions reduce the loss to approximately 0.19 dB/mm at 94 GHz.

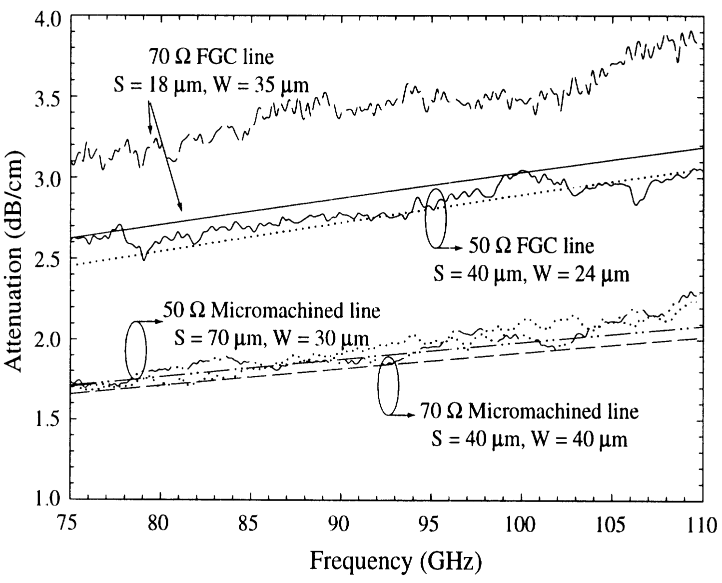
Table 5.4: Measured and modeled attenuation values from 85-95 GHz.

| Design | S/W ($\mu$m) | $\alpha$ (dB/mm) Measured | $\alpha$ (dB/mm) Modeled |
|---|---|---|---|
| 50 $\Omega$ FGC | 40/24 | 0.25-0.27 | 0.25-0.27 |
| 50 $\Omega$ MFGC | 70/30 | 0.17-0.19 | 0.17-0.19 |
| 70 $\Omega$ FGC | 18/52 | 0.33-0.34 | 0.27-0.28 |
| 70 $\Omega$ MFGC | 40/40 | 0.17-0.19 | 0.16-0.18 |

[1]Hewlett-Packard, Santa Clara, CA.
[2]GGB Industries, Naples, FL.




(a) Measured attenuation.




(b) Measured and modeled attenuation.

Figure 5.14: Measured attenuation for two FGC lines and two micromachined FGC lines of the same characteristic impedance. a) measured b) measured and modeled.

### 5.6.3 1:2 Combining Network

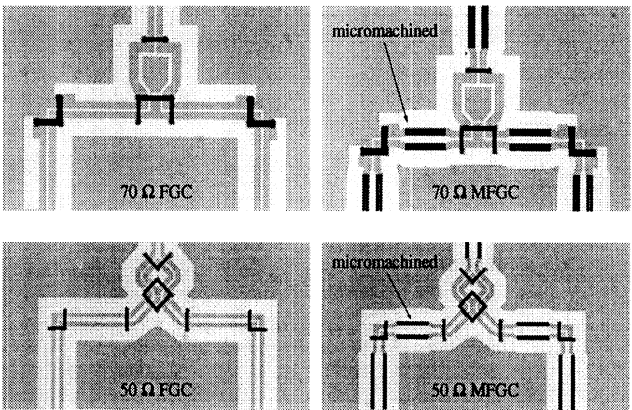
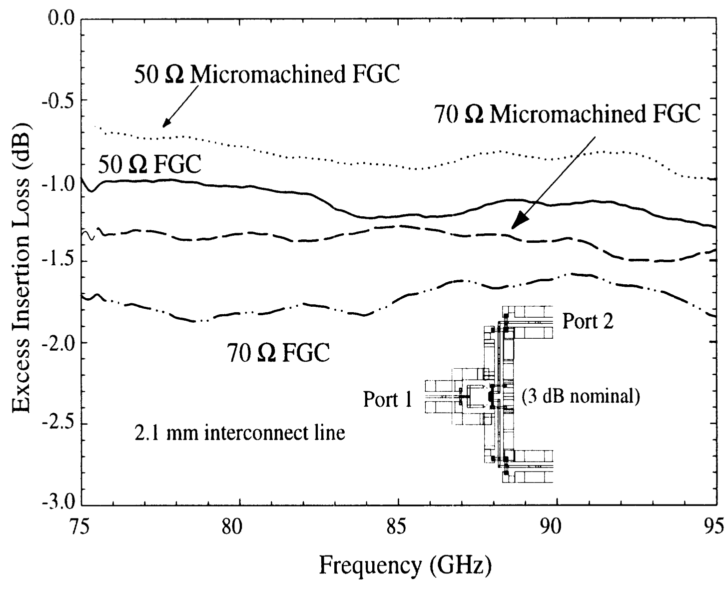


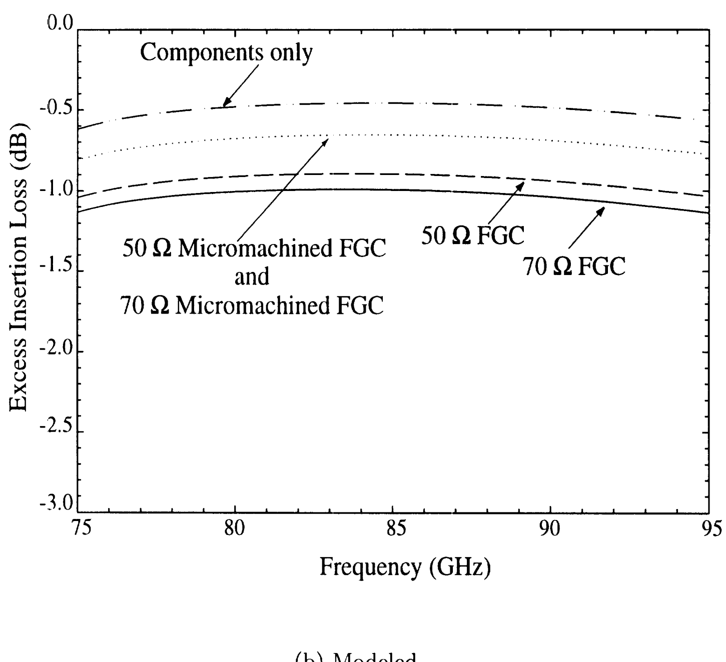

Figure 5.15: Photo of Wilkinson plus bend circuits.

Figure 5.15 shows photographs of four circuits consisting of Wilkinson power dividers and right angle bends for 50 and 70 Ω designs. The signal travels through a Wilkinson, a section of line, and a right angle bend, resulting in 3 dB of nominal loss. Figure 5.16 shows the measured and modeled excess insertion loss ($S_{21}$) for these circuits with 2.1 mm total interconnect length. At 85 GHz, the insertion loss of the 70 Ω circuit is 1.7 dB above the nominal of 3 dB. However, when this circuit is replaced with the micromachined version, the insertion loss is reduced to 1.3 dB at 85 GHz. This improvement of 0.4 dB represents a 9% increase in combining efficiency. Clearly, the high loss of this particular 70 Ω line makes it a poor choice for any circuit. However, it was chosen to demonstrate the loss improvement possible through micromachining. Similarly, the 50 Ω circuit yields excess insertion loss of 1.2 dB at 85 GHz, while the micromachined version reduces the loss to 0.8 dB, which also represents a 9% increase in combining efficiency.

The Wilkinson and right angle bend components are modeled yielding 0.5 dB excess loss at 85 GHz using Libra. Modeled results of the entire circuit, including the 2.1 mm of interconnects, show micromachined circuits with excess insertion loss values of 0.7 dB, closely matching the 50 Ω measured results. As previously established, the modeled 70 Ω component losses are conservative, particularly for the right angle bend. Thus the discrepancy between the modeled and measured insertion loss for the 70 Ω circuit. The modeled




(a) Measured.




(b) Modeled.

Figure 5.16: Excess insertion loss (above 3 dB nominal) of four Wilkinson plus bend circuits with 2.1 mm interconnect length.

insertion losses for the 50 and 70 Ω conventional circuits yield 0.9 and 1.1 dB excess insertion loss at 85 GHz, respectively. Thus the model predicts a 0.2-0.3 dB loss reduction while

measured results yield 0.4 dB improvements. The discrepancy is due to the conservative loss estimate of the component model.

Table 5.5: Estimated excess loss for 1:2 circuit networks as compared with measured results at 85 GHz. Interconnect loss is shown for 2.1 mm, and component loss is given for 1 Wilkinson and 1 bend. Measurement error is ± 0.1 dB

| Design 1:2 | Atten (dB/mm) | Intct Loss (dB) | Wilk, bend (dB) | Est loss (dB) | Meas loss (dB) | IE3D loss (dB) |
|---|---|---|---|---|---|---|
| 50 Ω FGC | 0.27 | 0.6 | 0.5 | 1.1 | 1.2 | 0.9 |
| 50 Ω MFGC | 0.19 | 0.4 | 0.5 | 0.9 | 0.9 | 0.75 |
| 70 Ω MFGC | 0.19 | 0.4 | 1.32 | 1.72 | 1.5 | 0.75 |
| 70 Ω FGC | 0.34 | 0.7 | 1.32 | 2.02 | 1.7 | 1.1 |

Table 5.5 summarizes the insertion losses of the four 1:2 networks at 85 GHz with three benchmarks: estimated measured loss, actual measured loss, and IE3D modeled loss. The estimated loss is the sum of the measured interconnecting line loss and the measured component loss. For example, the 50 Ω design includes 2.1 mm of interconnect line resulting with an estimated loss of approximately 0.6 dB. The measured component loss as taken from Table 5.3 is approximately 0.5 dB. The sum of these losses is approximately 1.1, which is 0.1 dB less than the total loss measured and 0.2 dB more than the IE3D predicted loss. These results match favorably and show modeled loss to be conservative as predicted. Thus all three loss benchmarks indicate insertion loss improvement of 0.15-0.2 dB with micromachining for the 50 Ω case and improvements of 0.2-0.4 dB for the 70 Ω case.

### 5.6.4 1:4 Combining Network

Shown in Figure 5.17 are 1:4 networks for 50 Ω micromachined and conventional designs. The input signal travels through 5.7 mm of interconnects, a reactive tee junction, two right angle bends, and one Wilkinson power divider, yielding 6 dB nominal loss. Measured and modeled insertion loss values are plotted in Figure 5.18. The model predicts insertion loss values of 2.2 and 2.3 dB above the nominal for the conventional 50 and 70 Ω designs at 85 GHz, respectively. The micromachined versions improve loss by 0.3 and 0.4 dB for the 50 and 70 Ω designs, respectively. Measurements of the 50 Ω designs yield similar improvements with 2.6 dB excess loss reduced to 2.0 dB with the micromachined circuit design.

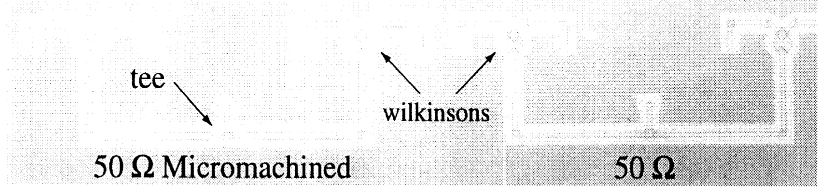
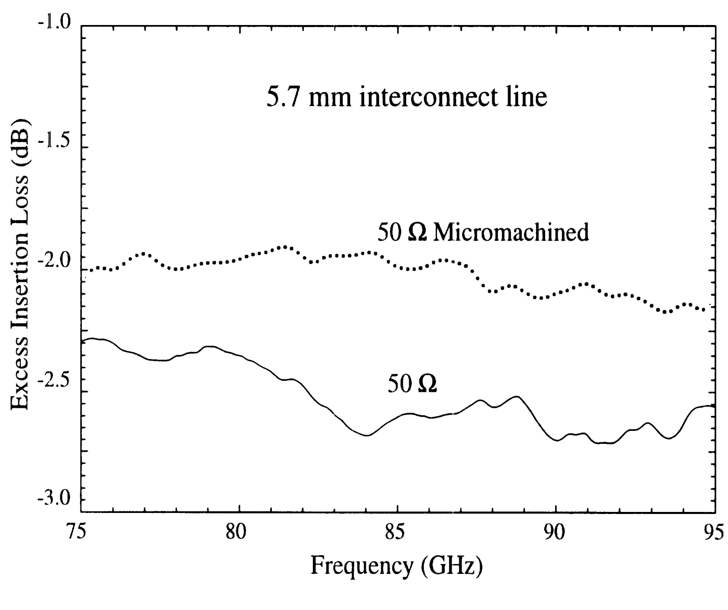
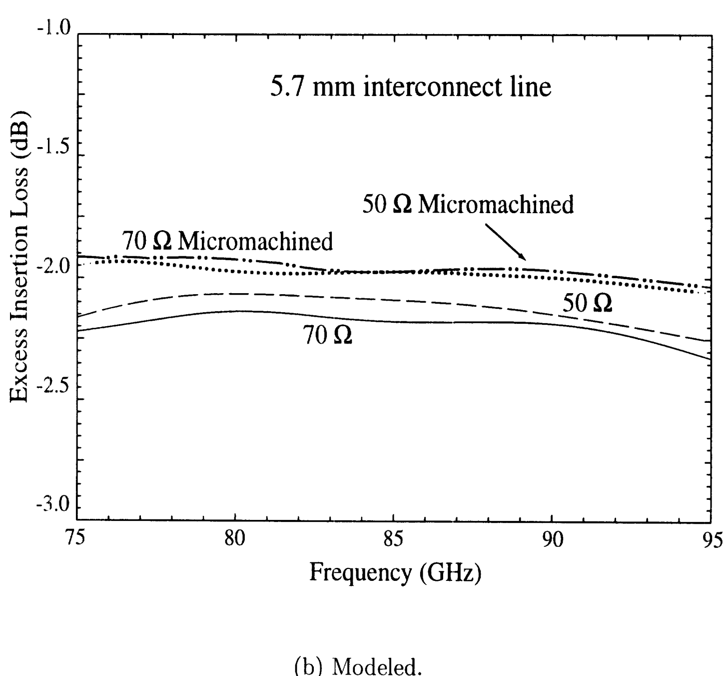



Figure 5.17: Photos of 1:4 networks.

Figure 5.19 demonstrates the potential in combining efficiency when interconnect lengths are extended up to 7 mm in a 1:4 combining network. A schematic of the combining circuit is embedded in the figure. Modeled excess loss and combining efficiency, beyond the nominal 6 dB, are plotted versus interconnect length for combining networks of each of the four lines. For example, a network of 4 mm in interconnect length provides 2.5 and 2.0 dB of excess loss for the 70 and 50 Ω conventional circuits, respectively, according to the modeled data. When micromachining is applied, these networks have excess losses of only 1.7 dB for the 70 and 50 Ω circuits. This difference of 0.3-0.8 dB can be quite substantial in a system with a goal of only 2 dB total loss, and becomes even more beneficial when several combining networks are used for multilayer applications or longer combining networks. As shown in Figure 5.19, a circuit signal path of 5 mm yields 2.9 dB of excess loss for the 70 Ω design which translates to only 48% efficiency. The corresponding micromachined design improves the combining efficiency by 1 dB to 15% with loss reduced to 1.9 dB. The 50 Ω design shows




(a) Measured.




(b) Modeled.

Figure 5.18: Excess insertion loss for 1:4 combining network with 5.6 mm interconnect length.

similar loss improvements, reducing the excess loss to 1.95 dB and 64 % efficiency. Also shown in Figure 5.19 are the measured values for the 50 Ω networks, presented in Figure

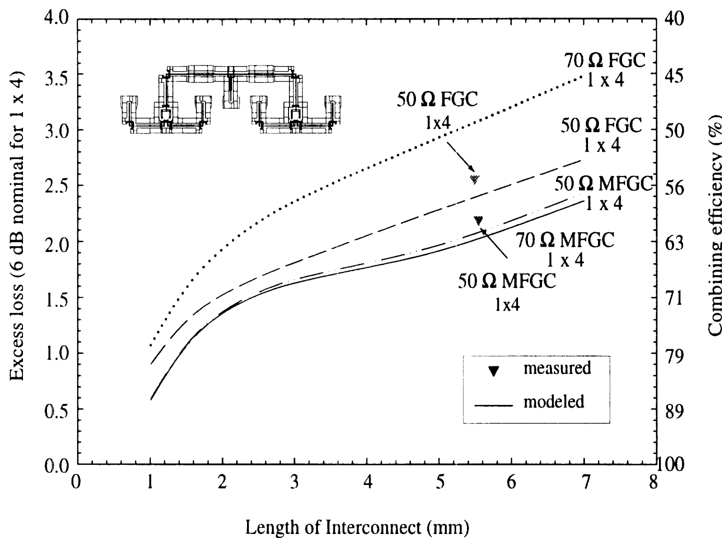
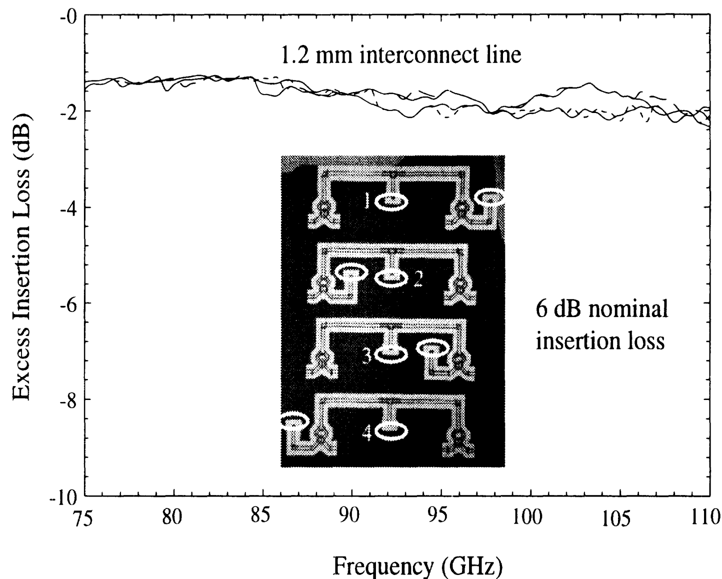


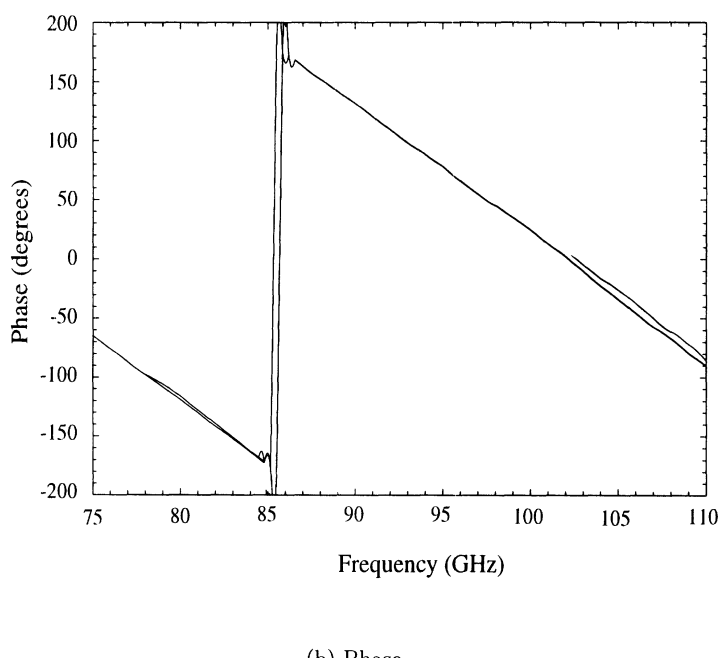

Figure 5.19: Excess loss and combining efficiency versus signal path length for micromachined and unmicromachined FGC lines.

5.19 as triangular data points. It has been observed that the length of interconnect within a circuit network may be equally important as the total interconnect length in terms of overall performance due to potential resonances along the bends and discontinuities. This is the reason for the non-linearity in the modeled curves of Figure 5.19. The line lengths have been added randomly in between components.

In measuring a 1:4 network, in which three of the four output ports are terminated with matched thin film resistors, it is important to establish power balance in each of the four signal paths. Ideally, one network would be fabricated and probes would be placed on the input port and on each of the four output ports. Since this measurement set-up is unavailable, four identical 1:4 networks are fabricated and each of the four output ports are measured separately. Figure 5.20(a) and 5.20(b) show the four measurements superimposed for insertion loss as well as phase for 50 Ω 1:4 networks. The total interconnecting line length is approximately 1.2 mm. All four measurements match closely, with insertion loss of 1.2 dB at 85 GHz ± 0.1 dB. The expected loss for this network at the same frequency is 1.2, which is the sum of the expected 0.84 dB component loss and the 0.33 dB line loss. An example of power imbalance in a 1:4 network is given in the appendices. Had micromachined been applied to this network, a 0.11 dB loss improvement would be expected based on the sum




(a) Insertion loss.




(b) Phase.

Figure 5.20: Example of signal balance in each of four 1:4 network output ports: a) Insertion loss (b) Phase.

of the expected component and line losses, and is within the error of the measurement.

Table 5.6 summarizes the insertion losses of the two 1:4 networks with 5.7 mm of in-

terconnecting lines at 85 GHz with three benchmarks: estimated measured loss, actual measured loss, and IE3D modeled loss. The estimated loss is the sum of the measured interconnecting line loss and the measured component loss. For example, the 50 Ω design includes 5.7 mm of interconnect line resulting with an estimated interconnect loss of approximately 1.6 dB. The measured component loss as taken from Table 5.3 is approximately 0.84 dB. The sum of these losses is approximately 2.4, which is 0.2 dB less than the total loss measured and 0.1 dB more than the IE3D predicted loss. For the micromachined case, the estimated loss is 1.94 dB and the measured loss is 2.0 dB and matches the IE3D model. Thus all three loss benchmarks indicate insertion loss improvement of 0.2-0.6 dB with micromachining.

Table 5.6: Estimated excess loss for 1:4 circuit networks as compared with measured results at 85 GHz. Interconnect loss is shown for 5.7 mm, and component loss is given for 1 Wilkinson, 1 tee, and 2 bends. Measurement error at 85 GHz is ± 0.1 dB.

| Design 1:4 | Atten (dB/mm) | Intct Loss (dB) | Wilk, 2 bends tee (dB) | Est loss (dB) | Meas loss (dB) | IE3D loss (dB) |
|---|---|---|---|---|---|---|
| 50 Ω FGC | 0.27 | 1.6 | 0.84 | 2.4 | 2.6 | 2.2 |
| 50 Ω MFGC | 0.19 | 1.1 | 0.84 | 1.9 | 2.0 | 2.0 |

### 5.6.5 1:8 Combining Network

Figure 5.21 shows photographs of four 1:8 networks consisting of one reactive tee, six Wilkinsons, and fourteen right angle bends. The total interconnecting length is approximately 6.8 mm for each signal path, which is physically required for this network, and has 9 dB nominal insertion loss. Figure 5.22 shows modeled results with 3 dB excess insertion loss for both micromachined cases and an additional 0.5 dB and 1 dB for the conventional 50 and 70 Ω FGC lines.

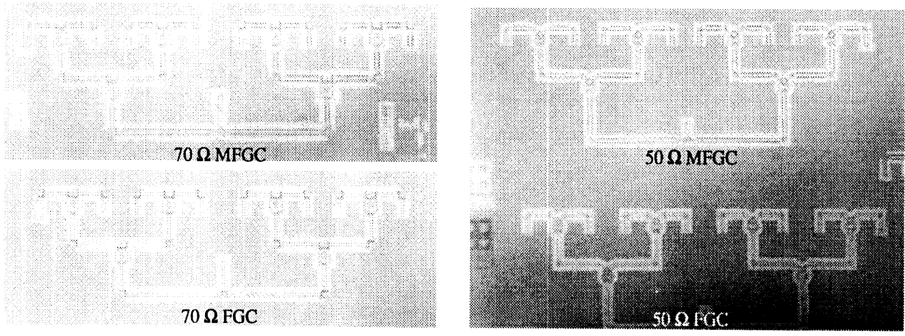



Figure 5.21: Photographs of fabricated 1:8 combining networks consisting of 1 reactive tee, 6 Wilkinsons, and 14 right angle bends.

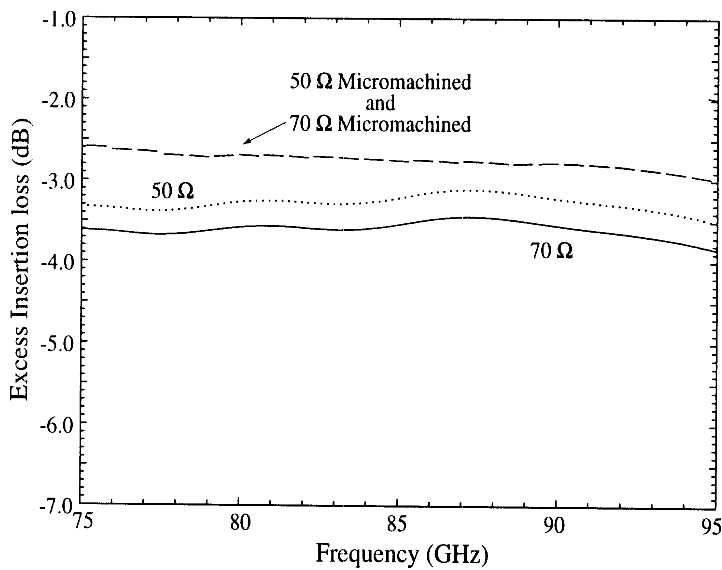


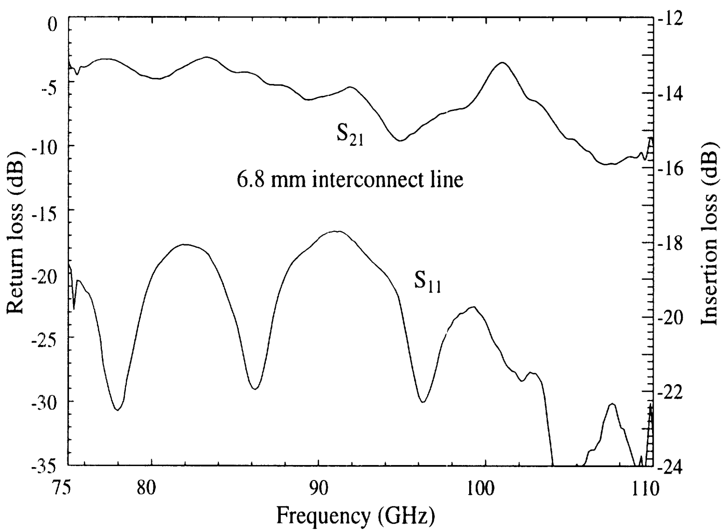

Figure 5.22: Modeled insertion loss for 1:8 combining networks.

Measured S-parameter results for the 50 Ω case are shown in Figure 5.23(a) with return losses below -17 dB from 75-110 GHz. Insertion loss values at 85 GHz are approximately 3 dB above the 9 dB nominal at 85 GHz. This loss is plotted with those of the three other circuit designs in Figure 5.23(b). At 85 GHz, the 70 Ω FGC 1:8 circuit is 7 dB above nominal. However, both micromachined circuit combining networks yield insertion losses close to 3 dB above nominal.

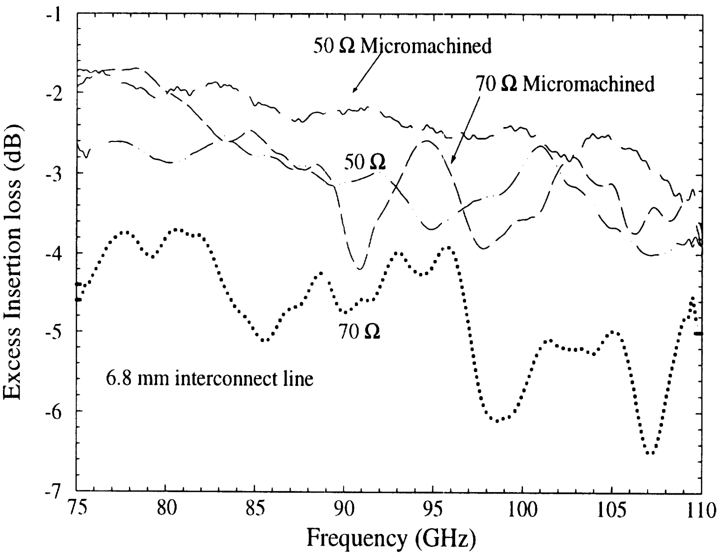
Table 5.7 summarizes the insertion losses of the four 1:8 networks at 85 GHz with three benchmarks: estimated measured loss, actual measured loss, and IE3D modeled loss. The estimated loss is the sum of the measured interconnecting line loss and the measured component loss. The 50 Ω design includes 6.7 mm of interconnect line resulting with an estimated loss of approximately 1.9 dB. The measured component loss as taken from Table 5.3 is approximately 1.34 dB. The sum of these losses is approximately 3.2, which is 0.3 dB more than the total loss measured and 0.1 dB more than the IE3D predicted loss. For the micromachined case, the estimated loss is 2.6 dB, the measured loss is 2.1 dB, and the IE3D model predicts 2.7 dB. The three loss benchmarks indicate insertion loss improvement of 0.4-0.8 dB for the 50 Ω case with micromachining, and 0.8-1.6 dB improvement for the 70 Ω case.

Table 5.7: Estimated excess loss for 1:8 circuit networks as compared with measured results at 85 GHz. Interconnect loss is shown for 6.8 mm, and component loss is given for 2 Wilkinsons, 1 tee, and 3 bends. Measurement error for the 50 and 70 Ω circuits is ± 0.2 and ± 0.4 dB, respectively.

| Design 1:8 | Atten (dB/mm) | Intct Loss (dB) | 2 Wilks,2 tees, 3 bends (dB) | Est loss (dB) | Meas loss (dB) | IE3D loss (dB) |
|---|---|---|---|---|---|---|
| 50 Ω FGC | 0.27 | 1.9 | 1.34 | 3.2 | 2.9 | 3.1 |
| 50 Ω MFGC | 0.19 | 1.3 | 1.34 | 2.6 | 2.1 | 2.7 |
| 70 Ω MFGC | 0.19 | 1.3 | 2.3 | 3.6 | 2.8 | 2.7 |
| 70 Ω FGC | 0.34 | 2.3 | 2.3 | 4.6 | 4.4 | 3.5 |




(a) Measured 1:8 combining network for 50 Ω design with 6.8 mm interconnect lengths.




(b) Insertion loss for all four networks.

Figure 5.23: Measured results for 1:8 combining networks.

## 5.7 Conclusions

In optimized combining network designs, parasitics from the junctions, bends, and Wilkinsons are minimized and the excess loss is determined by the interconnect length and interconnect loss. The ability to design a MFGC line for a particular characteristic impedance offers great flexibility in choosing an optimal low loss design. For this study, both 50 and 70 Ω Wilkinson power dividers, reactive tee junctions, and right angle bends were used to develop micromachined circuit combining networks. The modeled and measured MFGC lines were incorporated as interconnects in combining networks to demonstrate the effect of the interconnecting line as an influential loss mechanism.

Table 5.8 summarizes the attenuation results for the 1:2 (2.1 mm interconnect), 1:4 (5.7 mm interconnect), and 1:8 (6.8 mm interconnect) circuit combining networks presented in this chapter at 85 GHz. The estimated loss, measured loss, and IE3D modeled losses are shown with the last two rows of the table presenting the loss improvement obtained using micromachining. Depending on the circuit and its size, micromachining can improve the overall performance by 0.2-0.8 dB from 85-95 GHz. Likewise, micromachining applied to the 70 Ω designs improves the overall performance by 0.3-1.6 dB depending on circuit and size. When working at W-band, tenths of a dB in insertion loss are significant, especially when the total insertion loss goal of a multilayer circuit design is 2 dB.

Thus while maintaining a particular characteristic impedance, micromachined finite ground coplanar (MFGC) waveguides provide lower loss than the conventional alternative. When implemented into circuit combining networks in which half or more power is lost nominally, MFGC interconnects between components significantly reduce the excess loss. This loss improvement becomes more prominent with larger or multi-layer networks. Optimized circuit components are also essential to overall performance.

Table 5.8: Summary of excess insertion loss for 1:2, 1:4, and 1:8 circuit combining networks at 85 GHz. Error margins are excluded.

| Design | Est 1:2 dB | Meas 1:2 dB | IE3D 1:2 dB | Est 1:4 dB | Meas 1:4 dB | IE3D 1:4 dB | Est 1:8 dB | Meas 1:8 dB | IE3D 1:8 dB |
|---|---|---|---|---|---|---|---|---|---|
| 50 Ω FGC | 1.1 | 1.19 | 0.9 | 2.4 | 2.65 | 2.2 | 3.2 | 2.9 | 3.1 |
| 50 Ω MFGC | 0.9 | 0.88 | 0.75 | 1.9 | 2.0 | 2.0 | 2.6 | 2.1 | 2.7 |
| 70 Ω MFGC | 1.7 | 1.5 | 0.75 | n/a | n/a | n/a | 3.6 | 2.8 | 2.7 |
| 70 Ω FGC | 2.0 | 1.7 | 1.1 | n/a | n/a | n/a | 4.6 | 4.4 | 3.5 |
| Δ 50 | 0.2 | 0.31 | 0.15 | 0.5 | 0.6 | 0.2 | 0.6 | 0.8 | 0.4 |
| Δ 70 | 0.3 | 0.2 | 0.35 | n/a | n/a | n/a | 1.0 | 1.6 | 0.8 |

# CHAPTER 6

# MICROMACHINED W-BAND POWER CUBE

## 6.1 Introduction

High power requirements of typical radar systems for surveillance, communications, and guidance/detection, have necessitated the use of traditional waveguide architectures. Although these systems have satisfactory electrical performance, they are massive and costly. The advent of MMIC technology in the 1980's led to the expectation that high power monolithic circuits would solve these problems. However, the development of this technology has clearly demonstrated the difficulty in realizing high power systems in monolithic form. The main reasons for this power limitation are low power MMIC devices, high-loss interconnects and passive components, low-efficiency planar antennas, and limited integration capability.

The need to develop microwave monolithic circuits with high-power and low-cost leads to the following requirements for optimum high-frequency performance: lightweight hardware, high-density interconnect technology, high reliability, and advanced packaging. The development of high-power microwave circuits with both small size and low cost pose serious challenges. The response to this challenge is to use novel concepts in circuit design, fabrication, and implementation to establish significant new benchmarks in power output.

If several tens of watts of radiated power can be economically produced, applications such as moderate range adverse weather radars, weapon seakers, and tactical data links can be greatly enhanced in effectiveness and capability. The purpose of the Power Cube project is to do just that by developing a multi-layer silicon transmit array using silicon

micromachining and InP MMIC medium power amplifiers. Figure 6.1 compares the micromachined W-band power cube to a waveguide amplifier, consisting of an silicon IMPATT diode rather than the InP HEMT amplifiers used for this project. Characteristics of both structures are provided in Table 6.1, and show the waveguide amplifier as six times more costly and requiring twenty-one times more volume. As low cost and low volume are critical features in today's technology market, the development of a silicon micromachined power cube has become a worthwhile endeavor.

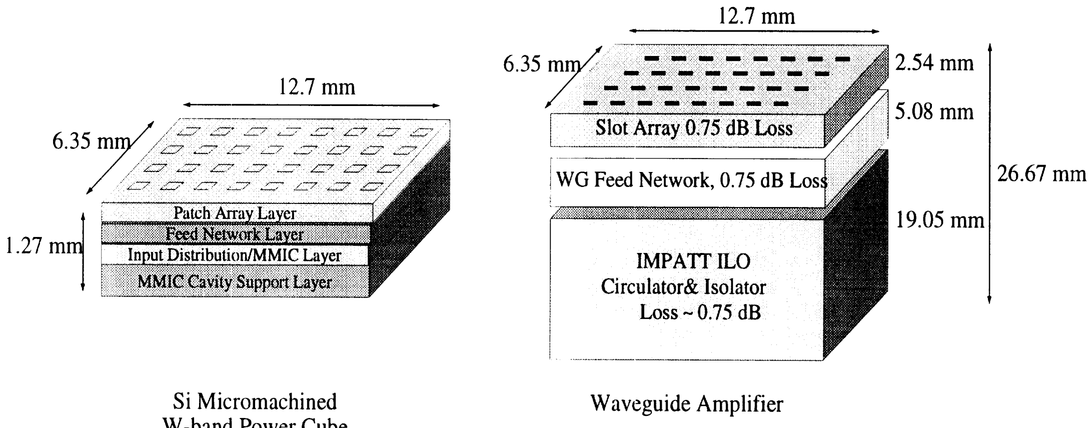



Figure 6.1: W-band micromachined power cube versus waveguide amplifier (courtesy Dr. Robert T. Kihm).

Table 6.1: Comparison of predicted W-band power cube performance and comparable waveguide amplifier (courtesy Dr. Robert T. Kihm).

| | Si Micromachined Power Cube | Waveguide Amplifier |
|---|---|---|
| $P_{rad}$ | 0.16 W | 0.28 W |
| Vol/wt | 102 mm$^3$/0.47g | 2150 mm$^3$/g |
| Active Device | InP HEMT Amplifier | Si IMPATT Diode |
| Est. Device Cost | $200 (8 chips) | $1000 (1 diode) |
| Fab/Assy Cost | $35 (Semi-automated) | $1500 (EDM+CCmilling) |
| Adjust/Tune | $0 | $100(2 hrs) |
| Cost/$P_{rad}$ | $1468/W | $9286/W |

## 6.2 Power Cube Overview

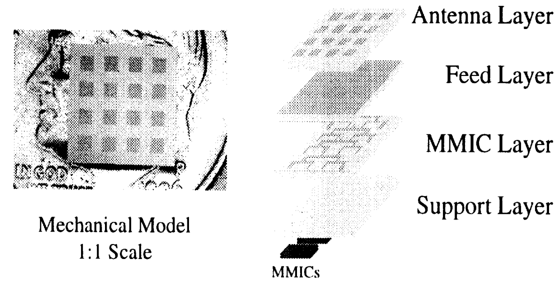



Figure 6.2: Model of micromachined power cube.

The Micromachined W-Band Power Cube project is a 30-month collaborative MAFET Thrust 3 program with Hughes/Raytheon, Jet Propulsion Laboratory (JPL), HRL Laboratories, and The University of Michigan. The goal of this project is to develop a 0.007 $in^3$ (102 $mm^3$) multilayer silicon transmit array building block (Figure 6.2) with 2 Watts/$in^2$ radiated power density by merging several complementary technologies. The University of Michigan's micromachined W-band component fabrication using silicon processing technology is responsible for design and fabrication of all passive components, including interconnecting transmission lines, vertical interconnects, power distribution networks, and patch antenna array elements. The 50 mW InP HEMT W-band flip-chip MMIC power amplifiers are designed and fabricated at HRL Laboratories. HRL is also responsible for development of microwave flip chip device bump technology. Finally, JPL's experience with advanced metallization systems to bond stacked silicon layers is utilized. However, U of M is ultimately responsible for silicon wafer bonding. Thus, the technical challenges involved for this project are high density component integration, reliable high-density flip-chip bumps, high yield 50 mW indium phosphide (InP) HEMT MMICs, and high thermal conductivity interlayer bonding.

As shown in Figures 6.3 and 6.4, the goal of the project is to power sixteen aperture-coupled, cavity backed microstrip patch antenna elements on the top silicon layer of a multilayer structure in a four-by-four array. Element to element spacing of $\lambda_g/2$ makes the array area approximately 36 $mm^2$. The input signal is divided into four through a

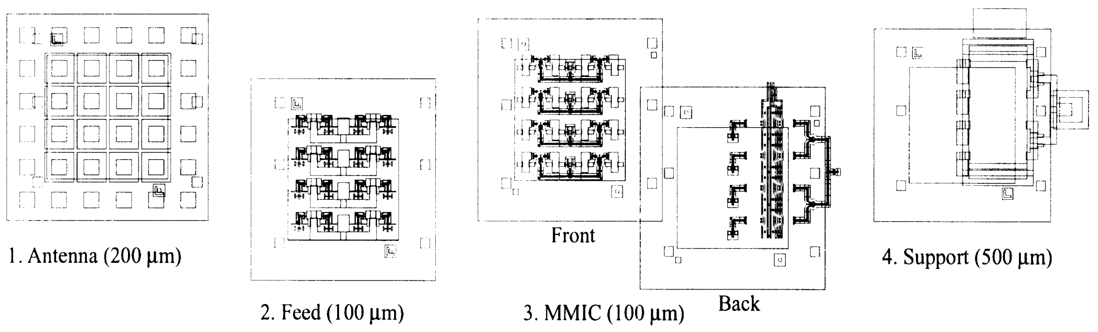



Figure 6.3: Illustration of power cube layers.

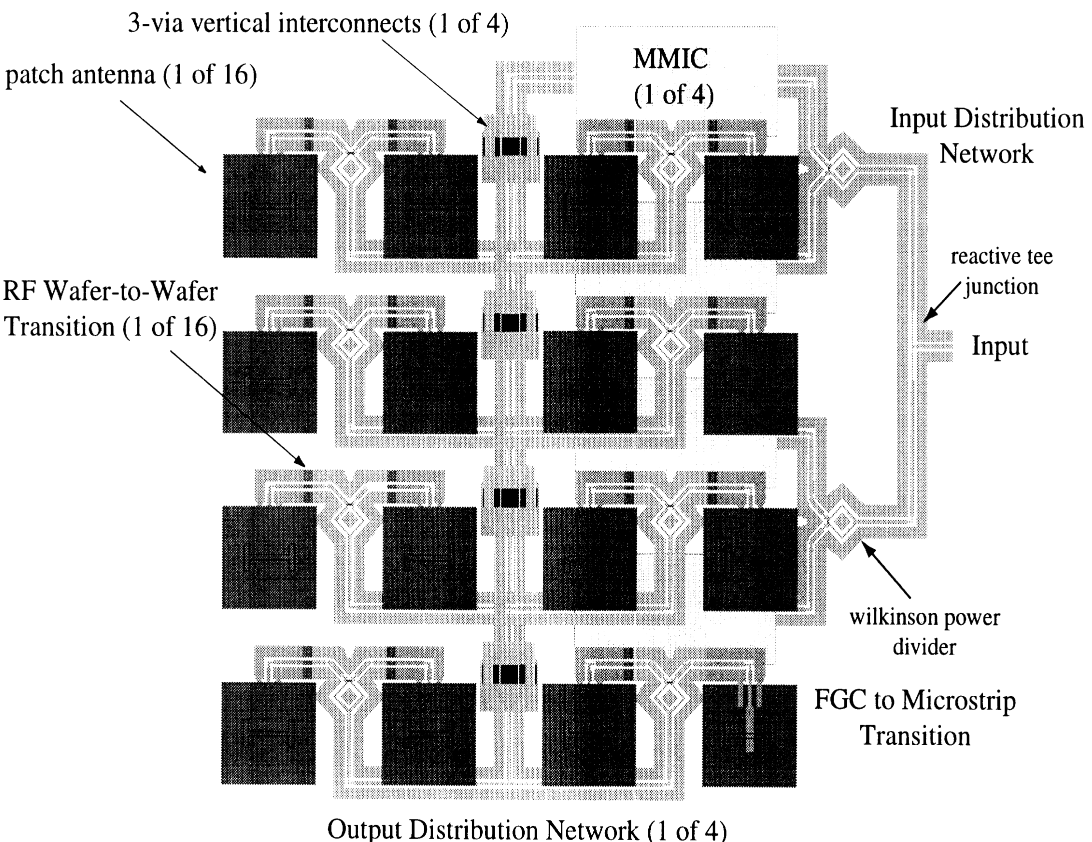



Figure 6.4: Top view illustration of power cube layers.

power distribution network consisting of one reactive tee junction, two Wilkinson power dividers, and six right angle bends on finite ground coplanar waveguide. As the signal power is equally divided twice, each of the four FGC output signals is reduced by 6 dB of nominal loss before feeding into the four flip-chip bonded InP MMIC amplifiers. These four

amplified FGC output signals propagate through 100 micron high vertical interconnects to emerge on the other side of the silicon wafer, and are then divided laterally into four output distribution networks, which are identical to the input distribution network. Since each of the signals is divided into four, sixteen feed signals result with 6 dB of nominal loss. Vertical transmission to the next silicon layer is achieved using wafer-to-wafer transitions. After transitioning to this layer, the FGC line is transformed to microstrip in order to feed the sixteen aperture-coupled micromachined patch antennas in phase.

## 6.3 Passive Component Integration

Passive components developed for the Power Cube project include the micromachined patch antenna, FGC to microstrip transition, lateral distribution network, single layer vertical interconnect, and wafer-to-wafer vertical interconnect. All of these components have been designed considering thinned high-resistivity (3000 $\Omega$-cm) silicon wafer thicknesses of 100 or 200 $\mu$m.

In order to acknowledge my colleagues' contributions to the project, a brief discussion of the antenna and distribution network is warranted. The aperture-coupled micromachined patch antenna and FGC-to-microstrip transition were developed by Dr. Gauthier and Dr. Raskin [34, 33]. Measured return loss of -18 dB at 94 GHz was achieved for an individual antenna with maximum efficiency of 58 $\pm$8%. Radiation patterns show a measured front-to-back ratio of -15 dB at 94 GHz. The distribution network, which consists of one reactive tee junction, two Wilkinson power dividers, and six right angle bends on finite ground coplanar waveguide, was originally designed by Prof. Thomas Weller and fabricated as a packaged network by Dr. Henderson [118].

The component contributions from this dissertation are the following: single wafer vertical interconnects (Chapter 3), wafer-to-wafer transitions (Chapter 4), and modified distribution networks (Chapter 5). In addition to individual components, this dissertation includes the following: passive component integration, fabrication integration, MMIC and Support Layer fabrication, bonding, and passive component measurements.

### 6.3.1 Packaging and Coupling Effects

Passive component integration includes finalizing the layout and design of all four layers. This, in turn, requires investigation of coupling and packaging in multilayer configurations. As shown in Figure 6.5, the MMIC layer is the most complex layer as it involves power distribution networks on both sides, vertical interconnects, solderable nickel pads, bonding pads, and RF wafer-to-wafer interconnects. The top of the Feed Layer consists of sixteen slots for patch antenna excitation and gold metallization elsewhere. As planar transmission lines may be adversely affected by nearby dielectric and conductive materials, it is important to investigate the effect of this metal plane and other neighboring FGC lines on the electrical signal at any point in the power cube. This is done by simulating various portions of the power cube in which the propagating FGC signal is in close proximity to other FGC lines or conductors laterally or vertically. Isolation of the FGC signals is critically important when attempting to maintain phase balance of one signal, which is split into sixteen signals both laterally and vertically through three silicon layers.

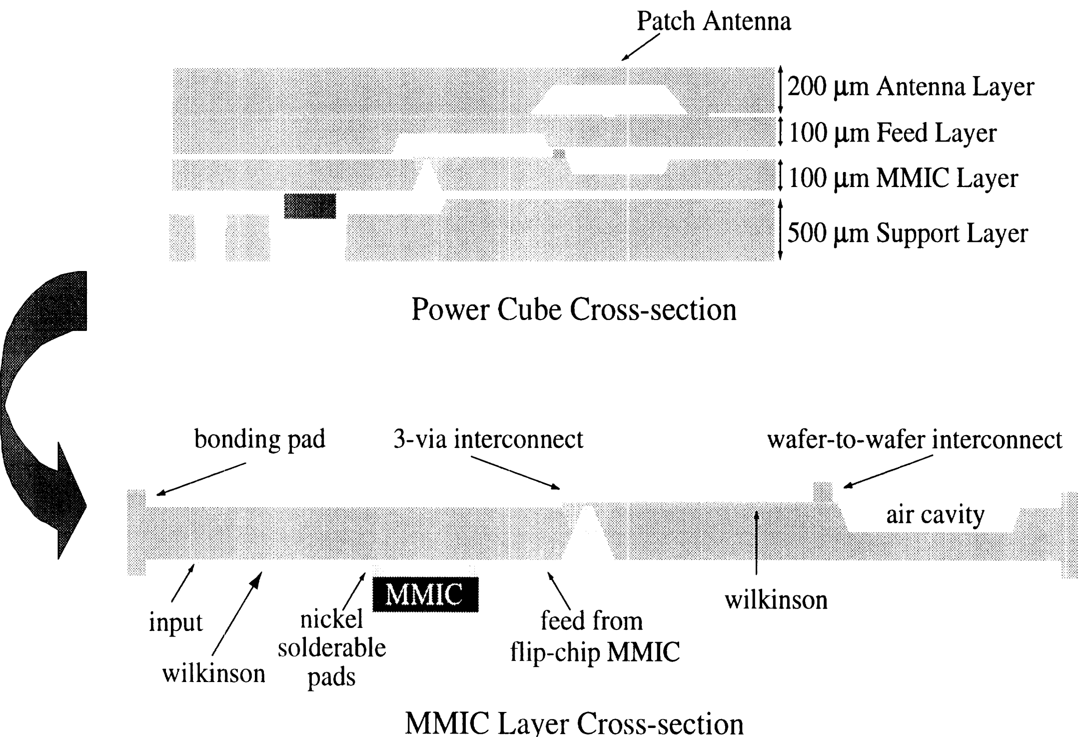



Figure 6.5: Cross section of power cube layers with close-up of MMIC layer cross section.

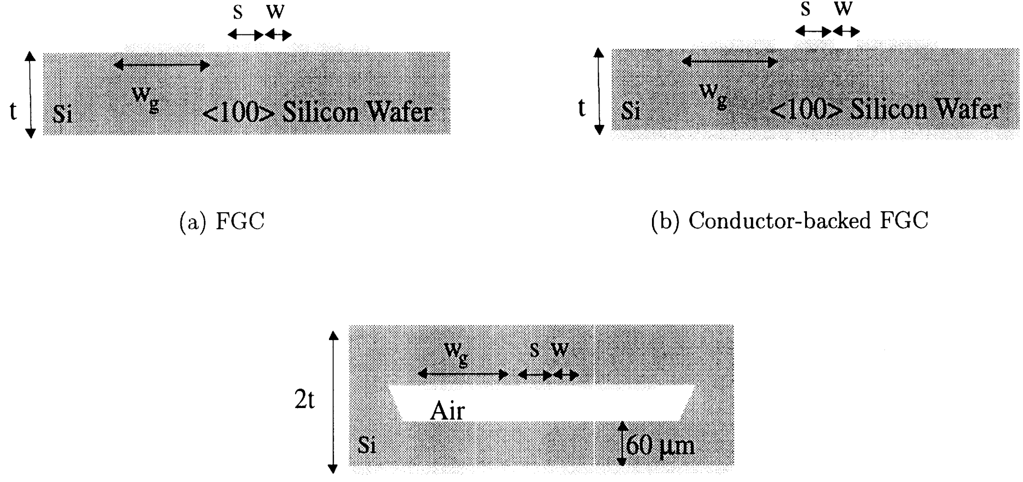
### Introduction

Although the electromagnetic fields in finite ground coplanar waveguides (FGC) are fairly well confined to the aperture regions, it is important to minimize interactions between adjacent circuits, especially in high density configurations. This interaction, known as crosstalk, may be due to substrate modes or parasitic coupling capacitance, and results in degraded electrical performance. In high-density circuits, on-wafer packaging becomes an important means of isolating circuits while preserving performance integrity. With multi-layered configurations, the vertical stacking of substrates necessitates a thorough understanding of propagating wave effects due to the surrounding environment. Figure 6.5 shows the specific high density three-dimensional application of interest, which consists of multiple conductive and dielectric layers.

This section addresses multilayer integration, as pertains to the power cube, by examining the effects of parasitic coupling between conductor planes and finite ground coplanar (FGC) lines printed on silicon substrate layers. The presence of parasitic modes due to close proximity of conducting metals is addressed and techniques to eliminate them are presented. Two line architectures appropriate for multilayer circuits are examined and their performance is discussed. Simulated results validate experimental data and assist in proposing performance enhancement solutions for multi-line multilayer environments.

### Line Architecture

The conventional FGC line, shown in Figure 6.6(a), demonstrates low-loss performance at frequencies as high as W- and D-bands. When a lower ground plane is added to the wafer, as may happen in a multilayer environment (Figure 6.6(b)), the line characteristics change slightly. The impedance decreases by a few ohms and the effective dielectric constant increases by a few tenths. This suggests that even though the field lines are concentrated in the aperture regions, the presence of a conductor through the silicon substrate attracts the fields slightly more into the substrate. When the FGC line is separated from the ground plane by a Si-micromachined cavity [84, 94], as shown in Figure 6.6(c), the characteristic impedance and effective dielectric constant are unaffected by the presence of




(a) FGC

(b) Conductor-backed FGC

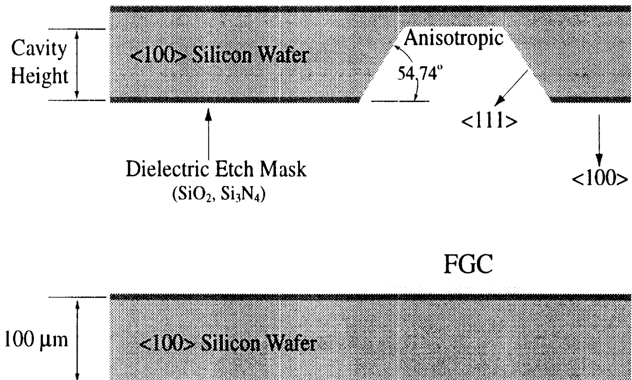
(c) Cavity-backed Micromachined FGC

Figure 6.6: Line architectures for multilayer circuits.

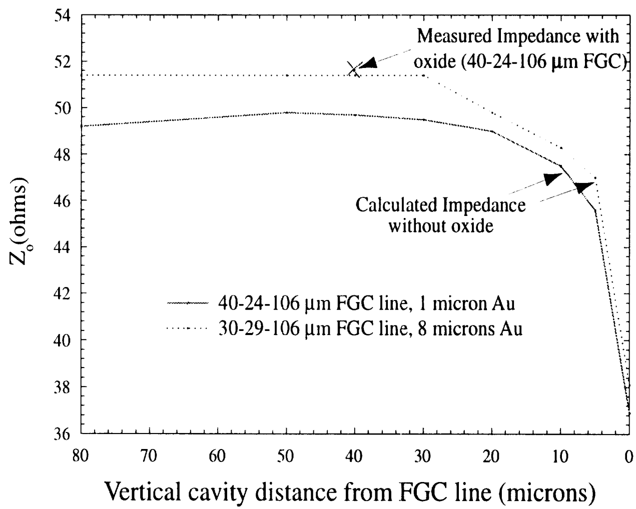
the ground plane. This architecture provides protection for air bridges as well. Herein, the two architectures of Figures 6.6(b) and 6.6(c) are examined as candidates for multilayer environments.

Micromachined air-dielectric cavities have been utilized to improve performance in a variety of high frequency antenna and circuit designs. For example, when air-dielectric cavities are placed beneath microstrip patch antennas, antenna efficiency is improved due to suppression of parasitic surface waves [84, 33]. Air-filled shielding cavities have also been used to realize high-density, low cost packages for microstrip and CPW circuits [94],[29].

Figure 6.7(a) shows a cross-section of a micromachined air cavity over an FGC line. To understand the effects of these cavities on line characteristics, a static solver [5] is utilized to perform a parametric study of the most critical parameter: cavity height. From Figure 6.7(b), in which impedance of two FGC lines is plotted as a function of cavity height, it can be seen that a cavity height below 30 $\mu$m affects the impedance of an 8 $\mu$m line while a cavity height below 20 $\mu$m affects the impedance of a 1 $\mu$m line. Note the FGC lines differ in aspect ratio as well as thickness. Impedance perturbation is chosen as the performance indicator for cavity height variation because it is a line characteristic reflecting




(a) Schematic of micromachined cavity over FGC line




(b) Effect of cavity height on FGC line.

Figure 6.7: Determination of cavity height.

capacitance, inductance, and resistance of the line. Modifications in these parameters due to surrounding dielectrics and conductors are reflected in the characteristic impedance. From this information obtained in Figure 6.7(b), a 40 $\mu$m cavity height is chosen for the power cube micromachined cavities over 1 $\mu$m FGC lines with dimensions 40-24-106 $\mu$m.

### Multi-Line Architecture Performance

In addition to studying a single circuit in a multi-layer environment, coupling effects between adjacent circuits are examined in order to fully understand trade-offs in the design

of high-density multilayer circuits. FGC lines in close proximity both laterally and vertically are considered, and all lines have 40 $\mu$m center conductors, 24 $\mu$m apertures, and 106 $\mu$m ground planes. Numerical simulations are performed as shown in Figure 6.8, with the two transmission lines on the same lateral plane or separated vertically using an integral equation based solver [132]. The cross-coupling is taken as the insertion loss between ports 1 and 2, with the two remaining ports left open-circuited for all coupling results. Terminating the remaining open ports with 50 $\Omega$ loads improves the insertion loss by 6 dB. Thus the coupling shown here is the worst case scenario.

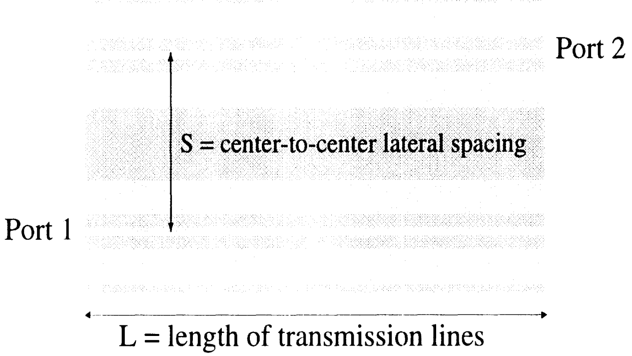
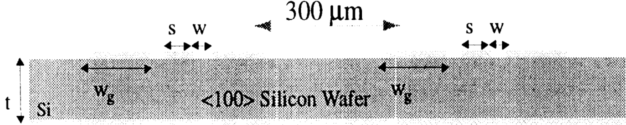



Figure 6.8: Layout of FGC lines for coupling simulations.

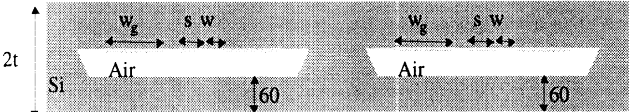
Figure 6.9 shows the cross-sectional views of the two line architectures printed on the same plane and separated laterally by 300 $\mu$m. Simulation results are shown in Figure 6.10 for the two architectures of length 1300 $\mu$m. Isolation below -40 dB from 75-110 GHz is provided by the cavity-backed micromachined line, while the conductor-backed line can couple to as much as -20 dB at 100 GHz.

To analyze the coupling effects in vertically integrated multilayer transmission lines, the same integral equation based numerical solver is used [132]. The lateral spacing between lines varies from 0 to 400 $\mu$m center-to-center, and cross coupling is simulated by measuring the insertion loss across ports 1 and 2 and leaving the remaining two ports open. Cross sections for the simulations are shown in Figures 6.11(a) and 6.12(a).

Simulated results for Figure 6.11(a) show a ripple in cross coupling ($S_{21}$) due to parasitics for line separations of less than 300 $\mu$m. The level of coupling for the lines separated by




(a) Conductor backed FGC




(b) Cavity backed micromachined FGC

Figure 6.9: Cross-sectional views for isolation simulations of two line architectures: a) Conductor-backed FGC b) Cavity-backed micromachined FGC.

0 and 100 $\mu$m is as high as -10 dB near the design frequency as shown in Figure 6.11(b). By introducing an air-dielectric layer between the metal conductors (Figure 6.12(a)), the ripple is eliminated completely and the coupling level for the closest spacing reduces to -18 dB as seen in Figure 6.12(b).

In summary, the performance of W-band circuits may be degraded when placed in a multi-conductor environment. Silicon micromachined, air-dielectric shielding cavities, realized between the two, reduces the parasitic coupling and maximizes propagation efficiency. This inhomogeneous line architecture, using silicon micromachining is ideal for multilayer integrated circuits. As pertains to the power cube, shielding cavities of 40 $\mu$m are implemented and separation between vertical lines is no less than 300 $\mu$m, keeping line-to-line coupling below -50 dB.

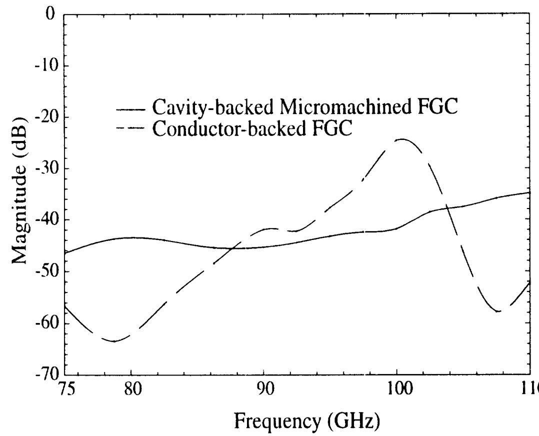
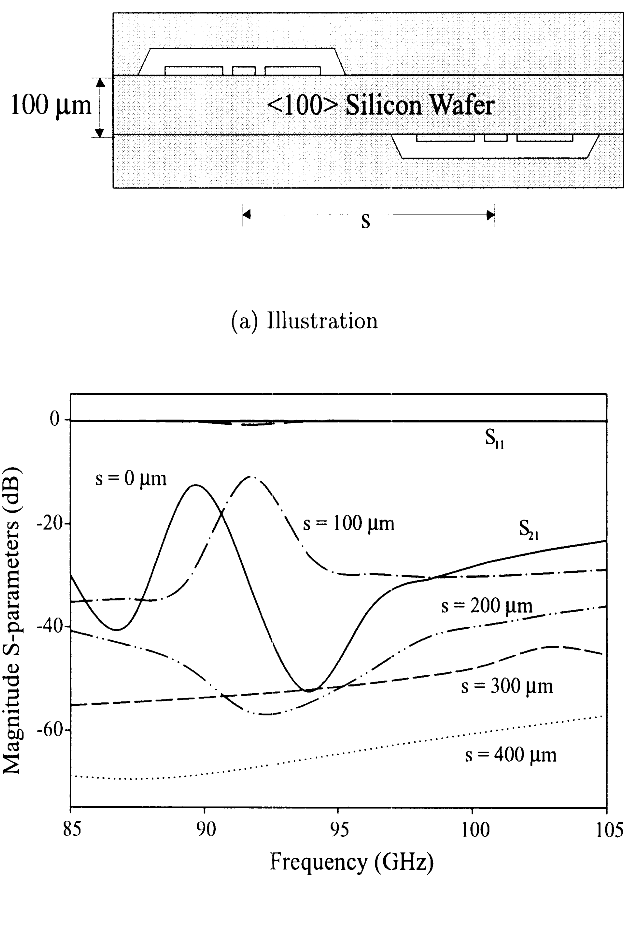


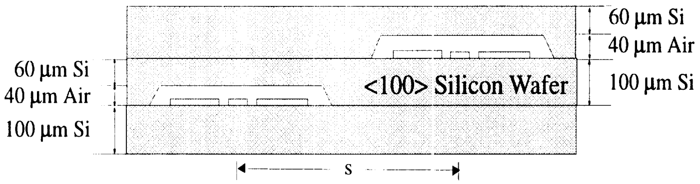

Figure 6.10: Simulation of architectures of Figure 6.9.



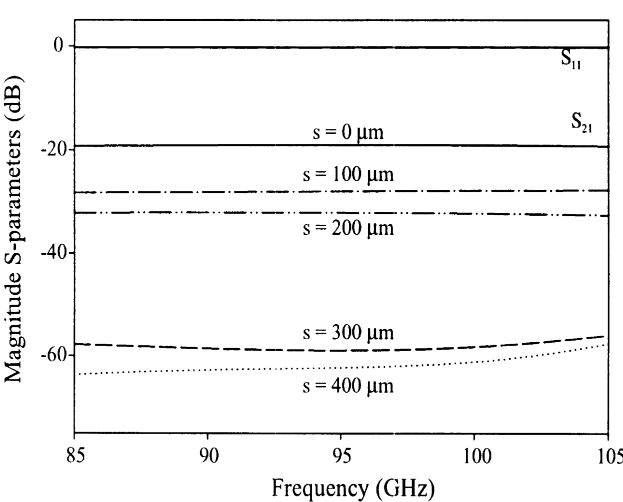

(a) Illustration

(b) Simulated S-parameters

Figure 6.11: FGC-to-FGC coupling through 100 microns Si. a) Illustration b) Simulated S-parameters. Note s equals the center-to-center lateral spacing.




(a) Illustration




(b) Simulated S-parameters

Figure 6.12: FGC-to-FGC coupling through 60 microns Si and 40 microns air cavity. a) Illustration b) Simulated S-parameters. Note s equals the center-to-center lateral spacing.

### 6.3.2 Fabrication

Fabrication of an individual component is much simpler than integrating and fabricating all components together because of the many compatibility issues that arise. For example, formation of the vertical interconnects dictates anisotropic etching of the vias prior to metallization. However, it is very difficult to pattern circuit metal around pre-existing micromachined areas, as in the case of the RF wafer-to-wafer interconnects and adjacent micromachined cavities. In other words, if a silicon region is micromachined and photoresist is spun on the sample, a wave of hills and valleys surrounds the micromachined edges making clean, uniform removal or application of photoresist difficult along the micromachined edges. Because of these and other issues, much time is spent developing the processes for each of the power cube wafers, integrating all of the component fabrication processes into a successful one.

Although all four wafer fabrication flows involve double-sided processing of high-resistivity (3000 $\Omega$-cm) silicon wafers, the MMIC layer fabrication flow is significantly more complex. The Support layer is 500 $\mu$m thick with only 7 steps, and the Antenna layer is 200 $\mu$m thick with 6 steps. Although both Feed and MMIC layers are thinned to 100 $\mu$m, the Feed Layer requires 11 steps as compared to the 19 steps required for the MMIC layer. As shown in Figure 6.13, this is due to the input/output distribution networks, vertical interconnects, dc bias lines, etc. Detailed fabrication information is given in the appendices for each power cube layer, however, discussion of the MMIC layer fabrication is presented here. Note that wafers thinned to 100 $\mu$m fracture much more easily than the conventional 500 $\mu$m silicon wafers, and special care is taken to protect them.

The MMIC layer wafers are scribed into 2 inch squares with 4000 Å $SiO_2$ on both sides. Since they are thinned to 100 $\mu$m, they are mounted on glass slides for each process step. The glass supports allow for easier handling and reduce probability for wafer fracture. Figure 6.14 illustrates the initial fabrication sequence, in which tantalum nitride (TaN) resistors are patterned first, and protected with a thin layer of PECVD nitride. After placing protective gold patches at the smaller via base locations, and patterning the via silicon dioxide ($SiO_2$), vias are anisotropically etched on both sides of the wafer. After selectively removing the

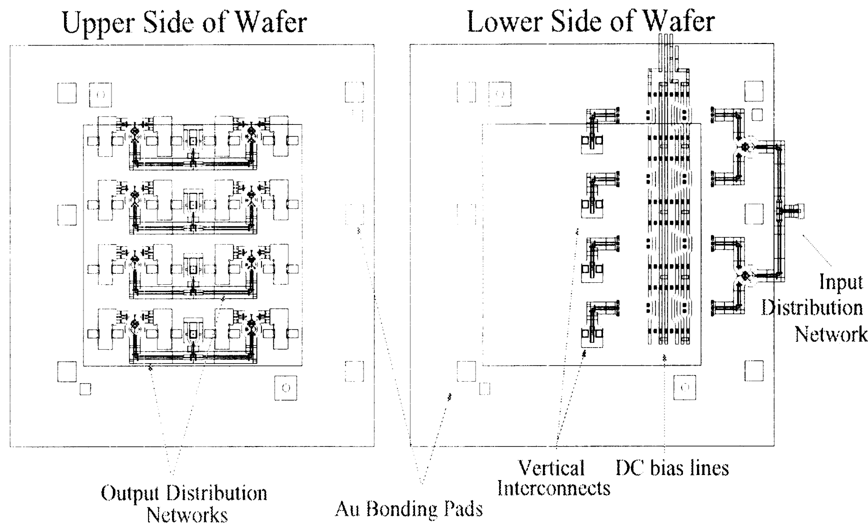



Figure 6.13: Upper and lower sides of MMIC layer, illustrating complexity of fabrication.

remaining $SiO_2$ from the via periphery, the circuit metal is evaporated simultaneously on the lateral surfaces and within the vias. This is done to both wafer sides using a modified lift-off process. The next step is the fabrication of the nickel solderable pads on the dc bias lines. These pads consist of a 60 $\mu$m circle of Au/Ni/Au (250/3000/500 Å), with an overlapping ring of Cr (5000 Å). The nickel provides a barrier to the underlying gold during the MMIC bumping process. It is covered with a thin film of gold to prevent oxidation and the chrome ring acts as a solder stop. Air bridges and the RF wafer-to-wafer interconnects are electro-plated simultaneously in a cyanide-based solution. The final step is anisotropic etching of the cavities to 40 $\mu$m.

This process did not result in a high yield. One reason for this is the anisotropic etchants ability to attack the TaN resistors despite the PECVD nitride covering. They appear to be attacked from underneath the TaN. Also two separate etching steps complicate the process run. The reason for the separate etches is the need for etching before circuit metallization and the difficulty in patterning FGC lines in close proximity to partially etched cavities.

Figure 6.15 shows a solution to these issues and the final fabrication sequence used for the MMIC layer. In this process, after patterning protective Au patches and patterning

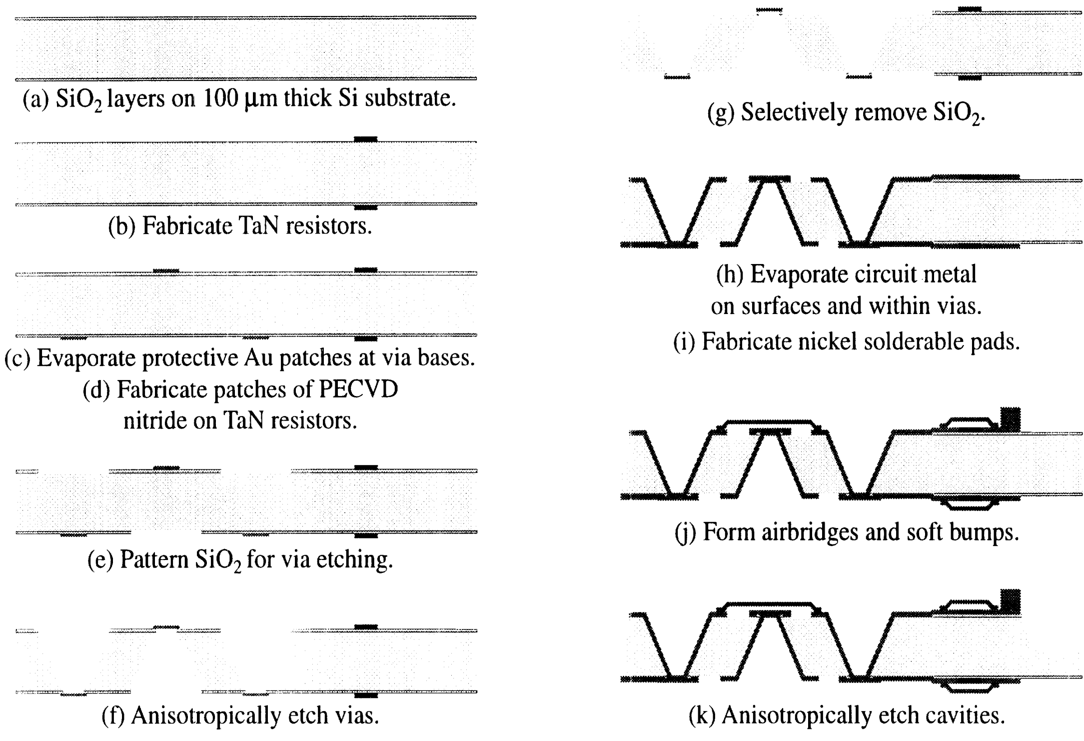



Figure 6.14: Fabrication flow.

the $SiO_2$, simultaneous anisotropic etching of the vias and cavities is performed. The TaN resistors are patterned using a lift-off process and are never exposed to the anisotropic etchant. This also eliminates the need for PECVD nitride. Simultaneous metallization of the circuit metal and vertical interconnects is completed as before. After fabrication of the nickel solderable pads, the air bridges and RF wafer-to-wafer transitions are electroplated. For this final step, the RF wafer-to-wafer transitions were moved 30 $\mu$m away from the cavity edge, easing the patterning process.

Photographs of the fabricated layers are shown in Figures 6.16 and 6.17. Figure 6.18 contains close-ups of the upper side of the MMIC layer, including reactive tee junctions, Wilkinson power dividers, TaN resistors, air bridges and RF electroplated wafer-to-wafer interconnects. The other side of the MMIC layer is shown in Figure 6.19, with close-up photos of the dc bias lines and vertical interconnects. It is also important to show the success of the vertical interconnect fabrication. Figure 6.20 reveals the uniform step coverage and adhesion around the rim of the via as well as the adhesion to the via floor and sidewalls.

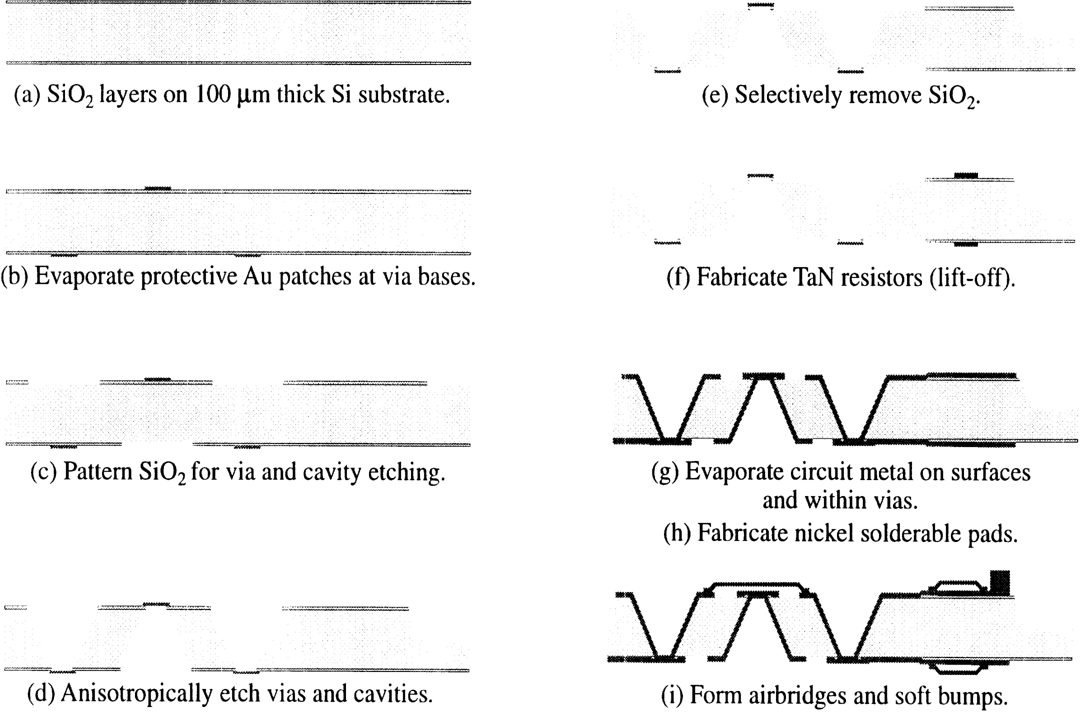



Figure 6.15: Revised fabrication flow.

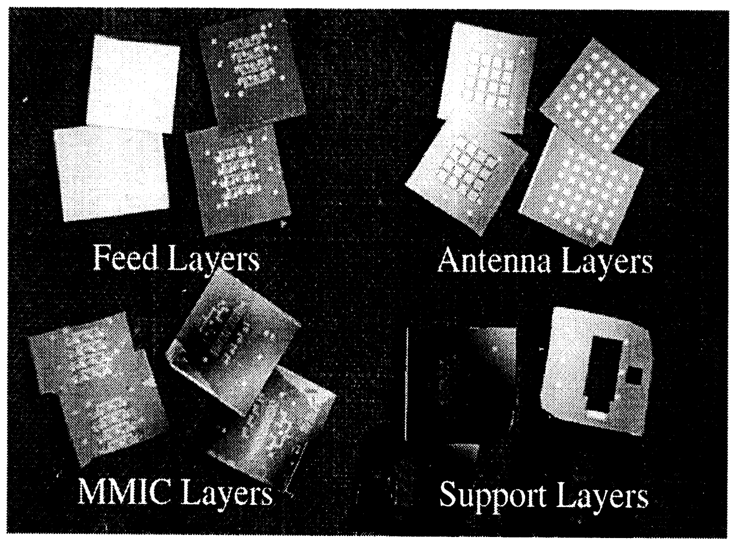



Figure 6.16: Photos of fabricated power cube layers.

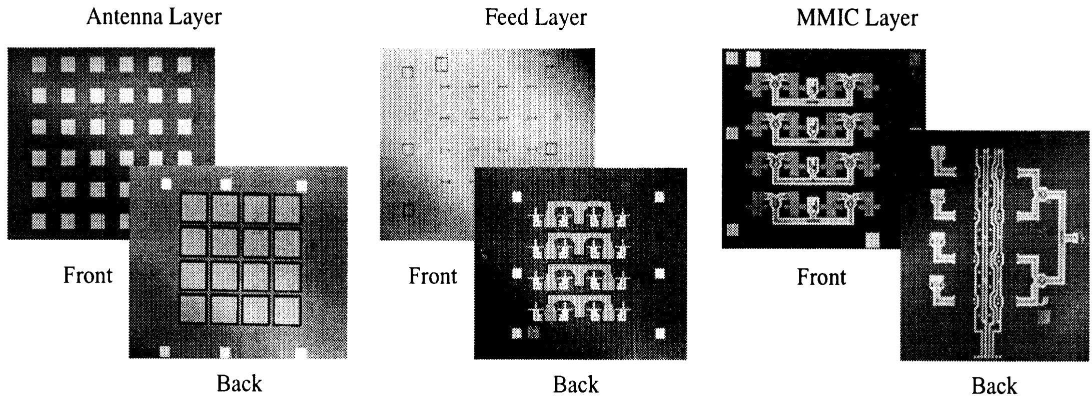



Figure 6.17: Photos of fabricated power cube layers.

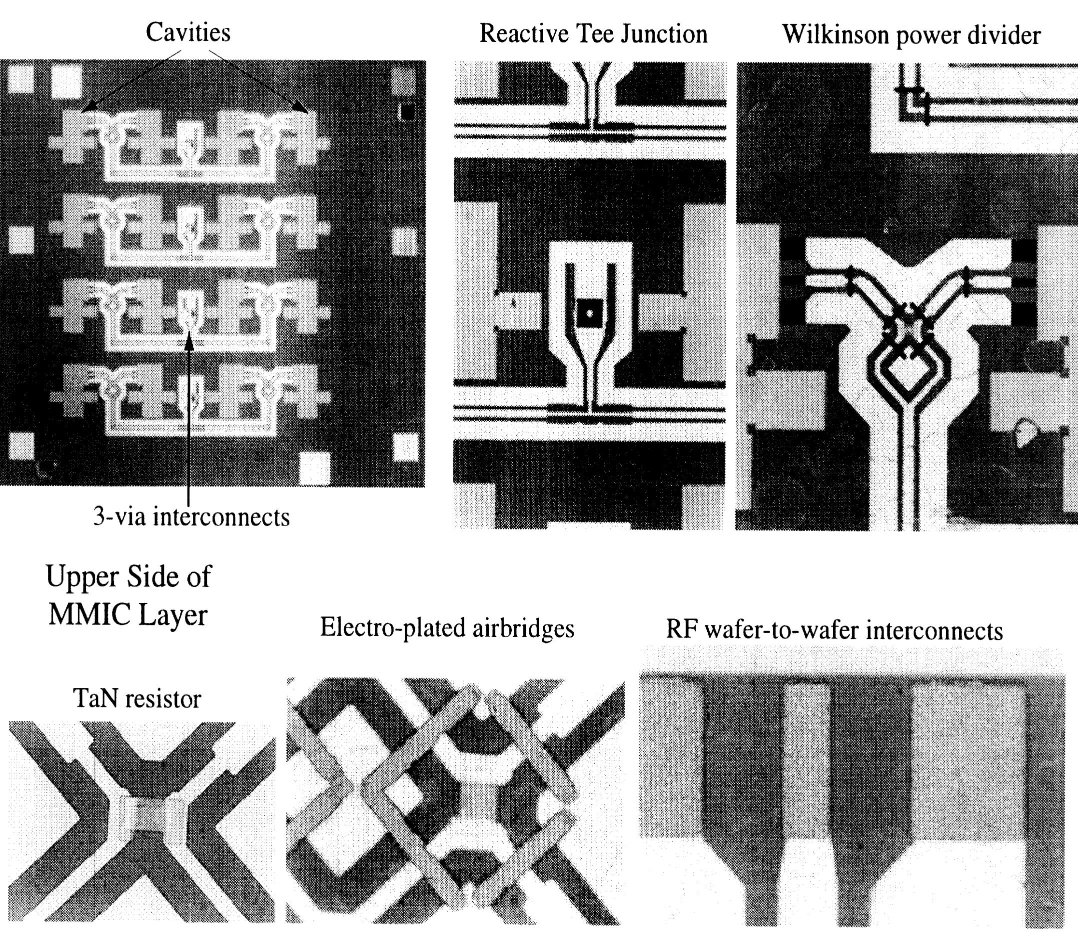



Figure 6.18: Photos of upper side MMIC layer.

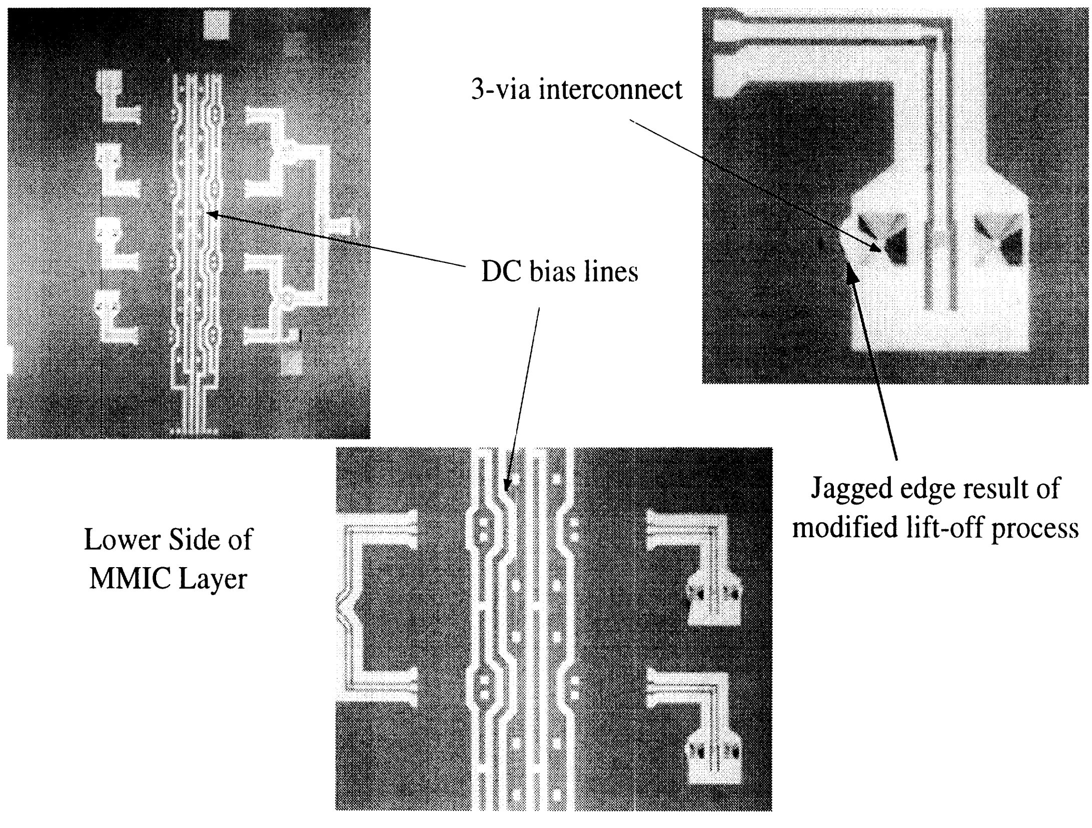



Figure 6.19: Photos of lower side MMIC layer.

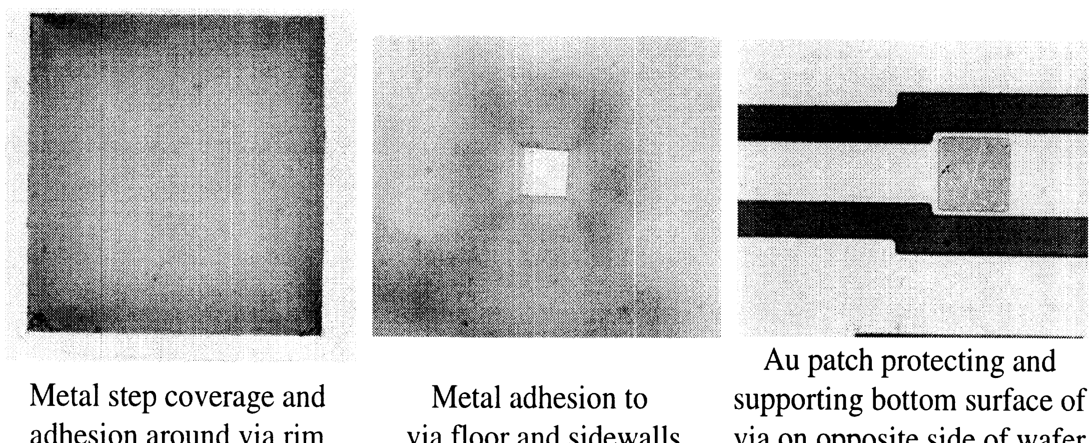


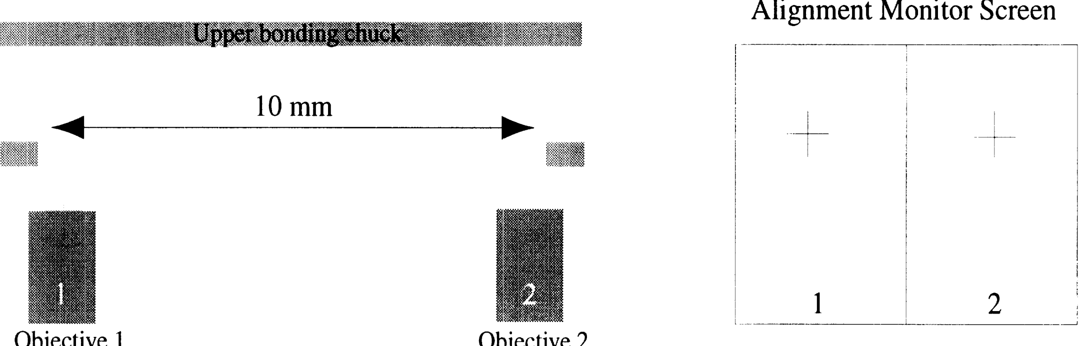

Figure 6.20: Via photos.

## 6.4 Wafer Alignment and Bonding

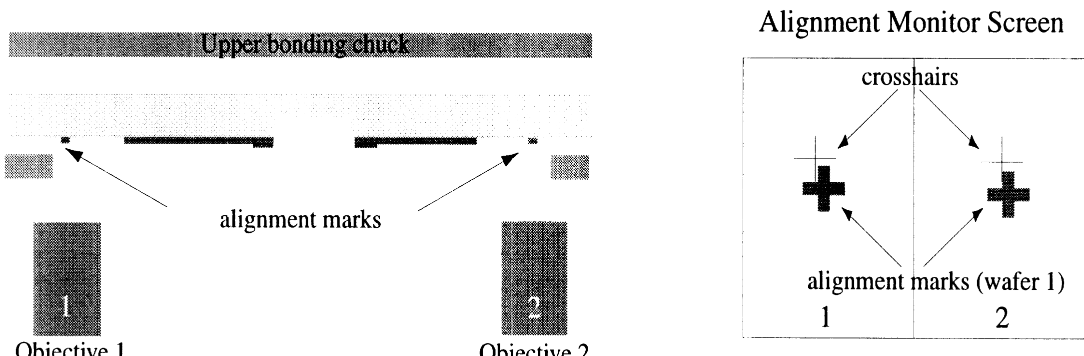
The method of alignment and bonding is similar to that explained in Chapter 4 for the RF wafer-to-wafer interconnect. Electronics Visions manual aligner and bonder are used (Figures 4.10)[116]. The experimental align and bond procedure begins as follows. To prevent surface contamination, the wafers are cleaned with organic solvents and then ultraviolet (UV) exposed for 30 minutes. First the wafers are aligned in the EV420 Manual Aligner (Figure 4.10(a)). With this equipment, aligning begins by loading the first sample and aligning it to cross-hairs on a monitor screen as shown in Figure 6.21. This sample is then vacuum held to an upper plate. The second wafer is then loaded and aligned to the same cross-hairs on the monitor screen. Once aligned the wafers are brought into close proximity and clamped together in the bond fixture. As shown in Figure 6.22, this bond fixture is then loaded into the vacuum bond chamber of the EV 501 Manual Wafer Bonder (Figure 4.10(b)).

However, as shown in Figure 6.23, no two layers can be bonded without crushing outer air bridges. For this reason, alignment of all four wafers is first achieved. Although this is done manually using IR alignment techniques for the power cube, custom tooling is available for this process in the Electronics Visions aligner. The four wafer alignment method is shown in Figure 6.24 in which the upper bonding chuck is lowered to form contact between upper and lower wafers. The lower wafer is held with a vacuum while the third wafer is aligned and flags are placed between the third wafer and the first two wafers. Finally, the fourth wafer is aligned and the bond chuck is raised to meet the other wafers. The entire bond jig is removed from the aligner and placed in the bonder.

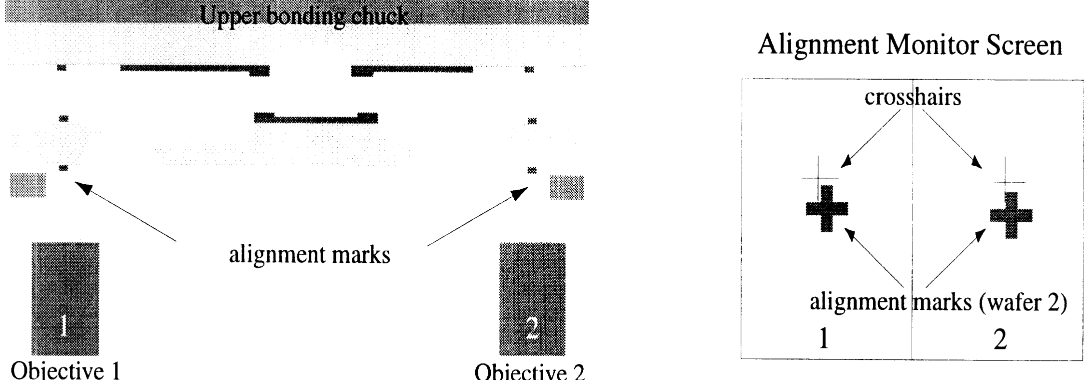
The bonding sequence for the aligned four wafer stack commences with a nitrogen ambient of $10^{-2}$ bar to maintain a low particulate environment and prevent oxidation. A small amount of pressure, 50 Newtons (N), is applied to the four samples while the top and bottom bond plates heat up to 350°C. Once temperature has stabilized, 200 N are applied for 30 minutes. Three power cubes were successfully bonded and sent to HRL Laboratories for MMIC bonding. Photos are shown in Figure 6.25.




(a) Alignment set-up for Electronics Visions bonding includes two alignment/bonding chucks, two microscope objectives, and a split view monitor screen allowing view of each objective. Lower chuck includes 10 mm diameter viewing hole.

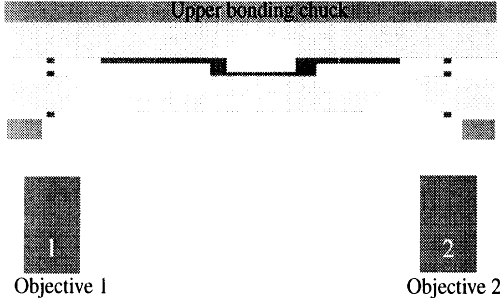



(b) First wafer is loaded onto lower chuck with alignment marks in view. Alignment marks are aligned to crosshairs on monitor screen.

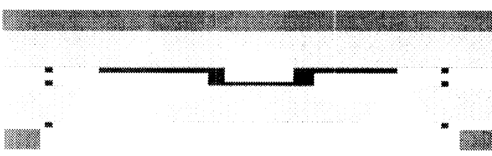



(c) First wafer is vacuum-held onto upper chuck and elevated while second wafer is loaded onto lower chuck and aligned to reference crosshairs.

Figure 6.21: Method of alignment for Electronics Visions equipment.




(d) Upper bonding chuck is lowered to form contact between upper and lower wafers. Alignment is complete.



(e) Entire alignment jig removed from aligner and placed in bonder for application of heat and pressure.

Figure 6.22: Method of alignment for Electronics Visions equipment continued.

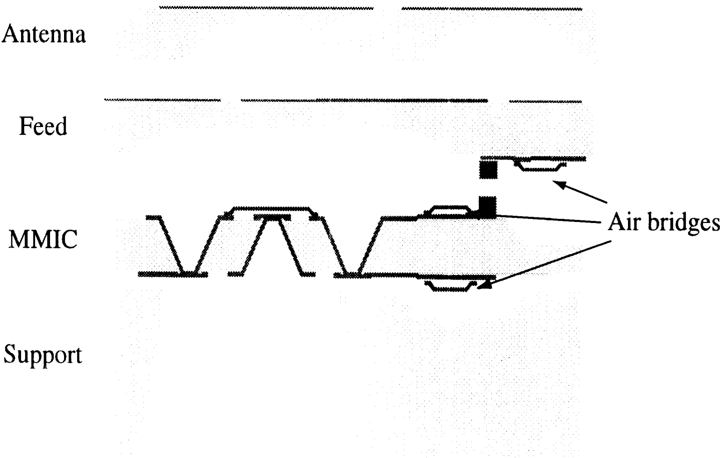
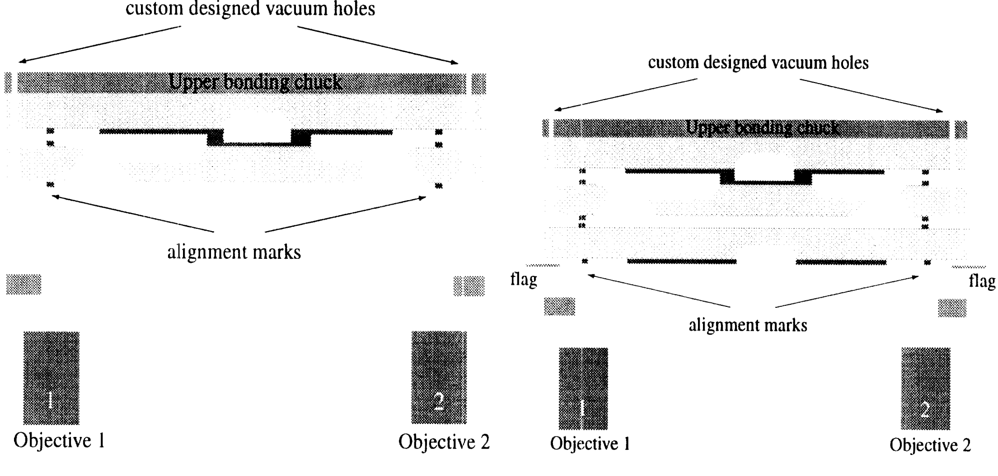
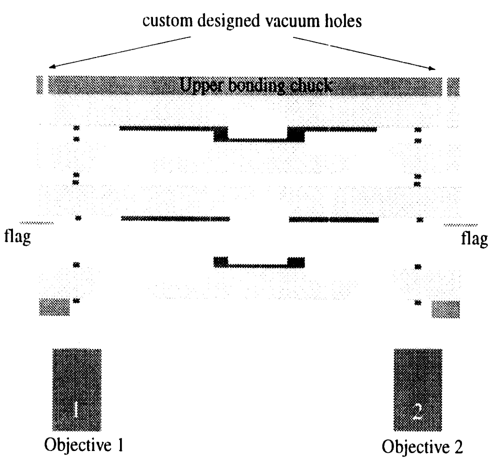



Figure 6.23: Illustration showing relative placement of air bridges on power cube layers.

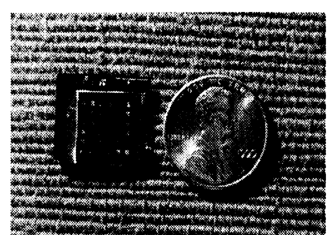



(a) Alignment of wafers 1 and 2. (b) Addition of wafer 3.

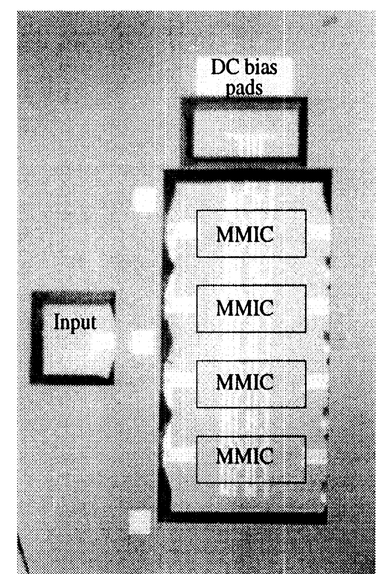



(c) Addition of wafer 4.

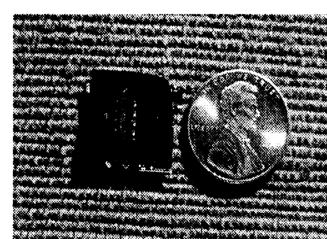
Figure 6.24: Custom four wafer stack alignment tooling available. Method illustrated: a) Upper bonding chuck is lowered to form contact between upper and lower wafers. Lower wafer is held with vacuum. b) Third wafer aligned and flags placed between third wafer and first two wafers. c) Fourth wafer aligned and bond chuck raised to meet other wafers. Entire bond jig removed from aligner and placed in bonder. Note conventional infrared (IR) alignment techniques used for power cube.



Bonded Power Cube
with Antenna Layer Face-up




Close-up of Bonded Power Cube
with Support Layer Face-up
(MMICs not yet flip-chip bonded)



Bonded Power Cube
with Support Layer Face-up

Figure 6.25: Photographs of bonded power cube layers.

## 6.5 Measurements

Although measurements of the active power cube are not available, individual passive component combination measurements prove the success of the fabrication integration and high-density passive component designs. Samples with individual components as well as component combinations were fabricated in parallel with the MMIC layer. Significant results from these samples are presented here.

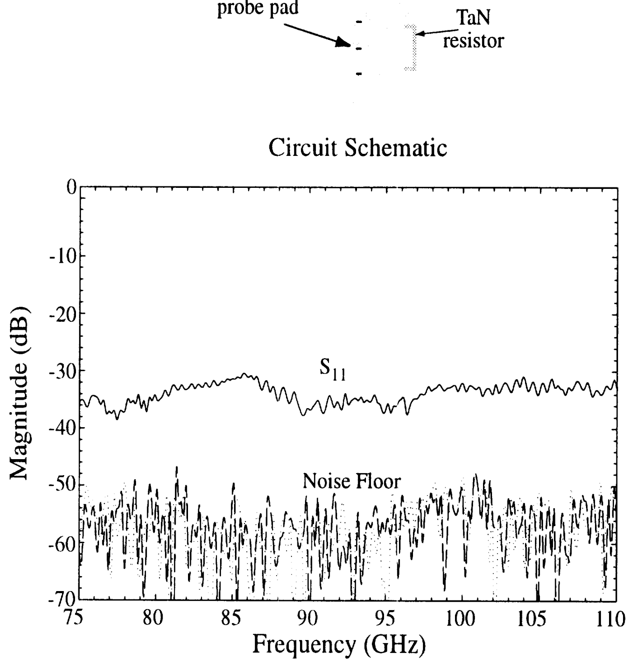



Figure 6.26: Measured 50 Ω resistor.

Figure 6.26 shows 37 dB measured return loss from a 50 Ω TaN resistor at 94 GHz. This result demonstrates the matched termination as 50 ±1 Ω using Equation 6.1, where $Z_o$ is 50 Ω and Γ is 0.014, proving the MMIC layer resistor fabrication successful.

$$Z_L = \frac{Z_o(1+\Gamma)}{1-\Gamma} \tag{6.1}$$

A right angle bend, reactive tee junction, and Wilkinson power divider are measured as shown in Figures 6.27, 6.28, and 6.29 with 50 ±1 Ω TaN resistive terminations. The right angle bend return loss is 26 dB at 94 GHz, and both the tee and Wilkinson return losses are below 15 dB at 94 GHz.

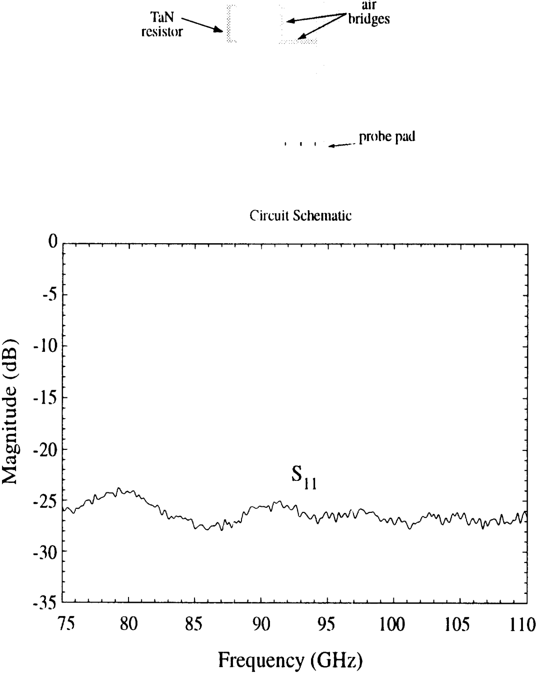



Figure 6.27: Measured right angle bend with 50 Ω termination.

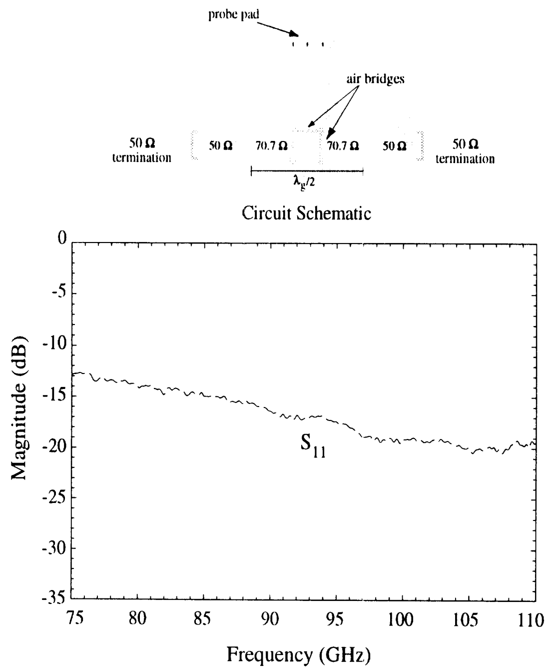



Figure 6.28: Measured tee with 50 Ω terminations.

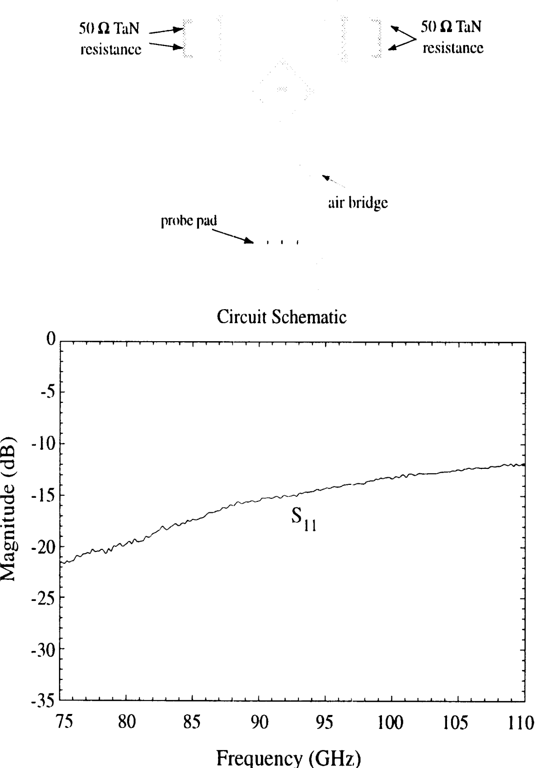



Figure 6.29: Measured input reflection coefficient of Wilkinson power divider with 50 Ω terminations.

Figure 6.30 displays the S-parameter measurements for the distribution network as designed for the power cube and after undergoing all fabrication processes for the MMIC layer. The superposition of measurements of three identical distribution networks indicates power balance in the network and consistent insertion loss. A damaged air bridge in the fourth network prevented balanced measurement, thus it is not shown here, but is discussed in the appendices.The expected loss of the network at 94 GHz is the sum of the 1 mm line loss (0.28 dB) and the component loss (0.84 dB), which is 1.12 dB above nominal, or 7.12 dB. The measured insertion loss from the three measurements at 85 GHz is 7.2 dB with a $\pm$ 0.1 dB deviation, matching closely to the expected value.

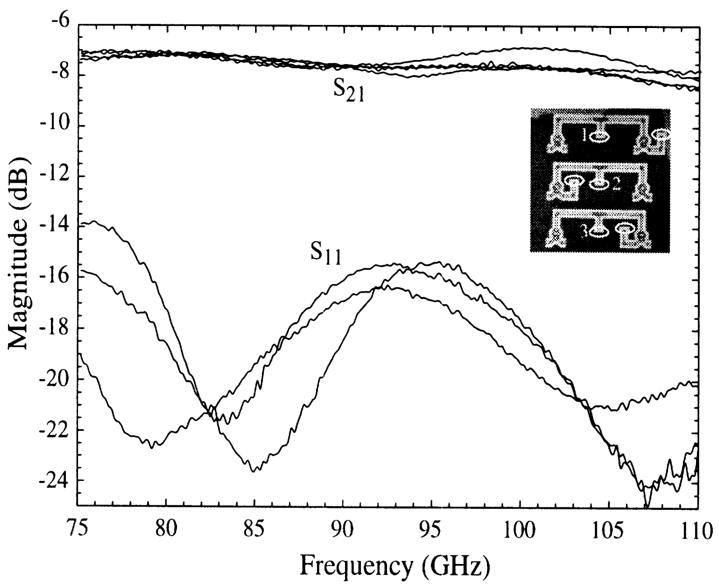
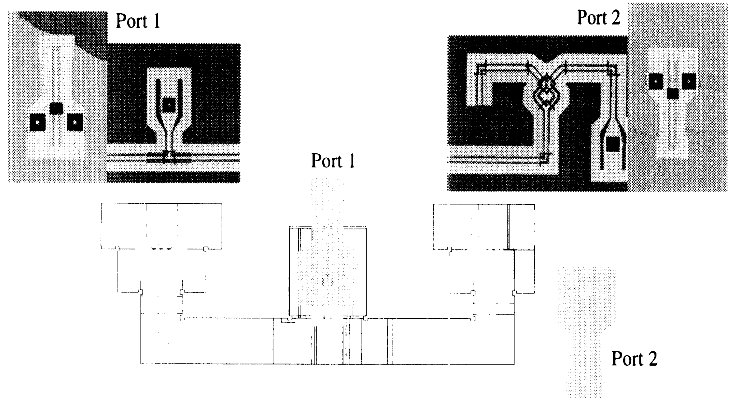


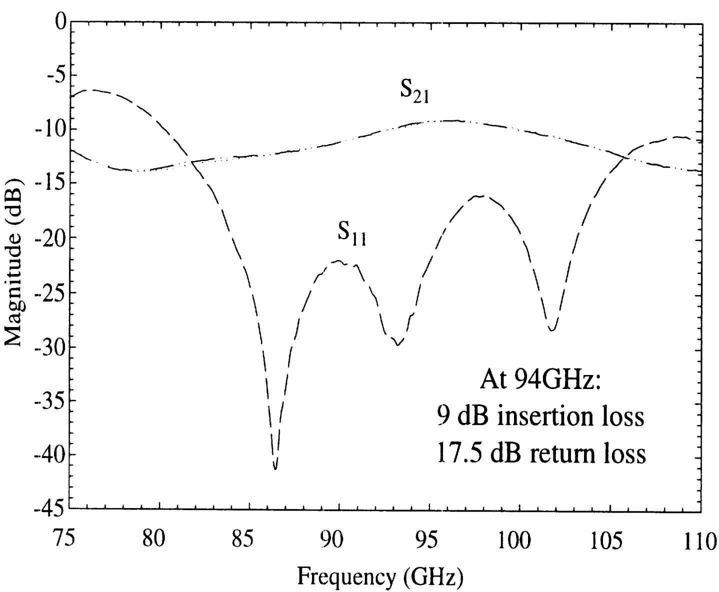

Figure 6.30: Measurements of distribution network.

As an example of component combination measurements, Figure 6.31(b) shows the measured S-parameters for the circuit illustrated in Figure 6.31(a). In this circuit, the RF signal propagates through a three-via interconnect to the other side of the 100 $\mu$m silicon wafer, a distribution network, and a second three-via interconnect to the original side of the 100 $\mu$m silicon wafer. At 94 GHz, the return and insertion losses are 17.5 dB and 9 dB, respectively. Nominal to the 9 dB insertion loss is the 6 dB from the Wilkinson and the reactive tee junction. The 3 dB of excess loss is due to the two vertical interconnects, feed line, and distribution network loss. Recall the insertion loss of a single vertical interconnect

is 0.5-0.6 dB and that of the entire back-to-back measurement including the feed lines is approximately 1.8 dB. The remaining 1.2 dB is attributed to the distribution network. Thus the measured insertion loss of this complex circuit is well-matched to the sum of the individual circuit component performances.




(a) Photo and schematic of passive component combination measurement of Figure 6.31(b).




(b) Measured passive component combination: via-distribution network-via.

Figure 6.31: Passive component combination of via-distribution network-via. a) Photo with illustration b) Measured S-parameters.

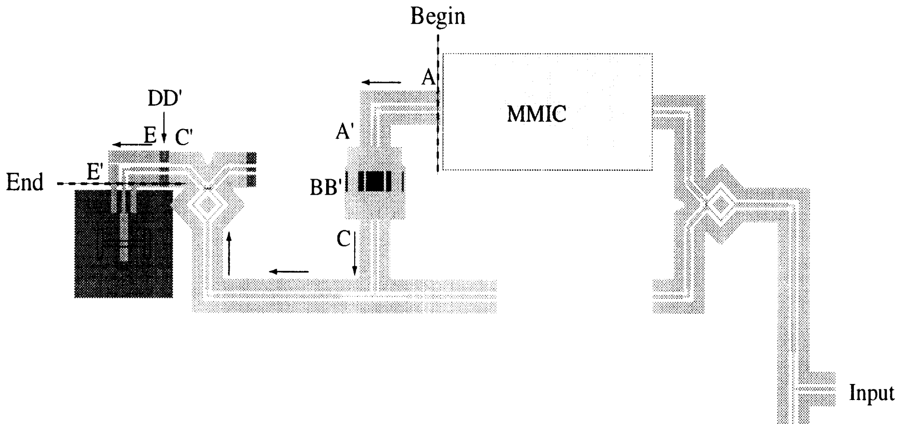
## 6.6 Conclusions

A W-Band multi-layer power cube has been designed, fabricated, bonded, and partially-tested at 94 GHz. This project was the impetus behind development of key FGC circuit components, such as vertical interconnects, wafer-to-wafer interconnects, and low loss distribution networks. In addition to these individual components, design and fabrication integration makes the power cube not only a densely integrated multilayer circuit, but an integrated conformal package utilizing thermocompression bonding. Although active power cube measurements are unavailable, the estimated loss from MMIC amplifier to the microstrip array excitation is 1.8-2.4 dB as shown in Table 6.6. The signal flow follows the illustrations in Figure 6.32 from point A to E' as well as the order presented in the table.

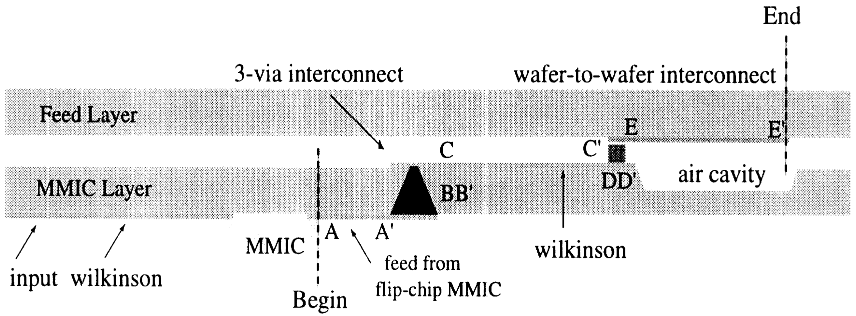
Table 6.2: Amplifier-to-Array loss at 94 GHz

| Element | Designation (Figure 6.32) | Loss (dB) |
|---|---|---|
| 1 mm FGC line | AA' | 0.24-0.29 |
| 1 vertical interconnect | BB' | 0.5-0.6 |
| Distribution network | CC' | 0.9-1.3 |
| Wafer-to-wafer transition | DD' | 0.1 |
| 0.5 mm FGC line | EE' | 0.12-0.15 |
| Total | AA'-EE' | 1.8-2.44 dB |

This is the only known W-band micromachined power cube at this time. The strong technology base established through this project forms a legacy for future technology maturation. The size of the transmit module is dictated by the $\lambda_g/2$ patch antennas. As the design frequency decreases, the array size will increase accordingly. Although the limitation of any technology is application specific, the power cube can be applied to frequencies as low as K-band, offering novel three-dimensional integration techniques.




Signal Path from MMIC Amplifier to Array (A-E')




Feed and MMIC Layer Cross-section

Figure 6.32: Illustrations of signal flow from output of MMIC amplifier (A) to antenna feed (E'). Component losses from AA'-EE' are given in Table 6.6.

# CHAPTER 7

# CONCLUSIONS AND FUTURE WORK

## 7.1 Summary

This thesis presents several novel low-loss W-band components utilizing silicon micromachining. It has been shown that a micromachined finite ground coplanar (MFGC) waveguide can reduce loss by 1.4 dB/cm resulting in 0.8 dB/cm attenuation at 94 GHz. This attenuation compares favorably with that of microshield lines. A compact 520 $\mu$m by 520 $\mu$m vertical interconnect for finite ground coplanar waveguide has demonstrated 0.55 dB loss per transition at 94 GHz. This micromachined three-via interconnect allows signal transfer from one side of a silicon wafer to the other. A wafer-to-wafer interconnect has also been demonstrated using thermocompression bonding. This compact 100 $\mu$m by 300 $\mu$m transition allows signal transfer of an FGC line from one silicon wafer to another with loss of only 0.1 dB. Additionally, micromachined FGC lines have been applied to lateral circuit combining networks in which electrical signals are divided into two, four, and eight signal paths resulting in 0.2-1.6 dB loss reduction as compared to conventional networks at W-band. Lastly, 50 and 70 $\Omega$ MFGC lines reduce the line attenuation by approximately 1 dB/cm while maintaining the same impedance as a conventional line.

These components have been integrated into a multilayer silicon micromachining W-band power cube demonstrating the synergy of micromachined RF component, flip-chip, and thermocompression wafer bonding technologies. This transmit module is not only a high-density multi-layer circuit, but an integrated conformal package utilizing thermocompression

bonding, and it the only known W-band multi-layer module at this time. The multi-layer silicon environment, with appropriate design and packaging, can provide a solution to the low power problems of conventional monolithic microwave integrated circuits (MMICs) by providing more power per unit area. Fabrication and packaging integration has been demonstrated and passive component measurements prove their success. The technology base established through this project forms a legacy for future technology maturation.

## 7.2 Future Work

Although ten years ago frequencies above 2 GHz were reserved for special communications, today, as we start the new millenium, hundreds of consumer products exist in the microwave and millimeter range. Two examples are PCS phones operating just below 2 GHz to consumer wireless devices at 2.4 GHz. Massive communication infrastrutures called Local Multipoint Distribution Service (LMDS) at 28-32 GHz are currently under consideration as well [126].This change has occurred because of the drive to decrease size and cost, and integrate functions using different substrate materials and design innovations.

The developmental research effort presented in this dissertation applies leading and novel technologies to W-band, or 75-110 GHz, with the overall goal of a low-loss, higher powered transmit module. Currently, several military and commercial applications will be greatly enhanced if several to tens of watts of radiated power can be produced economically at W-band. Some of these applications are moderate range adverse weather radars, weapon seekers, and line-of-sight covert communications.

### 7.2.1 Transmit and Receive Module with Focused, Steerable Array

The power cube presented in this dissertation is a transmit module. It does not have a phased array or array steering capabilities. MEMS technology, integrated sources, and mixers may be added to design a transmit and receive module. The stacked approach for the power cube can allow for integrated LO sources, mixers, and baseband circuitry. MEMS switches and phase shifters may be added to allow for transmit and receive using the same radiating elements and to allow for beam steering of a phased array.

### 7.2.2 Fabrication Enhancements

The fabrication of structures such as the Power Cube could be greatly eased with the development of effective lithography and planarization technologies for micromachined structures. Planarization technologies could assist in the integration of MEMS switches and phase shifters with the Power Cube. The development of custom bonding jigs for small thinned wafer pieces would greatly benefit the development of future multilayer wafer projects.

### 7.2.3 Adverse Weather UAV 35 GHz SAR Imaging System

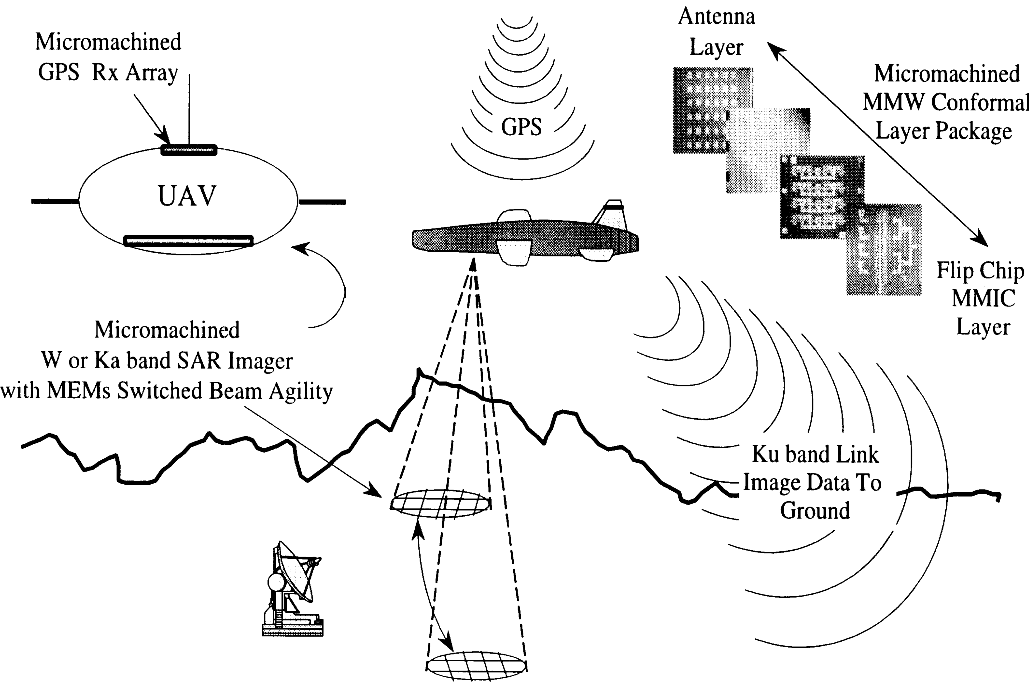



Figure 7.1: Power cube application: Adverse weather UAV 35 GHz Synthetic Aperture Radar (SAR) Imaging System. Courtesy Dr. Robert T. Kihm

Although originally designed at 94 GHz, the power cube technology may be used as low as Ka-band. The size of the cube is dictated by the size of the $\lambda_g/2$ patch antennas. One 35 GHz application is shown in Figure 7.1, in which a micromachined Ka-band SAR imager with MEMs switching beam agility is used.

# APPENDICES

# APPENDIX A

# AIR BRIDGE COMPENSATION

## A.1 Introduction

Air bridges are traditionally used to equalize ground planes on transmission lines such as finite ground coplanar waveguide (FGC). Often, these bridges can be implemented in physical circuits without accounting for them in the circuit design. However, at frequencies such as W-band, the capacitive loading of the air bridge can effect the current distribution and decrease the characteristic impedance of the line. One method of compensation is to place high impedance sections of line on either side of the bridge [118]. This appendix presents a method of modeling the appropriate high impedance lengths and discusses the benefits of air bridge compensation.

## A.2 Circuit Model

A photo of a fabricated air bridge is shown in Figure A.1. This bridge can be modeled as a shunt capacitance and its' equivalent low impedance can be compensated with high impedance sections. The equivalent circuit model is shown in Figure A.2 and the equivalent impedance of the high-low-high impedance section is shown from right to left in equations A.1-A.5.

$$Z_t = Z_2 \frac{Z_o + jZ_2 tan\beta l}{Z_2 + jZ_o tan\beta l} \tag{A.1}$$

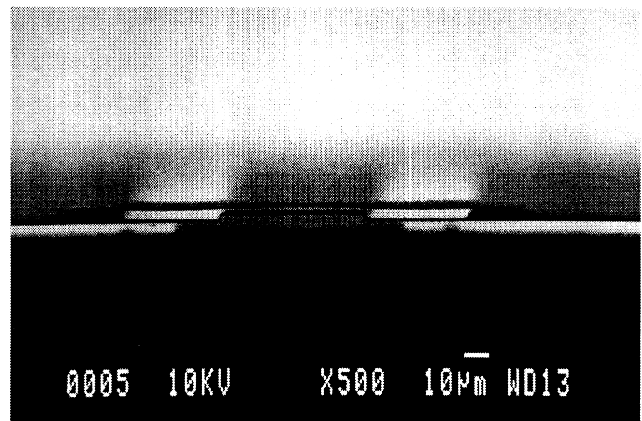



Figure A.1: SEM photo of air bridge of FGC line.

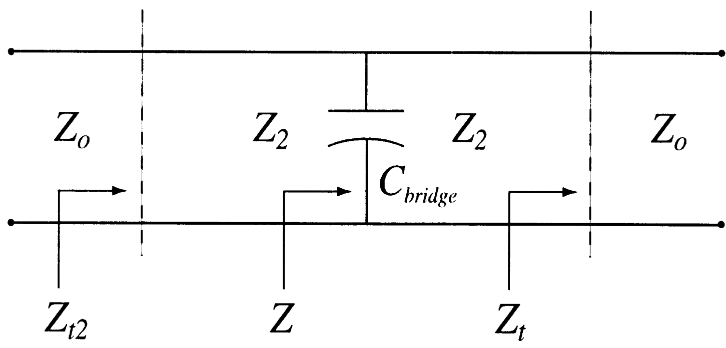



Figure A.2: Equivalent circuit model for air bridge with high impedance compensation.

$$t = tan(\beta l) \tag{A.2}$$

$$Z_t = Z_2 \frac{Z_o + jZ_2 t}{Z_2 + jZ_o t} \tag{A.3}$$

$$Z = (\frac{1}{Z_t} + j\omega C)^{-1} \tag{A.4}$$

$$Z_{t2} = Z_2 \frac{Z + jZ_2 t}{Z_2 + jZt} \tag{A.5}$$

Setting $Z_{t2}$ equal to the impedance of the line, $Z_o$, such that $\Gamma = 0$ and solving for $l$ yields two solutions for the high impedance section lengths. Thus for a given $Z_o$, $C$, $w$, and $Z_2$, solving $Z_{t2} = Z_o$ for $t$ yields two solutions, $t_1$ and $t_2$.

$$t_1(Z_o, C, w, Z_2) = -\frac{-Z_2^2 + Z_o^2 + \sqrt{Z_2^4 - Z_2^2(2 + C^2w^2Z_2^2)Z_o^2 + Z_o^4}}{CwZ_2^3} \tag{A.6}$$

$$t_2(Z_o, C, w, Z_2) = \frac{-Z_2^2 - Z_o^2 + \sqrt{Z_2^4 - Z_2^2(2 + C^2w^2Z_2^2)Z_o^2 + Z_o^4}}{CwZ_2^3} \tag{A.7}$$

Solving $t = tan(\beta l)$ where

$$\beta = \frac{2\pi}{\lambda} = \frac{2f\pi\sqrt{\epsilon_{eff}}}{c} \tag{A.8}$$

yields two $l$ values:

$$l_1 = \tan^{-1}(t_1)\frac{c}{2f\pi\sqrt{\epsilon_{eff}}} \tag{A.9}$$

$$l_2 = \tan^{-1}(t_2)\frac{c}{2f\pi\sqrt{\epsilon_{eff}}} \tag{A.10}$$

## A.3 Capacitance Calculation

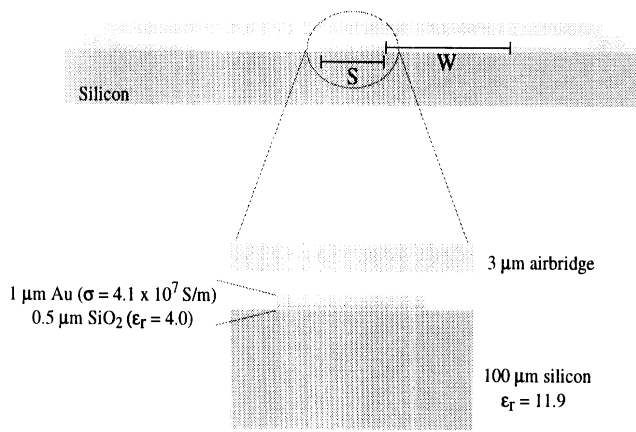



Figure A.3: Cross-section of FGC line with air bridge.

The shunt capacitance due to the air bridge over the FGC line can be determined my examining the 2-D cross-section [5]. As shown in Figure A.3, the 3 $\mu$m thick air bridge is 3 $\mu$m above the 1 $\mu$m FGC line, which sits on a 0.5 $\mu$m layer of $SiO_2$. The capacitance is solved numerically with and without substrates present producing $C_{sub}$ and $C_{air}$. The

potential on the line is such that 1 volt is applied to the center conductor and 0 volts are applied to the ground planes. From the capacitance values, the effective dielectric constant and characteristic impedance are calculated from Equations A.11 and A.12.

$$\epsilon_{eff} = \frac{C_{sub}}{C_{air}} \tag{A.11}$$

$$Z_o = \frac{1}{v_o \sqrt{\epsilon_{eff}} C_{air}} \tag{A.12}$$

Table A.1 shows the capacitance per unit length, $\epsilon_{eff}$, and $Z_o$ for three different FGC geometries with and without air bridges. For example, the per-unit-length capacitance of the 40-24-106 line doubles with the addition of an air bridge. In addition, the effective dielectric constant decreases from 6.2 to 1.89, as the field distribution becomes more concentrated in the air region, and the characteristic impedance decreases from approximately 57 Ω to 14 Ω.

| FGC Dimensions (μm) | $C_{sub}$ (F/m) | $C_{air}$ (F/m) | $\varepsilon_{eff}$ | $Z_o$ (Ω) |
|---|---|---|---|---|
| 18-35-100 | $1.08 \times 10^{-10}$ | $1.94 \times 10^{-11}$ | 5.56 | 72.76 |
| 18-35-100 w/ bridge | $1.77 \times 10^{-10}$ | $8.05 \times 10^{-11}$ | 2.20 | 27.92 |
| 26-52-100 | $1.07 \times 10^{-10}$ | $1.87 \times 10^{-11}$ | 5.70 | 74.45 |
| 26-52-100 w/ bridge | $2.09 \times 10^{-10}$ | $1.06 \times 10^{-10}$ | 1.97 | 22.45 |
| 40-24-106 | $1.47 \times 10^{-10}$ | $2.37 \times 10^{-11}$ | 6.2 | 56.61 |
| 40-24-106 w/ bridge | $3.30 \times 10^{-10}$ | $1.75 \times 10^{-10}$ | 1.89 | 13.89 |

Table A.1: Capacitance per unit length, $\epsilon_{eff}$, and $Z_o$ (Ω) for 3 FGC geometries with and without air bridges.

The capacitance of a particular air bridge width is equal to the capacitance per unit length multiplied by the physical width of the bridge. This is shown in Table A.2 for three different FGC geometries and air bridge widths varying 10-40 $\mu$m. For example, a 10 $\mu$m air bridge loads a 40-24-106 $\mu$m line by 2.77 fF, while a 40 $\mu$m air bridge loads a 40-24-106 $\mu$m line by 11.08 fF according to the capacitance model.

| Geometry under bridge (μm) | Capacitance 10 μm bridge | Capacitance 20 μm bridge | Capacitance 30 μm bridge | Capacitance 40 μm bridge |
|---|---|---|---|---|
| | | | | |
| 18-35-100 | 1.77 x$10^{-15}$ F | 3.54 x$10^{-15}$ F | 5.31 x$10^{-15}$ F | 7.08 x$10^{-15}$ F |
| | | | | |
| 26-52-100 | 2.09 x$10^{-15}$ F | 4.17 x$10^{-15}$ F | 6.26 x$10^{-15}$ F | 8.34 x$10^{-15}$ F |
| | | | | |
| 40-24-106 | 2.77 x$10^{-15}$ F | 5.5 x$10^{-15}$ F | 8.31 x$10^{-15}$ F | 11.08 x$10^{-15}$ F |

Table A.2: Capacitance per unit length multiplied by physical width determines capacitance of air bridges for 3 FGC geometries.

## A.4 Libra Model

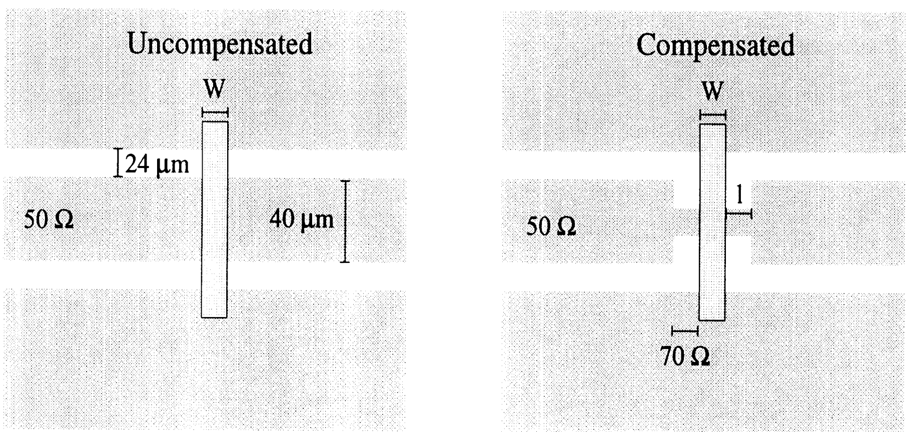



Figure A.4: Schematic of air bridge with and without compensation.

If, for example, an air bridge on a 50 $\mu$m line is compensated with 70 $\mu$m high impedance sections, the length of the sections can be determined given the width of the air bridge, the desired frequency, and its equivalent capacitance. Figure A.4 shows the schematics for the compensated and uncompensated versions of an air bridge on a 50 Ω line designed for 94 GHz. The high impedance sections will be 70 Ω with the air bridge width denoted by $w$ and the length of the high impedance section by $l$. Two 70 Ω geometries are possible: 18-35-100 and 26-52-100 $\mu$m. The geometry under the bridge is that of the 70 Ω line for simplicity.

Table A.3 shows capacitance and high impedance length values for various bridge widths for each of the 70 Ω lines. For example, a 20 $\mu$m bridge over a 18-35-100 $\mu$m line represents a capacitance of 3.54 fF. To compensate for this the high impedance lengths can be either 16 $\mu$m or 288 $\mu$m.

| High $Z_2$ FGC Dimensions (μm) | 20 μm bridge (W=20) | | | 30 μm bridge (W=30) | | | 40 μm bridge(W=40) | | |
|---|---|---|---|---|---|---|---|---|---|
| | C(fF) | $l_1$(μm) | $l_2$(μm) | C(fF) | $l_1$(μm) | $l_2$(μm) | C(fF) | $l_1$(μm) | $l_2$(μm) |
| | | | | | | | | | |
| 18-35-100 | **3.54** | **16** | **288** | 5.31 | 24 | 271 | 7.08 | 32 | 256 |
| | | | | | | | | | |
| 26-52-100 | 4.17 | 18 | 281 | 6.26 | 28 | 264 | 8.34 | 39 | 245 |

Table A.3: $C$, $l_1$, and $l_2$ for different air bridge widths and aspect ratios.

Figure A.5 shows the simulated results for this example as a function of frequency from 75-110 GHz. The uncompensated line yields return loss of 22 dB at 96 GHz, while both compensated lines show improved performance. The longer 288 $\mu$m compensation resonates with -38 dB return loss at 96 GHz, while the compensation with 16 $\mu$m high impedance sections yields a flat response with -44 dB return loss at 96 GHz. Thus modeled results show a significant improvement in return loss due to air bridge compensation.

## A.5 Measured and Modeled Circuits

Measured results for air bridges with and without compensation as compared to model results are shown here for air bridges 20, 30 and 40 $\mu$m wide over two different 70 Ω lines. These compensations are modeled for 94 GHz, and measurements match modeled data closely. Data is averaged from 90-100 GHz and tabulated for each measurement. The overall trend is 15-25 dB improvement in return loss with insertion loss increases of 0-0.1 dB for the short compensation. The longer compensation reduces return loss by 15 dB or more, but increases insertion losses by as much as 0.4 dB, and requires more space. Thus the short compensation is preferable when insertion losses are to be minimized.

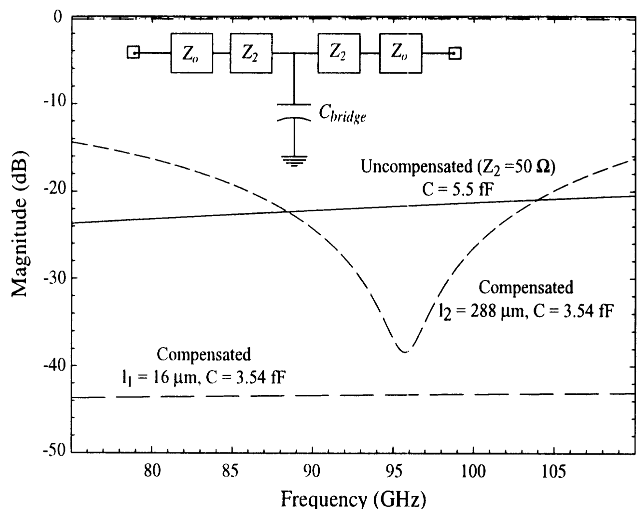



Figure A.5: Libra simulation of uncompensated air bridge and compensated air bridge with two different high impedance section lengths.

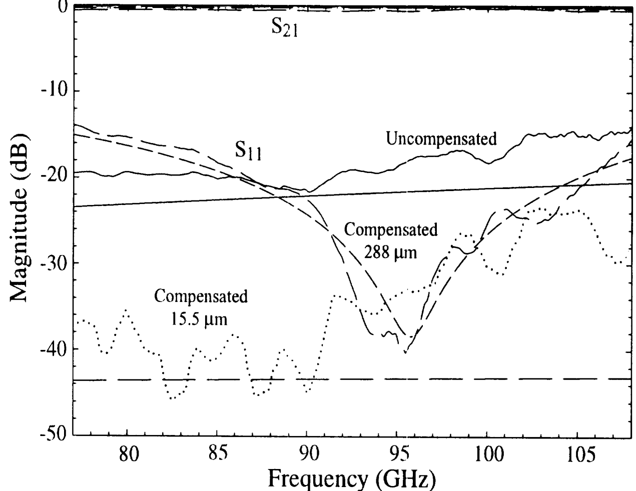



Figure A.6: Measured and modeled results for 20 $\mu$m air bridges with L1 =15.5 $\mu$m and L2 = 288 $\mu$m high impedance sections as compared to uncompensated. 50 Ω line dimensions 40-24-106 $\mu$m. 70 Ω line dimensions 18-35-100 $\mu$m.

| S-parameters | $S_{11}$ (dB) modeled | $S_{11}$ (dB) measured | $S_{21}$ (dB) modeled | $S_{21}$ (dB) measured |
|---|---|---|---|---|
| Uncompensated<br>C = 5.5 fF<br>Ave | -21.61 | -18.53 | -0.07 | -0.10 |
| Max | -21.14 | -15.42 | -0.06 | -0.00 |
| Min | -22.09 | -21.98 | -0.07 | -0.19 |
| Compensated<br>$C_{mod}$ = 3.54fF<br>70 Ω length = 288 μm<br>Ave | -31.16 | -31.85 | -0.25 | -0.55 |
| Max | -24.27 | -22.43 | -0.25 | -0.34 |
| Min | -38.39 | -46.65 | -0.27 | -0.68 |
| Compensated<br>$C_{mod}$ = 3.54 fF<br>70 Ω length = 15.5 μm<br>Ave | -43.29 | -33.12 | -0.07 | -0.17 |
| Max | -43.21 | -23.67 | -0.07 | -0.07 |
| Min | -43.37 | -47.60 | -0.08 | -0.27 |

Table A.4: Tabulated results of Figure A.6 averaged from 90-100 GHz.

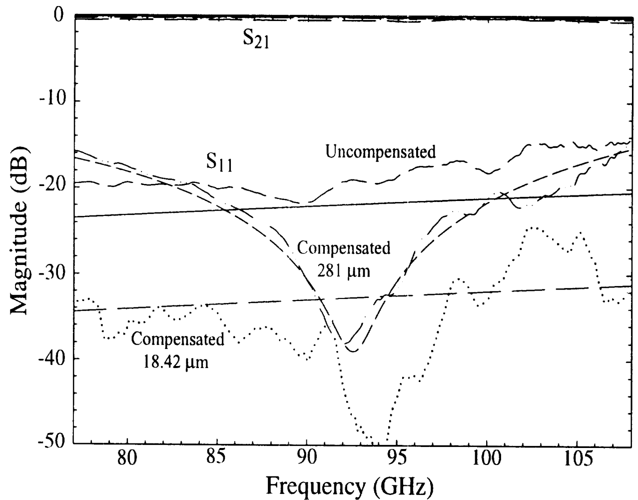



Figure A.7: Measured and modeled results for 20 $\mu$m air bridges with L1 =18.42 $\mu$m and L2 = 281 $\mu$m high impedance sections as compared to uncompensated. 50 Ω line dimensions 40-24-106 $\mu$m. 70 Ω line dimensions 26-52-100 $\mu$m.

| S-parameters | $S_{11}$ (dB) modeled | $S_{11}$ (dB) measured | $S_{21}$ (dB) modeled | $S_{21}$ (dB) measured |
|---|---|---|---|---|
| Uncompensated<br>C = 5.5 fF<br>Ave | -21.61 | -18.53 | -0.07 | -0.10 |
| Max | -21.14 | -15.42 | -0.06 | -0.00 |
| Min | -22.09 | -21.98 | -0.07 | -0.19 |
| Compensated<br>$C_{mod}$ = 4.17 fF, $C_{fit}$ = 5 fF<br>70 Ω length = 281 μm<br>Ave | -30.26 | -29.66 | -0.26 | -0.53 |
| Max | -21.62 | -20.05 | -0.24 | -0.31 |
| Min | -39.00 | -39.56 | -0.29 | -0.72 |
| Compensated<br>$C_{mod}$ = 4.17 fF, $C_{fit}$ = 5 fF<br>70 Ω length = 18.42 μm<br>Ave | -32.49 | -40.08 | -0.08 | -0.20 |
| Max | -31.98 | -28.00 | -0.08 | -0.02 |
| Min | -33.01 | -58.94 | -0.08 | -0.38 |

Table A.5: Tabulated results of Figure A.7 averaged from 90-100 GHz.

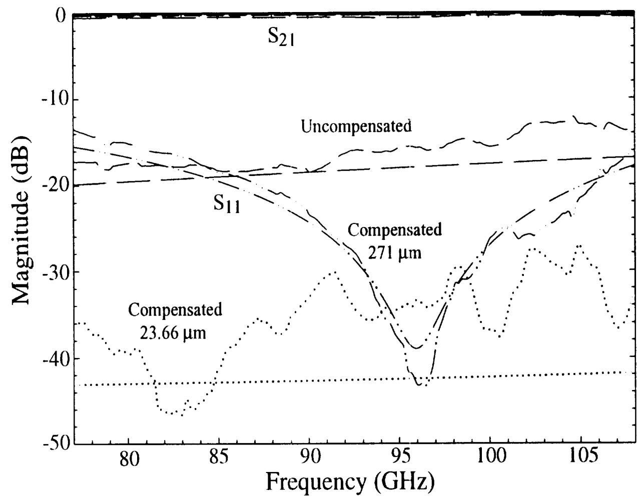



Figure A.8: Measured and modeled results for 30 $\mu$m air bridges with L1 =23.66 $\mu$m and L2 = 271 $\mu$m high impedance sections as compared to uncompensated. 50 $\Omega$ line dimensions 40-24-106 $\mu$m. 70 $\Omega$ line dimensions 18-35-100 $\mu$m.

| S-parameters | $S_{11}$ (dB) modeled | $S_{11}$ (dB) measured | $S_{21}$ (dB) modeled | $S_{21}$ (dB) measured |
|---|---|---|---|---|
| Uncompensated<br>C = 8.31 fF<br>Ave | -17.98 | -16.03 | -0.11 | -0.22 |
| Max | -17.51 | -13.61 | -0.10 | -0.06 |
| Min | -18.46 | -18.72 | -0.12 | -0.35 |
| Compensated<br>$C_{mod}$ = 5.31 fF<br>70 Ω length = 271 μm<br>Ave | -31.48 | -32.49 | -0.25 | -0.54 |
| Max | -24.34 | -23.40 | -0.24 | -0.34 |
| Min | -39.00 | -54.70 | -0.26 | -0.67 |
| Compensated<br>$C_{mod}$ = 5.31 fF<br>70 Ω length = 23.66 μm<br>Ave | -42.50 | -33.33 | -0.08 | -0.24 |
| Max | -42.29 | -25.54 | -0.08 | -0.09 |
| Min | -42.69 | -40.30 | -0.08 | -0.33 |

Table A.6: Tabulated results of Figure A.8 averaged from 90-100 GHz.

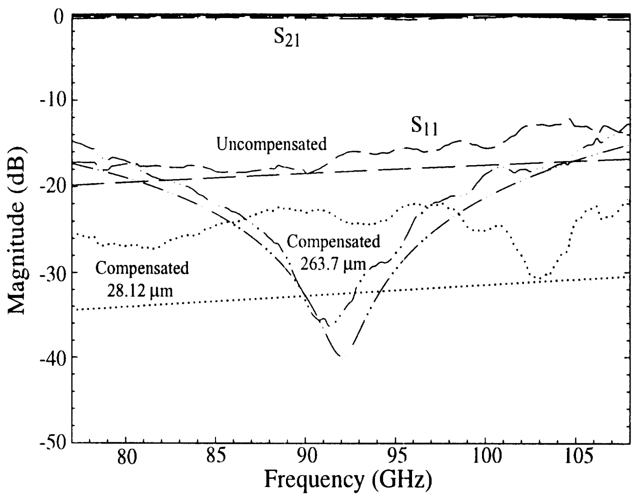



Figure A.9: Measured and modeled results for 30 $\mu$m air bridges with L1 =28.12 $\mu$m and L2 = 263.7 $\mu$m high impedance sections as compared to uncompensated. 50 $\Omega$ line dimensions 40-24-106 $\mu$m. 70 $\Omega$ line dimensions 26-52-100 $\mu$m.

| S-parameters | $S_{11}$ (dB) modeled | $S_{11}$ (dB) measured | $S_{21}$ (dB) modeled | $S_{21}$ (dB) measured |
|---|---|---|---|---|
| Uncompensated<br>C = 8.31 fF<br>Ave | -17.98 | -16.03 | -0.11 | -0.22 |
| Max | -17.51 | -13.61 | -0.10 | -0.06 |
| Min | -18.46 | -18.72 | -0.12 | -0.35 |
| Compensated<br>$C_{mod}$ = 6.26 fF, $C_{fit}$ = 7.5 fF<br>70 Ω length = 263.7 μm<br>Ave | -30.20 | -27.41 | -0.25 | -0.52 |
| Max | -21.28 | -17.69 | -0.24 | -0.39 |
| Min | -39.89 | -40.84 | -0.29 | -0.69 |
| Compensated<br>$C_{mod}$ = 6.26 fF, $C_{fit}$ = 7.5 fF<br>70 Ω length = 28.12 μm<br>Ave | -32.11 | -23.37 | -0.09 | -0.21 |
| Max | -31.47 | -20.63 | -0.09 | -0.04 |
| Min | -32.75 | -27.16 | -0.09 | -0.41 |

Table A.7: Tabulated results of Figure A.9 averaged from 90-100 GHz.

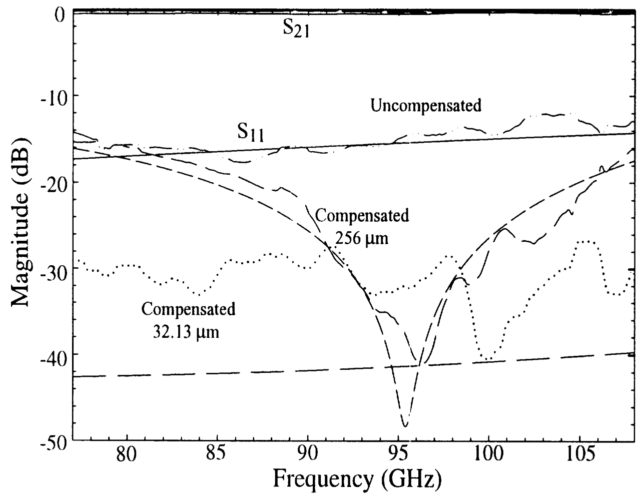



Figure A.10: Measured and modeled results for 40 $\mu$m air bridges with L1 =32.13 $\mu$m and L2 = 256 $\mu$m high impedance sections as compared to uncompensated. 50 $\Omega$ line dimensions 40-24-106 $\mu$m. 70 $\Omega$ line dimensions 18-35-100 $\mu$m.

| S-parameters | $S_{11}$ (dB) modeled | $S_{11}$ (dB) measured | $S_{21}$ (dB) modeled | $S_{21}$ (dB) measured |
|---|---|---|---|---|
| Uncompensated<br>C = 5.5 fF<br>Ave | -21.61 | -18.53 | -0.07 | -0.10 |
| Max | -21.14 | -15.42 | -0.06 | -0.00 |
| Min | -22.09 | -21.98 | -0.07 | -0.19 |
| Compensated<br>$C_{mod}$ = 3.54fF<br>70 Ω length = 288 μm<br>Ave | -31.16 | -31.85 | -0.25 | -0.55 |
| Max | -24.27 | -22.43 | -0.25 | -0.34 |
| Min | -38.39 | -46.65 | -0.27 | -0.68 |
| Compensated<br>$C_{mod}$ = 3.54 fF<br>70 Ω length = 15.5 μm<br>Ave | -43.29 | -33.12 | -0.07 | -0.17 |
| Max | -43.21 | -23.67 | -0.07 | -0.07 |
| Min | -43.37 | -47.60 | -0.08 | -0.27 |

Table A.8: Tabulated results of Figure A.10 averaged from 90-100 GHz.

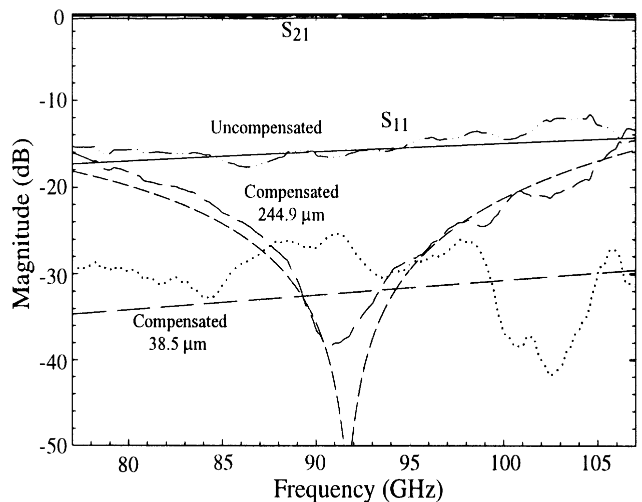



Figure A.11: Measured and modeled results for 40 $\mu$m air bridges with L1 =38.5 $\mu$m and L2 = 244.9 $\mu$m high impedance sections as compared to uncompensated. 50 Ω line dimensions 40-24-106 $\mu$m. 70 Ω line dimensions 26-52-100 $\mu$m.

| S-parameters | $S_{11}$ (dB) modeled | $S_{11}$ (dB) measured | $S_{21}$ (dB) modeled | $S_{21}$ (dB) measured |
|---|---|---|---|---|
| Uncompensated<br>C = 11.08 fF<br>Ave | -15.45 | -15.10 | -0.17 | -0.22 |
| Max | -14.98 | -12.64 | -0.15 | -0.11 |
| Min | -15.94 | -16.87 | -0.18 | -0.35 |
| Compensated<br>$C_{mod}$=8.34 fF, $C_{fit}$=9.5fF<br>70 Ω length = 244.9μm<br>Ave | -33.53 | -32.94 | -0.18 | -0.53 |
| Max | -25.58 | -23.23 | -0.18 | -0.37 |
| Min | -48.33 | -43.34 | -0.20 | -0.64 |
| Compensated<br>$C_{mod}$=8.34 fF, $C_{fit}$=9.5fF<br>70 Ω length = 38.5 μm<br>Ave | -41.36 | -31.69 | -0.09 | -0.27 |
| Max | -40.81 | -25.23 | -0.09 | -0.11 |
| Min | -41.84 | -48.83 | -0.09 | -0.46 |

Table A.9: Tabulated results of Figure A.11 averaged from 90-100 GHz.

## A.6 Conclusion

A method of modeling air bridge compensations is shown using an equivalent circuit model. Two lengths of high impedance compensation may be used. The longer section provides a resonance response and significantly reduced return loss, but insertion loss is increased by up to 0.4 dB. The shorter compensation section provides a flat response and maintains low insertion loss while reducing the return loss by as much as 25 dB. Modeled data is well-matched to measured, thus the modeling presented is an effective tool for design of air bridge compensations

# APPENDIX B

# POWER BALANCE OF CIRCUIT COMBINING NETWORKS

In circuit combining networks, in which a signal is divided into two or more paths, it is important to identify appropriate signal and power balance. It is also equally important to understand the cause of any power imbalance so as to prevent it from repeating. In this appendix, reasons for mismatch are proposed, simulated, and identified in a 1:4 circuit combining network measurement.

## B.1 Simulation

Figure B.2 shows the simulated effect when one of the three remaining output ports is mismatched on the 1:4 network presented in Chapters 5 and 6. As shown in the schematic of Figure B.1, one output port is terminated with a variable resistor and simulations are run with resistor values of 10, 50, 70, and 110 Ω. With a matched 50 Ω termination the insertion loss is quite flat. However, when mismatch exists ripple becomes apparent in insertion loss which varies ± 1.5 dB when a 10 Ω termination is applied, with a maximum value of 7 dB.

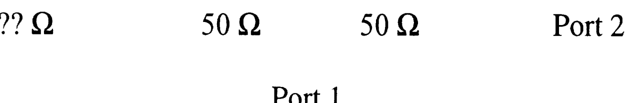



Figure B.1: Schematic of simulated network with one of three output port terminations varied from 50 Ω.

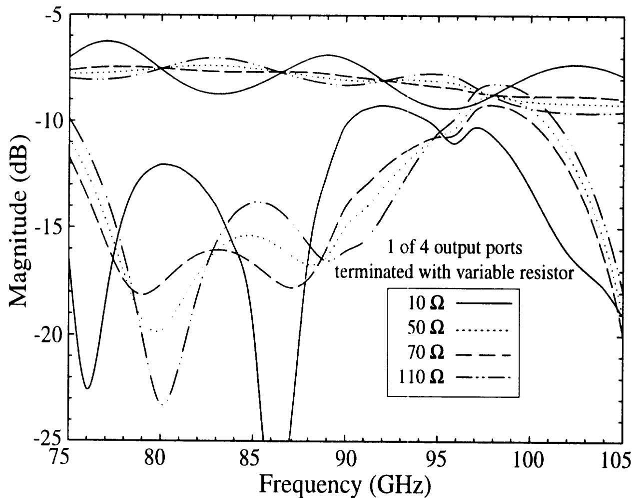



Figure B.2: Simulated effect of mismatch on 1:4 network.

## B.2 Measurement

A measurement of the 50 Ω 1:4 distribution network denoting power imbalance is shown in Figure B.3 in which one of the four measurements of identical circuits shows a ripple in insertion loss like that shown in simulation. The ripple in $S_{21}$ implies a power imbalance as the values fluctuate from -6.4 to -9 dB. The expected loss of the components alone is 0.84 dB thus measuring 0.4 dB excess insertion loss for the entire circuit is not physically possible. Thus one or more branches of the network experience power amplification while others experience power starvation. The expected loss of the network is the sum of the line loss (0.28 dB) and the component loss (0.84 dB), which is 1.12 dB above nominal, or 7.12 dB. The measured values of the other three circuits average 7.2 ± 0.1 dB at 85 GHz, validating the measurement.

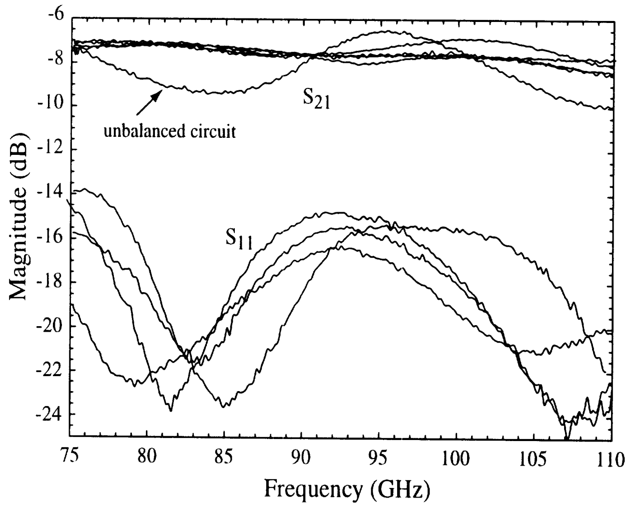



Figure B.3: Measured mismatch of 1:4 distribution network.

Possible reasons for mismatch include poor thin film resistor terminations, fallen air bridges, and unequal line lengths. For the measurement shown in Figure B.3, it is unlikely that thin film resistors are faulty based on surrounding measurements with well-matched terminations. Close examination of the circuit does reveal metal from an air bridge short-circuiting a center conductor in the Wilkinson power divider. Photographs of this are shown in Figure B.4.

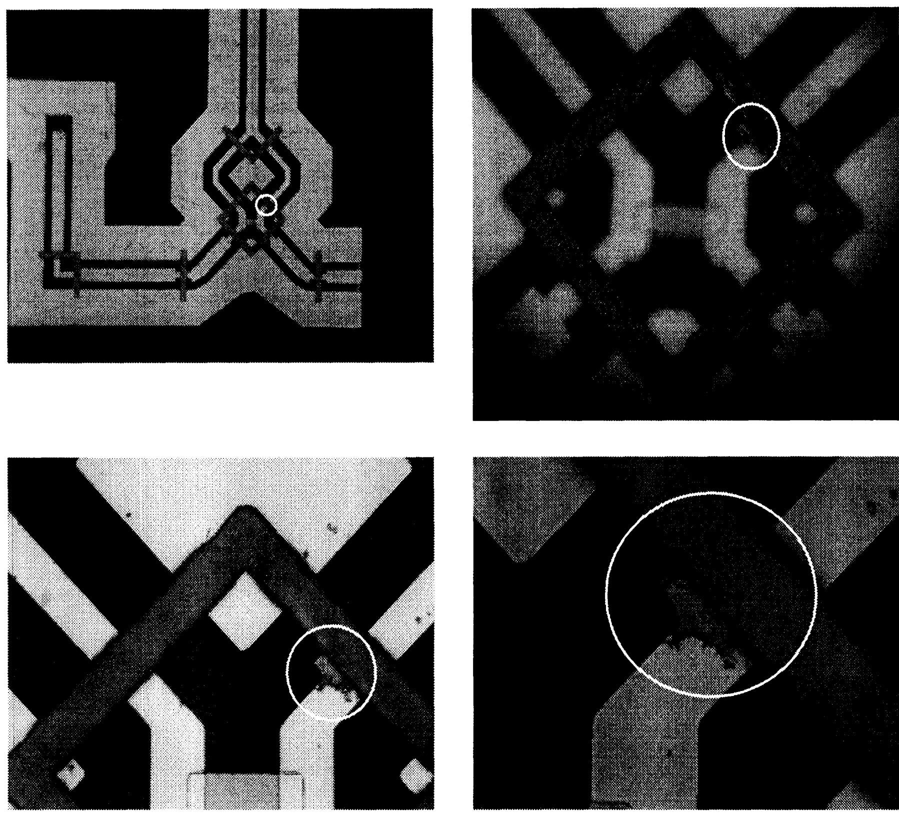


Figure B.4: Photographs of unbalanced distibution network with faulty air bridge circled.

## B.3 Conclusions

Thus, care must be taken when measuring networks with multiple branches. Ideally, four output ports would be measured simultaneously with four measurement output probes and one input probe. However, only two port measurements are possible and fabricating one circuit for each signal path and measuring each can help to discern between balanced and unbalanced measurements. Fabricating circuit combining networks in back-to-back configurations can also assist in determining the loss of the network. Additionally, replacing components with poor output port isolation, such as the reactive tee junction, can reduce cross talk between network branches.

# APPENDIX C

# FABRICATION PROCESSES

This appendix presents detailed fabrication processes for the following circuits: micromachined FGC lines, three-via vertical interconnects, micromachined circuit combining networks, membrane (microshield) filters, and the power cube.

## C.1 Micromachined FGC Lines

Wafers are 525 $\mu$m thick high-resistivity (3000 $\Omega$-cm) double-side polished silicon wafers with 7800 Å $SiO_2$ on both sides. All processing is single-sided.

1. Wafer clean
   (a) Soak in Acetone for 5 minutes.
   (b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.
   (c) Dry with nitrogen ($N_2$) air gun.
2. Circuit Metallization (electro-plating)
   (a) Evaporate electro-plating seed layer Cr/Au/Cr (500/1000/500 Å).
   (b) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
   (c) Spin positive photoresist 1827 for 30 seconds at 3 krpm.
   (d) Softbake 105 °C for 1 minute.
   (e) Align to circuit metallization mask and expose for 12 seconds at 20 mW/cm$^2$.

(f) Develop in MF 351 developer for 40 seconds.

(g) Rinse and dry with nitrogen ($N_2$) air gun.

(h) Examine circuit pattern under microscope.

(i) Descum in plasma asher for 1 minute at 80 W, 250 mT.

(j) Hardbake 130 °C for 1 minute.

(k) Etch Chrome in fresh Chrome etchant for 30 seconds.

(l) Examine gold circuit profile under microscope

(m) Electroplate gold (Au) in cyanide-based electroplating solution 2-3 $\mu$m.

(n) Remove photoresist with 30 minute hot PRS2000 soak.

(o) Etch gold (Au) seed layer in fresh gold etchant for 1 minute.

(p) Etch Chrome in fresh Chrome etchant for 30 seconds.

3. $SiO_2$ dielectric removal in Slot/Aperture Regions

(a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

(b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

(c) Softbake 105 °C for 1 minute.

(d) Align to aperture mask and expose for 12 seconds at 20 mW/cm$^2$.

(e) Develop in MF 351 developer for 40 seconds.

(f) Rinse and dry with nitrogen ($N_2$) air gun.

(g) Examine circuit pattern under microscope.

(h) Descum in plasma asher for 1 minute at 80 W, 250 mT.

(i) Hardbake 130 °C for 1 minute.

(j) Etch oxide in buffered hydrofluoric acid (BHF) for 7.8 minutes (1000 Å/min etch rate).

4. Silicon removal in Slot/Aperture Region Silicon removal may be obtained anisotropically along the crystalline $< 111 >$ planes, isotropically, or vertically with reactive ion etching. For this research effort, silicon was removed anisotropically using EDP.

(a) Etch anisotropically in EDP, KOH, or TMAH.

## C.2 Single-Layer Vertical Interconnect

Wafers are 100 $\mu$m thick high-resistivity (3000 $\Omega$-cm) double-side polished silicon wafers with 4000 Å $SiO_2$ on both sides. Since wafers are thinned, they are mounted on glass supports for each process step. Processing is double-sided with (side 1) denoting upper surface and (side 2) denoting lower surface.

1. Wafer clean

   (a) Soak in Acetone for 5 minutes.

   (b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.

   (c) Dry with nitrogen ($N_2$) air gun.

2. Mount wafers on glass support slides (side 1).

   (a) Spin positive resist 1827 at 1 krpm on glass slide.

   (b) Swab edges of slide with Acetone.

   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

   (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

   (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

3. Patch bottom via regions with Au using lift-off process (side 1). Size of patch is size of bottom via plus a 12 $\mu$m frame.

   (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm$^2$.

   (e) Image reversal bake at 130 °C for 1 minute.

   (f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.

(g) Develop in AZ 327 developer for 40 seconds.

(h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Evaporate Cr/Au (500/5000 Å).

(k) Soak samples in Acetone for metallization liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

4. Mount wafers on glass support slides (side 2).

   (a) Spin positive resist 1827 at 1 krpm on glass slide.

   (b) Swab edges of slide with Acetone.

   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

   (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

   (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

5. Patch bottom via regions with Au using lift-off process (side 2). Size of patch is size of bottom via plus a 12 $\mu$m frame.

   (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm$^2$.

   (e) Image reversal bake at 130 °C for 1 minute.

   (f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.

   (g) Develop in AZ 327 developer for 40 seconds.

   (h) Rinse and dry with nitrogen ($N_2$) air gun.

   (i) Examine edge profile under microscope.

   (j) Evaporate Cr/Au (500/5000 Å).

(k) Soak samples in Acetone for metallization liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

6. Mount wafers on glass support slides (side 1).

   (a) Spin positive resist 1827 at 1 krpm on glass slide.

   (b) Swab edges of slide with Acetone.

   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

   (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

   (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

7. Via Definition (side 1)

   (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

   (b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to aperture mask and expose for 10 seconds at 20 $mW/cm^2$.

   (e) Develop in MF 351 developer for 40 seconds.

   (f) Rinse and dry with nitrogen ($N_2$) air gun.

   (g) Examine circuit pattern under microscope.

   (h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

   (i) Hardbake 130 °C for 1.5 minutes.

   (j) Etch oxide in buffered hydrofluoric acid (BHF) for 4 minutes (1000 Å/min etch rate).

8. Mount wafers on glass support slides (side 2).

   (a) Spin positive resist 1827 at 1 krpm on glass slide.

   (b) Swab edges of slide with Acetone.

   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

(d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

(e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

9. Via Definition (side 2)

   (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

   (b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to aperture mask and expose for 10 seconds at 20 $mW/cm^2$.

   (e) Develop in MF 351 developer for 40 seconds.

   (f) Rinse and dry with nitrogen ($N_2$) air gun.

   (g) Examine circuit pattern under microscope.

   (h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

   (i) Hardbake 130 °C for 1.5 minutes.

   (j) Etch oxide in buffered hydrofluoric acid (BHF) for 4 minutes (1000 Å/min etch rate).

10. Silicon Removal for Vias

    (a) Anisotropic wet-etch using KOH through 100 $\mu$m at etch rate of 30 $\mu$m/hour.

    (b) Recipe: 300 g KOH pellets, 600 ml DI $H_2O$ at 65 °C

    (c) Note: Oxide etched at rate of 14 Å/min

11. Remove Oxide

    (a) Remaining oxide removed from entire sample

12. Mount wafers on glass support slides (side 1).

    (a) Spin positive resist 1827 at 1 krpm on glass slide.

    (b) Swab edges of slide with Acetone.

    (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

(d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

(e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

13. Circuit metallization using modified lift-off process (side 1).

    (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

    (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

    (c) Softbake 105 °C for 2 minutes.

    (d) Align to circuit metallization mask and expose for 4.5 seconds at 20 $mW/cm^2$.

    (e) Image reversal bake at 130 °C for 1 minute.

    (f) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

    (g) Develop in AZ 327 developer for 40 seconds.

    (h) Rinse and dry with nitrogen ($N_2$) air gun.

    (i) Examine edge profile under microscope.

    (j) Descum for 1 minute at 80 W, 250 mT with $O_2$ plasma.

    (k) Evaporate Cr/Au (500/9500 Å).

    (l) Soak samples in Acetone for metallization liftoff.

    (m) Soak samples in IPA for clean.

    (n) Dry with nitrogen ($N_2$) air gun.

14. Mount wafers on glass support slides (side 2).

    (a) Spin positive resist 1827 at 1 krpm on glass slide.

    (b) Swab edges of slide with Acetone.

    (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

    (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

    (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

15. Circuit metallization using modified lift-off process (side 2).

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

(c) Softbake 105 °C for 2 minutes.

(d) Align to circuit metallization mask and expose for 4.5 seconds at 20 $mW/cm^2$.

(e) Image reversal bake at 130 °C for 1 minute.

(f) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

(g) Develop in AZ 327 developer for 40 seconds.

(h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Descum for 1 minute at 80 W, 250 mT with $O_2$ plasma.

(k) Evaporate Cr/Au (500/9500 Å).

(l) Soak samples in Acetone for metallization liftoff.

(m) Soak samples in IPA for clean.

(n) Dry with nitrogen ($N_2$) air gun.

16. Mount wafers on glass support slides (side 1).

(a) Spin positive resist 1827 at 1 krpm on glass slide.

(b) Swab edges of slide with Acetone.

(c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

(d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

(e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

17. Airbridge Fabrication (side 1)

(a) Post Level

i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

iii. Softbake 105 °C for 2 minutes.

iv. Align to post mask and expose for 10 seconds at 20 $mW/cm^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.

viii. Contour bake at 130 °C for 4 minutes in oven on brick.

ix. Evaporate plating membrane of Cr/Au/Cr (500/1000/500 Å).

(b) Span Level

i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

ii. Softbake in oven only at 80 °C for 20 minutes.

iii. Remove edgebead resist if desired.

iv. Align to span mask and expose for 22 seconds at 20 $mW/cm^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

(c) Dektak (Profilometer brand name) resist profile and record PR height.

i. Etch Chrome in chrome etch for 40 seconds.

ii. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

(d) Sacrificial Layer Removal

i. Flood expose sample for 3 minutes at 20 $mW/cm^2$ to expose resist.

ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.

iii. Etch Chrome in fresh Chrome etchant for 30 seconds.

iv. Etch gold (Au) seed layer in fresh TFA gold etchant for 40 seconds.

v. Etch Chrome in fresh Chrome etchant for 30 seconds.

vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.

vii. Rinse in DI $H_20$ for 5 minutes.

viii. Soak in Acetone for 5 minutes.

ix. Soak in IPA for 5 minutes

x. Dry with nitrogen ($N_2$) air gun.

## C.3 Membrane Filters

Wafers are 525 $\mu$m thick high-resistivity double-side polished silicon wafers with a tri-dielectric membrane on both sides consisting of $SiO_2/Si_3N_4/SiO_2$ (6800/3100/4000 Å). Processing is double-sided with (side 1) denoting the upper surface and (side 2) denoting the lower surface.

1. Wafer clean
   (a) Soak in Acetone for 5 minutes.
   (b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.
   (c) Dry with nitrogen ($N_2$) air gun.
2. Circuit metallization lift-off process (side 1)
   (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.
   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.
   (c) Softbake 105 °C for 1 minute.
   (d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm$^2$.
   (e) Image reversal bake at 130 °C for 1 minute.
   (f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.
   (g) Develop in AZ 327 developer for 40 seconds.
   (h) Rinse and dry with nitrogen ($N_2$) air gun.
   (i) Examine edge profile under microscope.
   (j) Evaporate Ti/Pt/Au (300/200/9000 Å).
   (k) Soak samples in Acetone for metallization liftoff.
   (l) Soak samples in IPA for clean.
   (m) Dry with nitrogen ($N_2$) air gun.
3. Cavity patterning (side 2)

   To protect circuit metallization, photoresist is first spun on circuit side and then wafer is patterned on other side for cavity formation.

(a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm on circuit metal side.

(b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

(c) Hardbake at 130 °C for 2 minute.

(d) Spin adhesion promoter HMDS on other side for 30 seconds at 3 krpm.

(e) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

(f) Softbake 105 °C for 1 minute.

(g) Align to cavity mask and expose for 12 seconds at 20 $mW/cm^2$.

(h) Develop in MF 351 developer for 40 seconds.

(i) Rinse and dry with nitrogen ($N_2$) air gun.

(j) Examine under microscope.

(k) Hardbake at 130 °C for 1 minute.

(l) Remove exposed membrane $SiO_2/Si_3N_4/SiO_2$ (6800/3100/4000 Å) using reactive ion etching. $SiO_2$ removed with $CHF_3$ and $CF_4$. $Si_3N_4$ removed using $CF_4$ and $O_2$.

(m) Photoresist removal initiated in plasma asher with $O_2$ at 80 W for 5 minutes.

(n) Photoresist removed from both sides with Acetone soak.

(o) Soak samples in IPA for clean.

(p) Dry with nitrogen ($N_2$) air gun.

4. Cavity etch (micromachining)

Cavities etched where membrane removed using anisotropic etch. EDP is used here, although KOH or TMAH could be used. Etching 525 $\mu$m of silicon at an EDP etch rate of 65 $\mu$m/min translates to 8 hours of etching.

5. Wafer clean and support wafer mounting (side 1)

Circuit Wafer Clean

(a) Soak in Acetone for 5 minutes.

(b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.

(c) Dry with nitrogen ($N_2$) air gun.

(d) Dehydrate bake 105 °C for 1 minute.

Since samples have micromachined cavities, vacuum application on cavities may cause them to collapse. Thus samples must first be mounted on carrier wafers before processing continues. A carrier consists of a silicon wafer comparable in size to the circuit wafer with small pieces of silicon wafer (stands) placed on top using drops of photoresist around periphery used as spacer between support wafer and circuit wafer.

Support Wafer and Stand Clean

(e) Soak in Acetone for 5 minutes.

(f) Soak in Isopropyl Alcohol (IPA) for 5 minutes.

(g) Dry with nitrogen ($N_2$) air gun.

(h) Dehydrate bake 105 °C for 1 minute.

(i) Attach stands to support wafer with drops of 1827 photoresist.

(j) Hardbake at 130 °C for 2 minutes.

(k) Place small drops of 1827 photoresist on stands and gently place circuit wafer on stands/support wafer.

(l) Hardbake at 130 °C for 2 minutes.

6. Thin-Film Capacitor Fabrication: SiO insulating layer deposition (side 1)

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

(c) Softbake 105 °C for 1 minute.

(d) Align to SiO mask and expose for 4.5 seconds at 20 mW/cm$^2$.

(e) Image reversal bake at 130 °C for 1 minute.

(f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.

(g) Develop in AZ 327 developer for 40 seconds.

(h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Evaporate 1 $\mu$m SiO.

(k) Soak samples in Acetone for SiO liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

7. Support wafer mounting (side 1)

   (a) Soak support wafers and stands in Acetone for 5 minutes.

   (b) Soak support wafers and stands in Isopropyl Alcohol (IPA) for 5 minutes.

   (c) Dry with nitrogen ($N_2$) air gun.

   (d) Dehydrate bake 105 °C for 1 minute.

   (e) Attach stands to support wafer with drops of 1827 photoresist.

   (f) Hardbake at 130 °C for 2 minutes.

   (g) Place small drops of 1827 photoresist on stands and gently place circuit wafer on stands/support wafer.

   (h) Hardbake at 130 °C for 2 minutes.

8. Thin-Film Capacitor Fabrication: Upper metallization layer deposition (side 2).

   (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

   (c) Softbake 105 °C for 1 minute.

   (d) Align to capacitor metal mask and expose for 4.5 seconds at 20 $mW/cm^2$.

   (e) Image reversal bake at 130 °C for 1 minute.

   (f) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

   (g) Develop in AZ 327 developer for 40 seconds.

   (h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Evaporate Ti/Al/Ti/Au (500/7000/300/2000 Å).

(k) Soak samples in Acetone for metallization liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

## C.4 Power Cube

### C.4.1 Antenna Layer

Wafers are 200 $\mu$m thick high-resistivity (3000 $\Omega$-cm) double-side polished silicon wafers with 4000 Å $SiO_2$ on both sides. Processing is double-sided with (side 1) denoting upper surface and (side2) denoting lower surface.

1. Wafer clean

   (a) Soak in Acetone for 5 minutes.

   (b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.

   (c) Dry with nitrogen ($N_2$) air gun.

2. Bonding pad base metallization using lift-off (side 2).

   (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

   (c) Softbake 105 °C for 1 minute.

   (d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm$^2$.

   (e) Image reversal bake at 130 °C for 1 minute.

   (f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.

   (g) Develop in AZ 327 developer for 40 seconds.

   (h) Rinse and dry with nitrogen ($N_2$) air gun.

   (i) Examine edge profile under microscope.

(j) Evaporate Cr/Au (500/9500 Å).

(k) Soak samples in Acetone for metallization liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

3. Electroplate bonding pads (side 2)

   (a) Base level

      i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
      ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.
      iii. Softbake 105 °C for 2 minutes.
      iv. Align to mask and expose for 10 seconds at 20 mW/cm$^2$.
      v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.
      vi. Rinse and dry with nitrogen ($N_2$) air gun.
      vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.
      viii. Contour bake at 130 °C for 4 minutes in oven on brick.
      ix. Evaporate plating membrane of Cr/Au/Cr (500/1000/500 Å).

   (b) Pad level

      i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.
      ii. Softbake in oven only at 80 °C for 20 minutes.
      iii. Remove edgebead resist if desired.
      iv. Align to span mask and expose for 22 seconds at 20 mW/cm$^2$.
      v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.
      vi. Rinse and dry with nitrogen ($N_2$) air gun.
      vii. Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

   (c) Dektak (Profilometer brand name) resist profile and record PR height.

      i. Etch Chrome in chrome etch for 40 seconds.
      ii. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

(d) Sacrificial Layer Removal

  i. Flood expose sample for 3 minutes at 20 mW/cm$^2$ to expose resist.
  ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.
  iii. Etch Chrome in fresh Chrome etchant for 30 seconds.
  iv. Etch gold (Au) seed layer in fresh TFA gold etchant for 40 seconds.
  v. Etch Chrome in fresh Chrome etchant for 30 seconds.
  vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.
  vii. Rinse in DI $H_20$ for 5 minutes.
  viii. Soak in Acetone for 5 minutes.
  ix. Soak in IPA for 5 minutes
  x. Dry with nitrogen ($N_2$) air gun.

4. Antenna patch metallization using lift-off (side 1)

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.
(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.
(c) Softbake 105 °C for 1 minute.
(d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm$^2$.
(e) Image reversal bake at 130 °C for 1 minute.
(f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.
(g) Develop in AZ 327 developer for 40 seconds.
(h) Rinse and dry with nitrogen ($N_2$) air gun.
(i) Examine edge profile under microscope.
(j) Evaporate Cr/Au (500/9500 Å).
(k) Soak samples in Acetone for metallization liftoff.
(l) Soak samples in IPA for clean.
(m) Dry with nitrogen ($N_2$) air gun.

5. Pattern oxide for cavities (side 2)

(a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

(b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

(c) Softbake 105 °C for 2 minutes.

(d) Align to aperture mask and expose for 10 seconds at 20 $mW/cm^2$.

(e) Develop in MF 351 developer for 40 seconds.

(f) Rinse and dry with nitrogen ($N_2$) air gun.

(g) Examine circuit pattern under microscope.

(h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

(i) Hardbake 130 °C for 1.5 minutes.

(j) Etch oxide in buffered hydrofluoric acid (BHF) for 4 minutes (1000 Å/min etch rate).

6. Silicon Removal for cavities (side 2)

(a) Anisotropic wet-etch using KOH through 150 $\mu$m at etch rate of 30 $\mu$m/hour.

(b) Recipe: 300 g KOH pellets, 600 ml DI $H_2O$ at 65 °C

(c) Note: Oxide etched at rate of 14 Å/min

### C.4.2 Feed Layer

Wafers are 100 $\mu$m thick high-resistivity (3000 $\Omega$-cm) double-side polished silicon wafers with 4000 Å $SiO_2$ on both sides. Processing is double-sided with (side 1) denoting upper surface and (side2) denoting lower surface.

1. Wafer clean

(a) Soak in Acetone for 5 minutes.

(b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.

(c) Dry with nitrogen ($N_2$) air gun.

2. Bonding pad base metallization using lift-off (side 2)

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

(c) Softbake 105 °C for 1 minute.

(d) Align to circuit metallization mask and expose for 4.5 seconds at 20 $mW/cm^2$.

(e) Image reversal bake at 130 °C for 1 minute.

(f) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

(g) Develop in AZ 327 developer for 40 seconds.

(h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Evaporate Cr/Au (500/9500 Å).

(k) Soak samples in Acetone for metallization liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

3. Electroplate bonding pads (side 2)

   (a) Base level

      i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
      ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.
      iii. Softbake 105 °C for 2 minutes.
      iv. Align to mask and expose for 10 seconds at 20 $mW/cm^2$.
      v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.
      vi. Rinse and dry with nitrogen ($N_2$) air gun.
      vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.
      viii. Contour bake at 130 °C for 4 minutes in oven on brick.
      ix. Evaporate plating membrane of Cr/Au/Cr (500/1000/500 Å).

   (b) Pad level

      i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

ii. Softbake in oven only at 80 °C for 20 minutes.

iii. Remove edgebead resist if desired.

iv. Align to span mask and expose for 22 seconds at 20 $mW/cm^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

(c) Dektak (Profilometer brand name) resist profile and record PR height.

i. Etch Chrome in chrome etch for 40 seconds.

ii. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

(d) Sacrificial Layer Removal

i. Flood expose sample for 3 minutes at 20 $mW/cm^2$ to expose resist.

ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.

iii. Etch Chrome in fresh Chrome etchant for 30 seconds.

iv. Etch gold (Au) seed layer in fresh TFA gold etchant for 40 seconds.

v. Etch Chrome in fresh Chrome etchant for 30 seconds.

vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.

vii. Rinse in DI $H_20$ for 5 minutes.

viii. Soak in Acetone for 5 minutes.

ix. Soak in IPA for 5 minutes

x. Dry with nitrogen ($N_2$) air gun.

4. Circuit Metallization using lift-off (side 2)

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

(c) Softbake 105 °C for 1 minute.

(d) Align to circuit metallization mask and expose for 4.5 seconds at 20 $mW/cm^2$.

(e) Image reversal bake at 130 °C for 1 minute.

(f) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

(g) Develop in AZ 327 developer for 40 seconds.

(h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Evaporate Cr/Au (500/9500 Å).

(k) Soak samples in Acetone for metallization liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

5. Circuit Metallization of slots using lift-off (side 1)

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

(c) Softbake 105 °C for 1 minute.

(d) Align to circuit metallization mask and expose for 4.5 seconds at 20 $mW/cm^2$.

(e) Image reversal bake at 130 °C for 1 minute.

(f) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

(g) Develop in AZ 327 developer for 40 seconds.

(h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Evaporate Cr/Au (500/9500 Å).

(k) Soak samples in Acetone for metallization liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

6. Electroplate bonding pads (side 2)

(a) Base level

i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

iii. Softbake 105 °C for 2 minutes.

iv. Align to mask and expose for 10 seconds at 20 mW/cm$^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.

viii. Contour bake at 130 °C for 4 minutes in oven on brick.

ix. Evaporate plating membrane of Cr/Au/Cr (500/1000/500 Å).

(b) Pad level

i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

ii. Softbake in oven only at 80 °C for 20 minutes.

iii. Remove edgebead resist if desired.

iv. Align to span mask and expose for 22 seconds at 20 mW/cm$^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

viii. Dektak(Profilometer brand name) resist profile and record PR height.

ix. Etch Chrome in chrome etch for 40 seconds.

x. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

(c) Sacrificial Layer Removal

i. Flood expose sample for 3 minutes at 20 mW/cm$^2$ to expose resist.

ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.

iii. Etch Chrome in fresh Chrome etchant for 30 seconds.

iv. Etch gold (Au) seed layer in fresh TFA gold etchant for 40 seconds.

v. Etch Chrome in fresh Chrome etchant for 30 seconds.

vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.

vii. Rinse in DI $H_20$ for 5 minutes.

viii. Soak in Acetone for 5 minutes.

ix. Soak in IPA for 5 minutes

x. Dry with nitrogen ($N_2$) air gun.

7. Airbridge and RF transition fabrication (side 2)

(a) Post Level

i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

iii. Softbake 105 °C for 2 minutes.

iv. Align to post mask and expose for 10 seconds at 20 mW/cm$^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.

viii. Contour bake at 130 °C for 4 minutes in oven on brick.

ix. Evaporate plating membrane of Cr/Au/Cr (500/1000/500 Å).

(b) Span Level

i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

ii. Softbake in oven only at 80 °C for 20 minutes.

iii. Remove edgebead resist if desired.

iv. Align to span mask and expose for 22 seconds at 20 mW/cm$^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

viii. Dektak(Profilometer brand name) resist profile and record PR height.

ix. Etch Chrome in chrome etch for 40 seconds.

x. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

(c) Sacrificial Layer Removal

i. Flood expose sample for 3 minutes at 20 mW/cm$^2$ to expose resist.

ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.

iii. Etch Chrome in fresh Chrome etchant for 30 seconds.

iv. Etch gold (Au) seed layer in fresh TFA gold etchant for 40 seconds.

v. Etch Chrome in fresh Chrome etchant for 30 seconds.

vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.

vii. Rinse in DI $H_20$ for 5 minutes.

viii. Soak in Acetone for 5 minutes.

ix. Soak in IPA for 5 minutes

x. Dry with nitrogen ($N_2$) air gun.

8. Pattern oxide for cavities (side 2)

   (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

   (b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to aperture mask and expose for 10 seconds at 20 mW/cm$^2$.

   (e) Develop in MF 351 developer for 40 seconds.

   (f) Rinse and dry with nitrogen ($N_2$) air gun.

   (g) Examine circuit pattern under microscope.

   (h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

   (i) Hardbake 130 °C for 1.5 minutes.

   (j) Etch oxide in buffered hydrofluoric acid (BHF) for 4 minutes (1000 Å/min etch rate).

9. Silicon Removal for Cavities (side 2)

   (a) Anisotropic wet-etch using KOH through 40 $\mu$m at etch rate of 30 $\mu$m/hour.

   (b) Recipe: 300 g KOH pellets, 600 ml DI $H_2O$ at 65 °C

   (c) Note: Oxide etched at rate of 14 Å/min

### C.4.3 MMIC Layer

Wafers are 100 $\mu$m thick high-resistivity (3000 $\Omega$-cm) double-side polished silicon wafers with 4000 Å $SiO_2$ on both sides. Since wafers are thinned, they are mounted on glass supports for each process step. Processing is double-sided with (side 1) denoting upper surface and (side2) denoting lower surface.

1. Wafer clean
   (a) Soak in Acetone for 5 minutes.
   (b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.
   (c) Dry with nitrogen ($N_2$) air gun.
2. Mount wafers on glass support slides.
   (a) Spin positive resist 1827 at 1 krpm on glass slide.
   (b) Swab edges of slide with Acetone.
   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.
   (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.
   (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.
3. Patch bottom via regions with Au using lift-off (side 1)

   Size of patch is size of bottom via plus a 12 $\mu$m frame.
   (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.
   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.
   (c) Softbake 105 °C for 2 minutes.
   (d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm$^2$.
   (e) Image reversal bake at 130 °C for 1 minute.
   (f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.
   (g) Develop in AZ 327 developer for 40 seconds.
   (h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Evaporate Cr/Au (500/5000 Å).

(k) Soak samples in Acetone for metallization liftoff.

(l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

4. Mount wafers on glass support slides.

   (a) Spin positive resist 1827 at 1 krpm on glass slide.

   (b) Swab edges of slide with Acetone.

   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

   (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

   (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

5. Patch bottom via regions with Au using lift-off (side 2) Size of patch is size of bottom via plus a 12 $\mu$m frame.

   (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm$^2$.

   (e) Image reversal bake at 130 °C for 1 minute.

   (f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.

   (g) Develop in AZ 327 developer for 40 seconds.

   (h) Rinse and dry with nitrogen ($N_2$) air gun.

   (i) Examine edge profile under microscope.

   (j) Evaporate Cr/Au (500/5000 Å).

   (k) Soak samples in Acetone for metallization liftoff.

   (l) Soak samples in IPA for clean.

(m) Dry with nitrogen ($N_2$) air gun.

6. Mount wafers on glass support slides.

   (a) Spin positive resist 1827 at 1 krpm on glass slide.

   (b) Swab edges of slide with Acetone.

   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

   (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

   (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

7. Via Definition (side 1)

   (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

   (b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to aperture mask and expose for 10 seconds at 20 $mW/cm^2$.

   (e) Develop in MF 351 developer for 40 seconds.

   (f) Rinse and dry with nitrogen ($N_2$) air gun.

   (g) Examine circuit pattern under microscope.

   (h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

   (i) Hardbake 130 °C for 1.5 minutes.

   (j) Etch oxide in buffered hydrofluoric acid (BHF) for 4 minutes (1000 Å/min etch rate).

8. Mount wafers on glass support slides.

   (a) Spin positive resist 1827 at 1 krpm on glass slide.

   (b) Swab edges of slide with Acetone.

   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

   (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

   (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

9. Via Definition (side 2)

   (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

   (b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to aperture mask and expose for 10 seconds at 20 $mW/cm^2$.

   (e) Develop in MF 351 developer for 40 seconds.

   (f) Rinse and dry with nitrogen ($N_2$) air gun.

   (g) Examine circuit pattern under microscope.

   (h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

   (i) Hardbake 130 °C for 1.5 minutes.

   (j) Etch oxide in buffered hydrofluoric acid (BHF) for 4 minutes (1000 Å/min etch rate).

10. Silicon Removal for Vias and Cavities

   (a) Anisotropic wet-etch using KOH through 100 $\mu$m at etch rate of 30 $\mu$m/hour.

   (b) Recipe: 300 g KOH pellets, 600 ml DI $H_2O$ at 65 °C

   (c) Note: Oxide etched at rate of 14 Å/min

11. Mount wafers on glass support slides.

   (a) Spin positive resist 1827 at 1 krpm on glass slide.

   (b) Swab edges of slide with Acetone.

   (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

   (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

   (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

12. $SiO_2$ removal around via regions (side 1)

    $SiO_2$ is removed from around etched via regions to ensure step coverage of circuit metal. KOH yields a small amount of undercut.

(a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

(b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

(c) Softbake 105 °C for 2 minutes.

(d) Align to via oxide mask and expose for 10 seconds at 20 $mW/cm^2$.

(e) Develop in MF 351 developer for 40 seconds.

(f) Rinse and dry with nitrogen ($N_2$) air gun.

(g) Examine circuit pattern under microscope.

(h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

(i) Hardbake 130 °C for 1.5 minutes.

(j) Etch oxide in buffered hydrofluoric acid (BHF) for 4 minutes (1000 Å/min etch rate).

(k) Rinse in $DiH_2O$

(l) Dry with nitrogen ($N_2$) air gun.

(m) Soak in ACETONE to remove resist.

(n) Soak in IPA.

(o) Dry with nitrogen ($N_2$) air gun.

13. Mount wafers on glass support slides.

(a) Spin positive resist 1827 at 1 krpm on glass slide.

(b) Swab edges of slide with Acetone.

(c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

(d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

(e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

14. $SiO_2$ removal around via regions of other side (side 2)

$SiO_2$ is removed from around etched via regions to ensure step coverage of circuit metal. KOH yields a small amount of undercut.

(a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

(b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

(c) Softbake 105 °C for 2 minutes.

(d) Align to via oxide mask and expose for 10 seconds at 20 $mW/cm^2$.

(e) Develop in MF 351 developer for 40 seconds.

(f) Rinse and dry with nitrogen ($N_2$) air gun.

(g) Examine circuit pattern under microscope.

(h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

(i) Hardbake 130 °C for 1.5 minutes.

(j) Etch oxide in buffered hydrofluoric acid (BHF) for 4 minutes (1000 Å/min etch rate).

(k) Rinse in $DiH_2O$

(l) Dry with nitrogen ($N_2$) air gun.

(m) Soak in ACETONE to remove resist.

(n) Soak in IPA.

(o) Dry with nitrogen ($N_2$) air gun.

15. TaN resistors (More detailed information given in dissertation of Brown [11].) (side 1)

    (a) Clean sample in Acetone and IPA.

    (b) Reactively sputter 700 Åof $Ta_2N$ with sputtering pressure of 1 mtorr, a nitrogen ratio of 10%, and 3 Amp current for 2.5 minutes. This should result in 43 $\Omega$/sq sheet resistance.

    (c) Sputter W/Ti (5%) for 1 minute at 650 W in an Argon ambient at 7 mtorr, which should yield 100 Å.

    (d) Spin 1813 PR for 30 sec at 3.5 krpm.

    (e) Softbake 105 °C for 1 minute.

(f) Align and expose corners with edge bead removal mask for 30 seconds at 20 $mW/cm^2$.

(g) Develop in MF 351 developer for 40 seconds.

(h) Align TaN mask and expose for 6 sec. at 20 $mw/cm^2$.

(i) Develop in MF 351 developer for 30 seconds.

(j) Rinse and dry with nitrogen ($N_2$) air gun.

(k) Examine circuit pattern under microscope.

(l) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

(m) Hardbake 130 °C for 1.5 minutes.

(n) Etch exposed W/Ti and $Ta_2N$ in Semi-Group Reactive Ion Etcher (RIE). The etch is in an $SF_6$:Ar plasma with gas flows of 10 sccm and 5 sccm, respectively. The other etch parameters are 10 mtorr for 5 minutes at 100 W.

(o) Etch the top of the photoresist film to remove organic residue in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

(p) Soak in ACETONE to remove resist.

(q) Soak in IPA.

(r) Dry with nitrogen ($N_2$) air gun.

16. Repeat TaN resistors (side 2)

17. Mount wafers on glass support slides.

    (a) Spin positive resist 1827 at 1 krpm on glass slide.

    (b) Swab edges of slide with Acetone.

    (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

    (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

    (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

18. Circuit Metallization using modified lift-off process (side 1)

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

(c) Softbake 105 °C for 2 minutes.

(d) Align to circuit metallization mask and expose for 4.5 seconds at 20 $mW/cm^2$.

(e) Image reversal bake at 130 °C for 1 minute.

(f) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

(g) Develop in AZ 327 developer for 40 seconds.

(h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Descum for 1 minute at 80 W, 250 mT with $O_2$ plasma.

(k) Clean contact areas of thin film resistors with hydrochloric acid: DI $H_2O$ in 1:1 ratio. Rinse in DI water and dry. This step should be performed just before evaporation.

(l) Evaporate Cr/Au (500/9500 Å).

(m) Soak samples in Acetone for metallization liftoff.

(n) Soak samples in IPA for clean.

(o) Dry with nitrogen ($N_2$) air gun.

19. Mount wafers on glass support slides.

(a) Spin positive resist 1827 at 1 krpm on glass slide.

(b) Swab edges of slide with Acetone.

(c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

(d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

(e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

20. Circuit Metallization using modified lift-off process (side 2)

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

(c) Softbake 105 °C for 2 minutes.

(d) Align to circuit metallization mask and expose for 4.5 seconds at 20 mW/cm$^2$.

(e) Image reversal bake at 130 °C for 1 minute.

(f) Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.

(g) Develop in AZ 327 developer for 40 seconds.

(h) Rinse and dry with nitrogen ($N_2$) air gun.

(i) Examine edge profile under microscope.

(j) Descum for 1 minute at 80 W, 250 mT with $O_2$ plasma.

(k) Evaporate Ti/Au (500/9500 Å).

(l) Soak samples in Acetone for metallization liftoff.

(m) Soak samples in IPA for clean.

(n) Dry with nitrogen ($N_2$) air gun.

21. Mount wafers on glass support slides.

    (a) Spin positive resist 1827 at 1 krpm on glass slide.

    (b) Swab edges of slide with Acetone.

    (c) Gently place 100 $\mu$m Si wafer on slide, pressing corners down.

    (d) Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.

    (e) Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

22. Fabrication of Nickel Solderable Pads for MMIC Flip-Chip Bonding (side 1)

    Nickel solderable pads need to be fabricated for flip-chip bonding of the four MMICs. Nickel has a lot of tensile stress and is difficult to evaporate because it tends to peel up during evaporation taking the underlying photoresist with it. Because of this nickel is typically deposited in thin layers of 2000 Å. 500 Å of Ti may be interleaved with 2000 Å layers of Ni to form thicker Ni layers. Nickel also oxidizes rapidly, thus a thin layer of Au covers the nickel pad to prevent oxidation. Additionally, a ring of

Cr surrounds the Au/Ni pad, providing a solder stop during the flip-chip bonding process.

(a) Nickel circular pad deposition using lift-off process

 i. Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.
 ii. Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.
 iii. Softbake 105 °C for 2 minutes.
 iv. Align to nickel mask and expose for 4.5 seconds at 20 mW/cm$^2$.
 v. Image reversal bake at 130 °C for 1 minute.
 vi. Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.
 vii. Develop in AZ 327 developer for 40 seconds.
 viii. Rinse and dry with nitrogen ($N_2$) air gun.
 ix. Examine edge profile under microscope.
 x. Descum for 1 minute at 80 W, 250 mT with $O_2$ plasma.
 xi. Evaporate Ni/Au (2000/500 Å).
 xii. Soak samples in Acetone for metallization liftoff.
 xiii. Soak samples in IPA for clean.
 xiv. Dry with nitrogen ($N_2$) air gun.

(b) Mount wafers on glass support slides.

 i. Spin positive resist 1827 at 1 krpm on glass slide.
 ii. Swab edges of slide with Acetone.
 iii. Gently place 100 $\mu$m Si wafer on slide, pressing corners down.
 iv. Dehydrate bake Si wafer on glass carrier for 2 minutes at 80 °C.
 v. Hardbake Si wafer on glass carrier for 2 minutes at 130 °C.

(c) Chrome barrier ring deposition using lift-off process

 i. Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.
 ii. Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.
 iii. Softbake 105 °C for 2 minutes.

iv. Align to chrome mask and expose for 4.5 seconds at 20 mW/cm$^2$.

v. Image reversal bake at 130 °C for 1 minute.

vi. Flood expose (no mask) for 1 minute at 20 mW/cm$^2$.

vii. Develop in AZ 327 developer for 40 seconds.

viii. Rinse and dry with nitrogen ($N_2$) air gun.

ix. Examine edge profile under microscope.

x. Descum for 1 minute at 80 W, 250 mT with $O_2$ plasma.

xi. Evaporate Cr (2000 Å).

xii. Soak samples in Acetone for metallization liftoff.

xiii. Soak samples in IPA for clean.

xiv. Dry with nitrogen ($N_2$) air gun.

23. Airbridge fabrication (side 1)

(a) Post Level

i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

iii. Softbake 105 °C for 2 minutes.

iv. Align to post mask and expose for 10 seconds at 20 mW/cm$^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.

viii. Contour bake at 130 °C for 4 minutes in oven on brick.

ix. Evaporate plating membrane of Cr/Au/Cr (500/1000/500 Å).

(b) Span Level

i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

ii. Softbake in oven only at 80 °C for 20 minutes.

iii. Remove edgebead resist if desired.

iv. Align to span mask and expose for 22 seconds at 20 mW/cm$^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.

viii. Dektak(Profilometer brand name) resist profile and record PR height.

ix. Etch Chrome in chrome etch for 40 seconds.

x. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

(c) Sacrificial Layer Removal

i. Flood expose sample for 3 minutes at 20 mW/cm$^2$ to expose resist.

ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.

iii. Etch Chrome in fresh Chrome etchant for 30 seconds.

iv. Etch gold(Au) seed layer in fresh TFA gold etchant for 40 seconds.

v. Etch Chrome in fresh Chrome etchant for 30 seconds.

vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.

vii. Rinse in DI $H_20$ for 5 minutes.

viii. Soak in Acetone for 5 minutes.

ix. Soak in IPA for 5 minutes

x. Dry with nitrogen ($N_2$) air gun.

24. Airbridge and wafer-to-wafer transition (side 2)

(a) Post Level

i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

iii. Softbake 105 °C for 2 minutes.

iv. Align to post mask and expose for 10 seconds at 20 mW/cm$^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.

viii. Contour bake at 130 °C for 4 minutes in oven on brick.

ix. Evaporate plating membrane of Cr/Au/Cr (500/1000/500 Å).

(b) Span Level

i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.

ii. Softbake in oven only at 80 °C for 20 minutes.

iii. Remove edgebead resist if desired.

iv. Align to span mask and expose for 22 seconds at 20 $mW/cm^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.

viii. Dektak(Profilometer brand name) resist profile and record PR height.

ix. Etch Chrome in chrome etch for 40 seconds.

x. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

(c) Sacrificial Layer Removal

i. Flood expose sample for 3 minutes at 20 $mW/cm^2$ to expose resist.

ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.

iii. Etch Chrome in fresh Chrome etchant for 30 seconds.

iv. Etch gold(Au) seed layer in fresh TFA gold etchant for 40 seconds.

v. Etch Chrome in fresh Chrome etchant for 30 seconds.

vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.

vii. Rinse in DI $H_20$ for 5 minutes.

viii. Soak in Acetone for 5 minutes.

ix. Soak in IPA for 5 minutes

x. Dry with nitrogen ($N_2$) air gun.

### C.4.4 Support Layer

The support wafer is a mechanical wafer whose purpose is to support the circuits on the MMIC layer and the MMICs to be flip-chip bonded. The wafer is full thickness silicon

(500 $\mu$m) and is double-side processed with sides 1 and 2 denoted as upper and lower wafer surfaces, respectively.

1. Metallization of alignment marks and bias pad using lift-off (side 2)

   (a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

   (c) Softbake 105 °C for 2 minutes.

   (d) Align to alignment mark mask and expose for 4.5 seconds at 20 $mW/cm^2$.

   (e) Image reversal bake at 130 °C for 1 minute.

   (f) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

   (g) Develop in AZ 327 developer for 40 seconds.

   (h) Rinse and dry with nitrogen ($N_2$) air gun.

   (i) Examine edge profile under microscope.

   (j) Descum for 1 minute at 80 W, 250 mT with $O_2$ plasma.

   (k) Evaporate Cr/Au (500/5000 Å).

   (l) Soak samples in Acetone for metallization liftoff.

   (m) Soak samples in IPA for clean.

   (n) Dry with nitrogen ($N_2$) air gun.

2. $SiO_2$ dielectric removal for MMIC, input, and DC bias probe openings (side 2)

   (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

   (b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

   (c) Softbake 105 °C for 1 minute.

   (d) Align to aperture mask and expose for 12 seconds at 20 $mW/cm^2$.

   (e) Develop in MF 351 developer for 40 seconds.

   (f) Rinse and dry with nitrogen ($N_2$) air gun.

   (g) Examine circuit pattern under microscope.

(h) Descum in plasma asher for 1 minute at 80 W, 250 mT.

(i) Hardbake 130 °C for 1 minute.

(j) Etch oxide in buffered hydrofluoric acid (BHF) to completely remove oxide (1000 Å/min etch rate).

3. Bonding pad fabrication (side 1)

   (a) Base Level

      i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
      ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.
      iii. Softbake 105 °C for 2 minutes.
      iv. Align to post mask and expose for 10 seconds at 20 mW/cm$^2$.
      v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.
      vi. Rinse and dry with nitrogen ($N_2$) air gun.
      vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.
      viii. Contour bake at 130 °C for 4 minutes in oven on brick.
      ix. Evaporate plating membrane of Cr/Au/Cr (500/1000/500 Å).

   (b) Pad Level

      i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.
      ii. Softbake in oven only at 80 °C for 20 minutes.
      iii. Remove edgebead resist if desired.
      iv. Align to span mask and expose for 22 seconds at 20 mW/cm$^2$.
      v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.
      vi. Rinse and dry with nitrogen ($N_2$) air gun.
      vii. Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.
      viii. Dektak(Profilometer brand name) resist profile and record PR height.
      ix. Etch Chrome in chrome etch for 40 seconds.
      x. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

   (c) Sacrificial Layer Removal

i. Flood expose sample for 3 minutes at 20 mW/cm$^2$ to expose resist.

ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.

iii. Etch Chrome in fresh Chrome etchant for 30 seconds.

iv. Etch gold (Au) seed layer in fresh TFA gold etchant for 40 seconds.

v. Etch Chrome in fresh Chrome etchant for 30 seconds.

vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.

vii. Rinse in DI $H_20$ for 5 minutes.

viii. Soak in Acetone for 5 minutes.

ix. Soak in IPA for 5 minutes

x. Dry with nitrogen ($N_2$) air gun.

4. $SiO_2$ dielectric removal for protective cavities (side 1)

   (a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

   (b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

   (c) Softbake 105 °C for 1 minute.

   (d) Align to aperture mask and expose for 12 seconds at 20 mW/cm$^2$.

   (e) Develop in MF 351 developer for 40 seconds.

   (f) Rinse and dry with nitrogen ($N_2$) air gun.

   (g) Examine circuit pattern under microscope.

   (h) Descum in plasma asher for 1 minute at 80 W, 250 mT.

   (i) Hardbake 130 °C for 1 minute.

   (j) Etch oxide in buffered hydrofluoric acid (BHF) to partially remove oxide (1000 Å/min etch rate).

5. Silicon Removal for Cavities and MMIC, input, and DC bias probe openings (side 2)

   (a) Anisotropic wet-etch using KOH through 150 $\mu$m at etch rate of 30 $\mu$m/hour.

   (b) Recipe: 300 g KOH pellets, 600 ml DI $H_2O$ at 65 °C

   (c) Note: Oxide etched at rate of 14 Å/min

## C.5 50 and 70 Ω Micromachined Circuit Combining Networks

Wafers are 400 $\mu$m thick high-resistivity (3000 Ω-cm) double-side polished silicon wafers with 6600 Å $SiO_2$ on both sides. NiCr is used here instead of TaN because NiCr is not etched in KOH, the anisotropic etchant used to create the micromachined grooves. Processing is single-sided.

1. Wafer clean
   (a) Soak in Acetone for 5 minutes.
   (b) Soak in Isopropyl Alcohol (IPA) for 5 minutes.
   (c) Dry with nitrogen ($N_2$) air gun.
2. NiCr resistors Before depositing NiCr evaporate NiCr on glass slide and measure surface resistance with 4 point probe.
   (a) Spin adhesion promoter HMDS for 30 seconds at 4.5 krpm.
   (b) Spin image reversal photoresist AZ 5214 for 30 seconds at 4.5 krpm.
   (c) Softbake 105 °C for 2 minutes.
   (d) Align edge bead removal mask and expose for 1 minute at 20 mW/cm$^2$.
   (e) Develop in AZ 327 developer for 40 seconds.
   (f) Dehydrate bake 105 °C for 2 minutes.
   (g) Align to NiCr resistor mask and expose for 5 seconds at 20 mW/cm$^2$.
   (h) Image reversal bake at 130 °C for 1 minute.
   (i) Flood expose (no mask) for 1.5 minute at 20 mW/cm$^2$.
   (j) Develop in AZ 327 developer for 40 seconds.
   (k) Rinse and dry with nitrogen ($N_2$) air gun.
   (l) Examine edge profile under microscope.
   (m) Evaporate NiCr at 42 Ω/square (400 Å).

(n) Soak samples in hot PRS2000 for liftoff (10-15 min).

(o) Soak samples in DI H20 quench.

(p) Soak samples in Acetone for clean.

(q) Soak samples in IPA for clean.

(r) Dry with nitrogen ($N_2$) air gun.

3. Circuit metallization (lift-off)

(a) Spin adhesion promoter HMDS for 30 seconds at 2.5 krpm.

(b) Spin image reversal photoresist AZ 5214 for 30 seconds at 2.5 krpm.

(c) Softbake 105 °C for 2 minutes.

(d) Align edge bead removal mask and expose for 1 minute at 20 $mW/cm^2$.

(e) Develop in AZ 327 developer for 40 seconds.

(f) Dehydrate bake 105 °C for 2 minutes.

(g) Align to circuit metallization mask and expose for 4.5 seconds at 20 $mW/cm^2$.

(h) Image reversal bake at 130 °C for 1 minute.

(i) Flood expose (no mask) for 1 minute at 20 $mW/cm^2$.

(j) Develop in AZ 327 developer for 40 seconds.

(k) Rinse and dry with nitrogen ($N_2$) air gun.

(l) Examine edge profile under microscope.

(m) Evaporate Cr/Au (500/9500 Å).

(n) Soak samples in Acetone for metallization liftoff.

(o) Soak samples in IPA for clean.

(p) Dry with nitrogen ($N_2$) air gun.

4. Slot definition

(a) Spin adhesion promoter HMDS for 30 seconds at 3 krpm.

(b) Spin positive photoresist 1827 for 30 seconds at 3 krpm.

(c) Softbake 105 °C for 2 minutes.

(d) Align to oxide mask and expose for 10 seconds at 20 $mW/cm^2$.

(e) Develop in MF 351 developer for 40 seconds.

(f) Rinse and dry with nitrogen ($N_2$) air gun.

(g) Examine circuit pattern under microscope.

(h) Descum in plasma asher for 1 minute at 80 W, 250 mT in $O_2$ plasma.

(i) Hardbake 130 °C for 1.5 minutes.

(j) Etch oxide in buffered hydrofluoric acid (BHF) for 6.6 minutes (1000 Å/min etch rate).

5. Topside Airbridge Fabrication

   (a) Post Level

      i. Spin adhesion promoter HMDS for 30 seconds at 3 krpm.
      ii. Spin positive photoresist 1827 for 30 seconds at 3 krpm.
      iii. Softbake 105 °C for 2 minutes.
      iv. Remove edgebead resist if desired.
      v. Align to post mask and expose for 10 seconds at 20 $mW/cm^2$.
      vi. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.
      vii. Rinse and dry with nitrogen ($N_2$) air gun.
      viii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.
      ix. Contour bake at 130 °C for 4 minutes in oven on brick. May have to bake longer to avoid bubbling or contours in resist. Note reflow will occur.
      x. Evaporate plating membrane of Ti/Au/Ti (500/1500/500 Å).

   (b) Span Level

      i. Spin positive photoresist 1827 for 30 seconds at 3 krpm.
      ii. Softbake in oven only at 80 °C for 20 minutes.
      iii. Remove edgebead resist if desired.

iv. Align to span mask and expose for 22 seconds at 20 mW/cm$^2$.

v. Develop in MF 351:DI $H_2O$ (1:5) developer for 40-60 seconds.

vi. Rinse and dry with nitrogen ($N_2$) air gun.

vii. Descum in plasma asher for 1 minute at 80W, 250 mT in $O_2$ plasma.

viii. Dektak(Profilometer brand name) resist profile and record PR height.

ix. Etch Ti in BHF for 30 seconds.

x. Electroplate Au in cyanide-based plating solution for 2-3 $\mu$m.

(c) Sacrificial Layer Removal

i. Flood expose sample for 3 minutes at 20 mW/cm$^2$ to expose resist.

ii. Develop in MF 351:DI $H_2O$ (1:5) developer for 1 minute.

iii. Etch Ti in fresh BHF for 30 seconds.

iv. Etch gold(Au) seed layer in fresh TFA gold etchant for 40 seconds.

v. Etch Ti in fresh BHF for 30 seconds.

vi. Remove lower layer of photoresist by soaking in hot PRS2000 for 30 minutes.

vii. Rinse in DI $H_20$ for 5 minutes.

viii. Soak in Acetone for 5 minutes.

ix. Soak in IPA for 5 minutes

x. Dry with nitrogen ($N_2$) air gun.

6. Micromachining of aperture regions

(a) Etch samples in KOH for  1 hour.

(b) Remove excess oxide with BHF.

# APPENDIX D

# PRELIMINARY WORK

## D.1 Microshield Low-Pass Filters Up to 110 GHz

A new approach is presented for realizing millimeter-wave micromachined lowpass filters using lumped element with about ten times less area than comparable stepped-impedance implementation. A variety of microshield low pass filters based on a 0.075 Chebychev design utilizing MIM capacitors are fabricated and measured from 5-110 GHz, yielding excellent results [120].

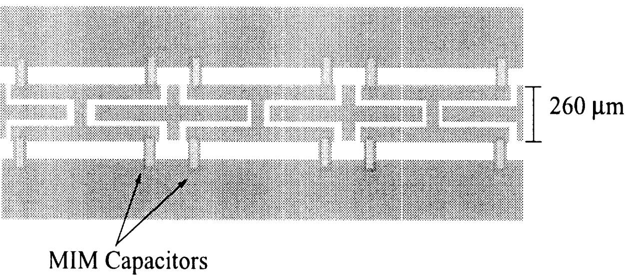



Figure D.1: Microshield low-pass filter top view.

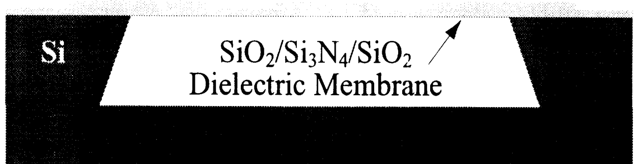



Figure D.2: Microshield low-pass filter cross-section.

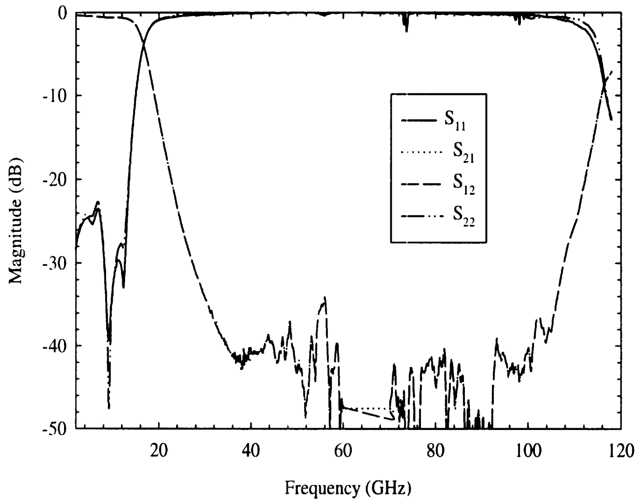



Figure D.3: S-parameters for low-pass filter measurement.

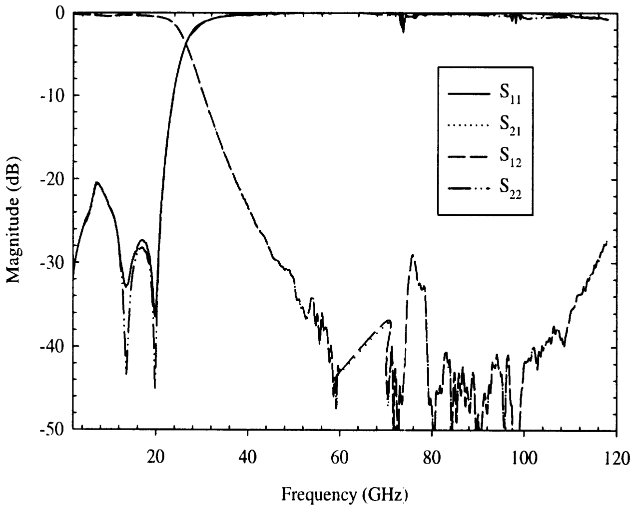



Figure D.4: S-parameters for low-pass filter measurement.

## D.2 Folded Resonators on GaAs

Compact layout is an important issue in microwave circuit design and is primarily influenced by circuit crosstalk and component size. In the case of coplanar waveguide (CPW) based stub designs, crosstalk and parasitic radiation can be minimized by using series stubs which are patterned in the center conductor, as opposed to a shunt stub configuration.

These types of stubs are useful for switches, filters, and DC and LO blocks. At low frequencies or on low permittivity substrates, however, they tend to occupy considerable amounts of spacer since they are often designed to be a quarter wavelength long. As a solution to this problem, the concept of folded series stubs has been introduced to silicon membranes. An extended study of non-folded, single-folded, and double-folded resonators is conducted on GaAs CPW lines. These results are in agreement with those initially fabricated on silicon and provide further insight into the performance of the designs [119].

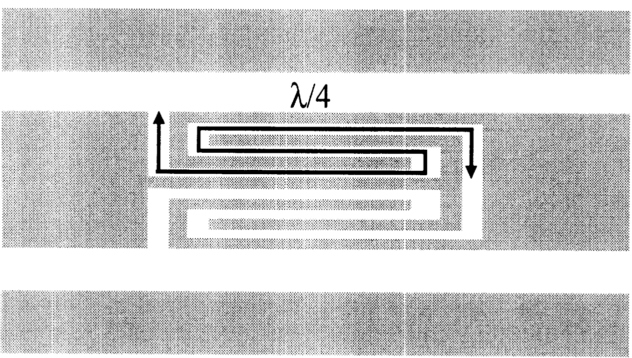



Figure D.5: Double-folded open-end series stub.

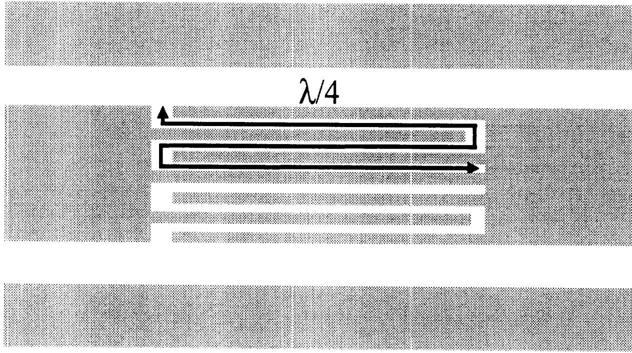



Figure D.6: Double-folded short-end series stub.

## D.3 Electro-Optic Probe System Response

Despite the success of external electro-optic (EO) probing in measuring ultrafast time-domain signals with an extremely large bandwidth, issues involving the invasiveness of the

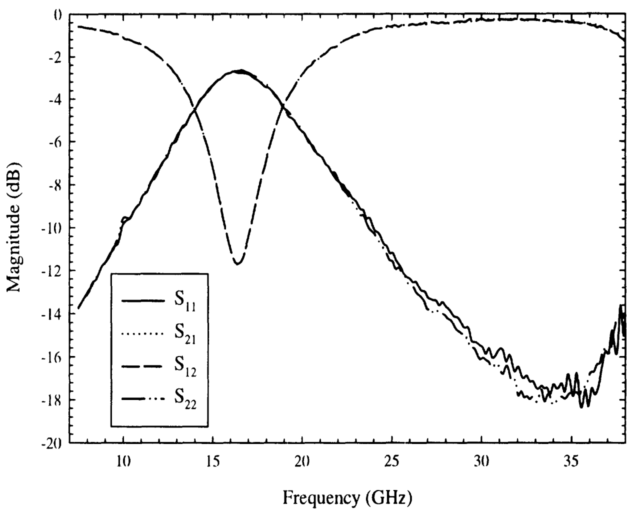



Figure D.7: Measured S-parameters for open stub.

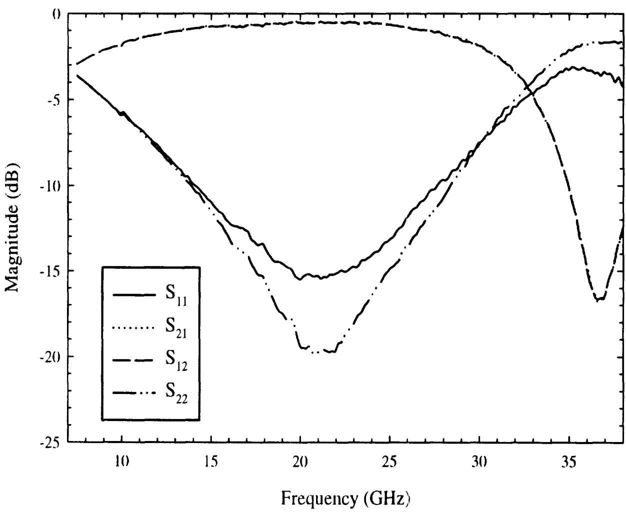



Figure D.8: Measured S-parameters for short stub.

probe, repeatability of the measured results, the ability to measure low frequencies, and the calibration of voltage signals, have served to impede the impact of EO sampling on high-speed-device and circuit testing. The main problem associated with the external probe is the high permittivity of EO materials. These materials are not only somewhat invasive, but exhibit a frequency response which is dependent on their position relative to a circuit under test.

For the first time the frequency-dependent behavior of the electric field interaction be-

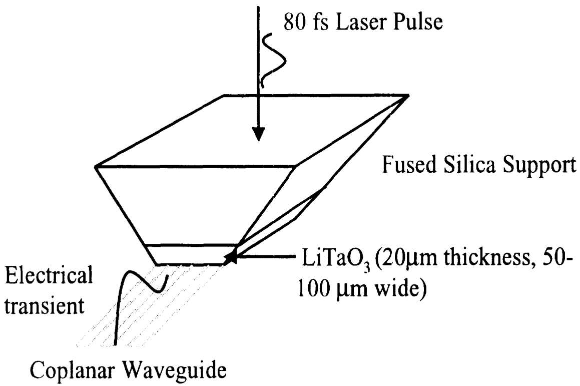



Figure D.9: Electro-optic crystal.

tween both high-and low-permittivity EO probes, and a coplanar transmission line circuit, using a finite-difference time-domain (FDTD) analysis is demonstrated. Additionally, by taking the Fourier transform of the time-domain waveforms, the coupling between the high- or low-permittivity probe and coplanar line demonstrate exclusion of frequencies below 500 GHz for the high-permittivity probe. Thus the simulations substantiate the dramatic benefit afforded by the use of the low-permittivity polymer probe [16, 17].

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