March 17, 1995

Development of Novel Planar Transmission Lines for High-Frequency Passive Circuit Component and Array Applications

Linda Katehi and Gabriel Rebeiz

Final Report

CONTRACT IDENTIFIERS

ONR Contract Number: N00014-92-J-1070

Period Covered by Report: 9/92 to 1/95

Name of Institution: University of Michigan

Scientific Personnel Partially or Fully Supported by this Contract:

Faculty	Students
Linda Katehi Gabriel Rebeiz	**Rhonda Drayton** (Supported 60% by ONR and 40% by a Minority Fellowship) **Tom Weller** (Supported 50% by ONR and 50% by a NASA Fellowship) **Steve Robertson** (Supported 30% by ONR and 70% by a NASA Fellowship)

29226-1-F = RL-2404

STUDENT PROFILES

This contract supported students part-time as indicated above. The rest of the support came through fellowships through GEM and the NASA Center of Space Terahertz Technology. A short description of this partial support and the relevance of the students work with the subject is described below:

Rhonda Drayton, expected to graduate in May 1995. She has been supported part time by this contract and the rest of her support has been provided by a minority fellowship. Specifically, she developed micromachined circuits for high-frequency applications and she fabricated and successfully measured the first micromachined circuits with an integrated package. At the present time, Rhonda is completing the development of micromachined antennas. This work will be presented in the 1995 IEEE Antennas and Propagation Symposium.

Tom Weller, expected to graduate in May 1995. He has been supported part time from this contract until March 1994 and full-time since then. The rest of his support came from the NASA Center of Space Terahertz Technology. He has developed the first membrane components which very effectively operated in frequencies up to 40 GHz. Tom's work has demonstrated the capability to effectively use membranes for the development of very efficient matching networks, filters and power dividers.

Steve Robertson, expected to graduate in Winter 1997. He has been supported part time from this contract since March 1994. The rest of his support came from the NASA Center of Space Terahertz Technology. He has developed the first membrane components which very effectively operated in W band. Steve has developed the first planar filters operating in W band with less than 1 dB insertion loss. This work will be presented in the 1995 IEEE Microwave Theory and Techniques Symposium.

HONORS and AWARDS

During the duration of this Contracts we received the following Awards and Recognitions:

- In September 1993, Prof. Rebeiz was awarded with the **Isaac Goga Gold Medal Award** by URSI, during the 24th General Assembly Meeting in Kyoto, Japan. This award is given only once every three years by URSI to the most prominent young Senior Member of IEEE.
- In May 1994, Prof. Linda Katehi at the University of Michigan has been awarded the **Humboldt Research Award** for Senior U.S. Scientists in recognition of her accomplishments in research and teaching. According to Prof. P. Russer of the Ferdinand-Braun-Inst. f. Hochstfrequenztchnik, Berlin, this is the first Humboldt Award given to a U.S. Scientist with specialization in Electromagnetic Modeling, Development and Characterization of Monolithic Circuits and Antennas.

- In June 1994, Ms. Rhonda F. Drayton received the **first prize in the student paper** competition by the IEEE Microwave Theory and Techniques Society during the **1994 International MTT-S Symposium** in San Diego, CA, for the paper co-authored with her advisor Prof. Linda Katehi "Development of Miniature Microwave Circuit Components Using Micromachining Techniques".
- In Fall 1994, Prof. Katehi became a **Fellow of IEEE**.
- In October 1994, Professor Katehi received **The University of Michigan Faculty Recognition Award**, in recognition of outstanding contributions to the intellectual environment of the University.

PATENTS

The work performed under this contract is pending for a U.S patent entitled "**Micromachined Monolithic Circuits with Integrated Packaging**". The patent application was filed in September 9, 1995 with the U.S. patent office in Washington DC.

PUBLICATIONS

PH.D DISSERTATIONS

1. Rhonda Drayton, Tom Weller and Steve Robertson have not graduated yet. The first two students are graduating in May 1995 and the third in Winter 1997. Their dissertations will become available to ONR upon their graduation.

JOURNAL PUBLICATIONS

1. N. I. Dib, R. F. Drayton, and L. P. B. Katehi, "A Theoretical and Experimental Study of Microshield Circuits", *Microwave and Optical Technology Letters*, Vol. 6, No. 6, pp. 333-339, May 1993.
2. Rhonda F. Drayton, N. I. Dib, and L. P. B. Katehi, "Design of Micromachined High Frequency Circuit Components", to be published January 1995 in *The International Journal of Microcircuits and Electronic Packaging*.
3. R. F. Drayton and L. P. B. Katehi, "Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques", submitted for publication in the *IEEE Transactions on Microwave Theory and Techniques*.
4. L. P. B. Katehi, et. al., "Micromachined Circuits for Millimeter- and Sub-millimeter-Wave Applications," *IEEE Antennas and Propagation Magazine*, Vol.35, No. 5, pp. 9-17, October 1993.
5. T.M. Weller, L.P.B. Katehi and G.M. Rebeiz, "High-Performance Microshield-Line Components," in press, *IEEE Transactions of Microwave Theory and Techniques* (expected date June 1995).
6. T.M. Weller, L.P.B. Katehi and G.M. Rebeiz, "A 250 GHz Microshield Bandpass Filter," in press, *IEEE Microwave and Guided Wave Letters.*

7. T.M. Weller, L.P.B. Katehi and G.M. Rebeiz, "Single and Double Folded-Slot Antennas on Semi-Infinite Substrates," submitted to the *IEEE Transactions on Antennas and Propagation.*

CONFERENCE PROCEEDINGS

1. L. P. B. Katehi, N. I. Dib, and R. F. Drayton, "Theoretical and Experimental Characterization of Microshield Circuits," *International Symposium on Signals, Systems, and Electronic Proceedings*, pp. 77-80, 1992.
2. R. F. Drayton and L. P. B. Katehi, "Microwave Characterization of Microshield Lines," *40th ARFTG Conference Digest*, pp. 171-176, Dec 1992.
3. R. F. Drayton and L. P. B. Katehi, "Experimental Study of Micromachined Circuits," *4th International Symposium on Space Terahertz Technology, Los Angeles*, CA, pp. 238-248, March 1993.
4. T.M. Weller, L.P.B. Katehi, G.M. Rebeiz, H.J. Cheng and J.F. Whitaker, "Fabrication and Characterization of Microshield Circuits," presented in the *1993 International Symposium on Space Terahertz Technology*, Los Angeles, California, March 1993.
5. R. F. Drayton and L. P. B. Katehi, "Study of Micromachined Quasi-Planar Lines," *1993 Antenna and Propagation/URSI Radio Science Symposium*, Ann Arbor, MI, p.30, June 1993.
6. R. F. Drayton and L. P. B. Katehi, "Micromachined Circuits for Mm-Wave Applications," *23rd European Microwave Conference*, Madrid, Spain, pp. 587-588, September 1993.
7. T.M. Weller, G.M. Rebeiz and L.P.B. Katehi, "Experimental Results on Microshield Transmission Line Circuits," presented in the *1993 International Symposium of Microwave Theory and Techniques Society*, Atlanta, Georgia, June 1993.
8. R. F. Drayton, C. Kidner, J. East, L. P. B. Katehi, "Micromachined Detector Mounts for Millimeter-wave Applications," *5th International Symposium on Space Terahertz Technology*, Ann Arbor, MI, May 1994.
9. Tom Weller, S.V. Robertson, L.P.B. Katehi and G.M. Rebeiz, "Millimeter and Submillimeter-Wave Microshield Line Components," presented in the *1994 International Terahertz Symposium*, Ann Arbor, MI.
10. R. F. Drayton and L. P. B. Katehi, "Development of Miniature Microwave Circuit Components Using Micromachining Techniques," *1994 IEEE MTT-S International Microwave Symposium*, pp. 225-228.
11. R. F. Drayton, T. M. Weller, and L. P. B. Katehi, "Development and Characterization of Miniaturized Circuits for High Frequency Applications Using Micromachining Techniques," presented at the *1994 The International Society for Hybrid Microelectronics Symposium.*
12. R. F. Drayton and L. P. B. Katehi, "Micromachined Conformal Packages for Microwave and Millimeter Wave Applications," to be presented at *1995 IEEE MTT-S International Microwave Symposium.*

13. R. F. Drayton and L. P. B. Katehi, "Microstrip Patch Antennas on Micromachined Low-Index Materials," submitted to the *1995 Antennas and Propagation Society International Symposium.*

14. Steve V. Robertson, Linda P.B. Katehi and Gabriel M. Rebeiz, "Micromachined Self-Packaged w-Band Bandpass Filters," accepted for presentation in the *1995 International Symposium of the IEEE Microwave Theory and Techniques Society*, Orlando, FL, May 1995.

15. I. Papapolymerou, Rhonda F. Drayton and Linda P.B. katehi, "Surface Wave Mode Reduction for Rectangular Microstrip Antennas," submitted for presentation in the *1995 International Symposium of Antennas and Propagation Society*, Seattle, WA, June 1995.

A BRIEF ANALYSIS OF THE RESEARCH FINDINGS

The work performed under this contact has resulted in what we consider to be major breakthroughs in planar technology. For the first time, it was demonstrated successfully that silicon micromachining can be used for a variety of high-frequency applications including packaging and high-performance interconnects. The success of our work can be summarized in the following:

- The work performed under this contract has resulted in **8 Journal publications** and **15 publications in Symposia proceedings**. Copies of these papers are attached in Appendices B and C respectively.
- The work has been submitted for a **U.S. patent** successfully and is pending decision.
- For her work under this contract, Rhonda Drayton received the **best paper award** in the Student Paper Competition during the 1994 IEEE Microwave Theory and Techniques Symposium (see attachment in Appendix A).
- All of the three students supported by this contract have been listed in the 1994 Technical Program Chairman's **Honor Roll** (see Appendix A).
- The work performed by this contract has attracted the interest of small companies which plan to commercialize some of our components.
- The work has also attracted the interest of **MA/COM** and **Martin Marietta** which plan to use some of our packaging ideas on their own planar circuits.

This contract allowed us to perform very innovative and original work which, we feel, will become a landmark in the years to come.

APPENDIX A

1994 IMS Technical Program Presentation Recognitions

Bob Eisenhart

At this year's Symposium there were two types of presentation competition. The first was the Student Paper Competition which followed an established format. This was judged by a select panel on all aspects of each presentation at a separate session on Tuesday evening. Each participant was then given a complimentary invitation to the Awards Banquet on Wednesday. The 1st, 2nd, and 3rd place winners were, respectively, Rhonda Drayton, University of Michigan; Steven Gearhart, University of Michigan and Peter Liao, University of California at Santa Barbara. They received their prizes at the Awards Banquet.

A second, and new competition this year, resulted in a "Technical Program Chairman's Honor Roll." This focused entirely on the *quality* of the *presentation* rather than the technical content and recognition was not limited to one or two speakers per session. All presenters were notified of the procedure and rating criteria, hopefully motivating them to put in that little extra effort. It is felt that this was very successful since there were many comments by registrants who specifically pointed out that the overall level of presentation was greatly improved over past years. This high quality was also evident in the rating scores received. In a rating system of 0 to 20 where 12 was defined as an average presentation, the average *rating* received was 14. The threshold for placement on the Honor Roll was for all scores greater or equal to 14, and resulted in the 165 presenters shown on the accompanying listing. These presenters have also received a Certificate of Recognition. When duplicate speakers and papers not receiving scores are removed, this represents more than 50% of the rated papers.

Aside from the Presentation Recognition, *all* presenters of contributed papers received a Symposium Medallion in appreciation for their part in the Symposium.

Thanks again to all involved in the Technical Program, and particularly those on the Technical Program Committee who took the time to provide reviews of the presentations. The results easily justified our efforts.

1994 IMS Technical Program Chairman's HONOR ROLL

F. Alessandri
R. Anholt
D. Antsos
M. A. Aust
J. W. Bandler
A. Bangert
M. Becker
E. M. Biebl
H. Blánck
C. Bohm
J. Bornemann
W. Boulais
S. Bouthillette
C. R. Boyd
R. L. Brown
T. Brukiema
S. C. Bundy
J. Burns
K. Chang
C. H. Chen
C. Y. Chi
Y. Cho
E. D. Cohen
M. Cohn
C. E. Collins
A. Constanzo
L. D'Evelyn
A. S. Daryoush
J. Detlefson
N. Dib
J. DiLorenzo
G. F. Dionne
R. F. Drayton
H. Eisele
M. Engles
R. Faraji-Dana
L. M. Felton
A. Ferrero
H. R. Fetterman
J. Frank
A. Galli
S. S. Gearhart
J. Goel
M. A. Gouker
R. Goyal
P. A. Grobelny
R. Hajji
P. Halloran
R. Heidemann
W. Heinrich
D. Heston
H. Heuermann
B. Hewitt
S. Hofschen
P. K. Ikalainen
T. Ishizaki
T. Ivanov
P. Jukkala
U. Karacaoglu
R. Kaunisto
T. Kawai
J. S. Kenney
K. W. Kobayashi
R. Kolc
B. Kraemer
M. Kubo
S. Lardizabal
J. Laskar
B. Lax
J. G. Leckey
L. Lefrancois
J. Lester
J. Y. Liang
U. Lott
J. F. Luy
M. R. Lyons
S. Maas
J. A. MacDonald
R. R. Mansour
M. J. Marcus
H. Matsumoto
S. R. Mazunder
R. McGowan
D. McQuiddy
I. Mehdi
W. Menzel
W. Mertin
J. E. Miller
K. Minot
S. Molenkonf
M. Mongiardo
A. Morini
L. Mullen
T. Nakagawa
S. Nakajima
M. Nakhia
T. D. Ni
T. N. Nielsen
H. Okazaki
G. Olbrich
P. Onno
J. Owens
D. Parker
S. T. Peng
A. Plattner
M. Pospieszalski
N. M. Pothecary
S. J. Prasad
S. Pritchett
M. M. Radmanesh
A. V. Raisanen
C. Rauscher
V. S. Reinhardt
A. C. Reyes
M. Righi
M. Rittweger
S. V. Robertson
P. Russer
K. Sabetfakhri
H. Sakai
B. C. Schmukler
J. S. H. Schumacher
R. Schwindt
F. Sechi
A. K. Sharma
H. Shigesawa
C. G. Shih
T. Shimura
R. N. Simons
C. Sinclair
P. M. Smith
P. M. So
F. Sterzer
M. L. Stevens
P. A. Stimson
G. Strauss
W. Struble
D. G. Swanson
S. Talisa
D. Teeter
J. C. Tippet
T. Tokumitsu
M. C. Tsai
H. S. Tsai
R. Vahldieck
T. Van den Broeck
F. Vergeyst
M. P. Versleijen
E. Vourch
H. Wang
M. R. Webb
C. J. Wei
R. Weigel
T. M. Weller
D. A. Willems
J. T. Williams
R. M. Wohlert
I. Wolff
E. Yamashita
H. W. Yao
S. Ye
M. Yousefi
A. H. Zaabab

Vol M

APPENDIX B

STUDY OF MICROSHIELD CIRCUITS

Nihad I. Dib, Rhonda F. Drayton, and Linda P. B. Katehi
[illegible]

KEY TERMS

Monolithic transmission line, planar discontinuities, integral equation, coplanar waveguide, radiation loss

ABSTRACT

A theoretical and experimental study of a new type of monolithic planar transmission line is presented. This line can operate without the need for via holes or the use of air bridges for ground equalization. Furthermore, it has shown the tendency to radiate less than the conventional coplanar waveguide (CPW) and can provide a wide range of impedances due to the many available parameters for design. The space-domain integral equation method is used to analyze several discontinuities of the proposed line. In order to validate the theory, measurements are performed on scaled models of a specific discontinuity. The experimental and theoretical results are in good agreement. In addition, it is demonstrated that the proposed line discontinuities radiate considerably less than the corresponding coplanar waveguide ones. © *1993 John Wiley & Sons, Inc.*

1. INTRODUCTION

The first planar transmission line, the stripline, was introduced almost 40 years ago and created the basis of a new and revolutionary hybrid technology. Since then, hybrid technology has evolved to monolithic technology, drastically increasing operating frequencies and consequently reducing weight and volume. In conventional planar transmission lines the power is propagating by creating an rf voltage difference between two planar conductors printed on the same (coplanar waveguides, coplanar strips) or opposite surfaces (stripline, microstrip, coupled strips) of a dielectric slab structure. In most cases, the geometry of the conventional lines permitted great design flexibility, tremendous reduction of the space occupied by the circuit, and realization of very large scale, very high frequency applications.

The planarization of the conductors in the above transmission lines provided the capability of integration, which led to unwanted mechanisms such as radiation and dispersion resulting in enhanced ohmic losses and electromagnetic coupling. These mechanisms are frequency dependent and impose serious limitations as we approach the submillimeter-frequency range. The ability to find new geometries [1–9] which reduce or eliminate the above loss or coupling mechanisms without affecting the monolithic character of the line will extend the operating frequencies long into the terahertz region and will improve circuit performance in existing applications.

As a common practice, elimination of radiation losses and reduction of electromagnetic coupling has been achieved by enclosing the planar circuits in shielding cavities. In most cases, the cavities have to be placed away from the circuit to avoid proximity effects, thus introducing cavity resonances which interfere with the electrical performance of the circuits. While shielding is possible in many circuit applications, in monolithic arrays where the environment has to remain open, radiation from the feeding structure and parasitic coupling to the radiating elements have been major issues.

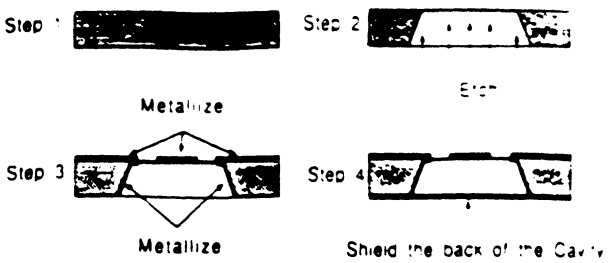

Figure 1 Fabrication process for the microshield line

This article presents a theoretical and experimental study of the *microshield line* (Figure 1), a new type of monolithic line appropriate for circuit and array applications [10]. This geometry may be considered as an evolution of the conventional microstrip line or coplanar waveguide and is characterized by low radiation loss, reduced electromagnetic interference and compatibility to antennas of microstrip or aperture type. In addition, the microshield geometry can create the basis of a new technology and can lead to novel ideas in antenna and array design [11]. In this new line, the ground plane has been deformed from its original planar form to totally or partially surround the inner strip conductor as a shielding microcavity. Such a structure can be made monolithically using etching and metal deposition techniques. Furthermore, the inner conductor can be suspended in air by using membrane technology [12]. This eliminates dielectric losses which could be high at millimeter-wave frequencies. Membranes have been effectively employed to provide high-efficiency monolithic antennas and arrays operating at frequencies as high as 2.5 THz [13].

One of the advantages of the microshield line, in comparison with the more conventional ones such as the microstrip or the coplanar waveguide, is the ability to operate without the need for via holes or the use of air bridges for ground equalization. Furthermore, due to the many available parameters in design, a wide range of impedances may be achieved. Specifically, by varying the size of the shielding microcavity (see Figure 1) the per-unit length capacitance of the line can increase or decrease from the value of the corresponding microstrip or coplanar waveguide resulting in lower or higher values of the characteristic impedance. One loss mechanism still found in this novel structure is conductor loss. Due to the geometry of the ground plane, conductor loss is expected to be slightly higher than microstrip and lower than conventional CPW. The presence of conductor losses limits the use of microshield lines and circuits to the lower end of the submillimeter-wave spectrum (up to 500 GHz).

In this article the process for the fabrication of the microshield line is described in Section 2, and its feasibility is demonstrated by building a microshield line low-pass filter feeding an aperture-type antenna. To provide an indication of the tendency of the microshield line to radiate less, several three-dimensional discontinuities are analyzed and their response is compared to the same discontinuity geometries in conventional coplanar waveguide form. In all cases, the microshield discontinuities show much lower radiation than the conventional CPW ones. The theoretical approach used to analyze these discontinuities is presented briefly in Section 3 and numerical results are given in Section 5. In addition, the characteristic impedance of the line is evaluated using FFM analysis. Moreover, measurements on scaled models (Section 4)

2. FABRICATION

The fabrication of microshield circuits is dependent on the thin dielectric membrane technology and the anisotropic etching of the supporting wafers. A Si membrane is a three-layer SiO_2–Si_3N_4–SiO_2 structure which must be slightly in tension to yield flat and rigid self-supporting characteristics. The SiO_2 layers are made by high-temperature thermal oxidation (1100°) while the Si_3N_4 layer is made by chemical vapor deposition at 800° [12]. After the development of the three-layer structure, the membranes are fabricated in two steps. First, an opening in the silicon-nitride layers is defined on the back of the wafer, and then the silicon is etched until a transparent membrane appears. The etching solution is anisotropic and yields pyramidal cavities which can be exploited for the development of microshield transmission lines. Figure 1 gives the most important steps of the procedure in a simplified way. Once the membranes are fabricated, it is easy to lithographically define several different microshield geometries for impedance and propagation constant measurements.

Figure 2 shows a picture of a low-pass microshield filter exciting an aperture-type antenna. The eight-section filter consists of alternating 50-Ω and 125-Ω microshield sections and has Chebyshev low-pass characteristics with 0.5-dB passband ripple and a cutoff frequency of 76 GHz. The filter also performs an impedance transformation from 100 Ω at the input to 50 Ω at the output. This circuit has been made as a proof of fabrication feasibility and it does not present an optimized design. In fact, in order to successfully design this antenna configuration many important issues associated with the microshield geometry have to be studied and understood. Some of these issues are (i) parasitic radiation, (ii) transitions from conventional planar lines to microshield structures, and (iii) electromagnetic coupling to neighboring circuit elements.

3. THEORY

The theoretical method used to analyze microshield line discontinuities is based on a space-domain integral equation (SDIE) which is solved using the method of moments. The SDIE approach has been previously applied to study several microstrip and coplanar waveguide (CPW) discontinuities and

Figure 2 A microshield line low-pass filter

terms of the geometries it can solve [13]. The boundary problem is split into two simpler ones by an equivalent magnetic current $\overline{M}$ on the slot apertures. The surface magnetic current radiates an electromagnetic field in the two regions above and below the slots. Continuity of the tangential electric field in the slots is satisfied. The remaining boundary condition applied is the continuity of the tangential magnetic field on the surface of the slot apertures, which leads to the following integral equation

$$0 = \int_{S_s} \int [\overline{G}_A(\mathbf{r}, \mathbf{r}') - \overline{G}_B(\mathbf{r}, \mathbf{r}')] \cdot \overline{M}(\mathbf{r}') \, ds' \qquad (1)$$

where $\overline{G}_{A,B}$ are the magnetic field dyadic Green's functions for the regions above and below the slots, respectively, and $\overline{M}$ is an assumed ideal current source feeding the microshield slot [14]. The free-space Green's function is expressed in the form of Sommerfeld integrals in space domain [15, 16], while Green's function in the shielding microcavity consists of double summations over the waveguide's eigenvalues [14]. Since the cavity dimensions are very small, higher-order microshield modes are not excited in the frequency range of interest.

The integral equation (1) is solved using the method of moments where the unknown magnetic current is expanded in terms of rooftop basis functions. Then Galerkin's method is applied to reduce the above equation to a linear system of equations:

$$\begin{pmatrix} Y_{yy} & Y_{yz} \\ Y_{zy} & Y_{zz} \end{pmatrix} \begin{pmatrix} V_y \\ V_z \end{pmatrix} = \begin{pmatrix} I_y \\ I_z \end{pmatrix}. \qquad (2)$$

where Y_{ij} ($i = y, z$; $j = y, z$) represent blocks of the admittance matrix, V_i is the vector of unknown y and z magnetic current amplitudes, and I_i is the excitation vector which is identically zero everywhere except at the position of the delta sources. Finally, the equivalent magnetic current distribution and consequently the electric field in the slots are obtained by matrix inversion. Away from the discontinuity, the electric fields form standing waves of the fundamental propagating mode. Using the derived electric field, an ideal transmission line method is applied to determine the scattering parameters of the discontinuity. From the scattering parameters, radiation loss can be evaluated as a function of the frequency and other geometrical parameters.

4. SCALED MODEL MEASUREMENTS

Experimental characterization of circuits requires accurate measurement of the scattering parameters, the effective dielectric constant, and radiation and conductor losses. Since two-port scattering parameter measurements are limited to 100 GHz from state-of-the-art vector systems, experimental characterization of the microshield line can be best performed on scaled models even if the structure itself is intended for submillimeter-wave applications. Due to the passive nature of the microshield, most of the information obtained from the scattering parameter measurements, excluding conductor losses, can be scaled with frequency to the submillimeter-wave region.

The rf measurements were performed in the 10–18-GHz frequency range on the HP 8510B automatic network

the membrane of the microshield line has been replaced by a 0.76-mm duroid layer ($\epsilon_r = 2.2$). In this configuration, the strip conductor is printed on this duroid layer and is shielded by a cavity milled on a metal block (see Figure 3). To determine the circuit performance, a one-tier through-reflect-line (TRL) calibration has been performed to eliminate the effects of the connector discontinuity from the measured data. The TRL deembedding required the fabrication and measurement of a through, an open, and two delay lines as calibration standards. Once calibrated, the *S*-parameter measurements

formance of the dielectric microstrip

5. RESULTS AND DISCUSSION

As mentioned earlier, several microstrip

treated in this article, namely

ends and two coupled open ends. Even

discontinuities which radiate more, a study of the above

ometries can give a very good indication of the radiation characteristics of the proposed structure. First, in order to

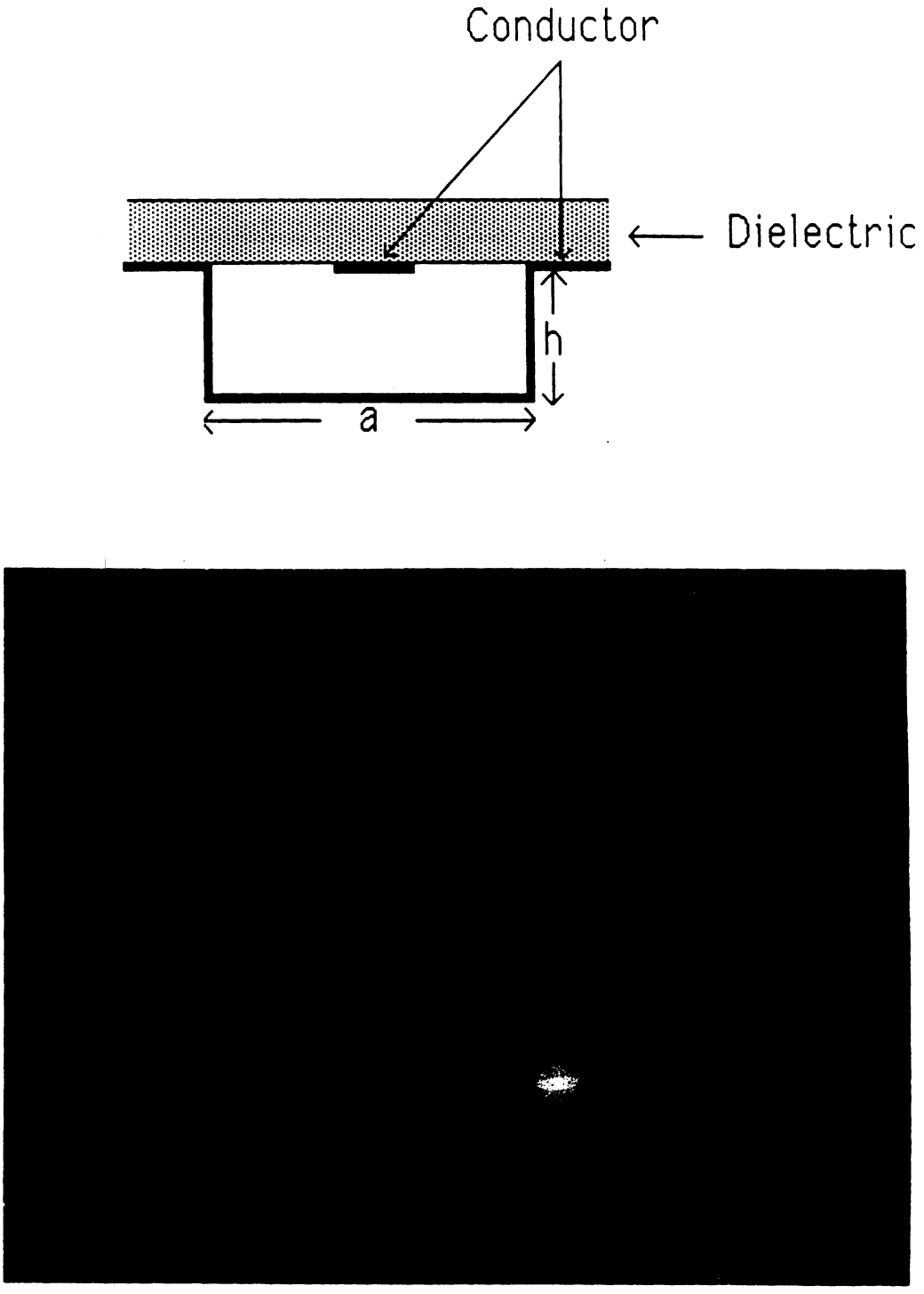

Figure 3 (a) A cross-sectional view of the dielectric microshield line. (b) Photograph of the parts of the dielectric used in scaled model measurements

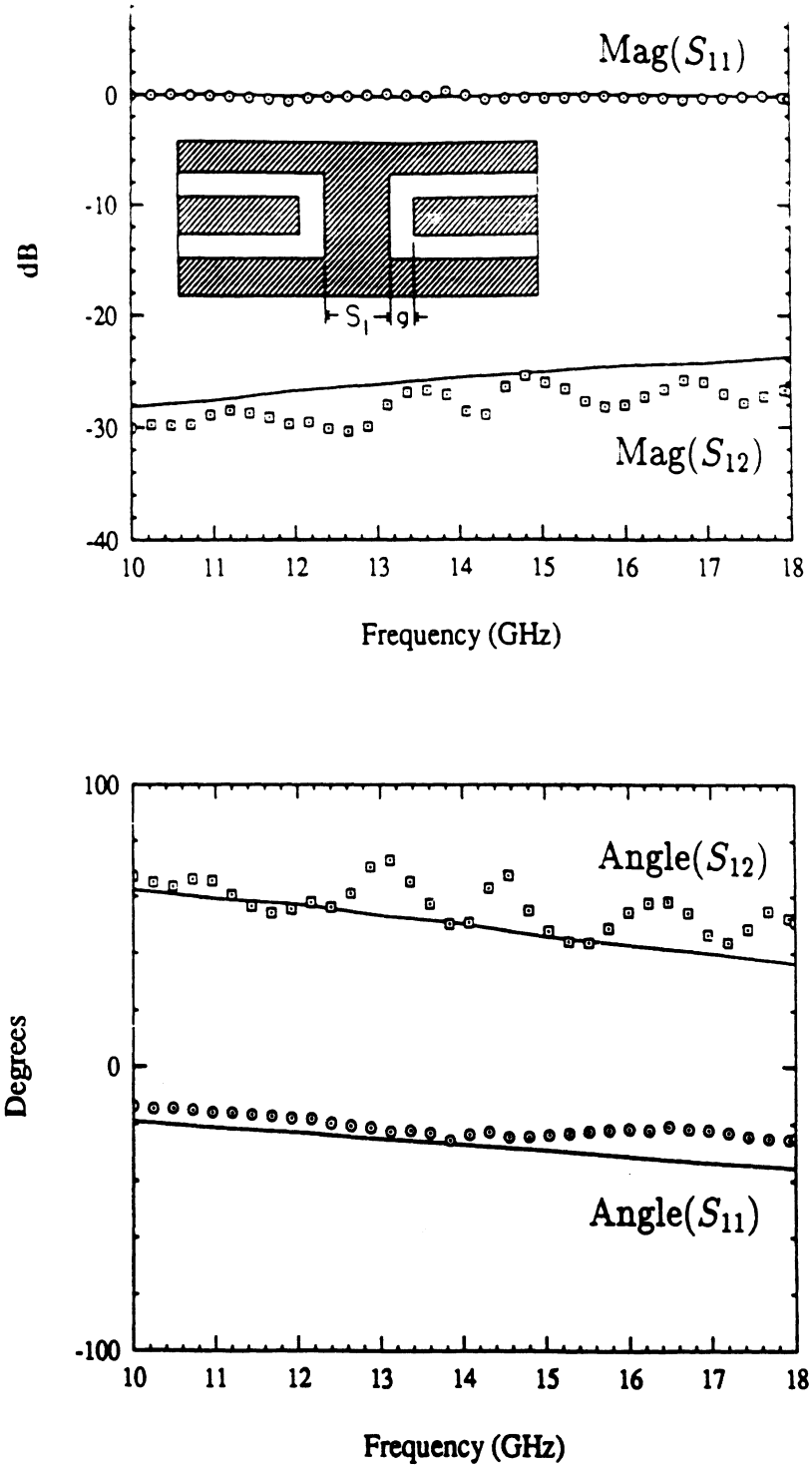

Figure 4 Scattering parameters (magnitude and phase) of a two open-end coupled dielectric microshield line discontinuity (S = g = 0.5 mm). Solid lines: theory, dots: experiment

validate the numerical method, scaled measurements were performed on the two coupled open-ends discontinuity. In this experiment, the microshield line has an inner conductor width of 1.5 mm, a slot width of 0.5 mm, and a microcavity width and height of 2.5 and 1.27 mm, respectively. Figure 4 shows the scattering parameters (magnitude and phase) as were evaluated theoretically and measured experimentally. The ripple seen in the measured data is mainly due to the very small coupling between the two lines, which intensifies the effect of connector repeatability.

In the numerical results shown in Figures 5–7, the m shield lines and the conventional coplanar waveguides an inner conductor width of 0.5 mm and slot widths of mm. The substrate used in the dielectric microshield ar the coplanar waveguide is 0.635 mm thick and has a diele constant ϵ_r = 2.1. The microcavity size [height (h) and w (a)] is specified in the figure captions. It is expected reducing the cavity size up to the point where the side touch the slot edges will improve field confinement. This ity size does not present an optimum design, and the re

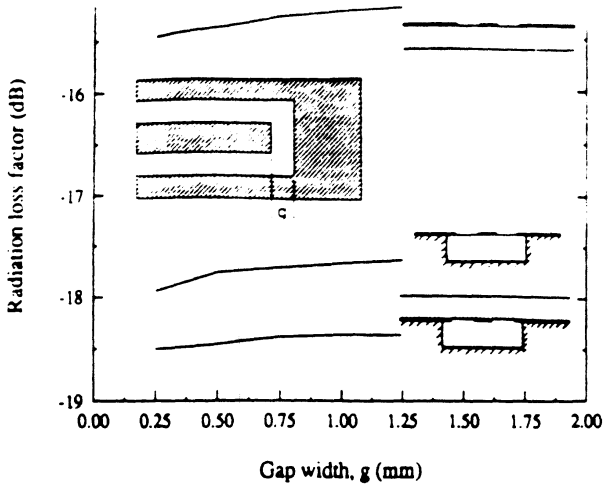

Figure 5 Radiation loss factor of an open-end line (h = 3 mm, a = 3 mm, f = 24 GHz)

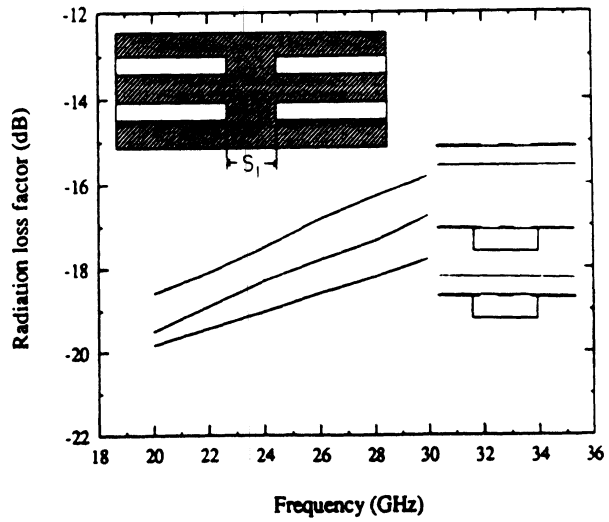

Figure 6 Radiation loss factor of two coupled short ends (h = 3 mm, a = 3 mm, S_1 = 0.25 mm)

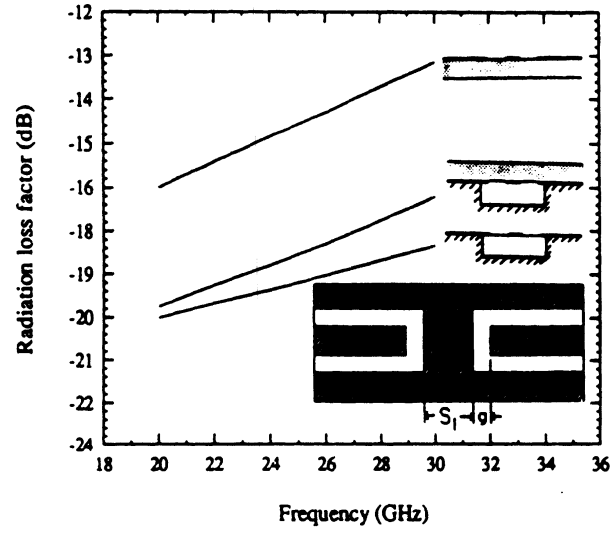

Figure 7 Radiation loss factor of two coupled open ends (h = 0.25 mm, a = 1 mm, S_1 = 0.5 mm, g = 0.25 mm)

electrical performance of the microshield [illegible] dimensions were merely used as examples to demonstrate capability of the proposed microshield line discontinuities radiate considerably less than the corresponding waveguide ones.

- **Open end.** Figure 5 shows the radiation loss factor, $10 \log(1 - |S_{11}|^2)$, of an open end as a function of gap width for the proposed microshield line and is compared to the coplanar waveguide open end. As can be noticed, the dielectric microshield open end has the lowest radiation loss, which is approximately half of that encountered in the conventional CPW open end. Low radiation results from good field confinement in the slots, which is due to the presence of the dielectric substrate and the shielding cavity.
- **Coupled Short Ends.** Figure 6 shows the loss factor, $10 \log(1 - |S_{11}|^2 - |S_{12}|^2)$, for two coupled shorted ends as a function of frequency. Again, the dielectric microshield has smaller radiation loss factor than the membrane microshield and the conventional CPW. Despite these differences, in all cases, the radiation loss is very small due to the type of the planar discontinuity.
- **Coupled Open Ends.** Figure 7 shows the loss factor for this discontinuity as a function of frequency. Here the cavity size is chosen such that the side walls touch the slot edges and with height equal to one slot width. It can be seen that radiation in the coupled microshield open ends is approximately one-third the radiation from coupled open ends made of conventional CPW. In addition, it can be seen that the dielectric microshield coupled open ends radiate more than the membrane microshield in contrast to the coupled short-end discontinuity (Figure 6). This may be due to the excitation of the surface waves from the open ends along the direction of propagation in the dielectric microshield line.

As mentioned earlier, in addition to low radiation, the microshield line has one more major advantage: the ability to achieve a wide range of impedances by appropriately varying the geometry of the line and the size of its microcavity. This range spans over the impedance ranges of the conventional microstrip line and coplanar waveguide. Figure 8 gives the characteristic impedance of a microshield line as a function of $S/(S + 2W)$ for a given cavity size, where S is the center conductor width and W is the slot width. The characteristic impedance has been obtained using a TEM analysis [18, 19]. This impedance should be the exact one as long as no higher-order modes are excited. It can be seen that as $S/(S + 2W)$ gets smaller, Z_0 approaches that of a microstrip line.

6. CONCLUSIONS

A new type of monolithic planar transmission line, the microshield line, has been proposed. This line has the following advantages:

- There is no need for via holes or air bridges for ground equalization.
- A wide range of impedances can be obtained.
- Wavelength is equal to the free-space wavelength which results in larger circuit dimensions.
- Radiates much less than the conventional CPW.

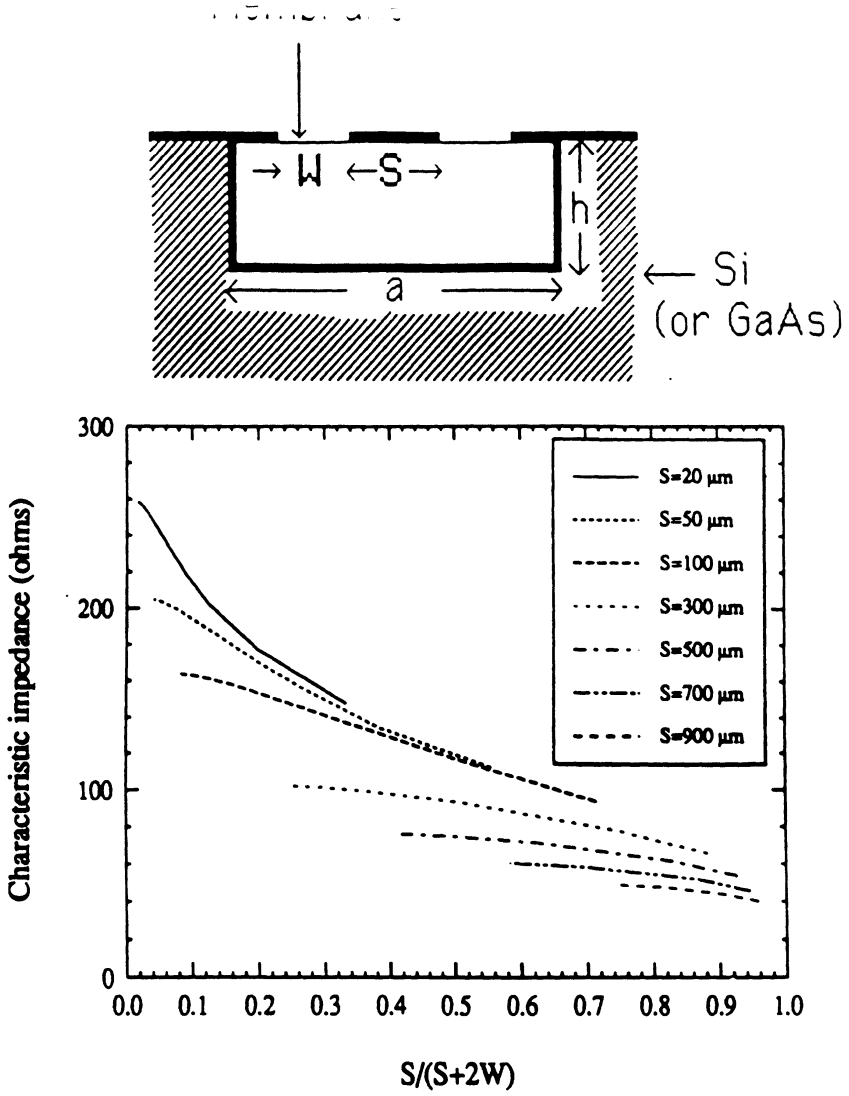

Figure 8 Characteristic impedance of a microshield line (a = 1.2 mm, h = 0.2 mm)

The loss factor of several discontinuities has been evaluated and compared with similar discontinuities in conventional CPW. It has been found that the microshield line has lower radiation which is approximately half of that encountered in the conventional CPW. Preliminary experiments on scaled models have been performed where good agreement with theoretical results has been obtained. In addition, it has been shown that the microshield line has the ability to achieve a wide range of characteristic impedances.

ACKNOWLEDGMENTS

This work has been supported by the Office of Naval Research under Contract No. N00014-92-J-1070, the NASA Center for Space Terahertz Technology, and NSF under Contract No. ECS 8657951. The authors would like to thank Dr. W. Harokopus for supplying computer programs and Professor G. Rebeiz and his group for their scientific support.

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Design of Micromachined High Frequency Circuit Components

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ABSTRACT

This paper describes the development of high frequency micromachined circuit components with emphasis on the design and fabrication steps. These passive components have been fabricated using silicon micromachining processes which allow for the development of high-frequency circuits that have a monolithically integrated package. Some advantages of such configurations include reduction in the overall size and weight, improved isolation between neighboring circuits, minimized parasitic radiation effects, as well as increased circuit density due to the individual shielding of circuit geometries. Presented are circuit design and fabrication issues with extensive discussions of the implemented design procedure and of the adopted micromachining processes. Success of the circuit development is verified by comparison of on-wafer measurements to modeled results in the 10-40 GHz range.

I. INTRODUCTION

Planar transmission lines such as microstrip, stripline, and coplanar waveguide (CPW) have become conventional structures to use in the design of microwave and millimeter wave circuits due to the flexibility provided in fabricating passive components with predefined electrical functions as well as the enhanced ease in mounting active devices. Although microstrip and stripline have been utilized the most in passive circuits, limitations in mounting active devices have made the use of coplanar waveguide more popular since its physical geometry provides inherit advantages. A commonly observed problem in many of these lines, however, is degradation in circuit performance that results when coupling mechanisms associated with parasitics are excited along with radiation effects that arise in dense circuit environments. In order to address the above concerns, the development of a

transmission line geometry that offers electrical performance comparable to conventional ones, maintains ease in device mounting and reduces undesirable coupling effects is required. This can be attained with independent shielding of specific circuit components that can be achieved using micromachining techniques.

Since most high frequency circuit applications address development, modeling, fabrication and experimental characterization of systems prior to packaging, the effect of the housing on the electrical performance is very difficult to predict. As a result, the electrical response of many packaged circuits suffers significant performance degradation, mainly attributed to the introduction of unwanted parasitics along with the excitation of multiple shielding resonances resulting from the interaction between the circuit board and metallic housing. To address the issue of proximity coupling and cavity resonances, monolithically integrated cavities can be developed which provide effective shielding to individual components while maintaining an overall geometry that is small enough to avoid the multiple resonance excitation in the range of operating frequencies. From a cost perspective, since conventional housing elements can be rather expensive and impractical to optimize for each generic circuit board, a solution toward cost minimization is easily achieved by using micromachining techniques. Consequently, for system level designs where weight and volume reduction as well as controllable parasitics are critical issues, overall system costs are directly reduced using these techniques. Industries related to satellite and mobile communications can benefit greatly from the technological development of miniature micromachined microwave components.

Although well-established in sensor applications, silicon micromachining is currently being investigated for the development of miniature circuit components used for high frequency systems. A completely shielded micromachined circuit can be excited by a planar transmission line of coplanar type that is surrounded by an air-filled cavity in the upper region and a substrate-filled one beneath the line as shown in Figure 1. To address the specific design issues of shielding and isolation, a variety of micromachining processes have been explored and studied to identify approaches which provide circuits with the best electrical performance at these frequencies. Demonstration of the concept of micromachined circuits for RF applications is given through simple circuit components such as a tuning stub and lowpass filter. These simple components have been developed and their performance has

been measured and compared to conventional transmission lines [1], in this case coplanar waveguide. More specifically, this paper presents the development of micromachined miniature circuit components for high frequency applications in two sections. The first section, *design approach for micromachined circuits*, provides a general overview of the approach required to develop the circuits along with a brief summary of the theoretical models used. It also extensively discusses the fabrication procedure developed and implemented through this effort. The second section, *experimental validation and discussion*, describes the measurement considerations needed for circuit characterization and discusses the results obtained both experimentally and theoretically for various circuit components.

II. DESIGN APPROACH FOR MICROMACHINED CIRCUITS

High frequency micromachined circuits are developed in two phases: (a) design and analysis and (b) fabrication and measurement. In the *design and analysis* phase, determination of an appropriate commercially available CAD tool is a critical issue to address. Theoretically, while full-wave techniques offer the most accurate model prediction, they are inappropriate to use as design tools due to their complexity and computer time intensive requirements. Consequently, initial circuit design is best achieved using simpler quasi-static models that are based on TEM or quasi-TEM approximations. After an entry level circuit design has been completed, the specific circuit geometry is determined and analyzed using full-wave analysis techniques to verify performance. Since these models require specification of the exact geometry, the modeled circuit provides a highly accurate prediction of the response. From this point, performance improvements can be subsequently obtained using an iterative method to fine tune the circuit dimensions for given design requirements. After an optimum design has been determined, fabrication is implemented using the procedures presented in section II-C below, and circuits are then tested to evaluate the overall circuit performance.

A. Design Procedure

To illustrate the procedures needed for realistic circuit development, a flow chart is presented in Figure 2. Using quasi-static or semi-empirical CAD tools, the basic circuit is designed electrically to meet the desired specifications. Once the appropriate response is obtained, the circuit geometry is determined and an analysis is performed using full-wave techniques such as the finite-difference time

domain (FDTD) method. During the analysis phase, the circuit response is evaluated and iterative changes are made to the geometry to improve the response. The final design of the micromachined circuit is then fabricated whereafter the response is measured using the experimental set-up described in section III-A. Having both theoretical and experimental results, comparisons are made to validate the circuit response. If the electrical response is within an acceptable performance margin, the procedure is complete; however, if the response is unacceptable, design objectives must then be reconsidered. In the case of high performance applications, discrepancies between theory and experiment mainly arise from fabrication tolerances. When design errors must be minimized, two options exist. The first option involves modifying the steps of the fabrication procedure that reduce the geometrical deviations between the theoretically modeled and the measured circuit. In instances where prototype cost is a critical issue, the second option involves modifying the electrical designs to make them less sensitive to fabrication tolerances while preserving desired electrical performance.

B. Theoretical Models Utilized

In the above design procedure, several comments can be made regarding the theoretical techniques implemented for the modeling of micromachined circuits. The characteristic impedance for basic transmission line structures such as the completely shielded feed line, used herein, has been computed using quasi-static models [2], while dispersion characteristics have been evaluated using the spectral domain technique [3]. This development is required in order to design appropriate feeding lines required for specific calibration procedures that operate in the 10 - 40 GHz range. Once the electrical behavior of the transmission lines is characterized, simple circuits are developed and modeled using a quasi-static software tool (PUFF [4]). This tool uses simple ideal transmission line theory and allows for easy design as a first iteration to the whole procedure. For more complicated circuit geometries, however, quasi-static models are inadequate and the use of full-wave analysis techniques is required. Upon completion of the design, analysis for verification is performed using full-wave models such as the finite difference time domain (FDTD) technique [5] since the fabricated geometries require versatility in modeling the exact shapes and dimensions of the realized planar lines and cavities (see Figure 1).

The finite difference time domain technique offers flexibility since an arbitrary geometry can be evaluated primarily by discretization. In this method, Maxwell's curl equations are expressed in discretized space and time domains and, then, are used to simulate the propagation of the initial excitation in the "leapfrog" manner [5]. To characterize any planar discontinuity, propagation of a specific time-dependent function through the structure is simulated using the FDTD technique. The time dependence of the excitation can be chosen arbitrarily; however, a Gaussian pulse is often used because it varies smoothly in time and its Fourier transform is also a Gaussian function centered at zero frequency. Following the time and space discretizations of the electric and magnetic field components, the FDTD equivalents of Maxwell's equations are then used to update the spatial distributions of these components at alternating half time steps [5]. The space steps, Δx, Δy, and Δz are carefully chosen such that integral numbers of them can approximate the various dimensions of the structure. As a rule of thumb and in order to reduce the truncation and grid dispersion errors, the maximum step size is chosen to be less than 1/20 of the smallest wavelength, which corresponds to the highest frequency represented in the pulse, existing in the computational domain. The Courant stability criterion is then used to select the time step to insure numerical stability.

In this paper, the electric conductors are assumed to be perfectly conducting with zero thickness and are treated by setting the tangential electric field components to zero at all time steps. For the electric field components lying on the dielectric-dielectric interface, the average of the two permittivities is used in the FDTD equations. To terminate the FDTD lattice at the front and back planes, the super-absorbing, first-order Mur boundary condition [6-8] is utilized to simulate infinite lines. The interested reader may consult [5,9,10] for a detailed description of the FDTD method.

Compared to other methods, the FDTD method is relatively easy to implement for complicated geometries. It requires only simple arithmetic operations in the solution process and also has the advantage of being flexible for time and frequency domain analyses. Frequency characteristics can subsequently be obtained by applying the Fourier transform on the time response of the discontinuity. The response in a wide frequency range starting from dc can be obtained by only one pulse simulation in contrast to frequency domain techniques which provide the response at a specific frequency and are hard to apply at very low frequencies due to long feeding line requirement.

C. Fabrication Procedures

The circuits mentioned above are a two silicon wafer system with <100> crystal orientation and rely primarily on micromachining of silicon. For high frequency circuit applications the fabrication processes are relatively new although they are fairly standard in microstructures. To understand micromachining technology for high frequency circuits, this section presents the fabrication as it applies to monolithically shielded geometries.

The micromachined circuits presented have a shielding environment that has been monolithically integrated into a two-wafer system and is made of cavities in both upper and lower regions. As shown in Figure 1, the upper region consists of a metallized air-filled cavity while the lower region has a substrate-filled cavity of high resistivity silicon, $\varepsilon_r = 11.7$, which is also metallized on the lower side. To measure the response of these circuits, grounded coplanar waveguide (GCPW) feeding lines are used followed by upper and lower cavities that are grounded through direct contact with the ground planes of the coplanar lines. Other important design issues are the development of accurate alignment marks between the various wafer layers that ensure repeatable alignment, a mechanism for exciting the individual circuits and the incorporation of a shielding environment for the individual circuits. Alignment is achieved by incorporating alignment and probing windows that are entirely etched through to expose the lower wafer surface. Shielding is achieved by developing a substrate-filled cavity beneath the line on the lower wafer while an air-filled cavity is formed over the line in the upper wafer. Descriptions of the individual wafer layers used to construct the completely shielded micromachined circuit are discussed in the next paragraph.

The *lower wafer* shown in Figure 3 is a high resistivity, single-side polished silicon having a dielectric mask of silicon dioxide and wafer thickness of 350 μm. To develop the circuits, the planar lines are printed using standard photolithographic techniques and a seed layer of titanium/gold/titanium is initially evaporated and then electroplated to achieve the appropriate metal thickness, in this case 3 microns. After the circuits and alignment marks are printed, the lower side of the wafer is patterned using an infrared alignment to expose the regions that form the lower cavity. Since the cavities must be underneath the individual circuits, the alignment windows and the lower cavities are defined on the

unpolished side of the wafer. Prior to anisotropically etching the silicon, the oxide is removed from these areas using buffered hydrofluoric acid (BHF). The anisotropic etchant, ethylene diamine pyro-catechol (EDP), uses the <111> crystal plane of <100> silicon wafers as an etch stop causing an etch angle profile of 54.75° to form non-vertical sidewalls in the cavities as seen in Figure 3c with the lower cavity having its widest dimension near the upper surface. Prior to evaporating the final metal, the oxide in the groove underneath the ground plane is removed and then metallized and plated to metal thickness of 3 microns to form direct contact.

The *upper wafer*, shown in Figure 4, requires patterning of both sides of the wafer prior to etching the cavity and probe windows. In this study, a low resistivity silicon wafer is used having a thickness of 500 μm with 7,500 Å of thermally grown oxide on both sides. After defining the probe window and alignment marks to be etched using photolithography, a thin metal layer of Ti/Au is evaporated for a lift-off procedure to mask the remaining silicon. This extra masking layer serves two purposes; it offers additional protection to the upper cavity roof and is used as a mask during infrared alignment to pattern the lower side of the windows as well as the upper cavities. Prior to etching, the oxide is removed from the areas where silicon is eventually etched as shown in Figure 4 and from the area where etch rulers are located that have widths corresponding to specific depths. This double sided etching process provides mechanical strength in multiple cavity wafers, Figure 5, by including a structural beam in the probe windows which increases handling ease during mounting of the upper wafer.

Integration of the upper shield to the lower shielded planar circuits is completed after alignment and attachment of the two wafers via the microscope using regular adhesion methods. The resulting configuration is shown in Figure 6 where the heights of the upper and lower cavities are 280 and 350 microns respectively, while the widths are 1180 and 980 microns respectively. In applications where only upper half shielding is required, fabrication is easily achieved by excluding the lower cavity formation.

III. EXPERIMENTAL VALIDATION AND DISCUSSION

A. Measurement Technique

In order to characterize the circuits up to 40 GHz, current measurement systems require the use of a probe station to measure planar geometries. The set-up used for this work consisted of an HP 8510B Network Analyzer, an Alessi probe station and Cascade Microtech ground-signal- ground probes with a probe pitch[1] of 150 μm. To accurately measure the circuit performance of the micromachined shielded circuits, the Thru-Reflect-Line (TRL) calibration technique is used [11,12] where standards and various circuit components having identical upper and lower shielded regions are fabricated using the fabrication process techniques described above. A one tier de-embedding method is implemented for on-wafer probing to calibrate the system reference plane along the transmission line [13]. As a result, all transitions between the ANA and the newly defined circuit reference plane are taken into account and the appropriate coefficients are computed to establish an accurate calibration.

B. Micromachined Circuit Component Characterization

Simple discontinuities have been implemented to show the realization of conventional circuits in a micromachined configuration. This paper investigates a *series open-end stub* and *a low-pass filter* and compares measured results to theoretical ones.

The ***series open-end tuning stub*** has physical dimensions shown in Figure 7. Comparison between measurements and full wave analysis results is shown in Figure 8. As observed from this figure, the theoretical and experimental results exhibit a shift in the resonant frequency of about 6.9% since the micromachined resonance occurs at 29 GHz compared to the 27 GHz response of the modeled circuit. Although the overall circuit performance is similar, the discrepancy in the resonant frequency can be attributed to the variations between the actual modeled circuit and the one fabricated and measured. The resonant frequency is affected by the fact that the measured line length behaves electrically shorter since there is rounding of the corners and edges of the stub fingers caused during fabrication. This is not accounted for in the model. In addition, metal thickness has been neglected although it has

1. Pitch is defined as the spacing between the center conductor to the ground probe tips.

been found to contribute considerably to frequency shifts [14]. Lastly, the difference in the magnitude between measurement and theory may be attributed to the fact that the theoretical model assumes a lossless system while in reality the circuit inheritly has both conductor and dielectric loss.

A ***five-section stepped-impedance lowpass filter***, designed as shown in Figure 9, has high and low impedances of 100Ω and 20Ω respectively and is surrounded by the cavity structure described above. In Figure 10 measurements are shown and compared to theoretical results derived from quasi-static models where conductor and dielectric losses are included. Regarding conductor losses, care was taken to incorporate the specific metallization thickness and the appropriate surface resistivity corresponding to the various sections of microstrip line widths [15]. To realize 100 and 20 ohm impedance steps, 20 μm and 380 μm wide conductor lines are used with slot widths of 210μm and 30μm. Electrically the low impedance sections propagate a coplanar waveguide mode due to the narrow slot width while the high impedance sections propagate a microstrip mode. These sections of lines are connected in series resulting in a mixed mode excitation, thus creating parasitics which cannot be easily accounted for in the quasi-static model. Despite this limitation, however, it can be seen that the measurement response is similar to the model. This is due to the relatively low frequency of operation which reduces the effect of the parasitic mechanisms. The total loss in the system, plotted on Figure 11, shows good agreement between theory and measured results thus confirming the effectiveness of the micromachined integrated shield and the elimination of loss associated with radiation effects.

Although the PUFF model incorporates the loss effects into the ideal transmission line theory, full-wave analysis for a lossless system using FDTD is much more reliable (accurate) in predicting the behavior of the micromachined component. Puff is limited in this respect, since it cannot account for parasitics or coupling due to radiation, whereas, the FDTD model has the advantage in that it models the electrical performance based on the exact physical circuit dimensions in both horizontal and vertical dimensions. The results in Figure 12 derived by FDTD show excellent agreement between measurement and theory with the exception of loss.

IV. CONCLUSION

In the above, simple circuit geometries used in conventional planar line designs have been implemented in micromachined form; namely, a series tuning stub and a stepped impedance lowpass filter. The results show that micromachining offers great design capabilities to high frequency application, while preserving electrical performance.

The development of micromachined circuits for the miniaturization of conventional microwave circuits has been proven successful. The fabrication of these lines has been presented and measured results have been shown and compared to quasi-static and full-wave theoretical ones. The data presented prove that monolithic integration of the shield using micromachining techniques allows for the development of circuit components that offer comparable performance to conventional circuits.

V. ACKNOWLEDGEMENTS

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Figures

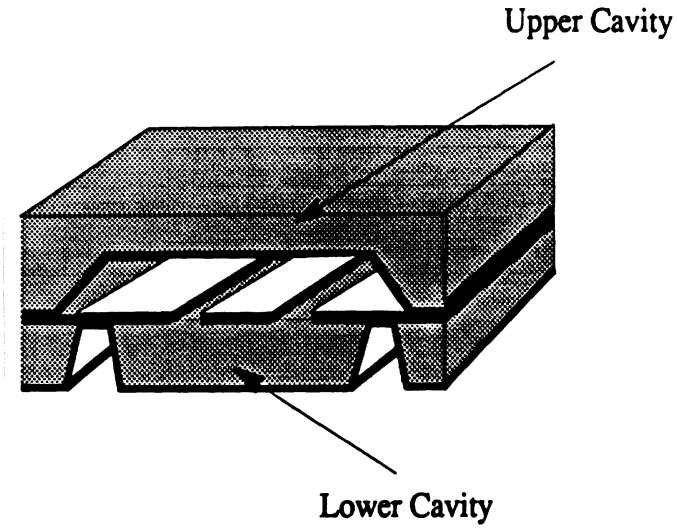


FIGURE 1. Three - dimensional cross section of micromachined lines where the shield and line are integrated monolithically.

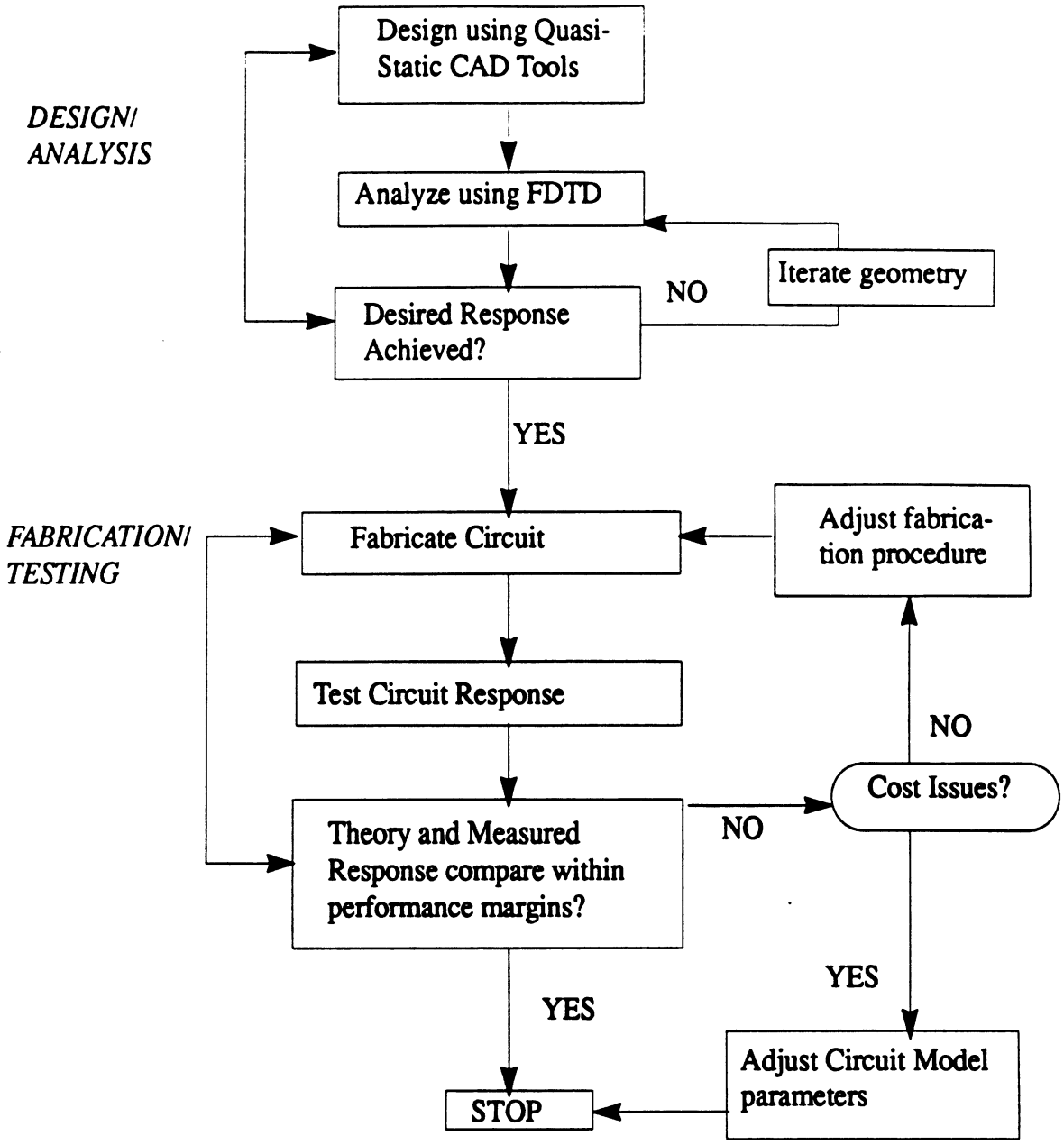


FIGURE 2. Design Procedure for Micromachined Circuits.

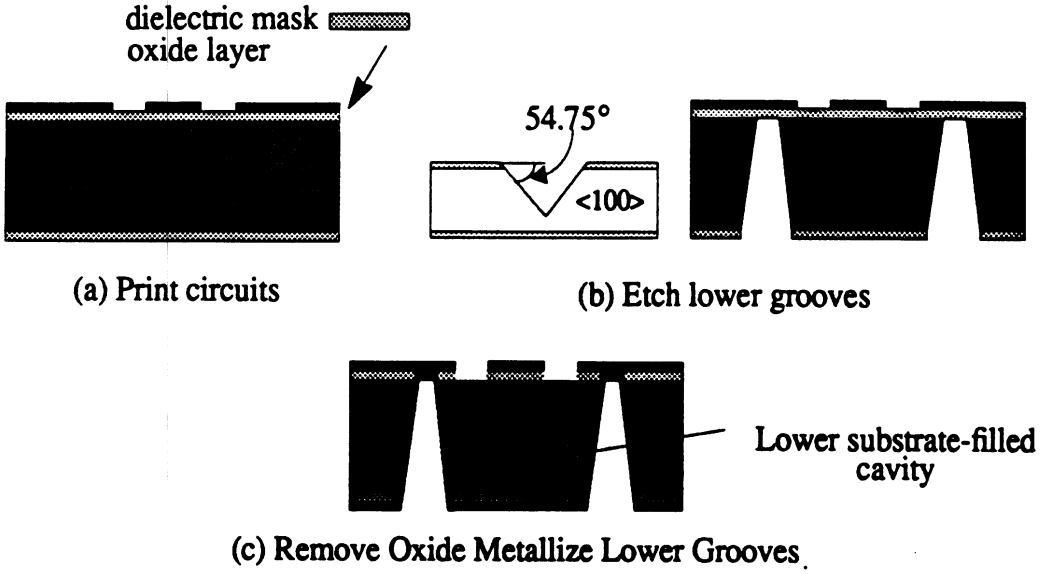
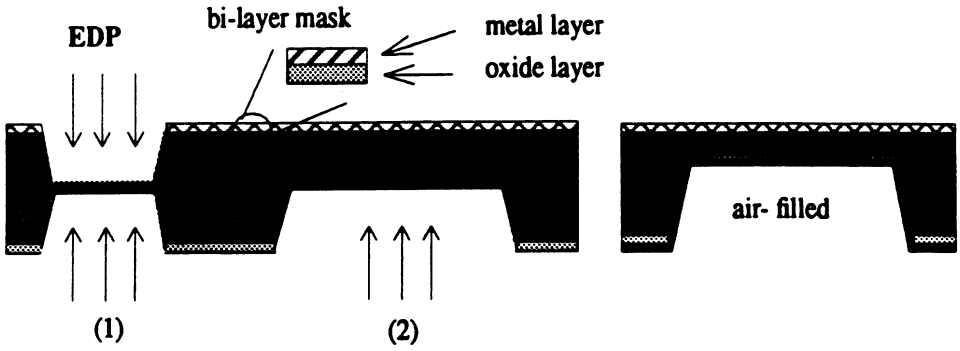
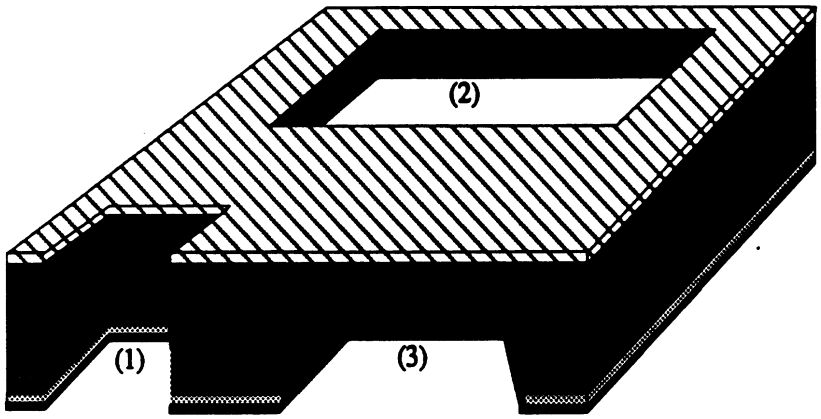


FIGURE 3. Lower Wafer Development. (a) Transmission lines are printed on the top surface.(b) Lower cavity is formed by etching v-grooves with an etch angle of 54.75 degrees in <100> silicon using anisotropic etchant. (c) Lower cavity grooves are metallized below the line.



(a) (1) Alignment marks and probe windows
(2) Upper cavity

(b) Metallize cavity



(c) Final cross-sectional view: (1) alignment mark, (2) probe window, (3) upper cavity

FIGURE 4. Upper Wafer Development. (a) Etch the probe windows and alignment marks from both sides while etching the cavity from one side only. (b) The cavities are metallized. (c) Final view of a section of the upper wafer.

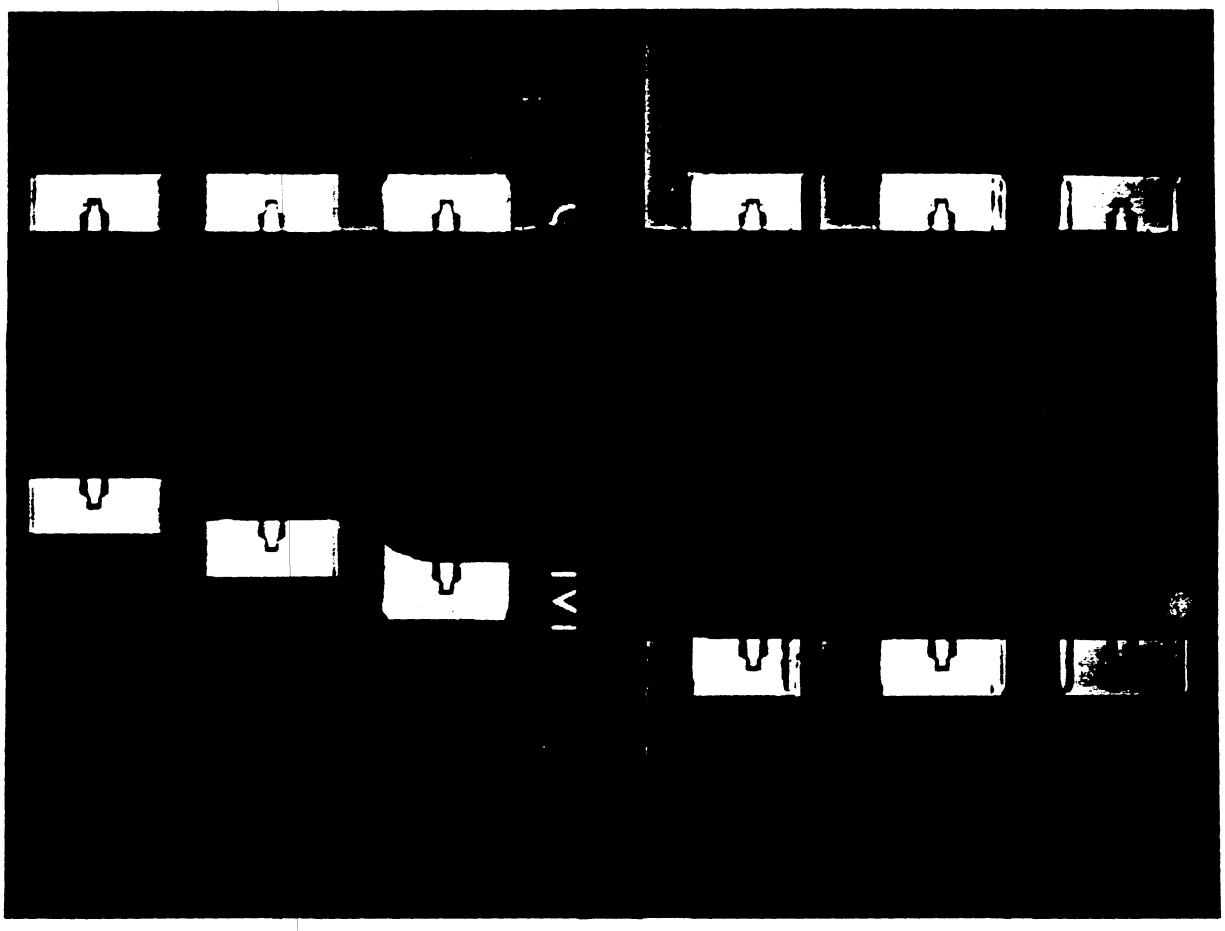


FIGURE 5. Photograph of circuit from top view where the probe windows are shown in relation to the transmission line wafer.

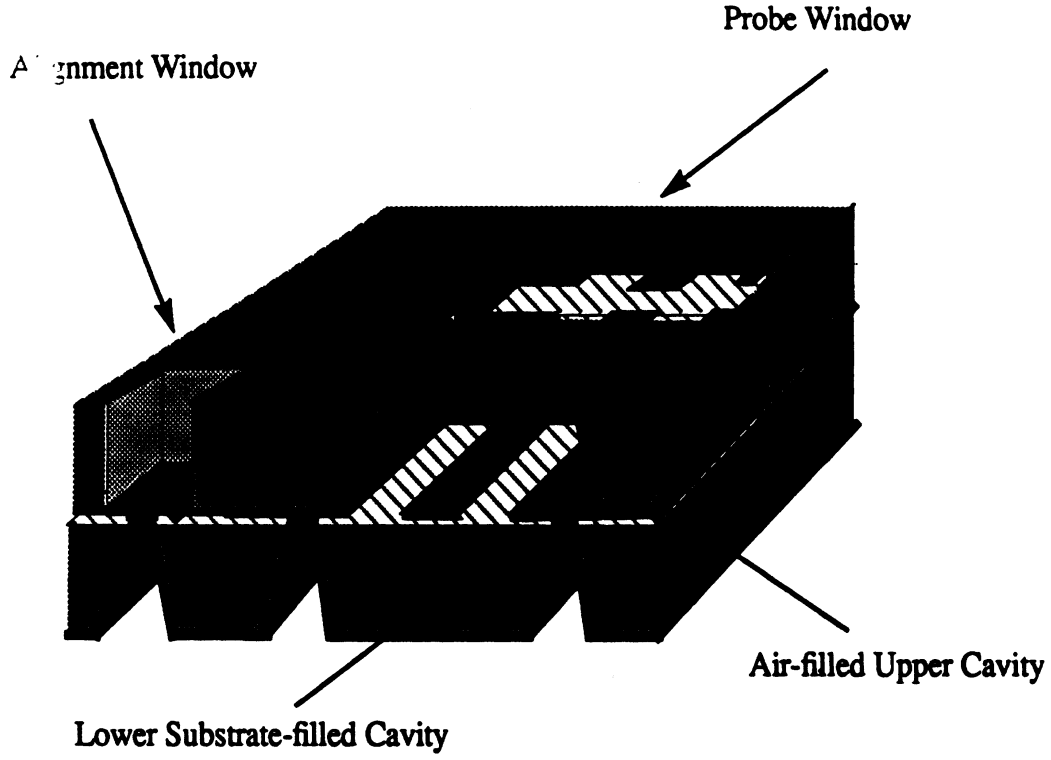


FIGURE 6. Completely Shielded Micromachined Circuit after lower and upper wafer alignment.

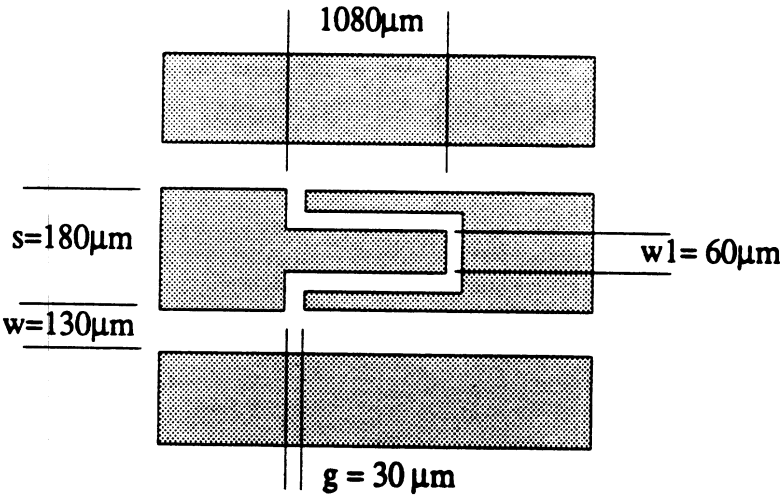


FIGURE 7. Series Open-End Tuning Stub.

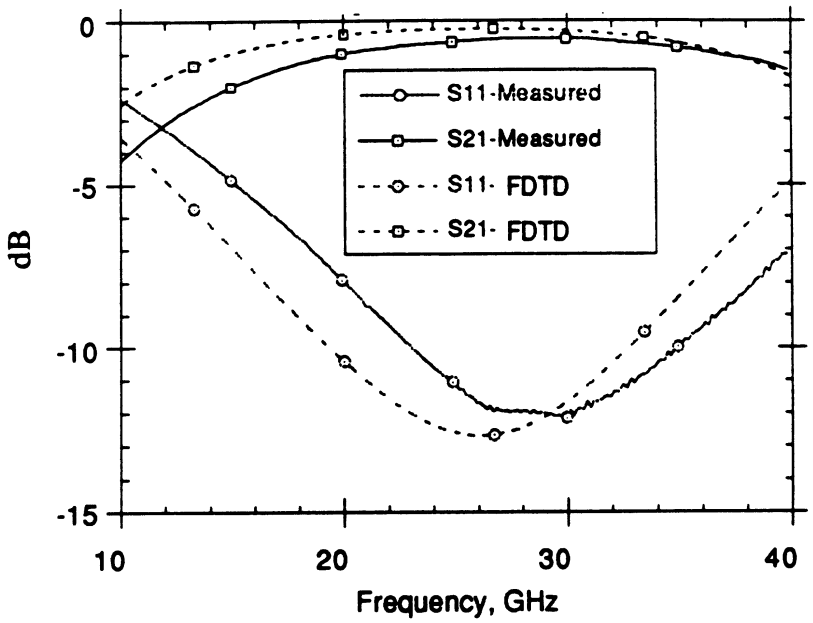


FIGURE 8. Measured vs. FDTD results for the Micromachined Shielded Series Open End Stub.

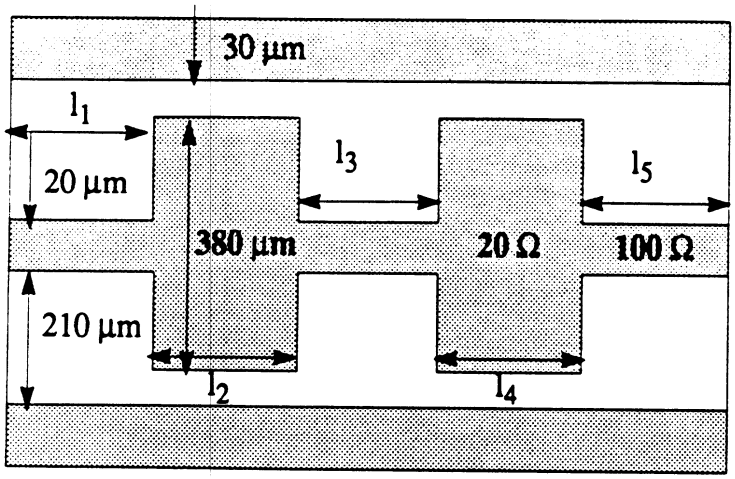
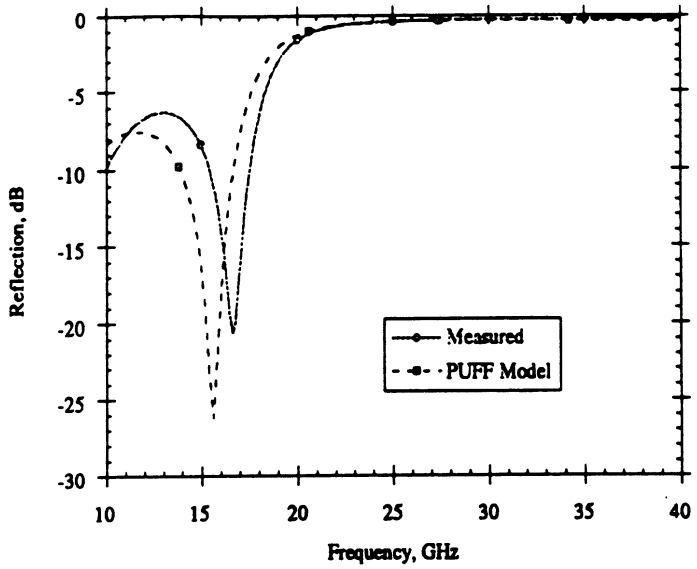


TABLE 1. Circuit Dimensions

Line Lengths (microns)
l_1= 988
l_2=703
l_3=940
l_4=722
l_5=988

FIGURE 9. Stepped Impedance Lowpass Filter Circuit Dimensions with low impedance sections of 20 ohms and high impedance sections of 100 ohms.



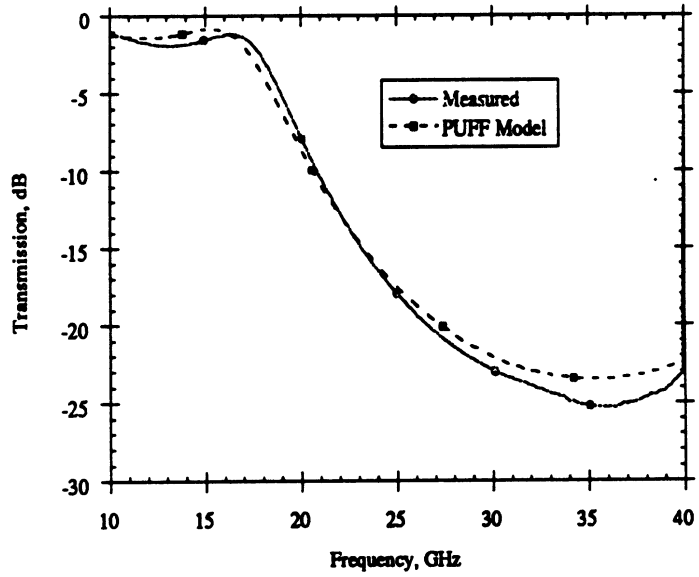


FIGURE 10. Comparison between the PUFF quasi-static model and measured results.

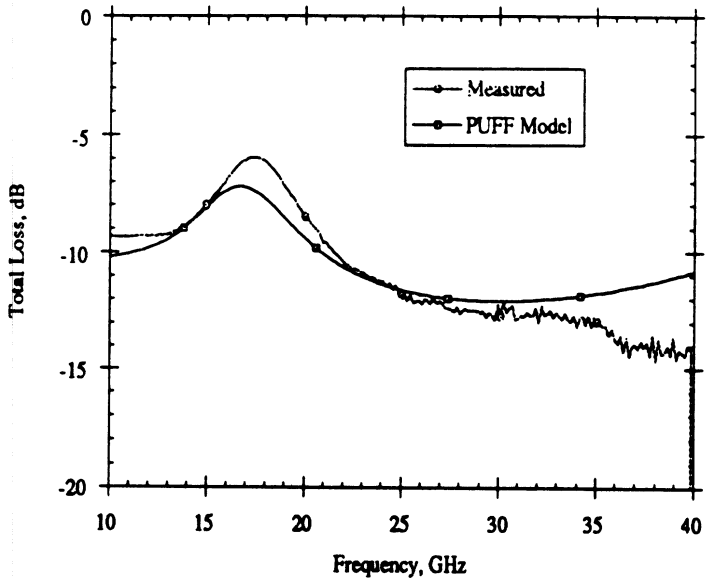


FIGURE 11. Comparison between measured and PUFF modeled Loss response.

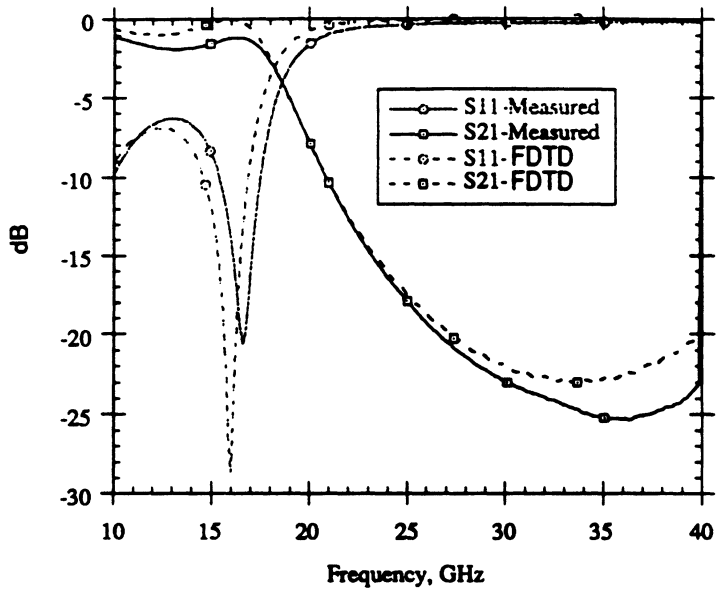


FIGURE 12. Measured and FDTD results for the Completely Shielded 5-section Lowpass Stepped Impedance Filter.

Figure Captions

Figure 1: Three - dimensional cross section of micromachined lines where the shield and line are integrated monolithically.

Figure 2: Design Procedure for Micromachined Circuits.

Figure 3: Lower Wafer Development. (a) Transmission lines are printed on the top surface.(b) Lower cavity is formed by etching v-grooves with an etch angle of 54.75 degrees in <100> silicon using anisotropic etchant. (c) Lower cavity grooves are metallized below the line.

Figure 4: Upper Wafer Development. (a) Etch the probe windows and alignment marks from both sides while etching the cavity from one side only. (b) The cavities are metallized. (c) Final view of a section of the upper wafer.

Figure 5: Photograph of circuit from top view where the probe windows are shown in relation to the transmission line wafer.

Figure 6: Completely Shielded Micromachined Circuit after lower and upper wafer alignment.

Figure 7: Series Open-End Tuning Stub.

Figure 8: Measured vs. FDTD results for the Micromachined Shielded Series Open End Stub.

Figure 9: Stepped Impedance Lowpass Filter Circuit Dimensions with low impedance sections of 20 ohms and high impedance sections of 100 ohms.

Figure 10: Comparison between the PUFF quasi-static model and measured results.

Figure 11: Comparison between measured and PUFF modeled Loss response.

Figure 12: Measured and FDTD results for the Completely Shielded 5-section Lowpass Stepped Impedance Filter.

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Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques

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ABSTRACT

The objective of this paper is to present a new concept in packaging: the development of self-packaged high frequency monolithic circuits using silicon micromachining technology. These circuits employ miniaturized housings to shield individual passive circuit components (e.g. CPW) or active elements or combinations of them. Primary advantages of such self-packaged configurations at these frequencies include reduction in overall size and weight and increased isolation between neighboring circuits. These characteristics make the presented micropackaged components appropriate for high density, multilevel interconnect circuits. In this paper, the fabrication procedures used to develop self-packaged components are described and performance curves of measured and theoretical results for typical high frequency circuit geometries are shown.

I. INTRODUCTION

Microwave and millimeter wave circuit design relies heavily on the use of planar transmission lines such as microstrip, stripline, and coplanar waveguide to achieve design flexibility as well as ease in mounting active components. While microstrip and stripline have been utilized the most in the development of passive circuits, limitations in the realization of desired circuit layout have introduced the use of coplanar waveguide or slotline, due to the inherent advantages posed by their geometries, to create what is known as uniplanar circuits. While the combination of the aforementioned lines offers versatility in circuit design, it intensifies parasitic mechanisms such as electromagnetic coupling and parasitic radiation which compromise performance and make

success in design conditional upon circuit performance requirements. Therefore, the development of a novel circuit geometry that offers the capability of self-packaging while preserving the structural characteristics of conventional uniplanar technologies can provide a new dimension to high frequency circuit design. Individual shielding to specific circuit components, provided in monolithic form, allows for more compact circuit configurations and successfully addresses the issue of high density. This individual shielding of circuit components is achieved through the use of monolithic cavities which are referred to as "micropackages" since they can exist in miniature form within a larger housing configuration. These self-packaged circuit geometries can be fabricated through the novel use of well established Si or GaAs micromachining technologies.

In typical applications, circuits are packaged in metallic housings which tend to introduce unwanted parasitics and multiple resonances and ultimately lead to overall performance degradation. In addition to the above, conventional housing structures can be rather costly and inappropriate for use in lightweight system designs. Micropackaging, on the other hand, can result in increased circuit density while performance requirements are attained through reduction of parasitic electromagnetic coupling in the substrate (substrate modes) and air (space waves). Circuit micropackaging is achieved through cavity regions which are fabricated in materials such as silicon or GaAs and are designed to electrically and/or hermetically encapsulate planar circuit components or subsystems. While preserving monolithic character, micropackaging allows for easy integration with other more conventional circuit arrangements and shielding environments. In applications related to cellular and mobile communications, the resulting self-packaged lightweight circuits offer controllable parasitics and are appropriate for systems with demanding performance requirements.

Although micromachining of silicon is a well established technology for sensor and biomedical applications, for the first time this technology is being applied to develop self-packaged circuit components for high frequency applications. The development of completely shielded micromachined circuits is presented in this paper. The circuit components may be of microstrip or coplanar

waveguide (CPW) type and are surrounded by an air-filled cavity in the upper region and a substrate-filled cavity in the lower region. Both cavities are integrated monolithically with the circuits, as shown in Figure 1. Since a comprehensive understanding of fabrication capabilities is critical for the development of these circuits, an extensive study of various fabrication techniques has been performed and a brief description of the findings is presented. To show applicability to high frequency circuit design, simple components such as tuning stubs and filters are developed and measured data are compared to theoretical results. In part (a), a general overview of the design approach is given followed by an extensive discussion of the fabrication procedures developed and implemented. In the part (b), measurement considerations are discussed, fundamental line characteristics are presented, and experimental results for various circuit components such as tuning stub elements and filters are shown.

The structures presented in this paper represent only one approach for implementing micromachining techniques to high frequency circuit design. The use of silicon fabrication processes can allow the circuit designer to alter the substrate geometry in a number of creative ways in an effort to optimize circuit performance and reduce its size. By using other approaches, effective forms of hermetic micropackaging mounts or other protective packaging types may be developed for use in hostile environments. Since micromachining has only been recently used in high frequency applications, the development of micromachined circuits is still in its infancy. Therefore, in an effort to outline the potential of this technology, this article presents the first generation of micromachined, self-packaged circuit components.

II. DEVELOPMENT OF MICROMACHINED CIRCUITS

In order to illustrate the versatility of micromachining, this effort concentrates on developing circuits that reside in partially or completely shielded environments. As it has been extensively discussed in the literature, poor circuit performance in circuits operating in open environments is attributed to free-space radiation and substrate mode excitation, while in shielded environments it

is mainly due to package resonances. The open environment described herein refers to circuits which are printed on a dielectric substrate and are free to radiate into free space. On the other hand, the term "shielded geometries" implies circuits which can be partially or completely shielded through cavities in the upper and/or lower regions. Since substrate modes occur in the dielectric substrate, introducing physical alterations to the substrate itself can result in elimination of these parasitic waves and improvement of circuit performance. In conventional packaging mounts unwanted parasitics can cause package resonances which interfere with circuit performance and provide very strict limitations to design. The proposed approach eliminates these resonances by developing micropackages (shielded structures) that are small in size, can follow individual circuit paths, and can be fabricated monolithically with the circuit. The result is a self-packaged circuit that can be effectively used with other conventional circuits within larger conventional housings either hybridly using flip-chip technology or monolithically in miniaturized packaged configurations. The following sections outline the steps needed to design the circuits mentioned above and extensively describe the silicon (Si) fabrication processes required for their development.

II.A Design

The first step in the design of high frequency circuits is the specification of the geometrical parameters needed to provide the desired electrical performance. While there exists a wide variety of commercially available computer aided design (CAD) tools for low-frequency applications, circuit design software for high-frequency applications is currently unavailable. Despite the lack of high-frequency CAD software, there is a wealth of high frequency circuit simulation tools that can be used indirectly in circuit design which produces satisfactory results but requires very long design cycles and extensive computation times. The micromachined self-packaged circuits presented here have been designed through such an iterative approach. In this iteration scheme, initial design is based on low-frequency software models that use quasi-static approximations [1-2]. Given this design, the geometrical parameters are changed in an iterative manner and the new cir-

cuit performance is predicted using the high-frequency analysis software which is based on full-wave models in frequency or time domains. When the predicted electrical performance closely matches the desired one, this iterative cycle is terminated [3-10].

Additional issues that need to be addressed during the design stages are package resonances and substrate mode excitation. As it has been extensively described in the literature [11-12], electrical packages can greatly affect circuit performance either through package resonances or through proximity coupling. The first effect is mostly related to the dimensions of the package while the latter is due to cross-coupling of neighboring circuits. Unfortunately these two mechanisms require contradicting measures which lead to design trade-offs. Ideally, a given circuit has an optimum package size that is small enough to eliminate resonances within the range of operating frequencies and that is physically far enough away from the circuitry so that it does not interfere with the circuit's electrical performance. Although circuits in open environments do not face the previously described problems, they are prone to parasitic radiation which is mostly associated with the excitation of substrate modes. Since the excitation of these modes is mostly dependent on the operating frequency and the physical thickness of the substrate, careful layout configurations in less dense circuit environments can sometimes reduce parasitic radiation, provided there is flexibility in circuit placement. In practical applications, however, circuit requirements greatly limit the flexibility in rearranging the location of the various circuit components such that any layout modifications, at best, can only weakly reduce parasitic loss [13].

During the characterization efforts performed, preliminary findings indicate that substrate modifications alone may have a substantial impact on substrate mode excitation. While researchers have been aware of the issues discussed above since the late seventies when planar monolithic and hybrid circuit approaches became fundamental to high-frequency circuit design, the existing at that time technology could not provide alternative solutions to substrate modes excitation. Recent advances in silicon micromachining techniques, however, allow for unique, yet simple practical solutions to the above problems. With the development of micropackages, dimensions

can be chosen simply by using waveguide and cavity models to predict geometrical dimensions that avoid unwanted resonances. In addition, the shape of the cavity can be designed so that it follows the circuit and does not physically affect its performance. For open circuits, substrate modifications using micromachining can be implemented to eliminate these unwanted substrate modes entirely, resulting in improved circuit performance.

II.B Fabrication Procedures

The micromachined circuits described here are made on a two silicon wafer system having a <100> orientation and primarily utilize silicon micromachining processes. Although fairly standard in sensor applications, these techniques are relatively new to high frequency circuit design. This section presents an extensive discussion on the fabrication steps required for the development of self-packaged circuits and provides a detailed description of the employed processes.

All circuits presented herein are of coplanar type, are printed on Si and are shielded by miniature cavities in either or both upper and lower surrounding regions. As seen in Figure 1, the upper region consists of a metallized air-filled cavity while the lower region is a substrate-filled cavity that is metallized on the lower side. Since the circuits are printed on the lower wafer, high resistivity silicon with $e_r = 11.7$ is required. In this configuration the upper and lower cavity regions provide ground plane equalization through direct contact with the ground planes of the coplanar waveguide lines. Issues important to consider during design include the fabrication of accurate alignment marks between the various wafers, the design of appropriate feeding lines for individual circuit excitation, and the development of enclosing environments that can be integrated monolithically with the specific circuits without degrading electrical performance. The following sections address these concerns comprehensively while describing the technique used for individual wafer development.

The *lower wafer* shown in Figure 2 is a high resistivity, single-side polished, 350 μm thick silicon substrate having a dielectric mask of silicon dioxide that has been thermally grown to 1.2 μm

thickness. To develop the circuits, the planar lines are printed using standard photolithographic techniques. Since electroplating is used to achieve the 3 micron metal thickness needed for Ka band operation, a seed layer of titanium/gold/titanium (Ti/Al/Ti) is initially evaporated. After the circuits and alignment marks are printed, the lower side of the wafer is patterned photolithographically and regions needed to form the lower cavity are defined using an infrared (IR) alignment procedure. With the substrate-filled cavities being underneath the individual circuits, alignment windows are needed and through this process are defined together with the lower cavities on the backside of the wafer. Prior to anisotropically etching the silicon, the oxide is removed from the areas that define the cavity sidewalls using buffered hydrofluoric acid (BHF). The anisotropic etchant, ethylene diamine pyrocatechol (EDP), uses the <111> crystal plane as an etch stop for <100> silicon wafers resulting in etch angles profiles of 54.75° [14]. The created cavities have pyramidal sidewalls as seen in Figure 2b, where the lower cavity is shown to have its largest width near the upper surface and smallest width at the bottom of the cavity (Figure 2c), simulating an inverted pyramid. The lower cavity shielding is formed when the oxide underneath the CPW ground plane is removed and a seed layer of Ti/Au is evaporated. To provide appropriate ground plane thickness to this lower shielding package, the seed layer is electroplated on the backside of the wafer to 3 microns.

The *upper wafer* shown in Figure 3 contains both upper cavities and alignment marks that are formed by etching from both sides of the wafer. Since these cavities only provide ground plane equalization and shielding without interfering with the signal path, it is not necessary to use high resistivity Si. The upper shielding in this work is developed using 500 μm thick low resistivity Si with 7500Å of thermally grown oxide on both sides. After defining the probe window and alignment marks using photolithography, a lift-off procedure is employed to open the areas to be etched while providing an additional masking layer of Ti/Au metal on the backside of the wafer. This layer serves two purposes, it offers protection on the back of the cavity regions and acts as a mask during backside IR alignment. On the lower side, the cavities are defined and the oxide is

removed to expose the silicon surface as shown in Figure 3. The patterns are then etched in EDP to a desired dimension which is monitored through "etch rulers" that consist of rectangular widths corresponding to specific etch depths. Since this wafer must be handled frequently after etching the multiple cavities and windows, additional mechanical strength can be provided by including a structural beam in the layout as seen in Figure 4, where the beam is located in the middle of the probe window.

After fabrication the cavities in the upper wafer are aligned to the planar circuits and cavities in the lower wafer and the two wafers are securely bonded together to complete the formation of the micropackage (Figure 5). Since the above procedures concentrate on the development of a completely shielded configuration, it should be noted that designs requiring partial shielding can be easily done by following the necessary wafer development scheme.

III. EXPERIMENTAL RESULTS AND DISCUSSION

III.A Measurement Considerations

In order to measure circuit performance up to 40 GHz, conventional on-wafer characterization is employed in conjunction with the Thru-Reflect-Line (TRL) calibration technique [15-17]. The measurement set-up uses an HP 8510B Network Analyzer that operates up to 40 GHz, an Alessi probe station, and Cascade Microtech ground-signal-ground probes that have a probe pitch[1] of 150 μm. This calibration is achieved using standards that have upper and lower shielded regions identical to those of the circuits of interest and are developed using the fabrication procedures described above. A one tier de-embedding technique is used for on-wafer probing which calibrates the system reference plane to a point within the shielded transmission line. This results in characterization of all transitions located between the input and output ports of the ANA and the newly defined reference plane.

1. Pitch is defined as the separation between the center conductor and the ground plane pin.

Measurements have been performed on partially and completely shielded configurations and are completed in two steps. Circuits with upper-half shielding, only, are characterized first. In this arrangement, the cavities are mounted on the coplanar waveguide (CPW) circuits and the whole structure is mounted on duroid with e_r = 2.2 and thickness of 3.175 mm to prevent the formation of a parallel plate waveguide between the ground planes of the CPW and the wafer chuck. The next step of this investigation deals with the characterization of various circuit geometries which are completely shielded as it has been described in previous section. Since the circuits under test are completely isolated from the outside environment, they are placed directly onto the probe station wafer chuck in the measurement set-up.

III.B Characterization of Partially or Completely Shielded Circuits

The characterization of partially as well as entirely self-packaged circuits can provide a very comprehensive understanding of the effect of micropackaging on circuit performance. The following sections present a systematic theoretical and experimental investigation which has been performed on a variety of circuits. These circuits can be grouped into three categories: (a) circuits with upper shielding (US) (b) circuits with lower shielding (LS) and (c) circuits with complete shielding (CS).

III.B.1 Delay Lines and Cavity Dimensions

To accurately characterize the presented micromachined geometries, the first issue to address is the development of feeding lines needed to provide the appropriate excitation. Since the measurement system reference impedance is 50 ohms, the feedline dimensions are determined to meet this requirement. For the circuit components presented in this paper, the feedlines were designed using CAD tools available at the University of Michigan [1]. For the on-wafer probe station, coplanar waveguide feedlines were designed to have circuit dimensions of 100 μm center conductor width and 60 μm slot width. These were determined using design equations from Ghione et. al [18]. Matching impedances in the shielded region resulted in planar line dimensions of 180 μm

center conductor width and 130 μm slot width. The cavity dimensions for these lines are given in Table 1 of Figure 6.

The micromachined circuits in this study can have several transitions which minimize the mismatch between the probe and shielded geometries (Figure 7). Specifically, completely shielded structures and partially shielded embodiments have similar transitions although one of the shielding regions is absent. The first transition occurs between two 50 ohm sections of grounded CPW (GCPW) where the first section (A-B) is a probe feeding pad having center conductor width of 100 μm and slot width of 60 μm that tapers (B-C) outward to a wider line having center conductor width of 180 μm and slot width of 130 μm. The next transition is a discontinuity (D-D) that occurs between the open GCPW line and the completely shielded GCPW. At this transition the conducting line dimensions remain the same but an upper shield has been integrated monolithically and has dimensions that are chosen such that the impedance of the line is not effected by the presence of the shield. As mentioned earlier, the upper region is an air-filled cavity with a width of 1200 μm and height of 280 μm while the lower region is a dielectric-filled cavity that is designed narrower and has width of 950 μm and height equal to 350 μm. The lower cavity dimensions provides the minimum cavity width in which the sidewalls will not interfere with the field confinement. Since the calibration reference planes are located inside this shielded region, all measured circuits have similar feedline transitions to allow use of the same calibration standard set.

The response of a through line for open CPW and upper shielded CPW has been measured and results are shown on Figure 8. As indicated by these results, the open CPW line suffers from parasitic radiation in the form of substrate modes which is indicated by the ripple shown in the data toward the higher frequency end of the band. When the same line is packaged in the upper air region only, coupling into substrate modes is reduced resulting in a flatter response over the entire frequency range.

For the lower shielded (LS) and completely shielded (CS) through line, a plot is shown in Figure 9 for the line attenuation in dB/mm which includes the effects of both dielectric and conductor loss. The results shown on the figure indicate that the lower shielded line has performance comparable to data presented by Taub [19] for losses in coplanar waveguide which is printed on silicon wafers with similar resistivity (3000 ohm-cm) and with the same aspect ratios. It is interesting to observe that attenuation in the completely shielded line (CS) is slightly higher than the lower shielded line (LS) due to additional conductor loss that is present in the upper shield. In conclusion, the data shown indicate that both LS and CS cases provide a favorable alternative to the use of grounded CPW which is known to suffer from excitation of substrate modes. In the open-end series stub section discussed later, a more thorough description of micropackaging effects on circuit performance will be presented in order to show the benefits of either partial or complete shielding compared to open environment circuit designs.

III.B.2 Short-End Tuning Stub

Various simple discontinuities are implemented to show the realization of conventional circuits into micromachined self-packaged design configurations. Figure 10 shows the physical dimensions of a series short-end tuning stub element [20] located within a completely shielded embodiment while Figure 11 shows a comparison between measured and full wave analysis results. The theoretical and experimental data are plotted and show similar electrical performance except for a shift in the resonant frequency which is attributed to the geometrical variations between the model and actual circuit geometry. Since the theoretical results do not account for losses, the difference in the level of the transmission coefficients is expected. Another geometrical variation that may also be responsible for the observed differences is the trapezoidal shape of the cavity walls as oppose to the rectangular shape assumed by the models. Furthermore, the theoretical model assumes identical widths whereas the upper cavity is actually wider than the lower cavity (see Figure 6). Both of these effects can alter the circuit parasitic capacitances, thus, modifying the bandwidth and resonant frequency. Lastly, since the model assumes perfectly rectangular corners

in the stub fi: -s, the measured line lengths can appear electrically shorter since the stub fingers suffer from rounding of corners and edges as a result of the fabrication procedures.

III.B.3 Filters

A five-section stepped-impedance CS lowpass filter has been designed as shown in Figure 12 with high and low impedances of 100 Ω and 20 Ω, respectively. Figures 13 and 13 show a comparison between measurements and theoretical results derived from quasi-static models with both conductor and dielectric losses are accounted. In the PUFF [2] model, care was taken to incorporate the specific metallization thickness and the appropriate surface resistivity which correspond to the various sections of microstrip line widths. To realize 100 and 20 ohm impedance steps, 20 μm and 380 μm wide conductor lines are used with slot widths of 210 μm and 30 μm. In the low impedance section the line excites a coplanar waveguide mode due to the narrow slot width while the high impedance section excites a microstrip mode. This mixed mode operation produces parasitic inductances and capacitances that cannot be easily accounted for in the quasi-static model. Despite this limitation however, at relatively low operating frequencies the effects of such parasitics are reduced and, as seen in Figures 13 and13, the measurements agree very well with the theoretical data. The total loss in the system, as shown in Figure 15, shows good agreement between theory and measured results indicating that the circuit has negligible radiation loss and confirms the effectiveness of the micropackage. The level of loss can be attributed to the aspect ratios of the low and high impedance sections which are known to cause higher loss in both the coplanar waveguide mode [21] and the microstrip mode [22]. Additional validation of the response of the self-packaged filter is provided through a comparison between theory and experiment seen on Figure 13. The plotted data show excellent agreement between measurements and the finite difference time domain model applied for the analysis of a completely shielded (CS) geometry where loss effects have been neglected.

III.B.4 Open End Tuning Stub

The open-ended tuning stub [20] shown in Figure 17 will be used to illustrate the electromagnetic effects from a variety of micropackaging configurations. Performance curves will be shown for the upper (US), lower (LS) and completely shielded (CS) configurations. These results will be compared to open CPW and a discussion will be presented on the nature of the various effects on the circuit response.

In the case of open CPW, loosely bound fields tend to leak power strongly and destructively into substrate modes. When shielding occurs in either or both regions, the propagating modes become tightly bound to the line and radiation is reduced significantly compared to the case of the open CPW. The circuit performance shown in Figure 13 compares the open CPW to the CS geometry. The open CPW shows performance degradation above 25GHz due to the excitation of a strong substrate mode, while completely shielded circuits exhibit a very smooth response even at higher frequencies due to reduction of parasitic radiation and surface waves. When comparing the US to the LS configuration (Figure 19) for the same circuit geometry, the LS has the smoothest response due to the substantial reduction of substrate leakage. However, although the circuit performance for the US show a few ripples at the higher frequencies, overall performance improvements are observed as a nearly symmetric response is obtained. While the LS and CS scattering parameter measurements appear virtually identical in Figures 13 and 19, existing differences will become more apparent when observing the total loss data.

A comparison between the total loss of self-packaged components and open environment components, as seen in Figure 20, shows that open configurations exhibit the highest overall loss. Of the self-packaged components, the US configuration has the highest loss which is mainly due to conductor loss and excitation of a strong surface waves. The lowest loss is presented by the LS geometry since the fields are primarily confined in the dielectric-filled cavity causing a reduction of parasitic radiation effects into air. In these circuits the LS package size is chosen to be small enough to suppress unwanted resonances. Lastly, the CS geometry exhibits loss performance that

is compromised slightly when compared the to LS case due to the presence of the upper shield. In general, however, micropackages with partially or completely shielded environments can offer significant improvement in electrical performance over open environment circuits. In instances where maximum reduction in loss is needed, the lower shielded configuration is the ideal choice while optimum isolation in either or both regions requires use of the completely shielded configuration.

IV. CONCLUSION

The development of micromachined cavities for micropackaging of high frequency circuits has been proven successful. The fabrication of these structures has been presented and measured data have been compared to theoretical results. The response of simple circuit geometries used in conventional planar line designs were implemented as through lines, series tuning stubs, and a stepped impedance lowpass filter. Since the derived data show that the monolithic incorporation of a shielding cavity with the circuit results in improved performance, "self-packaged" configurations provide the ability to evaluate specific designs more comprehensively. Lastly, as a result of the good agreement between measured data and theoretical predictions for basic components, the above study strongly indicates the potential of micropackaged circuits in high frequency circuit applications.

V. ACKNOWLEDGEMENTS

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LIST OF FIGURES

FIGURE 19. Comparison of reflection (S11) and transmission (S21) coefficients between upper and lower shielded CPW environments for an open-end series stub.

FIGURE 20. Loss comparison of an open-end series stub in open (CPW), upper (US), lower (LS) and completely shielded (CS) environments.

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FIGURES

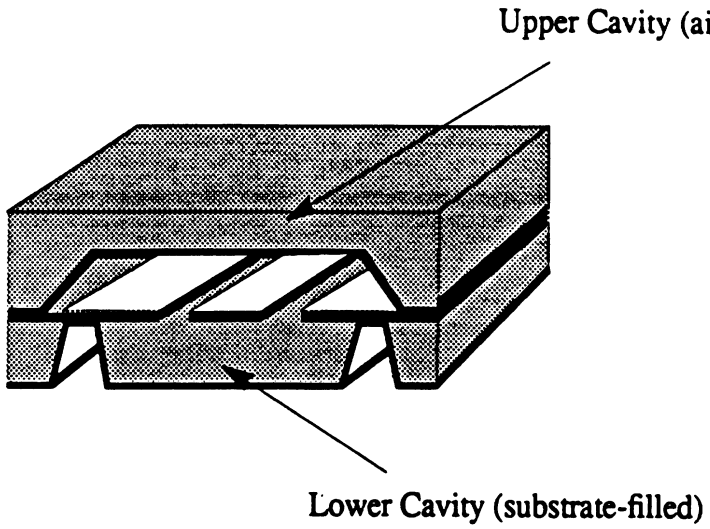


FIGURE 1. Three-dimensional cross-section of a micropackaged circuit where the shield and line are integrated monolithically.

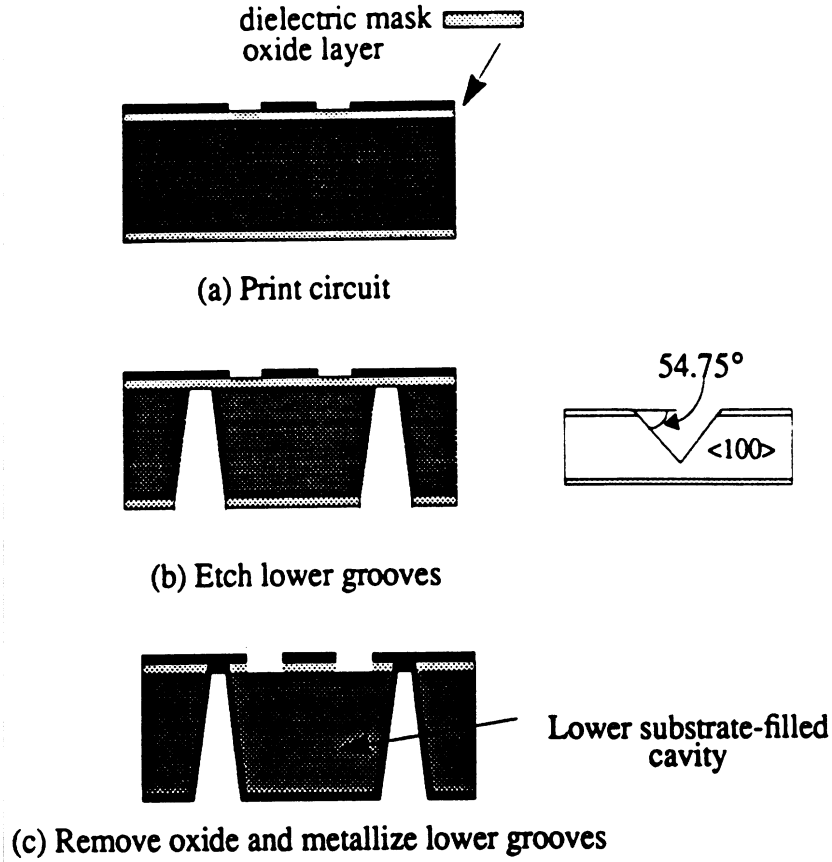
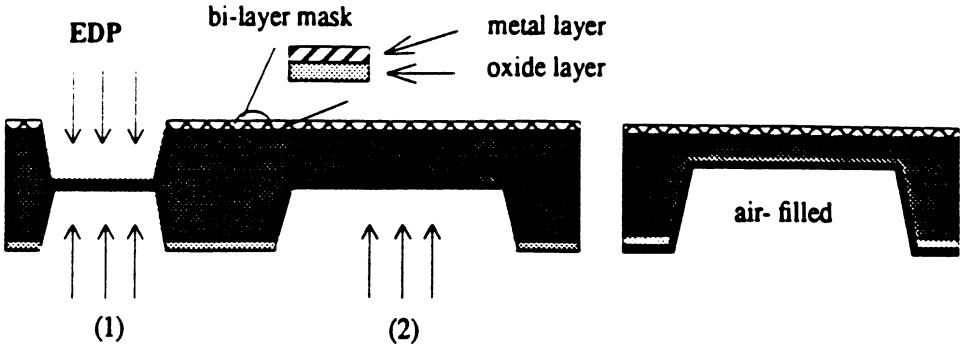
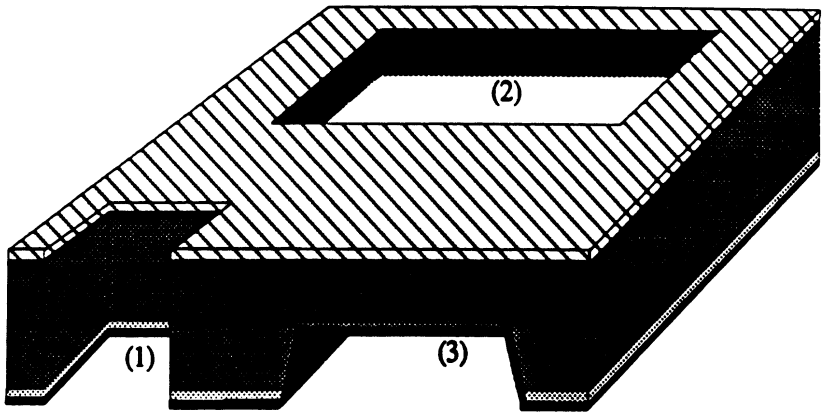


FIGURE 2. Lower Wafer Development. (a) Transmission lines are printed on the top surface.(b) Lower cavity is formed by etching v-grooves. (c) Lower cavity grooves are metallized below the line forming direct contact to the upper ground planes.



(a) (1) Alignment marks and probe windows
(2) Upper cavity

(b) Metallize cavity



(c) Final cross-sectional view: (1) alignment mark, (2) probe window, (3) upper cavity

FIGURE 3. Upper Wafer Development. (a) Probe windows and alignment marks are etched from both sides while the cavity etched from one side only. (b) The upper cavity is metallized. (c) The upper wafer sectional view after processing.

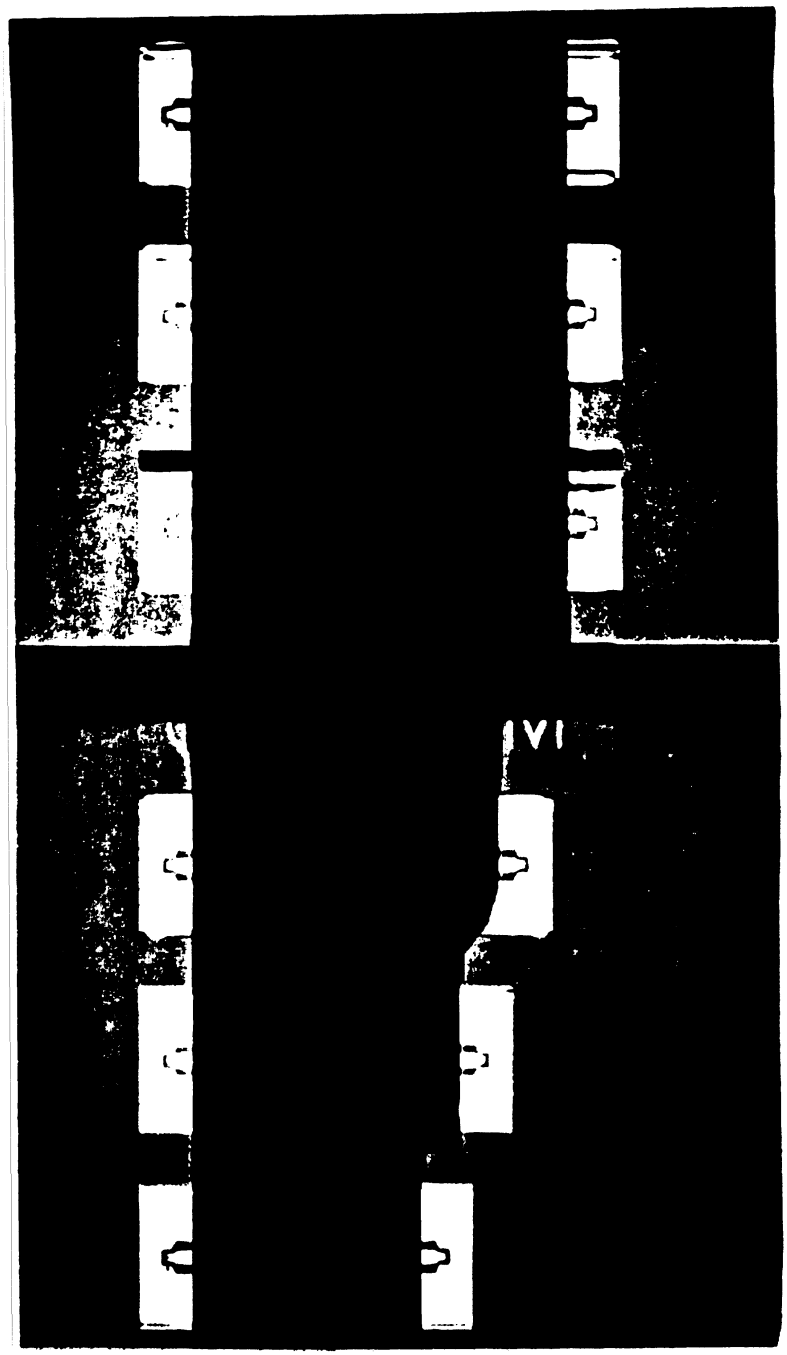


FIGURE 4. Photograph of circuit from the top view where the probe windows are shown in relation to the circuit wafer.

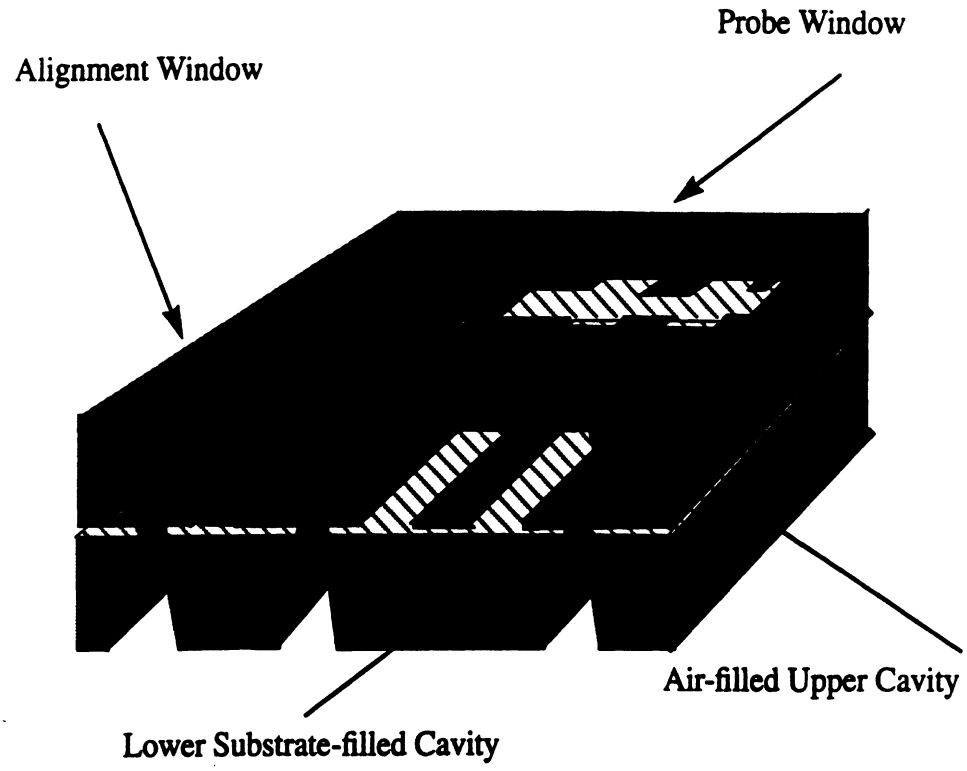


FIGURE 5. Completely shielded micropackaged circuit after lower and upper wafer alignment.

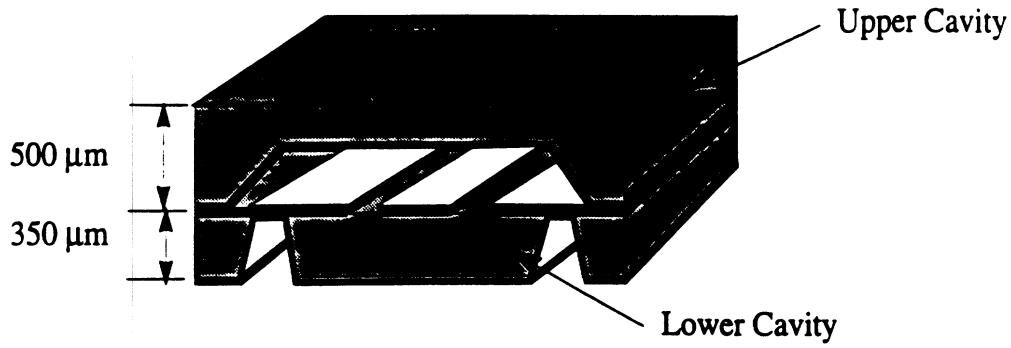


TABLE 1. Cross Sectional Dimensions of Shielded Circuits

Cavity	height (µm)	width-max (µm)	width -min (µm)
Upper	280	1200	800
Lower	350	950	500

FIGURE 6. Dimensions for the completely shielded micropackaged circuit.

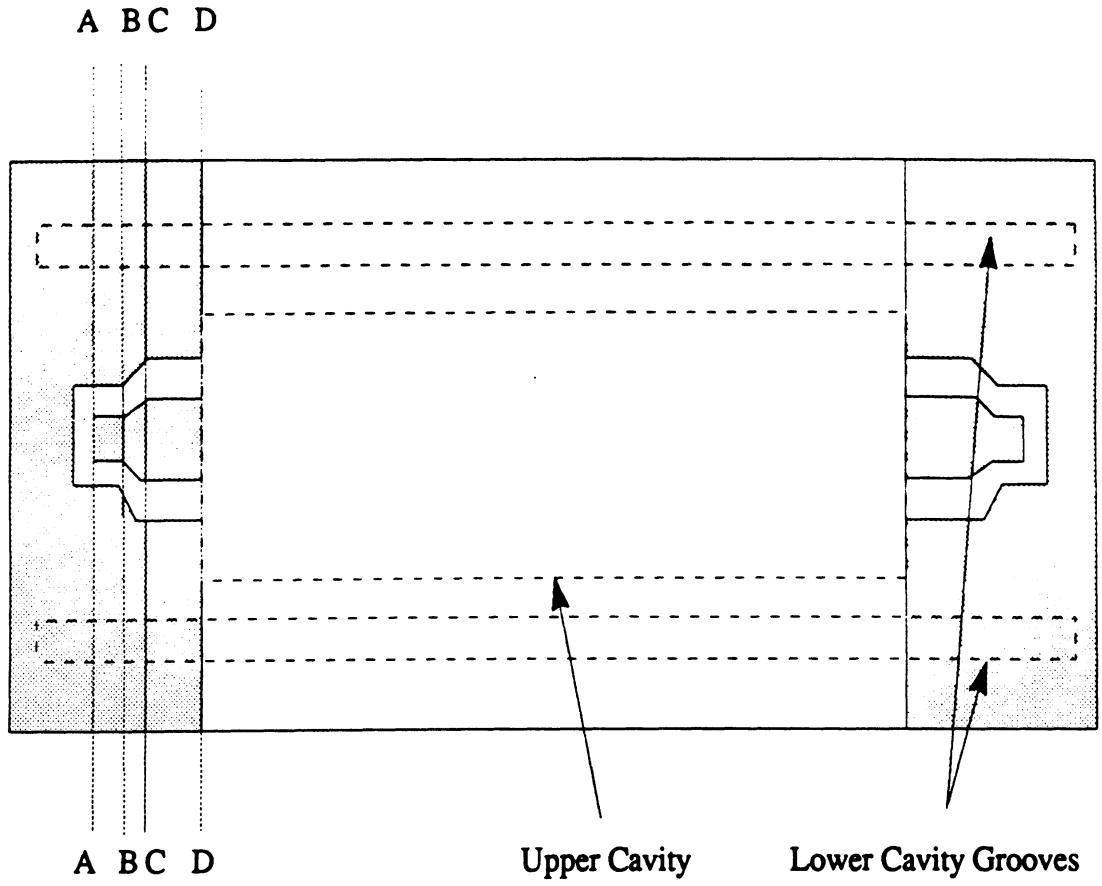


FIGURE 7. Various transitions of a completely shielded micropackaged circuit used for on-wafer probing.

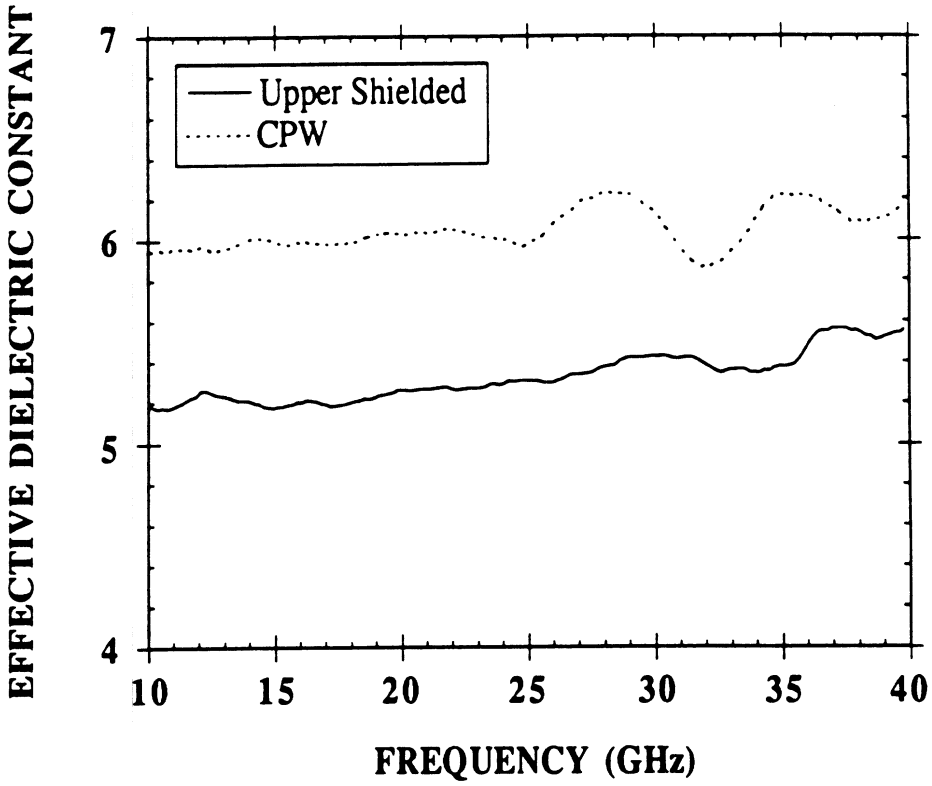


FIGURE 8. Effective dielectric constant for an upper shielded and open CPW through line.

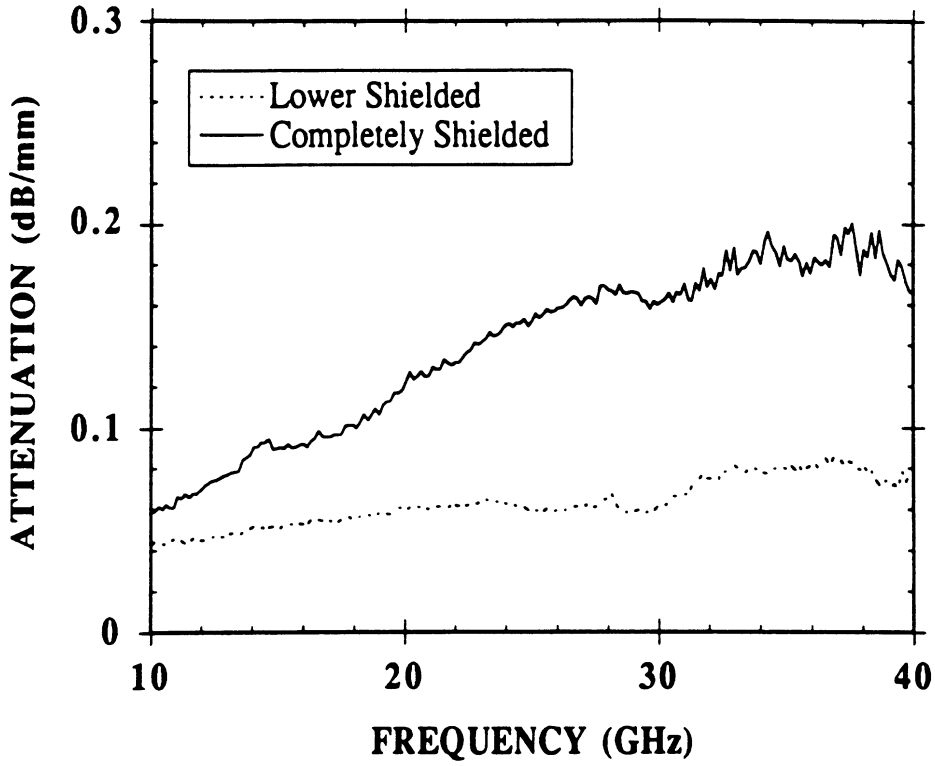


FIGURE 9. Attenuation constant for a completely shielded and lower shielded through line.

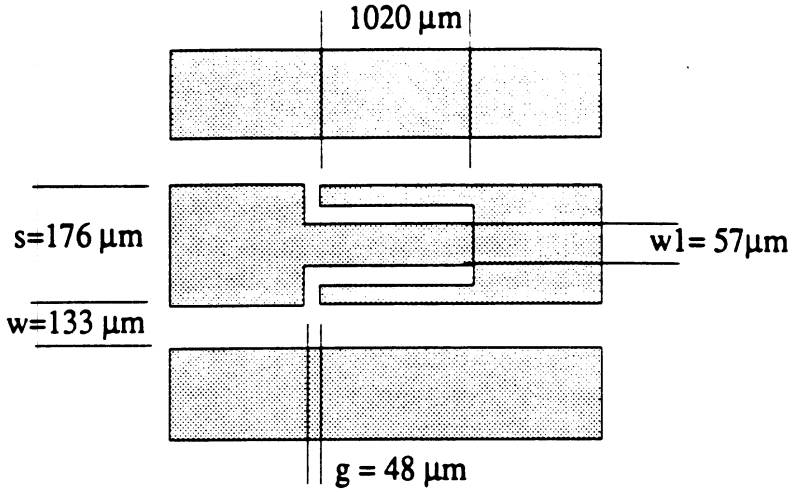


FIGURE 10. Series short-end tuning stub dimensions.

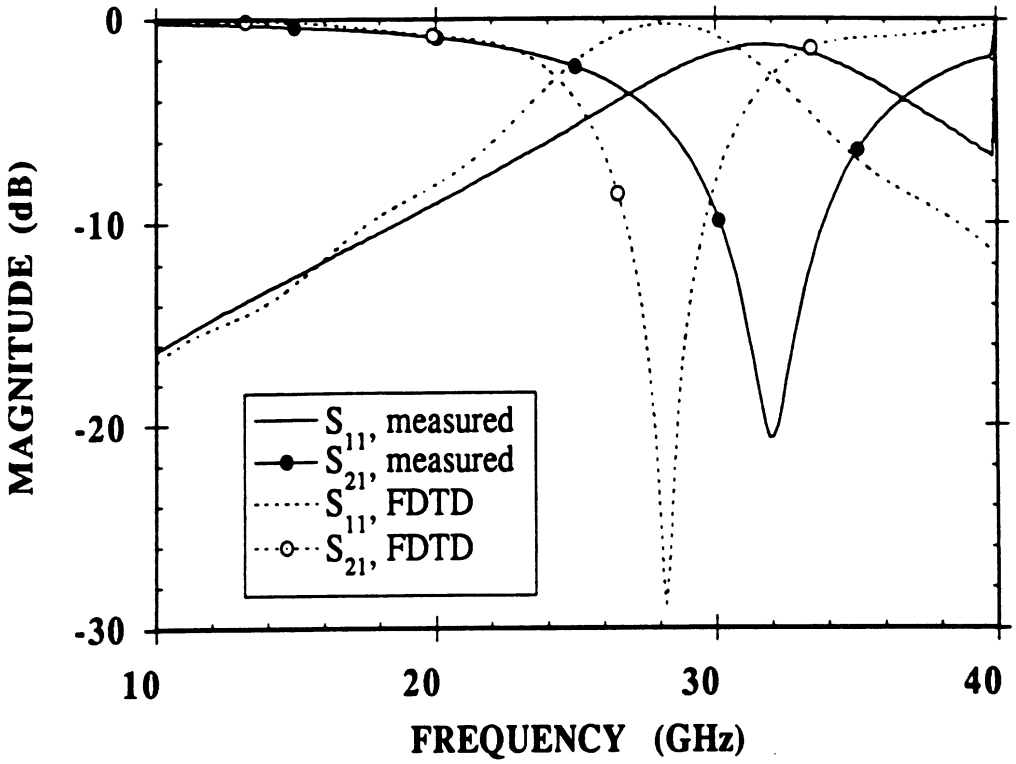


FIGURE 11. Comparison between FDTD model and measured results for reflection (S11) and transmission (S21) coefficients of a completely shielded short-end tuning stub.

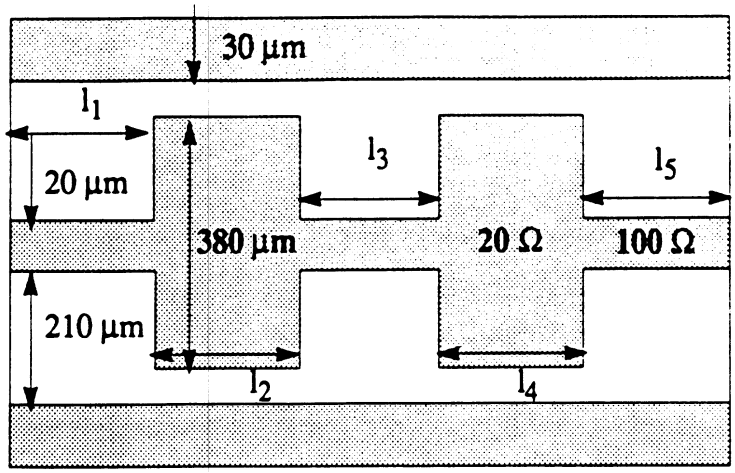


TABLE 2. Actual Circuit Dimensions

Line Lengths (microns)
l_1= 988
l_2=703
l_3=940
l_4=722
l_5=988

FIGURE 12. Dimensions of a 5-section stepped impedance lowpass filter having low impedance sections of 20 ohms and high impedance seetions of 100 ohms.

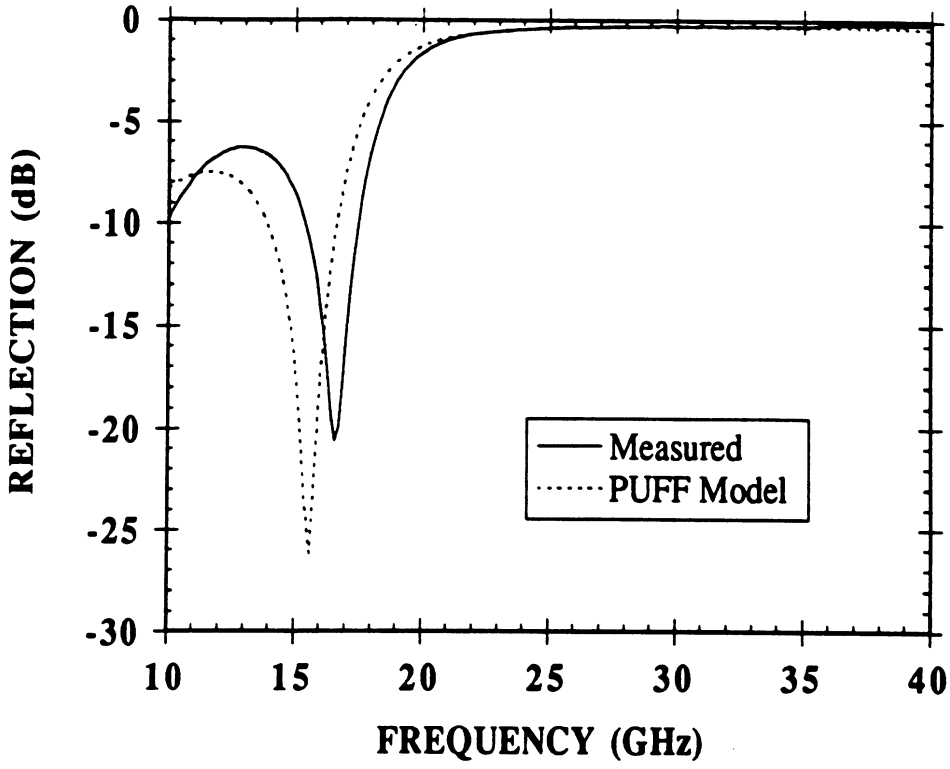


FIGURE 13. Comparison of reflection coefficient between the PUFF model and measured results for a 5-section stepped impedance lowpass filter.

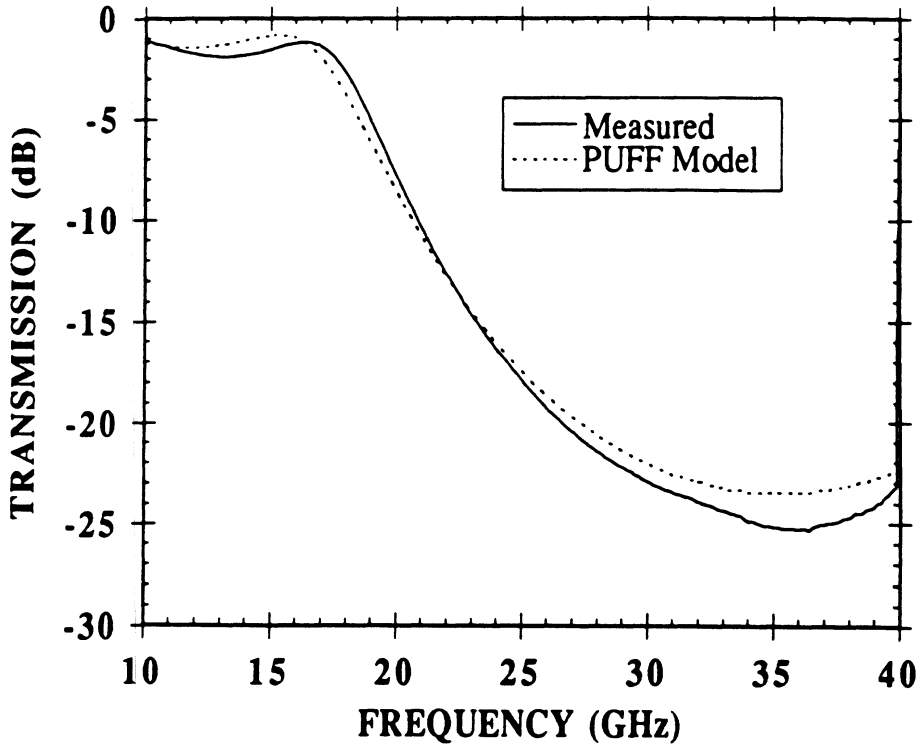


FIGURE 14. Comparison of transmission coefficient between the PUFF model and measured results for a 5-section stepped impedance lowpass filter.

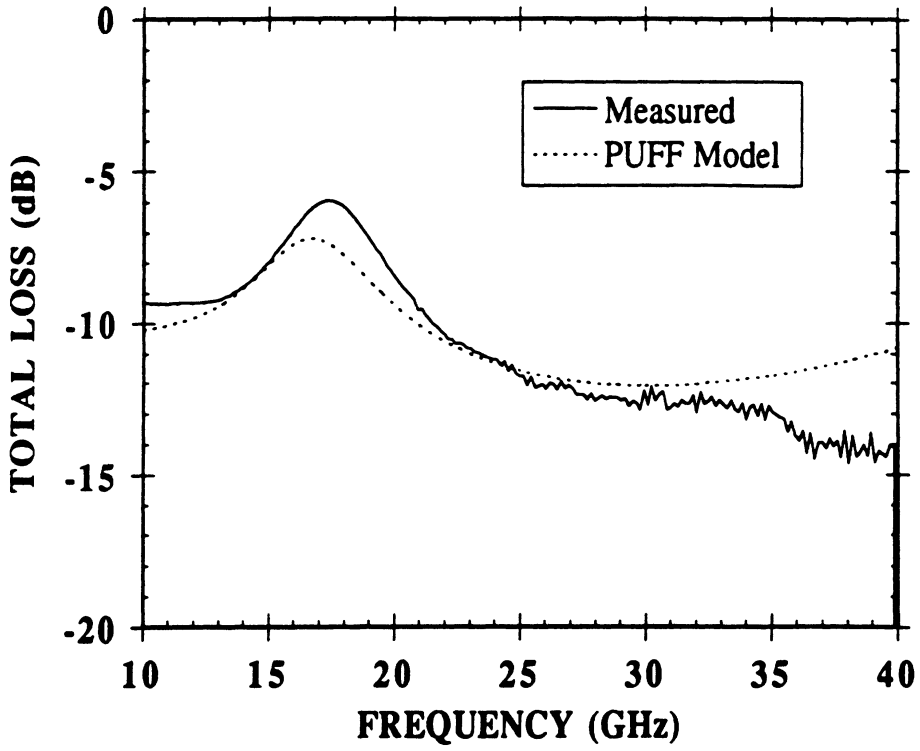


FIGURE 15. Loss comparison between the PUFF model and measured response for a 5-section stepped impedance lowpass filter.

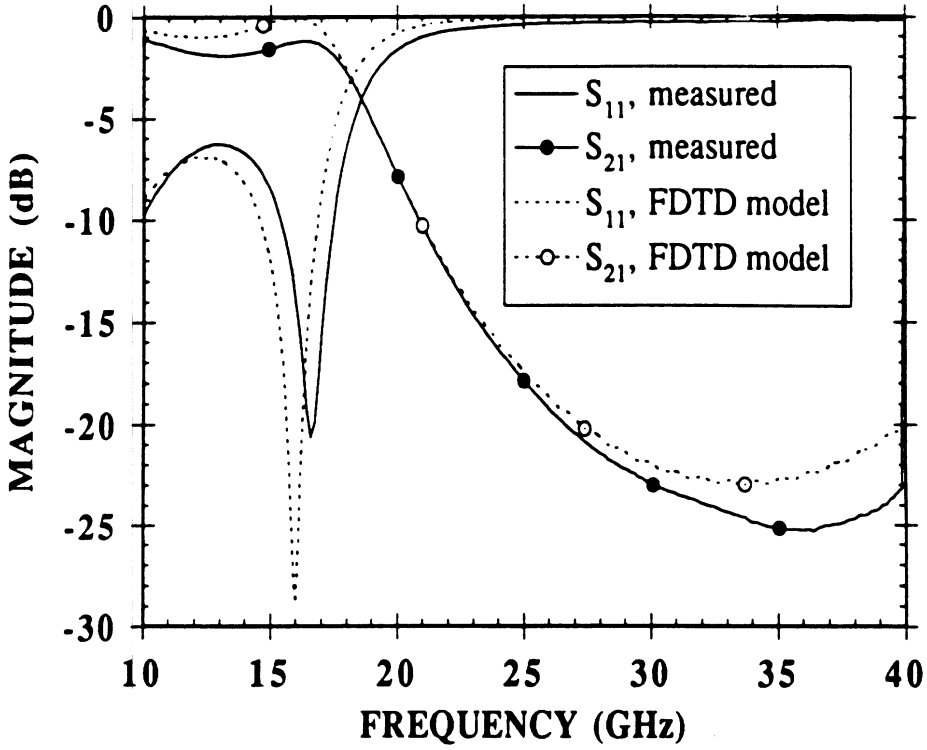


FIGURE 16. Comparison between the FDTD model and measured results for reflection (S11) and transmission (S21) coefficients of a 5-section stepped impedance lowpass filter.

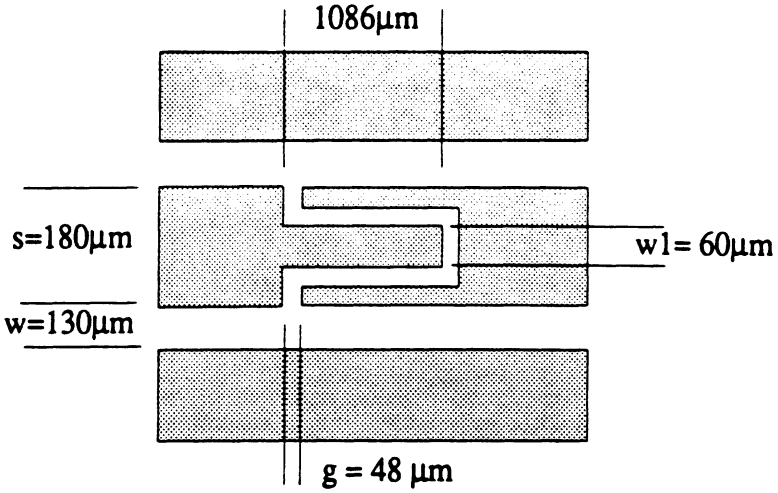


FIGURE 17. Series open-end tuning stub circuit dimensions.

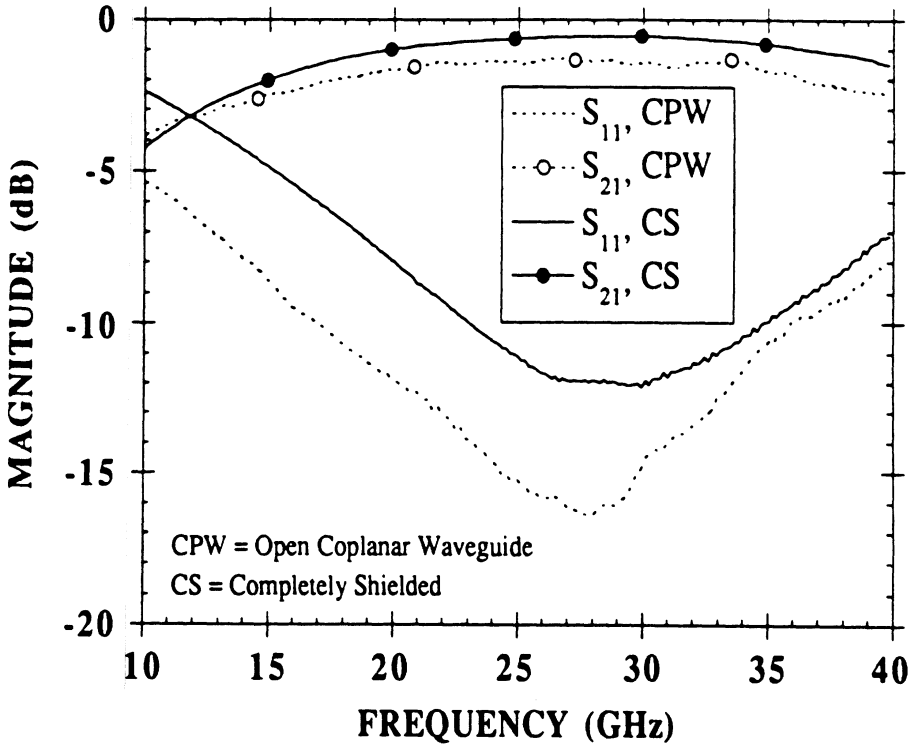
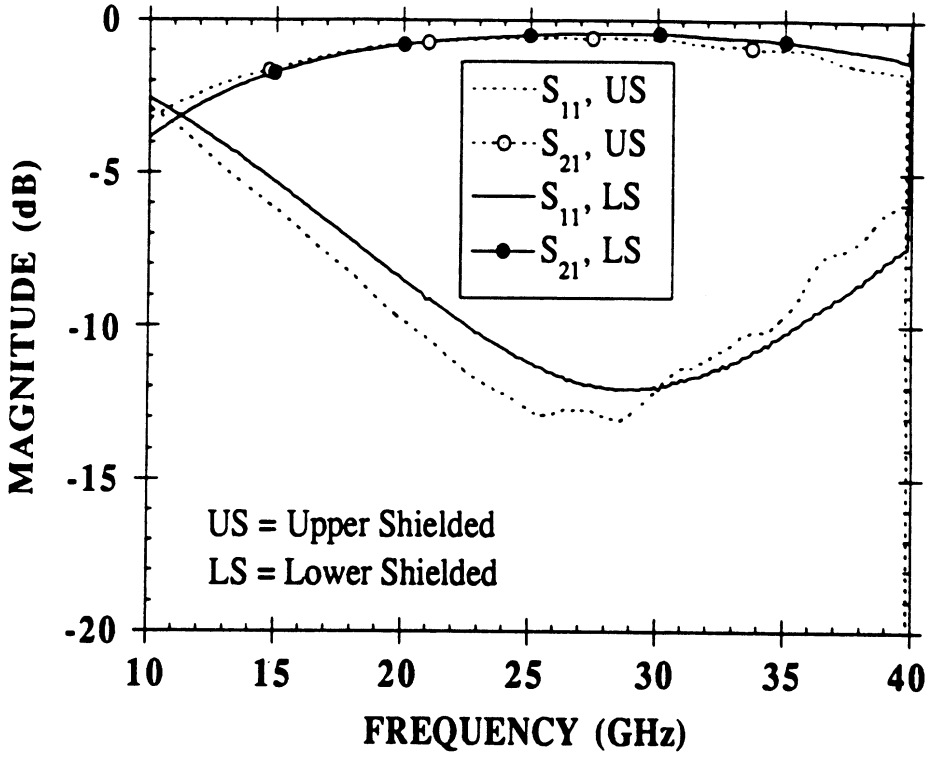


FIGURE 18. Comparison of reflection (S11) and transmission (S21) coefficients between open and completely shielded CPW environments of an open-end series stub.



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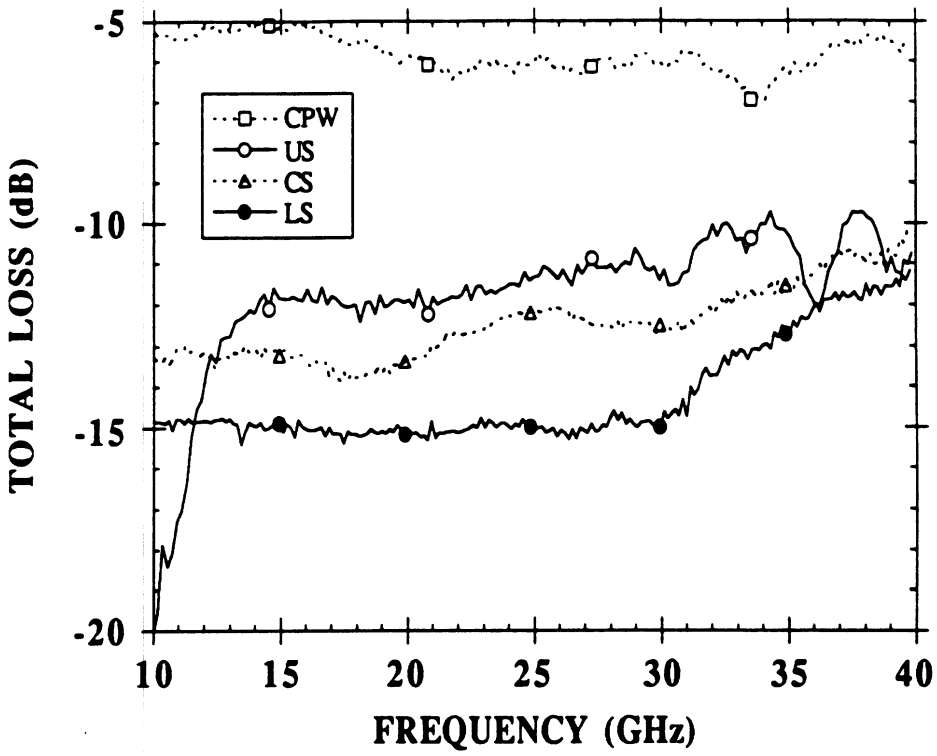

FIGURE 20. Loss comparison of an open-end series stub in open (CPW), upper (US), lower (LS) and completely shielded (CS) environments.

Micromachined Circuits for Millimeter- and Sub-millimeter-Wave Applications

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The University of Michigan
Ann Arbor, MI 48109-2122

Abstract

This article reviews recent developments in Si micromachining, as it applies to the design of millimeter- and sub-millimeter-wave circuits. Advances in semiconductor-processing techniques have made it possible to create monolithic geometries which are not bound to the surface of the wafer. These use a third dimension, to provide shapes and exhibit electrical functions, which are not possible through standard microstrip or coplanar-waveguide technologies. A variety of recently developed circuits are presented herein, which demonstrate the numerous capabilities micromachining offers to the circuit and antenna designer.

1. Introduction

Microwave and millimeter-wave planar-integrated circuits and antennas are the central nervous system in communication and radar systems. In the past decade, the microwave field has been experiencing a technological revolution due to advances in solid-state devices, insulating and semiconducting materials, and circuit-analysis techniques. Furthermore, the planarization of transmission lines to microstrip, stripline, or coplanar-waveguide form provides great flexibility in design, reduced weight and volume, and compatibility with active devices and radiating elements.

There are drawbacks to these planar geometries, however. These include frequency-dependent mechanisms, such as parasitic coupling and radiation, as well as increased ohmic loss, dielectric loss, and dispersion. These effects can seriously deteriorate electrical performance, and can lead to costly and time-intensive design cycles [1-2]. Suppression of some of these electromagnetic mechanisms, such as parasitic radiation and coupling, has led to improved performance, but requires very sophisticated packages, which add considerably to the volume, weight, and cost of the circuit [3-5]. Elimination of other deleterious effects, such as dispersion and high ohmic loss, which are inherent in conventional planar lines, will require fundamentally new approaches to planarization and circuit integration. This article addresses the development of relevant transmission-line technology, aimed at providing superior performance in the aforementioned respects.

Recent advances in semiconductor-processing techniques offer an historic opportunity to distinguish the monolithic from the planar character, and to provide integration along all the directions of three-dimensional space [9-13]. The capability to add one more dimension, and a few more parameters, in the circuit design, can lead to revolutionary geometries. These reduce ohmic loss and eliminate electromagnetic-parasitic effects, without affecting the monolithic character. Operating frequencies are thereby extended, and circuit and array performance are improved. A variety of monolithic, quasi-planar transmission-line geometries, which will support transverse-electromagnetic (TEM) wave propagation, can be developed using semiconductor micromachining. These lines are characterized by:

- Superior electrical performance
- Low weight and small volume
- Easy fabrication
- Great potential for low cost

The characteristics shown above may be prioritized according to pre-existing needs, resulting in a number of approaches which use micromachining for millimeter- and sub-millimeter-wave circuit design.

The evolution of micromachined circuits and antennas for these frequency ranges is still in its infancy. However, presented here is a description of recent accomplishments in this area, with emphasis on the effort performed at the University of Michigan. There are two techniques which have shown promise, and which have extensively used micromachining to realize novel circuits. The first utilizes a membrane-supported transmission-line configuration [9- 11], and has superior preformance as the highest priority. The second technique introduces new concepts in packaging for miniaturized circuits, using integrated-shielding cavities, and emphasizes size/volume/cost reduction [12-14]. The merits of each approach, in relation to electrical performance, fabrication, and compatibility, will be presented, and the impact of the newborn technologies on the state of the art will be discussed.

2. Membrane-supported circuit and antenna technology

Membrane-supported radiating elements, such as the integrated-horn antenna, were developed for the first time, in 1987, by G. M. Rebeiz and D. B. Rutledge. They have been researched, since 1988, at the University of Michigan, by G. M. Rebeiz and L. P. B. Katehi, under the support of the NASA Center for Space Terahertz Technology. During these past five years, antennas have been successfully used in a wide variety of applications, which cover the millimeter- and sub-millimeter-wave spectrum [6-8]. The fabrication of these radiating elements led to the establishment of a membrane technology which is reliable, repeatable, and easy to employ. In view of these capabilities, a membrane-supported transmission line, called microshield, was proposed at the 1991 MTT-S International Microwave Symposium [9]. The microshield, which is only one of the possible membrane-supported geometries, may be considered as an evolution of the conventional microstrip or coplanar waveguide. It is characterized by zero dielectric loss, very low radiation loss, reduced electromagnetic interference, and compatibility with conventional technologies, such as microstrip and coplanar waveguide. This transmission medium creates the basis of a new monolithic technology, which can provide generic

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designs appropriate for circuit and antenna applications in the millimeter- and sub-millimeter-wave region.

Membrane supported transmission lines are quasi-planar configurations, in which a pure, non-dispersive TEM wave is propagated through a two-conductor system, embedded in a homogeneous environment. Homogeneity of the environment can be accomplished by using a 1.5-mm-thick dielectric membrane, or a few-micron-thick diaphragm, to support the signal lines, while ground is provided by a metallized-micromachined cavity. This cavity is fabricated in Si wafers, using etchants such as KOH (potassium hydroxide) or EDP (ethylene diamine pyrocatechol), and is then metallized, using evaporation or plating. The signal lines are created by metal deposition on the membranes or diaphragms, or can be grafted onto the supporting structure by lift-off techniques. Similar processing methods are available for GaAs wafers. Due to the cavity shielding, and the pure TEM character of the propagating mode, these lines possess a large single-mode frequency band (DC to >1 THz), and have very low losses and zero signal dispersion. Consequently, circuit components made of these line geometries can provide electrical performance which is superior to those of conventional planar circuits.

The success of membrane-supported circuits relies on the development of thin-film dielectric membranes or diaphragms, which possess good electrical and mechanical properties. These thin-film layers are grown on Si or GaAs wafers, and are used to support the planar-conducting-strip lines. In view of the previously mentioned performance objectives, the thin films must have low losses at microwave and millimeter-wave frequencies, as well as compatibility with semiconducting and conducting materials. The mechanical considerations include reduced sensitivity to applied pressure and temperature variations, along with increased membrane or diaphragm sizes.

In the example circuits presented in this article, the membranes are in a tri-layer $SiO_2/Si_3N_4/SiO_2$ configuration, with constituent thicknesses of 7000, 3000, and 4000 Å, respectively. This size makes the membrane transparent to propagating signals at frequencies as high as 3 THz, and provides a near-homogeneous, air-filled environment to the propagating electromagnetic wave. This leads to very fast wave velocities, zero dispersion, and zero dielectric loss. The base layer (7000 Å) is grown using thermal oxidation, while the final two layers are formed using a chemical-vapor-deposition process. The effective dielectric constant of the 1.4-mm-thick membrane is approximately 4.9, using a simple averaging of the oxide ($\varepsilon_r = 3.9$) and nitride ($\varepsilon_r = 7.5$) layers. The material has very low loss from DC ($\rho > 10^{14}$ Ω-cm) to well into the THz frequency range. To date, membrane dimensions as large as 2.0 mm × 1.9 cm have been fabricated for use in microshield lines, with the average size being around 1.8 mm × 1.0 cm. The total fabrication yield on these membranes is greater than 95 percent.

As shown in Figure 1, various configurations of membrane lines may require the use of two or three wafers, to provide a cavity shield on one or both sides. This cavity shield is necessary for some uniplanar geometries, where multiple ground planes or other conductors are in close proximity to the signal line. Figure 1a shows a coplanar-stripline geometry, made of two high-resistivity <100> Si wafers, in which the electric field is confined to the surface area between the two strips. In this case, shielding by the cavity is not required and, depending on the application, the line may operate in a variety of environments [15, 16]. The geometry shown in Figure 1b, the microshield line, is a similar two-wafer

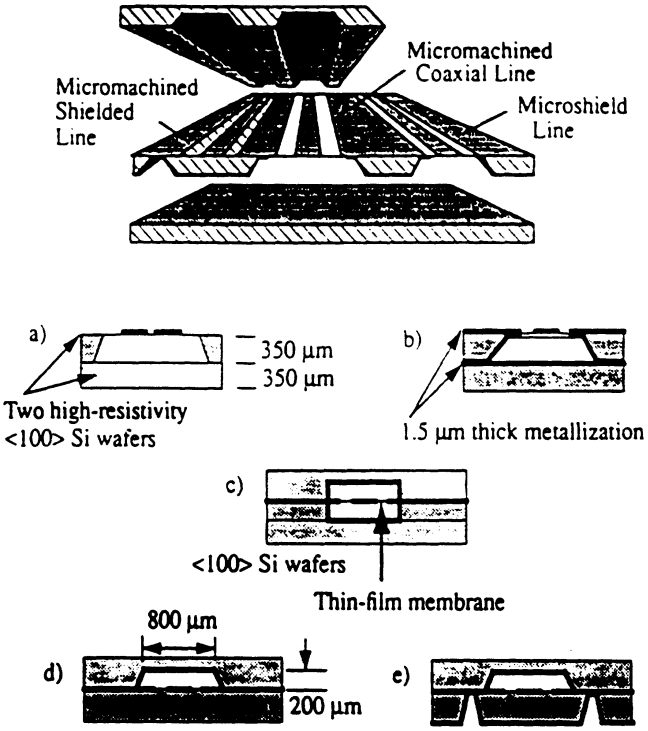
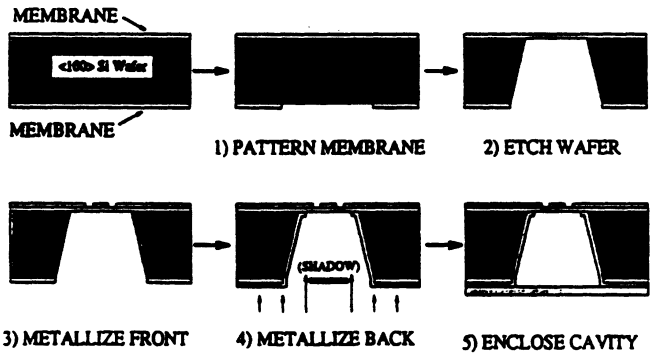


Figure 1. Illustrated here are five possible configurations of the micromachined quasi-planar transmission lines. The dimensions given are characteristic of lines designed to operate up to 40 GHz. The metallization, shown in black, is typically 1.5 microns thick. The line features will vary from 10 to 1000 microns.



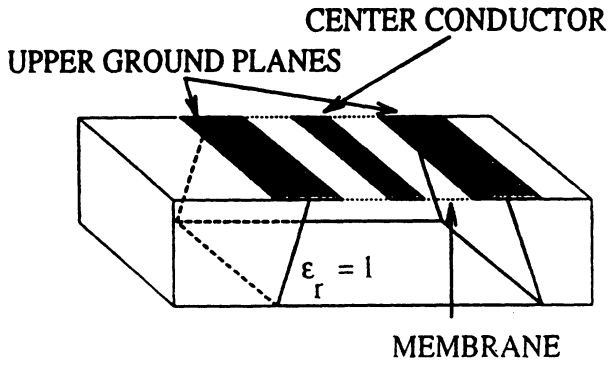


Figure 2. Fabrication process for a microshield transmission line.

arrangement, where the signal line, printed on a thin-film membrane or diaphragm, is shielded on one side by a metallized cavity. Here, the field is confined between the signal line and the metallized cavity on the lower side, while it is free to radiate in free space on the top side. Geometries of this form are very appropriate for monolithic antenna and receiver applications, where the feeding lines and other circuit components are printed on the same wafer. Figure 1c shows a three-wafer configuration made of <110> high-resistivity silicon wafers. In this structure, the signal line is shielded by a metallized cavity on both sides. Such a line suffers no radiation loss, and also retains the dispersionless characteristics mentioned above. A line of this type is a monolithic version of the coaxial line, and is expected to have very low propagation losses.

2. 1 Fabrication

The fabrication of the microshield line, shown in Figure 1b, begins with a Si wafer which has membrane layers on both sides. The membrane is a 1.4-mm-thick composite $SiO_2/Si_3N_4/SiO_2$ material which, as stated before, is grown using a combination of thermal oxidation and chemical-vapor-deposition processes. The transmission-line structure is formed by first removing photo-lithographically-defined regions from the membrane layer on the back side of the wafer. This pattern serves as an etch mask, allowing pyramidal cavities to be opened in the wafer using anisotropic Si etchants, such as ethylene diamine pyrocatechol (EDP) or potassium hydroxide (KOH). When the wafer has been etched through to the front side, the upper-membrane layer will behave as an etch stop, thereby forming the exposed membrane surface with surrounding silicon walls below (see Figure 2). The final step in the fabrication process is the metallization of the line pattern on the upper-membrane surface, and of the cavity sidewalls underneath. A photoresist lift-off technique, with metal evaporation, is used to deposit the circuit pattern on the top side of the membrane layer. Evaporation is also used for metal deposition from the back side onto the cavity sidewalls, but here some shadowing is required, to protect selected areas of the membrane from metallization. A diced or micromachined silicon mask is used to shield the region between the inner edges of the upper ground planes and the center conductor, thus preventing metallization of the membrane below the slots. The finished circuit is then mounted on a ground plane, to fully enclose the lower shielding cavity. Typical cavity dimensions for circuits designed for the 10-40 GHz range are 355 μm high by 1000-2000 μm wide. These dimensions are reduced as the operating frequency increases. The slot- and signal-line widths will vary, depending on the desired characteristic impedance level of the transmission line, but generally range from 10 μm to 1 mm.

2.2 Measurements

The procedure described above has been used to design and fabricate very-low-loss, ultra-fast lines, and high-performance circuits. Recent measurements have shown astonishing performance.

2.2.1 Loss measurements

Loss measurements on membrane-coupled strips (MCS) and membrane-coplanar waveguide (MCW) were performed, using electro-optic sampling from 50 GHz to 500 GHz [15-16]. In order to generate and measure electrical pulses having picosecond duration, the optoelectronic technique of photoconductive switching, along with a sub-picosecond-temporal-resolution electro-optic sampling characterization system have been employed

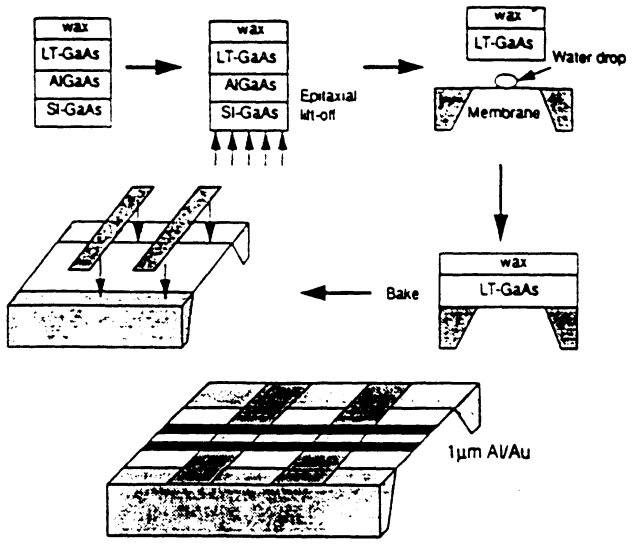


Figure 3. Major steps in the preparation of coupled strip lines for electro-optic sampling experiments. A low-temperature GaAs (LT-GaAs) layer is removed from its substrate support, and attached to the membrane using van der Walls forces. The metal lines are then printed over the LT-GaAs slices.

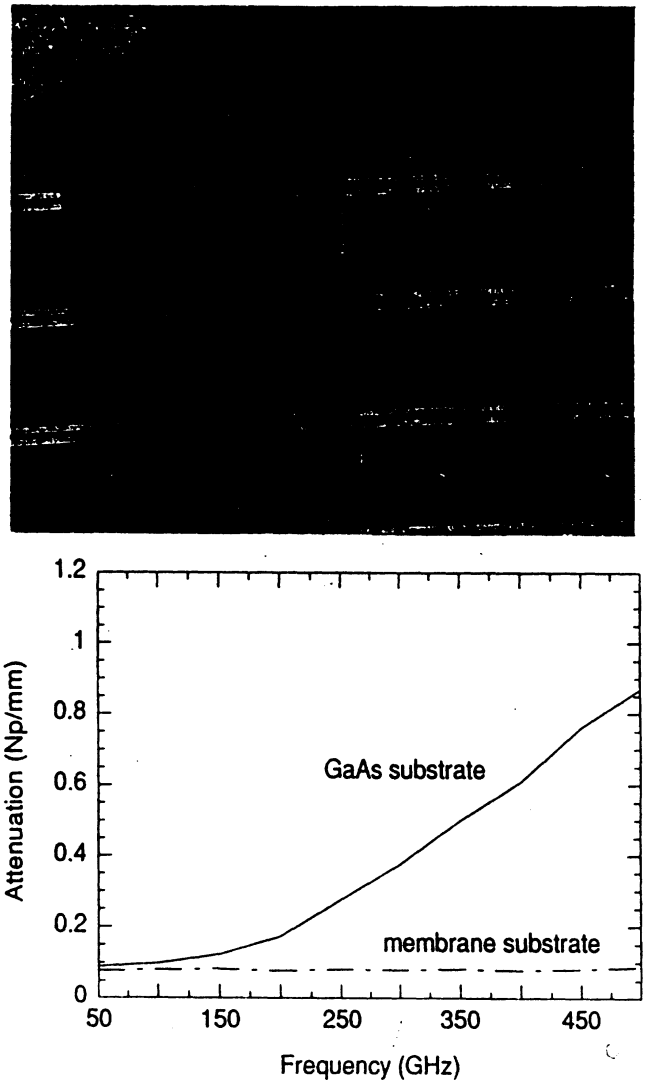


Figure 4. A photograph of multiple membrane-coupled strip (MCS) lines, which cross two LT-GaAs slices and are supported by the 1.5-micron-thick membrane (dark area). Also shown are loss measurements using electro-optic sampling on lines with GaAs and membrane substrates.

Pulse	1mm	3mm	5mm
Rise Time	0.72ps	0.84ps	0.76ps
FWHM	1.16ps	1.16ps	1.21ps

*Measurement error: 0.07ps

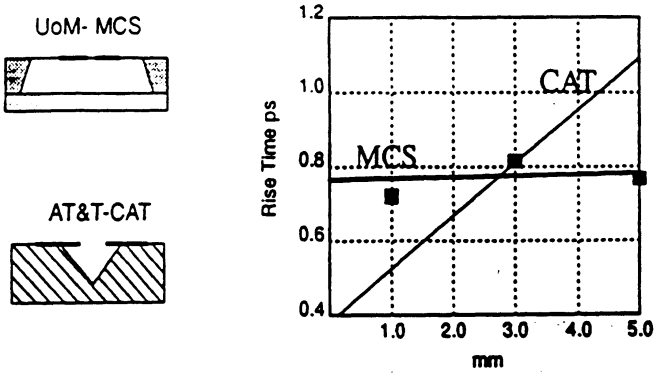


Figure 5. Pulse rise-time vs. distance for the MCS line and the CAT line.

[11, 15]. For the measurement of transients in the time domain, reflections from any source near the probing point will cause a loss of accuracy in the acquisition of clean, easily analyzed signals. Therefore, it was necessary to integrate a 200-μm-wide photoconductive-generator patch with the signal lines, which are fabricated on the membrane. The sub-picosecond-lifetime photoconductor employed was a 1-μm-thick layer of GaAs, grown by molecular-beam epitaxy at the low substrate temperature of ~200°C (known as LT-GaAs). This photoconductor was lifted off its substrate, through etching techniques, to form a free-standing film supported on a wax layer, and was then grafted to the membrane substrate using van der Walls bonding techniques [20]. The MCS was then defined on the membrane using standard photolithographic techniques, as summarized in Figure 3.

Figure 4 shows the total loss, in Np/mm, from 50 GHz to 500 GHz, for a coupled stripline ($w = s = 20$ μm) printed on a 100-micron-thick GaAs substrate (—), and supported by a dielectric membrane (——). The picture of multiple MCS lines, included in the figure, clearly shows the well-defined boundaries of the dielectric membrane, and the two vertically-oriented LT-GaAs patches, which are under the lines. These experimental results confirm the low-loss behavior of MCS, and the superiority of this transmission line over conventional substrate-printed lines.

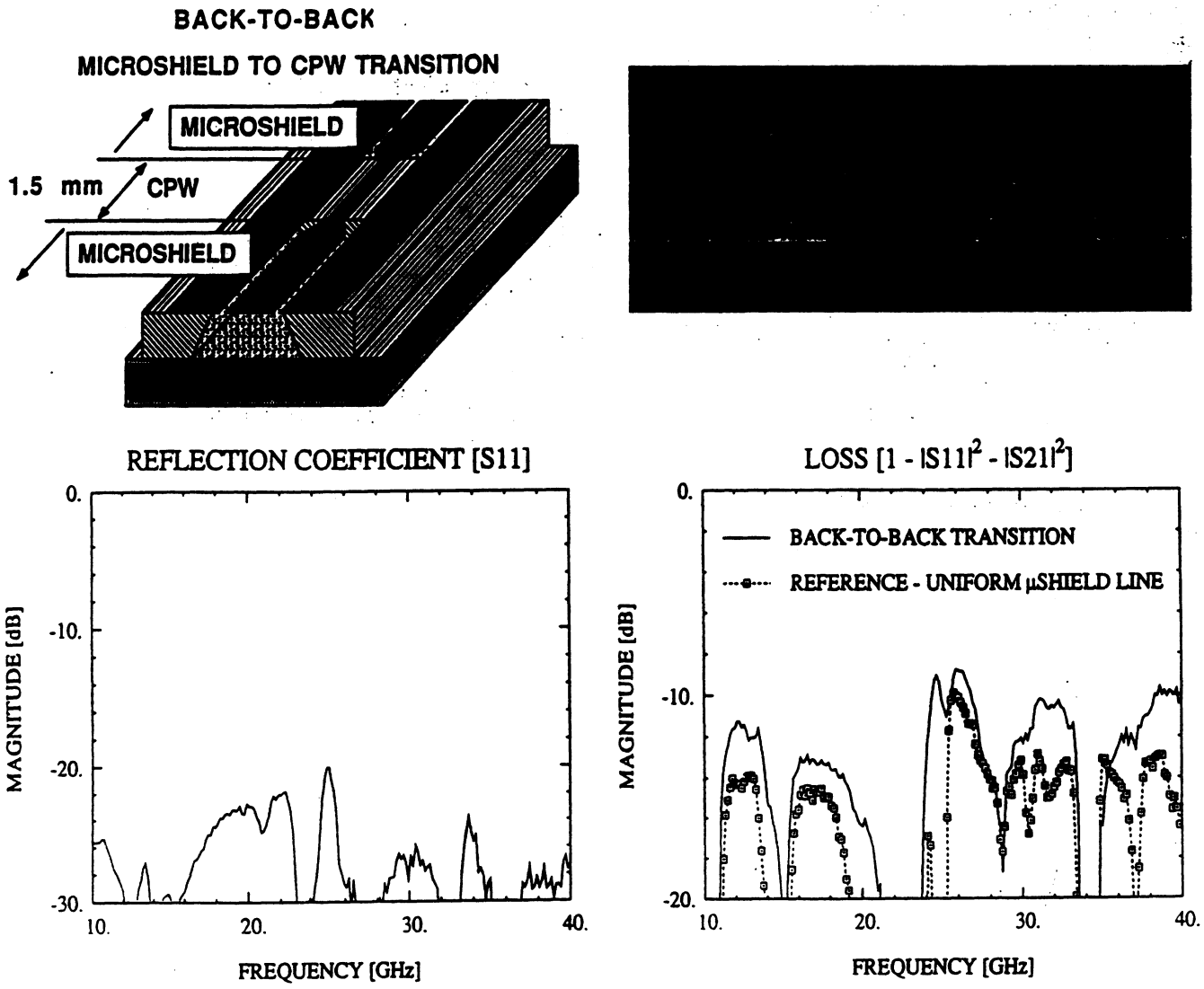


Figure 6. A diagram of a back-to-back microshield-to-coplanar-waveguide (CPW) transition. The photograph shows the back side of the circuit, with the ground plane removed. The middle CPW section is 1.5 long. Also shown are the measured S_{11} values, and the total loss performance.

In Figure 5, the measured pulse risetime vs. distance, for the same membrane lines, shows negligible dispersion, compared to recently published results for the coplanar air transmission line (CAT) The CAT, which was developed at AT&T, was considered to be the fastest transmission-line geometry available to date. The measured results shown in Figures 4 and 5, however, indicate that the membrane-supported line has the lowest loss and fastest phase velocity of any monolithic transmission line ever built

2.2.2 CPW-to-microshield transition

The primary motivation for designing a CPW-to-microshield transition lies in the interest of using membrane geometries as part of a complex monolithic circuit, which combines a variety of uniplanar technologies. Figure 6 shows the measured performance of a back-to-back transition, from 10 GHz to 40 GHz. This transition has been designed in such a way as to preserve the form of the field, and to equalize the characteristic impedance in the different lines. As a result, from 10 to 40 GHz, the reflection (S_{11}) is below -22 dB and the total loss, ($1-|S_{11}|^2-|S_{21}|^2$), is less than -10 dB [10, 17]. Note that these data include the effects of two transitions and a connecting section of line. This performance clearly demonstrates the ability to achieve low-loss CPW/microshield integration in millimeter-wave applications.

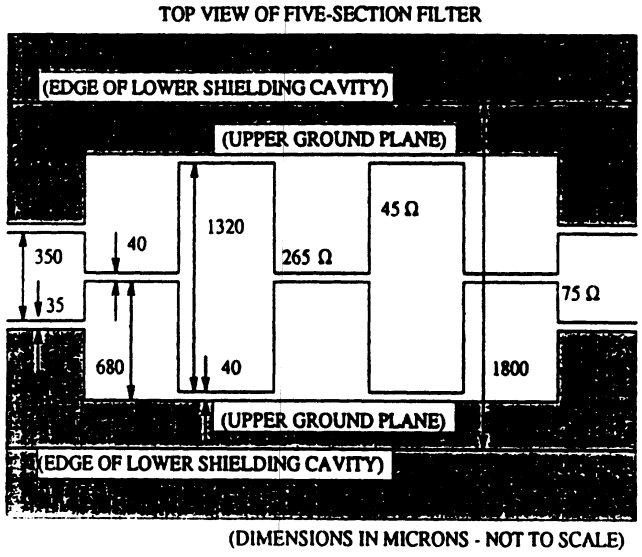


Figure 7. A schematic diagram of a microshield five-section stepped-impedance filter. The photograph shows a thru-line (top) and a 5- and a 7-section filter.

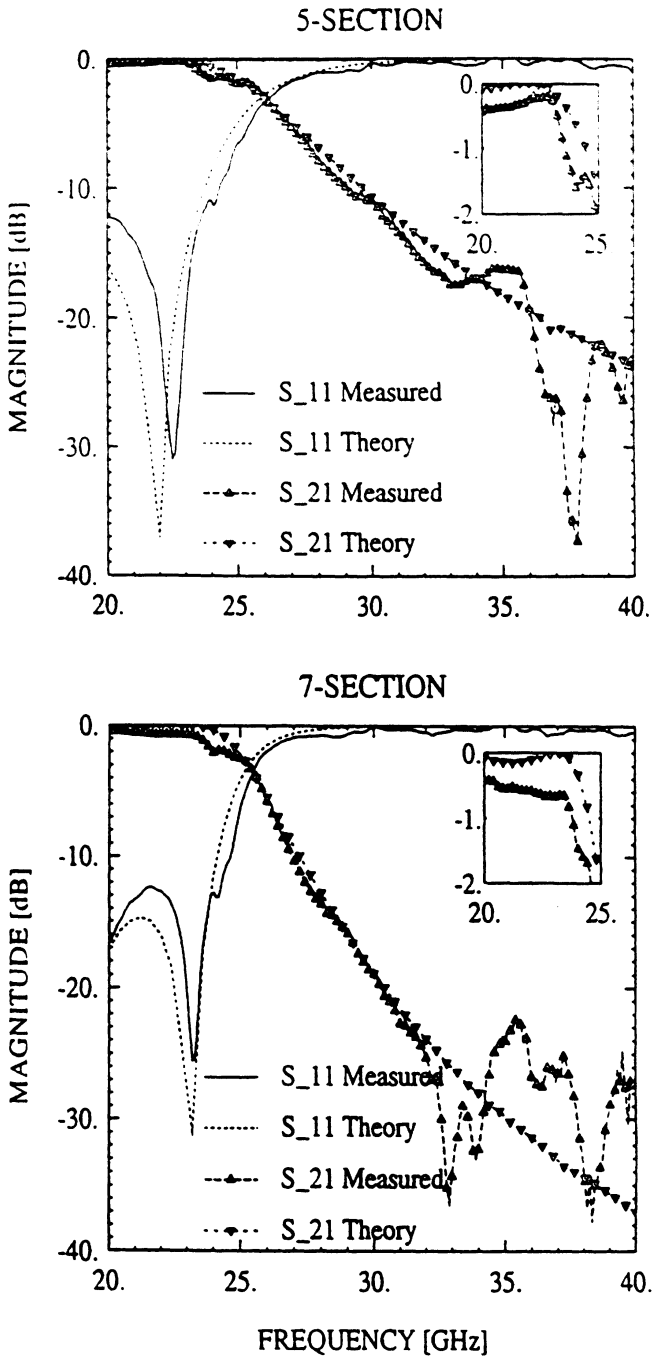


Figure 8. The measured and theoretical response of five- and seven-section microshield low-pass filters.

2.2.3 Microshield stepped-impedance low-pass filters

Stepped-impedance filters are commonly used for applications which do not require a sharp cutoff, such as in the rejection of out-of-band mixer harmonics. Illustrated in Figure 7 is a schematic of a five-section 0.5 dB-ripple Chebyshev filter, which has been fabricated and tested. Also shown is a photograph of a microshield thru-line (top), and both a five- and a seven-section low-pass filter. The measured performance of these filters is shown in Figure 8 [10, 17], along with the theoretical response which was obtained using

ideal-transmission-line theory[1]. The agreement between the experimental and theoretical data is quite good, and the performance illustrates the potential for low-loss microshield circuit components.

3. Micromachined quasi-planar circuits

Micromachining may also be used effectively to develop miniaturized circuits, in which the package has been fabricated and integrated with the rest of the circuitry. Circuit design requires the use of two silicon wafers, one of which has upper-half shielding cavities that have been etched anisotropically, while the other wafer has the planar circuits that have been printed using photolithographic techniques, with or without the lower cavities (see Figures 1d, 1e) [12, 14].

3.1 Fabrication

Micromachined circuits, consisting of conducting lines and metallized cavities, are developed in two stages, using a two-wafer system. In this section, a comprehensive discussion of the fabrication of upper-half-shielded (Figure 1d) as well as completely-shielded (Figure 1e) micromachined circuits is presented.

In order to provide a shielded environment in the upper-half region of the planar lines, cavities and alignment marks are created on a low-resistivity Si wafer (385 μm) having a 1.4-μm-thick, tri-layer dielectric mask, consisting of $SiO_2/Si_3N_4/SiO_2$. The alignment marks are etched completely through the wafer. However, the cavity heights are less than the total wafer thickness, thus requiring a separate etch depth. To prepare the wafer for the anisotropic etching in these areas, the etch pattern is first defined in the tri-layer mask, using standard photolithographic techniques. Removal of the mask requires the use of buffered HF, and a plasma etcher for the upper oxide and nitride layers, respectively. The wafer is then repatriated to expose and remove the lower oxide only in the alignment-mark pattern, while preserving the oxide mask in the cavity areas. Using the tri-layer as a mask for the anisotropic etchants, KOH or EDP, an initial depth is obtained for the alignment marks. Next, the remaining oxide in the cavity areas is removed, using buffered HF, and the wafer is then etched to produce both the alignment windows, which extend vertically through the wafer, and the desired cavity depth. Finally, the cavity regions are metallized using evaporation techniques.

For the upper-half-shielded circuits, planar lines are defined on a high-resistivity Si wafer using standard photolithographic and metal-evaporation techniques. The upper cavity is then aligned to the planar circuits via microscope, and the two wafers are attached using regular adhesion methods or Si-to-Si electrobonding. A similar procedure is followed for completely-shielded circuits which incorporate cavities beneath the planar lines. Prior to the planar-line metallization, however, cavity sidewalls are established by anisotropically etching grooves on the backside of the high-resistivity wafer. This wafer is subsequently metallized from the back, to complete the lower-side shielding. The fabrication process for both upper-half and completely-shielded circuits is illustrated in Figure 9.

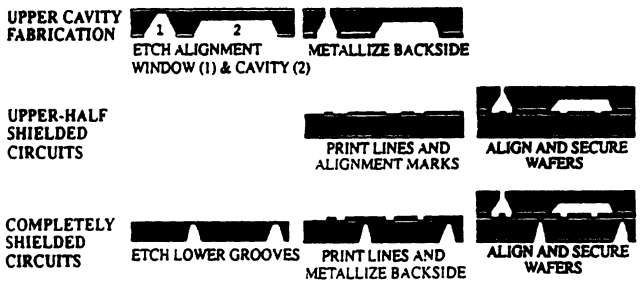


Figure 9. The development of micromachined shielded circuits.

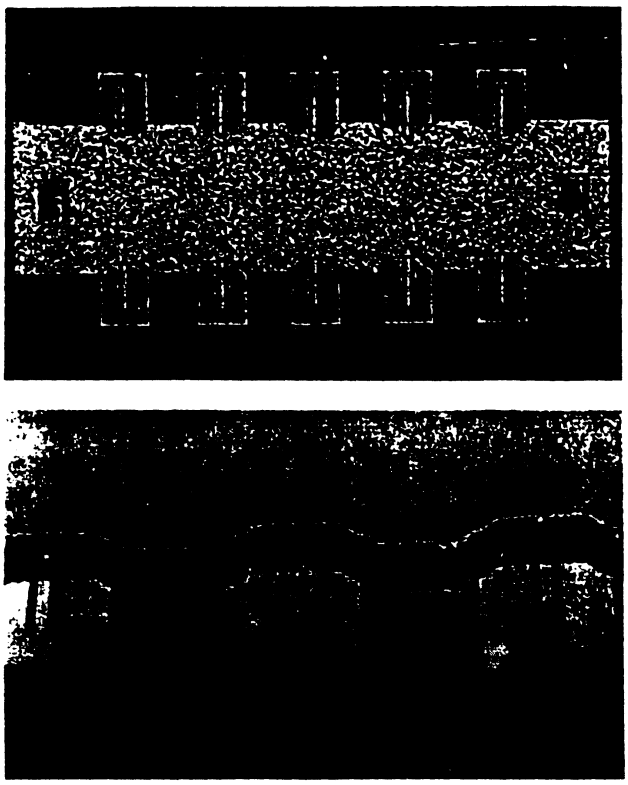


Figure 10. Photographs of micromachined shielded circuits. (a) A top view of five upper-half-shielded circuits, with alignment marks on the far left and right sides. (b) A close-up view of three circuits with the shielding in place.

3.2 Measurements

As with the membrane-supported circuits, the micromachined shielded circuits are measured using an HP 8510B Network Analyzer system, which operates at frequencies up to 40 GHz. Measurements are obtained from Cascade Microtech high-frequency GSG probes, via an Alessi probe station. In order to suppress parallel-plate and microstrip modes between the circuits and the wafer chuck of the probe station, the circuit wafer is placed on 1/8" thick 5880 RT/Duroid, with $\varepsilon_r = 2.2$. The thru-reflect-line (TRL) calibration is performed, to eliminate the effects of connectors, cables, and probes from the measured data, and to accurately establish a known reference plane. After calibrating, scattering-parameter measurements of the circuits are obtained, to compare theoretical and experimental data.

The circuits described here are shielded by miniature micromachined cavities in the upper-half region, which are 800 μm wide and 200 μm high, as shown in Figure 1d. Each circuit is fed by open coplanar waveguide, which serves as a transition from the

[1]The theoretical data include quasi-static corrections for the line-length extension at impedance steps [18].

GSG probes to the actual micromachined circuit (see Figure 10). Initial characterization of these lines was obtained by measuring the scattering parameters of a delay line. Figure 11 shows that the total loss of the line is about 0.08 dB per guided wavelength, λ_g. Additional circuits have also been measured as part of this effort, including an open-end series stub, designed to resonate at 30 GHz, and an open-end gap (see Figures 12a, 12b). Figure 13 shows a comparison between experimental data for these circuits, and theoretical results which were derived using a full-wave space-domain integral-equation method [19]. The discrepancy between theory and experiment is due to the fact that the theoretical data assume completely shielded and lossless circuits, while the experiments have been performed on upper-half-shielded circuits, with ohmic losses and radiation losses present.

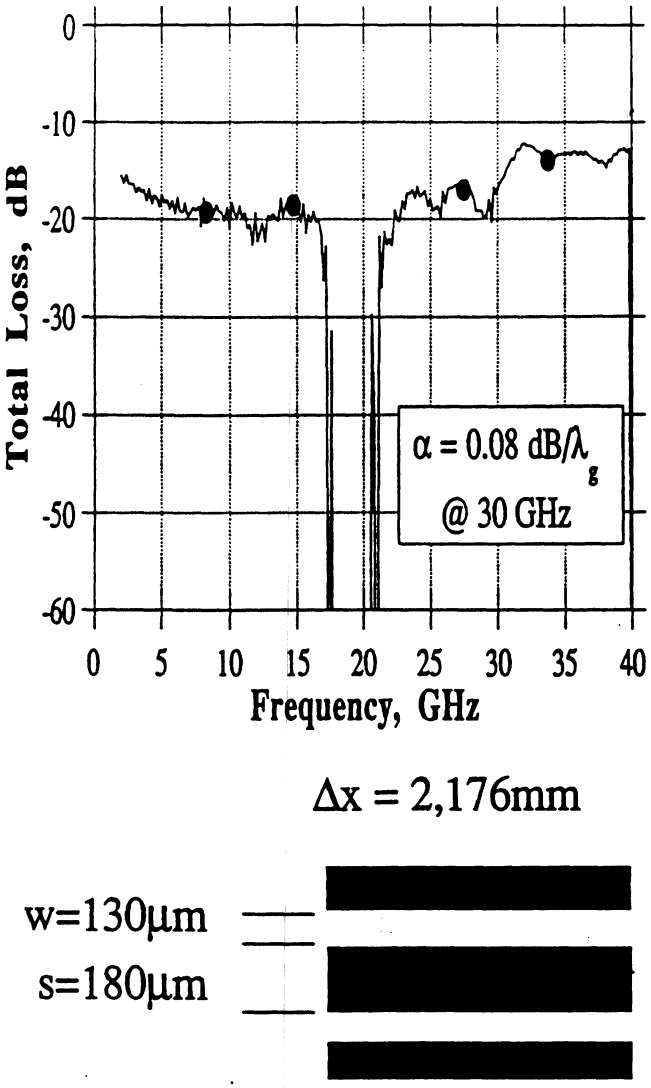


Figure 11. The delay-line characteristics for upper-half-shielded micromachined circuits.

The measured total loss for the open-end series stub and open-end gap, implemented in both CPW and the upper-half-shielded micromachined line, is given in Figure 14. The data show that the total loss is 3 dB lower for the micromachined circuits, from 10 GHz to 40 GHz. This reduction is due to lower parasitic radiation, and it emphasizes the effectiveness of the integrated cavity. Even further reduction of the loss is expected for the completely shielded micromachined circuits, which are presently in development at the Radiation Laboratory of the University of Michigan.

4. Conclusions

Two approaches for the development of micromachined circuits for millimeter- and sub-millimeter-wave applications have been discussed. These new technologies provide a means to overcome the drawbacks typically associated with conventional planar-transmission lines, such as microstrip and coplanar waveguide. The examples shown demonstrate the use of micromachining to effectively incorporate a third dimension into the geometry of monolithic circuits, thus introducing additional parameters in the design, and resulting in structures with superior electrical performance (membrane-supported circuits), and reduced volume and weight (micromachined-shielded circuits). The membrane-coupled strip (MCS) line, for example, has been experimentally verified as the fastest monolithic transmission line to date, and has demonstrated extremely low propagation losses up to 500 GHz. High-performance circuit components, such as low-pass filters, have also been fabricated using the microshield configuration, and low-loss integration of this line with conventional coplanar waveguide has been achieved. Finally, micromachined circuits, which incorporate miniaturized shielding packages in a monolithic design, have been described. Preformance of these circuits shows that the low-volume, low-weight packaging is effective in reducing signal loss, without degrading the desired frequency response.

The capabilities of micromachining certainly extend beyond the limited number of applications presented in this article. The recent advances in Si and GaAs processes allow us to extend circuit

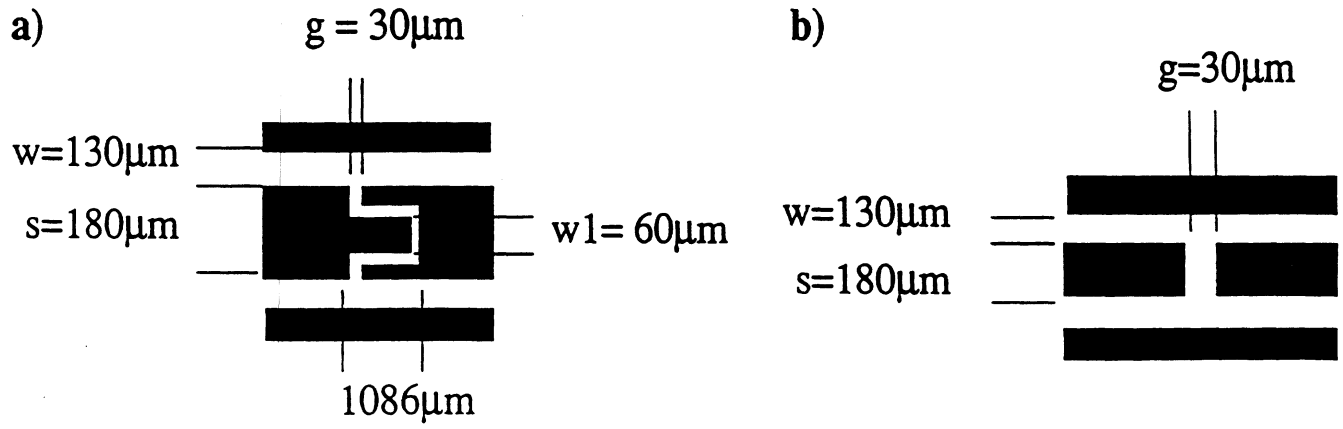


Figure 12. Circuit descriptions for (a) an open-end series stub and (b) an open-end gap.

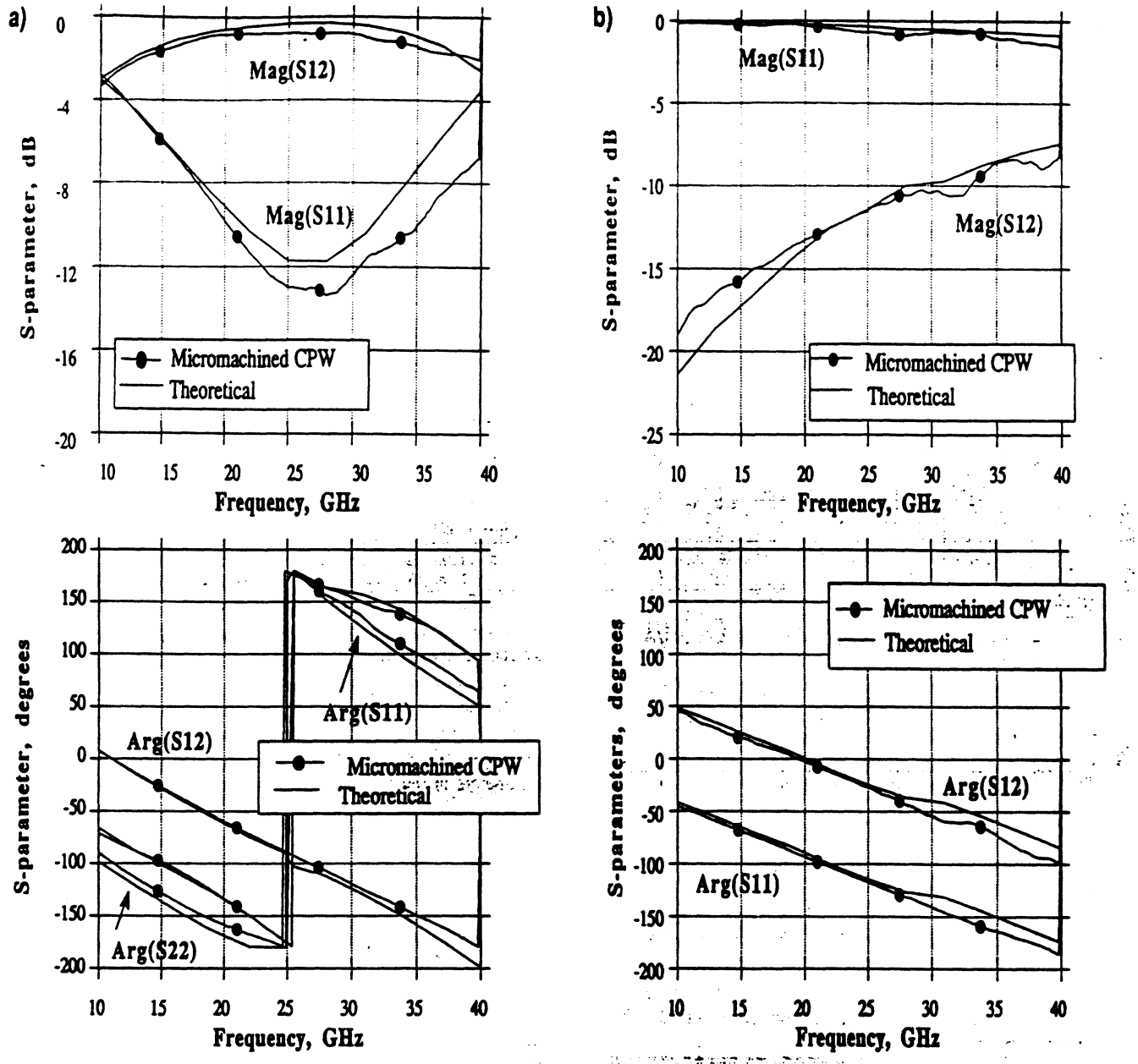


Figure 13. Comparisons of theoretical and experimental data for upper-half-shielded micromachined circuits. (a) Open-end series stub; (b) open-end gap.

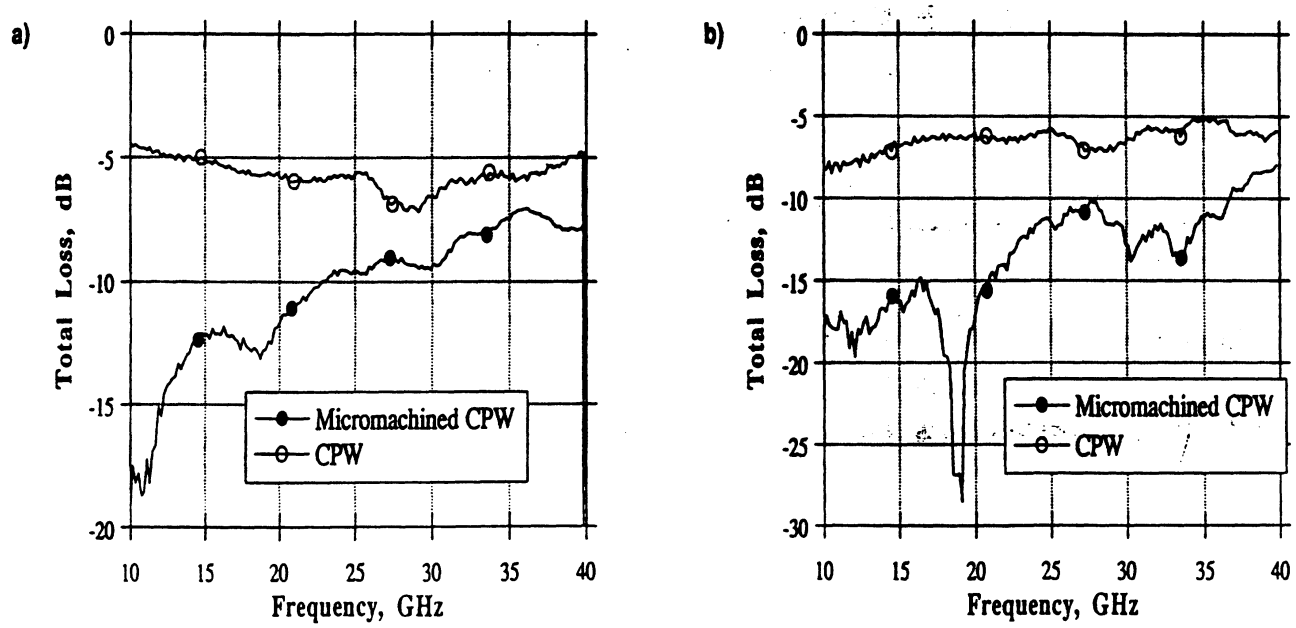


Figure 14. The total loss for micromachined circuits versus CPW. (a) Open-end series stub; (b) open-end gap.

geometries beyond single planes in novel ways, and to investigate techniques to improve current millimeter- and sub-millimeter-wave systems by reducing size and cost, and by providing superior performance. Similar opportunities exist to experiment with configurations that can provide new functions, and introduce new concepts in circuit design.

5. Acknowledgments

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High Performance Microshield Line Components

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Abstract

Several millimeter-wave passive components have been fabricated using the microshield transmission line geometry, and their performance is presented herein. Microshield is a quasi-planar, half-shielded design which uses a thin dielectric membrane (1.5 μm) to support the conducting lines. This approach provides a nearly homogeneous, air-filled environment and thus allows extremely broad-band TEM operation. The paper examines the conductor loss and effective dielectric constant of microshield lines and presents results on transitions to conventional coplanar waveguide, right-angle bends, different stub configurations, and lowpass and bandpass filters. Experimental data is provided along with numerical results derived from an integral equation method. The microshield line is shown to be very suitable for high performance millimeter- and submillimeter-wave applications.

I. INTRODUCTION

The microshield line was introduced in 1991 [1] as an alternative transmission medium to coplanar waveguide for millimeter- and submillimeter-wave applications. It is a partially shielded, quasi-planar transmission line in which the center conductor and upper ground planes are surrounded by air and supported by a 1.5 μm-thick dielectric membrane, as shown in Figures 1 and 2. This configuration allows single-mode, TEM wave propagation over a very broad bandwidth with minimal dispersion and zero dielectric loss. Furthermore,

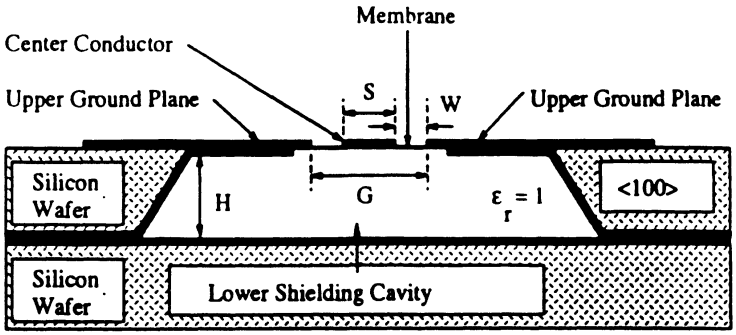


Figure 1: The microshield transmission line geometry (not to scale). The dark lines indicate metallization, which is typically 1-2 microns thick.

the metallized lower shielding cavity minimizes signal cross-talk between adjacent lines and eliminates radiation into parasitic substrate modes. A description of these and other advantages of the microshield geometry can be found in previous communications [2, 3, 4], along with a summary of the fabrication process.

The objective of this paper is to present results from a detailed study which emphasizes microshield circuit design and measurement in the 10-40 GHz frequency range. An important part of the project has been the development of a good transition between the microshield line and the measurement probe contact pads, which must be printed on the surrounding high-resistivity silicon substrate for mechanical support. This transition is covered in detail in section II. The conductor loss of microshield, discussed in section III, has been measured on lines of different aspect ratios and values as low as 0.03 dB/mm at 35 GHz have been obtained. These results demonstrate the potential for low-loss, millimeter-wave interconnect lines and passive circuit elements. The data are also consistent with the findings from recent opto-electronic sampling experiments, in which low-loss signal propagation on membrane lines was measured up to 1 THz, well beyond the upper frequency limits of similar GaAs and quartz supported lines [5]. In Section IV, some of the advantages offered by the very low effective dielectric constant of the microshield line are covered. The performance of several microshield circuits such as transitions to cpw lines, right-angle bends, series stubs, lowpass filters, and bandpass filters is presented in Section V.

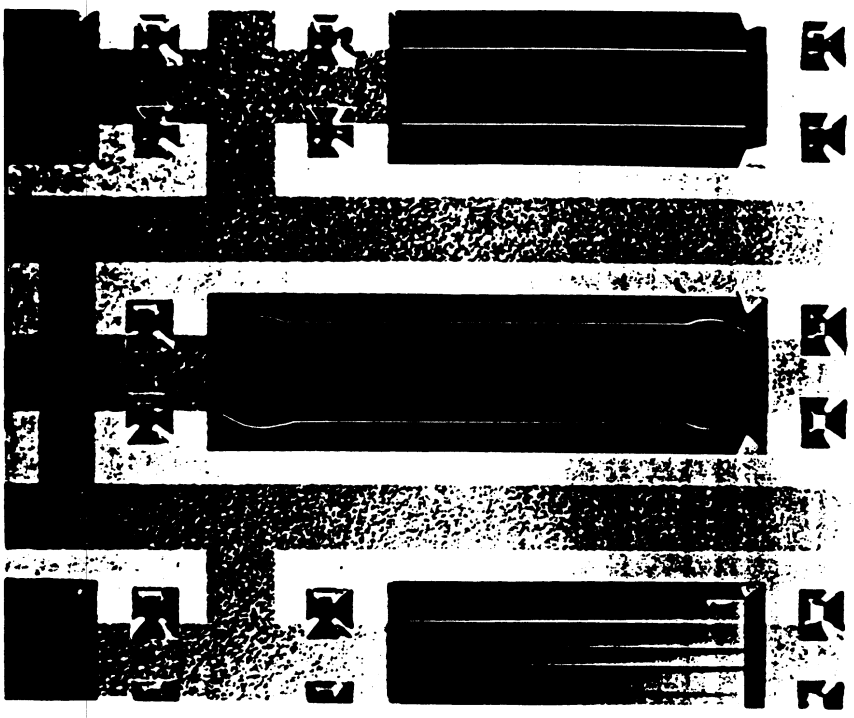


Figure 2: Photograph of the backside of a wafer, shown with the ground plane removed. The circuit in the center is a 5-section stepped-impedance lowpass filter (refer to Figure 15).

A theoretical analysis is provided as a validation of the measurements and also as a means to predict the performance beyond the 40 GHz limit of the measurement setup. The theory involves a full-wave analysis which is based on a space domain integral equation (SDIE), similar to that described in [6] but capable of analyzing non-shielded geometries. The SDIE is derived by replacing the slots in the metallization by fictitious metal surfaces, and then imposing magnetic currents on the surfaces which must satisfy the field continuity conditions. The method of moments is used to discretize the integral equation and solve for the magnetic currents, or electric fields, in the slots, from which the scattering parameters can be determined. It is assumed that all conductors are infinitely thin and perfectly conducting, and that the shape of the lower shielding cavity is rectangular. In addition, the effect of the thin membrane layer is approximated by assuming that the lower cavity is homogeneously filled with a material which has a dielectric constant slightly greater than 1 (see section IV).

In this paper it is shown that the characteristics of the microshield line are well-suited for specialized millimeter-wave and submillimeter-wave applications. Obviously, integrating the thin dielectric membrane on silicon or GaAs substrates requires additional steps in the fabrication process, but in many cases this is offset by eliminating the procedures for air-bridges and substrate thinning. Furthermore, the circuit yield is very high, exceeding 95% in a research laboratory, and the substrate etch can be one of the last steps in the process, thereby increasing yield. These factors, combined with the very broad-band, low-loss performance, make microshield a viable transmission line option for systems operating at mm-wave frequencies.

II. MEASUREMENT AND SYSTEM CALIBRATION

In this section the measurement setup is described along with some details regarding the line standards needed for calibration. The measurements are made using a microwave probe station and an HP 8510B vector network analyzer. Since the membranes cannot withstand repeated probe contact, the contact pads are made with grounded coplanar waveguide (gcpw) on the silicon substrate, and a transition is made onto the microshield line. The conductor-

backing of the cpw pads is a continuation of the ground plane which completes the lower shielding of the microshield. A one-tier TRL technique [7] is utilized to calibrate to reference planes which are on the microshield line.

It was found that the geometry of the probe contact pads and the transition section have an important effect on the quality of the calibration. The initial design, shown in Figure 3, consisted of 55Ω gcpw contact pads followed by a 735 μm long gcpw impedance matching section. This configuration was intended to act as a low-loss transition to the 75Ω microshield line, the effects of which could be removed with the TRL calibration. Even though the non-calibrated return loss from the thru and delay lines was consistently better than 12 dB, the performance of this design was rather poor and the repeatability suffered due to unwanted interaction between the calibration lines and nearby circuits. Typical results for the calibrated insertion loss of a microshield delay line are also shown in Figure 3.

The cause of the measurement errors is the leakage of power into undesired substrate modes along the length of grounded cpw line, which cannot be accounted for correctly using the standard HP 8510B TRL calibration software. The discontinuities at the probe contact pads, impedance steps, and the end of the microshield cavity are all possible sources of excitation for undesired parallel plate modes and TM_n and TE_n surface waves [8]-[16]. Also, as reported in [12], the finite lateral extent of the ground planes can result in distinctly predictable resonances in gcpw delay lines.

The leakage mechanism associated with the transition in Figure 3 exhibits a consistent structure across the 20-40 GHz band, apart from the sharp resonance seen around 35 GHz. The circuit dimensions suggest that the primary problem is leakage into the TEM parallel plate mode [10]. Different authors have shown that the ground plane spacing (S+2W) must be kept small compared to the ground plane width, G, and the substrate height, H, in order to maintain propagation in the cpw-like mode [13, 15, 16]. Furthermore, since the power leakage increases with distance, a shorter length of gcpw between the probe contact pads and the microshield line will also reduce this problem. One way to eliminate the leaky modes is

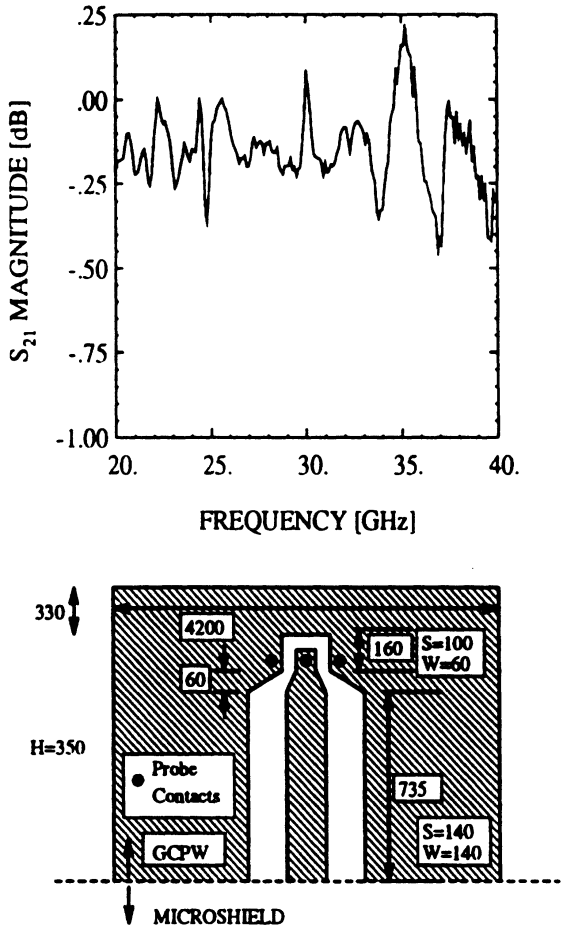


Figure 3: A transition from the cpw microwave probes to the microshield line, and the measured S_{21} of a microshield delay line using this design. All dimensions are in microns.

to integrate metallized cavities in the back of the substrate near the probe contact points. These modifications were implemented into the transition design shown in Figure 4, and the significant improvement in the calibration is demonstrated in the same figure. The ripple near 13 GHz appears to be a resonance which occurs when the total length of the 'thru' calibration line becomes a half-wavelength. Also, in a later design, the ripple near 36 GHz was reduced by completely eliminating the 300 μm length of gcpw line.

III. ATTENUATION

The attenuation characteristics of the microshield line have been investigated by comparing measured data on different microshield geometries against experimental and theoretical results for coplanar waveguide which are found in the literature [16, 18, 19]. At low frequencies, the two types of lines are expected to perform equally well, since dielectric and radiative losses are relatively small. Thus the attenuation is dominated by conductor loss, which should be about the same in microshield and cpw due to the similar geometry of the metallization. At higher frequencies, however, the microshield line gains an increasing advantage since it has essentialy zero dielectric loss and does not radiate energy into the substrate, unlike a substrate-supported cpw line. This characteristic has been verified by recent electro-optic sampling experiments, which provided attenuation data on membrane lines up to 1000 GHz [5].

The comparison between the microshield and cpw attenuation is shown in Figure 5. The microshield data in curves A and B was generated by averaging the measured insertion loss for several lines with lengths between 2.3 mm and 8.5 mm, while the gcpw data of point H was taken from measurements of a microshield-to-gcpw transition on a high-resistivity silicon wafer (ρ > 2000 Ω-cm). The cpw curves which are shown for comparison were chosen either because the dimensions are similar to the microshield lines (curves C,F,G) or to illustrate the effects of reducing the line geometry (curves D,E). All pertinent geometrical parameters for the cpw and microshield examples are given in the table beneath the figure, and it is

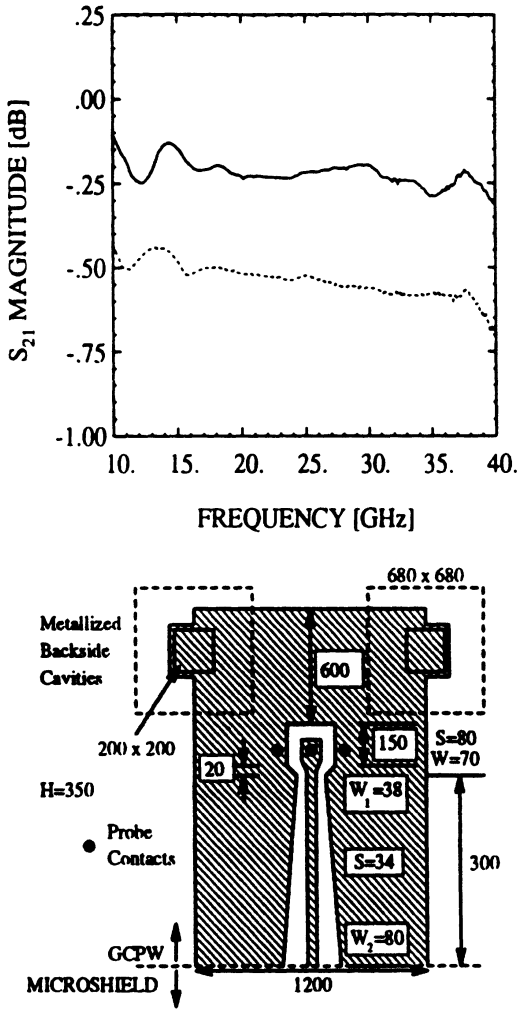


Figure 4: Measured S_{21} of two microshield delay lines of different length, using the modified transition from the cpw probes. The cavities are etched from the backside of the wafer and are pyramidal in shape; the dotted line is the cavity size at the bottom of the wafer. All dimensions are in microns.

noted that the conductor thickness is only about 2 skin depths at 25 GHz for all but two cases[1].

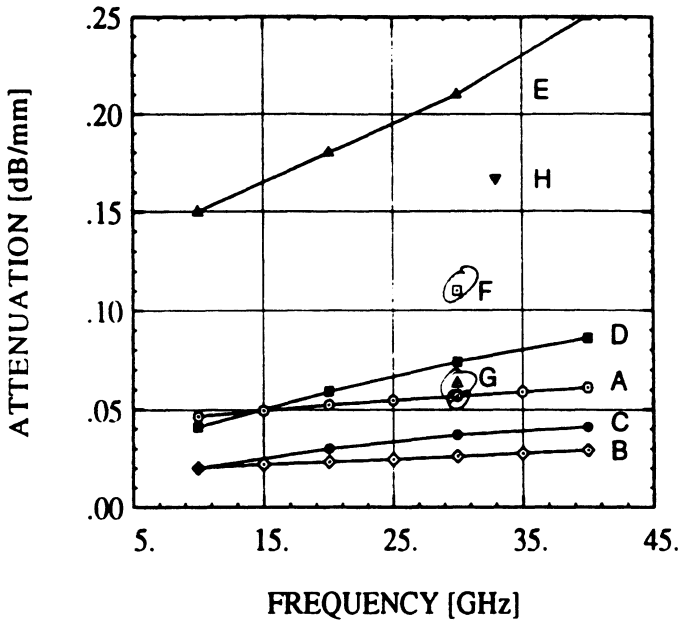
Several aspects of the information shown in Figure 5 deserve comment. First, the curves indicate that the loss for microshield and cpw lines of similar size is nearly the same at low frequencies, as expected. Also, the previous assertion that the microshield line performs better as the frequency increases is supported by the trends in the data. The second point is that the results for the microshield lines are consistent with the cpw loss behavior outlined in [17] by Jackson; namely, for a constant ground plane separation, an aspect ratio (S/S+2W) of 0.83 (curve A) gives much higher loss than an aspect ratio of 0.63 (curve B). A smaller shielding structure, however, may cause the behavior to deviate from that of the cpw line, particularly as the cavity size is reduced to the point that the lower ground plane and sidewalls affect the configuration of the fields. A third point relates to a comparison between the cpw and microshield data in terms of loss per electrical length, as the wavelength in the air dielectric is about 2.5 times longer than in GaAs and about 1.5 times longer than in quartz. The *calculated* loss for cpw in points F and G is about 0.1 dB/λ_g lower than the *measured* loss in curve A for the microshield line, which has identical center conductor and slot widths. This is a relatively small difference, however, some of which can be explained by errors in the measured and/or theoretical data.

The results presented here confirm that the microshield line is free from unexpected or excessive conductor-loss mechanisms, and has performance which is comparable to conventional substrate-supported coplanar waveguide at lower frequencies. Furthermore, the absence of dielectric-related loss and the ability to maintain non-dispersive, single-mode propagation over a very broad bandwidth lead to low attenuation well into the millimeter-wave frequencies.

IV. ADVANTAGES OF AN AIR SUBSTRATE

Due to the air substrate of the microshield line, the effective dielectric constant, $\epsilon_{r,eff}$, is

[1]The technique used in [18] assumes zero conductor thickness.



Curve	Line	ϵ_r	Substr	S	W	H	t	Z_O Ω	Data	Ref.
A	μshield	1.0	Air	250	25	355	1.2	75	Meas	–
B	μshield	1.0	Air	190	55	355	1.2	100	Meas	–
C	cpw	12.8	GaAs	232	84	100	-	50	Calc	[18]
D	cpw	12.8	GaAs	69	28	100	-	50	Calc	[18]
E	cpw	12.9	GaAs	88	16	500	1.0	30	Meas	[19]
F	cpw	12.9	GaAs	250	25	500	1.0	30	Calc	[16]
G	cpw	4.0	Quartz	250	25	250	1.0	50	Calc	[16]
H	gcpw	11.7	Si	50	125	355	1.2	73	Meas	–

Figure 5: Attenuation for microshield and coplanar waveguide lines. S is the center conductor width, W the slot width, H the substrate height, and t the metal thickness (in μm). The width of the lower shielding cavity for the microshield lines is 1800 microns.

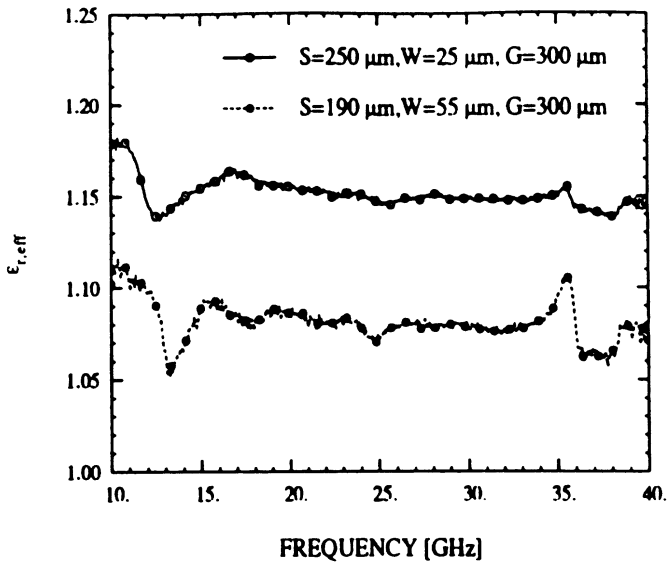


Figure 6: Measured effective dielectric constant, $\epsilon_{r,eff}$, on two microshield lines with different aspect ratios. The cavity heigth (H) is 350 μm.

very close to 1. Because of the membrane, however, $\epsilon_{r,eff}$ is slightly increased since a fraction of the fields will be contained within the thin dielectric layers. The membrane is a 1.5 μm-thick tri-layer composite of $SiO_2/Si_3N_4/SiO_2$ with constituent thicknesses of approximately 7000Å/3000Å/4000Å. The dielectric constant of the oxide is 3.9, and that of the nitride is 7.5. As shown in Figure 6, the measured $\epsilon_{r,eff}$ changes from around 1.09 to 1.15 as the slot width is reduced from 55 to 25 μm. The increase is a result of greater field confinement in the slot and thus in the membrane, and represents a decrease of nearly 3% in the guided wavelength. This dependence on the slot width is similar to the characteristics of cpw lines on a substrate such as GaAs or quartz [19].

There are several potential advantages of the nearly homogeneous air-dielectric. These include the absence of substrate moding problems, which in turn reduces dispersion and losses due to parasitic radiation. Another advantage is the improved electrical performance of discontinuities such as shorts, opens, steps and bends. As an example, the effective length extension[2] of a grounded coplanar short-end on substrates with ϵ_r=1.25 and 12.9

[2]The effective length extension, ΔL_{sc}, is the position at which an ideal short circuit would result in the same impedance seen at the physical end of the line.

(GaAs) is shown in Figures 7 and 8. The value of 1.25 was chosen to yield an *effective* dielectric constant around 1.12, in order to simulate the microshield line. The plots are theoretical results from the full-wave analysis described in the introduction, and from an expression by Getsinger which is applicable for quasi-TEM lines printed on an infinitely-thick dielectric [20]. In Figure 7, all lines have S=W=100μm with substrate heights of 350 and 700μm, while in Figure 8, all lines have a characteristic impedance around 65 Ω. Since the end-effect is completely inductive for pure-TEM operation, the *physical* size of the length extension is nearly independent of the dielectric constant. The shorter wavelength in the GaAs substrate, however, makes the extension become longer electrically. A similar argument can be made regarding the performance of coplanar open-ends. Under the quasi-TEM conditions, the physical length of the effective length extension, ΔL_{oc}, is roughly independent of ϵ_r, for small values of ΔL_{oc}. Again, this results in an increased electrical length when the substrate dielectric constant is higher, and these end effects can become significant since ΔL_{oc} is typically at least twice as large as ΔL_{sc} [21]. Thus, the air-filled environment of the microshield geometry offers the optimum conditions for making circuit performance less susceptible to these frequency dependent phenomena.

V. MICROSHIELD CIRCUIT COMPONENTS

V.1 Transitions to Coplanar Waveguide

An electrically short, low-loss transition between microshield and gcpw is important for measurement calibration purposes and for applications which could integrate circuit components configured in both types of lines. Essentially any means of coupling power into or out of a microshield circuit will require transmission lines printed on a solid substrate to provide mechanical strength at the connection.

It has been found that the similarities of the field configurations in cpw and microshield make broad band, low-loss transitions quite easy to achieve [3], despite the large difference in the dielectric constants of the transmission media. Although a rigorous optimization has not been conducted, designs based on a simple matching of quasi-static characteristic impedance

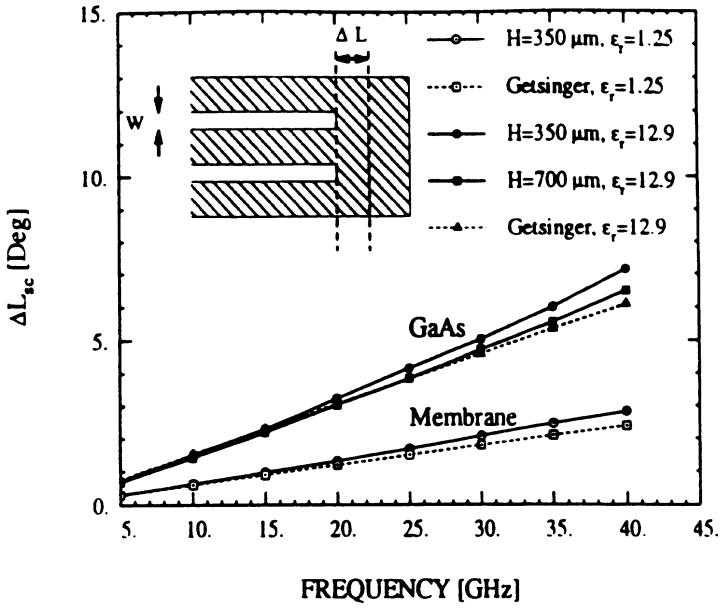


Figure 7: Effective length extension (in degrees) for a short-end discontinuity on lines with equal aspect ratios of $(S/S + 2W) = 0.33$. The characteristic impedance for the lines are 135 Ω (ϵ_r=1.25) and 55 Ω (ϵ_r=12.9). The line parameters are S=100 μm, W=100 μm and the substrate height H is given in the legend.

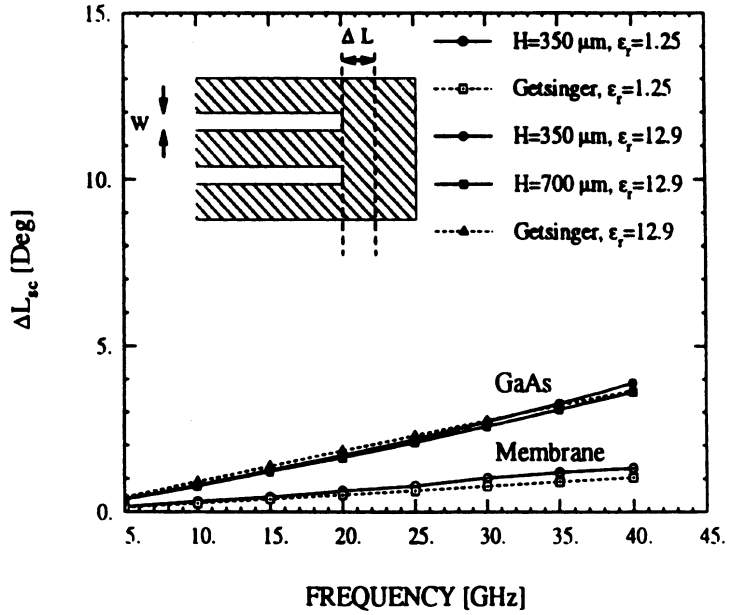
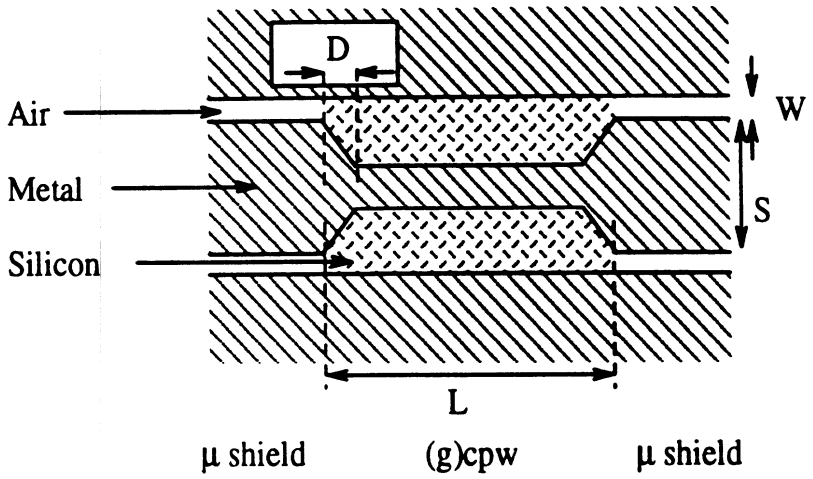


Figure 8: Effective length extension (in degrees) for a short-end discontinuity on lines with equal characteristic impedance (65 Ω). The parameters are S=165 μm, W=10 μm for the line with ϵ_r=1.25, and S=40 μm, W=67 μm for the line with ϵ_r=12.9. The substrate height H is given in the legend.

values have demonstrated very good performance up to 40 GHz. Three designs are given in Figure 9; the 'wide' design has slot widths which are nearly twice the substrate height, and thus will propagate a mode which is similar to that of microstrip, whereas the 'match' and 'taper' designs have narrower slots, leading to propagation of a cpw-like mode. The measured data on these transitions is shown in Figure 10 and the lower plot shows that a return loss below 20 dB across the entire band has been obtained. For the cpw curves, the ground plane beneath the transition section was removed. Also, the noise in the data is due to the calibration, since the original probe-to-microshield transition was used for these measurements (Figure 3).

The effect of a field mismatch between the microshield and gcpw lines is evident by comparing the 'wide' and 'match' gcpw designs, which have a similar characteristic impedance but different configurations of the electromagnetic fields. As mentioned, the 'match' design, like the microshield, will have a primarily cpw-like mode since the fields will tend to concentrate in the narrow slots. The slot widths in the 'wide' design, however, lead to propagation in more of a microstrip-like mode since there is greater influence from the lower ground plane. This influence can be examined by computing the change in the characteristic impedance as the substrate height (H) is varied. If H goes from 350 μm, as used in the current lines, to 1 cm, the changes in Z_0 for the microshield and 'match' gcpw lines are only 5.8% and 6.2%, respectively, but for the 'wide' gcpw the change is 31%. The field mismatch is clearly reflected in the data, which shows that $S_{11,match}$ is 4-6 dB lower than $S_{11,wide}$ across the entire band.

Additional transitions were tested which have smaller geometries for both the microshield and gcpw lines than those in Figure 9, and are therefore more appropriate for compact circuit configurations. The performance for two of the designs is shown in Figure 11. These circuits were measured using the modified probe-to-microshield transition (Figure 4) and thus the data has much less structure than in the previous figure. The strong resonances occur at frequencies for which the length of the gcpw sections are multiples of $\frac{\lambda_{eff}}{2}$. Each transition



Design	H	L	S	W	D	Z_o Ω
WIDE	350	1460	120	650	0	71
MATCH	350	1460	60	180	0	75
TAPER	350	1460	70	175	140	71

Figure 9: Three transitions from 75Ω microshield line (S=350 μm, W=35 μm) to cpw and grounded cpw. The dimensions for the (g)cpw lines are given in the table in microns, and the characteristic impedance values are for the grounded cpw configuration (i.e. with a lower ground plane).

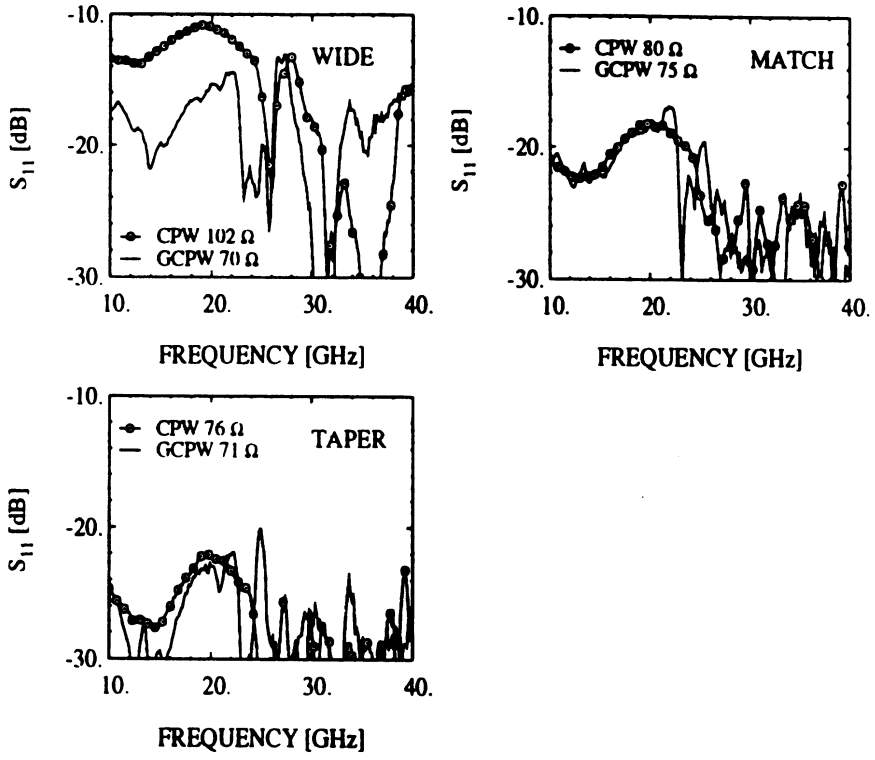


Figure 10: Measured S_{11} for three transitions from 75 Ω microshield line to cpw and grounded cpw (gcpw). The plots are labeled in the upper right hand corner to correspond to the designs in Figure 9.

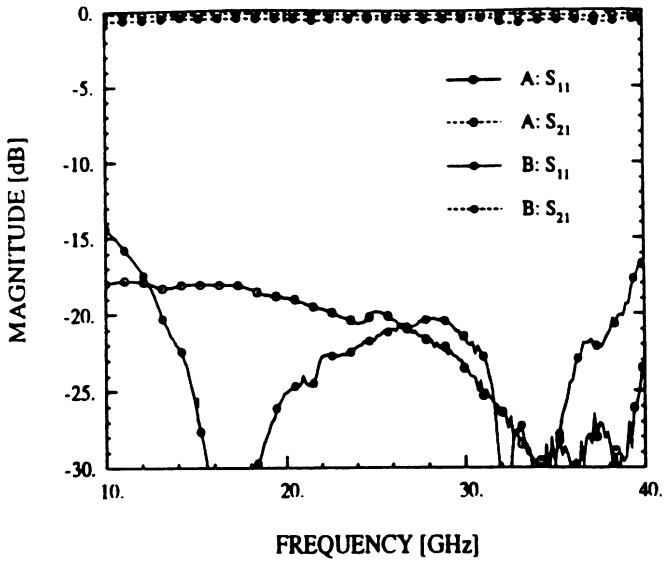


Figure 11: Measured scattering parameters for two transitions from 75 Ω microshield line to cpw and grounded cpw (gcpw). The center conductor width (S) and slot width (W) for the microshield are 250 and 25, respectively. In curve A, the gcpw dimensions are S=50, W=125 and the length of the line is L=1460. In curve B, the gcpw dimensions are S=30, W=80 and L=3500. All dimensions are in microns.

has a reasonably low reflection across the entire band, and it is expected that a rigorous full-wave analysis could lead to further design improvements.

V.2 Right-Angle Bend

A very common circuit 'element' in millimeter-wave systems is the right-angle bend. This structure gains significance with increasing frequency due to the parasitic capacitance and inductance which are associated with the abrupt change in the field orientation. These problems, combined with the mode-conversion which can also occur, result in a high reflection of the incident power (large S_{11}). In microstrip form, the typical means of improving the return loss is to miter the outside corners of the signal line [22]. This approach is less effective for coplanar waveguide [23], and alternative approaches such as air-bridges and dielectric overlays are adopted [24]. Both of these techniques are meant to offset the effects of different electrical path lengths along the two slots. Without this type of compensation, the asymmetry of the cpw right-angle bend will lead to excitation of the unwanted slot-line

mode.

Many of the problems inherent to bends which are printed on conventional cpw-line can be minimized with the microshield geometry. The absence of the high dielectric constant material has two important effects: it leads to a reduction in the parasitic capacitance and, for a fixed physical size, it reduces the difference in electrical path lengths through the two slots. The shielding cavity, furthermore, provides continuous ground plane equalization without introducing additional discontinuities, thus improving upon the conventional air-bridge. A comparison between the measured performance of a microshield-line bend and a typical cpw-line bend on GaAs [23] is shown in Figure 12. The cpw bend has a much smaller geometry and incorporates air-bridges which are placed very close to the discontinuity. The microshield bend has an S_{11} which is at least 8 dB lower over the 10-40 GHz band. Even when the lower ground plane was removed and the microshield bend was mounted on a styrofoam block, the S_{11} stayed below -20 dB, indicating that conversion into the slot-line mode is minimal. The noise in the data below 18 GHz is due to calibration error.

V.3 Open-End and Short-End Series Stub

Another common coplanar waveguide component is the open-end series stub, which was previously analyzed by Dib *et al.* [6]. The passband resonance of the stub occurs when the mean length is $\frac{\lambda_{eff}}{4}$, and the associated radiation loss $(1 - |S_{11}|^2 - |S_{21}|^2)$ is very low due to the location of the stub within the center conductor. The stop-band resonance occurs when the stub length is $\frac{\lambda_{eff}}{2}$ and is considerably stronger than the passband resonance, resulting in higher radiation losses. To demonstrate these characteristics, a comparison between measured and theoretical results for a typical open-end stub is given in Figure 13. The theoretical data, which are in good agreement with the measured results, extend out to 70 GHz in order to show the stop-band response. Since the attenuation in the measured circuit is dominated by conductor loss, the radiation loss is calculated using the theoretical scattering parameters. Small errors in the numerical results caused erratic behavior of the radiation loss above 60 GHz, and these results are not shown. Also, the shift in the predicted frequency

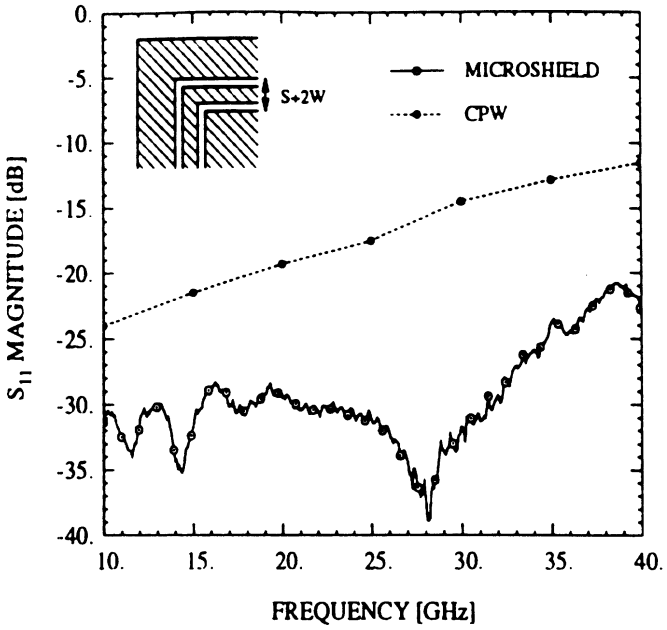


Figure 12: Measured performance of right-angle bends fabricated using a microshield line and a cpw line on GaAs. The cpw bend has S=39, W=24, H=90 and uses 2 μm-high air-bridges on each side of the bend [23]. The microshield line has S=250, W=25 and H=350. All dimensions are in microns.

response is believed to result partly from using an inaccurate value for the effective dielectric constant (refer to Section I), as the slot widths in the actual circuit were 3-5 μm smaller than expected due to fabrication problems. As presented in section IV, this causes $\epsilon_{r,eff}$ to increase and therefore reduces the resonant frequency. The performance seen in the figure is typical of designs with gap widths L_2 as small as 60 μm, as was verified experimentally and theoretically. Furthermore, the response is more narrow band than a stub with similar transverse dimensions printed on silicon [25].

The short-end series stub, like the open-end stub, is useful for a variety of circuits including bandstop filters, pin diode switches and attenuators, and has been reported by several authors [6, 26, 27]. The geometry offers the same advantages of compactness and low radiation loss. Unlike the open-end version, however, it has a much wider 3-dB bandwidth than a comparable stub printed on alumina or GaAs [25] (roughly 70% compared to 35%). The performance for a typical design which is $\frac{\lambda_{eff}}{4}$ at $\approx$ 30 GHz, along with results obtained from

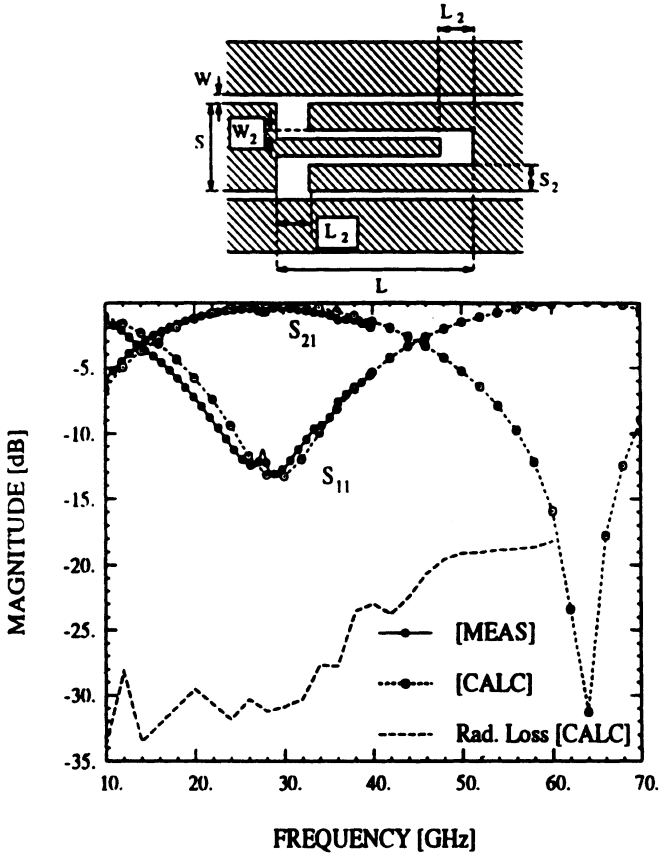


Figure 13: Measured and calculated S-parameters for a microshield open-end series stub. The stub dimensions are L=2500, L_2=200, S=250, S_2=80, W=25, and W_2=25. All dimensions are in microns.

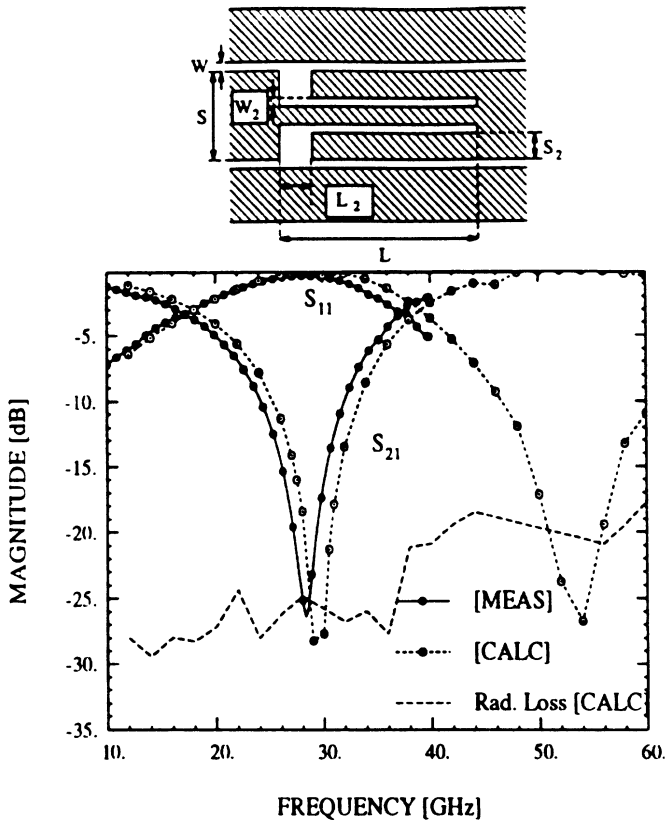


Figure 14: Measured and calculated S-parameters for a microshield short-end series stub. The stub dimensions are L=2500, L_2=200, S=250, S_2=80, W=25, and W_2=25. All dimensions are in microns.

the full-wave analysis, are shown in Figure 14. The shift in the frequency response is similar to the one in Figure 13 and carries the same explanation. As with the open-end stub, small variations in the dimensions have no significant effects on the shape or bandwidth of the response, but may change the resonant frequency if the mean length is altered.

V.4 Lowpass Filters

The stepped-impedance approach to lowpass filter design is a relatively easy technique to use, and it is well suited for applications which do not require a sharp roll-off in the insertion loss. Often, however, the filter specifications call for high rejection over multiple-octave bandwidths, a requirement which may be difficult to meet using conventional substrate-supported lines due to the propagation of higher order modes. Thus the very broad, single-mode band-

width of the microshield line can provide superior filter performance in this respect. In addition, the absence of the dielectric-related loss mechanisms, both attenuation and parasitic radiation, results in very low passband insertion loss.

Stepped-impedance filters using 5-, 7-, and 9-sections have been designed and tested. Some of the results were previously presented in [3], where it was shown that the measured performance compared very well with ideal transmission line theory, as a result of the pure TEM nature of the microshield propagating mode. In Figure 15, the measured data for a 5-section filter is compared with results from the full-wave analysis described in section I. The rejection is greater than 20 dB up to 75 GHz, which is about 1.5 octaves above the 3-dB point at 26 GHz. The measured passband insertion loss of this filter is between 0.2 and 0.5 dB from 20-23 GHz. The noise in the measured data is due to the transition design shown in Figure 3.

As mentioned previously, a short-end series stub can be utilized to make circuits such as bandstop filters by cascading multiple stubs in series. It is also possible to take advantage of the broad bandwidth of this stub to design high performance lowpass filters. One example is the addition of a short-end stub onto the end of the stepped-impedance lowpass filter described above. The stub has a length of 940μm, with other dimensions identical to those listed in Figure 14, and resonates around 90 GHz. By comparing the theoretical performance of this new filter in Figure 16 to the performance without the stub in Figure 15, it is clear that there is a significant improvement in the stopband of the filter. Another example is a very compact, easy to design lowpass/bandstop filter with a corner frequency of 52 GHz, which is simply the series combination of two 90 GHz stubs. This design has a total length of 1.98 mm, using a 100 μm spacing between the stubs, and thus would have very low conductor loss along with the low radiation loss. The predicted performance is shown in Figure 17. By reversing the second stub to make the circuit longitudinally symmetric, the roll-off is more gradual and thus the low-band ripple in S_{21} is reduced. The predicted peformance for this configuration is shown in Figure 18.

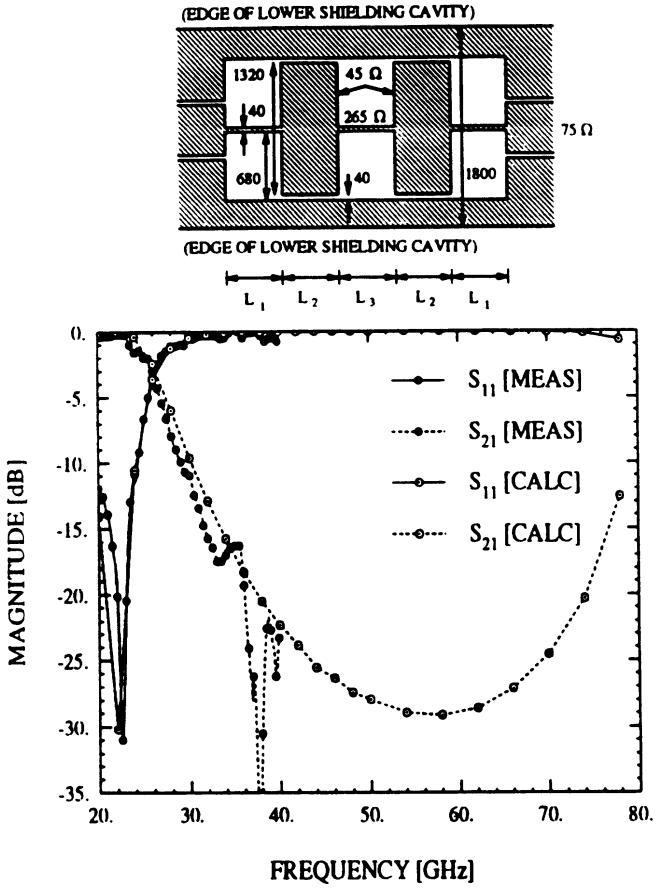


Figure 15: Measured and calculated S-parameters for a microshield lowpass filter. The lengths of the different sections are $L_1 = 745$, $L_2 = 1200$, and $L_3 = 1189$ (microns).

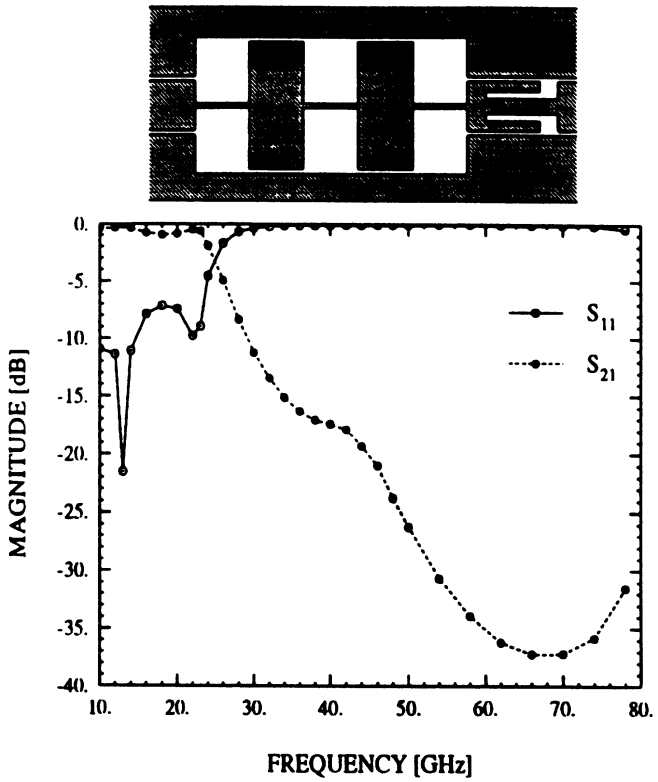


Figure 16: Theoretical performance of the filter shown in Figure 15 with a 90 GHz short-end series stub attached.

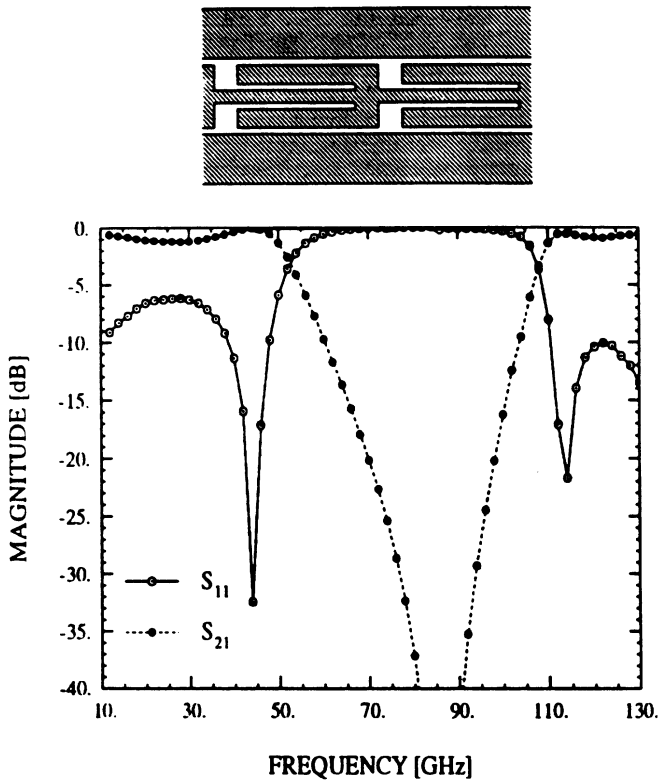


Figure 17: Theoretical performance of two 90 GHz short-end series stubs (asymmetric configuration).

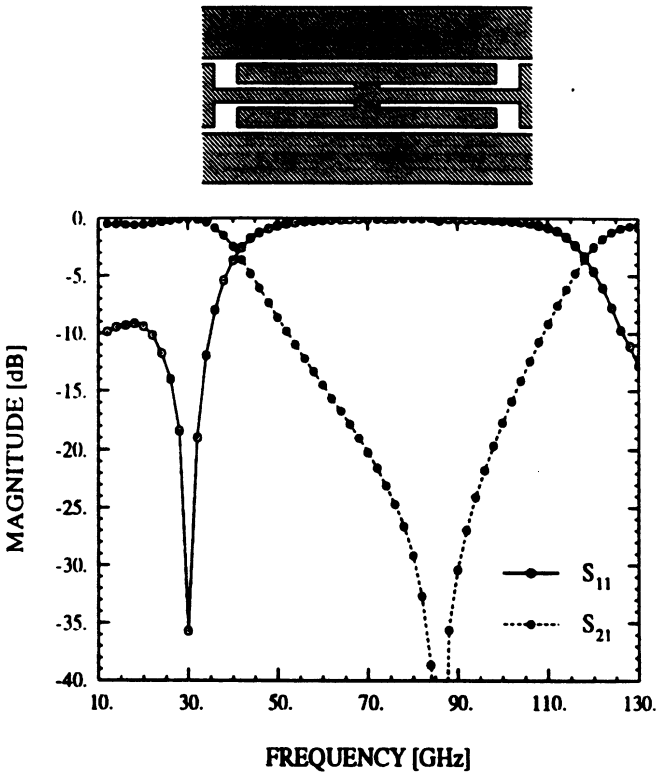


Figure 18: Theoretical performance of two 90 GHz short-end series stubs (symmetric configuration).

V.5 Low-Loss Bandpass Filters

By cascading multiple open-end stubs in series, it is quite simple to realize a bandpass response with high out-of-band rejection and low loss. A three-section design was fabricated using the stub dimensions given in Figure 13, with each section separated by 150 μm. The measured response, shown in Figure 19, has an insertion loss of only 1.0 dB from 22-32 GHz, which is competitive with the best shielded bandpass filters using suspended stripline [28]. The performance of this microshield filter could be further improved using thicker metallization[3] or larger slot widths to minimize the conductor loss. The calculated data is generated by using the scattering parameters found from the full-wave analysis of a single stub and treating the filter as three non-coupled elements in series. The agreement between the measured and calculated performance is quite good and indicates that there is very little electromagnetic coupling between the stubs, even though the stub separation is only 150 μm. The response of the filter can also be modeled almost exactly by cascading the *measured* results for a single stub, and this approach accurately predicts the 1.0 dB insertion loss.

VI. CONCLUSIONS

This paper presents a comprehensive introduction to the microshield transmission line and several passive circuit components. The measured performance from 10-40 GHz is very good and in certain cases superior to the performance which is characteristic of conventional coplanar waveguide circuits. Clearly, there are differences between the microshield line and a substrate-supported line, including larger circuit dimensions due to the low dielectric constant and the use of the thin dielectric membrane. At the same time, however, there are the advantages of very broad-band TEM operation, a wide range of characteristic impedance, no requirement for air-bridges, and the possibility of using much thicker substrates at higher frequencies without the need for mechanical thinning. At submillimeter

[3] All circuits fabricated in this study had a metallization thickness of 1 μm.

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wavelengths, furthermore, the larger electrical size could simplify fabrication. Thus, the microshield line shows significant potential for high-performance millimeter wave applications, and is a strong candidate for submillimeter wave designs.

ACKNOWLEDGEMENTS

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A 250 GHz Microshield Bandpass Filter

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Abstract - A four-section, planar bandpass filter has been designed, fabricated and tested at 130-360 GHz. The filter is based on the microshield line, a half-shielded transmission line in which the conducting lines are supported on a 1.4 μm-thick dielectric membrane. The insertion loss of the filter is less than 1.5 dB at 250 GHz, demonstrating the excellent performance of the microshield geometry. Also, a Monte Carlo routine was developed in conjuction with a semi-empirical/semi-analytical model to allow the S-parameters of the filter to be derived from scalar power measurements.

I. INTRODUCTION

The potential for high performance planar circuits which are implemented in conventional substrate-supported microstrip or coplanar waveguide is severely limited at sub-millimeter wave frequencies. This shortcoming is primarily due to dielectric and radiation losses, and the most common solution is to utilize waveguide-based designs [1]. One quasi-planar transmission line which can overcome these difficulties is the microshield line. Introduced in 1991 [2], microshield is a half shielded geometry, similar to CPW, which uses a thin (around 1.4 μm) dielectric membrane to support the conducting lines and upper ground planes above a metallized shielding cavity. It is characterized by low loss, broad band TEM propagation and has previously been demonstrated in circuits operating at Ka-band [3, 4] and W-band [5]. In the work presented here, microshield is utilized to fabricate the first planar bandpass filter at 250 GHz. This paper also describes a quasi-optical measurement technique which was developed in order to determine the filter S-parameters

in the presence of reflections at the filter input and output ports, due to the receiving antenna and the microbolometer used for power detection, respectively.

II. BANDPASS FILTER

The bandpass filter consists of a compact configuration of open-end series stubs which provides both low loss and longitudinal symmetry. Application of the open-end stub to filter design has been examined in previous publications, in which it was noted that the location of the stub within the center conductor leads to greater field confinement and thus lower radiation loss than is characteristic of straight gap-coupled resonators or stubs with lateral extension [6, 7]. The design applied here utilizes four quarter-wavelength stubs which are resonant at 250 GHz, with the second and fourth stubs reversed relative to the first and third (Figure 1).

III. MEASUREMENT TECHNIQUE

At frequencies above 115 GHz, there are currently very few options available for microwave circuit characterization. Electro-optic sampling and waveguide-based approaches are possible techniques, but were not available for this project. Therefore, an alternative technique based on quasi-optical methods was developed which uses a semi-empirical/semi-analytical model to extract the circuit S-parameters.

The objective of the quasi-optical measurement is to determine the amount of power transmitted through the filter as a function of frequency, using the circuit shown in Figure 2. In this figure, RF power is supplied from a Gunn diode/tripler pair and coupled into the circuit through a CPW-fed, double folded-slot antenna [8]. A thin-film bismuth microbolometer detector [9] is placed at the output of the filter, in parallel with an RF short which is positioned approximately a quarter-wavelength away (L_4). The RF short is a silicon oxide (SiO) thin-film capacitor which allows DC biasing of the bolometer detector and presents an open circuit at the output of the filter. The power measurement is made by modulating the RF signal with a 1 KHz square wave and using a lock-in amplifier to detect the 1 KHz voltage across the bolometer. As a means of calibration, a similar circuit is utilized in which the filter is replaced by a straight length of microshield transmission line. Using the measured absolute responsivity (in Volts/Watt) of the bolometers in each circuit,

one can determine the ratio of the power received through the filter (P_{filt}) to that received through the transmission line (P_{TL}).

IV. S-PARAMETER EXTRACTION

The remaining step involved in characterizing the filter is to extract its S-parameters using the experimental values for P_{filt}/P_{TL}. An equation which relates the scalar power measurement data and all the pertinent vector quantities in the system is derived from the circuit model in Figure 2:

$$P_{filt}/P_{TL} = |S_{21,a}|^2 \left|1 - \Gamma_{ds}\Gamma_b e^{-2\gamma(L_1+L_2+L_3)}\right|^2 \left(\frac{1-|\Gamma_a|^2}{1-|\Gamma_b|^2}\right) \times \left|1 + \left(S_{11,a}^2 - S_{21,a}^2\right)\Gamma_{ds}\Gamma_a e^{-2\gamma(L_1+L_3)} - S_{11,a}\left(\Gamma_{ds}e^{-2\gamma L_1} + \Gamma_a e^{-2\gamma L_3}\right)\right|^{-2} \quad (1)$$

where γ is the propagation constant of the microshield line. In order to resolve the unknowns in Eqn. 1, a Monte Carlo routine (MCr) has been implemented which uses a combination of empirical and analytical data for initial values. Estimates for Γ_a and Γ_b are computed using measured values for the bolometer DC resistance and values for γ extrapolated from 10-40 GHz measurements. Initial values for the antenna reflection coefficient (Γ_{ds}), on the other hand, have been determined using a full-wave analysis [8]. After specifying upper and lower limits for all the parameters in Eqn. 1, the MCr is then used to fit them to the model. An important point is that the initial range for the magnitude of the filter S-parameters is between 0 and 1, i.e. they are unconstrained. However, the quantity $|S_{11,a}|^2 + |S_{21,a}|^2$ is restricted to a range which encompasses the expected overall filter loss. Also, the range for the phase is 80° about the values predicted by a full-wave analysis of the filter.

In order to investigate this method of solution, the filter S-parameters from the full-wave analysis were used along with randomly generated values for the remaining unknowns to compute exact values for P_{filt}/P_{TL}. The MCr was then applied to this hypothetical data set and the accuracy proved to be very good. As shown in Figure 3, the MCr-extracted $|S_{21,a}|$ follows the true distribution almost exactly and the maximum passband error is about 0.45 dB. As a consequence of the weaker dependence of Eqn. 1 on $|S_{11,a}|$ it is more difficult to resolve this parameter. Likewise, it is only possible to determine the phase of the S-parameters when the magnitude of the respective unknown

is quite large. Even then, due to the rapid phase variation in the 4-element filter, the results can only approximate the overall distribution.

V. RESULTS AND CONCLUSION

Using the measurement technique described in section III and the S-parameter extraction technique described in section IV, the performance of the filter was measured at eight frequencies from 130-360 GHz. Due to the limited RF power and the low responsivity of the bolometers (typically around 2 Volts/Watt), the dynamic range is limited to approximately 20 dB. As shown in Figure 4, the S-parameters extracted from the raw measured data are very close to the predicted response from the full-wave analysis. The measured pass-band insertion loss for this four-section filter is around 1.5 dB, and the low frequency stop-band provides excellent rejection. These results confirm that high-performance, planar circuits are realizable at millimeter- and submillimeter-wave frequencies using the microshield line configuration.

ACKNOWLEDGEMENTS

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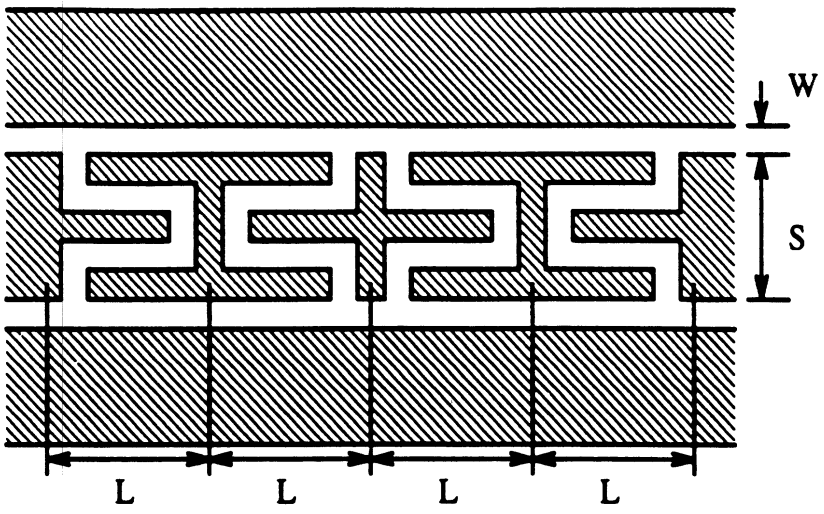
Figure 1: The four-section microshield bandpass filter (not to scale). The metallization pattern is shown in (a), where L=250, S=50 and W=10. A cross-sectional view is shown in (b), where H=200, W_1=320 and W_2=40. The geometry is comprised of three silicon wafers which are used to support the membrane and filter metallization, form the cavity sidewalls, and complete the lower ground plane, respectively. In (b), metallization is indicated by the dark lines. All dimensions are in microns.

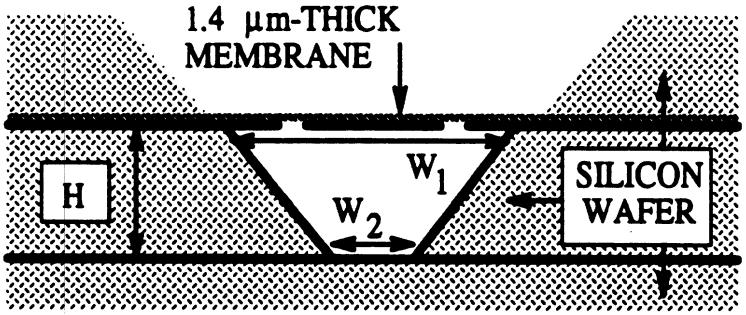
Figure 2: Diagram of the circuit used in the quasi-optical measurement, where DUT stands for device under test. The upper illustration shows a circuit which has a bandpass filter as the DUT. The reflection coefficients Γ_a and Γ_b may be different, in general, to allow for fabrication tolerances between the bolometers of the filter circuit and the transmission line circuit.

Figure 3: Comparison between the MCr-extracted values (markers) and the "exact" predicted filter response from a full-wave analysis (lines), using a hypothetical set of system parameters to compute P_{filt}/P_{TL}.

Figure 4: Comparison between the results extracted from raw measured data (markers) and the predicted filter response from the full-wave analysis (lines).



(a)



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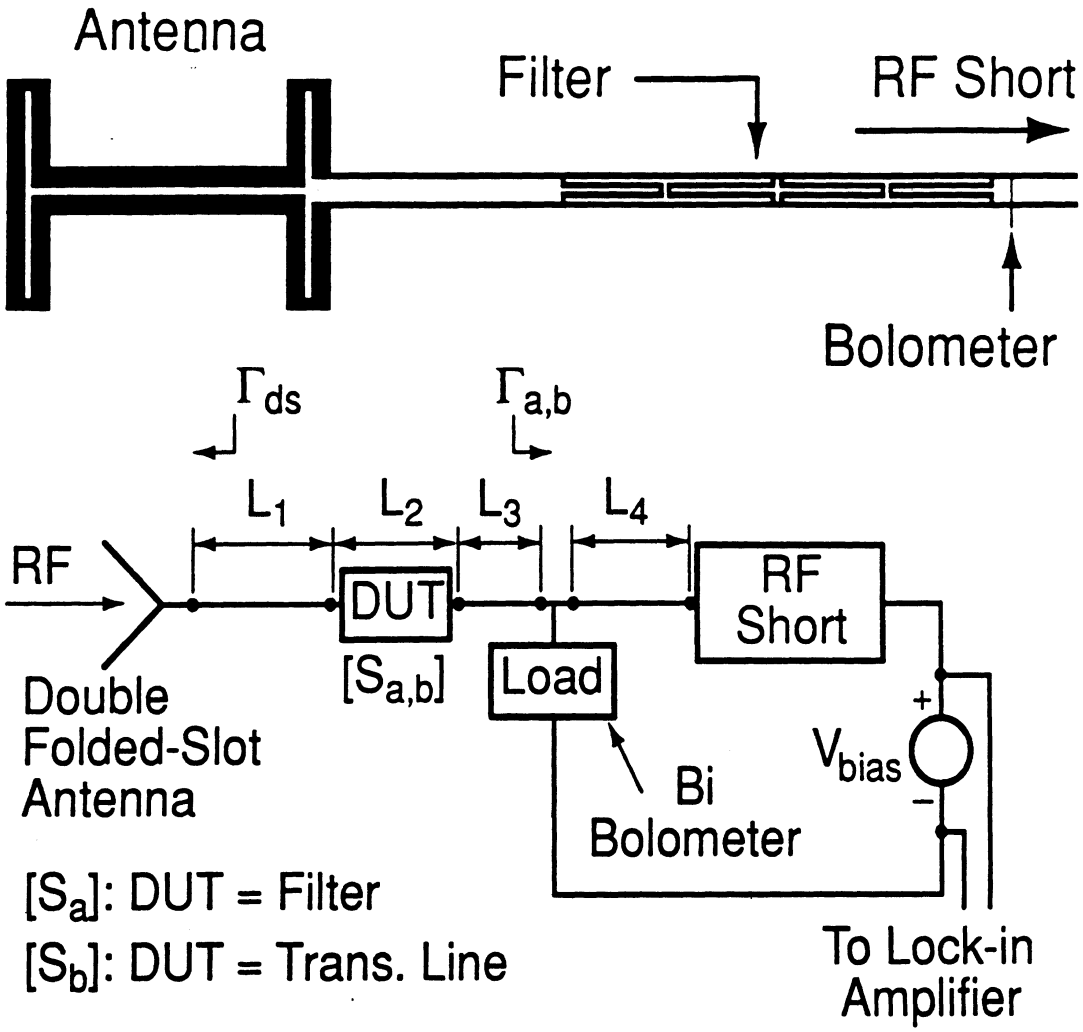
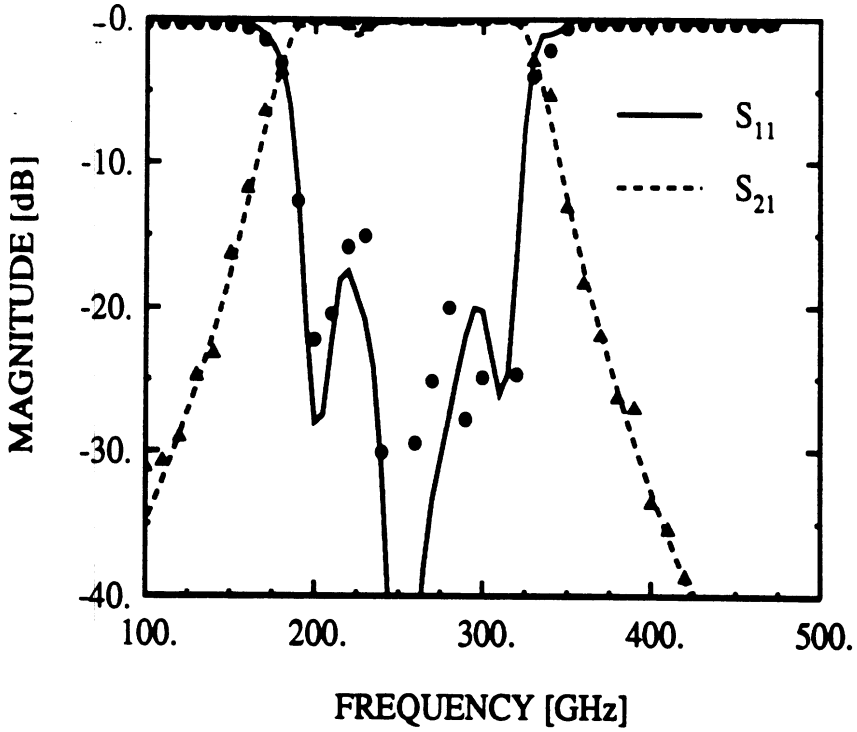

Antenna
Filter
RF Short
Bolometer
Γ_{ds}
$\Gamma_{a,b}$
L_1
L_2
L_3
L_4
RF
DUT
$[S_{a,b}]$
Load
RF Short
Double Folded-Slot Antenna
Bi Bolometer
V_{bias}
+
−
$[S_a]$: DUT = Filter
$[S_b]$: DUT = Trans. Line
To Lock-in Amplifier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S_{11}
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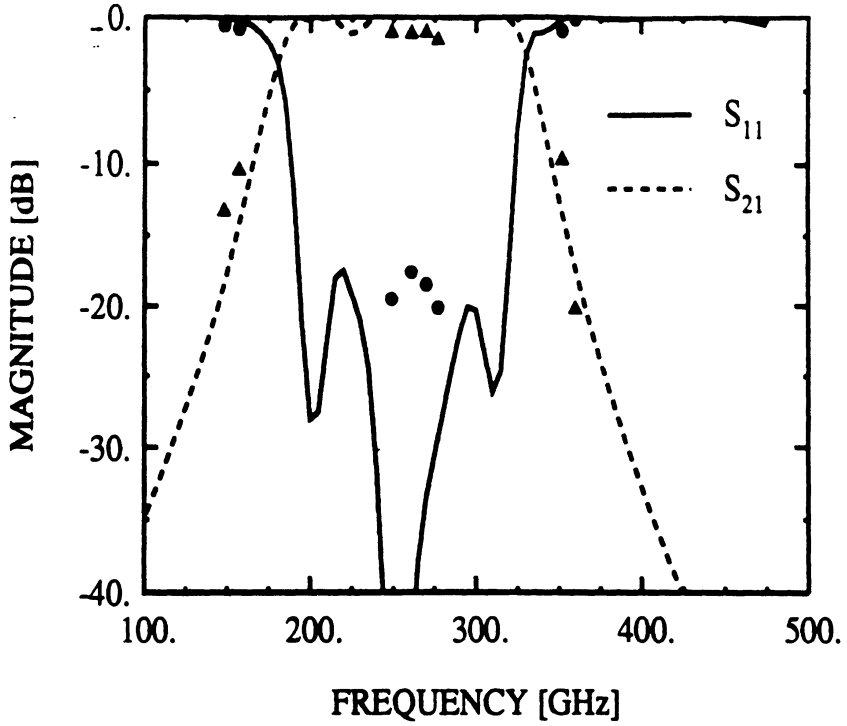
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Submitted to IEEE Trans. Antennas Propagat., September 1994.

Single and Double Folded-Slot Antennas on Semi-Infinite Substrates

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Abstract - In this paper, design guidelines are presented for single and double folded-slot (DFS) antennas on a dielectric half-space. The DFS antenna consists of two folded-slot elements which are separated by a half-wavelength, and are fed from one end using a coplanar waveguide transmission line. A space-domain integral equation technique, based on the free-space Green's function, has been used to compute the resonant circumference and self and mutual impedances of single folded-slots on various substrates. In addition, the input impedance and radiation patterns of several DFS designs are included. Specific examples are presented for air, quartz and silicon substrates, and measured data for DFS antennas on air and silicon substrates is provided to validate the calculated results. Finally, details pertaining to the derivation and evaluation of the moment method admittance terms are described.

I. INTRODUCTION

As is well known, planar antennas consisting of patches, dipoles or slots, fed by a microstrip transmission line, are extremely useful due to their low cost, light weight, and flexibility of design. They have been extensively analyzed (e.g. [1]) and are used in applications which range from complex conformal arrays for radars to quasi-optical spatial power combiners [2]. As the popularity of the coplanar waveguide (CPW) transmission line has increased significantly in recent years, antenna elements which are suitable for a CPW-feed configuration have also become important [3, 4, 5]. In this paper, design guidelines for CPW-fed, single and double folded-slot (DFS) antennas on a dielectric half-space are presented. The DFS antenna consists of two planar, folded-slot elements which are displaced along a CPW line by a half-wavelength, resulting in a compact geometry which provides a modest amount of beam-shaping.

In order to characterize the antennas, a space domain integral equation technique has been employed which determines the magnetic current, or electric field, in the apertures of the metallization. It is a standard formulation based on the expansion of the unknown current in terms of

subsectional basis functions, the coefficients of which are solved for using the method of moments with Galerkin testing. A unique feature of this implementation, however, is the approach used to calculate the admittance terms for overlapping piecewise sinusoidal basis functions, in particular the handling of the 1/r singularity. A general outline of the formulation is presented in section II, while the details pertaining to the evaluation of the admittance terms are the subject of the appendix.

The calculated and experimental results presented here are intended to provide a thorough introduction to the characteristics of single and double folded-slot antennas on semi-infinite substrates. The data primarily pertain to air (ϵ_r=1), quartz (ϵ_r=4) and silicon (ϵ_r=11.7) substrates. In section III, the resonant circumference, self impedance, and mutual impedance of the folded-slot are examined. This is followed by an analysis of several double folded-slot designs in section IV, which includes the input impedance (Z_{in}), directivity and far-field patterns.

II. THEORY

The formulation used here is a space domain integral equation technique based on the free-space dyadic Green's function. In this approach, continuity of the tangential electric ($\vec{E}$) and magnetic ($\vec{H}$) fields in the apertures of the CPW feed line and antenna is enforced, resulting in an integral equation involving the aperture electric field (or magnetic current, $\vec{M}$) as the unknown parameter. Since $\vec{M} = \vec{E} \times \hat{n}$, where $\hat{n}$ is the outward unit normal in each half-space, continuity of $\vec{E}_{tan}$ is satisfied by setting $\vec{M}_{sup} = -\vec{M}_{sub} = \vec{M}$. In this expression, $\vec{M}_{sup}$ and $\vec{M}_{sub}$ refer to the equivalent magnetic currents on the surfaces of the upper and lower dielectric half-spaces, respectively. The continuity of $\vec{H}_{tan}$ is expressed in terms of the following equation:

$$\hat{n} \times \int_{S'} [\bar{\bar{G}}_{sup}(\vec{r},\vec{r}') + \bar{\bar{G}}_{sub}(\vec{r},\vec{r}')] \cdot \vec{M}(\vec{r}')ds' = \vec{J} \tag{1}$$

where $\bar{\bar{G}}$ is the free-space dyadic Green's function and $\vec{J}$ is the current excitation which is assumed with the ideal current source model. To solve this equation, the aperture is first subdivided and piecewise sinusoidal basis functions are utilized to approximate the magnetic current distribution. These functions are of the form:

$$\begin{aligned} T(\zeta,\xi) &= f(\zeta)p(\xi) \\ f(\zeta) &= \begin{cases} \frac{\sin(k_m(\zeta-\zeta_{n-1}))}{\sin(k_m l_{n-1})} & \text{if } \zeta_{n-1} < \zeta < \zeta_n \\ \frac{\sin(k_m(\zeta_{n+1}-\zeta))}{\sin(k_m l_{n+1})} & \text{if } \zeta_n < \zeta < \zeta_{n+1} \end{cases} \\ p(\xi) &= \begin{cases} 1 & \text{if } \xi_{n-1} < \xi < \xi_n \\ 0 & \text{else} \end{cases} \\ l_{n\pm1} &= |\zeta_n - \zeta_{n\pm1}| \end{aligned} \tag{2}$$

where k_m is a scaling parameter which is typically equal to the free-space wavenumber. By applying the method of moments with Galerkin testing to Eqn. 1, the following system of equations is obtained:

$$\begin{pmatrix} \langle Y_{xx} \rangle & \langle Y_{xz} \rangle \\ \langle Y_{zx} \rangle & \langle Y_{zz} \rangle \end{pmatrix} \begin{pmatrix} \{M_x\} \\ \{M_z\} \end{pmatrix} = \begin{pmatrix} \{\tilde{J}_x\} \\ \{\tilde{J}_z\} \end{pmatrix} \tag{3}$$

where $\langle Y_{\zeta\xi}(\zeta, \xi = x, z) \rangle$ represents a block of the admittance matrix, $\{M_{\zeta,\xi}\}$ is a coefficient vector for the current expansion functions, and $\tilde{J}_\zeta$ is the weighted integral of J_ζ over a subsection. The mechanics involved in deriving expressions for the admittance terms have been presented in previous publications, and the particular method adopted here was utilized by Barkeshli and Volakis [6]. Although the details of that analysis will not be repeated here, the approach taken to accurately compute the self-cell term when using the PWS basis functions is outlined in the appendix.

After solving Eqn. 3 for $\{M\}$, the normalized self impedance is determined by analyzing the magnetic current standing-waveform in the antenna feedline [7]. A cubic-spline interpolation can resolve the values and positions of the current minima and maxima, from which the guided wavelength (λ_g), standing-wave ratio (swr), and distance from the reference plane to the first current maxima (d_{max}) can be calculated. The impedance is then found using ideal transmission line equations. The mutual impedance between two folded-slots is determined by inverting the admittance matrix and extracting the (i,j) element of the resultant impedance matrix, where i refers to the subsection at the input port of the first antenna and j refers to the subsection at the input of the second antenna. This element, Z_{ij}, directly relates the voltage at port i due to a source current at port j. Finally, the directivity and far-field patterns are determined with standard expressions from the literature (e.g. [8]) since the complete magnetic current distribution in the antenna elements is known.

III. SINGLE FOLDED-SLOT ANTENNA

This section provides calculated results for the resonant frequency and self and mutual impedances of the single folded-slot antenna on different semi-infinite substrates (Figure 1). As with the simple slot antenna, the radiation pattern is simply that of a magnetic dipole, and thus is not included in this analysis. The frequency behavior of the self impedance for the three designs described in Table 1 is given in Figure 2. It is seen that the first useful resonance coincides with the peak in the real part of the self impedance, since the first zero crossing of the imaginary part is associated with a near short-circuit impedance. The dependence of this first resonance on the dielectric constant of the substrate material, ϵ_r, is examined in Figure 3. This data shows the circumference of the antenna normalized to the free-space wavelength at the resonant frequency, where the circumference is given by $C = 2(L_a + S_a + W_{a2} - W_{a1})$. The curves can be approximated by using a quasi-static

expression for the effective dielectric constant:

$$C/\lambda_o \approx \frac{C_o}{\sqrt{(\epsilon_r + 1)/2}} \tag{4}$$

where C_o is the value of C/λ_o for $\epsilon_r = 1.0$. For the designs considered in Figure 3, this constant is equal to 0.97 and 0.99 for $S_a/L_a = 0.01$ and 0.04, respectively. Equation 4 underestimates the full-wave result, however, indicating that the actual effective dielectric constant is a few percent lower than the quasi-static approximation. It is also worth noting that the results in Figures 2 and 3 take into account the effects of the CPW feedline, as discussed in section II. The feedline will slightly reduce the effective slot circumference, thereby increasing the resonant frequency. Finally, the plots in Figure 4 contrast Z_{self} for a folded-slot (design C) and a comparable slot antenna. The peak in $\mathrm{Re}(Z_{self})$ at the first resonance for the folded-slot is four times smaller than for the slot, which is the dual of the relationship between folded-dipoles and standard dipole antennas [8]. The self impedance of each antenna at its respective second resonance, however, is 16 Ω.

The mutual coupling between two or more folded-slot antennas is useful information for designing arrays. Shown in Figures 5-7 is the mutual impedance, Z_{12}, between two folded-slots of designs A-C, respectively, at the first resonance. The antennas are in the broadside configuration with each input port positioned as shown in Figure 1, and the separation distance S is measured between the center of the folded slots. As opposed to the self impedance data, these calculations do not include the CPW feedlines. Ideally, the CPW lines do not radiate, however, such that negligible differences are incurred by their omission. By comparing the plots in Figure 7 to those in Figure 8 for the comparable slot antenna pair, it is clear that the impedance coupling between the slots is four times as strong as the coupling between folded-slot antennas, as found above for Z_{self}. The impedance coupling between two folded-slots of design C at the second resonance (Circumference = $0.47\lambda_o$) is shown in Figure 9. In this case, the coupling is nearly the same as for the slot antenna at its second resonance ($L_a = 0.33\lambda_o$).

IV. DOUBLE FOLDED-SLOT ANTENNA

The design of the double folded-slot antenna is primarily based on two parameters: the folded-slot elements and the connecting line between them. General guidelines for each of these are given below, and typical performance characteristics of the designs given in Table 2 are discussed in the following sections. In what follows, the frequency at which the E- and H-plane patterns are peaked at broadside and the two sidelobes in the E-plane are symmetric is defined as the center frequency, f_c.

IV.1 Design Guidelines

- *Folded-Slot Element* - The total circumference, measured through the center of the slots, should be approximately equal to 1.0-1.04 λ_g, where λ_g is the guided wavelength of the prop-

agating CPW mode at f_c. In computing this wavelength, the same quasi-static approximation used in Eqn. 4 has been applied. Widening the slot width W_{a2} decreases the center frequency and also tends to increase the reactive component of Z_{in} around f_c. If the slot width is too narrow, however, there tends to be greater variation in Z_{in} versus frequency. Using a width for W_{a2} around $\lambda_g/60$ is a good compromise between the two effects.

- *Connecting Line* - The separation between the two elements must provide a 180° phase shift for the guided CPW mode and the radiating space wave, and this may be accomplished using a meander line such as that shown in Figure 10. In this design the path length through the connecting line ($2L_{c1} + L_{c2} + 2L_{c3}$) must be approximately equal to 0.5 λ_g and the physical distance ($2L_{c1} + L_{c2}$) must be approximately equal to 0.5 λ_{ant}, where λ_{ant} is the wavelength in the dielectric half-space. The factor for each length, as derived from the full-wave analysis, ranges from 0.503-0.51 (versus 0.5), and increases as the slot width W_{a2} narrows. A similar design with a symmetric meander on each side of the center line could also be used, however the single-meander version is adequate and does not cause significant slot-line mode excitation, since each bend is complimentary to a bend in the opposite direction. Also, note that a comparable end-fed double slot antenna requires a 360° element separation in order to feed each antenna in phase. The DFS geometry, therefore, is much more compact.

IV.2 Radiation Patterns

Since each of the slots is equivalent to a magnetic dipole, the E-plane for the double folded-slot antenna is parallel to the feedline and normal to the plane of the antenna. With the correct phasing between the elements, the main beam points at $\Theta = 90°$, i. e. broadside. The H-plane is parallel to the slots and has one lobe that is symmetric about $\Phi = 90°$, which is simply the pattern for a single magnetic dipole. In order to demonstrate typical characterisitcs, the E- and H-plane patterns for design B are shown in Figures 11 and 12. Due to limitations in the experimental setup, the measured patterns are only strictly valid from about 30° to 150°. It can be observed that a deeper null exists in the E-plane toward $\Theta = 180°$, and also that the sidelobe facing the feedline rises quickly as the frequency increases.

Without the additional beam shaping which is provided by a dielectric lens, the half-power beamwidths of the DFS antenna are approximately 50° in the E-plane and 76° in the H-plane. For the air substrate geometry, standard approximations (e.g. [8], pg. 32) predict a directivity of about 7 dB from these beam sizes, and the moment method results fall into the range of 7±.25 dB. On the quartz and silicon substrates, the directivity is greater since there is preferential radiation into the higher dielectric constant material [1]. Typically, patterns with the main lobe near broadside and sidelobes below -12 dB are possible over 8-10% bandwidths.

IV.3 Input Impedance

The input impedances for the five geometries given in Table 2 are presented in Figures 13-16. By comparing these results to the impedance of a single slot or a single folded-slot, it is seen that the general characteristics around the first resonance are similar. For the DFS, however, the resonance is shifted down in frequency relative to the other two types of antennas, occurring when the slot circumference is only around 0.8 λ_g. Consequently, the center frequency, which is given in the last column of Table 2, occurs in a band where the impedance is slowly varying. This leads to the broad-band nature of the double folded-slot antenna.

The results for the air-substrate designs A and B are shown in Figures 13 and 14, respectively. The impedance is between 55-75 Ω, with an imaginary part less than $\pm$j10 Ω, over a 20-25% bandwidth. The discrepancy between the experimental and calculated values is primarily due to interference from the (large) flange mount coaxial connector which is 2 cm from the antenna. Low sidelobe levels exist at the same frequencies at which the agreement is very good, but the sidelobes illuminate the connector outside the center frequency band (see Figure 11). In Figure 15, calculated values for the low frequency designs on quartz and silicon are shown. As expected, the impedance is scaled down by approximately $(\epsilon_{r,eff})^{\frac{1}{2}}$ relative to the levels for the air substrate, where $\epsilon_{r,eff}$ is the effective dielectric constant for the propagating CPW mode. Finally, the characteristics of a higher frequency design on silicon are given in Figure 16, in order to validate the full-wave analysis when the meander line is included. The parameters for this geometry differ from the design rules stated in Section IV.1, however this was the only measured data available to the authors. In general, the agreement between the calculated and experimental values is good, with the exception of the ripple which is present in the measurements. In this case, the additional structure can be explained by reflections at the interface between free-space and the Stycast lens ($\epsilon_r = 12$) that was attached to the substrate in order to simulate the semi-infinite dielectric half-space. A matching layer could be used to minimize this interference.

V. CONCLUSION

This paper has presented a broad investigation into the characteristics of single and double folded-slot antennas on semi-infinite substrates. These antennas are naturally suitable for coplanar waveguide feedline configurations and are therefore easily integrated with active devices. The double folded-slot antenna is a compact planar geometry which measures approximately one half of a guided wavelength on each side. It provides a broad-band input impedance and a directivity of at least 7 dB, depending on the substrate. Also included in the paper was the outline of a rigorous full-wave analysis that was used to characterize the antennas, along with design guidelines for DFS antennas on air, quartz and silicon substrates.

ACKNOWLEDGEMENTS

This work was supported by the Office of Naval Research and the NASA Center for Space Terahertz Technology. The authors would also like to thank Steve Mollenkopf for his help in making the measurements.

APPENDIX

This appendix provides an outline of the method which was used to compute the self-cell term of the admittance elements in Eqn. 3. It was shown in [6] that the co-polarized term, $Y_{\zeta\zeta}$, takes the following form in each dielectric half-space above and below the plane of the antenna metallization:

$$Y_{\zeta\zeta} = \frac{-2jY_i}{k}\left[k^2 A_{\zeta\zeta} - B_{\zeta\zeta}\right] G(\bar{r}/\bar{r}') \tag{5}$$

where Y_i is the intrinsic admittance of the dielectric medium, k is the wave number and

$$\begin{aligned} A_{\zeta\zeta} &= \int ds' \int ds\, T_s(\zeta',\xi') T_o(\zeta,\xi) \\ B_{\zeta\zeta} &= \int ds' \int ds\, \dot{T}_s(\zeta',\xi') \dot{T}_o(\zeta,\xi) \\ G(\bar{r}/\bar{r}') &= \frac{e^{-jkr}}{4\pi r} \\ r &= \sqrt{(\zeta-\zeta')^2 + (\xi-\xi')^2} \end{aligned} \tag{6}$$

where $\dot{T}(\zeta,\xi)$ denotes the derivative of T with respect to ζ. The variables T_o and T_s represent the testing and expansion functions, respectively, and the corresponding unprimed and primed coordinates refer to the domain of the 'observation' and 'source' cells. Due to the form of the PWS functions shown in Eqn. 2, $Y_{\zeta\zeta}$ is a summation of four sub-contributions which result from the interactions of the two sides of the expansion and test functions. Using the standard technique of adding and subtracting the singularity, each of the sub-contributions can be rewritten using this general form:

$$\begin{aligned} I &= \beta \int ds' \int ds \cos(k_m\zeta + \alpha)\left[\frac{\cos(kr)-1}{r} - \frac{j\sin(kr)}{r}\right] \\ &\quad + \beta \int ds' \int ds \frac{\cos(k_m\zeta+\alpha)}{r} \end{aligned} \tag{7}$$

where α and β are independent of the observation coordinates ζ and ξ The first integral on the right-hand side of Eqn. 7, I_1, is well-behaved in the limit as $r \to 0$ and is therefore easy to handle numerically. It is the second integral, I_2, for which an analytical solution is required, however this is not possible without some type of approximation to the integrand. In this case, a second order expansion of the cosine function has been used which puts I_2 in the following form:

$$I_2 \approx \beta \int ds' \int ds \left(\frac{\left(1-\frac{\alpha^2}{2}\right) - k_m\zeta\alpha - \frac{(\zeta k_m)^2}{2}}{r}\right) \tag{8}$$

For typical cell sizes, this approximation introduces less than 0.3% error. Furthermore, using relations from [9], a closed form solution for the interior integral may now be obtained:

$$
\begin{aligned}
I_2 \approx \beta \int ds' \Bigg[\Bigg[& \left(1 - \frac{(\alpha + \zeta' k_m)^2}{2}\right) \left\{ \tilde{\xi} \ln(\tilde{\zeta} + r) + \tilde{\zeta} \ln(\tilde{\xi} + r) \right\} \\
& - \left(\frac{k_m}{2} (\alpha + \zeta' k_m) \right) \left\{ \tilde{\xi} r + \tilde{\zeta}^2 \ln(\tilde{\xi} + r) \right\} \\
& - \left(\frac{k_m^2}{2} \right) \left\{ \frac{\tilde{\xi} \tilde{\zeta} r}{6} + \frac{\tilde{\zeta}^3 \ln(\tilde{\xi} + r)}{3} - \frac{\tilde{\xi}^3 \ln(\tilde{\zeta} + r)}{6} \right\} \Bigg]_{\zeta} \Bigg]_{\xi}
\end{aligned}
\tag{9}
$$

where

$$
\begin{aligned}
\tilde{\xi} &= \xi - \xi' \\
\tilde{\zeta} &= \zeta - \zeta' \\
r &= \sqrt{\tilde{\zeta}^2 + \tilde{\xi}^2}
\end{aligned}
\tag{10}
$$

The evaluation of the cross-polarization admittance elements, $Y_{\zeta\xi}$ and $Y_{\xi\zeta}$, can be handled in a similar manner.

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List of Figures

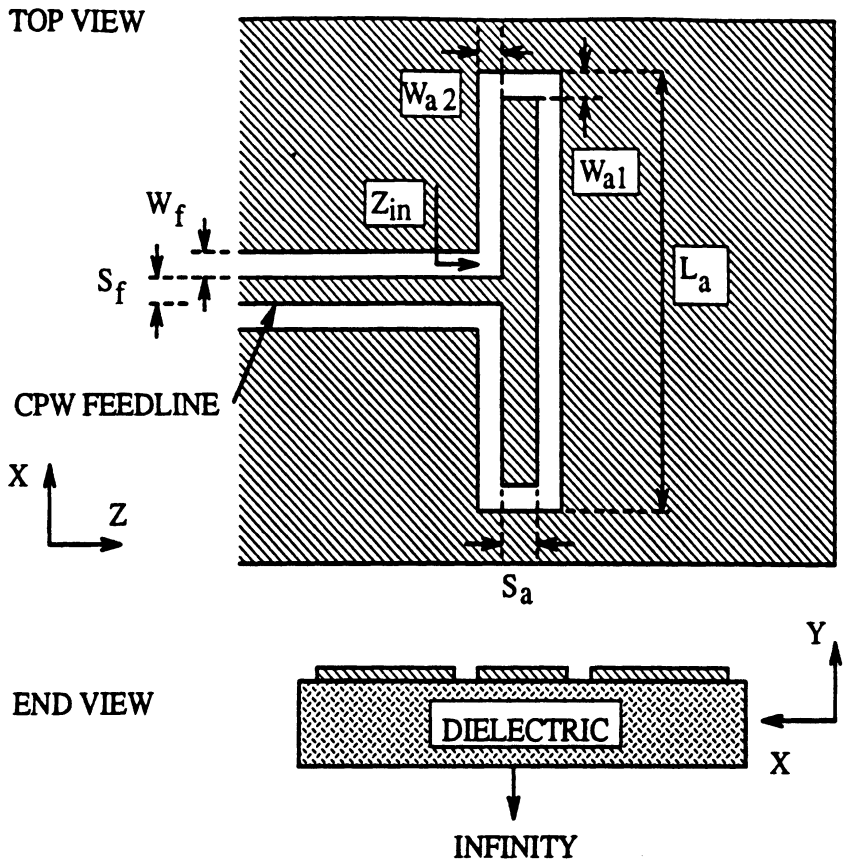

Figure 1: Single folded-slot antenna on a dielectric half-space (not to scale). The cross-hatched areas indicate metallization.

Design	ϵ_r	W_f / S_f	W_{a1} / W_{a2} / S_a / L_a
A	1.0	.10/.40	.10/.20/.10/10.0
B	4.0	.10/.40	.10/.20/.10/10.0
C	11.7	.10/.40	.10/.20/.10/10.0

Table 1: Parameters for different folded-slot antenna designs (refer to Figure 1). ϵ_r refers to the dielectric constant of the lower half-space and all dimensions are in millimeters.

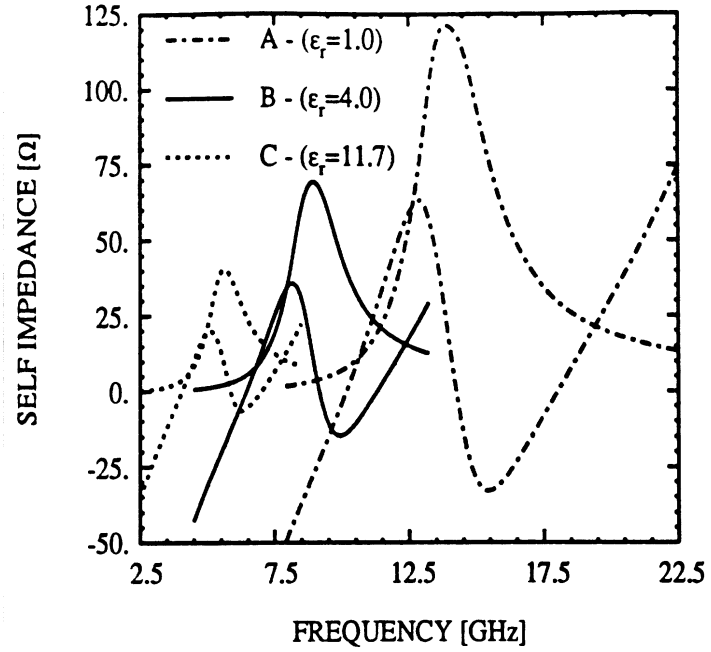

Figure 2: Calculated self impedances for folded-slot designs A, B, and C from Table 1.

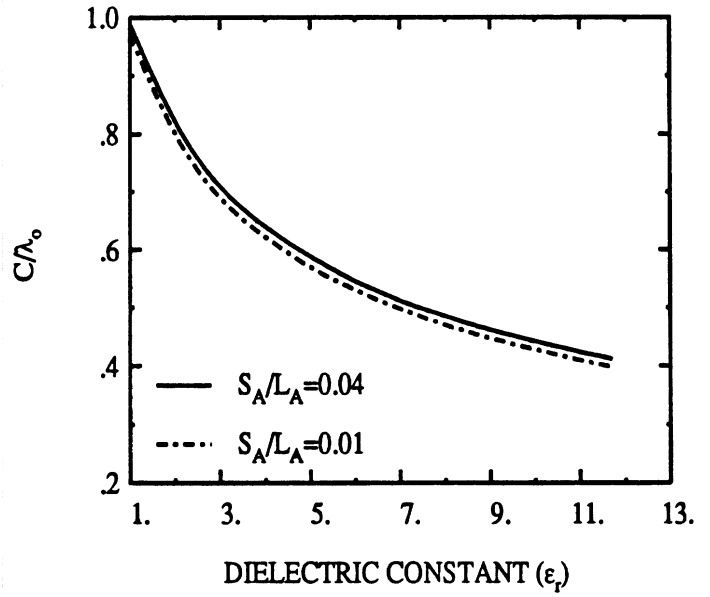

Figure 3: Resonant circumference of a folded-slot antenna versus the dielectric constant of the semi-infinite substrate. The antenna dimensions are $W_{a1}/L_a = 0.01$, $W_{a2}/L_a = 0.02$, $L_a = 10$ mm, and S_a is given in the figure. The results include the effects of the CPW feedline with dimensions $W_f = 0.1$ mm and $S_f = 0.4$ mm.

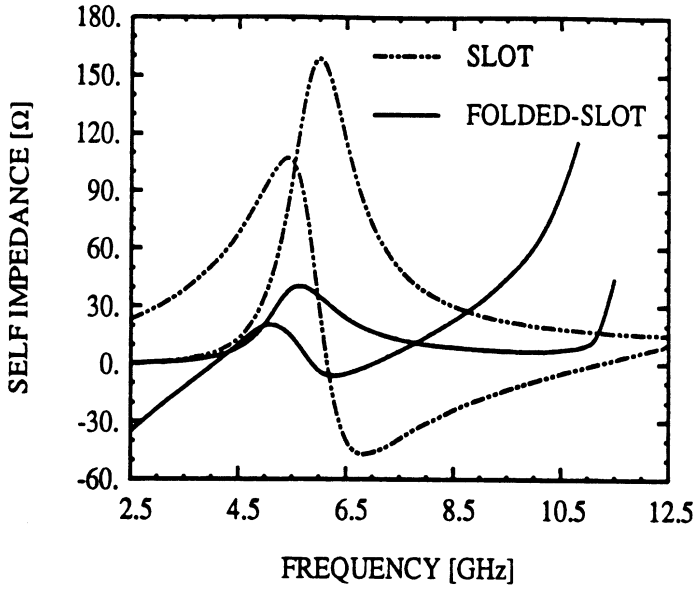

Figure 4: Calculated self impedances for folded-slot design C (ϵ_r = 11.7) from Table 1 and a comparable slot antenna. The dimensions of the slot are W_a/L_a = 0.02 and L_a = 10 mm.

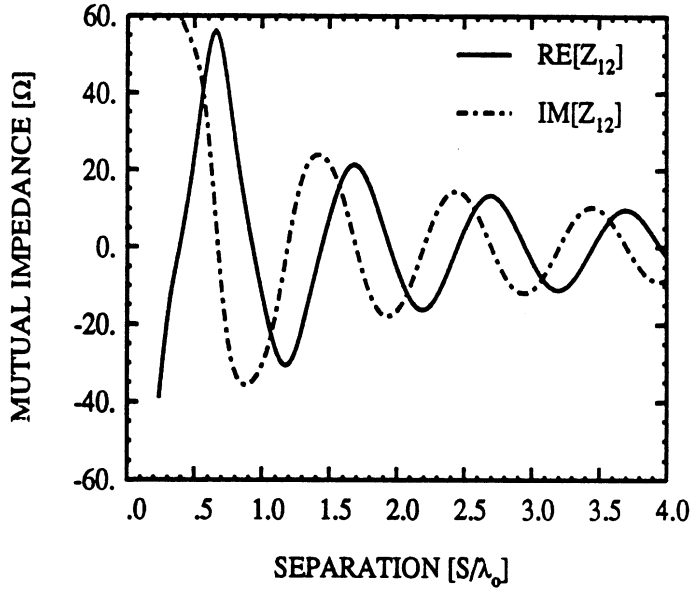

Figure 5: Calculated mutual impedance for two folded-slot antennas of design A (ϵ_r = 1.0) from Table 1 versus separation distance. The antennas are aligned in a broadside configuration, and the computations are performed at the first resonance of a single folded-slot (Circumference = $0.97\lambda_o$).

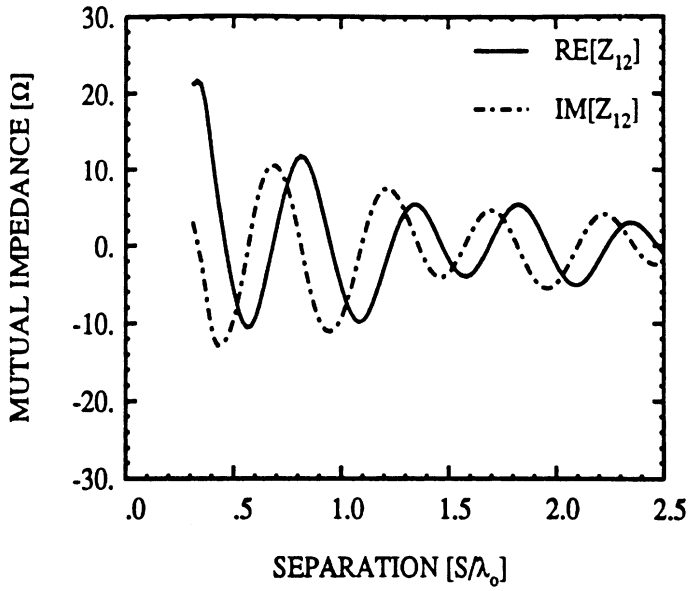

Figure 6: Calculated mutual impedance for two folded-slot antennas of design B ($\epsilon_r = 4.0$) from Table 1 versus separation distance (broadside configuration). The computations are performed at the first resonance of a single folded-slot (Circumference = $0.62\lambda_o$).

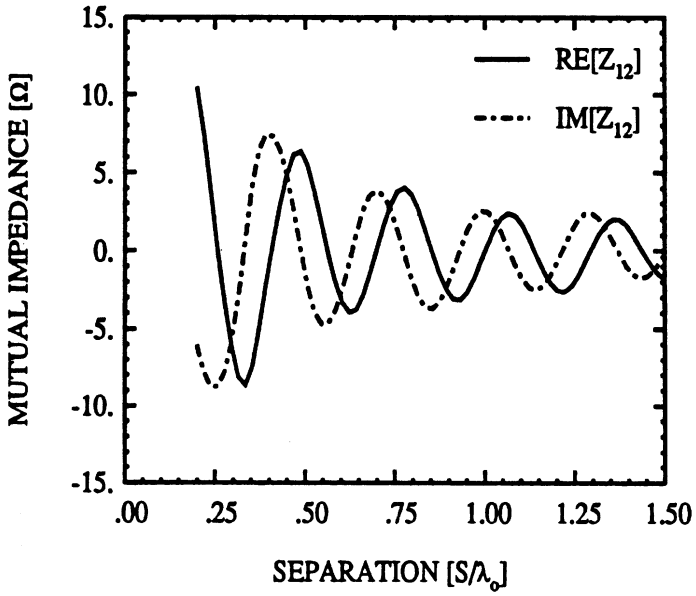

Figure 7: Calculated mutual impedance for two folded-slot antennas of design C ($\epsilon_r = 11.7$) from Table 1 versus separation distance (broadside configuration). The computations are performed at the first resonance of a single folded-slot (Circumference = $0.40\lambda_o$).

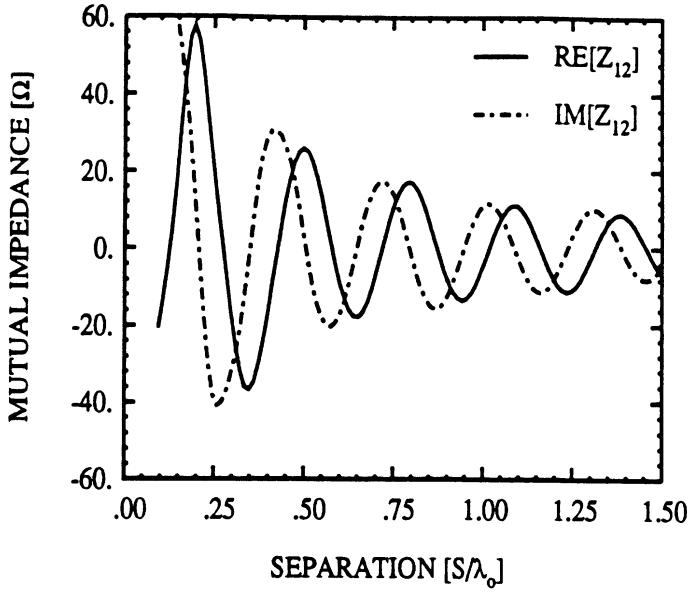

Figure 8: Calculated mutual impedance for two slot antennas on a silicon substrate ($\epsilon_r = 11.7$) versus separation distance, where the antenna dimensions are $W_a/L_a = 0.02$ and $L_a = 10$ mm. The antennas are aligned in a broadside configuration, and the computations are performed at the first resonance of a single slot ($L_a = 0.19\lambda_o$).

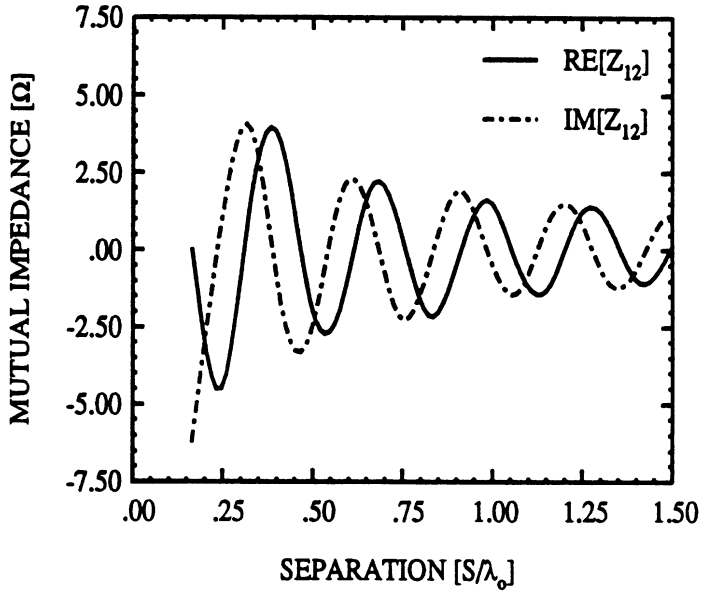

Figure 9: Calculated mutual impedance for two folded-slot antennas of design C ($\epsilon_r = 11.7$) from Table 1 versus separation distance (broadside configuration). The computations are performed at the second resonance of a single folded-slot (Circumference = $0.47\lambda_o$).

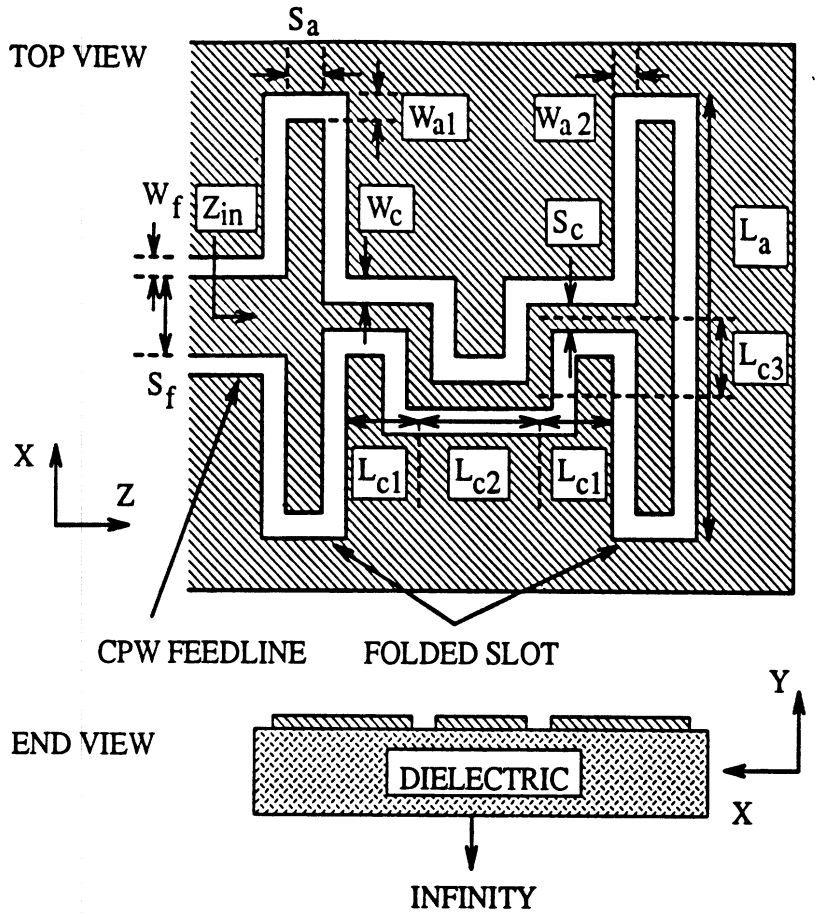

Figure 10: Double folded-slot antenna on a dielectric half-space (not to scale). The E-plane pattern is in a plane parallel with the feedline and normal to the page, at $\Phi = 90°$ and $\Theta = 0\text{-}180°$; the feedline is at $\Theta = 180°$.

Design	ϵ_r	W_f / S_f	W_{a1} / W_{a2} / S_a / L_a	W_c / S_c / L_{c1} / L_{c2} / L_{c3}	f_c
A	1.0	.100/3.30	.415/.415/.415/25.0	.415/.415/12.6/0.00/0.00	6.06
B	1.0	.100/3.30	.415/1.66/.415/25.0	.415/.415/12.6/0.00/0.00	5.68
C	4.0	.264/1.58	.264/.528/.264/15.8	.264/.264/4.17/4.17/1.65	6.05
D	11.7	.165/.495	.165/.330/.165/9.92	.165/.165/2.44/2.44/1.30	6.05
E	11.7	.060/.030	.040/.040/.150/2.55	.040/.070/.455/.700/.545	23.8

Table 2: Parameters for several double folded-slot antenna designs (refer to Figure 10). ϵ_r refers to the dielectric constant of the lower half-space. All dimensions are in millimeters and the center frequency, f_c, is in GHz.

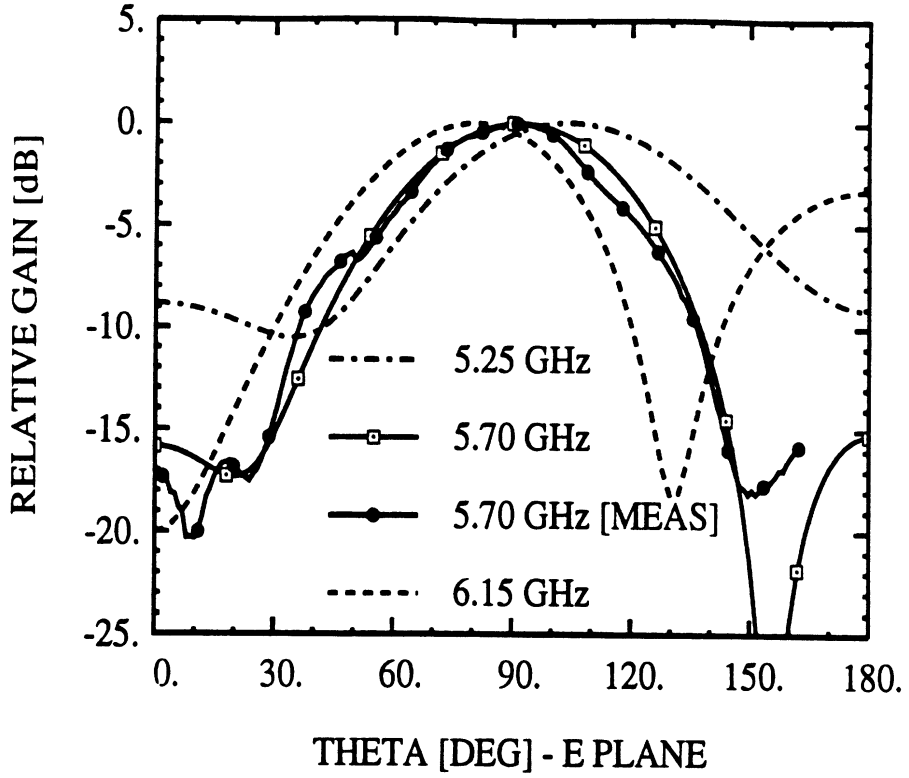

Figure 11: E-plane patterns for the double folded-slot antenna design B, at three different frequencies.

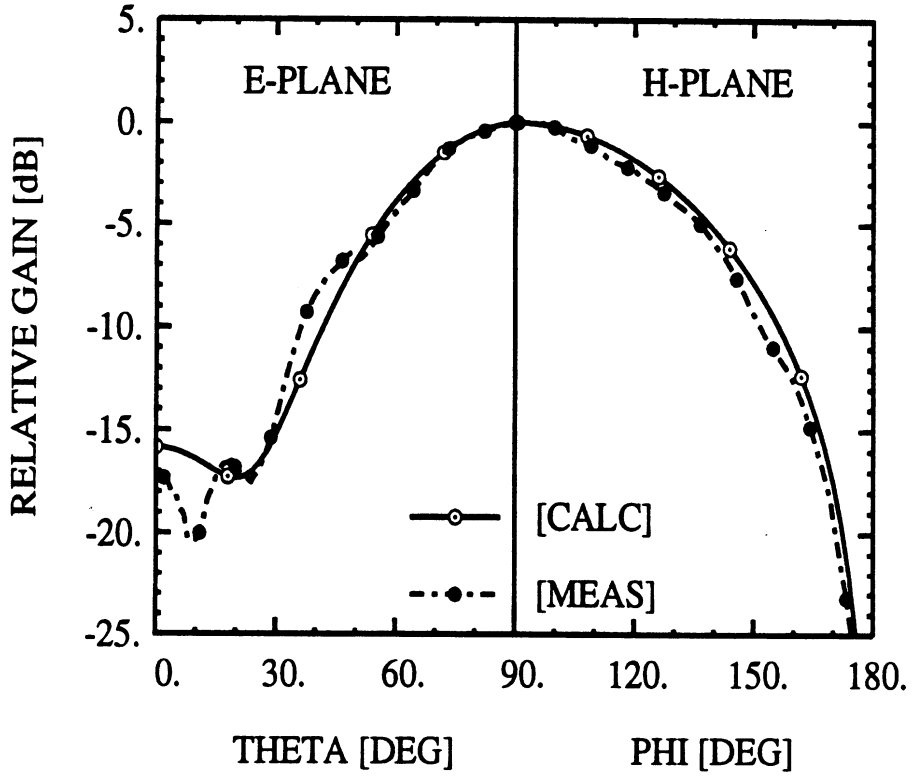

Figure 12: E- and H-plane patterns for the double folded-slot antenna design B at 5.7 GHz.

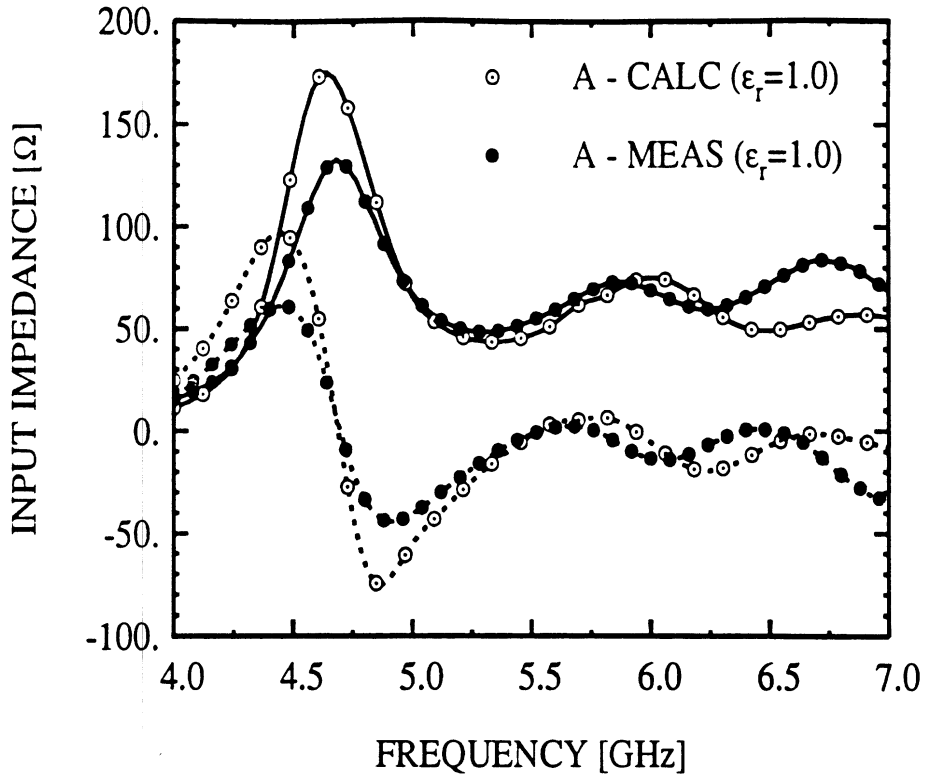

Figure 13: Calculated and measured input impedance for design A from Table 2.

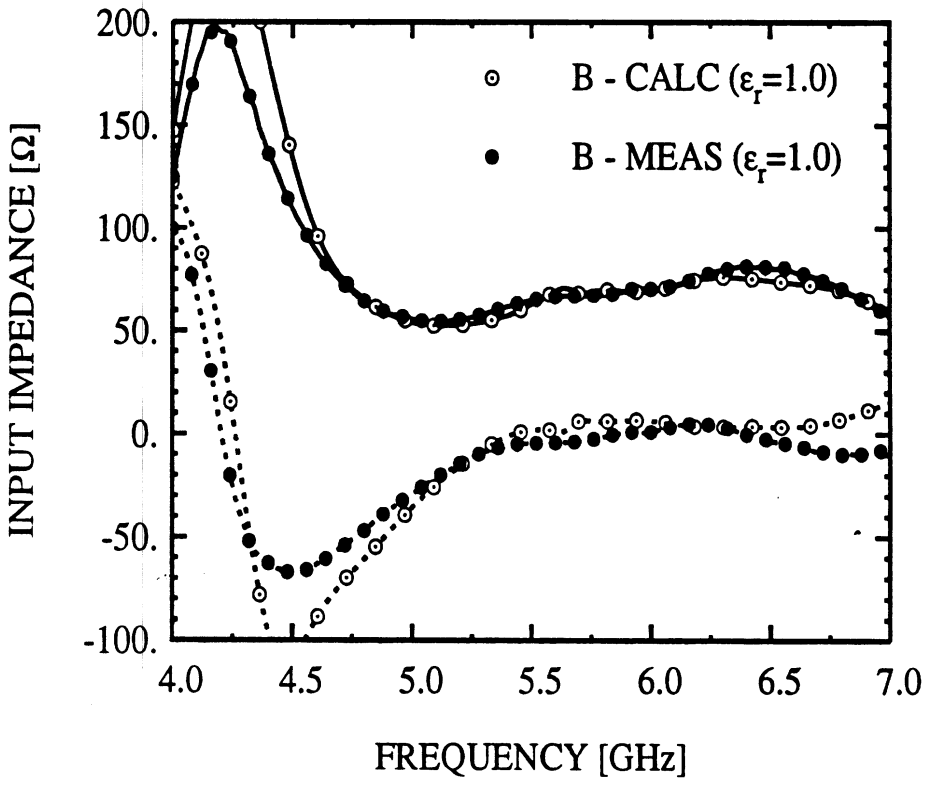

Figure 14: Calculated and measured input impedance for design B from Table 2.

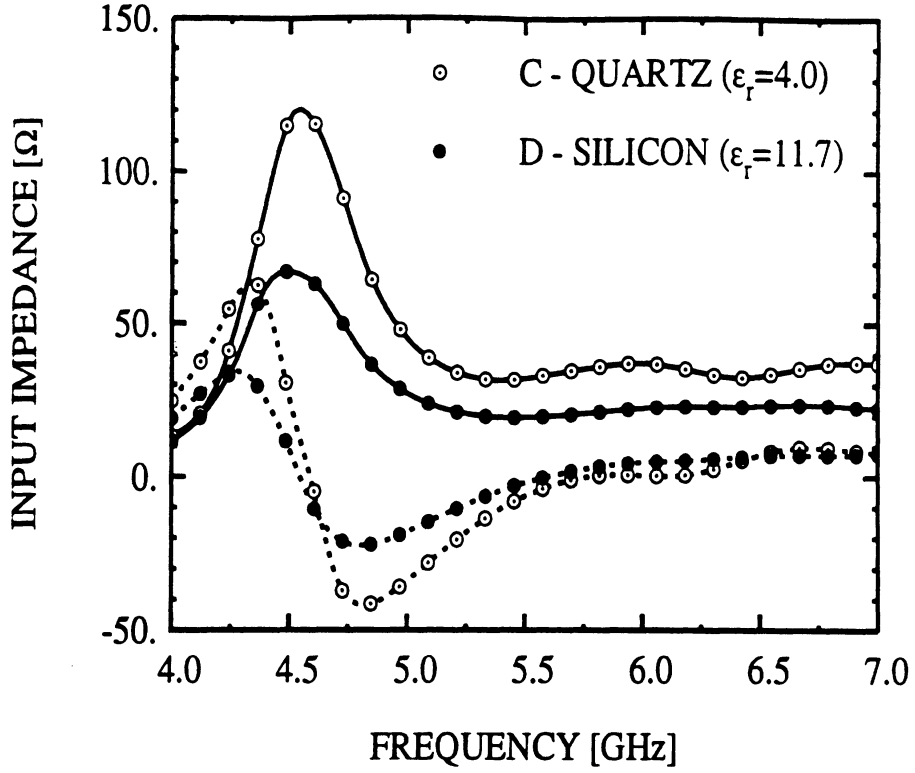

Figure 15: Calculated input impedance for designs C and D from Table 2.

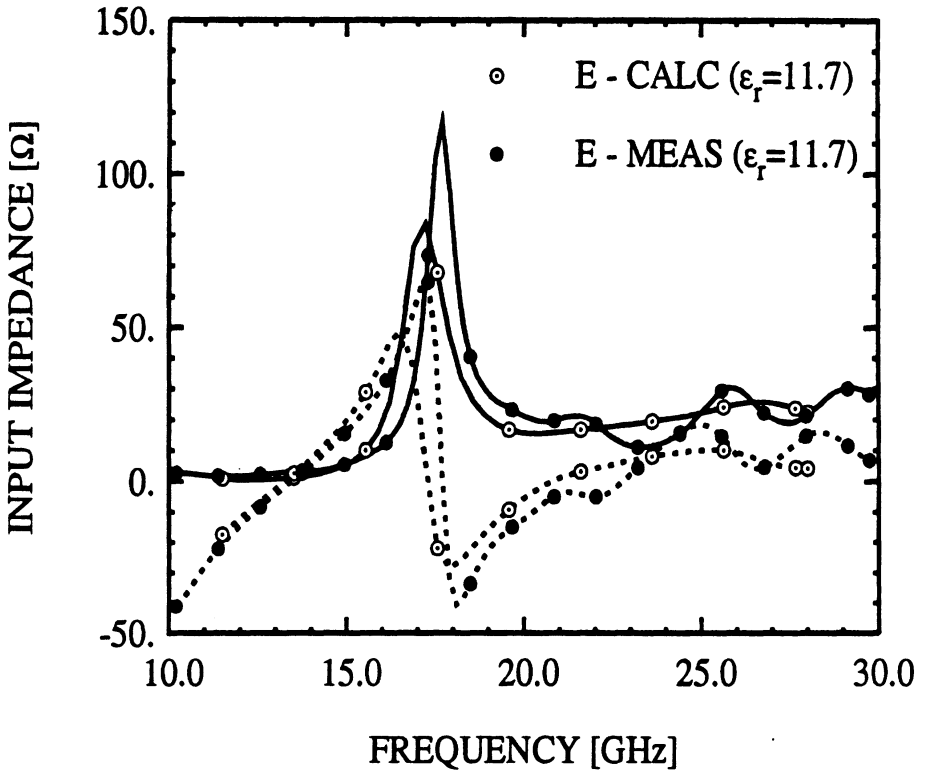

Figure 16: Calculated and measured input impedance for design E from Table 2. The measured data is from [11].

APPENDIX C

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Theoretical and Experimental Characterization of Microshield Circuits

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ABSTRACT

A theoretical and experimental study of the microshield line, a recently proposed new type of monolithic planar transmission line, is presented. The Space Domain Integral Equation method is used to analyze a specific discontinuity of the proposed line. It is shown that microshield line discontinuities tend to radiate less than the conventional coplanar waveguide (CPW) ones. In order to validate the theory, measurements are performed on scaled models in the range 10-18 GHz. The experimental and theoretical results are in good agreement. Moreover, it is shown that the microshield line can provide a wide range of characteristic impedances due to many available parameters of design.

1 INTRODUCTION

The microshield line, a new monolithic structure which can provide generic shapes appropriate for circuit and array applications, was proposed in [1]. This new geometry is characterized by low radiation loss [1], reduced electromagnetic interference [2] and compatibility to antennas of microstrip or aperture type [3]. In this configuration, the ground plane is warped to totally or partially surround the inner strip conductor as a shielding microcavity. Such a structure can be made monolithically using dielectric etching and metal deposition techniques as will be described below (see Fig. 1). In these lines the inner conductor can be printed on a thin substrate layer (Fig. 3(b)) or can be suspended in air by using membrane technology (Fig. 3(a)). As it has been demonstrated [4, 5], membranes can be effectively employed to provide high-efficiency monolithic antennas and arrays operating at very short wavelengths.

One of the advantages of the microshield line is that there is no need for via-holes or air-bridges for ground equalization because of the existence of the shielding microcavity. In addition, a wide range of characteristic impedances can be obtained due to the many available parameters in design. Moreover, preliminary theoretical analysis has shown that the microshield line discontinuities tend to radiate less than the CPW ones [1]. On the other hand, the presence of conductor losses is expected to limit the use of microshield lines and circuits to the lower end of the sub-mm-wave spectrum.

2 FABRICATION

The fabrication of microshield circuits is dependent on the thin dielectric membrane technology and the anisotropic etching of the supporting wafers. A Si membrane is a 3-layer $SiO_2/Si_3N_4/SiO_2$ structure which must be slightly in tension to yield flat and rigid self-supporting characteristics. The SiO_2 layers are made by high temperature thermal oxidation (1100°), while the Si_3N_4 layer is made by chemical vapor deposition at 800° [4]. After the development of the three-layer structure, the membranes are fabricated in two steps. First, an opening in the silicon-nitride layers is defined on the back of the wafer, and then the silicon is etched until a transparent membrane appears. The etching solution is anisotropic and yields pyramidal cavities which can be exploited for microshield transmission-lines. Figure 1 gives the most important steps of the procedure in a simplified way. Once the membranes are fabricated, it is easy to lithographically define several different microshield geometries for impedance and propagation constant measurements.

The microshield geometry can create the basis of a new technology and can lead to novel ideas in antenna and array design. Figure 2 shows a picture of a low-pass microshield filter exciting an aperture type trapezoidal antenna. This circuit has been made as a proof of fabrication feasibility and it does not present an optimized design. In fact, in order to successfully design this antenna configuration many important issues associated with the microshield geometry have to be studied and understood. Some of these issues are (i) dispersion (ii) parasitic radiation, (iii) transitions from conventional planar lines to microshield structures and (iv) electromagnetic coupling to neighboring circuit elements.

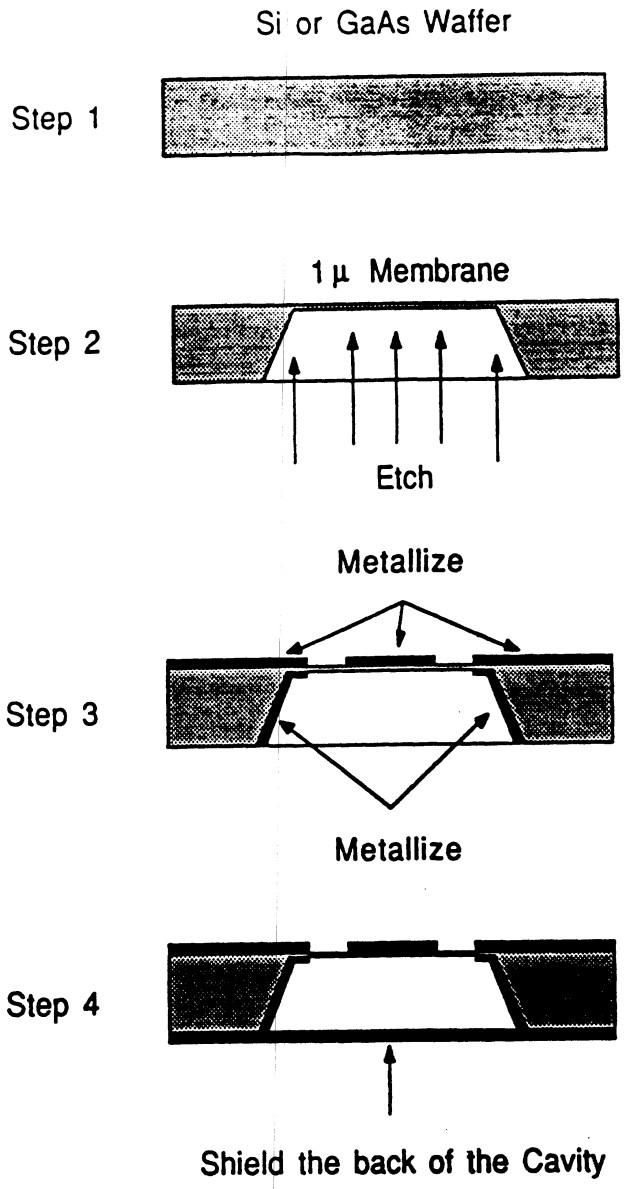

Figure 1: **Fabrication process for the microshield line.**

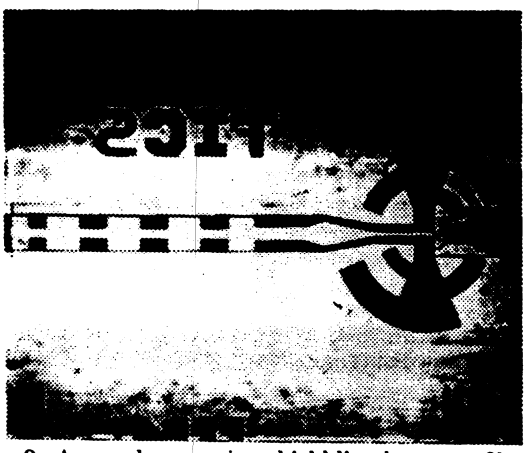

Figure 2: A membrane microshield line low-pass filter.

3 THEORY

The theoretical method is based on a space domain integral equation (SDIE) method [1, 6]. The original boundary problem is split into two simpler ones by introducing an equivalent magnetic current $\bar{M}_s$ on the slot aperture. This surface magnetic current radiates an electromagnetic field in the two regions, above and below the slots, so that the continuity of the tangential electric field on the surface of the slots is satisfied. The remaining boundary condition to be applied is the continuity of the tangential magnetic field on the surface of the slot apertures which leads to the desired integral equation. This integral equation is solved numerically using the method of moments where the unknown magnetic current is expanded in terms of appropriate basis functions. Then, Galerkin's method is applied to reduce this equation to a linear system of equations which is solved to provide the field distribution on the membrane slots. From the field distribution, the scattering parameters and radiation loss from the discontinuity under consideration are computed as functions of frequency using standard techniques [6]. The details of the SDIE method may be found in [1, 6].

4 SCALED MODEL MEASUREMENTS

Although the microshield line is intended for sub-mm wave applications, its experimental characterization can be best performed on scaled models. This is due to the fact that 2-port scattering parameters measurements are limited to 100 GHz from the state of the art vector systems. In addition, since the microshield line is a passive structure, most of the information obtained from the scattering parameter measurements, excluding conductor losses, can be scaled with frequency to the sub-mm wave region. In these models, the membrane of the microshield line has been replaced by a 30 mils duroid layer ($\epsilon_r = 2.2$) as shown in Figure 3(b). In this configuration, the strip conductor is printed on this duroid layer and is shielded by a cavity milled on a metal block. The RF measurements were performed in the 10-18 GHz frequency range on the HP 8510B Automatic Network Analyzer. To determine the circuit performance, a one-tier Thru-Reflect-Line (TRL) calibration has been performed to eliminate the effects of the connector discontinuity from the measured data.

5 RESULTS

The theoretical technique presented previously has been applied to a number of membrane and dielectric microshield and conventional coplanar discontinuities in order to compare circuit performance. The numerical results

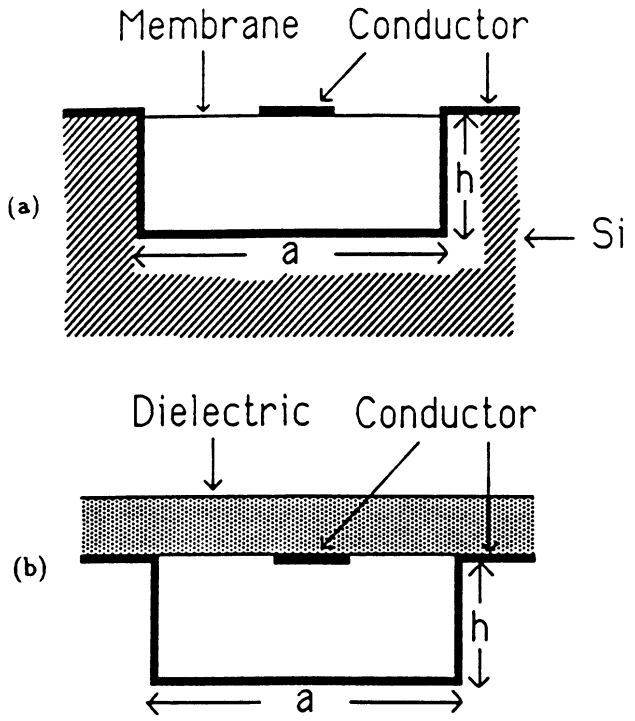

Figure 3: (a) A simplified cross section of the membrane microshield line. (b) The dielectric microshield line suitable for scaled measurements.

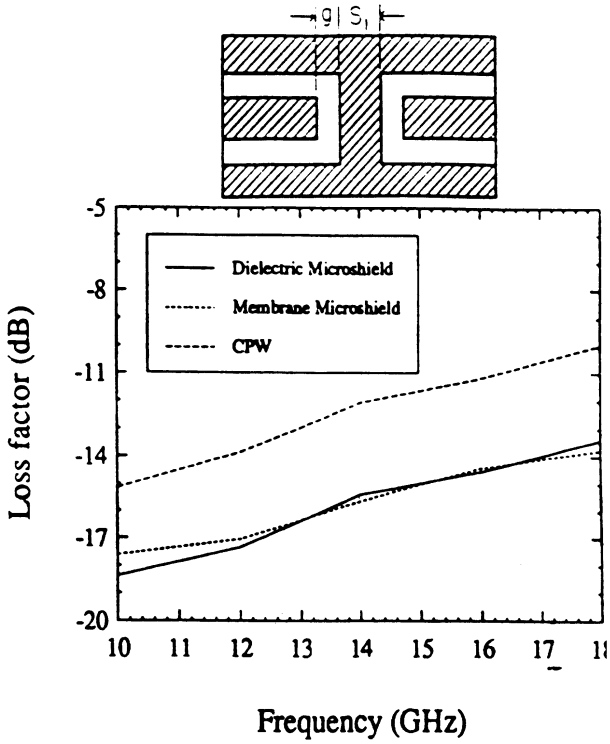

Figure 4: Radiation Loss factor of coupled open-ends di continuity (S_1=120 mils, g=20 mils).

of this study have been presented in [1] and provide very strong indications about the exciting low-loss performance of microshield structures. In this paper, the same methodology is applied to similar microshield discontinuities and the theoretical results in the form of scattering parameters are compared to experimental ones performed on scaled models. The specific discontinuity discussed here is the open-end coupled microshield line configuration with an inner conductor width of 60 mils, slot-width of 20 mils and microcavity width and height given by 100 mils and 50 mils, respectively. Figure 4 shows the radiation loss factor of such a discontinuity in the microshield line and is compared to that corresponding to conventional CPW. It can be seen that radiation from the coupled microshield open-ends is approximately one half the radiation from coupled open-ends made of conventional CPW. In addition, for this specific discontinuity with the above dimensions, the dielectric microshield line and the membrane microshield line have almost the same radiation loss factor.

For the same configuration, Figure 5 shows the scattering parameters and the loss factor as were evaluated theoretically and measured experimentally. The comparison between theory and experiment is very good. The ripple seen in the measured data is mainly due to the very small coupling between the two lines which intensifies the effect of connector repeatability. Other results on scaled mode will be shown in the Symposium. In addition to the scale models, a variety of membrane microshield discontinuiti have been fabricated and measurements of their scatterir parameters using a Cascade probe station are underwa Results from these measurements will be presented in tl Symposium.

Figure 6 gives the characteristic impedance of a m croshield line as a function of $S/(S+2*W)$ for a given ca ity size. This characteristic impedance has been obtain using a quasi-TEM analysis based on the Point Matchir Technique [7]. Recently, a closed form expression of tl characteristic impedance of the microshield line has be derived using Conformal Mapping techniques [2], whi will be presented in the symposium too.

6 ACKNOWLEDGMENTS

This work has been supported by the Office of Naval R search under contract No. N00014-92-J-1070 and by tl NASA Center for Space Terahertz Technology. The a thors would like to thank Prof. G. Rebeiz for his scientif support.

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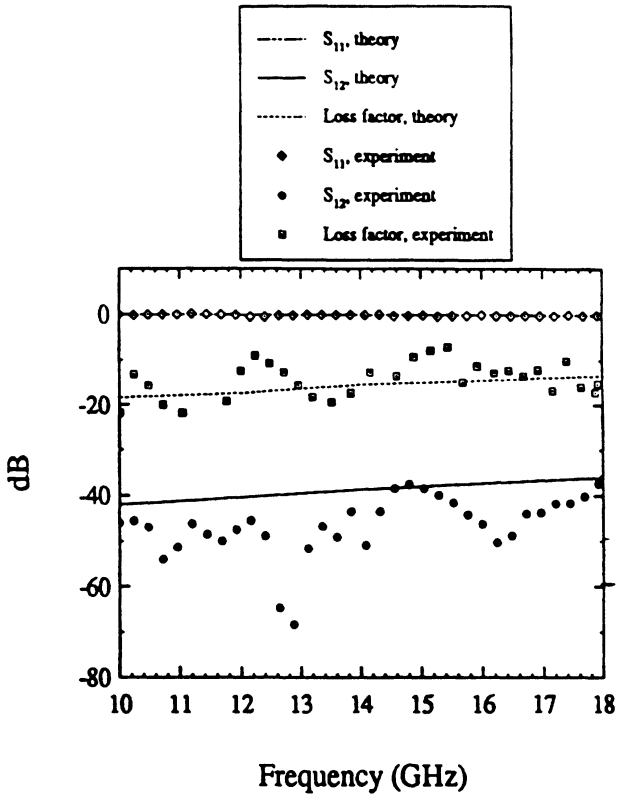

Figure 5: Scattering parameters and loss factor of coupled open-end dielectric microshield lines discontinuity (S_1=120 mils, g=20 mils).

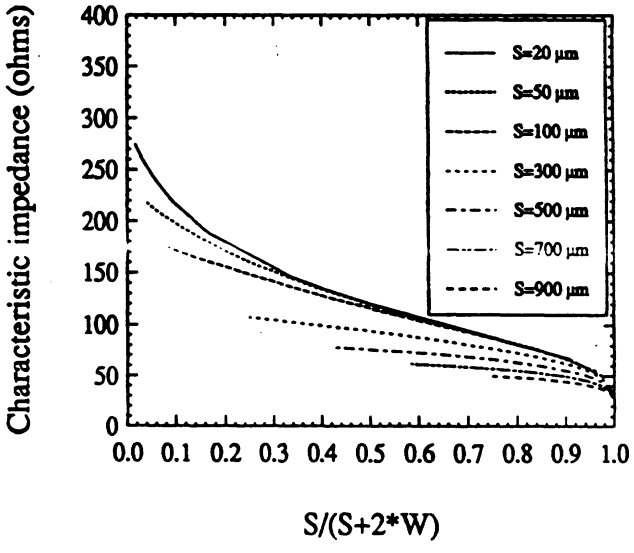

Figure 6: Characteristic impedance of a membrane microshield line (a=1200 μm, h=200 μm).

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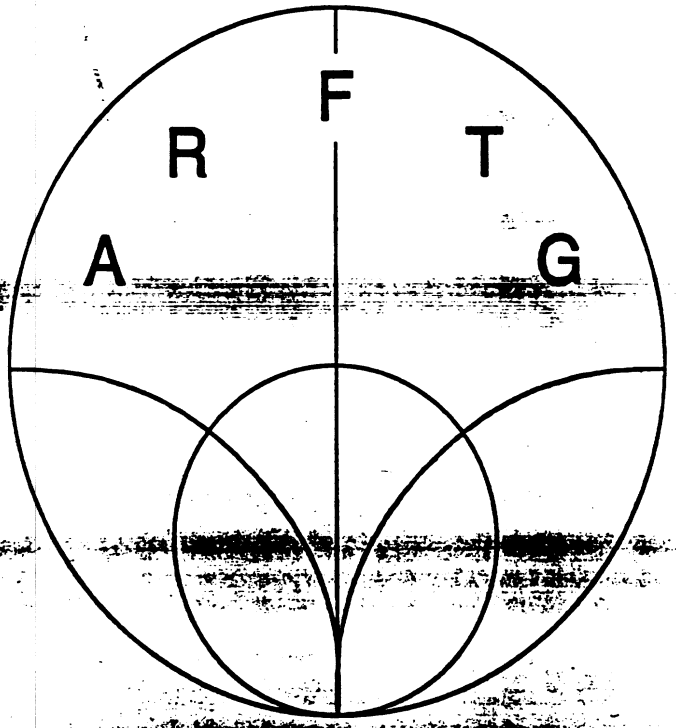

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MICROWAVE CHARACTERIZATION OF MICROSHIELD LINES

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ABSTRACT

An experimental characterization of a new type of monolithic planar transmission line, the microshield, is presented. Theoretically, it is shown to have the tendency to radiate less than the conventional coplanar waveguide (CPW). To characterize the line, experimental measurement of a scattering parameters of the microwave model is essential. This paper presents characterization through the design, fabrication and measurement of the line and a discontinuity such as the two coupled open-end line. The frequency dependence of the effective dielectric constant is measured and compared to the computed values. Although proposed for applications at lower sub-mm-wave frequencies, fabrication in a hybrid fashion allows for use at microwave frequencies. Present applications of microshield technology are seen in Microtech Cascade probes and feed throughs for package connections in CPW interconnects. In addition, it is possible to use the microshield to connect MMIC's by designing the shield width to accommodate an MMIC. Therefore characterization of the microshield line and discontinuities is necessary.

1 INTRODUCTION

The microshield is a novel monolithic planar transmission line that can provide generic shapes useful for circuit and array applications [1]. The geometry of the line exhibits lower radiation loss than the conventional coplanar waveguide (CPW) line, reduced electromagnetic interference [2] and compatibility to antennas of microstrip and aperture type [3].

Geometrically, the microshield can be made such that the ground plane totally or partially surrounds the inner conductor strip as a shielding microcavity (Fig1). This structure is made monolithically by incorporating dielectric etching and metal deposition techniques as well as thin film membrane technology. Since the dielectric substrate can be reduced to a micron, which is significantly smaller than a wavelength, a pure TEM mode is possible. Consequently, these lines are designed to operate in the lower sub-mm-wave region of the spectrum (frequencies up to 500 GHz).

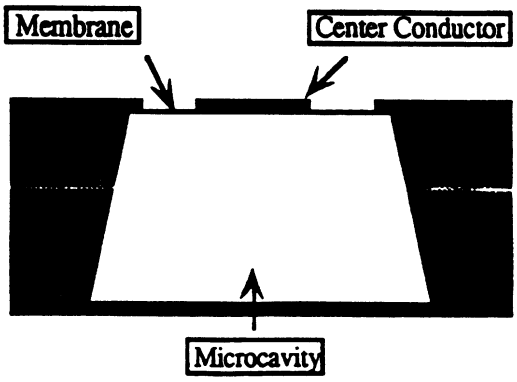

Figure 1: Microshield Transmission Line

Experimentally, characterization is obtained through a scaled model of the microshield line due to limitations in state of the art vector measurement systems to 100 GHz. Since the line is passive and linear, most characteristics, excluding conductor losses, can be obtained from the scattering parameter measurements which can be scaled with frequency to the lower sub-mm-wave region. These conductor losses which can be obtained from other studies on the CPW lines are expected to offer limitations in the use of the microshield lines for circuit applications.

As an advantage, the necessity for airbriges or via holes is eliminated since the center conducting line is in such close proximity to the microcavity for which the ground planes are tied together. In addition, a wide variety of characteristic impedances are obtained through variations in the design parameters such as microcavity height and width as well as the conductor and slot width. Finally, radiation losses are significantly lower than those of the conventional CPW or microstrip due to the microcavity enclosure.

Although the primary focus is on the characterization of the microshield for lower sub-mm-wave applications, at microwave frequencies a hybrid form of the microshield can be observed in Microtech Cascade probes and feed through packaging using CPW interconnects. In addition, it is possible to use the microshield for MMIC excitation by designing the shield width to accomodate the device. Therefore, characterization of the microshield line and discontinuities is necessary.

2 MICROWAVE MODEL

The fabrication of the microshield circuits is dependent on thin dielectric membrane technology [4] as well as anisotropic etching techniques. The structure consists of an inner strip conductor printed on thin substrate layer. This conductor is then shielded by the microcavity to form the microshield line.

The scaled microwave model is designed for operation in the frequency range of 10-15 GHz (Fig 2). This microwave model requires the design of a test fixture and circuits that effectively simulate geometrical characteristics of the microshield transmission line. Therefore, the microwave model looks very similar to the inverted microstrip line.

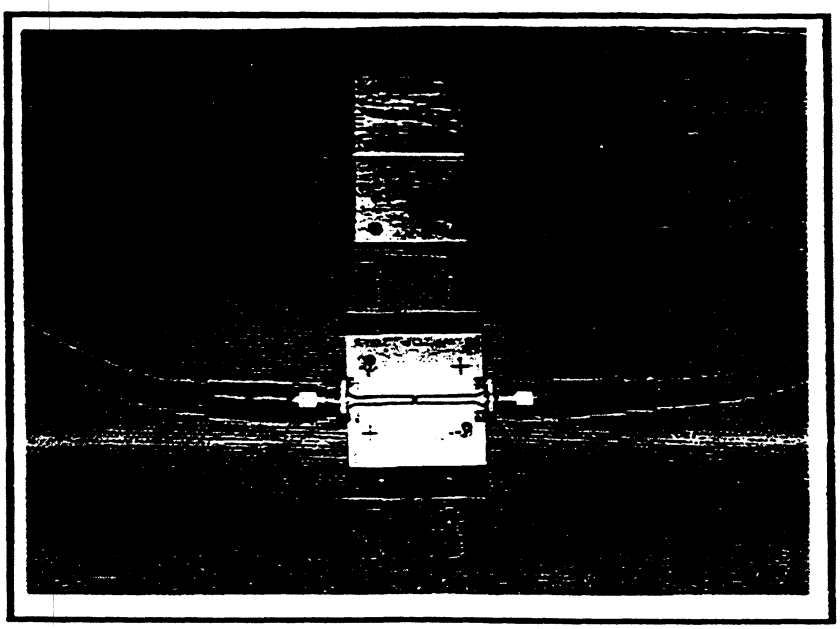

Figure 2: Microwave Model of the Microshield Transmission Line

The design criteria for the fixture requires matching of the fields at the discontinuity between coaxial excitation and transmission line. Thus, the resulting characterization is a tri-fold process. First, various transitions are evaluated to provide maximum excitation to the line. Second, the circuits are evaluated to determine the minimum thickness and dielectric constant of the substrate which are feasible for accurate characterization of the line. Thirdly, the results of the above processes are combined to evaluate the overall performance of the line.

The test fixture is designed so that a cavity encloses the conducting line. A cavity is machine milled into an aluminum block and then a conducting line, which is printed on a substrate, is center aligned over the cavity. Center positioning of the conducting line ensures excitation of the CPW mode and suppression of the slot mode in the line. Once alignment is obtained, the circuit substrate backing is supported by a PVC block on its edges to offer mechanical strength to the substrate surface and support for the coaxial connectors. After mounting the circuit, the connectors are placed on the circuit and secured for measurement.

3 CIRCUIT DESIGN AND FABRICATION CONSIDERATIONS

The circuits are designed for 10-15 GHz on duroid, $e_r = 2.2$, with substrate thickness of 30 mils. While thinner substrates have been tested, flexibility in the dielectric backing resulted in poor ground plane contact. This leads to leakage and poor measurement repeatability. For improvement, ground planes are included on the circuit surface to ensure contact of the cavity ground to the CPW ground. While this enhanced the performance, it is observed that a substrate thickness of 30 mils provides the most repeatable measurements for characterization.

To ensure excitation of the CPW mode, the ground planes of the CPW line are extended inside the cavity. Connection between the coaxial line and the CPW line are obtained by field matching rather than impedance matching. It is observed that the CPW line of 72 ohms matches optimally to coaxial line of 50 ohms [5]. Implementing the above considerations results in a fixture that is easily characterized during calibration.

The circuits are fabricated using standard photolithography and wet etching techniques. Due to the frequency range of interest, conventional wet etching techniques are sufficient given circuit dimensions.

4 MEASUREMENT CONSIDERATIONS

Characterization of the fixture and discontinuities are obtained through the Thru-Reflect-Line (TRL) calibration technique which eliminates the effects of the connector discontinuities from the measured data. Since precision calibration standards of the microshield microwave model are not available for the ANA, a two-tier de-embedding technique is utilized to characterize the line[5]. The two-tier de-embedding technique consists of calibrating the ANA using precision coaxial standards and then performing a calibration of the test fixture using the calibration standards designed for the line. For field matching, the transmission line is terminated with linear tapers.

Since the cavity structure is the basis for mechanical support in the fixture design, coaxial excitation was obtained using Omni Spectra flange mount tabs. These connectors have a Teflon diameter of 187 mils and a tab width of 60 mils. The connectors are modified to include ground connections for the CPW line and are mounted to the circuit via the test fixture. Proper contact is maintained by using silver conducting paint.

Experimentally, the propagation constant of the line is obtained from the measurement of a long delay line (Fig 3). For the characterization of discontinuity effects, the two-coupled open-

end line is measured. The scattering parameters are shown in Fig 4 and Fig 5 while the radiation loss factor is shown in Fig 6. The comparison between theory and experiment is very good. The ripple seen in the measured data is mainly due to the very small coupling between the two slot lines which intensifies the effect of connector repeatability.

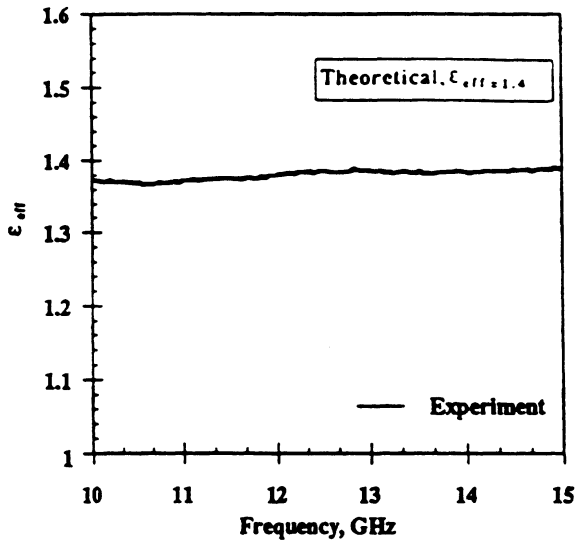

Figure 3: Effective Dielectric Constant of the Microshield Microwave Model

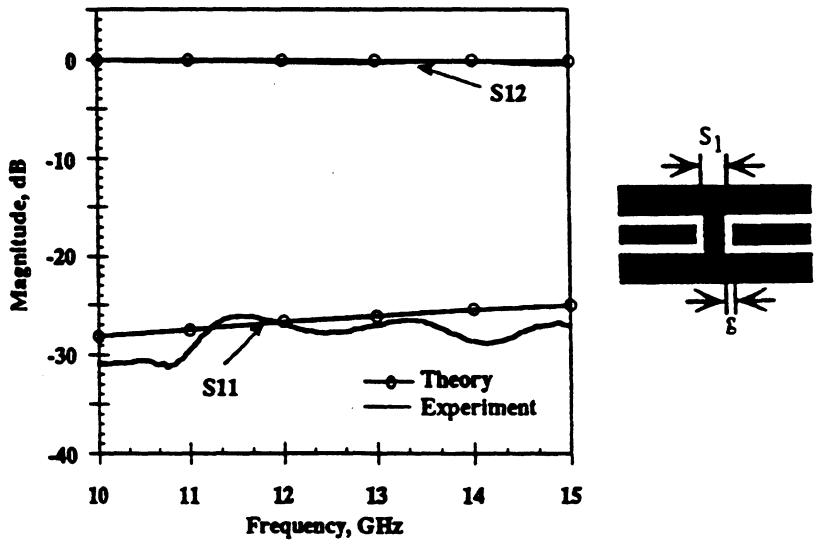

Figure 4: Two Coupled Open End Line Scattering Parameter Magnitude (S_1=20 mils and g = 10 mils)

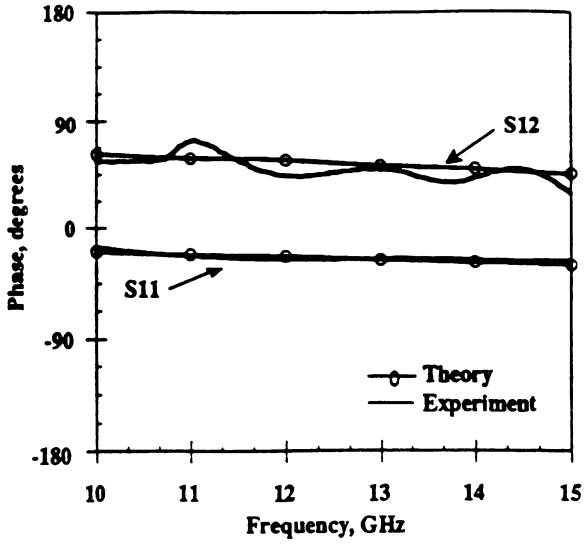

Figure 5: Two Coupled Open End Line Scattering Parameter Phase (S_1=20 mils and g = 10 mils)

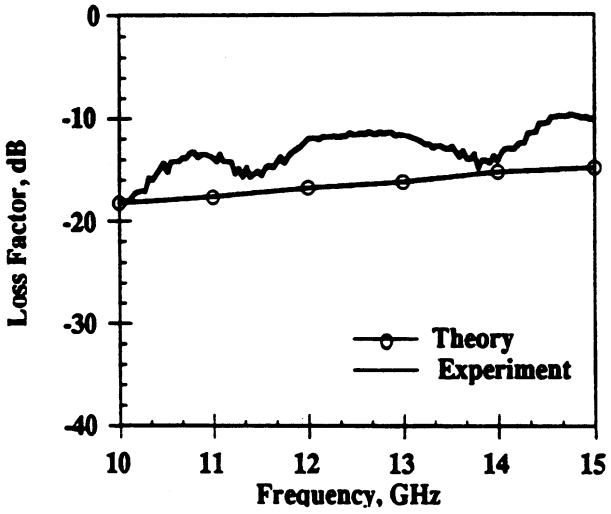

Figure 6: Two Coupled Open-End Line Radiation Loss Factor (S_1=20 mils and g = 10 mils)

5 CONCLUSION

A preliminary characterization is shown for the microwave model of the microshield transmission line. Circuit design and fabrication procedures have been presented. In addition, the experimental setup to measure the scattering parameters has been described. The results of this prelimenary study indeed show less radiation than the conventional coplanar waveguide (CPW) lines in range of 10-15 GHz.

6 ACKNOWLEDGEMENTS

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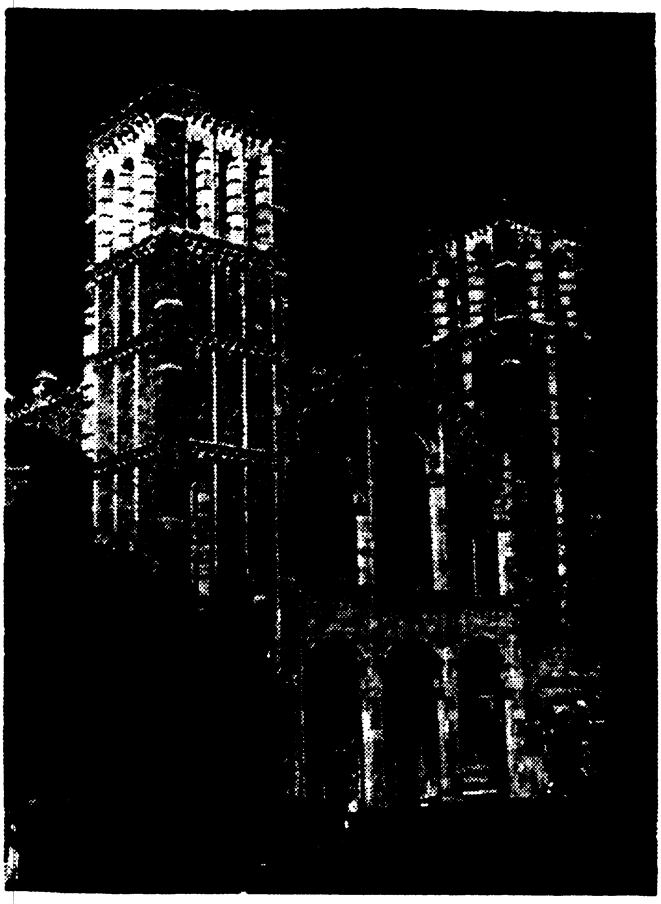

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EXPERIMENTAL STUDY OF MICROMACHINED CIRCUITS

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1.0 Abstract

Planarization of transmission lines such as microstrip, stripline, and coplanar provide enhanced flexibility in array design, compatibility to active devices and radiating elements, as well as reduced volume and weight. However, many unwanted frequency dependent mechanisms are introduced from these planar lines which cause degradation in the electrical performance of the circuit. As a result, the development of new geometries which reduce the effect of such mechanisms as ohmic loss and electromagnetic interference without affecting the monolithic character will result in extended operating frequencies and improved electrical performance of circuits and arrays. This paper presents the development of micromachined circuits which provide shielding of conventional lines using micromachining techniques. Presented is a description of the fabrication and characterization of these circuits. In addition, the study will show information about the propagation characteristics of the line and scattering parameters for a variety of micromachined circuits with comparison to theoretical and conventional circuit geometries.

2.0 Introduction

The thrust for the development of cost effective, lightweight electrical systems which exhibit improved electrical performance can be attributed to communications, commercial and military applications. One application in the area of communications is for the development of miniature satellites, microsats, which contribute to reduction in weight and improved fuel economy. Commercial applications will benefit from this development of high intelligence highway systems which require parallel processing of vast amounts of information transfer to maintain efficient operation of such systems. On the other hand, military applications will require development of PIN cards used for identifying military personel.Thus, the impetus for investigating micromachined circuits is due to the strong desire to develop inexpensive circuits that provide improved electrical performance with reduced volume and weight.

Currently, monolithic quasi-planar geometries which exhibit electrical and geometrical resemblance to waveguide shielded transmission lines and circuits are possible to implement due to recent advances in semiconductor processing techniques. Silicon based monolithic waveguides have been successfully developed for use in the sub-millimeter wave frequencies using silicon

micromachining techniques by JPL [1] and University of Michigan[2]. The waveguide is split along the broad wall and each half is formed by etching a channel through an appropriately oriented silicon wafer. Finally, a polyamide bonding technique is used to glue the etched channels to a smooth silicon wafer. In addition their performance has been measured and has been found very satisfactory[1].

Similarly, a shielded transmission line structure, Figure 1, can be developed by replacing the waveguide with a cavity which is etched into Si using KOH and then metallized using evaporation techniques. Then the planar transmission line is created by metal deposition on the Si semiconductor substrate and attached to the original wafer using electrobonding techniques. The results are lines and circuits which evolve from the conventional metallic waveguide and waveguide-shielded components with the advantages mentioned above.

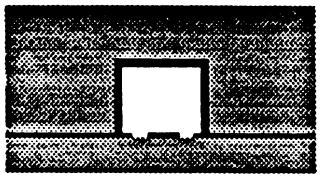

FIGURE 1. Micromachined CPW

As a result, this study will present the development of micromachined circuit, which use an etched cavity as a shield to planar geometries. After describing the fabrication and experimental procedures needed to characterize these novel circuits, scattering parameter measurements will be shown. Finally, results regarding the propagating characteristics of the line and a variety of circuit geometries will be presented and compared to theoretical models as well as conventional geometries.

3.0 Fabrication Procedure

In order to implement the development of a micromachined circuits, technology resulting from recent advances in semiconductor processes is used. These circuits are created by attaching the shielding structure to the planar line structure using electrobonding techniques. Although the shield and lines require the use of standard photolithography, the planar lines use a bilayer process technique for metal definition while the shield uses anisotropic wet etching methods for the development of the cavity structure.

Initially, a Si wafer having a membrane ($SiO_2/Si_3N_4/SiO_2$) dielectric surface is used to develop the cavity structure since depths of varying heights are required. Using photolithography to define the areas to be etched, the first oxide layer is etched using BHF while the nitride layer is etched using plasma etching. After repatterning the wafer to protect the areas to be etched later, the second oxide layer is removed while the remaining membrane layers serve as a mask for any unpatterened sections of wafer. Once the initial depth is obtained for the alignment marks, the remaining cavity areas are then exposed and etched to the required depth. The result is the development of a structure which has sections etched entirely through the wafer, the alignment marks,

and sections etched partially through, the cavities. Once the etch is complete, the shielding portion of the micromachined circuit is metallized using evaporation techniques.

Secondly, transmission lines are designed which consist of calibration standards and various circuit geometries necessary to characterize the electrical performance of the micromachined circuits. The lines, developed on a separate wafer, use photolithography to pattern circuit areas and the bilayer process to develop the appropriate line depth and width with the use of evaporation techniques.

Lastly, the micromachined circuits are developed by aligning the cavity structure to the transmission line structure. Once aligned, they are secured using electrobonding methods.

4.0 Measurement Procedure

Characterization of the circuits require the use of the following experimental arrangement: an HP 8510B Network Analyzer modified to operate up to 40 GHz, an Alessi Probe Station, and Cascade Probe Tips. To reduce the effects of possible substrate modes in the high resistivity silicon substrate, the circuits are isolated from the wafer chuck by 1/8" thick 5880 duroid, er=2.2.

To accurately measure the circuit performance of the micromachined circuits, the Thru-Reflect-Line (TRL) calibration technique is used. In order to perform this calibration, standards were fabricated using the above process. A one tier de-embedding technique was used for on-wafer calibration which calibrates the system reference plane along the transmission line. As a result, the calibration takes into account all transitions between the ANA and the reference plane.

The micromachined circuit, Figure 2, requires several transitions along the feed line to excite the micromachined circuit. The first transition is a taper between two 50 ohm sections of cpw-line. This transition is necessary to provide excitation to the desired line via the Cascade 150 μm pitch probes with minimal mismatch to the probes. The input port, having center conductor width of 100μm and slot width of 60 μm, is transitioned into a line with center conductor width of 180 μm and slot width of 130 μm. The second transition occurs between cpw and micromachined cpw circuit. The micromachined circuit is of coplanar type line which includes a micromachined shielding cavity having height of 200 μm and width of 800 μm. Subsequently, the required input line of all circuits measured will be of this type.

FIGURE 2. Micromachined circuit with various transitions

5.0 Measurements and Discussion

5.1 Philosopy of the Experimental Study

In order to facilitate a complete preliminary study of micromachined circuits, it is necessary to compare the measured results to both theoretical models as well as conventional geometries.

The *theoretical model* used for the micromachined circuits is based on the space domain integral equation (SDIE). With the appropriate Green's function for the lower half space and upper cavity region of the two dimensional circuit, unknown magnetic surface currents used to replace the slots, M_S, can be determined for a given electric source, J_S, using the method of moments. Once M_S is known, Galerkin's method is applied to reduce the above integral equation to a linear system of equations.For a given field distribution, the scattering parameters of the equivalent network is computed using standard techniques. [3,4]

The *coplanar waveguide* circuits, Figure 3b, are design to be identical in geometry to the micromachined planar circuits, Figure 3a. However, the design includes separate calibration standards for the cpw and micromachined circuits.

The resulting measurement will therefore show the response of micromachined circuits as compared to the theoretical model and conventional coplanar waveguide.

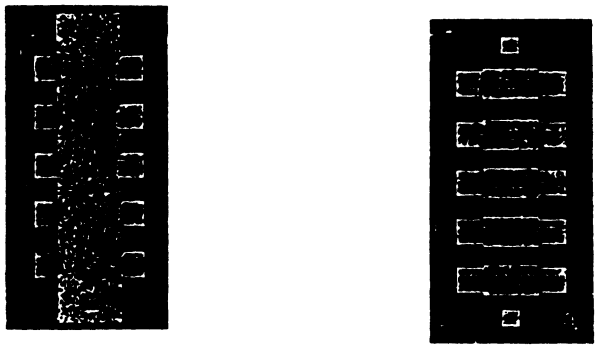

FIGURE 3. (a) Micromachined Circuits and (b) Open CPW Circuits

5.2 Measurements

A through line is used to provide information about the propagating characteristics of the micromachined transmission line. Figure 4 below shows the effective dielectric of a line having length of 2088μm and dimensions as stated above. The results show good agreement between the measured micromachined circuit and the theoretical model, which is based on Full Wave Analysis[3].

The two circuit designs presented are an open end series stub in Figure 5a, designed to have gap spacing of 30 μm, and open end gap in Figure 5b, designed to resonate at 30 GHz with resonate stub length of 1086μm

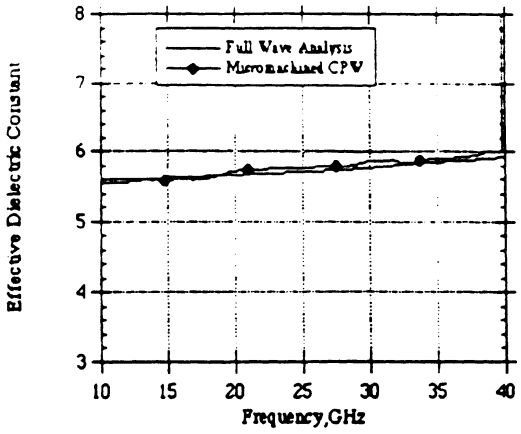

FIGURE 4. Effective Dielectric Constant

and slot width of 30 μm. The scattering parameters for the above circuits have been measured and are compared to the theoretical model for the micromachined cpw circuit. In addition they are compared to conventional cpw circuits of the same type.

(a) Open End Series Stub (b) Open End Gap

FIGURE 5. (a) Open End Series Stub and (b) Open End Gap

For the open end series stub in Figure A1.a, theory and experiment are in excellent agreement both in magnitude and phase as seen in Figures A1.b and A1.c. For the same circuit, comparison with the cpw line is shown in FiguresA2.a and A2.b. The line geometry is identical for both circuits, however, the micromachined circuit provides a shielding environment. In Figure A2.c, the total loss of this micromachined circuit varies between 6 dB and 2 dB at the high end below that of conventional cpw lines.

The open end gap in Figure B1.a, shows very close agreement in magnitude and phase with the theoretical results as seen in Figures B1.b and B1.c. As stated initially, it is very important to avoid distortion of the circuit performance when the shield is included. As a result of Figures B2.a and B2.b, comparison between the micromachined circuit and cpw show similarities in the overall circuit performance. The distinction between the lines occur when observing the total loss of the circuits. In Figure B2.c, the total loss, which is again reduced, indicates improvement in the overall performance of the circuit due to the micromachined cavity of the line.

To indicate the potential for this technology, Figure 6 shows a geometrical description of a milled circuit as compared to the new micromachined circuits. The milled represents one circuit while the micromachined circuit represents 5 different circuits housed on the silicon wafer that is about 1/6 of a 3" wafer.

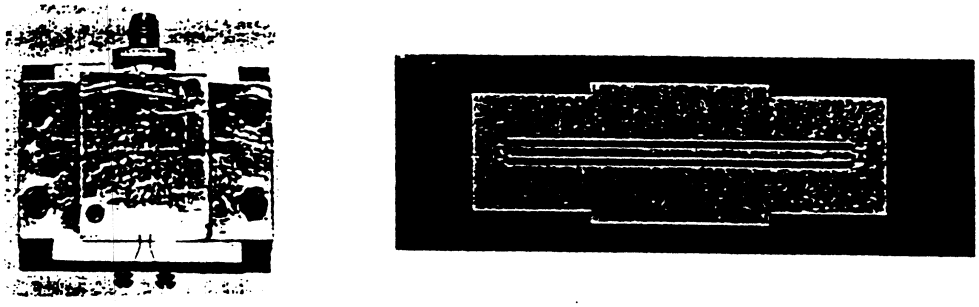

FIGURE 6. Milled Circuit and Micromachined Circuit

In addition to the physical reduction in the size and volume, circuit geometries of similar type indicate promise for applications at terahertz frequencies. However, of the two, the micromachined circuits offer the most flexibility in testing due to state of the art measurement systems available namely the probe station. These circuits and system offer more repeatable measurements along with ease in the fabrication methods used. Figure 7 shows the loss performance of similar geometries between the micromachined and milled circuit. Since the circuits are passive in nature, losses, except ohmic, can be scaled appropriately to the terahertz frequencies to give reasonable indicators of expected circuit performance.

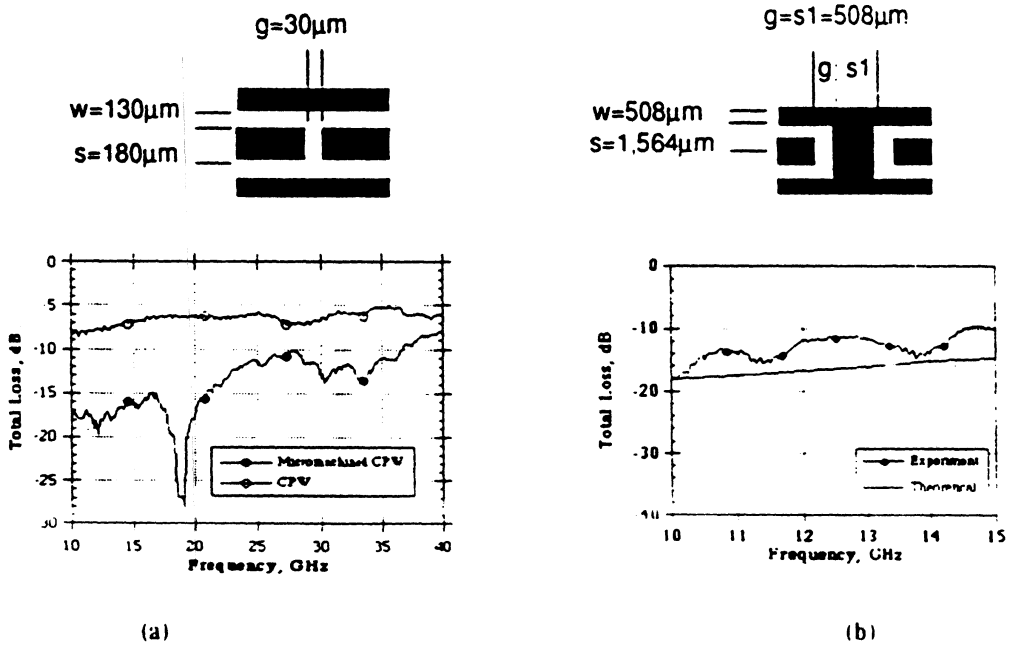

FIGURE 7. Losses of (a) Micromacnined circuit vs. (b) Milled circuit

6.0 Summary

Micromachined circuits have been built and tested. The results show that the scattering parameter measurements are in very good agreement with the theoretical model used. The study also shows comparison between the cpw and micromachined cpw. The results indicate consistently that the shielded geometry results in reduction in the total loss of the various circuits measured. When compared to machine milled circuits of similar geometry, the losses are comparable. As a result, micromachined circuits show encouraging preliminary results which warrant further development of these lines for more complicated geometries.

Acknowledgments

This work was partially supported by the Office of Naval Research and the NASA Center of Space Terahertz Technology. The authors would also like to thank Nihad Dib for theoretical model contributions.

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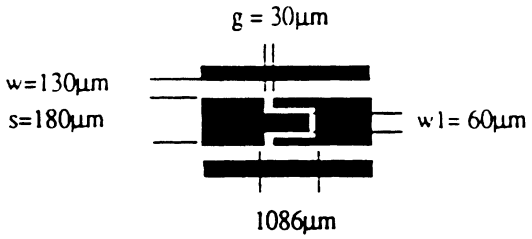
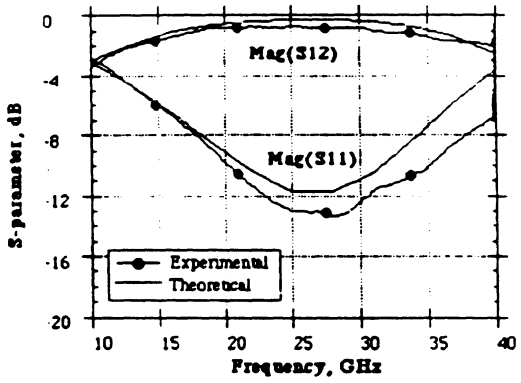
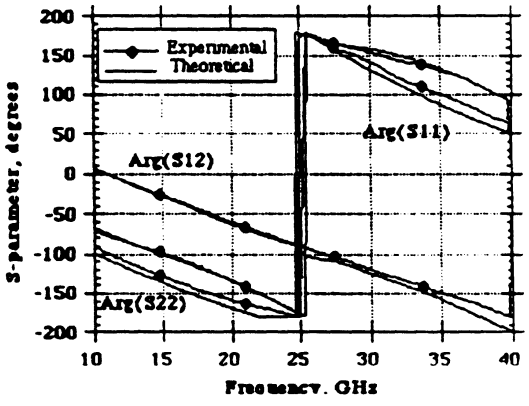
Figures



(a) Physical Geometry

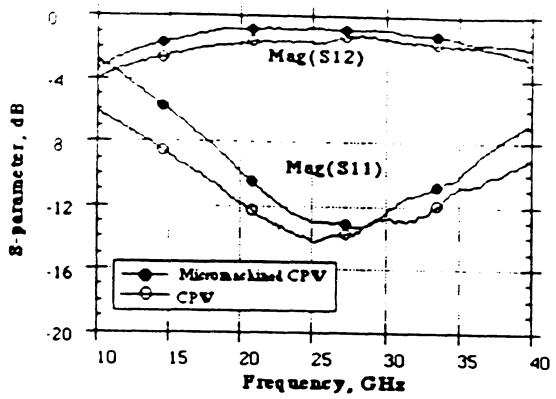


(a) Magnitude of Scattering Parameter

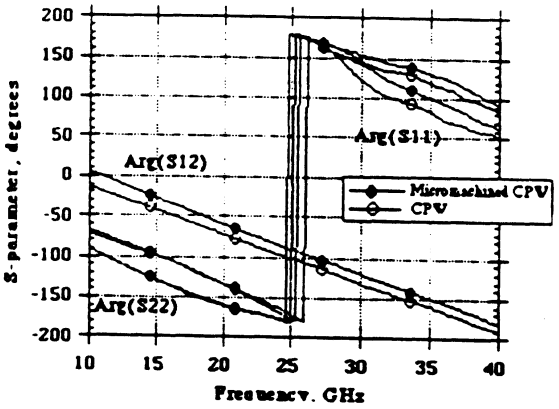


(b) Phase of Scattering Parameter

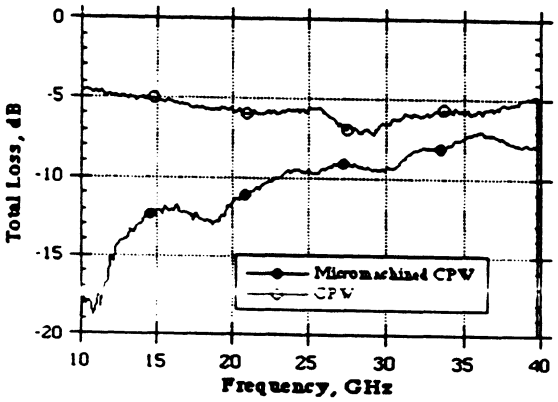
FIGURE A1. Micromachined CPW, Theoretical vs. Experimental: Open End Series Stub



(a) Magnitude of Scattering Parameters

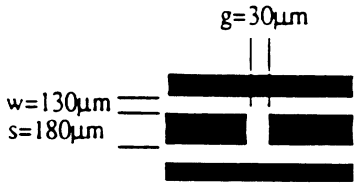


(b) Phase of Scattering Parameters

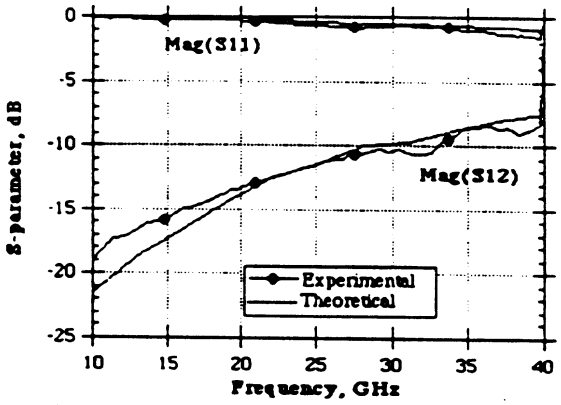


(c) Total loss

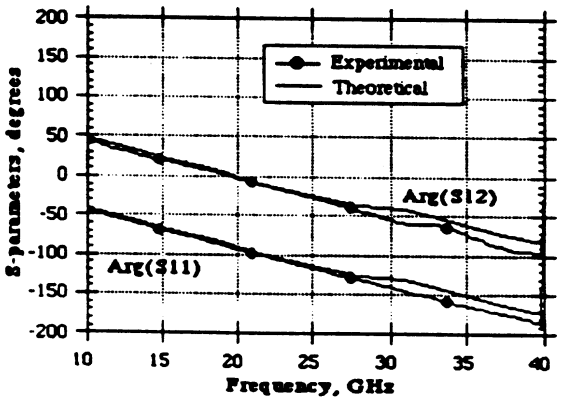
FIGURE A2. Micromachined CPW vs. CPW LIne: Open End Series Stub



(a) Circuit geometry

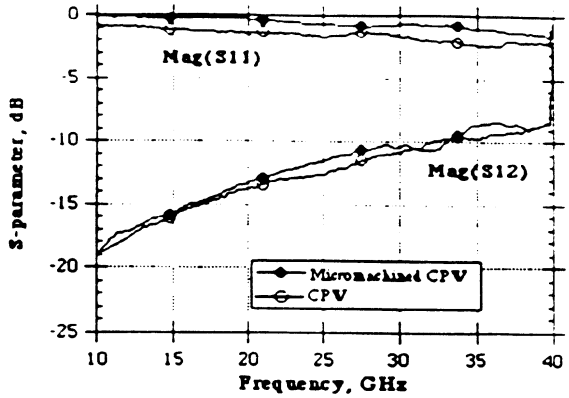


(b) Magnitude of scattering parameters

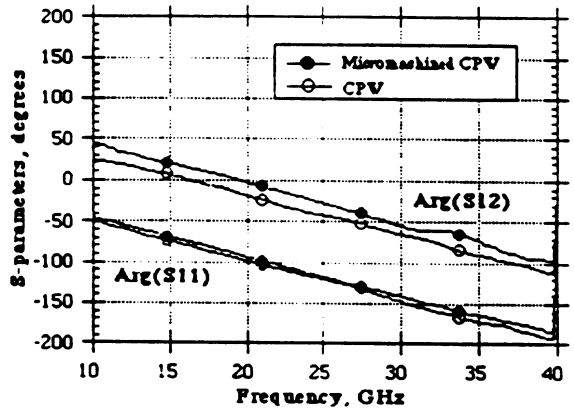


(c) Phase of scattering parameters

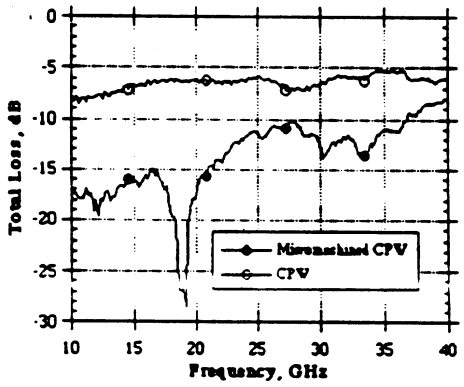
FIGURE B1. Micromachined CPW, Theoretical vs. Experimental: Open End Gap



(a) Magnitude of Scattering Parameters



(b) Phase of Scattering Parameters



(c) Total Loss

FIGURE B2. Micromachined CPW vs. CPW Line: Open End Gap

FABRICATION AND CHARACTERIZATION OF MICROSHIELD CIRCUITS

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Abstract

Microshield is a partially shielded, planar transmission line in which the center conductor and upper ground planes are surrounded by air and supported by a 1.5 μm thick dielectric membrane. This configuration allows single-mode, TEM wave propagation over a broad bandwidth with very low dispersion and zero dielectric loss. A lower shielding cavity is used to minimize radiation loss, vary the characteristic impedance, and prevent power loss into substrate modes. These properties highlight the potential of microshield as a high performance medium for submillimeter wave transmission. Here we present an overview of the fabrication of microshield lines, and report on the recent progress in the characterization of various circuit structures. Theoretical and experimental results are shown for lowpass filters, transitions to grounded coplanar waveguide, and different resonant stub designs. A description of an ultrafast electro-optic sampling experiment using membrane-based coplanar strip transmission lines is also included, and preliminary data is presented for line losses up to 500 GHz.

I Introduction

In 1988 a submillimeter wave integrated-horn antenna was developed which contained a dipole suspended on a 1.5 μm thick dielectric membrane inside a silicon cavity [1]. The success of this technique has led to the application of the membrane technology to a variety of antenna geometries, including wideband millimeter wave power meters and corner cube arrays at 1.2 THz [2, 3]. The potential for low-loss, non-dispersive electromagnetic wave transmission eventually led to the introduction of the microshield transmission line in 1991 [4].

Microshield is a partially shielded, planar transmission line in which the center conductor and upper ground planes are surrounded by air and supported by the dielectric membrane. This configuration, which is shown in Figure 1, allows single-mode, TEM wave propagation over a broad

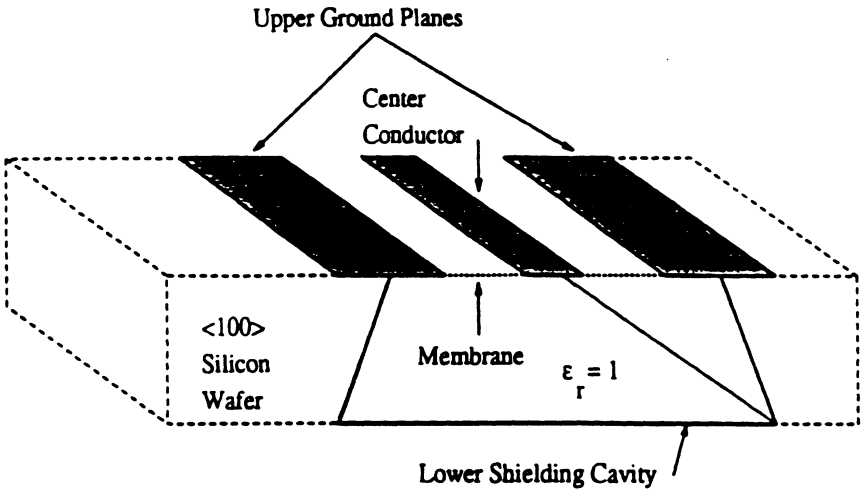

Figure 1: Illustration of the microshield transmission line geometry.

bandwidth with very low dispersion and zero dielectric loss. The lower shielding cavity is used to minimize radiation loss, vary the characteristic impedance, and prevent power loss into substrate modes. It also serves to equalize the upper ground planes, thereby eliminating the need for air-bridges or via-holes. Based on the potential high-performance from this geometry, the microshield line is currently being investigated as an alternative for submillimeter wave-guiding applications.

The characteristics of the microshield geometry were first examined in the theoretical study by Dib, et al [4, 5]. It was shown, for example, that discontinuities in microshield radiate less than comparable coplanar waveguide circuits, primarily due to the field confinement provided by the lower shielding cavity. Even on uniform transmission lines, frequency-dependent radiation into the substrate, which increases with the relative permittivity, can be significant at submillimeter wave frequencies. This loss mechanism is clearly minimized with microshield, since the conductors are completely surrounded by air. Finally, characteristic impedances ranging from around 30 Ω to over 280 Ω can easily be obtained by varying the center conductor width, upper ground plane spacing, and the height and width of the shielding cavity. Accurate, closed-form expressions for the characteristic impedance have been derived using a conformal mapping approach [5].

Here we present an overview of the fabrication of microshield lines and report on the recent progress in the characterization of various circuit structures. Theoretical and experimental results

from 20-40 GHz are shown for lowpass filters, transitions to grounded coplanar waveguide (gcpw), and two resonant stub designs. The insertion loss of a 5-section filter was measured at < .3 dB at 25 GHz, and the response compared nearly identically with ideal transmission line theory predictions. A low-loss transition to gcpw was also fabricated which had an S_{11} below -15 dB across the frequency range. The last section describes an ultra-fast optoelectronic sampling experiment using coplanar strip transmission lines printed on the dielectric membranes. Preliminary data on the loss characteristics up to 500 GHz demonstrates a definite advantage of membrane lines versus lines printed on high dielectric constant materials such as silicon or GaAs.

II Microshield Fabrication

The fabrication of microshield begins with a silicon wafer which has membrane layers on both sides. The membrane is a composite $SiO_2/Si_3N_4/SiO_2$ material which is grown using a combination thermal oxidation/chemical vapor deposition process. The wafers used here are 340 μm thick, high-resistivity silicon wafers with a < 100 > orientation. The microshield structure is formed by first removing photolithographically defined regions from the membrane layer on the back side of the wafer. This pattern serves as an etch mask, allowing pyramidal [1] cavities to be opened in the wafer using anisotropic Si etchants, such as ethylene diamine pyrocatechol (EDP) or potassium hydroxide (KOH). When the wafer has been etched through to the front side, the upper membrane layer will behave as an etch stop, thereby forming the exposed membrane surface with surrounding silicon walls below.

The final step in the fabrication process is the metallization of the circuit pattern and the lower cavity sidewalls. A tri-layer photoresist/aluminum/photoresist technique with metal evaporation is used to deposit the circuit pattern on the top side of the membrane layer. Evaporation is also used for metal deposition from the backside onto the cavity sidewalls, but here some shadowing is required to protect selected areas of the membrane from metallization. A diced or micro-machined silicon mask is used to shield the region between the inner-edges of the upper ground planes and

[1] The pyramidal shape of the cavity is due to the varying rate at which the etchant attacks different surface orientations inside the silicon.

the center conductor, thus preventing metallization of the membrane below the slots. The finished circuits are then mounted on a ground plane to fully enclose the lower shielding cavity.

III Theoretical Characterization

A rigorous full-wave analysis is being developed for use in the theoretical characterization of microshield circuits. The formulation involves a space-domain integral equation (SDIE) that is generated through the application of equivalent currents. This approach has previously been applied in a variety of electromagnetic problems, such as the characterization of coplanar waveguide [6], rectangular waveguide junctions [7], and scattering from microstrip patches [8]. This method is also well-suited to the study of microshield transmission lines, as it provides a relatively simple means of studying the different types circuit geometries which are possible. These geometries include step changes in the height and width of the shielding cavity and abrupt changes in the dielectric material, in addition to discontinuities in the metallization patterns of the signal line and upper ground planes.

The first step in the analysis is to simplify the circuit geometry by applying the equivalence principle. Here fictitious metal surfaces are introduced in the slots of the metallization which transform each region of a circuit into either a closed metallic cavity (inside) or a ground plane in free space (outside). Upon each side of these surfaces magnetic currents are imposed which act as equivalent sources. To determine the strength of these unknown currents the condition of continuous tangential electric and magnetic fields is enforced over each of the fictitious planes. Since $\vec{M} = \vec{E} \times \hat{n}$, where $\hat{n}$ is the outward unit normal in each region, continuity of $\vec{E}_{tan}$ is strictly satisfied by setting $\vec{M}_{lower} = -\vec{M}_{upper} = \vec{M}$. The continuity of $\vec{H}_{tan}$ is expressed in terms of the following integral equation:

$$\hat{n} \times \int_{S'} [\bar{\bar{G}}_{ext}(\vec{r},\vec{r}') + \bar{\bar{G}}_{int}(\vec{r},\vec{r}')] \cdot \vec{M}_s(\vec{r}')ds' = \vec{J}_s \qquad (1)$$

where $\bar{\bar{G}}_{ext,int}$ are the magnetic field dyadic Green's functions external and internal to the metallic cavities, respectively, and $\vec{J}_s$ is the current assumed with the ideal current source model, which

is used as the excitation. The solution to (1) is obtained by first dividing each surface into subsections, and then expanding the unknown magnetic currents using localized piecewise-sinusoidal basis functions. Equation (1) is then enforced in an average sense over each of the subsections, and is solved by using the method of moments (Galerkin's method) to generate a system of linear equations based on the mutual coupling, or admittance, between each of the currents. The solution of this system yields the complex coefficients of these basis functions, which is equivalent to finding the tangential electric field. This field is in the form of pure standing waves, such that standard transmission line theory may be then used to extract the scattering parameters of the circuit under analysis [6].

The formulation summarized above is used for the characterization of circuits which have discontinuities in just the upper metal layers. By extending this approach, it will be possible to analyze circuits such as T-junctions, shunt stubs with conformal cavities, and transitions between microshield and other planar lines such as coplanar waveguide. This extension primarily involves the use of equivalent current sheets in multiple planes, which serves to separate cavity discontinuities into homogeneous regions. The work in this area is currently in progress.

IV Theoretical and Experimental Results

In this section we present results on the performance of grounded coplanar waveguide (gcpw) to microshield transitions, stepped-impedance lowpass filters and different resonant stub designs. All measurements were made from 20-40 GHz, using an Alessi microwave probe station connected to an HP 8510B network analyzer. The system was calibrated using the TRL (thru-reflect-line) technique. For the theoretical data, ideal transmission line theory was used to characterize the lowpass filters and proved to be very accurate. The resonant stub designs were characterized using the full-wave analysis, and this section includes a study of the effect of shield-geometry variation on the stub performance. The formulation for characterization of the gcpw-microshield transitions is currently being developed, and thus only experimental data is presented.

IV.1 (Grounded) CPW to Microshield Transitions

The primary motivation for investigating the gcpw-to-microshield transition lies in optimizing the design for circuit measurements. As mentioned, these measurements are made using a microwave probe station. Since the membranes cannot reliably withstand the force of repeated probe contact, the contact pads for must be formed in gcpw, which necessitates the use of transitions from the gcpw to the microshield line under test. In order to calibrate the system, these transitions need to be designed for low reflection.

There were four microshield-gcpw-microshield transitions which were measured. The structures consist of a section of grounded cpw of length $\frac{\lambda_{g,cpw}}{2}$ at 40 GHz, which is positioned in the center of a microshield line. The design is illustrated in Figure 2. In all cases the microshield geometry has a center conductor width, s, of 350 μm and a slot width, w, of 35 μm. The characteristic impedance for this line is 75 Ω. For the four different designs, $s + 2w$ in the gcpw was also held constant at 420 μm, and center conductor widths of 35, 70, 140, and 280 μm were tested. These geometries result in characteristic impedances of 88, 71, 54, and 36 Ω, respectively.

The measured S_{11} for the transitions is given in Figure 3. The best performance, less than -15 dB from 20 to 40 GHz, is obtained with the 70 μm transition, which is the design with the closest impedance match. This transition also had a measured loss, $(1 - |S_{11}|^2 - |S_{21}|^2)$, below -15 dB across the entire band.

IV.2 Stepped-Impedance Lowpass Filters

Stepped-impedance lowpass filters were investigated since they are relatively easy to design and could demonstrate the low loss, TEM characteristics of microshield. In order to obtain the impedance ratios required to implement the chosen designs, a center conductor width ratio of 33 : 1 was necessary. The conductor widths and the impedances are shown in the schematic diagram of the 5-section filter given in Figure 4.

The measured performance for 5- and 7-section 0.5 dB ripple Chebyshev designs is shown in Figure 5. Also shown is the theoretical response obtained using ideal transmission line theory,

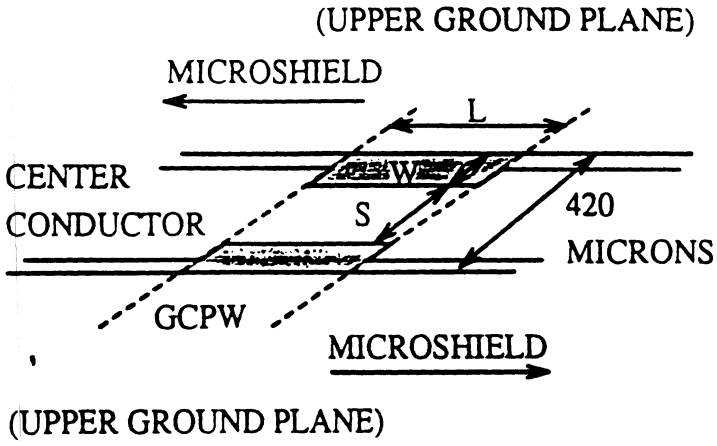

Figure 2: Illustration of the microshield to grounded cpw (coplanar waveguide) transition. The center conductor width, S, the slot width, W, and the length of the gcpw, L, are all indicated. L is $\frac{\lambda_g}{2}$ at 40 GHz. The slots in the gcpw are shaded to indicate that the substrate dielectric changes from air in the microshield to silicon in the gcpw section.

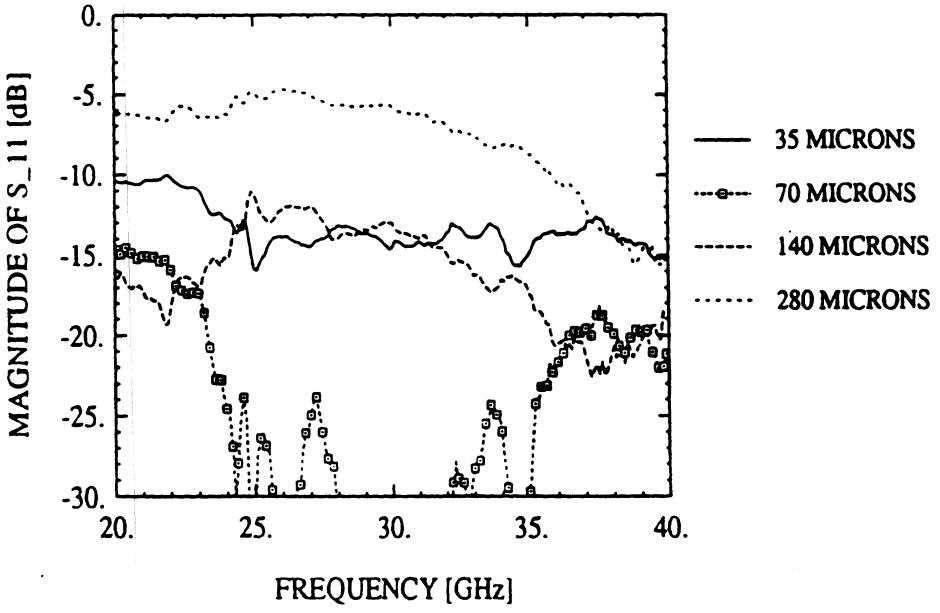

Figure 3: Measured S_{11} response of four different microshield to grounded cpw transitions. The microshield center conductor width is 350 microns. Each plot corresponds to a different center conductor width for the gcpw. In all cases, 2s+w is 420 microns for both microshield and gcpw lines.

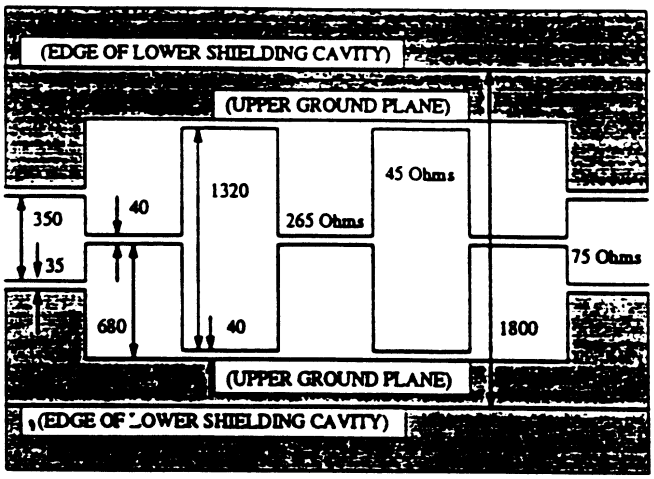

Figure 4: Diagram of the 5-section stepped-impedance lowpass filter (not to scale). Dimensions are given in μm and the different impedance sections are indicated. The shaded regions are the upper ground planes, which have been marked to indicate the positions of the lower shielding cavity sidewalls. The distance between the cavity sidewalls is 1800 μm.

with empirically-derived corrections for the effective line extension at impedance steps [9]. The agreement is quite good, and the differences near cutoff (shown in the insets) result from a peak in the measured loss which is not accounted for by the theory.

IV.3 Resonant Stubs

In this section the performance of a microshield shorted resonant stub is presented. The design which was implemented consists of a stub which is formed in the center conductor, and is of length $\frac{\lambda_g}{4}$ at the resonant frequency. This will be referred to as the in-line series shorted stub (ILS). A comparison of the measured and calculated results is first shown, followed by an illustration of the effects of varying the shielding cavity dimensions. In addition, the characteristics of the ILS stub are compared to those of a stub which is formed in the upper ground planes, which is referred to as the ground plane series stub (GPS). It is noted here that the measured ILS circuit had cavity dimensions of height, h_c = 340 μm, and width, w_c = 1800 μm, as measured at the top of the cavity.

The measured and predicted performance of the ILS stub is shown in Figure 6, where Ckt. A refers to the theoretical data. A schematic of the upper metallization pattern is also shown in the figure. The deep resonance at 28 GHz is shifted down in frequency relative to the ideal

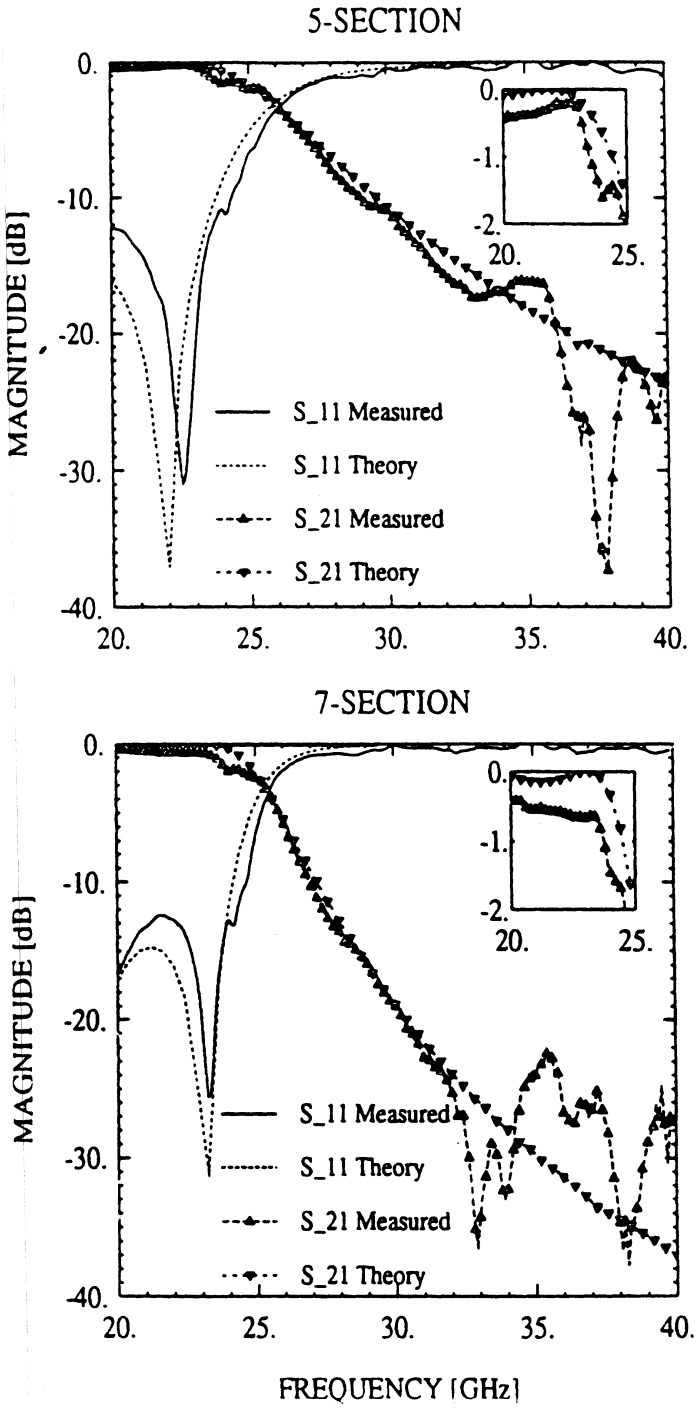

Figure 5: Measured and theoretical response of a 5- and a 7-section stepped-impedance microshield filter.

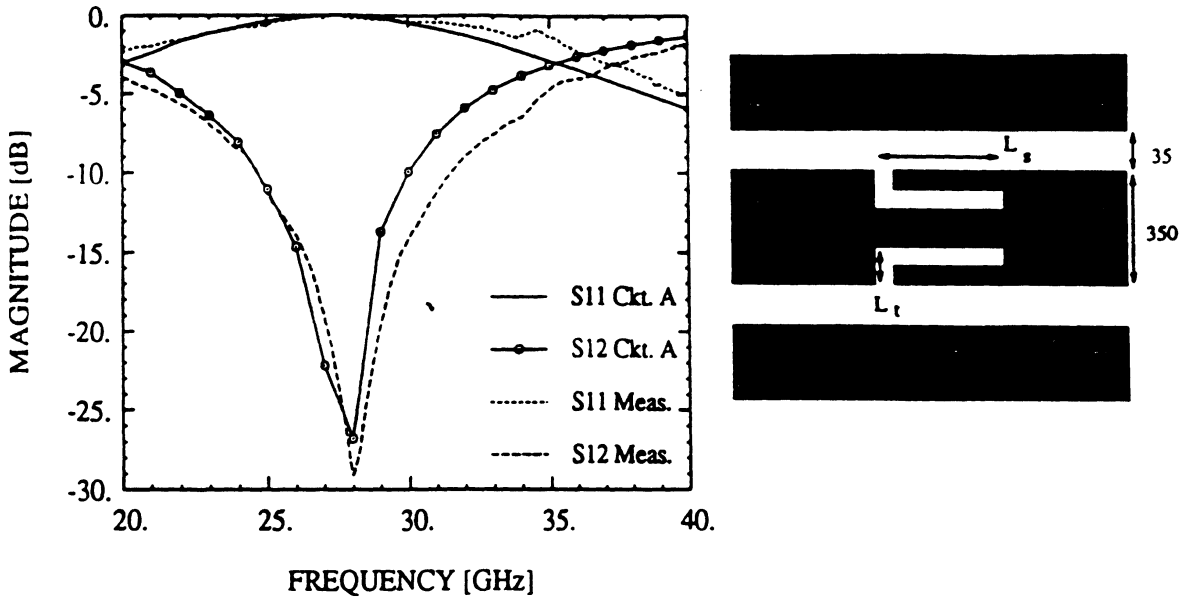

Figure 6: Measured and calculated response of the in-line series shorted stub, where Ckt. A refers to the calculated data. In the diagram on the right (not to scale), L_s = 2500 and L_t = 120. All dimensions are in μm.

response, since the physical stub length is $\frac{\lambda_g}{4}$ at $\approx$ 29.3 GHz, when account is taken of the short transverse slot lengths, L_t. In Figure 7, the effects of a reduced cavity size and upper shielding are demonstrated. The Ckt. B results represent the predicted performance with a lower cavity of dimensions h_c = 100 μm and w_c = 420 μm, which is the practical minimum cavity size for this circuit. Clearly, the cavity has only second order effects, which can be explained by the small slot width of only 35 μm. The Ckt. C results represent the predicted performance for the geometry of Ckt. A when shielded symmetrically above and below. In this case near-ideal stub performance is obtained, as the resonance has shifted to $\approx$ 29.5 GHz.

As mentioned, a comparison has been made between the in-line series shorted stub and an alternative design called the ground plane series stub. The theoretical performance of each stub, using the symmetric shielding configuration, is shown in Figure 8. The upper metallization pattern for the GPS is also given in this figure, where the total stub length is 2370 μm, corresponding to a resonant frequency of around 32 GHz. The GPS has a much narrower 3-dB bandwidth, roughly 14% versus 52% for the ILS, but will radiate much more strongly in an open environment.

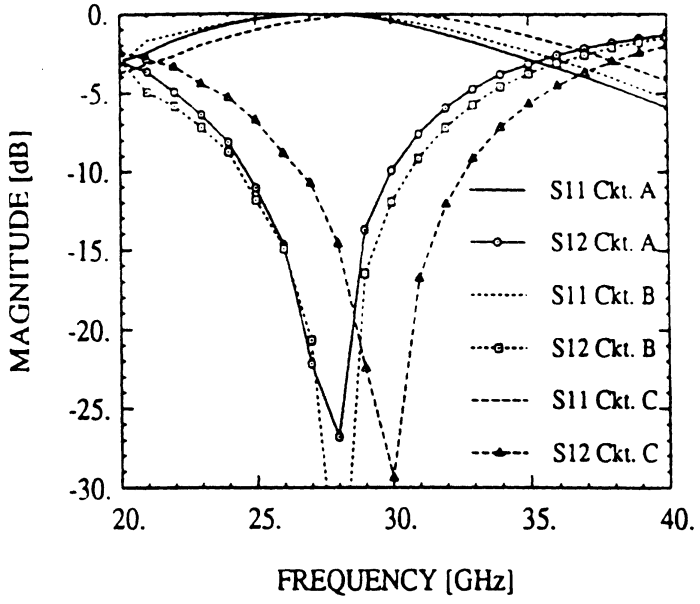

Figure 7: Theoretical response of different in-line series shorted stub geometries. Ckt. A has lower shielding cavity dimensions of 1800 × 340 μm (width by height), the Ckt. B cavity is 420 × 100 μm, and Ckt. C has the same cavity dimensions as A but is symmetrically shielded on the top and bottom.

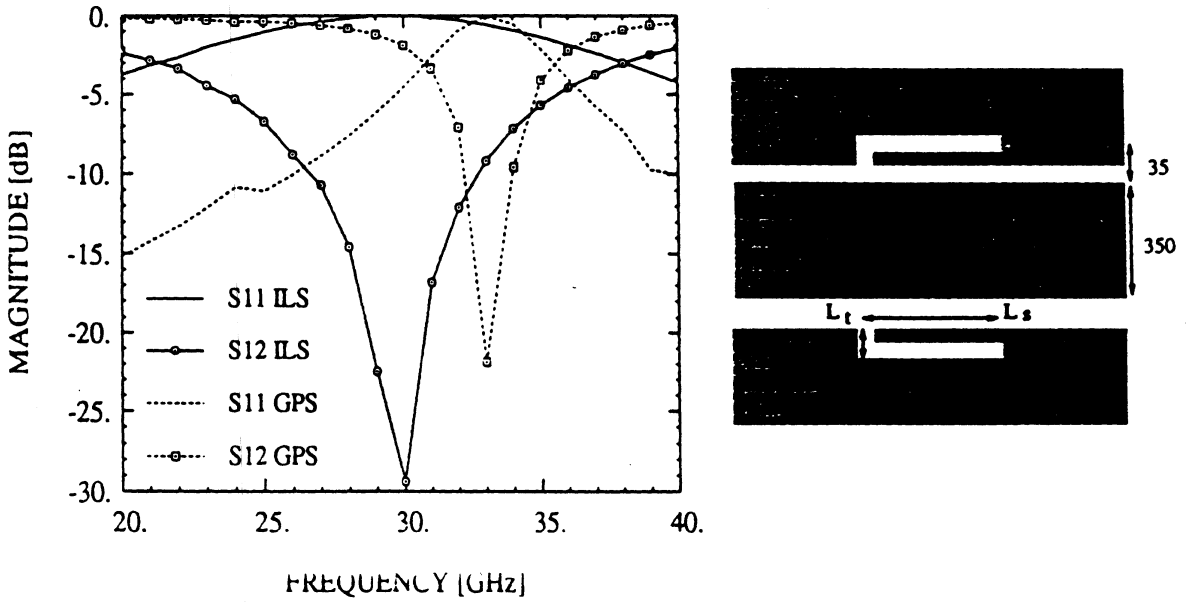

Figure 8: Theoretical response of the in-line series stub (ILS) versus the ground plane series stub configuration (GPS). The circuits are symmetrically shielded and have the same cavity dimensions as Ckt. A in Figure 7. In the diagram on the right (not to scale). L_t = 420 μm and L_s = 1950 μm.

V Electro-optic Sampling Experiment

Another interesting structure that has been fabricated on the micron-thick membranes is a simple coplanar strip transmission line (CPS). This structure, devised in order to push the limits of high-frequency, guided-wave transmission, should be capable of supporting millimeter- and submillimeter-wave electronic signals with very little induced distortion. This is due to the fact that the degree of phase velocity dispersion experienced in hybrid-mode propagation on planar transmission lines, as well as the amount of frequency-dependent radiation of energy into the substrate of such structures, increases with the permittivity of the substrate. Therefore, the electric field of a signal travelling on a uniform CPS on a membrane substrate experiences essentially a homogeneous dielectric above and below the plane of the membrane, i.e. air. This leads to propagation that has no radiation loss, no substrate dielectric loss, and no dispersion due to a frequency-dependent effective permittivity. In this preliminary investigation, we have demonstrated that pulses having subpicosecond rise times and single-picosecond durations propagate for lengths as great as 5 mm without loss of fidelity. The usable frequency content of these pulses extends from dc to nearly 1 THz, and by taking Fourier transforms, we have computed the attenuation and phase velocity of the time-domain signals on the line. Between 50 and 500 GHz, it has been observed that dispersion is negligible and attenuation is very small, arising presumably only from ohmic losses in the metal conductors. In order to generate and measure electrical pulses of such short duration and high frequency content, the optoelectronic technique of photoconductive switching, along with an ultra-high-speed electro-optic sampling characterization system, have been employed. These techniques are both based on the use of laser pulses of extremely short duration ($\leq$ 100 fs). The photoconductive source requires the ultra-short laser pulse to convert a dc bias to a subpicosecond electrical transient, while electro-optic sampling uses the optical pulse with an electro-optic crystal to produce a sampling gate having a duration of only several tenths of a picosecond. A probe tip fashioned from the electro-optic crystal is dipped into the electric field above the transmission line under test, and without any electrical contact the propagating waveform is measured. For the measurement of transients in the time domain, reflections from any source near the probing

point cause a loss of accuracy in the acquisition of clean, easily analyzed signals. Therefore, it was necessary to integrate a 200-μm-wide photoconductive-generator patch with the CPS fabricated on the membrane. This was a convenient alternative compared with transporting a short electrical transient onto the CPS via inductive wirebonds or through the use of an unwieldy flip-chip geometry. The photoconductor of choice, having subpicosecond carrier lifetime, high dark resistivity, high responsivity, and high dielectric breakdown, was a 1-μm layer of GaAs grown by molecular beam epitaxy at the low substrate temperature of $\sim$ 200 deg C (LT-GaAs). This photoconductor was lifted off its substrate to form a free-standing film through etching techniques, and then grafted to the membrane substrate using a van der Waals bonding technique. The CPS was then defined on the LT-GaAs and the membrane using standard photolithographic techniques. The pulse output after optical excitation of the photoswitch was measured at distances of 1, 3, and 5 mm from the generator, with no discernable distortion except for a small decrease in peak amplitude at the 5 mm propagation distance. The measured pulse rise time was $\leq$ 0.75 ps, and the FWHM (full width at half maximum) was $\leq$ 1.2 ps. When the Fourier transforms of the time-domain signals were compared, the phase velocity between 50 and 500 GHz was found to be flat, indicating the absence of dispersion. The attenuation, shown in Figure 9, was found to increase only slightly, to about 0.8 dB/mm at 500 GHz. This result can be directly compared to the propagation of a subpicosecond pulse along a CPS of the same dimensions on a GaAs substrate. While the attenuation at 50 GHz is only about 0.7 dB/mm for this structure, at 500 GHz it is in excess of 9.5 dB/mm. This is mainly due to the extreme radiation loss present even in uniform lines that are fabricated on high-permittivity substrates. A much larger degree of phase-velocity dispersion also results from propagation on the GaAs-substrate line, leading to pulses with rise times and durations that rapidly expand with increasing propagation distance.

VI Conclusion

This paper has presented a review of the recent progress made in the experimental and theoretical characterization of microshield transmission line circuits. Low loss transitions from microshield to grounded coplanar waveguide have been successfully designed and measured, and

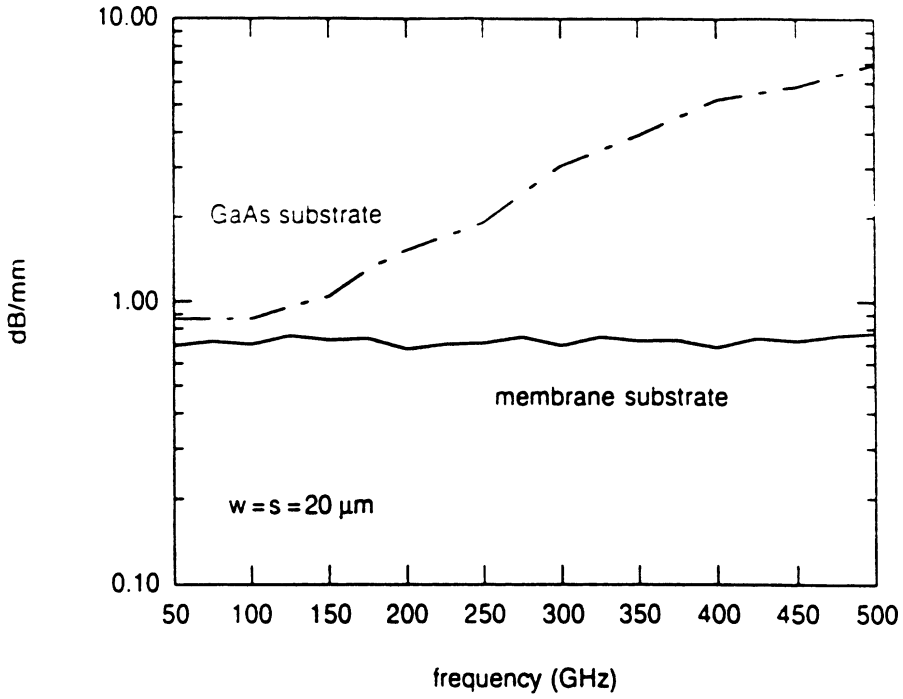

Figure 9: Measured attenuation of a coplanar stripline (CPS) printed on a GaAs substrate compared to a line printed on a dielectric membrane. The measurements were made using an electro-optic sampling technique. The conductor and slot widths of the CPS are both 20 μm.

stepped-impedance lowpass filters demonstrated very good performance and compared quite well to ideal transmission line theory. A brief study of different microshield resonant stub designs has also been presented. Finally, a preliminary study using an ultra-fast electro-optic sampling technique has shown that coplanar strip lines, printed on the dielectric membranes, show strong potential as a low loss transmission medium for THz-frequency applications.

VII Acknowledgements

This work has been supported by the Office of Naval Research under contract No. N00014-92-J-1070, the NASA Center for Space Terahertz Technology, and the NSF under the Center for Ultrafast Optical Science. The authors would like to thank Prof. G. Rebeiz's group for their assistance, and particularly Mr. Walid Ali-Ahmad.

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STUDY OF MICROMACHINED QUASI-PLANAR LINES

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Recent industrial trends in space and communication technology show the development of systems that have high rate information transfer as well as improved fuel economy. High rate transfer results from the improved electrical performance of circuit components while better fuel economy results from the development of smaller lightweight systems. Currently, planarized transmission lines such as microstrip, stripline, and coplanar waveguide provide enhanced flexibility in antenna and array design, compatibility with active devices and radiating elements, and reduction in size and weight. However, such lines produce unwanted frequency dependent mechanisms such as parasitic radiation and coupling which interfere with wave propagation. Consequently, a need exists for the development of transmission lines without the above limitations which exhibit improved electrical performance while offering additional reduction in the size and weight of circuits.

With recent advances in semiconductor processes, namely micromachining, Si or GaAs semiconductor substrate materials may be utilized to create planar transmission lines and their shielding cavities in monolithic form. Serving a dual purpose, the cavity can reduce electromagnetic interference and parasitic radiation while introducing additional design parameters. Geometrically, the planar transmission lines are created by metal deposition on a Si substrate whereas the shielding is created by etching a cavity into Si using KOH. After metallizing both surfaces using evaporation techniques, the two wafers are attached by electrobonding. The result is the development of lines that offer improved electrical performance and the potential to incorporate an integrated package.

In this paper a novel transmission line, which exhibits the advantages discussed above, is presented . A discussion of the fabrication procedure required to develop this line as well as the measurement technique used for characterization are presented. In addition, various line properties such as propagation constant and characteristic impedance are shown and compared to conventional lines, such as microstrip and coplanar waveguide.

Quasi-Planar Transmission Line

EXPERIMENTAL RESULTS ON MICROSHIELD TRANSMISSION LINE CIRCUITS

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Abstract — **Presented here are the first experimental data on microshield circuits which use the membrane technology. Microshield shows potential for improved performance relative to current planar transmission line geometries. This paper will describe results on stepped-impedance filters and coplanar waveguide-to-microshield transitions.**

I. INTRODUCTION

This paper presents for the first time an extensive experimental study of microshield transmission line circuits which are fabricated using membrane technology [1]. The microshield line was introduced in 1991 and has been shown, using proven theoretical techniques, to exhibit desirable waveguiding properties [2]. These properties include pure TEM propagation and zero dispersion in a wide, single mode frequency band, low radiation loss, zero dielectric loss, and a broad range of possible line impedance. The lower shielding cavity, furthermore, provides ground plane equalization and thus eliminates the need for air bridges or via holes.

Several types of microshield circuits have now been fabricated and measured, including filters, stubs, and transitions from grounded coplanar waveguide (gcpw) to microshield. The transitions are of immediate interest because the preferred measurement technique requires initial contact to gcpw, as discussed below. Additionally, transmission lines with drastic step changes in the dielectric material may provide novel capabilities and are worthy of investigation. Stepped-impedance filters are examined since they are simple to design and are shown to effectively demonstrate microshield performance. The fabrication and characterization of the transitions and filters are reviewed here.

II. FABRICATION AND DESIGN

The foremost characteristic of microshield circuit fabrication is the utilization of the membrane technology described by Rebeiz, et al [1]. For the work described here, 340 μm thick < 100 > silicon wafers, with 1.5 μm $SiO_2/Si_3N_4/SiO_2$ membrane layers, have been used. The microshield structure is created by first removing photolithographically defined regions from the membrane layer on the back side of the wafer. This pattern serves as an etch mask, allowing pyramidal cavities to be opened in the wafer using anisotropic Si etchants, such as ethylene diamine Pyrocatechol (EDP). The upper membrane layer will behave as an etch stop, thereby forming the exposed membrane surface with a surrounding cavity below [3].

The final steps in the fabrication process are the metallization of the circuit pattern and the cavity sidewalls. A tri-layer photoresist/aluminum/photoresist technique with metal evaporation is used to deposit the circuit pattern on the top side of the membrane layer. Evaporation is also used for metal deposition on the cavity sidewalls, but here some shadowing is required to protect selected areas of the membrane from backside metallization. A diced or micromachined silicon mask is used to shield the region between the inner-edges of the upper ground planes, thus preventing metallization in the slots. The finished circuits are then mounted on a ground plane to fully enclose the lower shielding cavity. A photograph of a 5- and a 7-section lowpass filter is shown in Figure 1.

An important design objective in this project is to develop a low loss transition from grounded coplanar waveguide to microshield. This is necessary because the measurement device is a microwave probe station, and the probe contacts must be formed in gcpw since the membranes cannot reliably withstand multiple probing attempts While the design of a transition should include consideration of the characteristic impedance, it must also be considered that each of these lines is a mixed coplanar-microstrip guiding structure, for which the relative slot widths, center conductor width, and ground plane separation all determine the mode of propagation. Guidelines for the design of gcpw can be found in [4, 5], while those for the microshield line are found in [3]. Although one transition design was chosen a priori for measurement purposes, three other variations were tested and their performance is reviewed in the following section.

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III. EXPERIMENTAL RESULTS

A. (Grounded) CPW to Microshield Transitions

The primary motivation for investigating the gcpw-to-microshield transitions lies in optimizing the design for measurement purposes, as discussed above. One can envision, however, alternative reasons for utilizing short segments of cpw along a microshield line (or vice versa): a simple means of fixed phase delay or advance, as the phase velocity will be lower in cpw than in microshield; mechanical support to facilitate mounting hybrid active devices along a microshield line; and obtaining very large impedance ratios for filter purposes are all possibilities. To our knowledge, such planar transmission line circuits with similar metallization, yet drastic dielectric changes, have not previously been explored.

There were four microshield-gcpw-microshield transitions which were measured. The structures consist of a section of grounded cpw of length $\frac{\lambda_{g,cpw}}{2}$ at 40 GHz, which is positioned in the center of a microshield line. The design is illustrated in Figure 2. In all cases the microshield geometry has a center conductor width, s, of 350 μm and a slot width, w, of 35 μm. The characteristic impedance for this line is 75 Ω. For the four different designs, $s + 2w$ in the gcpw was also held constant at 420 μm, and center conductor widths of 35, 70, 140, and 280 μm were tested. These geometries result in characteristic impedances of 88, 71, 54, and 36 Ω, respectively.

The measured S_{11} for the transitions is given in Figure 3. The best performance, less than -15 dB from 20 to 40 GHz, is obtained with the 70 μm transition, which is also the design with the closest impedance match. This transition also operates with very low radiation loss, as shown in Figure 4. It should be noted, however, that the S_{11} response is very dissimilar to that expected from ideal transmission line theory, which would predict a gradual rolloff to a perfect match at 40 GHz. These discrepancies may be partially explained by the field-configuration considerations mentioned above, as the microshield line is operating in a strongly cpw-like mode, whereas the grounded cpw line will exhibit more of a hybrid cpw/microstrip characteristic due to the smaller height-to-slot width ratio.

B. Stepped-Impedance Low Pass Filters

Stepped-impedance filters are commonly used for applications which do not require a sharp cutoff, such as in the rejection of out of band mixer harmonics. They are a desirable test circuit for the new microshield technology primarily because they are quite easy to design and their performance may be used to qualify impedance calculations, the degree of TEM mode propagation, and the level of conductor and radiation loss.

A schematic diagram of the 5-section filter desi given in Figure 5. The measured performance for 5- a section 0.5 dB ripple Chebyshev designs is shown in F 6. Also shown is the theoretical filter response obtain ing ideal transmission line theory, with empirically-de corrections for the effective line extension at impe steps [6]. The agreement is quite good, and the differ near cutoff can be explained by the peak in the radi loss, shown in Figure 7. Also, no correction for cond loss is included in the theoretical data.

IV. CONCLUSION

Experimental results on microshield stepped-impedanc ters and transitions to grounded coplanar waveguide been presented. The filter response compared very to ideal transmission line theory when effective line le corrections for impedance steps were employed. The transition performance demonstrates an S_{11} below -1 from 20 to 40 GHz.

V. ACKNOWLEDGEMENT

This work has been supported by the Office of Naval search under contract No. N00014-92-J-1070 and the N/ Center for Space Terahertz Technology. The authors w like to thank Prof. G. Rebeiz's group for their assista and particularly Mr. Walid Ali-Ahmad.

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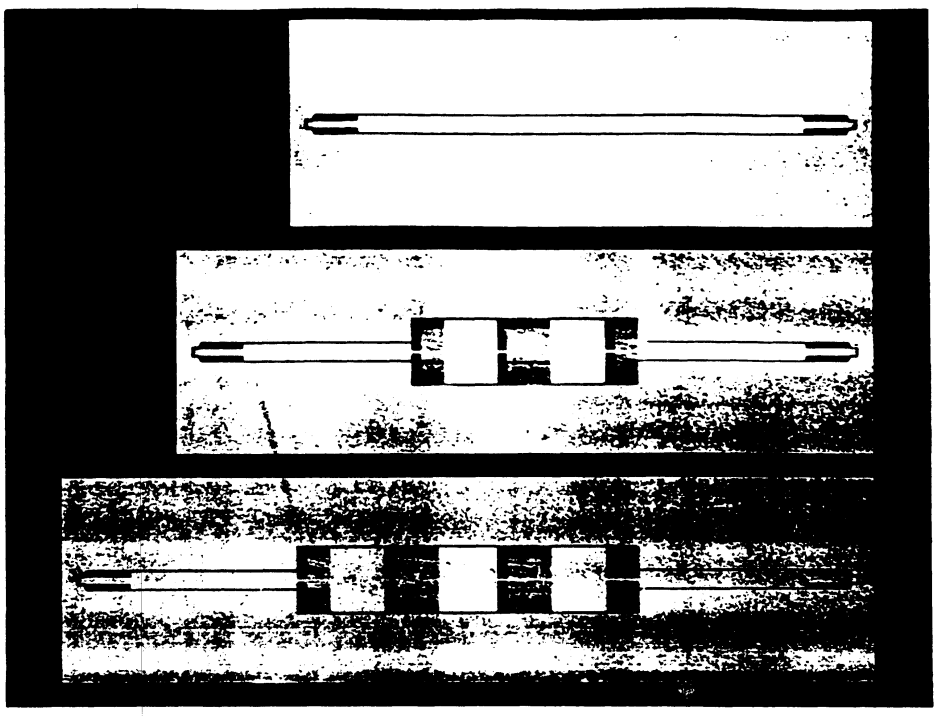

Figure 1: Photograph of a 5- and a 7-section microshield stepped-impedance low pass filter. The upper metallization is 340 μm from the lower ground plane, producing the shadows which are seen around the center conductor and upper ground plane edges. The thin center conductor sections are 40 μm wide and the width of all ground planes is 0.42 cm. The grounded coplanar waveguide-to-microshield transitions occur where the line narrows on either end of the circuits.

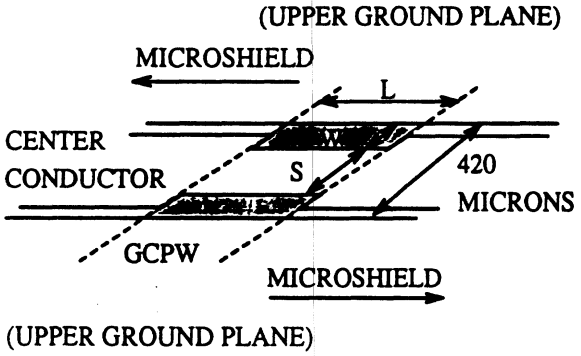

Figure 2: Illustration of the microshield to grounded cpw (coplanar waveguide) transition. The center conductor width, S, the slot width, W, and the length of the gcpw, L, are all indicated. L is $\frac{\lambda_g}{2}$ at 40 GHz. The slots in the gcpw are shaded to indicate that the substrate dielectric changes from air in the microshield to silicon in the gcpw section.

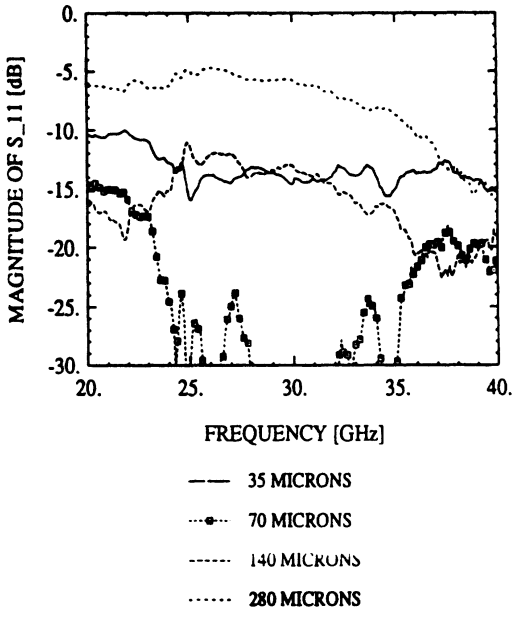

Figure 3: Measured S_{11} response of four different microshield to grounded cpw transitions. The microshield center conductor width is 350 microns. Each plot corresponds to a different center conductor width for the gcpw. In all cases, 2s+w is 420 microns for both microshield and gcpw lines.

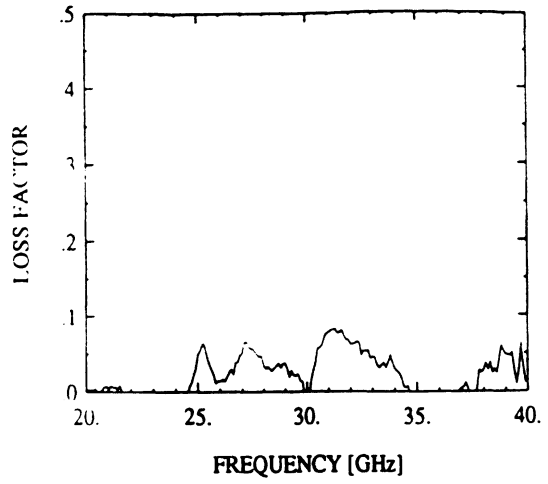

Figure 4: Measured loss factor, $(1- \mid S_{11} \mid^2 - \mid S_{21} \mid^2)$, for the 70 micron microshield to grounded cpw transition.

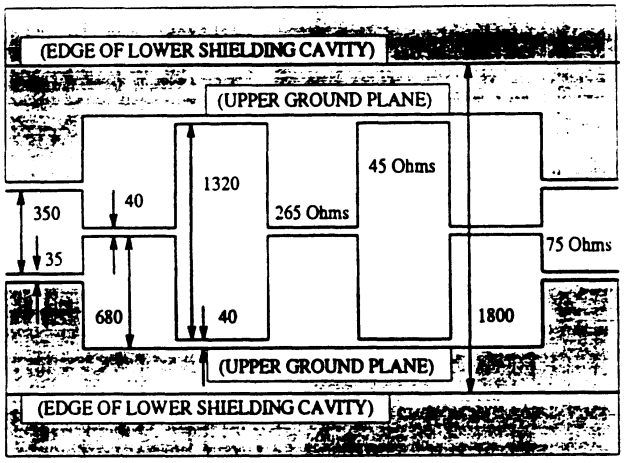

Figure 5: Diagram of the 5-section stepped-impedance low-pass filter (not to scale). Dimensions are given in μm and the different impedance sections are also indicated. The shaded regions are the upper ground planes, which have been marked to indicate the positions of the lower shielding cavity sidewalls.

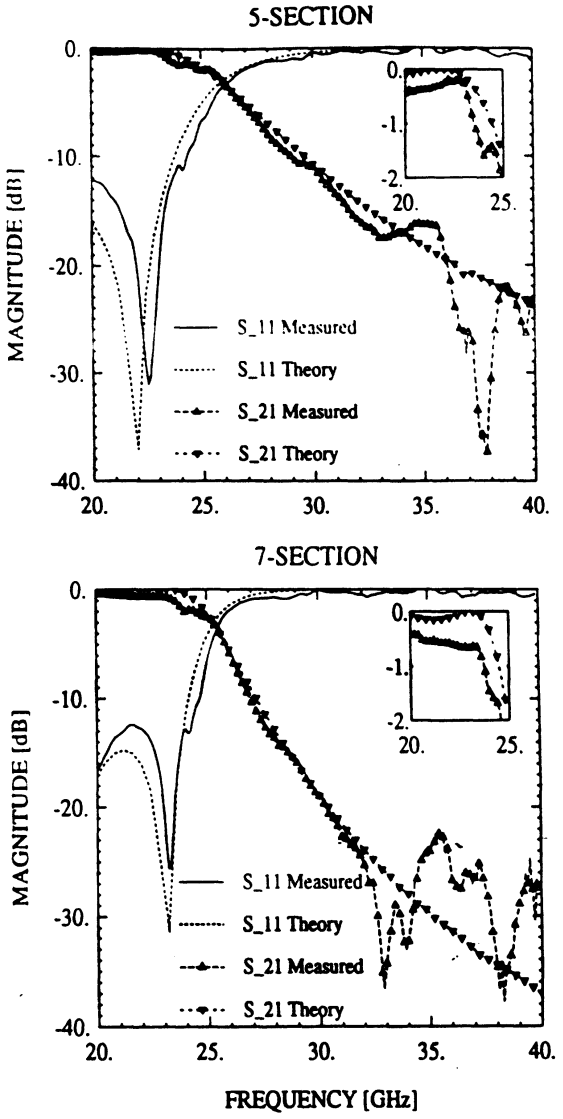

Figure 6: Measured and theoretical response of a 5- and a 7-section stepped-impedance microshield filter.

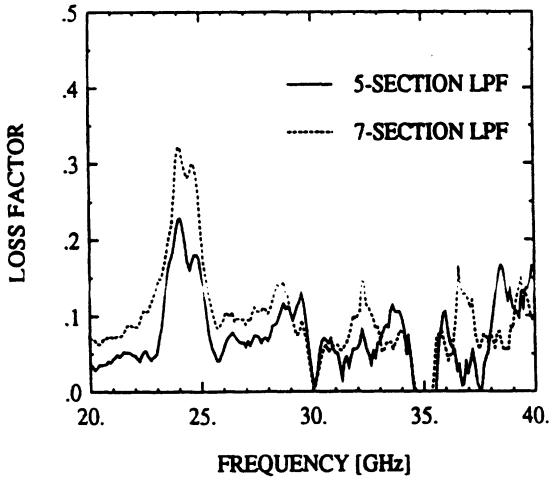

Figure 7: Measured loss factor, $(1- \mid S_{11} \mid^2 - \mid S_{21} \mid^2)$, fo the 5- and 7-section low pass filters.

Millimeter and Submillimeter Wave Microshield Line Components

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Abstract

Recent efforts at the University of Michigan have resulted in the successful development of high-performance planar components which operate in Ka- and W-Bands. These circuits are fabricated using silicon micromachining techniques, and they are placed on a thin dielectric membrane which is shielded by a metallized cavity on one side (see Fig. 1). This type of line, called microshield line, has exhibited very low radiation and ohmic losses for frequencies as high as 1 THz.

A variety of microshield components have been fabricated and their performance has been measured at the facilities of the Radiation Laboratory at the University of Michigan and NASA Lewis Research Center. These circuit components exhibit superior performance compared to planar components made with conventional microstrip or coplanar technology. In this paper, basic transmission line properties such as dispersion and attenuation are first examined. This is followed by a sample of the measured results obtained at Ka-Band for right angle bends, low-pass filters, and band-pass filters. Furthermore, extension of this technology to higher frequencies is explored.

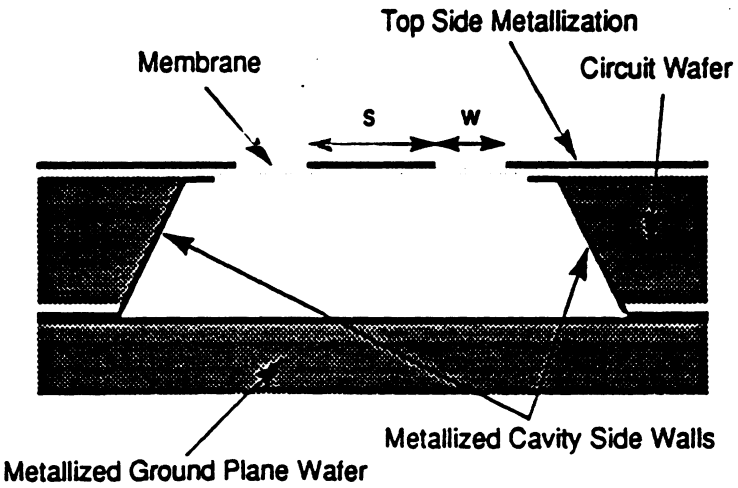

Figure 1. Microshield line uses micromachining techniques to suspend components in air on a thin dielectric membrane.

1. Introduction

The need for high performance microwave circuit components which could operate in the THz freqeuncy range led to the development of the microshield line in 1991 [1]. Microshield line uses silicon micromachining and membrane technology to locally remove the substrate underneath a conventional CPW type transmission line. The resulting configuration propagates a pure TEM wave in a homogeneous air dielectric with very low loss and virtually no dispersion over an extremely wide bandwidth [2].

In this work we present results showing the high performance characteristics of microshield line. Measurements of loss and effective dielectric constant show the low loss and low dispersion as expected. Microshield line components are compared to conventional planar components. In particular, right angle bends show better return loss performance when fabricated with microshield line instead of CPW. Also, planar filters for high frequency applications which normally suffer due to the presence of a dielectric substrate are shown to operate effectively when implemented using microshield line.

2. Fabrication

Microshield circuits are fabricated on high-resistivity (> 2,000 Ω-cm) silicon wafers with a 1.5 μm-thick $SiO_2/Si_3N_4/SiO_2$ composite deposited on both sides [3]. After the circuit metallization is patterned on the top side of the wafer using evaporation and lift-off, infrared alignment is used to pattern the backside membrane. The membrane layers are then etched to expose the silicon, at which point ethylenediamene pyro-catechol (EDP) anisotropic silicon etchant is used to define cavities underneath the circuit metallization. Once the silicon has been etched away, the top side membrane remains in tension to support the circuits. Next, the cavity side walls are metallized using a shadow mask evaporation which prevents an RF short from occurring between the signal line and the upper ground planes. Finally, the wafers are placed on a metallized ground plane wafer to completely shield the cavity (2-D geometry shown in Fig. 1).

3. Microshield Line Characteristics

A. Effective Dielectric Constant

Due to the air substrate of the microshield line, the effective dielectric constant, $\varepsilon_{r,eff}$, is very close to 1. The presence of the membrane, however, causes a slight increase in $\varepsilon_{r,eff}$ since a fraction of the fields will be contained within the thin dielectric layers which have

relative dielectric constants of 3.9 (SiO_2) and 7.5 (Si_3N_4). As shown in Figure 2, the measured $\varepsilon_{r,eff}$ changes from around 1.09 to 1.15 as the slot width is reduced from 55 to 25 μm. This increase is a result of greater field confinement in the slot and thus in the membrane, and represents a decrease of nearly 3% in the guided wavelength. This dependence on the slot width is similar to the characteristics of CPW lines on a substrate such as GaAs or quartz [4]. As the line geometry approaches single micrometer dimensions which are comparable to the membrane thickness, $\varepsilon_{r,eff}$ could increase to around 2.0.

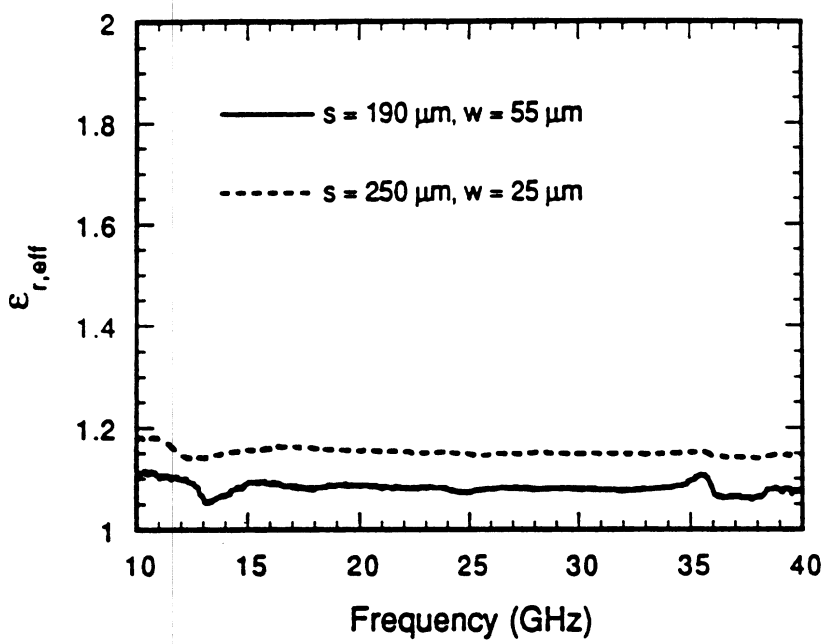

Figure 2. Effective dielectric constant at Ka-Band for two geometries of microshield line.

B. Attenuation

The attenuation characteristics of the microshield line have been investigated by comparing measured data on different microshield geometries against experimental and theoretical results for coplanar waveguide which are found in the literature. At low frequencies, the two types of lines are expected to perform equally well, since dielectric and radiative losses are relatively small and attenuation is dominated by conductor loss, which should be about the same in microshield and CPW due to the similar geometry of the metallization. At higher frequencies, however, the microshield line gains an increasing advantage since it has essentially zero dielectric loss and does not radiate energy into the substrate, as with a substrate-supported CPW line. This characteristic has been verified by recent electro-optic sampling experiments, which have provided attenuation data on membrane lines up to 1000 GHz [2].

The comparison between the microshield and CPW attenuation is shown in Figure 3. The curves shown for comparison were chosen either because the CPW dimensions are similar to the microshield dimensions (curves C,F,G) or to illustrate the effects of reducing the line geometry (curves D,E). All pertinent geometrical parameters for the CPW and microshield examples are given in Table 1 beneath the figure, and it is noted that the conductor thickness is only about 2 skin depths at 25 GHz for all but two cases (note: the technique used in [5] assumes zero conductor thickness).

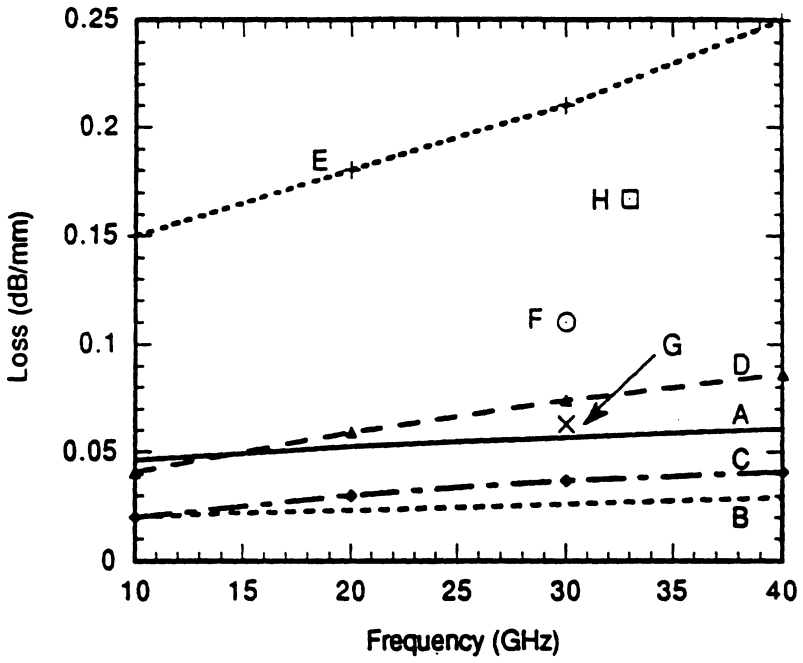

Figure 3. Comparison of microshield and CPW attenuation.

Table 1. Attenuation for microshield and coplanar waveguide lines. S is the center conductor width, W the slot width, H the substrate height, and t the metal thickness (in μm). The width of the lower shielding cavity for the microshield lines is 1800 μm.

Curve	Line	ε_r	Substr.	S	W	H	t	Z_0 (Ω)	Data	Ref
A	μshield	1.0	Air	250	25	355	1.2	75	Meas	—
B	μshield	1.0	Air	190	55	355	1.2	100	Meas	—
C	CPW	12.8	GaAs	232	84	100	—	50	Calc	[5]
D	CPW	12.8	GaAs	69	28	100	—	50	Calc	[5]
E	CPW	12.9	GaAs	88	16	500	1.0	30	Meas	[6]
F	CPW	12.9	GaAs	250	25	500	1.0	30	Calc	[4]
G	CPW	4.0	Quartz	250	25	250	1.0	50	Calc	[4]
H	GCPW	11.7	Si	50	125	355	1.2	73	Meas	—

The results presented here confirm that the microshield line is free from unexpected or excessive conductor-loss mechanisms, and has performance which is comparable to conventional substrate-supported coplanar waveguide at lower frequencies. Furthermore, the absence of dielectric-related loss and the ability to maintain non-dispersive, single-mode propagation over a very broad bandwidth lead to low attenuation well into the millimeter-wave frequencies.

4. Microshield Line Components

A. Right Angle Bends

A very common circuit 'element' in millimeter-wave systems is the right-angle bend. This structure gains significance with increasing frequency due to the parasitic capacitance and inductance which are associated with the abrupt change in the field orientation. These problems, combined with mode-conversion, result in a high reflection of the incident power (large S_{11}). In coplanar waveguide designs, the typical means of improving the return loss is to utilize air-bridges or dielectric overlays [7]. Both of these techniques are meant to offset the effects of different electrical path lengths along the two slots. Without this type of compensation, the asymmetry of the CPW right-angle bend will lead to excitation of the unwanted slot-line mode.

Many of the problems inherent to bends which are printed on conventional CPW can be minimized with the microshield geometry. The absence of the high dielectric constant material has two important effects: it leads to a reduction in the parasitic capacitance and, for a fixed physical size, it reduces the difference in electrical path lengths through the two slots. The shielding cavity, furthermore, provides continuous ground plane equalization without introducing additional discontinuities, thus improving upon conventional air-bridges. A comparison between the measured performance of a microshield-line bend and a typical CPW bend on GaAs [8] is shown in Figure 4; the microshield bend has an S_{11} which is at least 8 dB lower over the 10-40 GHz band. The noise in the data below 18 GHz is due to calibration error.

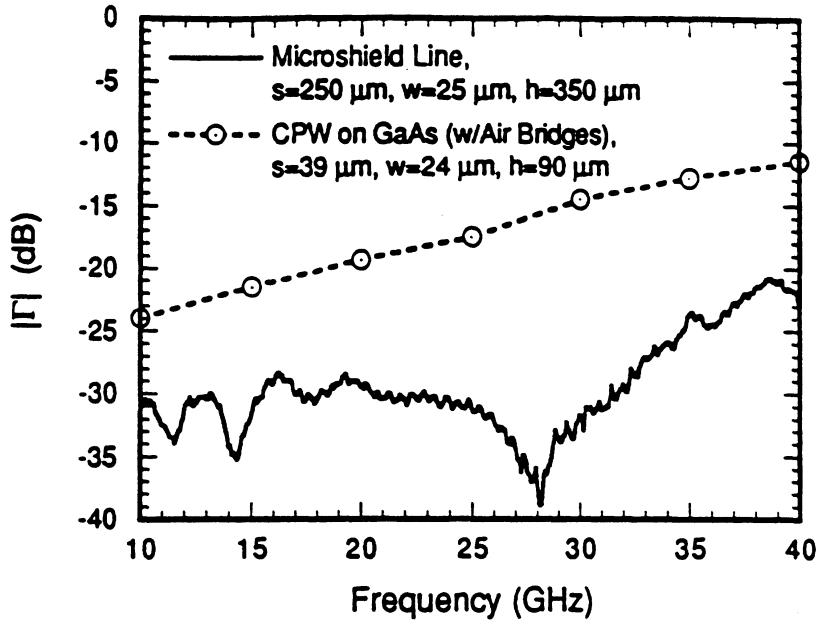

Figure 4. Performance of microshield and CPW right-angle bends.

B. Low-Pass Filters

The stepped-impedance approach to low-pass filter design is a relatively easy technique to use, and it is well suited for applications which do not require a sharp roll-off in the insertion loss. Often, however, the filter specifications call for high rejection over multiple-octave bandwidths, a requirement which may be difficult to meet using conventional substrate-supported lines due to the propagation of higher order modes. Thus, the very broad, single-mode bandwidth of the microshield line can provide superior filter performance in this respect. In addition, the absence of dielectric-related loss reduces both attenuation and parasitic radiation, resulting in very low passband insertion loss.

Stepped-impedance filters using 5-, 7-, and 9-sections have been designed and tested. Some of the results were previously presented in [9], where it was shown that the measured performance compared very well with ideal transmission line theory, as a result of the pure TEM nature of the microshield propagating mode. In Figure 5, measured data for a 5-section filter is compared with results from a full-wave moment-method analysis. The rejection is greater than 20 dB up to 75 GHz, which is about 1.5 octaves above the 3-dB point at 26 GHz. The measured passband insertion loss of this filter is between 0.2 and 0.5 dB from 20-23 GHz.

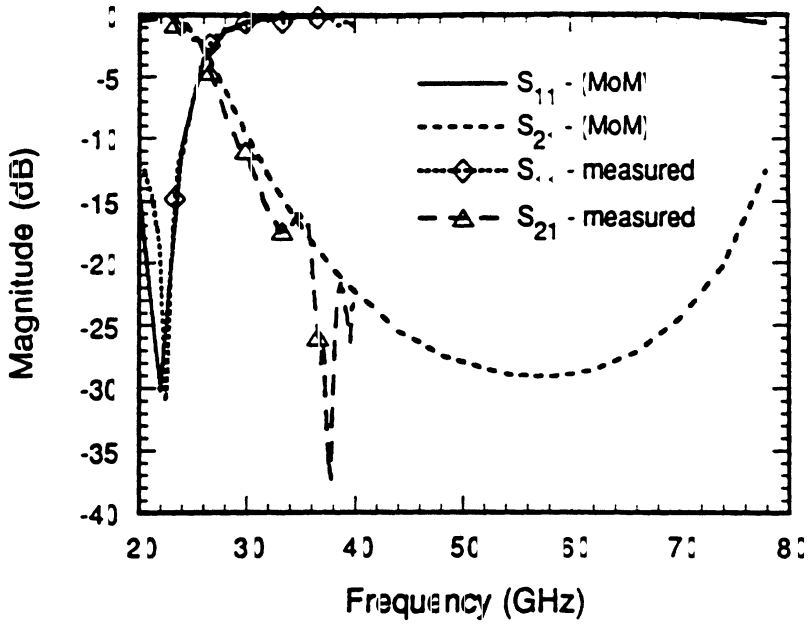

Figure 5. Performance of a 5-section stepped-impedance low-pass filter.

C. Band-Pass Filters

By cascading multiple open-end tuning stubs in series, it is quite simple to realize a bandpass response with high out-of-band rejection and low insertion loss. The geometry of a three-stage design is shown in Figure 6, in which each section is separated by 150 μm. The measured response, shown in Figure 7, has an insertion loss of only 1.0 dB from 22-32 GHz, which is competitive with the best shielded bandpass filters using suspended stripline [10]. The performance of this microshield filter could be further improved using thicker metallization (since the one micron thickness is equivalent to just over two skin-depths) or larger slot widths to minimize the conductor loss. The calculated data included in the plot is generated by using the scattering parameters found from the full-wave analysis of a single stub section and treating the filter as three non-coupled elements in series. The agreement between the measured and calculated performance is quite good and indicates that there is very little electromagnetic coupling between the stubs, even though the stub separation is only 150 μm. The response of the filter can also be modeled almost exactly by cascading the *measured* results for a single stub, and this approach accurately predicts the 1.0 dB insertion loss.

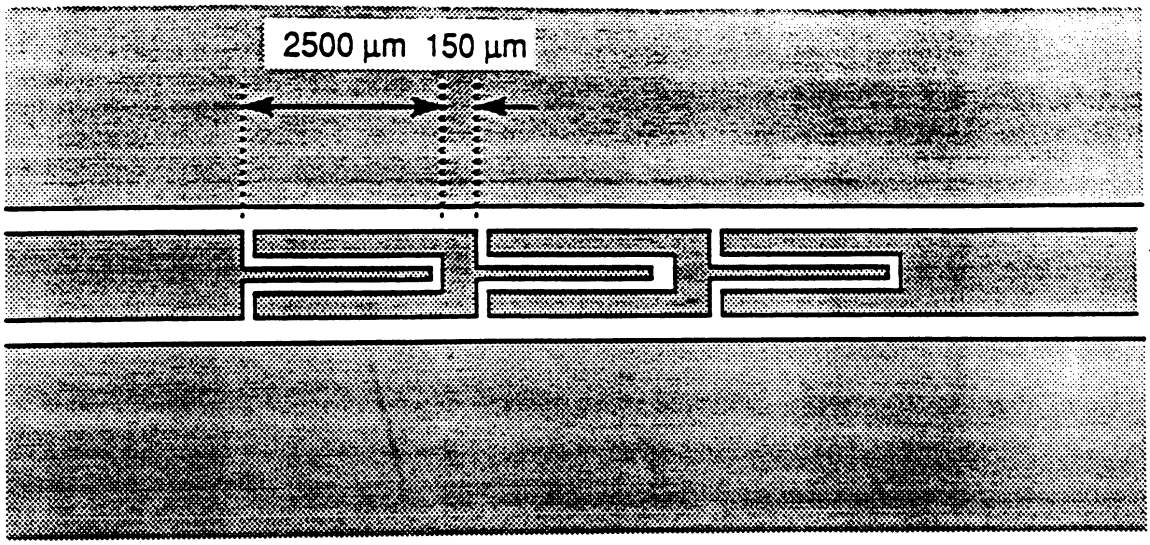

Figure 6. Geometry of a microshield line bandpass filter.

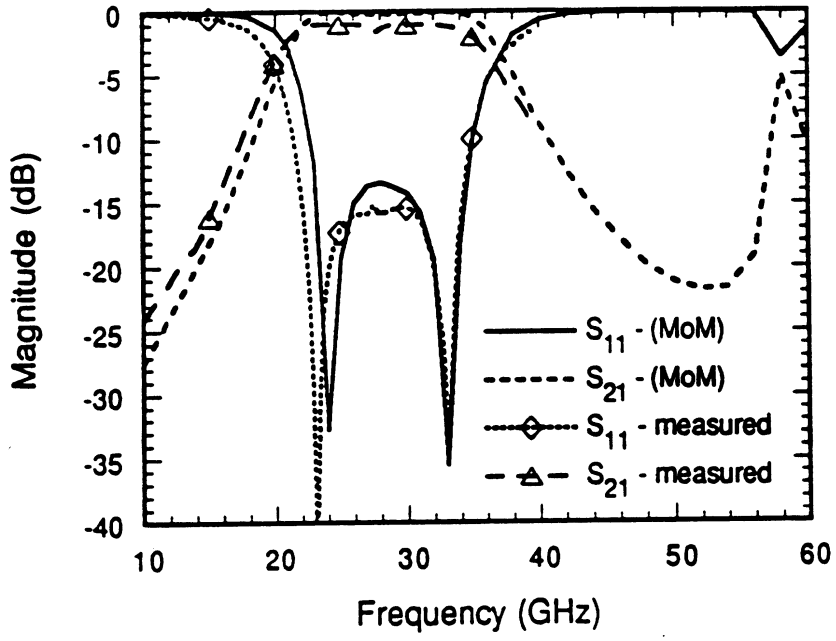

Figure 7. Performance of a microshield line bandpass filter.

5. Conclusions

Microshield line has been shown to be a very low loss, low dispersion transmission line well into the sub-millimeter wave frequency range. This work has demonstrated microshield circuit components with excellent performance at frequencies as high as 40 GHz, and continuing work at the University of Michigan has realized a 90 GHz low-pass filter and a 250 GHz band-pass filter. This recent work will be presented in detail in forthcoming publications.

6. Acknowledgments

This work was supported by the NASA Center for Space Terahertz Technology and the Office of Naval Research.

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Micromachined Circuits for Mm-Wave Applications

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ABSTRACT

A novel transmission line which utilizes micromachining techniques in the development of circuits for millimeter-wave applications is presented. Micromachined circuits incorporate the fabrication of an upper-half shielding environment with the circuit geometry. The circuit development requires the use two silicon wafers where one has cavities that have been etched using anisotropic etching while the other one has the planar circuits which have been printed using standard photolithographic techniques. Afterwards, the two wafers are aligned and secured using bonding techniques to form a circuit that has an upper-half shielded cavity incorporated monolithically. This paper presents a detailed description of the fabrication procedure necessary for upper-half shielded (UHS) circuits as well as for completely shielded (CS) circuits. Experimental results of the upper-half shielded circuits will be presented and compared to theoretical data as well as data for conventional coplanar waveguide circuits of the same type.

INTRODUCTION

Uniplanar transmission lines, such as microstrip, coplanar waveguide and slotline have provided enhanced flexibility in high-frequency circuit design, reduced weight and volume, and compatibility to high-speed active devices. Planarization, however, gives rise to unwanted frequency dependent mechanisms such as parasitic coupling and radiation which deteriorate electrical performance and lead to costly and time intensive design cycles. Suppression of these electromagnetic mechanisms has led to improved performances but has required very sophisticated packages which considerably add to the volume, weight and most important cost of the circuits. Consequently, the development of new packaging techniques which minimize cost and reduce volume and weight can have a major impact in today's technology and can lead to high volume markets.

This paper presents the development of miniaturized circuits of coplanar waveguide type where the package has been fabricated and integrated with the rest of the circuit using Si-based Micromachining [1],[2]. The characterization of these circuits has been completed both theoretically and experimentally with very close agreement between theory and experiment. In the following sections the fabrication process of micromachined circuits is described and theoretical as well as experimental data are presented and discussed for a variety of three-dimensional structures.

FABRICATION

Micromachined circuits, consisting of conducting lines and metallized cavities, are developed in two stages using a two-wafer system. In this section a comprehensive discussion is presented on

the development of completely shielded as well as upper-half shielded micromachined circuits. First, the cavity structure, Figure 1, is etched into a low resistivity Si wafer (353μm) having a 1.4 μm dielectric tri-layer of oxide/nitride/oxide. This wafer requires the production of alignment marks which are etched through the entire wafer along with cavities which are etched through partially. In this process, the areas to be etched are defined using standard photolithographic techniques. Since the tri-layer must be removed in the areas of silicon to be etched, the upper oxide layer is etched using buffered HF while the middle nitride layer is etched by a plasma etcher. The wafer is then repatriated to expose and remove the lower oxide layer in the areas that will be etched entirely while preserving the lower oxide layer in the areas that will be etched partially.

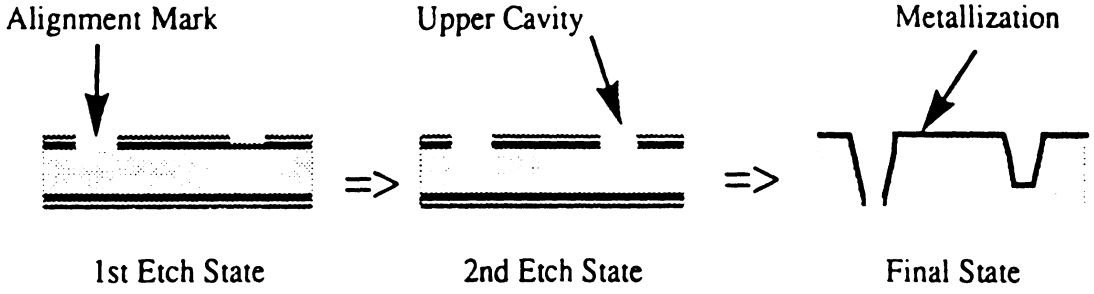


FIGURE 1. Development of cavity regions on the upper wafer for Micromachined circuits.

Since the tri-layer dielectric is used as a mask when anisotropically etching, with KOH or EDP, the initial desired depth is etched into the silicon surface. Next, the remaining lower oxide layer in the cavity areas is removed using buffered HF and the wafer is etched for the remaining depth to produce both the alignment windows and appropriate cavity depth.

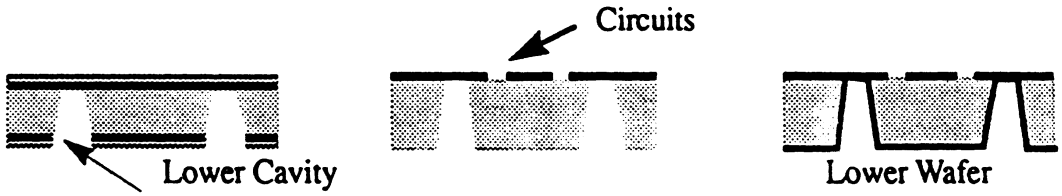


FIGURE 2. Development of cavity regions and circuits on the lower wafer for the Micromachined circuits.

For the development of completely shielded circuits, cavities must be incorporated below the surface of the circuit layer. This is done by anisotropically etching grooves in the backside of a high resistivity Si wafer (353μm) having the tri-layer dielectric mask as described above. Next, planar CPW-like geometries are printed, using photolithographic and metal evaporation techniques for a lift-off procedure. Once complete, the cavity structure is then metallized using evaporation techniques.

FIGURE 3. Micromachined Completely Shielded and Upper-Half Shielded Circuit in two-dimensions.

Finally, alignment of the upper cavity to the planar circuits is obtained via microscope and the two wafers are attached using regular adhesion methods or Si-to-Si electrobonding. While the procedure

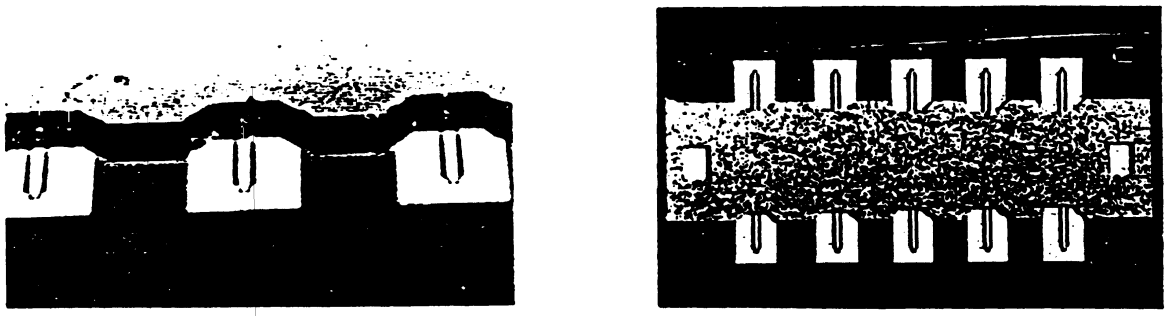
described above concen ra es on the development of completely shielded circuits. the upper-half shielded circuit follows he same procedure with he exclusion of the lower cavity etching step.

RESULTS AND DISCUSSION

MEASUREMENT SYSTEM:

The micromachined circuits are measured using an HP 8510B Network Analyzer sys em, which oper-a.es a. frequencies up to 40 GHz. Measurements are ob.ained from Cascade Micro.ech high frequency GSG probes via an Alessi probe station. In order to suppress parallel plate and microstrip modes between the circuits and the wafer chuck of the probe station, the circuit wafer is placed on 1/8" thick 5880 RT/Duroid having e_r=2.2. The Thru-Reflect-Line (TRL) calibration is performed to eliminate the effects of the connectors, cables and probes from .he measured data and to accurately establish a known reference plane for the various circuits. After calibrating, scattering parameter measuremen s of the circuits were obtained to compare theoretical and experimental data.

CIRCUIT DESCRIPTION:



(a) Front View (b) Top View

FIGURE 4. Micromachined Shielded CPW, Cavity Dimensions: height = 200 μm and width = 800 μm.

The fabricated and tested circuits are both open CPW and micromachined upper-half shielded CPW, as shown on Figure 4. The cavity region for these circuits are 800μm wide and 200μm high. Each circuit is fed by ungrounded open coplanar waveguide which has feed lines that transition from center conductor width of 100 μm to 180μm and slot width of 50μm to 130 μm. Since the TRL calibration is used, calibration standards are also fabricated to include identical cpw feed line to shielded region transitions for accurate calibration of the micromachined circuits.

MEASUREMENT RESULTS:

The experimental results shown are for the micromachined upper-half shielded (UHS) circuit. Initial characterization is obtained by measuring the scattering parameters of a through line where the performance characteristics are extracted. Below in Figure 5 is a graph that shows that the total loss of the through line, is about 0.08 dB/λ_g.

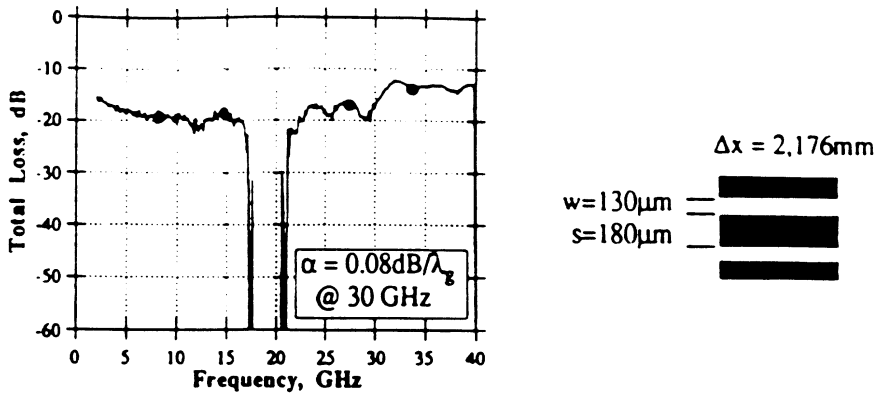


FIGURE 5. Through line characteristics for the Micromachined Upper-Half Shielded CPW.

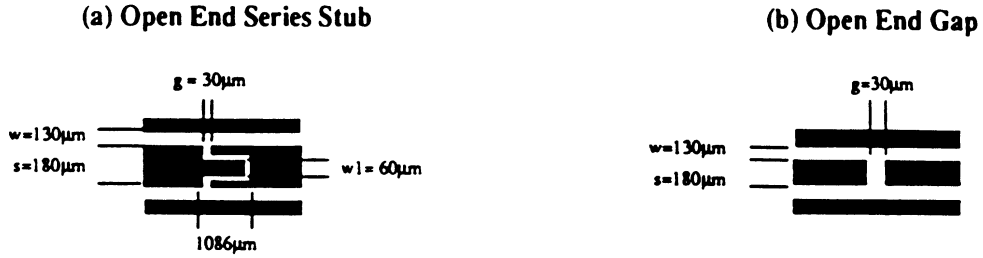


FIGURE 6. Circuit description for the (a) Open End Series Stub and the (b) Open End Gap.

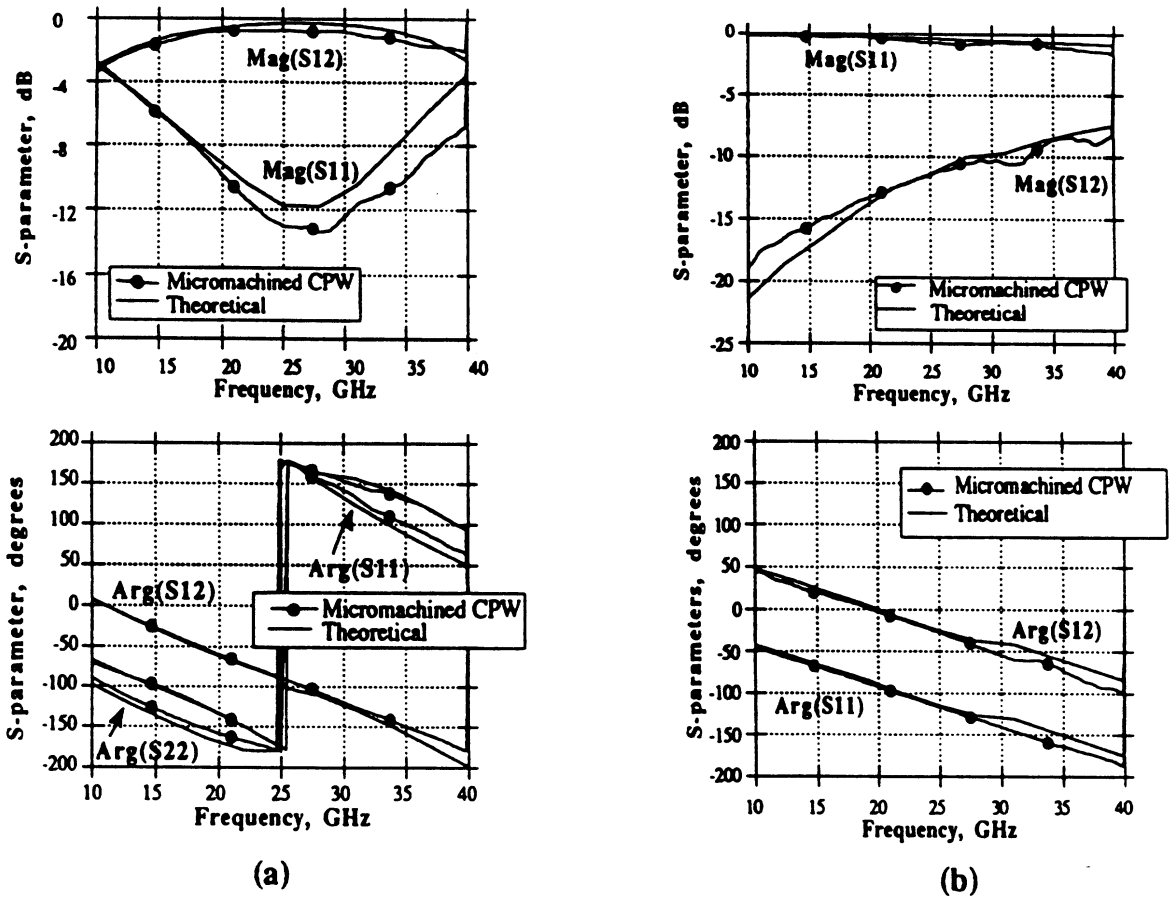


FIGURE 7. Micromachined UHS CPW, Theoretical vs. Experimental.: (a) Open End Series Stub and (b) Open-End Gap.

Various circuits were measured as part of this characterization effort which include an open-end series stub, designed to resonate at 30 GHz, and an open-end gap as shown above in Figure 6. Figure 7 shows a comparison between theoretical and experimental data for the micromachined UHS open-end series stub and open-end gap respectively. The theoretical results were derived using a full-wave space-domain integral equation technique [3] and agree very well with the experimental results in both the

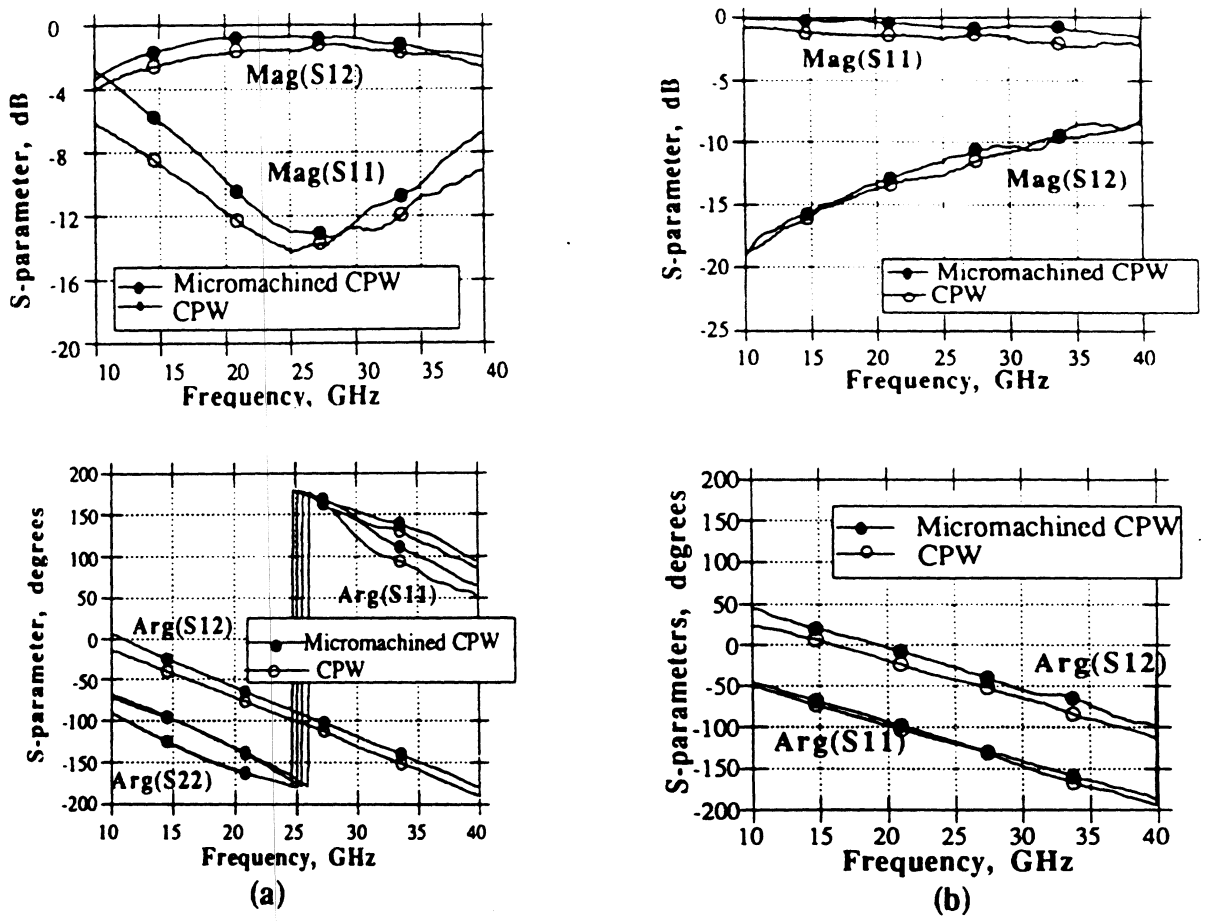


FIGURE 8. Micromachined UHS CPW vs. CPW: (a) Open End Series Stub and (b) Open End Gap.

magnitude and phase. Figure 8 shows a comparison between experimental data for the micromachined UHS CPW and open CPW in the case of the open end series stub and open end gap circuits. The results indeed verify that the micromachined cavity does not affect the electrical performance of the planar circuit.

Similarly, Figure 9 below shows experimentally measured total loss for the open end series stub and open end gap. The total loss is reduced by an average of 3 dBs from 10 to 40 GHz for the micromachined UHS CPW as compared to the open CPW. This reduction is due to elimination of radiation in the upper-half region of the circuit and emphasizes the effectiveness of the integrated cavity. Although the primary focus has been on the upper-half shielded circuits, some experimental results for the completely shielded geometries will be presented at the conference.

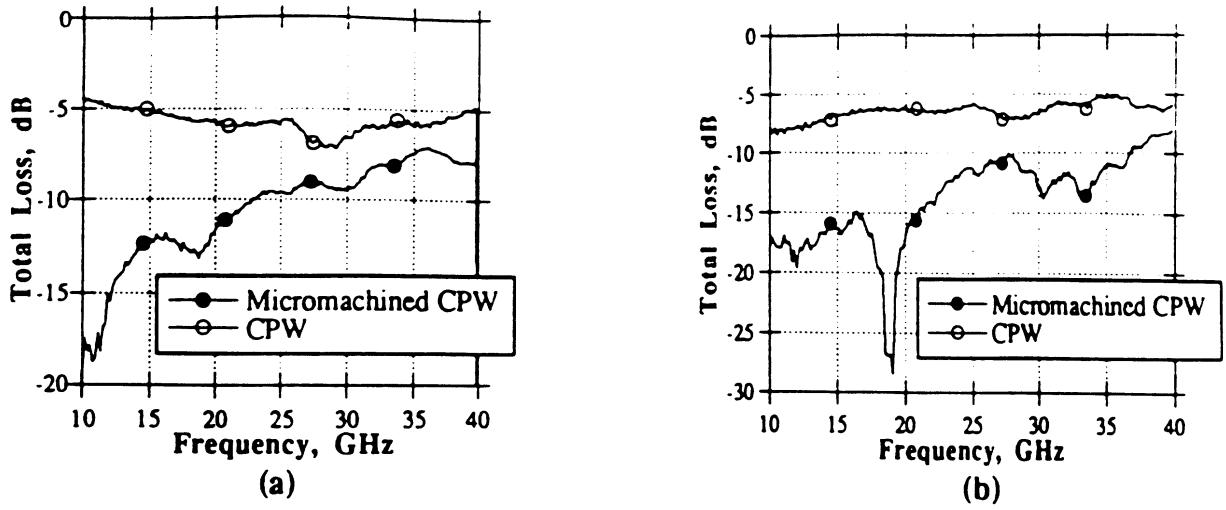


FIGURE 9. Micromachined UHS CPW vs. CPW Total Loss: (a) Open End Series Stub and (b) Open End Gap.

CONCLUSION

In conclusion, we have presented the development of micromachined circuits of simple geometries. The fabrication has been shown for both the completely shielded and upper-half shielded circuits. Comparisons have been shown between the upper-half shielded circuits and theory as well as open CPW measurements. Thus, with the improvement of the above loss performance combined with smaller volume and lower weight, micromachined circuits indeed make a very good candidate for development of integrated microwave and millimeter-wave packages.

ACKNOWLEDGMENTS

This work was partially supported by the Office of Naval Research and the NASA Center of Space Terahertz Technology.

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MICROMACHINED DETECTOR MOUNTS FOR MILLIMETER WAVE APPLICATIONS

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Abstract

High frequency circuit development requires that circuits are miniature in size with good electrical performance. These types of circuits can be achieved by utilizing micromachining techniques that allow individual planar geometries and shielding environment to be fabricated monolithically. This paper will present the development of such circuits including a detector mount where the advantage of this configuration is a lowcost circuit system with small weight and volume. Since the shield is integrated with the planar geometries, characterization is simplified and the resulting circuit performance is comparable to conventional planar lines. At the higher frequencies this is particularly useful since various geometries can be easily fabricated using silicon micromachining techniques.

1.0 Introduction

Micromachined circuits have been studied at the University of Michigan for development of passive circuit components [1] where the individual planar geometries and shielding environment are fabricated monolithically resulting in miniaturization of conventional circuit components. The advantage of this configuration is a lightweight circuit system with small weight and volume. In addition, characterization of such systems is simplified since the shield is integrated with the planar components resulting in circuit performance that is comparable to conventional planar lines. For higher frequency applications, this is particularly useful since various geometries can be easily fabricated to desired dimensional requirements using silicon micromachining techniques.

This paper presents the development of a variety of micromachined circuits including a detector mount that utilizes the advantages of micromachining to create the circuit components and a

mounting structure for planar diodes. A description of the development of the system and the sub-components required along with a discussion of circuit performance is presented.

2.0 Fabrication Issues

The mounting structure is a two silicon <100> wafer system which relies primarily on standard fabrication processes and etching techniques. The semiconductor processing steps include standard photolithography techniques for wafer patterning along with lift-off and evaporation techniques for metallization of the patterned areas. Ethylene diamine pyrocatechol (EDP), an anisotropic etchant, is used to etch silicon where it selectively stops on the <111> crystal plane resulting in sidewall angles of 54.7° as shown in Figure 1.

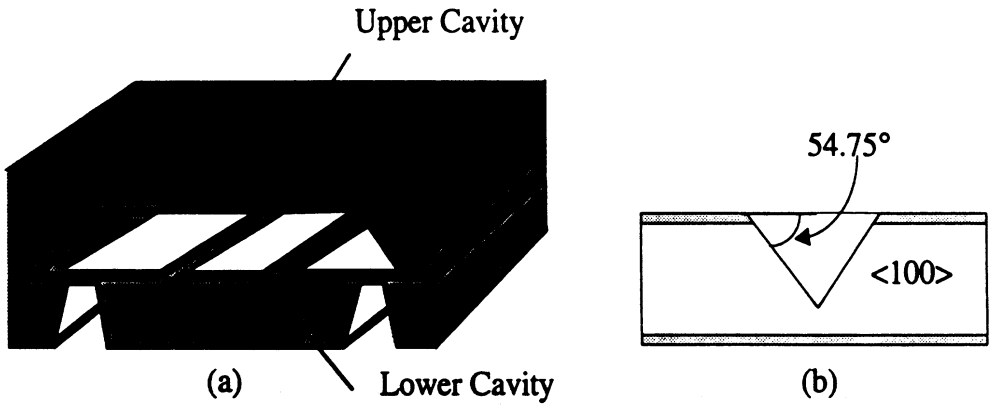

FIGURE 1. Two wafer silicon system of the transmission line with integrated shielding environment.

In Figure 1, the top wafer shows the air-filled upper cavity, having a width of 1200 μm and height of 280 μm, that is metallized after etching low resistivity silicon. On the bottom wafer coplanar waveguide transmission lines are printed on the polished side of high resistivity silicon using photolithography with lift-off and evaporation techniques for metallization. Since the etched grooves on the bottotm side of this wafer define the lower substrate-filled cavity, they are metallized last to provide the lower shielded region having a height of 350 μm and width of 950 μm. Once the indi-

vidual wafers are fabricated, they are secured using adhesion techniques while alignment is done via alignment windows.

3.0 Circuit Design and Results

Since micromachining techniques allow the integration of the shield with the transmission line components, circuit parameters are needed to establish a feedline that matches to 50 ohm systems. For the configuration shown in Figure 1, the transmission lines are coplanar waveguides having a conductor width of 180 μm and a slot width of 130 μm with above shielding dimensions.

For very high frequency circuits, initial circuit performance can be determined using on-wafer measurement techniques in the Ka-band. The results provide good indicators of the expected circuit response when scaled to terahertz frequencies excluding loss performance. In order to accurately measure the circuits, however, the measurement test wafer contains various circuit components having identical upper and lower shielded regions in addition to individual calibration lines, needed for the performance of a Thru-Reflect-Line (TRL) de-embedding [2,3]. Resulting experimental measurements of the micromachined circuits are thus obtained using on-wafer probing techniques [4] via a measurement system which consists of an HP 8510B Network Analyzer, Alessi Probe Station, and Cascade Microtech ground-signal-ground (GSG) probes with 150μm pitch.

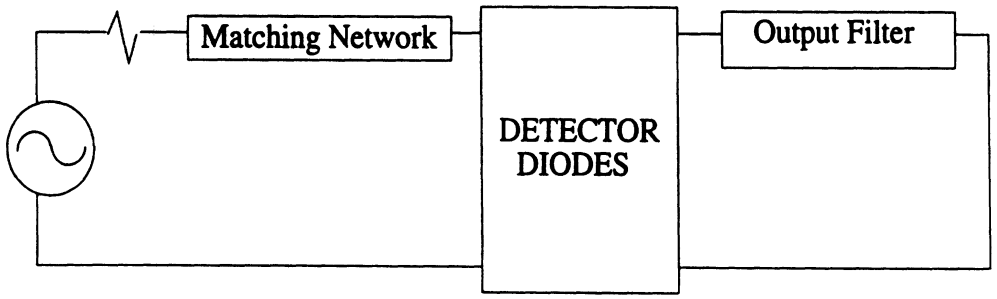

FIGURE 2. Detector Mounting Structure Design Scheme

Specific design issues are addressed in order to develop a micromachined detector which requires the use of the circuit shown in Figure 1 [5]. The design procedure begins by determining [6] and evaluating the range of realizable impedances available to implement a lowpass filter with a requirement of -20 dB insertion loss and the open circuit input impedance at the design frequency. Using the cross-sectional dimensions of the shielded regions given above, the high and low impedances are determined where the low impedance sections have a conductor width of 380 μm and slot width of 30 μm and high impedance section has conductor width of 20 μm and slot width of 210 μm. The filter response shown below in Figure 2 for a 5 section stepped impedance filter is compared to results obtained from a finite difference time-domain model [7].

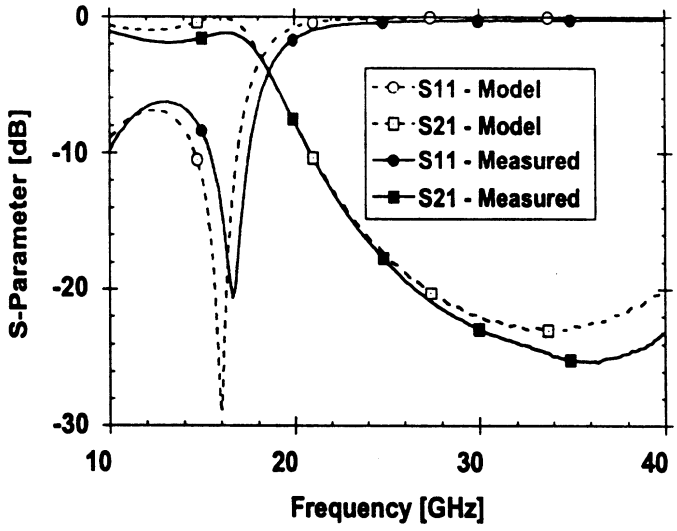

FIGURE 3. 5-section Stepped Impedance Lowpass Filter

The above response is needed in order to match the output of the filter design. Since the transmission lines are coplanar waveguides, this detector scheme uses the diodes in an anti-parallel configuration across the slots. In order to determine an appropriate input matching network the dc parameters of the diodes must be determined to minimize the power reflected from the diode input.

4.0 Conclusion

Subsystem components have been developed for a detector mounting scheme. In order to complete the detector system, in-house or commercially available diodes may be used which determine the type of appropriate input matching network. From a circuit perspective, micromachining can be used to develop detector mounting structures quite easily, where the problem is addressed from a component level prior to cascading these elements into the overall system.

5.0 Acknowledgments

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Development of Miniature Microwave Circuit Components Using Micromachining Techniques

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ABSTRACT

Miniature microwave circuit components are presented that were developed using silicon micromachining techniques. Although micromachining is very well known in sensor applications, it is used, herein, for the first time in microwave applications. This paper presents the development of micromachined lines and describes the theoretical and experimental characterization of circuit components such as filters and tuning stubs.

1.0 INTRODUCTION

In the past, planar transmission lines such as microstrip, stripline, and coplanar waveguide have provided flexibility in the design of microwave circuits and ease in mounting active components. In almost all design cycles, these circuits are typically developed and tested in an open environment. Once the performance is characterized, however, these circuits are mounted into a metal housing which may introduce unwanted parasitics and multiple resonances leading to the degradation of the overall circuit performance. In addition, this approach is costly and rather impractical for developing lightweight systems since the main contribution to the overall weight is the circuit housing. Miniaturized high frequency circuits with an integrated housing offer lightweight and controllable parasitics, which makes them appropriate for cellular and mobile communications in view of the system requirements.

In an effort to develop miniaturized circuits which perform comparably to conventional transmission lines, micromachining techniques can be used. Ultimately, complex micromachined systems such as detectors, mixers, and integrated receivers can be developed, thus leading to a new advanced technology. However, in order to make the development of such systems possible, realization of primary high frequency circuit components like filters and tuning stubs is required.

This paper presents the development of miniature high frequency circuit components which incorporate a monolithic shielding environment. The study includes an discussion of the fabrication procedures as well as an extensive theoretical and experimental characterization of tuning stubs and stepped impedance filters.

2.0 FABRICATION

Micromachining processes are fairly standard in sensor applications, however, they are relatively new to high frequency circuit applications. The miniaturized circuits mentioned above are a two silicon <100> wafer system and rely primarily on the micromachining process of silicon etching. This etching is done using ethylene diamine pyrocatechol (EDP) which is an anisotropic etchant to silicon. Other semiconductor processing steps include standard photolithography techniques used for wafer patterning along with lift-off and evaporation techniques used for metallization of the patterned areas.

In Figure 1, the top wafer shows the upper cavity, having a width of 1200 μm and depth of 280 μm, that is metallized after etching low resistivity silicon. On the bottom wafer, transmission lines of coplanar waveguide type are printed on the polished side of high resistivity silicon using photolithography, lift-off techniques and evaporation techniques for metallization of 1μm. Since the etched grooves on bottom side of the wafer define the lower substrate-filled cavity, they are metallized last to provide the lower shielded region having a depth of 350 μm and width of 950 μm. Once the individual wafers are fabricated, they are secured using adhesion techniques while alignment is done via alignment windows. This process results in a monolithic shielded transmission line, Figure 2, that is reduced considerably in size compared to conventional structures placed in a metal housing.

3.0 RESULTS AND DISCUSSION

In this paper results are presented for a seven section stepped impedance filter and a series shorted stub. To determine the desired characteristic impedance of the miniature circuits, quasi-static models by Dib based on point matching techniques[1] are applied to obtain the appropriate line and cavity dimensions. Once the circuits are fabricated and actual dimensions are determined, the measured results are then compared to theoretical ones. The stepped impedance filter was designed using PUFF [2], a quasi-static model that allows for synthesis and analysis of simple circuits of microstrip form. Intricate geometries like the series short stub, however, require the use of more sophisticated models. Among the various full-wave analysis techniques, the space domain integral equation is appropriate to accurately compute the electric field distribution in planar shielded geometries as the ones considered here. This approach uses Galerkins method to determine the electromagnetic fields and simple network analysis to derive the scattering parameters[3].

The measurement test wafer contains various circuit components having identical upper and lower shielded regions in addition to individual calibration lines, needed for the performance of a Thru-Reflect-Line (TRL) de-embedding [5,6]. Resulting experimental measurements of the micromachined circuits are thus obtained using on-wafer probing techniques [4] via a measurement system which consists of an HP 8510B Network Analyzer, Alessi Probe Station, and Cascade Microtech ground-signal-ground (GSG) probes with 150μm pitch.

A seven-section stepped-impedance lowpass filter, designed as shown in Figure 3, has high and low impedance of 100Ω and 20Ω respectively and is surrounded by the cavity structure described above. In Figures 4 and 5 measurements are shown and compared to theoretical results derived from quasi-static models where conductor and dielectric losses are included. Regarding conductor losses, care was taken to incorporate the specific metallization thickness and the appropriate surface resistivity corresponding to the various sections of microstrip line widths [7]. To realize 100 and 20 ohm impedance steps, 15 μm and 380 μm wide conductor lines are used with slot widths of 215μm and 30 μm. In the low impedance section, however, the line excites a coplanar waveguide mode due to the narrow slot width

while the high impedance section excites a microstrip mode. This results in sections of line that operate in a mixed mode and create parasitics that cannot be easily accounted for in the current model. Despite this limitation, however, it can be seen in Figure 4 that the magnitude and phase measurements agree very well with the model. This is due to the relatively low operating frequency which reduces the effect of the parasitics. The total loss in the system, as shown in Figure 5, shows good agreement between theory and measured results indicating that the circuits have negligible radiation loss thus confirming the effectiveness of the micromachined integrated shield. The level of loss is due to the fact that low and high impedance sections have aspect ratios that have been shown to cause higher loss for both the coplanar waveguide mode [8] and the microstrip mode[7]. Minimizing the effect of the conductor loss can be done by increasing the metallization thickness to about 3 μm, as opposed to 1μm used in this effort.

Figure 6 shows the physical dimensions of a series short tuning stub while Figure 7 shows comparison between measurements and the full wave analysis results. Since the theoretical results do not account for losses, the difference in the magnitude between measurements and theory is expected. While the overall circuit performance is similar, the discrepancy in the resonant frequency can be attributed to the variations in actual cavity dimensions and those allowable in the model. The model assumes that the cavity is rectangular, whereas, in reality the cavity is trapezoidal due to anisotropic etching. Furthermore, the upper cavity is wider than the lower cavity (see Figure 1) while the model assumes identical widths. In addition, the measured line length behaves electrically shorter due to rounding of the corners and edges of the stub fingers during fabrication.

Overall, both the series short stub and the low pass filter show good agreement with the theoretical predictions. As a result, the above study indicates the capability of micromachining to provide high frequency circuit components with a performance comparable to conventional circuits.

4.0 CONCLUSION

The development of miniature microwave circuits has been proven successful. The fabrication of these lines has been presented and measured results have been shown and compared to quasi-static and full-wave theoretical ones. The data presented show that monolithic integration of the shield using micromachining techniques allows for the development of circuit components that offer comparable performance to conventional shielded circuits. To further improve the circuit performance and reduce conductor losses, appropriate metallization thickness for the ground plane as well as the conducting line should be incorporated. The miniature form of these circuits is verified when comparing the geometrical cross-section to waveguide E-plane circuits which are commercially available for a wide range of frequencies.

5.0 ACKNOWLEDGEMENTS

This work has been supported by the Office of Naval Research under contract No.N00014-92-J-1070 and the NASA Center for Space Terahertz Technology. The authors would like to thank Dr. Nihad Dib for his contribution of theoretical models.

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LIST OF FIGURES

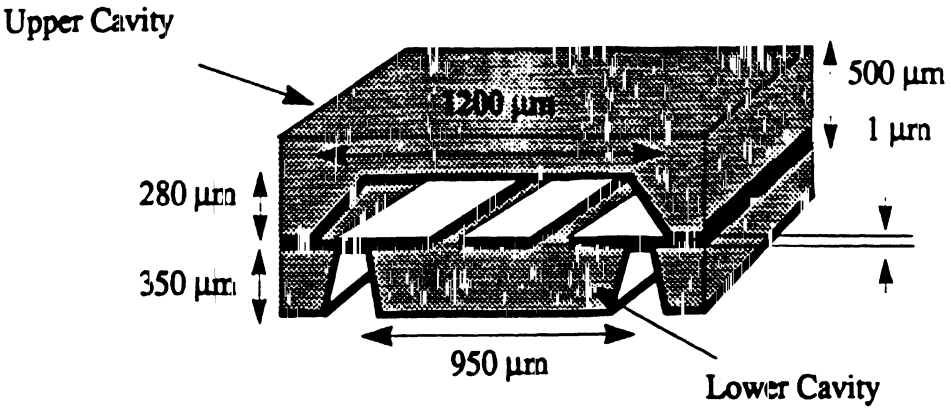

FIGURE 1. Miniature Microwave Circuit in Completely Shielded Form

FIGURE 2. Photograph of Miniature Microwave Circuit in Completely Shielded Form.

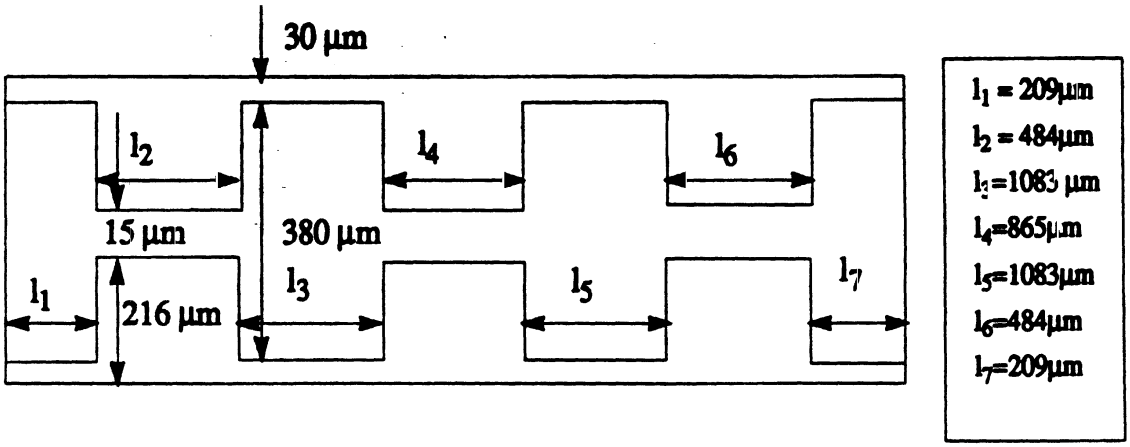

FIGURE 3. Stepped Impedance LowPass Filter Circuit Dimensions with low impedance sections of 20 Ω and high impedance sections of 100 Ω

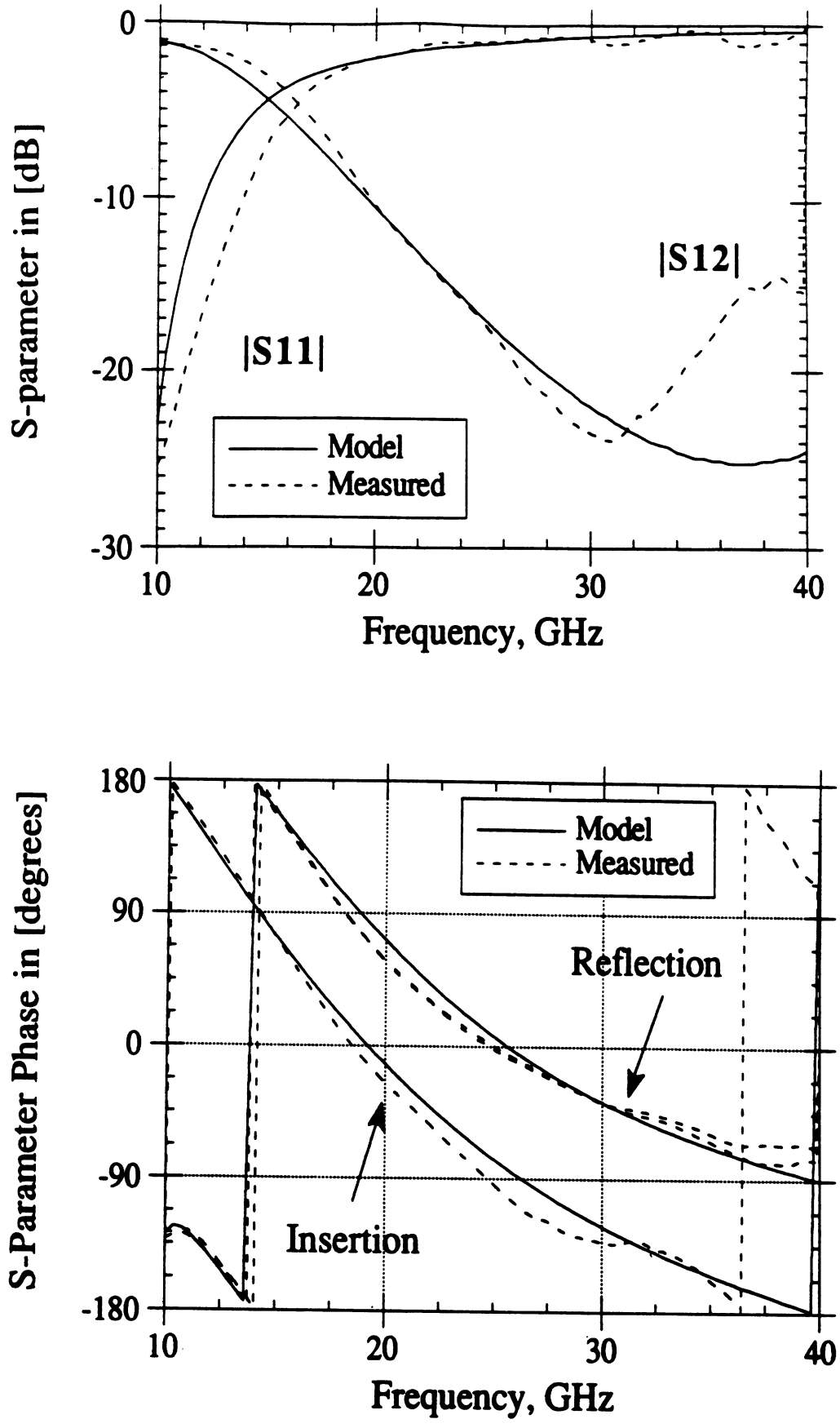

FIGURE 4. Theoretical and Experimental Results for the Completely Shielded Stepped Impedance Low Pass Filter. The top view shows the magnitude of the S-parameters while the lower view shows the phase.

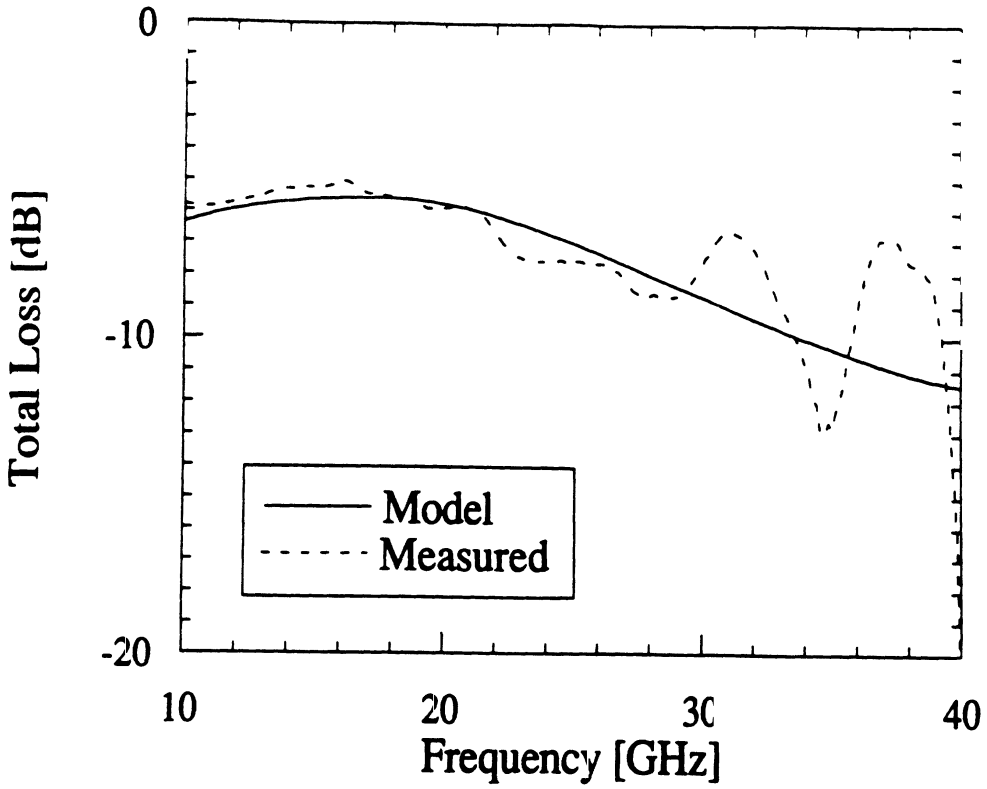

FIGURE 5. Measured and Theoretical Total Loss Measurement for the Completely Shielded Stepped Impedance Low Pass Filter

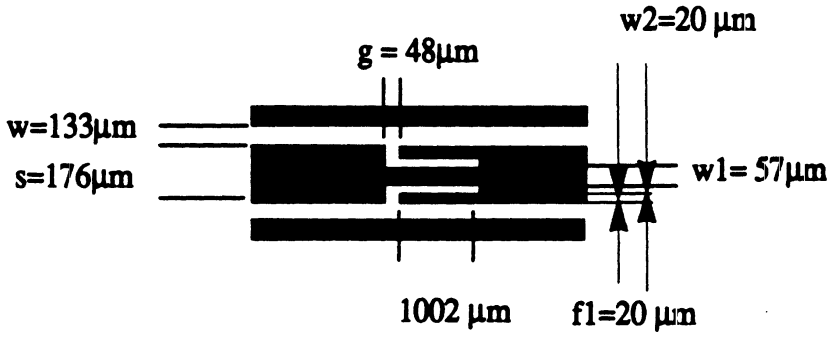

FIGURE 6. Circuit description for the Series Short Stub.

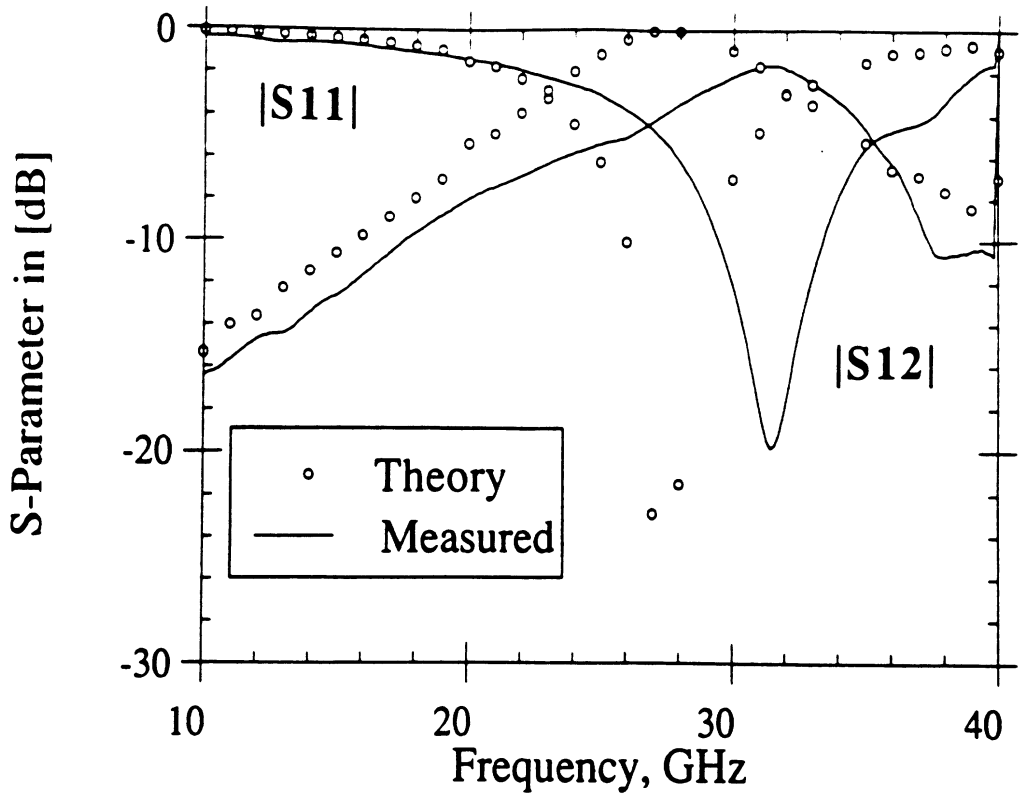

FIGURE 7. Measured and Theoretical Results for the Completely Shielded Series Short Tuning Stub

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Development and Characterization of Miniaturized Circuits for High-Frequency Applications using Micromachining Techniques

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Abstract

Wireless and personal communications systems require lightweight, high frequency circuits that provide compactness as well as optimum electrical performance. In order to advance current capabilities in these areas, two design approaches have recently been developed at the University of Michigan. One approach that is directed toward circuit miniaturization utilizes micromachining techniques to realize integrated packages for individual circuit geometries. Another approach that is used to realize high-performance circuits involves the use of dielectric membranes to support the conducting lines. This paper presents the development of these concepts and discusses the fabrication techniques and the performance characteristics of some representative circuits.

Key words: micromachining, dielectric membrane, integrated package, coplanar waveguide, high frequency circuits

INTRODUCTION

High frequency circuit design plays an increasingly important role in the development of complex wireless and personal communication systems. These systems require a wide variety of (monolithic) microwave integrated circuits which utilize planar transmission lines, such as coplanar waveguide, microstrip and slotline. While each of these lines offers greater design flexibility, reduced weight and volume, and simpler integration with active devices when compared to non-planar guiding structures, planarization has resulted in some undesirable side effects. Inherent in these structures are unwanted frequency dependent mechanisms such as parasitic coupling and radiation, as well as conductor and dielectric loss that often result in electrical performance degradation. In order to reduce the coupling and radiation effects, sophisticated packages are usually developed to improve the circuit performance. Unfortunately, they add considerably to the volume and weight of the circuit, and the overall manufacturing cost. Transmission loss can be reduced by using a low loss material such as alumina, but this requires laser dicing techniques and cannot be utilized in an MMIC implementation. A solution that can address the above issues and provide an inexpensive alternative is the use of micromachining. Unwanted radiation can be suppressed by developing packages that are integrated monolithically with the circuit, while dielectric loss can be eliminated by developing circuits on free-standing dielectric membranes.

Presented here are two approaches that use micromachining extensively to realize novel circuits. The first approach introduces packaging of miniaturized circuits with integrated cavities, and emphasizes size/volume/cost reduction. The second approach involves a membrane-supported transmission line configuration and emphasizes superior performance as its main objective. While both techniques are compatible with silicon and GaAs processes, the work described here is exclusively silicon-based. This paper describes the design of each new geometry, along with an outline of the fabrication procedures. Performance is shown that indicates the effectiveness of the dielectric membrane-supported line as a low loss transmission line. Also included are curves that show the response of a completely shielded tuning stub and a membrane supported right-angle bend at Ka-band.

MICROMACHINED CIRCUIT METHODOLOGY

The process steps applied in this work come primarily from a mature silicon micromachining technology. They are standard practice, for example, in developing microstructures for sensor applications. For high frequency circuit design, however, the use of micromachining is relatively new. Therefore, the following sections describe the specific fabrication steps required to implement the new circuit geometries: monolithically integrated shielded circuits and dielectric membrane-supported circuits.

Monolithically Integrated Shielded Circuits

Circuit miniaturization can be achieved by implementing structures which minimize the size and weight of the housing element used to package circuit components. By developing cavities that follow the path of individual circuits and provide good isolation, the effective circuit area is reduced and the overall packing density can be increased. This concept has been explored using micromachining techniques and the resulting procedure will be described in the following section.

The micromachined circuits presented here have a shielding environment that has been integrated using a two-wafer system. Individual circuits are isolated by including a substrate-filled cavity beneath each line in the lower wafer and an air-filled cavity in the upper wafer (Figure 1). The integration of windows that are etched entirely through the upper wafer allows repeatable alignment of the wafers. Finally, for measurement purposes the circuits are fed through grounded coplanar waveguide (GCPW) lines that transition from microwave probe pads into the shielded lines.

The *lower wafer* shown in Figure 2 is a high resistivity, silicon wafer with ε_r of 11.7 and a thickness of 350 μm. To develop the circuits, the planar lines and alignment marks are printed on the silicon dioxide masking layer using standard photolithographic techniques. Next, the lower side of the wafer is patterned using an infrared alignment to expose the regions that form the lower cavity. Prior to anisotropically etching the silicon, the oxide mask is removed from the these areas using buffered hydrofluoric acid (BHF). The anisotropic etchant, ethylene diamine pyrocatechol (EDP), uses the <111> crystal plane of <100> silicon wafers as an etch stop. This causes an etch angle profile of 54.75° on the sidewalls of the cavities as seen in Figure 2b, with the lower cavity having its widest dimension near the upper surface. Prior to the final metallization of the lower cavities, the oxide in the groove underneath the ground plane is removed. This allows direct metal-to-metal contact between the lower cavity and the CPW ground planes.

The *upper wafer* requires patterning of both sides prior to etching the cavity, probe windows and alignment marks. In this study, a low resistivity silicon wafer is used having a thickness of 500 μm with 7,500 Å of thermal oxide on both sides. In Figure 2d, probe windows and alignment marks to be etched are defined on the lower side of the wafer using a lift-off procedure where a thin layer of Ti/Au is deposited. Next, cavities and alignment windows are defined on the opposite side using an infrared alignment, followed by oxide removal in the open areas using BHF to expose the silicon surface for etching. To monitor the etch depth, rectangular marks called etch rulers are also patterned that have widths which correspond to specific depths. The double-sided etching process allows structural beams with constant width to be created in the probe windows as shown in Figure 3, to provide additional mechanical strength to wafers with multiple cavities. After etching, the cavities seen in Figure 2e and 2f are then metallized to the appropriate thickness.

Completely shielded circuits are developed after alignment and attachment of the upper wafer to the lower shielded planar circuits using a microscope. The resulting configuration is shown in Figure 1 where the heights of the upper and lower cavities are 280 and 350 microns, respectively, and the widths are 1180 and 980 microns, respectively.

Dielectric-Membrane Supported Circuit

The objective of the membrane-supported circuit technology is to obtain high performance, broadband operation with minimal dielectric loss or radiation into substrate modes. The first application of this technology was in developing the microshield line [1], which is a partially shielded configuration that is very similar to conventional coplanar waveguide, except that the substrate has been removed. This line has demonstrated excellent performance in a number of circuit applications from Ka-band to W-band [2,3] and the attenuation characteristics have proven to be excellent up to 1 THz [4]. The membrane approach has also been used to implement an air-substrate microstrip line, which was used to design an extremely low-loss Wilkinson power divider at 33 GHz [5].

The basic processing involved in dielectric membrane-supported circuits is similar to that just described for the monolithically integrated shielded circuits. The primary distinction is the use of a thin (1.5 micron-thick) dielectric tri-layer which is composed of SiO_2/

Si_3N_4/SiO_2, grown using a combination of thermal oxidation and chemical vapor deposition. This membrane is deposited on both sides of a silicon wafer and is used both as an etch mask for the micromachining steps and also to support the conducting lines of the transmission line. As with the integrated shielded circuits, the main process steps are the metallization of the planar transmission line patterns and the etching of the silicon cavities and alignment marks. The metallization is done using standard photolithographic, evaporation and lift-off techniques, with a metal thickness typically around 1-1.2 microns. Metal systems of Ti/Pt/Au or Ti/Al/Ti/Au are generally used. The etch steps are performed using photolithographically defined patterns in the membrane, with anisotropic silicon etchants such as EDP or KOH (potassium hydroxide). These steps are meant to remove silicon from beneath the conducting lines in order to form a free-standing membrane.

The fabrication sequence for the microshield line is outlined in Figure 4. In this figure, the micromachining precedes the metallization steps but it is also possible to pattern the planar lines on the upper wafer surface before the etch. Also shown in the illustration is the metallization of the lower shielding cavity that results from the silicon removal. This step is completed with the aid of a "shadow mask" wafer, which is processed along with the membrane wafer, and has rectangular slots that are etched entirely through. The "shadow mask" is attached temporarily to the back of the membrane wafer to prevent metallization under the slot between the center conducting line and the upper ground plane. Etched alignment marks are used to align the "shadow mask" to the membrane wafer, and the two wafers are separated after the backside evaporation. The final step in the microshield process is to mount a lower ground plane wafer to the membrane wafer in order to enclose the lower shielding cavity. Silver epoxy or photoresist may be used as an adhesive. Although the transmission line geometry of the membrane-supported microstrip is different from microshield, the fabrication steps are very similar. The reader is referred to [5] for details.

CIRCUIT PERFORMANCE

The measurement setup used for this work consisted of an HP 8510B Network Analyzer, an Alessi probe station and Cascade Microtech ground-signal-ground probes with a probe pitch of 150 μm. To accurately measure the circuit performance of the micromachined circuits, the Thru-Reflect-Line (TRL) calibration technique is used [6,7] with the standards and circuit components having identical feedlines. A one tier de-embedding method is implemented to establish the system reference plane along the planar transmission line [8]. As a result, all transitions between the ANA and the newly defined circuit reference plane are taken into account and the appropriate error coefficients are computed to establish an accurate calibration.

A comparison of the attenuation characteristics of the lines with integrated shielding and the membrane-supported microshield line is shown in Figure 5. Due to the absence of dielectric loss and the low radiation loss, the microshield line provides the optimum loss performance for a coplanar waveguide-type geometry. This has been proven in electro-optic sampling experiments which compared identical coplanar waveguide geometries on quartz, GaAs and a membrane. These tests demonstrated that the membrane-supported lines had significantly lower loss as the frequency increased into the submillimeter-wave region [4]. It is also evident from Figure 5 that the lines with the integrated shielding have very good loss performance. The configuration which has shielding on only the lower side performs nearly as well as the microshield line and is typical of conventional coplanar waveguide. The excess loss, in this case, results from the silicon in the lower half-space of the circuit. When the shielding is added to the upper half-space to eliminate radiation effects and provide circuit-to-circuit isolation, the attenuation is slightly increased (upper curve). This is believed to result from increased conductor loss.

Another example of the performance of circuits with integrated shielding is shown in Figure 6. This figure compares experimental and calculated results for an open-end series stub, a component which is often used for circuits such as bandpass filters and switches. The calculated results were obtained using a finite difference time domain (FDTD) analysis and show reasonably good agreement with the measured data. More importantly, the smooth characteristics of the measurements indicate that the circuit does not suffer from unwanted radiation or resonance effects.

Finally, a comparison between right-angle bends fabricated using microshield and conventional coplanar waveguide on GaAs [9] is given in Figure 7. The bend, shown in Figure 8, is a very common circuit 'element' in millimeter-wave systems, and gains significance with increasing frequency due to the parasitics which are associated with the abrupt change in the field orientation. The difference in the path lengths through the inner and outer slots, furthermore, leads to propagation of an unwanted even mode, which radiates more than the desired odd mode. The absence of a substrate in the microshield line, however, leads to a reduction in the parasitic capacitance and reduces the difference in electrical path lengths through the two slots for a fixed physical size. It has also been demonstrated that the

even and odd mode propagation velocities are much closer on a membrane-supported line than on GaAs. Therefore, in the event of even mode excitation, less signal degradation will occur with the microshield line. As shown in the figure, these advantages lead to a reflection which is at least 8 dB lower over the 10-40 GHz band.

CONCLUSION

This paper has presented two new approaches for high frequency circuit design which are based on micromachining techniques. The first approach centers on miniaturized shielding for individual circuits with the goal of high packing densities without degradation due to crosstalk. The second approach is directed at developing very high performance circuits using membrane-supported transmission lines. Realization of these concepts has been achieved and examples pertinent to high frequency applications for each approach have been shown. The measured data demonstrate the high level of performance which can be achieved.

ACKNOWLEDGEMENTS

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FIGURES

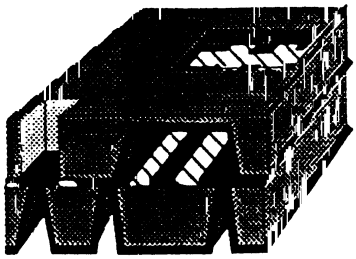


FIGURE 1. A three - dimensional cross-section of micromachined lines where the shield and line are integrated monolithically.

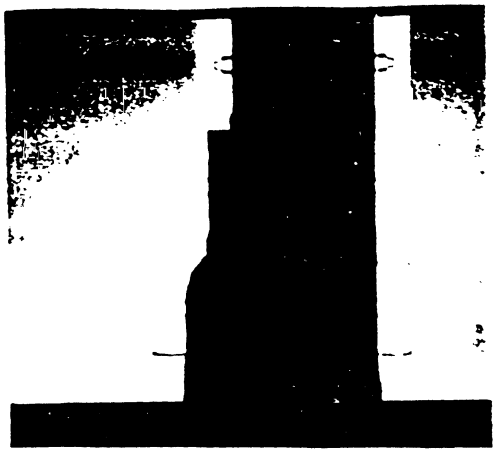


FIGURE 3. Photograph of micromachined completely shielded circuits. In this top view, the dark areas represent the upper cavity areas while open areas represent the probe windows needed for on-wafer probing.

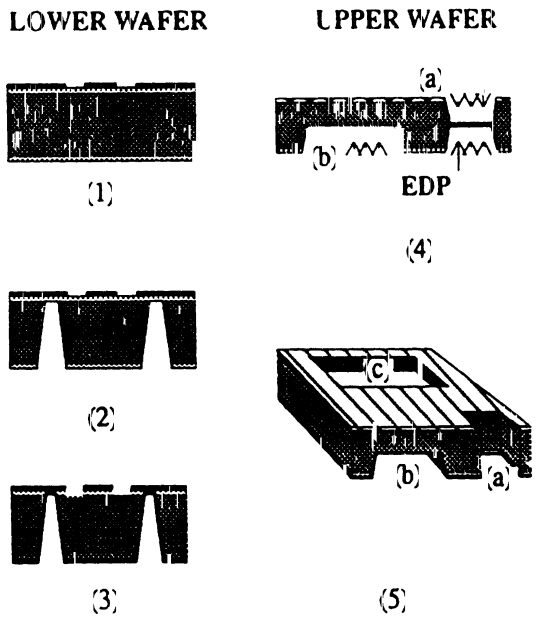


FIGURE 2. The lower wafer is developed by (1) printing transmission lines on the top surface, (2) forming lower cavities by etching v-grooves in <100> silicon using an anisotropic etchant that result in an etch angle of 54.75°, and (3) metallizing the lower cavity beneath the line. The upper wafer is developed by (4) etching probe windows and alignment marks (a) from both sides while the cavity (b) is etched from one side only; (5) the cavities are then metallized as shown in the 3-D section of the upper wafer which include the probe windows (c).

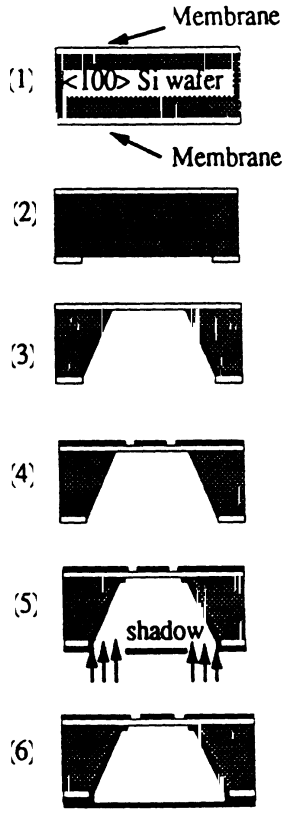


FIGURE 4. Fabrication steps of microshield line: (1) membrane wafer, (2) pattern membrane, (3) etch wafer, (4) metallize front of wafer, (5) metallize back of wafer, (6) enclose cavity.

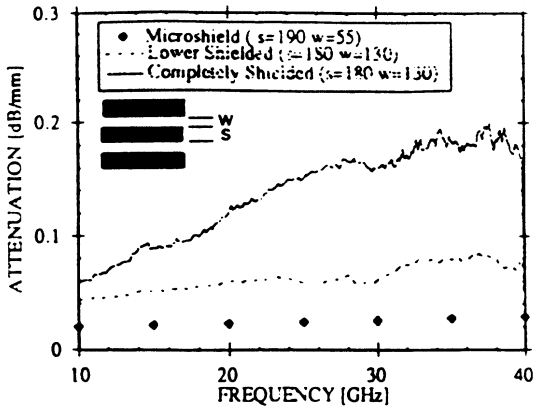
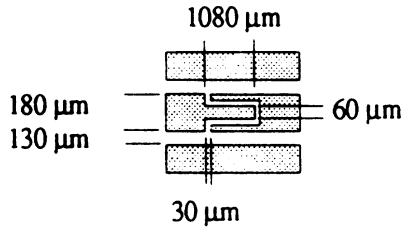


FIGURE 5. Loss performance of the microshield line compared to both shielded transmission lines. All dimensions are in microns.



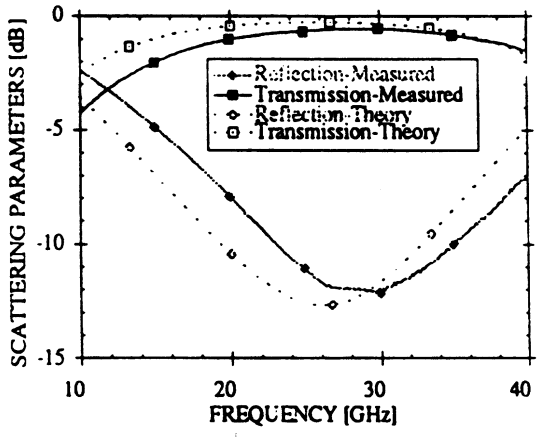
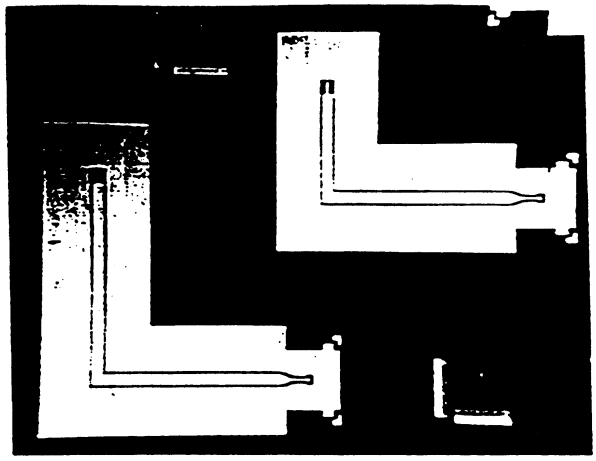


FIGURE 6. Performance of an open-end series stub for the completely shielded transmission line compared to FDTD theoretical results. All dimensions are in microns.



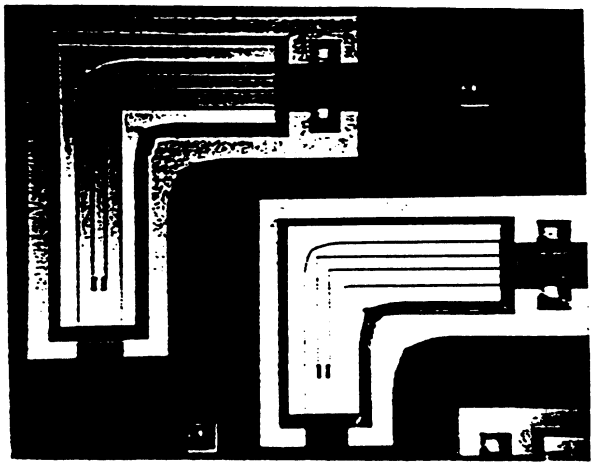


FIGURE 7. Photograph of two microshield right angle bends. The top photo shows the front side of the circuits and the lower photo shows the backside with the bottom ground planes removed. The shielding cavities shown in the lower photo are 1.6 mm wide.

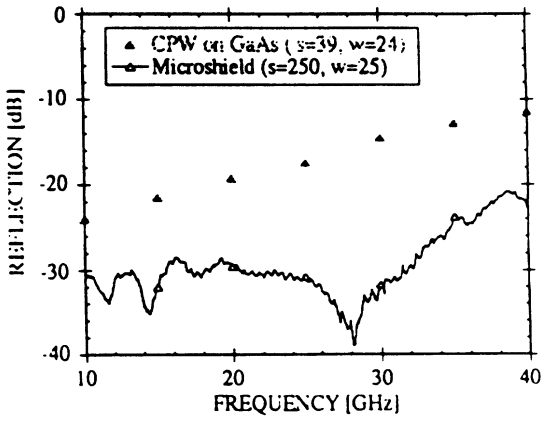


FIGURE 8. Performance of a right-angle bend on microshield and GaAs. All dimensions are in microns.

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Micromachined Self-Packaged W-Band Bandpass Filters

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Abstract

Experimental and theoretical results are presented for membrane supported W-band bandpass filters which utilize silicon micromachining technology to create self-packaged, shielded circuits. A coupled line shielded microstrip implementation of a 5-element 0.5 dB equal ripple Chebyshev filter achieves a minimum insertion loss of 3.1 dB with a 6% bandwidth centered at 94.7 GHz. The measured filter performance shows very sharp cutoff with out of band attenuation better than 25 dB and input return loss better than 8 dB. Results are also presented for a 5-element filter that achieves a minimum insertion loss of 1.4 dB with an 11.3% bandwidth centered at 94.7 GHz, and a 3-element filter with 0.6 dB insertion loss and 16.4% bandwidth at 94.9 GHz. Efforts to model filter performance using commercially available software and FDTD techniques are discussed.

1. Introduction

Planar microwave and millimeter-wave circuits take advantage of microelectronics processing technology to realize compact, low-cost, high-performance applications. As the operating frequency increases, however, planar circuits fabricated on typical silicon and gallium arsenide substrates begin to suffer from power loss through substrate modes and dispersion caused by the discontinuity in permittivity at the dielectric/air interface. At even higher frequencies, these problems become prohibitive and realization of microwave circuits such as filters and couplers becomes very difficult.

Recently, efforts have been made to reduce or eliminate these problems by utilizing silicon micromachining techniques. One method employs selective silicon etching to remove

the substrate underneath planar circuits which are then supported by thin dielectric membranes in free space [1]. This technique has resulted in a new type of transmission line called microshield line which has very low loss and nearly zero dispersion up to frequencies as high as a few terahertz [2]. Circuit components realized in microshield line have shown excellent performance compared to conventional ones [3],[4], and microshield line has shown excellent performance in planar W-Band low-pass filters [5]. In addition, silicon micromachining allows for the development of miniature self-packaged components appropriate for densely packaged microwave and millimeter-wave circuit applications [6].

In this work, we present a series of self-packaged bandpass filters which have been realized in W-Band using micromachining techniques. The filters are implemented in shielded microstrip coupled line geometries and employ dielectric membranes and micromachined shielding cavities. Measured results presented here show very high performance, low loss bandpass filters that are centered at approximately 94 GHz and have bandwidths ranging from 6% to 16.4%. The filters were designed using commercially available software and low frequency scale modeling. Finite difference time domain analysis [7] was used to verify the design and confirm the measurements.

2. Filter Design

The filters were designed for coupled line shielded microstrip implementations using the commercially available software package PARFIL [8] running on an IBM compatible PC. Filter parameters were calculated for a ground plane spacing of 100 μm and an upper shielding height of 500 μm. The designs used an internal impedance of 90 Ω and assumed an air dielectric everywhere. Three 94 GHz filters were designed using PARFIL, with two 5-element filters designed for bandwidths of 4.3% and 8.5%, and a 3-element filter designed for 12.8% bandwidth.

The filter designs were optimized by constructing a 47:1 scale model of the 4.3% bandwidth 5-element filter designed for 2.00 GHz. A 76 μm thick polyethylene film was suspended over an aluminum sheet metal ground plane, with circuit metallization patterns

defined on the polyethylene using copper tape. Measurements of the model filter on an HP 8720B 2-port network analyzer revealed a filter center frequency of 1.958 GHz, and measured bandwidth of approximately 3.5%, which agreed fairly well with the calculated performance. Through further experimental iteration, it was found that the resonator lengths required shortening by 5.3% to shift the center frequency up to the desired value. FDTD analysis at 94 GHz verified the findings of the low frequency modeling experiment.

To facilitate on-wafer probing measurements, a matching network was designed to transition from a CPW-style probe pad to microstrip. Since the filter design impedance was 90 Ω and the probing system was matched to 50 Ω, the CPW-to-microstrip transition had a dual purpose: (1) to transform the circuit impedance from 50 Ω to 90 Ω, and (2) to transfer the fields from a horizontally opposed CPW type distribution to a vertically oriented microstrip distribution. To accomplish these two tasks, a Klopfenstein taper and a microshield line geometry were chosen. The Klopfenstein taper was geometrically desirable since it promoted a gradual transfer from the CPW mode to the microstrip mode, and microshield line has been shown to support both of these modes [9].

The taper was designed using a point matching method (PMM) algorithm [10] to calculate the characteristic impedance of the microshield line for various 2-dimensional geometries. For a 220 μm constant width center conductor, it was found that varying the slot width from 10 μm to 290 μm obtained the desired range of impedances from 55 Ω to 81 Ω. These results were used to design the taper shown in figure 1 based on the method found in [11]. At the beginning of the transition, the narrow slots of the microshield line promote a high horizontal field concentration which is compatible with the wafer probe geometry. At the end of the transition, where the impedances approach the higher range, the slots of the microshield line are much wider (as wide as twice the height above the ground plane), forcing the fields to concentrate in the area between the center conductor and the lower ground plane, like a microstrip mode. At the end of the taper, the CPW upper ground planes are terminated, and the pure microstrip mode is launched.

3. Measurements

The filters were fabricated on 500 μm thick high resistivity wafers with dielectric membranes grown on both sides using anisotropic silicon etching [5] (see figure 2). Three wafers were used to create the self-packaged shielded microstrip line, and figure 3 illustrates a 2-dimensional cross-section of the assembly. Micromachining of the ground plane wafer was implemented using a two step etch process [6] which allowed the creation of windows for on-wafer probing measurements (figure 4).

The measurements were performed using an HP 8510C Vector Network Analyzer with Model 120 Picoprobe 150 μm pitch coaxial probes. A through-reflect-line (TRL) calibration was performed using the NIST de-embedding software and the following circuits: a 4 mm thru line, a 6 mm delay line, and a 2 mm offset open.

The measured response of the 5-element, 4.3% bandwidth filter is shown in figure 5. The filter achieves a minimum insertion loss of 3.1 dB and a wider than designed bandwidth of 6% at a center frequency of 94.7 GHz. The plot in figure 6 compares the measured insertion loss with that predicted by the FDTD analysis. The discrepancy in bandwidth occurs since the FDTD analysis does not consider the effect of the thin dielectric membrane. The presence of the membrane slightly increases the capacitances of the even and odd mode impedances in the coupled line sections, thereby increasing the bandwidth and the center frequency of the filter. Previous measurements of microshield line components have shown that the membrane does influence the response of membrane supported circuits [3].

PARFIL is used to include conductor loss in the filter analysis, since the FDTD code does not treat the finite conductivity of the metal. A value of 2.44×10^{-8} Ω-cm for the resistivity of gold is used, and the surface roughness is assumed negligible since the gold was evaporated. The loss tangent is taken to be zero in the air dielectric. The loss in the filter is observed to be due entirely to conductor loss, since the measured insertion loss of 3.1 dB agrees very well with the calculated value of 3.3 dB.

The measured S-parameters of two other filters are depicted in figures 7 and 8. The response plotted in figure 7 of a 5-element filter designed for 8.5% bandwidth indicates a minimum insertion loss of 1.4 dB with an 11.3% bandwidth centered at 94.7 GHz. Measurements of a 3-element, 12.8% designed bandwidth filter are shown in figure 8. This filter has a minimum insertion loss of 0.6 dB, a center frequency of 94.9 GHz, and a bandwidth of 16.4%.

4. Conclusions

We have presented high performance planar W-Band bandpass filters which are fabricated using silicon micromachining and membrane technologies and are self-packaged. The filters display excellent performance as measured on a W-Band probe station, including low passband insertion loss and high out of band signal rejection. The theoretical results match the measurements very well.

5. Acknowledgments

This work was supported by NASA. The authors wish to thank Dr. N. Dib for providing the FDTD code and Mr. G. Ponchak at NASA Lewis Research Center for his time and for the use of the W-Band network analyzer and the wafer probing apparatus.

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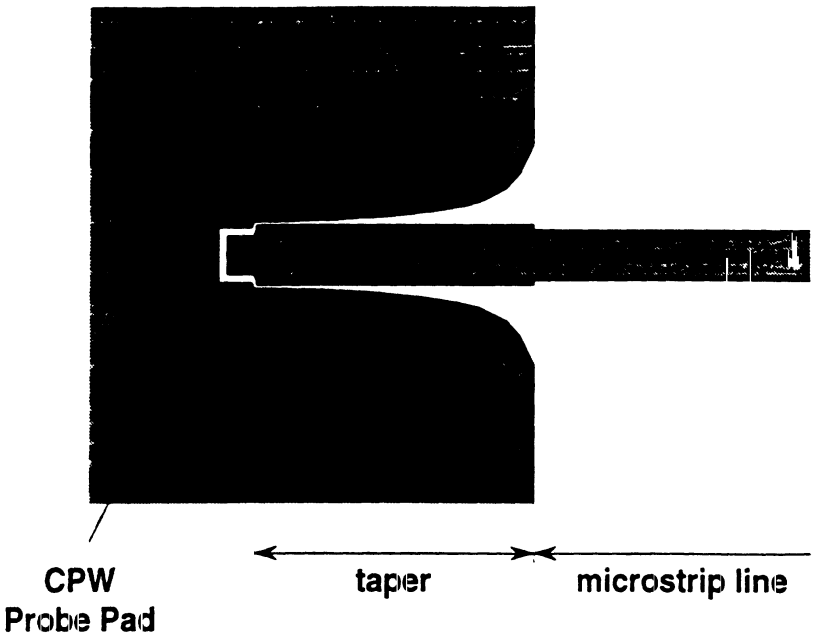

Figure 1. The Klopfenstein taper used as a CPW-to-microstrip transition.

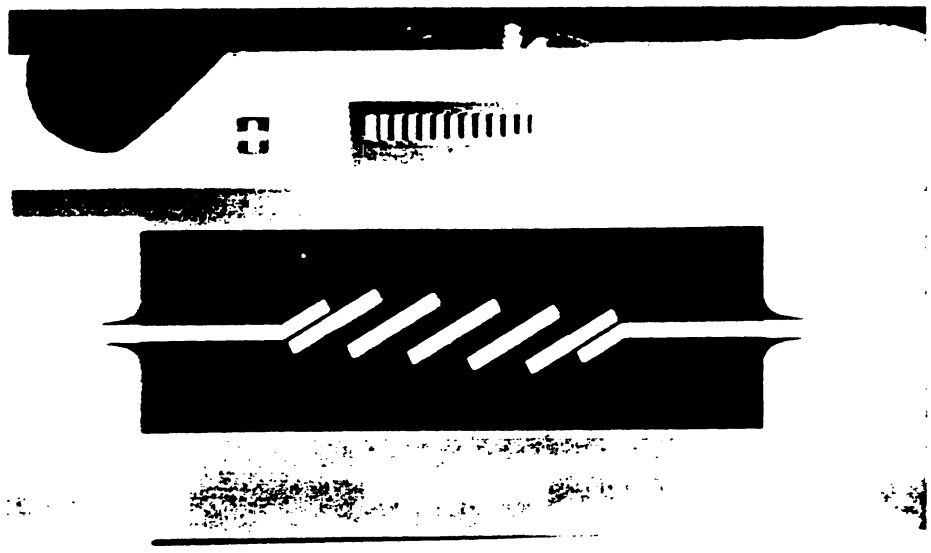

Figure 2. Photograph of the 4.3% designed bandwidth coupled line filter after selective removal of the silicon substrate. The membrane area appears darker than the surrounding silicon in the picture.

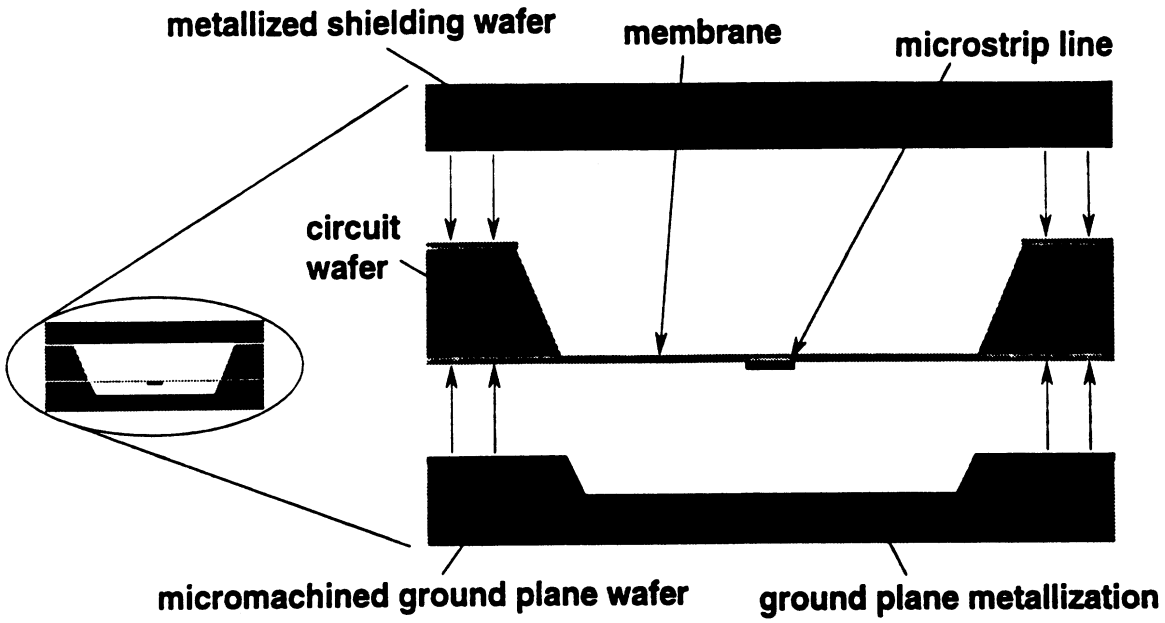

Figure 3. Two-dimensional geometry of the micromachined shielded microstrip.

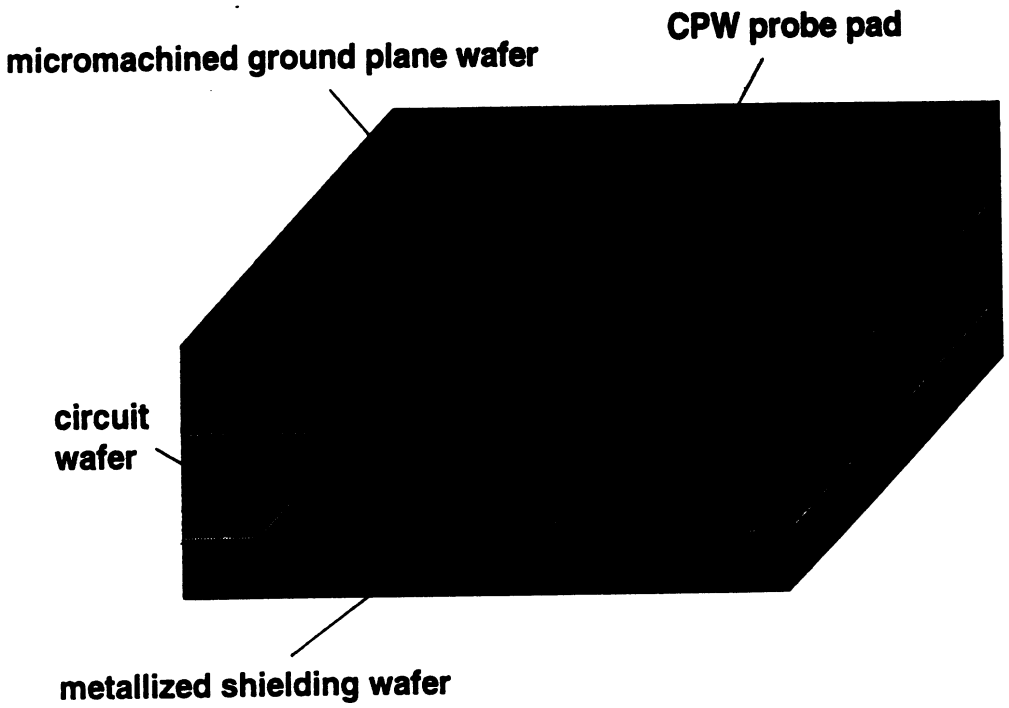

Figure 4. A 3-dimensional view of the self-packaged membrane microstrip geometry, showing the probe window and exposed CPW probe pad.

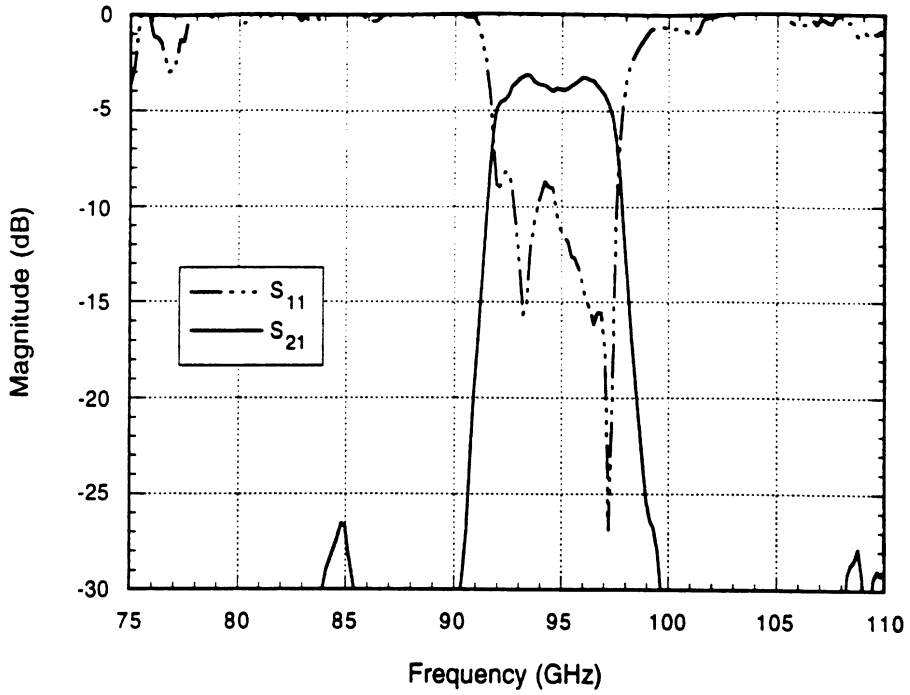

Figure 5. Measured S-parameters of a 5-element bandpass filter with 3.1 dB minimum insertion loss, 6.1% bandwidth, and 94.7 GHz center frequency.

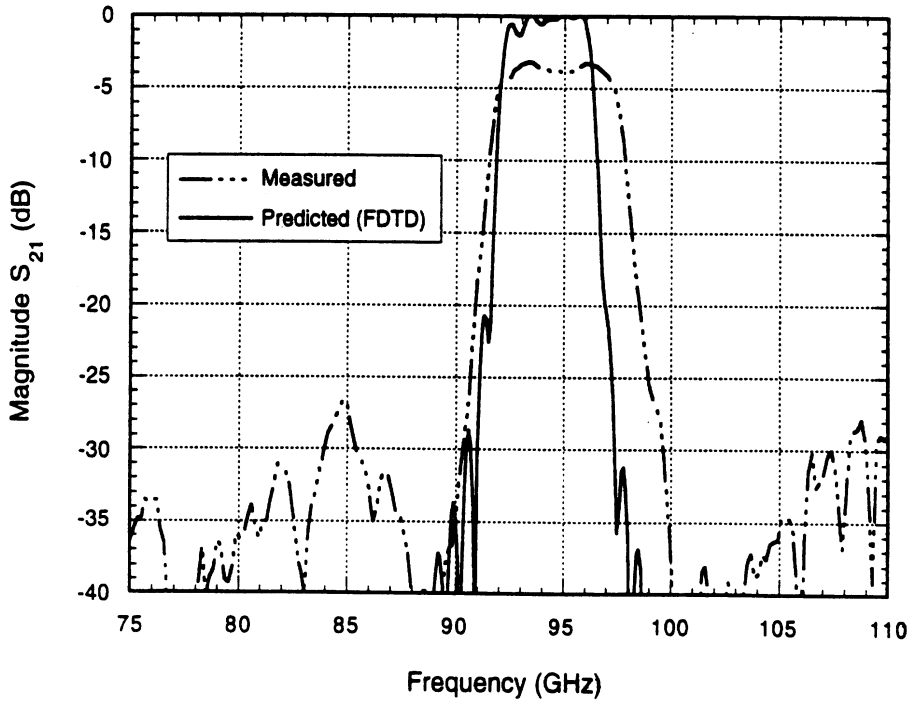

Figure 6. FDTD results compared with the measured S-parameters of a 5-element bandpass filter.

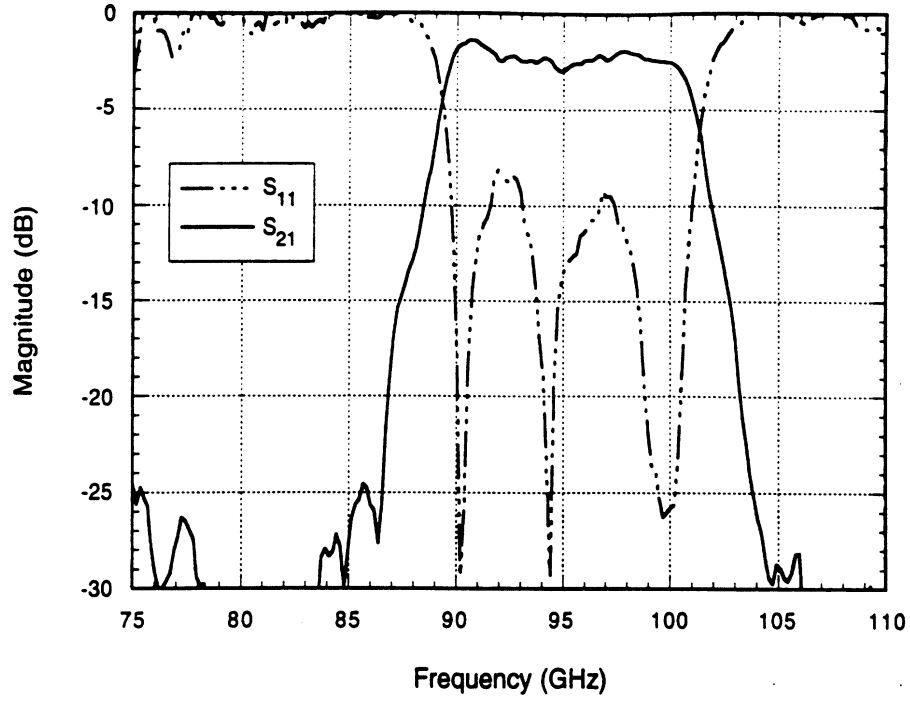

Figure 7. Measured S-parameters of a 5-element bandpass filter with 1.4 dB minimum insertion loss, 11.3% bandwidth, and 94.7 GHz center frequency.

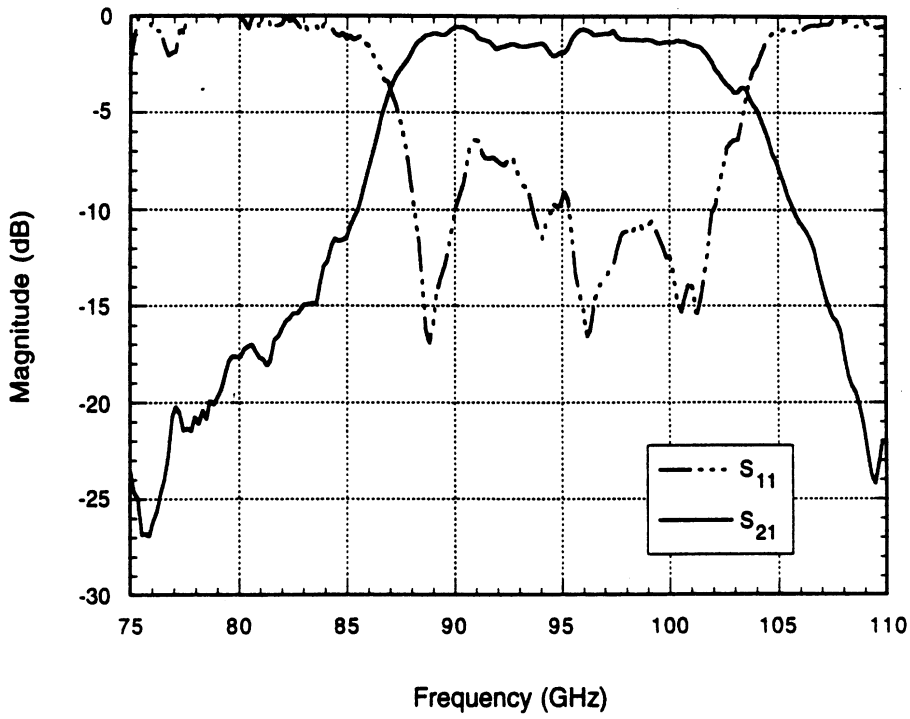

Figure 8. Measured S-parameters of a 3-element bandpass filter with 0.6 dB minimum insertion loss, 16.4% bandwidth, and 94.9 GHz center frequency.

Surface Wave Mode Reduction For Rectangular Microstrip Antennas

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I. Introduction

Rectangular microstrip antennas are being used for several years in communication systems and other applications (radars, telemetry, navigation, biomedicine), due to their advantages over conventional antennas [1]. With the recent development of micromachining techonology, there is an increased interest in incorporating patch antennas with other components fabricated with this technology. However, micromachined circuits are usually fabricated on high dielectric constant substrates, such as Silicon, and are required to operate in high frequencies. Under these conditions, the excitation of surface waves is pronounced, thus leading to lower efficiency, degradation of the antenna radiation pattern and polarization characteristics and undesired coupling between array elements. Several approaches have been proposed in order to reduce surface wave power excitation [2-3]. In [3], Jackson et al. achieved a complete elimination of the dominant TMo surface wave mode for circular patches, by use of a specific design of the antenna element. In this paper, a similar approach will be followed for the rectangular patch, in an effort to reduce significantly the TMo surface wave mode.

II. Analysis

Our purpose is to design a rectangular patch antenna operating at f=23 GHz (K-band), with a dielectric constant of $\varepsilon_r = 10.8$ and thickness of h=25 mils, with a suppressed TMo surface wave mode. Since for the given substrate, higher order modes exist at frequencies above 40 GHz, only the dominant mode needs to be eliminated.

According to the equivalence principle and the cavity model, in terms of radiation a rectangular microstrip patch can be modeled as a rectangular loop of magnetic current. From the cavity model, the electric field of the dominant TM_{10} mode for the geometry shown in Fig.1 is given by:

$$E_z = A\cos(\pi y/b) \qquad \text{(II.1)}$$

where a,b are the width and the resonant length of the patch, respectively. Here the assumption is made that the patch is fed in such a way that only the TM_{10} mode is excited. Thus, the radiating edges will be at y=0,b. The equivalent magnetic current at these two edges is: $\vec{M} = 2\vec{E}\times\hat{n} = 2A\hat{x}$ (y=0,b).

As it is known, a single Hertzian magnetic dipole, oriented in the x direction at a height z' above the ground, will give rise to a TMo surface wave field given by:

$$\Psi = K(z,z')H_1^{(2)}(\beta_{TMo}\rho)\sin\phi \qquad \text{(II.2)}$$

where β_{TMo} is the propagation constant of the TMo mode and K(z,z') is an amplitude factor that depends on the height of the source and the observation point. By integrating over the two radiating edges of the rectangular patch for the magnetic current distribution, the total surface wave field radiated by the magnetic currents takes the form:

$$\Psi = -4A\frac{B(z)}{\beta_{TMo}}H_1^{(2)}(\beta_{TMo}\rho)\tan\phi\cos(\beta_{TMo}\frac{b}{2}\sin\phi)\sin(\beta_{TMo}\frac{a}{2}\cos\phi) \qquad \text{(II.3)}$$

where $B(z) = \int_0^h K(z,z')dz'$.

In order to derive the above expression the far field approximation for the phase of the radiated surface wave is used. The pattern of (II.3) is shown in Fig. 2 (dashed line). By setting $b = \frac{\pi}{\beta_{TMo}}$ nulls are placed at the location of the peaks of the lobes at $\phi = \frac{\pi}{2}, \frac{3\pi}{2}$ so that four minor lobes replace the two major lobes (Fig. 2- solid line). As a result, the surface wave pattern is reduced.

Choosing b according to the above formula, results in greater resonant length than the one chosen for the design frequency. In order to overcome this decrease in operating frequency, the material in a rectangular region under the patch is removed (Fig. 3a,b), thus creating a lower effective dielectric constant which will permit the

desired increase in operating frequency. The length of this "cored" region is found from the transcedental equation, which is derived from the field expressions of the dominant mode of the cavity, after applying the boundary conditions at the various interfaces.

III. Results

In order to test the accuracy of this analysis, an antenna was designed according to the above procedure and was compared with a conventional patch. Simulations were run using the FDTD method [4]. Measurement of the field inside the dielectric region showed a suppressed electric field for the reduced-surface-wave (RSW) antenna, which was more than 10 db lower than the field of the conventional patch (Fig. 4). Measurement of the reflection coefficient also with the help of FDTD, showed good agreement between the resonant frequencies of the cored patch and the conventional patch.

Acknowledgements

The authors would like to thank the Office of Naval Research for the financial support of this project and Dr. Nihad I. Dib for providing the FDTD programs.

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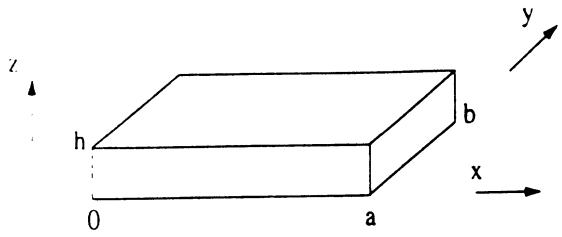

Fig. 1

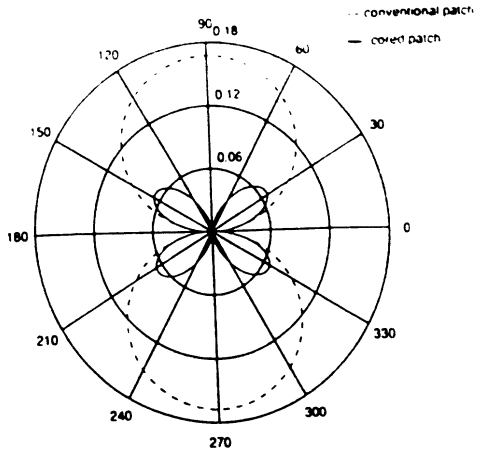

Fig.2

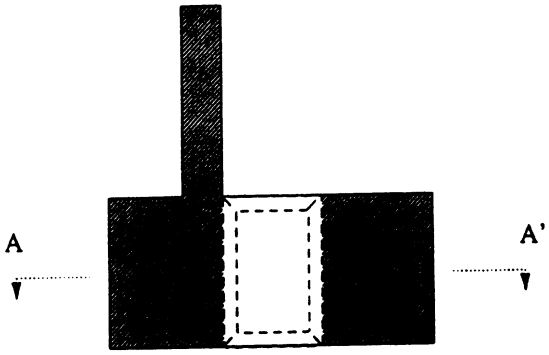

Fig. 3a

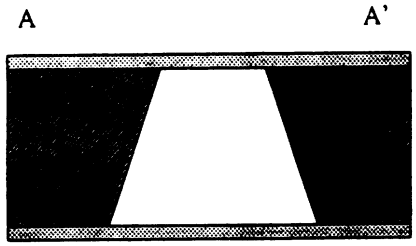

Fig. 3b

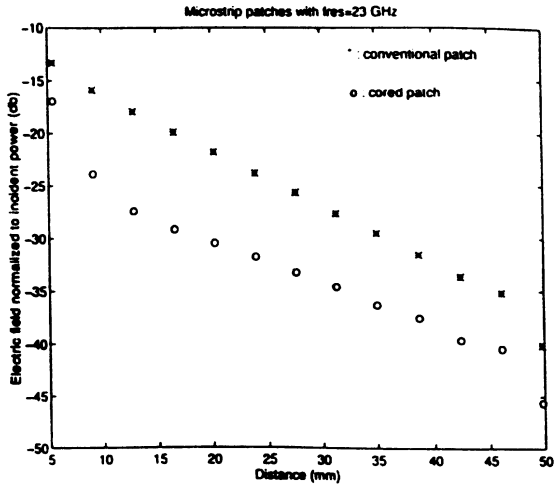

Fig. 4

Microstrip Patch Antennas on Micromachined Low-Index Materials

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Introduction

Microstrip patch antennas have been used extensively in vehicle and communication systems in the past several decades. These antennas provide low profile, low-weight, and low-cost along with easy integration into planar circuit designs and array configurations [1]. The conventional planar microstrip geometry, however, has limited bandwidth (2-5%) and poor efficiency as well as limited power capability when probe fed or microstrip fed. There are several factors which influence these parameters, the patch geometry and medium directly, and feeding structure indirectly.

The patch antenna is primarily influenced by the dielectric constant and thickness of the substrate material. With this in mind, the highest bandwidth will be observed in designs implemented on thick, low index materials [2]. The efficiency of the antenna is affected primarily by the excitation of substrate modes. While these modes are inherently excited in the substrate and for that reason cannot be eliminated entirely, reduction will result in improved performance since the energy lost to these modes will now be available as useful power [3]. Surface waves in low index materials are lower than those excited in high index ones thereby making them the preferred medium.

Currently, designs are often implemented on low index materials for high patch efficiency, and wide bandwidth which can be increased further using wideband impedance matching networks and or aperture coupling methods [2]. In contrast, circuit application requirements for high density and compactness are best achieved on thin high index materials. As mentioned above however, these can have adverse effects on the patch performance. Since patch antennas are relatively simple to implement in many applications, it is important to address the requirements of both the antenna and feeding structures. In the past certain design tradeoffs were acceptable due to technology limitations. However, with the aid of new emerging technologies and the vast knowledge of the patch antenna behavior, these issues can now be addressed effectively. A variety of approaches have been proposed [4] for improved antenna efficiency where material underneath the patch is modified to alter its electrical properties.

Herein, an alternative approach is proposed which allows for easy implementation using micromachining. The goal of this approach is to develop an "effective" low index material underneath the antenna while the feeding circuit is kept on the high index one. The design of a conventional patch antenna fed by a microstrip is developed using micromachining techniques to decrease the height of the high index material underneath the patch while the material under the feedline remains unaltered. This approach reduces the value of the effective dielectric constant only in the area under the antenna, since it is comprised of a mixed dielectric medium of high index material and air.

Design/Fabrication Approach

The patch geometry was initially designed using PCAAD CAD tool [5] for resonances at 20 GHz. This CAD tool is based on the uses a cavity model which determines the antenna resonant length (1/2 guided wavelength) and width for a given substrate material and thickness. Since a center probe fed excitation is assumed in PCAAD, for a planar configuration, an inset microstrip is used to match the antenna to the given feedline impedance. This design is implemented to provide a symmetric antenna design.

The objective of this work is to explore the implementation of planar designs on localized low index materials. Initial investigation is implemented at 1.07 GHz on stycast, having ε_r=12, with thickness of 6.6 mm. These are chosen to simulate the response of a patch on silicon substrate of thickness 350 microns at desired operating frequency of 20 GHz. Since the actual circuit will be used in a planar configuration with horizontal feeding structure, the microwave model is excited by using a coaxial probe to feed a inset microstrip feed line. The geometry is shown in Fig.1 where the feed line is located on 100% material while the patch is located on 50-50 percent stycast - air dielectric material. When two pieces are brought into contact, the air region runs directly underneath the patch antenna and extends horizontally into the substrate material as shown in the lower geometry of Fig.1 dashed lines.

At the desired operating frequency, the design is implemented using micromachining etching processes to chemically remove the material from underneath the patch. A detailed description of this procedure is described in [6]. An additional wafer is mounted underneath to enclose the cavity below the patch and provide the microstrip ground plane. The circuit wafer consists of high resistivity silicon with ε_r = 11.7 and thickness of 350 microns while the ground plane wafer can be a low resistivity material. The microstrip feed in this arrangement is excited through a coplanar waveguide transition.

Results and Conclusions

In Fig.2, a comparison is shown between the microwave model and the theoretical results for the return loss of the patch. The theoretical results are based on finite difference time-domain method for the microstrip inset fed antenna. The FDTD [7]

results presented correspond to a patch design with a silicon substrate and are compared to the modeled results on the stycast material. The measured and theoretical results have similar shape although there is a 100 MHz difference in the resonant response. This resonance shift can be improved by implementing a finer mesh in the direction normal to the cavity where the 50-50 material-air interface lies.

The above design will be implemented next on silicon using micromachining techniques. The presentation will describe the fabrication and measurement procedures utilized and will present measured and theoretical results on the performance of the micromachined antenna. This design offers the advantage of reducing the effects of surface wave excitation which can result in improved bandwidth and antenna efficiency.

Acknowledgments

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Figures

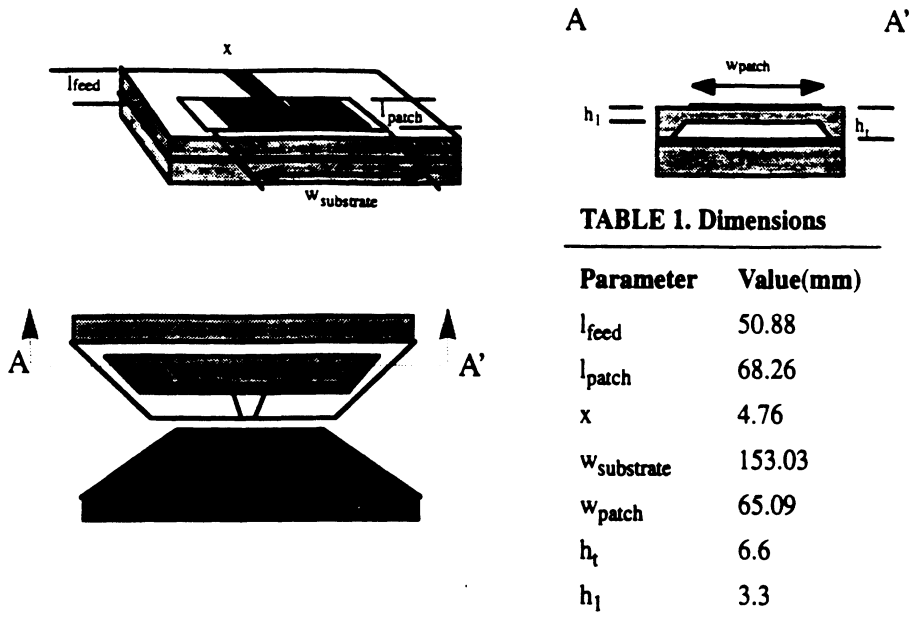

TABLE 1. Dimensions

Parameter	Value(mm)
l_{feed}	50.88
l_{patch}	68.26
x	4.76
$w_{substrate}$	153.03
w_{patch}	65.09
h_t	6.6
h_1	3.3

Figure 1. Micromachined patch antenna with effective low index material.

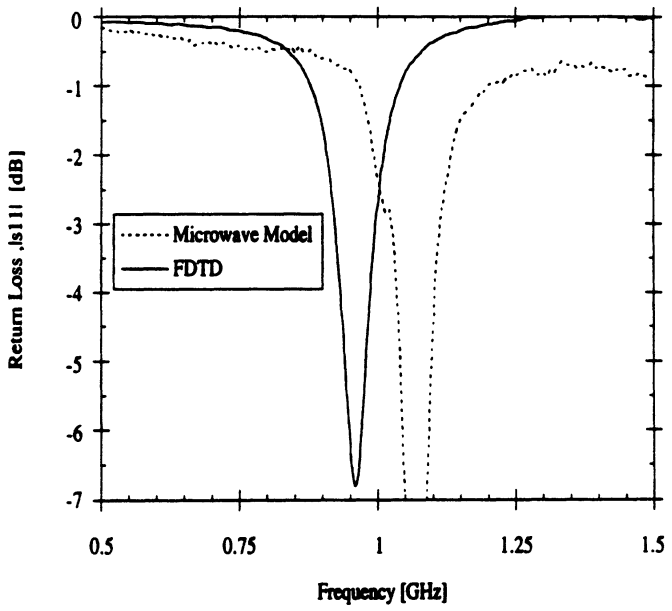

Figure 2. Measured and theoretical results of a microwave model on stycast material.