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SUBSTRATE RESPONSE OF A FLOATING GATE *n*-CHANNEL MOS MEMORY CELL SUBJECT TO A POSITIVE LINEAR RAMP VOLTAGE

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Abstract—A computer simulated substrate response of an *n*-channel MOS floating gate transistor to a positive linear ramping gate voltage was investigated. Device parameters, such as the channel length, effective electron mobility, substrate doping level and the gate voltage ramping rate were changed to see their effects on the substrate response. The substrate response was monitored by using the response of the surface potential at the mid-channel point. In the one-dimensional analysis it was found that the surface potential at the mid-channel point increased initially and dropped quickly after passing through its peak value and then decreased slowly. The mid-channel surface potential reached a higher peak value if the device had (1) a longer channel length, (2) a lower effective electron mobility, (3) a higher gate voltage ramping rate, or (4) a lower substrate doping level. Solutions show that the conditions for the mid-channel point to reach its peak surface potential faster are: (a) a shorter channel length, (b) a higher effective electron mobility, (c) a higher gate voltage ramping rate, and (d) a lower substrate doping level.

INTRODUCTION

In a floating gate MOS memory transistor, the memory state of the transistor ("on" or "off") is determined by the sign and the quantity of the charge stored at the floating gate. Figure 1(a) shows the cross-sectional view of an *n*-channel floating gate device. Both the floating gate and the upper gate of the device are n^+ doped polycrystalline silicon layers. The insulator on top of and underneath the floating gate is silicon dioxide thermally grown from the polycrystalline silicon floating gate and from the single crystal silicon substrate, respectively. To distinguish these two oxides, they are named poly-oxide and wafer oxide in Fig. 1(a). Charges can be injected from the substrate to the floating gate by avalanche injection[1, 2], tunneling through a thin layer of wafer oxide[3], or channel conduction injection[4]. Instead of injection from the substrate, charges can be put on the floating gate from the upper gate through the poly-oxide via tunneling[5, 6]. When tunneling is used, the electric field across the tunneled oxide is the dominant factor in determining the floating gate charging rate. In order to calculate the electric field existing in the tunneled oxide, the substrate voltage distribution function is needed. This need comes about because the substrate can drop an appreciable amount of the applied gate voltage across the space charge layer at the substrate surface, expecially when the gate voltage has a very short pulse width.

In practice the applied voltage is usually a pulse which does not jump from an initial value to the final value instantaneously. In the following analysis, we assume that the voltage increases linearly from the initial value

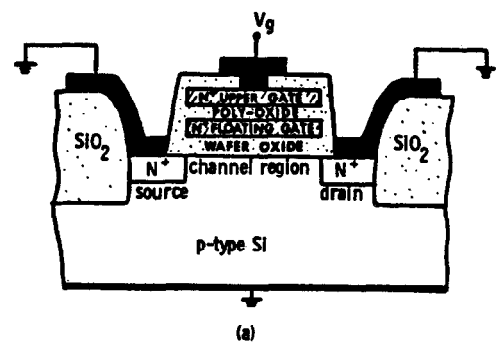

Fig. 1(a). The cross-sectional view of a floating gate MOS memory cell.

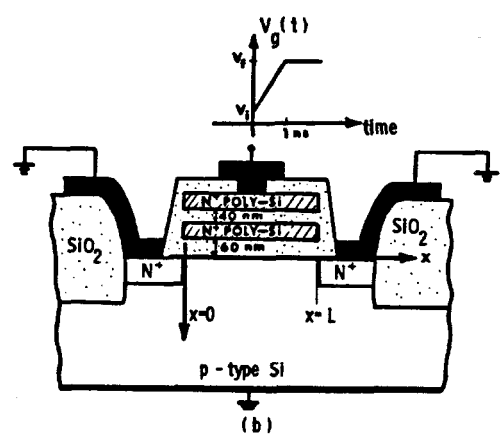

Fig. 1(b). The bias condition, coordinate system, oxide thicknesses and the applied gate voltage of a device.

to the final value with a rise time on the order of one nanosecond and then stays at the final value until turn-off.

Consider the application of a negative voltage to the upper gate of a device with a p-type substrate. Holes, the majority carriers in the substrate will accumulate at the substrate surface with a time constant ϵ_s/σ, where ϵ_s is the permittivity of the silicon and σ is the conductivity of the substrate. For a 1 Ω-cm p-type substrate, the time constant is on the order of 10^{-12} sec. In other words, the substrate response to the negative applied voltage contributes negligible delay in comparison with the gate voltage rise time (10^{-9} sec). If a positive gate voltage is applied, holes under the gate (i.e. the channel region) will be pushed out of the substrate surface leaving a space charge of negatively charged acceptors behind. This positive voltage will form a potential well for electrons and cause electrons to drift from the source and the drain regions into the channel region. Thermal generation of electron-hole pairs in the space charge region will assist the establishment of quasi-equilibrium; however, the time constant for this process is on the order of one microsecond and is much slower than charge injection from source and drain contacts. Thermal generation is, therefore, neglected in our analysis. Since the space charge response to the changing gate voltage is a non-steady state condition, its width is greater than the quasi-equilibrium value. Therefore, a sizable fraction of the gate voltage will drop across this region. If the source, drain, and substrate are all connected together as shown in Fig. 1(b), there will be a transient electron drift until the surface potential of the substrate along the channel becomes uniform. The surface potential is the potential measured from the silicon side of the Si–SiO_2 (wafer oxide) interface to the grounded substrate contact. It takes time for electrons to drift from the source and drain regions and form an electron layer within the channel region. In other words, there will be a delay in forming a conducting channel even when the gate voltage exceeds the turn-on voltage of the device. The delay time will depend on the channel length of the device, the effective electron mobility along the channel, the substrate doping level, the bias condition of the source and the drain and the ramping rate of the gate voltage.

Zahn[7] and Burns[8] investigated the delay time of a MOS transistor. In comparison with their device structure, the floating gate constitutes an additional equipotential plane inserted between the upper gate and the substrate, making the analysis of the transient response more complicated.

Since the n-channel floating gate memory cell can respond to the negative applied gate voltage very quickly, only the positive gate voltage case will be discussed in the following sections. In this report we concentrate on the surface potential of the channel region during and immediately following the ramping period. We use 1 nsec as the ramping period throughout the report. The time scale dealt with will be no longer than 1.2 nsec after the gate voltage has started to ramp up.

FORMULA DERIVATIONS

As shown in Fig. 1(b), a simple one-dimensional model is used in this analysis where the x-axis is along the channel direction. The oxide thicknesses used in these calculations and the shape of a typical applied gate voltage are also shown.

To derive the equations, the following assumptions will be used:

(1) there exists an effective electron mobility in the channel region which is independent of the driving electric fields; (2) source and drain regions are the only electron reservoirs; (3) substrate doping is uniform.

Without losing the physical characteristics of the substrate response, we also use the following simplifying assumptions: (4) initially, there is no trapped charge in the oxides and no net charge at the floating gate; (5) the flat band voltage of the device is zero and (6) the parasitic capacitance of the device is small and can be neglected.

In the channel region, the surface potential, ψ, and the applied gate voltage, $V_g(t)$, are coupled through the following equations,

(a) charge conservation equation[9, 10]

$$C_1(V_{fg}-\psi)=qn+[2q\epsilon_s N_A(\psi-kT/q)]^{1/2} \tag{1}$$

(b) continuity equation[9, 10]

$$q\frac{\partial n}{\partial t}=\frac{\partial}{\partial x}\left(qn\mu_n E+qD_n\frac{\partial n}{\partial x}\right) \tag{2}$$

where C_1, wafer oxide capacitance per unit area (F/cm^2); V_{fg}, floating gate potential (V); ψ, surface potential of the substrate (V); q, electron charge (1.6×10^{-19}C); n, electron density in the substrate (cm^{-2}); N_A, substrate doping density (cm^{-3}); k, Boltzmann's constant (1.38×10^{-23} J/K); T, absolute temperature of the device (K); t, time (s); μ_n, effective electron mobility along the channel (cm^2/Vsec); E, electric field at the channel region (V/cm); D_n, electron diffusivity at the channel region (cm^2/sec).

The first term of the r.h.s. of eqn (1) is the electron charge per unit area and the second term is the ionized acceptor charge per unit area. On the r.h.s. of eqn (2), the second term in the parenthesis is the diffusion component which is much smaller than the electric field drift component. Hence, we use the Einstein relation to replace the diffusivity D_n by $(kT\mu_n/q)$ even though μ_n is the effective mobility.

Combining eqns (1) and (2), we have

$$\frac{\partial n}{\partial t}=\frac{\partial}{\partial x}\left(D^*\frac{\partial n}{\partial x}\right) \tag{3}$$

where

$$D^*=\frac{qn\mu_n}{C_1}\left\{1-\left[\frac{q\epsilon_s N_A}{2C_1^2\left(V_{fg}-\frac{kT}{q}-\frac{q}{C_1}\right)+q\epsilon_s N_A}\right]^{1/2}\right\}+\frac{kT}{q}\mu_n.$$

In writing eqn (3), the relation $E=-(\partial\psi/\partial x)$ has been

used. The term V_{fg} is related to the gate voltage by the expression:

$$V_{fg} = V_g - \frac{q}{LC_2}\int_0^L \left[n + \sqrt{\left(\frac{2\epsilon_s N_A}{q}\left(\psi - \frac{kT}{q}\right)\right)}\right] dx \tag{4}$$

where

$$V_g = \begin{cases} V_i & t < 0 \\ V_i + (V_f - V_i)t/\tau & 0 < t \le \tau \\ V_f & t > \tau \end{cases} \tag{5}$$

V_i, initial gate voltage (V); V_f, final gate voltage (V); τ, gate voltage ramping period (s), C_2, poly-oxide capacitance per unit area (F/cm^2); L, channel length (cm).

The integral in eqn (4) represents the total charge in the upper gate, which, by charge conservation, equals the total charge induced in the substrate. The upper gate charge divided by the poly-oxide capacitance is just the voltage drop across the poly-oxide.

There are two boundary conditions for eqn (3). The first one is

$$\left.\frac{\partial n}{\partial x}\right|_{x=L/2} = 0. \tag{6}$$

This condition is due to the structure and the bias condition of the device being symmetric in the x direction. The second boundary condition describes the electron concentration at $x = 0$. To make this condition manageable, we assume that the electrons at $x = 0$ can respond to the applied gate voltage and reach their quasi-equilibrium values instantaneously. The argument for this assumption is that the separation between $x = 0$ and the electron reservoir (the source region) is so small that electrons can reach the quasi-equilibrium condition in a time much shorter than the time scale we will deal with. Using Boltzmann's statistics, the relationship between the floating gate voltage and the surface potential at $x = 0$ can be written as

$$C_1(V_{fg} - \psi_0) = \frac{2\epsilon_s q N_A}{\beta}\left[(e^{-\beta\psi_0} + \beta\psi_0 - 1) + \left(\frac{N_i}{N_A}\right)^2 (e^{\beta\psi_0} - \beta\psi_0 - 1)\right]^{1/2} \tag{7}$$

where ψ_0, surface potential at $x = 0$; $\beta = (q/kT)$; N_i, intrinsic carrier density of silicon (cm^{-3}).

The electron density can be evaluated by using eqns (7) and (1). Another method for calculating the electron density at $x = 0$ is to integrate the conduction band electron concentration from the substrate to the Si–SiO$_2$ interface. To do that, the knowledge of the electron distribution perpendicular to the channel direction is needed. The calculated electron density difference between these two methods is very small[10]. The difference decreases exponentially as the surface potential increases. In this report, we use 0.304, 0.404 and 0.495 V as the minimum surface potential for 10^{15}, 10^{16} and 10^{17} cm^{-3} substrate doping materials, respectively. In doing this, the error introduced by using eqns (7) and (1) to calculate the boundary condition at $x = 0$ is less than 5%[10].

Since a minimum surface potential requirement has been imposed in eqn (7), the applied gate voltage is forced to have a larger than zero initial voltage.

The initial condition of the device is that the surface potential and the electron concentration are uniform along the entire channel. This initial condition is equivalent to assuming that the cell was at the initial gate voltage for sufficient time such that the entire channel is in quasi-equilibrium with the initial gate voltage before the beginning of the gate voltage ramp.

We have the nonlinear differential equation, eqn (3), two boundary conditions, eqns (6) and (7), and the initial conditions of the surface potential. Equation (3), however, is written in terms of the internal floating gate potential. The floating gate potential is coupled to the external gate voltage through eqn (4). The two step solution algorithm used was (1) to estimate a value of floating gate voltage and solve eqn (3) to obtain the surface potential $\psi(x, t)$, and (2) to use the value of $\psi(x, t)$ in eqns (1) and (4) to obtain an improved value of the floating gate potential. Convergence of the iterative procedure was defined when the difference in successive floating gate potentials was less than 10^{-6} V.

SIMULATION RESULTS

The surface potential, $\psi(x, t)$, is an important parameter in determining the channel region response to an applied gate voltage. Since electrons are supplied from the source and drain regions, the last place the electron concentration can reach its quasi-equilibrium value will be at the mid-channel point. In the following, the value of the mid-channel point surface potential $\psi((L/2), t)$ will be used to monitor the channel region response of the device.

Figure 2 shows the surface potential change with respect to time when the applied gate voltage ramps from 1.461 to 40 V in 1 nsec and then remains at 40 V. The parameters of the device are: channel length = 6 μm, substrate doping level = 10^{16} cm^{-3}, the effective elec-

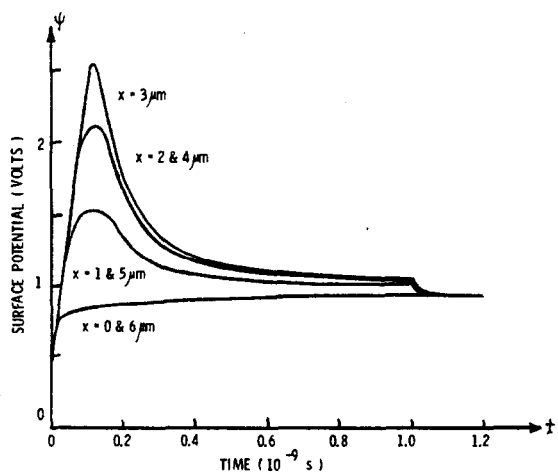

Fig. 2. The surface potential variation vs time at different channel positions.

tron mobility = 400 cm²/Vsec, wafer oxide thickness = 60 nm and the poly-oxide thickness = 40 nm. The maximum surface potential found in Fig. 2 is 2.6 V. Since the substrate is grounded, this peak surface potential can produce a maximum depletion layer field of 4.46×10^4 V/cm perpendicular to the channel direction. This field is much smaller than the electric field (5.3×10^5 V/cm) needed to cause the avalanche multiplication of electrons in the depletion region[11]. The maximum electric field along the channel direction is found to be 6.7×10^3 V/cm which is smaller than the maximum field perpendicular to the channel direction. Therefore, the applied gate voltage cannot cause avalanche multiplication in the channel region.

Figure 2 shows that the surface potential at positions not too close to the source and drain regions increase to peak values and then decrease. This decrease is very fast after passing the peak value and then slows down even though the applied gate voltage is still increasing at the same rate. The shape of Fig. 2 can be explained as follows: initially, the applied gate voltage is small and so is the electron concentration. The initial increase in the gate voltage forms a deep depletion layer and results in an increase of the surface potential with time. While the surface potential is building up with time, the electron concentration at the positions $x = 0$ and $x = L$ are also increasing due to the increase of the gate voltage. The two factors (1) deeper potential well, and (2) many available electrons, result in a rapid flow of electrons into the channel and a fast decrease of the surface potential. This corresponds to the response shown in Fig. 2 just after the peak value has been reached. After filling the potential well with electrons, the electron driving force, i.e. the gradient of the potential well, decreases drastically. This causes the electrons to move into the channel at a slower rate than before but still fast enough to fill the potential well more rapidly than the applied gate voltage can create it. Therefore the surface potential decreases slowly as shown at the tail of the curve in Fig. 2 before $t = 1$ nsec.

The peak surface potential value corresponds to the time at which the depletion width is at its maximum. This can be shown by writing the surface potential in terms of the depletion width W[9]

$$\psi = \frac{qN_A}{2\epsilon_s} W^2. \tag{8}$$

The electron contribution to the surface potential was neglected in eqn (8) since the electrons form only a shallow sheet at the substrate surface. At the peak value of the surface potential, $(\partial\psi/\partial t) = 0$ implies $(\partial W/\partial t) = 0$. So that W has also reached its maximum value. At that moment there will be no change in the substrate ion charge. Any change of charge in the substrate will come from electrons. In other words, when the surface potential reaches its peak value, the rate change of the induced negative charge in substrate caused by the gate voltage will be equal to the rate change of the electrons. This is expressed analytically as

$$C_1 \frac{\partial}{\partial t}(V_{fg} - \psi) = q \frac{\partial n}{\partial t}. \tag{9}$$

Since $(\partial\psi/\partial t) = 0$ at the moment,

$$\frac{C_1}{q} \frac{\partial V_{fg}}{\partial t} = \frac{\partial n}{\partial t}, \tag{10}$$

which says that the rate change of the floating gate voltage is solely determined by the rate change of the electrons.

The surface potential at $x = 0$ (and $x = L$) shows a different result from the other curves in Fig. 2. It increases with the increasing of the gate voltage. This is as expected since we assume that, at these two points, the substrate response can follow the gate voltage change and reach their quasi-equilibrium conditions instantaneously.

With the same device parameters and applied gate voltage as used in Fig. 2, Fig. 3 shows the electron concentration variation along the channel at different times. Figure 4 shows the change of the floating gate voltage with time and the ratio of the floating gate voltage to the applied gate voltage. As to the electric field across the oxides, Fig. 5 shows the results of the field across the poly-oxide, E_2, the minimum wafer oxide field (at $x = (L/2)$) and the maximum wafer oxide field (at $x = 0$ and $x = L$). In calculating the values of the oxide fields E_1 (in wafer oxide) and E_2 (in poly-oxide), we assume that the floating gate collects a negligible amount of charge during the ramping period. This can be justified by calculating

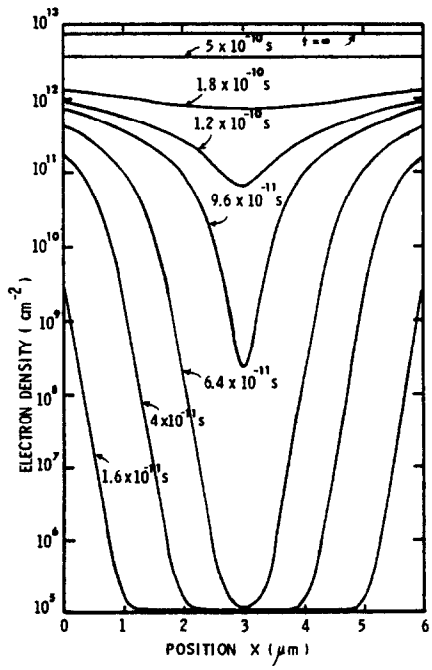

Fig. 3. The substrate electron density along the surface channel at different times.

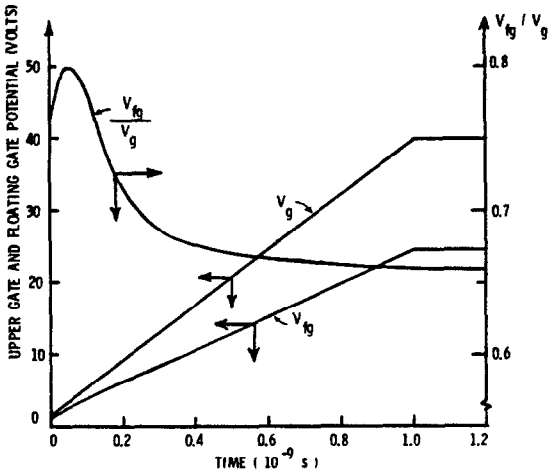

Fig. 4. The floating gate potential, the applied gate voltage, and the ratio of the two voltages vs time.

the divergence of the oxide currents at the floating gate. As shown in Fig. 5, the maximum oxide field in wafer oxide and poly-oxide in the ramping period (1 nsec) is less than negligible current flow in the wafer oxide [6, 12] and less than 1 A/cm^2 in poly-oxide [6, 13–16]. The charge flow through the poly-oxide in the ramping period (1 nsec) is less than 10^{-9} C/cm^2. Hence the change of charge at floating gate is less than 10^{-9} C/cm^2. By Gauss' law, 10^{-9} C/cm^2 produces an electric field of 3×10^3 V/cm in our one-dimensional analysis. This electric field is much smaller than the 10^6 V/cm produced by the external gate voltage. Therefore, the assumption used in obtaining Fig. 5 (that we can neglect the field produced by the floating gate charge) is valid.

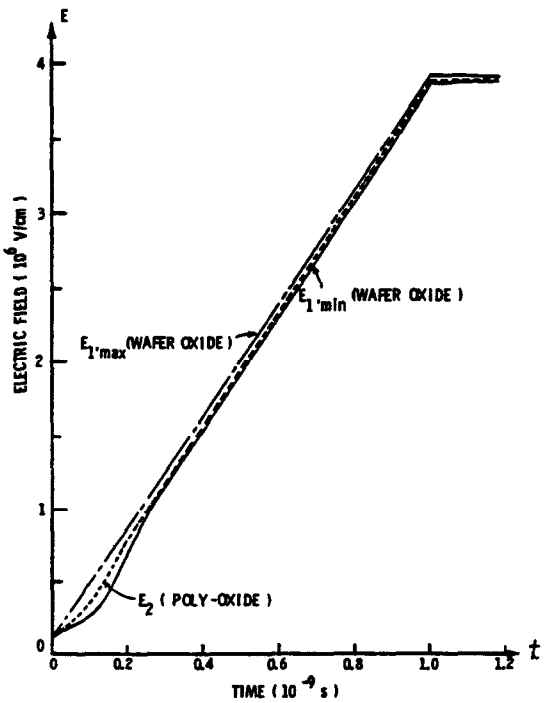

Fig. 5. The oxide field variation vs time.

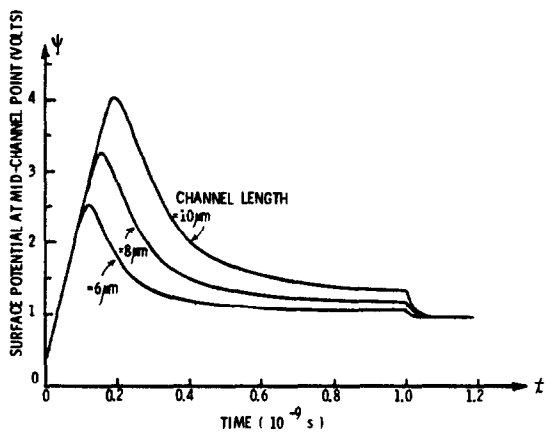

Fig. 6. The variation of surface potential (at $x = (L/2)$) vs time with channel length as a parameter.

For devices having different channel lengths, the mid-channel surface potential variation with respect to time is shown in Fig. 6. Allowing only the channel length to vary, all other factors, such as the device parameters and applied gate voltage, are the same as used in Fig. 2. For longer channel length devices, it takes a longer time for electrons to drift to the midchannel point and balance the induced substrate charges there. Therefore, a long channel device can build higher peak surface potentials compared to a short channel device.

For different effective electron mibilities, Fig. 7 shows the mid-channel point surface potential variation. Again, the parameters used are the same as in Fig. 2 except for the effective electron mobility. In terms of reaching the peak surface potential, increasing effective electron mobility has a similar effect as reducing the channel length. Devices having a higher effective electron mobility need less time to reach the peak potential at the mid-channel point and exhibit a lower peak surface potential there.

Figure 8 shows the surface potential time response at the mid-channel point with different gate ramping rates.

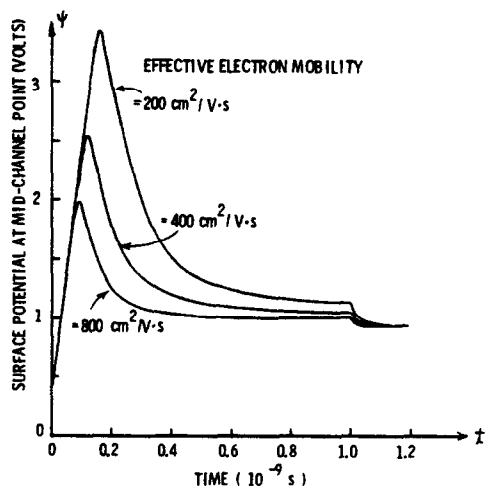

Fig. 7. The variation of surface potential (at $x = (L/2)$) vs time with effective electron mobility as a parameter.

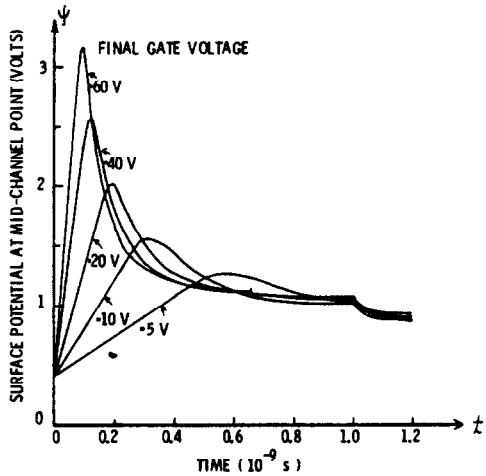

Fig. 8. The variation of surface potential (at $x = (L/2)$) vs time with final gate voltage as a parameter.

Except for the final gate voltages marked on each curve, all other parameters are the same as used in Fig. 2. To satisfy the assumption that we can neglect the oxide charge and the floating gate charge during the ramping period, the maximum gate voltage used in Fig. 8 is 40 V. Figure 8 shows that the higher the ramp rate (corresponding to the higher final gate voltage), results in less time needed for the mid-channel point to reach its peak value. This is due to the higher voltage ramp rate creating a steeper potential well than a slower ramp rate, so that the field-aided electrons pour into this steeper well more quickly. But a high gate voltage ramp rate enhances the rate of increase of the surface potential. This is because a high ramp rate produces a higher gate voltage than a slower ramp does at a given time. We have higher peak surface potentials for higher gate voltage ramp rates even though it takes a shorter time to reach the peak value.

For substrate doping level variations the time response of the mid-channel surface potential is shown in Fig. 9.

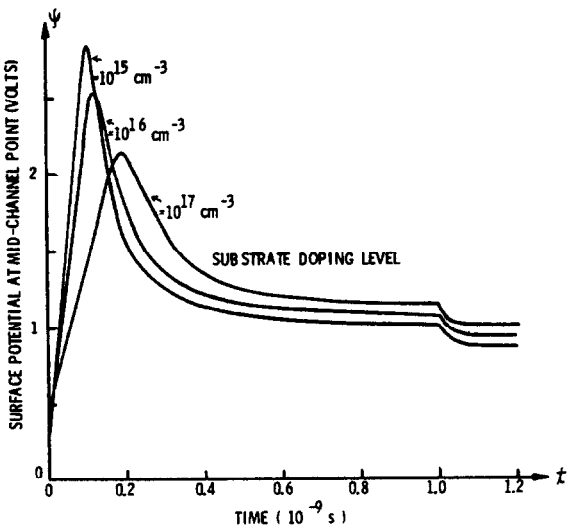

Fig. 9. The variation of surface potential (at $x = L/2$)) vs time with substrate doping level as a parameter.

All parameters except the doping level and the initial gate voltage are the same as used in Fig. 2. Since we use eqn (7) to evaluate the boundary condition at $x = 0$ and limit the error to less than 5%, the initial voltages for different doping levels are not the same. We have V_i = 0.592, 1.461 and 4.221 V for substrate doping 10^{15}, 10^{16} and 10^{17} cm^{-3}, respectively. Results show that the lower substrate doping has higher peak surface potential and needs less time to reach the peak value than the higher doping device does.

DISCUSSION

In eqn (2) we assumed that the drift velocity v can be expressed by

$$v = \mu_n E \tag{11}$$

where μ_n is a constant mobility not dependent on the magnitude of the electric field E. Since an electron does not move faster than its scattering-limit velocity v_{sl} (10^7 cm/sec in silicon) we should not have electric fields higher than (v_{sl}/μ_n) in our simulation. Otherwise, we underestimate both the time needed for the surface potential to reach its peak value and the magnitude of the peak surface potential. For the parameters used in Fig. 7, the maximum drift fields found were 9.7×10^3, 6.7×10^3 and 4.5×10^3 V/cm when the effective electron mobility had values of 200, 400 and 800 cm^2/Vsec, respectively. Therefore, the maximum electron drift velocity at the conditions used in our simulation was less than the scattering-limit velocity.

The second assumption used in previous sections was that the source and drain regions are the only electron sources in the device. We already mentioned that avalanche multiplication to generate electrons in the substrate is not possible with the device parameters chosen. This is because the maximum electric field in the depletion region does not exceed the threshold field (5.3×10^5 V/cm) needed to cause avalanche multiplication. The other possible electron sources are (a) electron generation in the depletion region through the thermal generation process, and (b) electron diffusion from the substrate into the depletion region. Usually, the thermal generation time constant of a good device is a microsecond or longer which is much longer than the nsec time scale we are dealing with in this report. Therefore, we neglect the thermal generation process as an electron source. The electron diffusion process mentioned here is electron diffusion from the substrate to the surface depletion region. This is perpendicular to the channel direction and is not the diffusion process along the channel direction which was included in eqn (2). It has been shown that the number of electrons entering into the depletion region through the substrate diffusion process is smaller than the thermal generation process[17]. Therefore, we also neglect this diffusion process as an electron source.

SUMMARY

With a positive linear ramping voltage applied to the upper gate of a MOS floating gate transistor, the time

dependence of the surface potential of the substrate has been simulated. The effects of channel length, effective electron mobility, gate voltage ramping rate and substrate doping level were considered. Results show that, at positions not too close to the source and drain regions, the substrate surface potential varies with time in the following way: (1) Initially, due to the small quantity of electrons available, the depletion layer in the channel region widens to compensate for the increase of the surface potential with time. (2) The increased surface potential creates a deep potential well for electrons. At the same time, the electron supply at the source and drain regions is increasing. Therefore, many electrons pour into and fill the potential well. This leads to a rapid decrease of the potential well and the surface potential. (3) Finally, the reduced force exerted on electrons due to the decreased potential well causes a further slow decrease of the surface potential.

With the parameters chosen in this report, the surface potential at the mid-channel point reaches its peak value before the end of the ramping voltage. It is found that (1) longer channel length, (2) lower effective electron mobility, (3) higher gate voltage ramping rate, or (4) lower substrate doping level gives higher mid-channel surface potentials. The mid-channel point reaches its peak value faster if (a) channel length is shorter, (b) effective electron mobility is higher, (c) gate voltage ramping rate is higher, or (d) substrate doping level is lower.

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