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Section A

CAMAC modules for recording arbitrarily long time series

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Two CAMAC modules have been designed to record the time of arrival of up to 32768 sequential events. The system consists of a clock module to generate a gated clock pulse train and a memory module to record event arrival time. Two memory modules can be operated in ping–pong mode to capture a time series of indefinite length, limited only by the capacity of the data acquisition computer storage medium. The maximum clocking frequency of 25 MHz provides a minimum digitization period of 40 ns and an inter-event deadtime of 2 clock cycles. These circuits have been used in a number of experiments for a wide variety of time measurements. They are particularly suited for interpolating event occurrences relative to high precision UTC time signals distributed by satellites. A synchronized output pulse has also been provided to allow an external time-to-digital converter to determine event arrival time relative to the clock phase. This permits time-of-flight measurements over long baselines with a fraction of a nanosecond accuracy.

1. Introduction

Even though the accurate measurement of time series is a common problem in physics and astronomy, there are few commercial devices designed to accommodate high repetition rate or low deadtime. The timing requirements of a stereoscopic ground-based gamma-ray detector system has led to the development of a set of CAMAC electronics modules providing 40 ns absolute accuracy and less than one ns relative accuracy. The design was generated to satisfy the requirements of a broad range of other time series measurements, even those that generate indefinitely large data sets. The module designs will be discussed followed by a description of their use in various experiments.

2. Circuit description

The event recording system has been designed to record the arrival times of an event series of indefinite length with a maximum deadtime of 80 ns (2 clock cycles). The timing data is captured by a memory module driven by a continuous clock pulse train from an associated clock module. Each of these modules is described below.

The CAMAC clock module has been designed to provide the required gated clock pulse train to one or more memory modules. Although an internal 20 MHz crystal oscillator is the normal source of this clock pulse train, an external clock of any acceptable frequency can be enabled to provide the time base. A set of CAMAC commands (listed in table 1) control the activities of the clock module. In addition, toggle switches and NIM inputs provide direct user control over enabling or disabling the internal or external oscillators.

The clock module also incorporates additional circuitry to test the memory module (see fig. 1). A 16 bit counter is incremented by the same clock pulse train as the 32 bit counter inside the memory module. The digital comparator generates a pulse every time the counter contains the value loaded in a 16 bit selection register. This pulse is used as an event input signal to the event module. By selecting the proper register value an event can be made to occur at any desired time. This is particularly useful for testing system timing when using two memory modules in ping–pong mode.

The CAMAC event memory module uses a 32 bit counter, running continuously at the input clock frequency, as a timepiece. To circumvent ripple count propagation delays, a set of latches is used to store the most recent value of the counter throughout the ensuing clock cycle. When an event is detected at the input, a synchronized pulse is generated which enables a second set of tri-state latches to transfer the clock count to the SRAM read/write data bus during the memory write cycle. Up to 32768 such events can be recorded using one board.

As shown in fig. 2, the NIM level event input signal is synchronized to the system clock. Several signals are generated by this circuitry as shown in fig. 3 below.

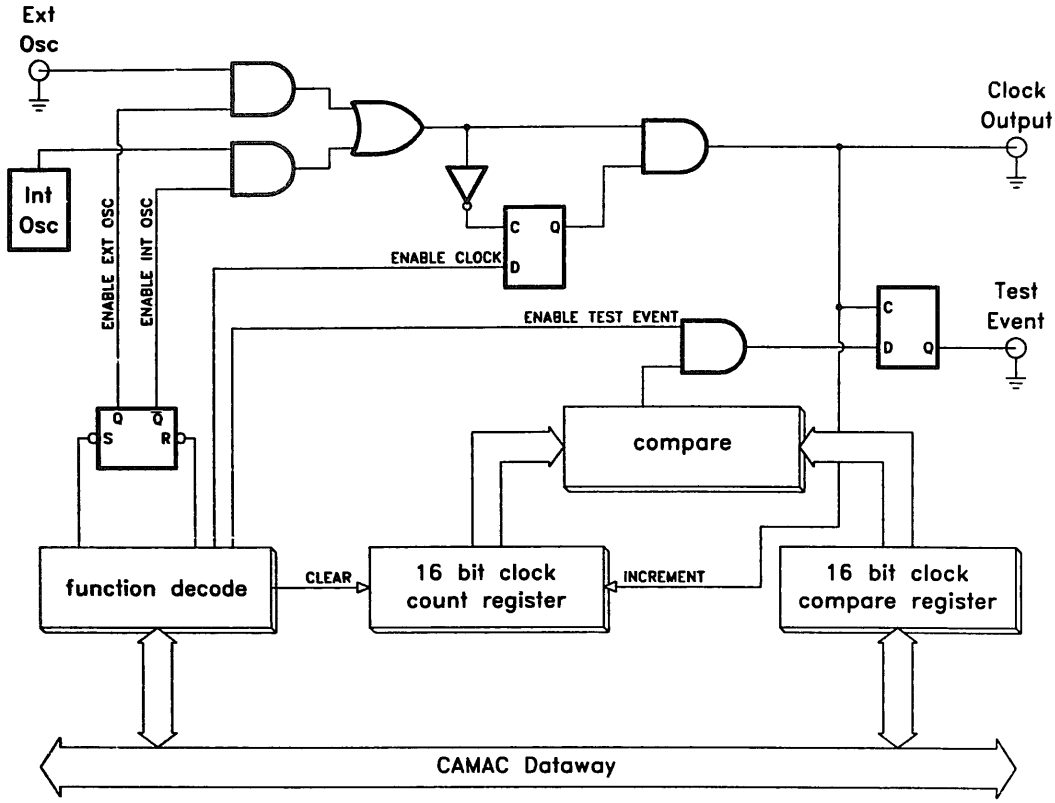

Fig. 1. Clock module block diagram.

First, the SYNCH output goes high when the event has been synchronized to the clock. This edge can be used in conjunction with a time-to-digital converter (TDC) to determine the time of arrival of the event relative to the system clock. By combining the TDC data with the digital clock count recorded in memory, an event arrival time can be determined to a relative accuracy of better than one ns. This is most useful for establishing the timing between observations of a single event by several widely separated detectors. Second is a latch pulse that latches in the present value of the 32 bit counter. Half a clock cycle later a write pulse strobes the SRAM chips and writes that value into the location designated by the memory address register. This write

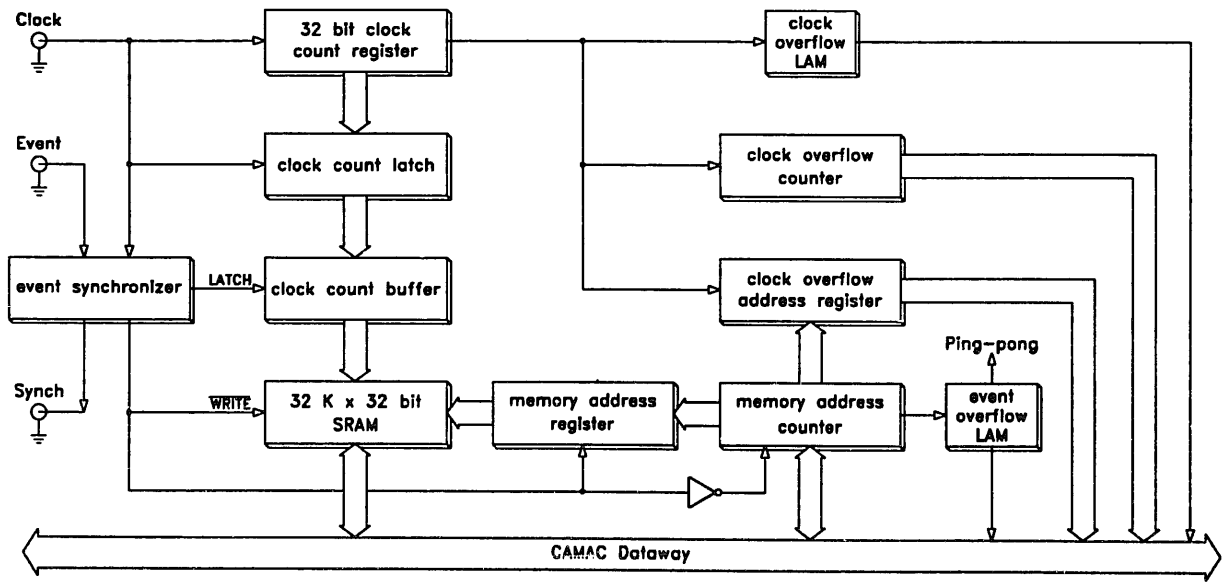

Fig. 2. Memory module block diagram.

Table 1
List of CAMAC Clock Module commands

Function	Description
F9·A0	Clear clock counter register
F9·A1	Clear clock compare register
F16·A0	Load clock compare register
F24·A0	Disable clock
F24·A1	Select internal clock
F24·A2	Disable test event output
F24·A3	Disable toggle switch
F26·A0	Enable clock
F26·A1	Select external clock
F26·A2	Enable test event output
F26·A3	Enable toggle switch

pulse to the SRAM is active low and is also used to increment the address counter on the rising edge. The fourth signal that comes from the synchronizer circuit is a synchronized pulse that is passed to a slave board which uses it to generate the latch and write signals. This is done so that only one board is responsible for synchronizing the event. It should be noted that the synchronization circuit imposes a two clock cycle dead-time during which events will not be accepted, which leads to a 12.5 MHz event frequency limit.

When the 32 bit clock count register overflows, several operations must be performed to prevent time series aliasing. To allow the data acquisition system to correctly determine the event arrival time, the contents of the memory address counter are latched into the clock overflow address register when overflow occurs. This clock overflow address register must be read out every time the counter overflows. Consequently, a CAMAC look-at-me (LAM) is asserted to notify the host computer that the register must be read out. The board also counts the number of clock register overflows to provide the data acquisition software with the ability to reconstruct the total lapsed time even if not all clock overflow LAMs are sensed or serviced.

When the 32768th event has been written, the board stops recording and asserts a LAM to notify the host computer system that it needs to be read out. If a second board (slave) is connected via a front panel connector and enabled (though not started) [1] before the master board overflows, the slave module will record ensuing events when the master unit stops, creating a seamless time series record. Similarly, when the slave is full, the recording task will revert to the master (which must have been read out previously). In this manner the two modules can keep recording events indefinitely by "ping–ponging" back and forth, as long as the data readout rate is faster than the average event rate.

The seamless "ping–pong" process is made possible by the one write cycle look ahead that the memory address register provides prior to memory overflow. This allows enough time for a signal to be passed, via the front panel connector, to the companion memory module to enable recording before the end of the write cycle. Two other signals passed between modules are the "To Slave" and "From Master" which are part of the event synchronization circuitry shown in fig. 3 and described earlier.

The memory module records event arrival times relative to an arbitrary initial time since the counter is always counting even when the board is not recording events. It is possible, however, with the use of the controllable clock module described previously to define the exact time when the counter starts to count and thus to define the relative offset. The external NIM inputs for the clock module are useful for this purpose.

The CAMAC Dataway can write to and read from the SRAM and memory address counter as well as read the latched address register and overflow counter. The operations are accomplished by asserting one or more of the commands listed in table 2.

Clearly, these commands provide the user with a considerable amount of control over the internal activities of the memory module and increase the flexibility of its integration into different data acquisition systems. Since access to the SRAM memory is bidirectional these commands also allow the memory modules to be used simply as an in-crate 128 kbyte buffer.

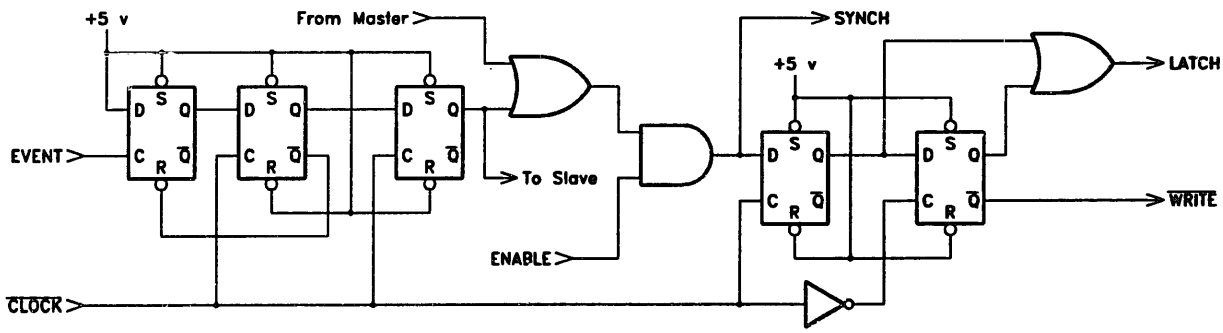

Fig. 3. Memory module event synchronization circuit.

Table 2
List of CAMAC Memory Module commands

Function	Description
F0·A0	Read memory (16 bits at a time)
F0·A1	Read memory address register
F0·A2	Read 16 bit clock overflow address register
F0·A3	Read 16 bit clock overflow counter
F8·A0	Test clock overflow LAM
F8·A1	Test event overflow LAM
F9·A0	Clear module
F9·A1	Clear address register
F9·A3	Clear clock overflow counter
F10·A0	Clear counter overflow LAM
F10·A1	Clear memory overflow LAM
F16·A0	Write memory (16 bits at a time)
F16·A1	Write memory address register
F24·A0	Disable clock overflow LAM
F24·A1	Disable event overflow LAM
F24·A2	Disable event recording
F24·A3	Disable ping–pong
F25·A0	Start recording events
F26·A0	Enable clock overflow LAM
F26·A1	Enable event overflow LAM
F26·A2	Enable event recording
F26·A3	Enable Ping–Pong

The combination of the CAMAC clock and memory modules provides a very flexible and reliable data acquisition tool for use in many different areas of research. The 40 ns accuracy of timing data can be augmented with a conventional TDC to determine the arrival time of the event to better than a nanosecond. Running a second set of memory modules with a clock 180 degrees out of phase would increase the accuracy of time measurements by a factor of two if somewhat faster performance is required.

3. System use in gamma-ray astronomy

The Whipple stereoscopic gamma-ray detector system [2] at Mt. Hopkins consists of two 10-m diameter telescopes separated by 140 m. Each telescope asynchronously records the Cherenkov light images of TeV air showers with a trigger rate of a few Hertz. Approximately 30% of these events are coincident observations of the same shower. The event clock system records each event time relative to a global positioning system (GPS) one second reference marker and establishes the relative time of arrival between telescopes to an accuracy of one nanosecond or better. This latter measurement unambiguously selects true event coincidences and provides a significant constraint on the shower trajectory.

Fig. 4 shows a schematic diagram of the event timing logic. One 20 MHz clock module provides the time base distributed to event memory modules at both telescopes. This clock is also retransmitted from the remote telescope back to the source in order to monitor temperature-induced drifts in propagation time through the intervening coaxial cables. Whenever an event occurs in the local telescope, its arrival time is recorded with two event memory modules: one driven by the direct output of the adjacent clock generator module and the other driven by the round-trip clock signal.

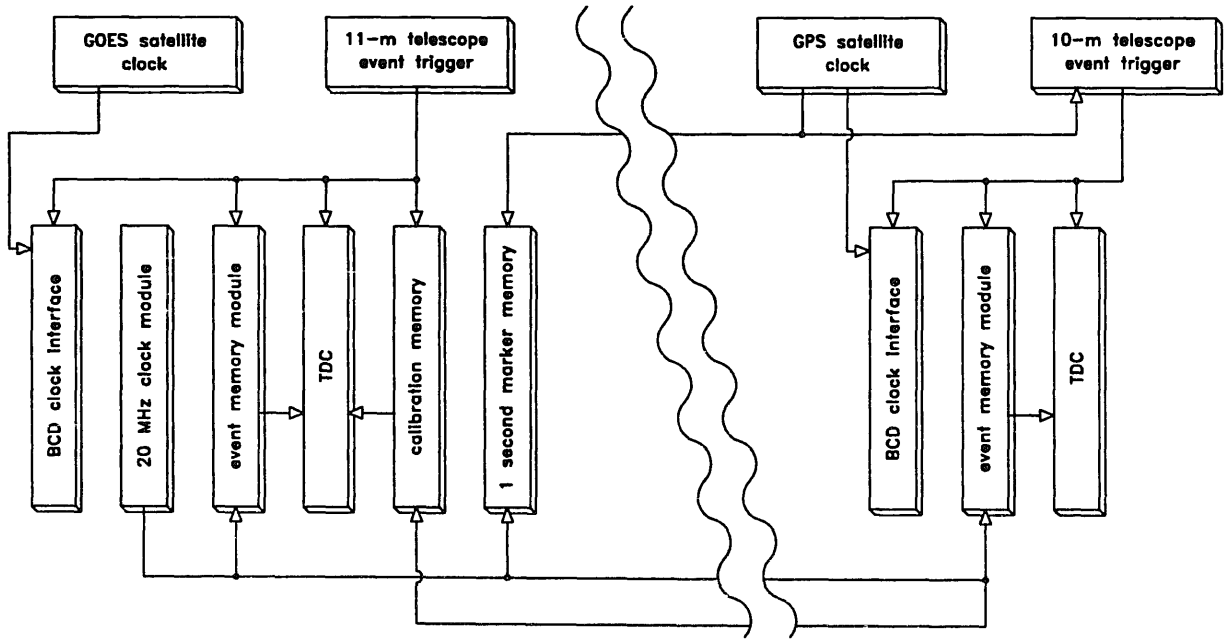

Fig. 4. Event timing logic at Whipple.

The memory modules can only record event times to the nearest clock period, an interval of 50 ns. To do better, a LeCroy 2228 TDC is used to measure the time between the event pulse (TDC start) and the memory module SYNCH pulse (TDC stop). This combination of digital and analog measurements determines the event time to an accuracy of a fraction of a nanosecond relative to the 20 MHz base clock. A similar scheme is implemented at the remote telescope. In subsequent off-line data analysis the relative time between shower observations can be established to an accuracy of one nanosecond even though the separation distance between telescopes corresponds to a 400 ns transit time.

An additional set of event memory modules is triggered by one second UTC marker pulses from a Kinemetrics model GPS-DC Mark III GPS synchronized clock receiver. These periodic pulses determine the reference origin for the 20 MHz clock train. Finally, the UTC identity of each precision second mark is recorded by a CAMAC module which latches a 48-bit BCD code containing the day-of-year, hour, minute, second, and millisecond from the GPS clock parallel output port. For redundancy, an identical interface provides the same function for the output of a Kinemetrics 468-DC GOES synchronized clock.

4. Other applications

The study of chaos and non linear dynamics has created an enormous interest in the behavior of relatively simple systems which can display remarkably complex evolution. It is sometimes difficult to tell whether a system is truly random or else chaotic but nevertheless deterministic. At the University of Michigan, Robert Savit has been developing statistical measures [3] that might distinguish between these two hypotheses. He suggested that the time sequence generated by radioactive decay might be an interesting test of a system which is understood to be intrinsically random. The event clock system was accordingly designed to record an arbitrarily long time series by allowing two adjacent memory modules to swap (ping–pong) the tasks of storing event arrival times and dumping the previous contents to the host computer. The design particularly addressed the problem of eliminating spurious aliasing effects which might affect the statistical analysis. The nuclear process we chose to monitor was orthopositronium annihilation following from the β^+ decay of ^{22}Na. Each event was identified by the coincidence of gamma-ray conversions in two oppositely facing scintillation counters. The experiment was conducted by Chris Pentzell and formed the basis for an undergraduate senior thesis [4].

Measurement of time series has also been incorporated into two experiments for a graduate laboratory course. One of the experiments is a fairly straight-forward measurement of the lifetime of stopped muons. The 50 ns clock period allows the exponential decay curve to be followed over at least 200 time bins. The data from an overnight run is accurate enough to easily observe the apparent 5% decrease in lifetime due to μ^--interactions with carbon nuclei. The second experiment explores the time series of a nonlinear system. The particular example is the "dripping faucet" which has been extensively studied and described by the Santa Cruz group [5].

We have also found the event clock system to be remarkably convenient for testing electronic equipment. Recently our group developed a simple current-to-frequency converter for measuring μA currents [6]. The intrinsic period stability of this circuit was monitored by accumulating 32 768 consecutive pulses and analyzing the statistics of various subsets of the data. There is a very broad category of problems where obtaining a long time series would help uncover and diagnose subtle equipment failures.

5. Conclusion

A CAMAC event timing system has been designed to digitally record the occurrence of electrical trigger signals with an accuracy of 40 ns and arbitrary depth. The system has been successfully used in a variety of experiments covering astrophysics, nuclear physics and nonlinear dynamics. This work has been supported by the US Department of Energy contract DE-AC02-76ER01112.

References

[1] The two CAMAC commands, shown in table 2, "Enable event recording" and "Start event recording" perform different tasks. The "Enable" makes it possible for either board to start recording if it is activated by another signal – either a "Start command or a ping–pong signal. The "Start" command therefore determines which of two boards will start recording first.

[2] Carl Akerlof, Richard Lamb, David Lewis, Don Meyer, and Trevor Weekes, Proc. SPIE 33rd Annu. Int. Symp. EUV, X-Ray, and Gamma-Ray Instrumentation for Astronomy and Atomic Physics, San Diego, CA, USA, August 7–11, 1989, SPIE Conf. Proc. Vol. 1159, p. 270.

[3] Robert Savit and Matthew Green, Physica D50 (1991) 95; Physica D50 (1991) 521.

[4] Christopher Pentzell, University of Michigan senior thesis (unpublished) (1991).

[5] Robert Shaw, The Dripping Faucet as a Model Chaotic System (Aerial Press, Santa Cruz, CA, 1984).

[6] Dov Frishman and Carl Akerlof, Nucl. Instr. and Meth. A311 (1992) 306.