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THE UNIVERSITY OF MICHIGAN
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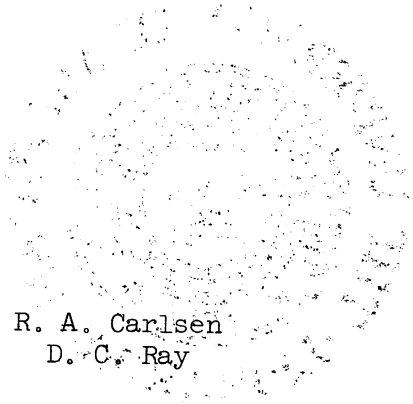
COMPUTER COMPONENTS DEVELOPMENT



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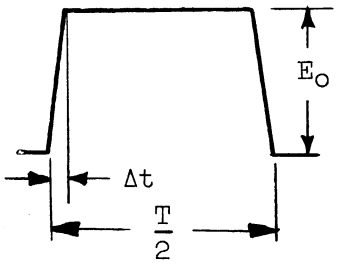


$\Delta t = T/10$

Ideal Information Pulse

I	Gate current
I'	Input gate current
I^*	Minimum input clamp current
I_f	Forward diode current
I_{BO}	Initial reverse diode current after switching
I_B	Reverse diode current
I_3	Grid pull-down current
i_d	Instantaneous diode current (general)
i_c	Diode C instantaneous current
i_b	Diode B instantaneous current
V_d	Voltage drop across diode (general)
$V_A, V_B, V_C, \ldots$	Voltage drop across particular diodes A, B, C, ...
$E_{1,2,\ldots n}$	Supply voltages
E_o	Amplitude of input (or output) pulse
E_b	Back bias voltage
E_g	Grid voltage swing
E_n	Amplitude of noise clipping
A_c	Amplitude of clock voltage
C_o	Capacitance of an "and" gate input
C_1	Capacitance at the "and" gate output
C_g	Effective capacitance at the grid
T	Basic clock period
Δt	Rise and fall time of an idealized information pulse
prf	Pulse repetition rate
ϵ	Dynamic noise voltage
a/b	Ratio of initial back current to steady-state forward current

ABSTRACT

The speed of operation of a diode gating structure is limited by 1) the amount of noise which can be tolerated in the circuit and 2) the magnitude of current required per gate input. Both of these limiting factors are dependent on the reverse transient properties of the semiconductor diodes used in the gate structure. As frequency of operation is increased, the reverse transient is accentuated by the required increase in gate currents. This report is a study of the effect of various diode parameters on overall gate performance.

OBJECTIVE

The purpose of this contract was to investigate experimentally and theoretically the possibliity of increasing the speed of operation of the dynamic circuitry of SEAC-type computer components. This particular report deals with the design limitations of the diode gating structure.

1. INTRODUCTION

Diode Gating Structure

1.1 DESIGN PHILOSOPHY

The purpose of this contract is to investigate experimentally and theoretically the possibility of increasing the speed of operation of the dynamic circuitry of SEAC-type computer components by at least an order of magnitude.

The investigation has proceeded along three lines: investigation of the pulse amplifier, pulse transformers, and diode gating structures. The basic philosophy followed in the design of circuitry for high-speed operation has been the reduction of voltage swing. That is, as frequency of operation is increased the available voltage swing is reduced while the over-all current remains constant. As a consequence of this approach, high g_m tubes are required for low-current gates at high frequency.

Other reports in this series deal with the pulse amplifier and design aspects of the problem. This particular report deals with design and limitations of the diode gating structure.

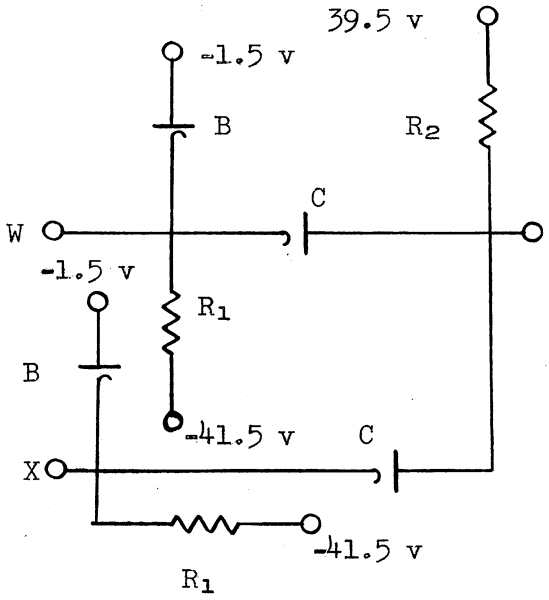
1.2 OPERATION OF GATING STRUCTURE

The circuit of a typical gate structure is shown in Fig. 3.2-1a. This circuit consists of two parts—an "and" gate followed by an "or" gate. The typical "and" structure shown below has the C diodes arranged in such a manner that the output voltage is equal to the lowest voltage applied to the diodes. Let us assume, therefore, that we have two voltage levels, 0 and 1. The 1 level shall be the highest level. If all the inputs of the "and" structure are high, then the output is high or in the one state. However, if any one of the inputs to the "and" structure is low or in the zero state, the output of the "and" structure is also in the zero state. This can be verified by studying the circuit given. The "and" gate output is clamped to the zero level by the B clamp diode and pull-down resistor R_1. Therefore, in the absence of any signal the gate is automatically clamped to the zero level.

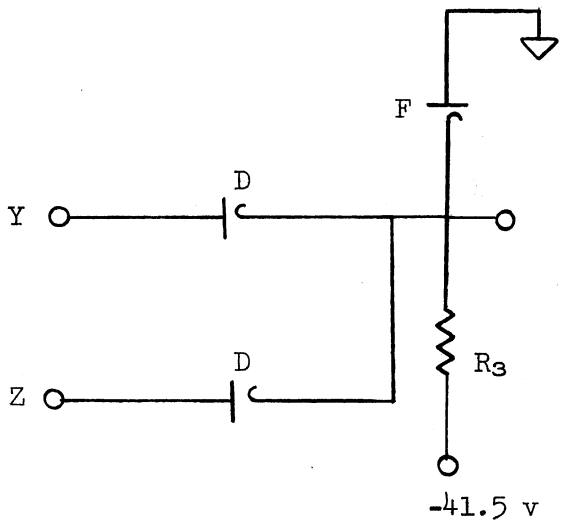
A typical "or" gate is shown below. The "or" gate implements the logical function Y + Z which is the disjunction of Y · Z. The gate must provide

an output if either of the inputs are high. This can be verified by an examination of the circuit.

If either of the preceding "and" gates provides a 1 output, it can be seen that the output of the "or" gate is 1. On the other hand, if neither of the "and" inputs provides a high output the "or" output will be zero.



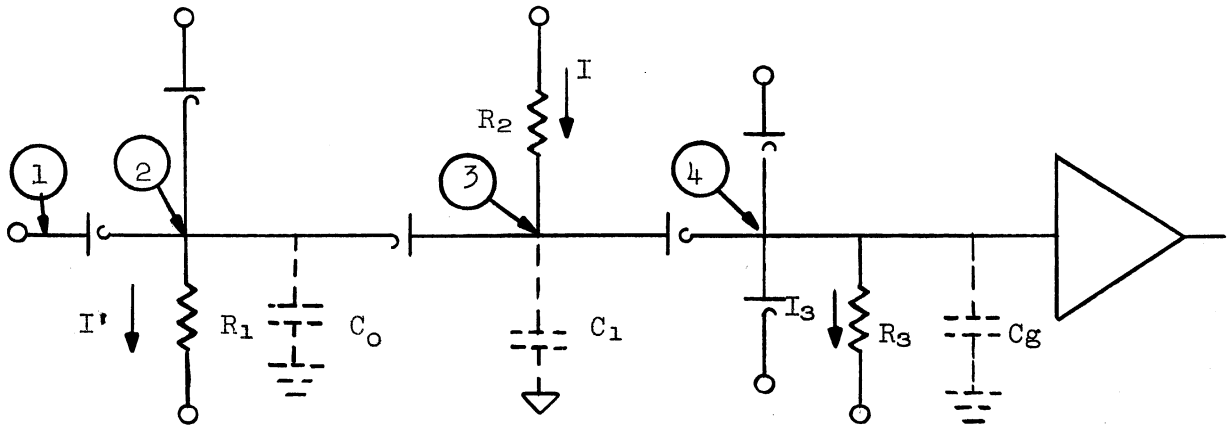
Typical "and" gate W · X



Typical "or" gate Y + Z

1.3 GATE REQUIREMENTS FOR IDEAL DIODES

Some general remarks can be made regarding the gate configuration below where perfect diodes are assumed.



First, if the gate voltage swing is small compared to the supply voltages, the charging and discharging of the capacitance associated with the gate occurs at approximately constant current. If the grid capacitance C_g is required to discharge in time Δt through the grid pull-down resistance R_3, the grid pull-down current I_3 is then:

$$I_3 = \frac{E_g C_g}{\Delta t} . \qquad (1)$$

The gate current I required to swing the grid E_g volts in Δt seconds is given by:

$$I = \frac{(E_g + E_n)C_1}{\Delta t} + \frac{E_g C_g}{\Delta t} + I_3 , \qquad (2)$$

where

$I = 2I_3$ if C_1 is neglected,
$\Delta t = T/10$,
T = the clock period, and
E_n = amplitude of the noise clipping at the "or" gate input.

Example: Let T = 100 μsec (10 Mc operation)
E_g = 1 volt
E_n = 1 volt
C_g = 30 μμf
C_1 = 5 μμf
I_3 = 3 ma
I = 7 ma

Second, the input gate current must satisfy two requirements, namely, I' must be greater than I and must satisfy Equation (3). Equation (3) is the requirement placed on the input gate current by the discharge time of the circuit input capacitance. The input capacitance of each gate must discharge through the input pull-down resistance.

$$I' \geq \frac{E_o C_o}{\Delta t} , \qquad (3)$$

where

E_o = amplitude of the signal applied to the gate input.

A condition defined as "and" diode-limiting must be avoided. Note that the grid can rise no further positive during a pulse than the maximum potential of point (3) which is in turn determined by the amplitude of the input pulse at point (2). This action may be used to advantage to obtain grid clipping if the input pulse has a flat top. However, if noise is present in the input pulse, it will then also appear on the grid pulse.

The grid-pulse rise time is also influenced by another factor. The grid pulse can rise no faster than the slowest rising input, but in a clocked computer the information inputs are up before the clock pulse arrives. This

stresses the necessity of having a well-shaped clock pulse with a rise and fall time less than or equal to the rise time desired for the grid pulse.

If the above requirements are met, that is, if (1) the input signal is more positive than the grid clip level, and (2) the slowest input rises faster than the desired grid rise, then in the ideal diode case, the grid wave-shape is independent of the input wave shape and is a function of gate current I and any wave shaping that may be done on the grid.

These requirements are fundamental to gating operation, and although they were considered for the ideal diode case, they apply equally well to the nonideal diode case with only slight modification.

2. APPLICATION OF NONIDEAL DIODES TO GATING CIRCUITS

Unfortunately, the diodes in a gating structure are far from ideal; therefore, the emphasis has been placed on the effect of diode transients on the circuit of Fig. 3-2-1.*

It is the diode transient characteristics, particularly the reverse transients, which ultimately limit high-speed gating performance. For example, the reverse transient current of the pulsed "and" diode is primarily responsible for noise at the "and" gate output. If the frequency of operation would be increased by a factor of two with E_g held constant, the gate current I and the initial forward current of each of the pulsed "and" diodes would be increased by approximately a factor of two. Increased forward current would accentuate noise, thus demanding increased noise clipping, and ultimately a large gate current is required to charge capacitance C_1 the additional ΔE_n voltage.

Therefore, emphasis has been placed on diode transients and their resulting effect on the operation of a high-speed logical circuit. The following sections discuss Theory of Semiconductor Properties (2.1), Diode Transients (2.2), and Diode Specification (2.3) for the logical gating circuit.

2.1 THEORY OF SEMICONDUCTORS

The purpose of this section is to outline some of the basic principles necessary to an understanding of semiconductor diodes. A short section on basic semiconductor properties is included mainly to introduce semiconductor terminology. This is followed by a short discussion of the mechanism of current flow and those equations leading up to a solution for the reverse current as a function of time.

*A discussion of various logical configurations is included in Appendix A. The circuits of Fig. 3.2-1 were found to be superior to the others considered.

2.1.1 Basic semiconductor properties[1].—Electrical conductivity is a measure of the number of charge carriers per unit volume which are available to move under the influence of an electric field. Semiconductors, as the name implies, are materials with a conductivity between that of metals and insulators. Two materials, silicon and germanium, are of the semiconductor type and in the pure form (intrinsic) have resistivities of 60 Ω/cm and 60 KΩ/cm, respectively. These intrinsic materials are of little practical use until additional impurity (donor and acceptor) atoms have been added to the initially pure crystalline structure. The addition of a donor atom introduces (or donates) an extra electron or carrier into the crystal structure. The presence of some relatively few impurities of this type greatly increases the conductivity over that of the initially pure germanium.

In the same manner, if an atom with 3 valence electrons (acceptor impurity) is introduced into the crystalline structure, the added impurity has an affinity for the neighboring valence electrons of the intrinsic germanium. The capture of the needed valence electron then generates an absence of an electron (or hole). The hole is propagated in a random fashion throughout the crystal until such a time as the hole recombines with a free electron.

If two blocks of germanium with donor-type impurity (type N) and acceptor impurity (type P) are fused and a potential is applied to the fused block, a current flows. In the N-type material the current is composed of moving electrons which are called majority carriers and moving holes which are called minority carriers. In the P-type material the electrons are the minority carriers and the holes are the majority carriers. At any particular cross section in the block the total current is the sum of the majority and minority carriers.

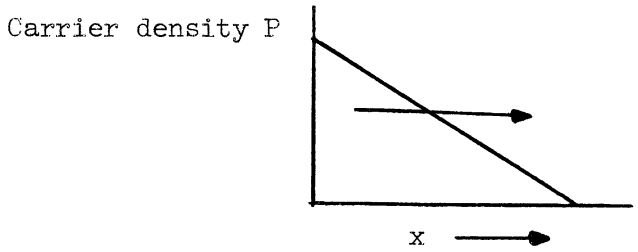
2.1.2 Mechanism of current flow[1,2,10].—Carrier movement in semiconductors is the result of the superposition of two effects, drift and diffusion.[1] Drift is the motion resulting from the force associated with an applied electric field. Diffusion, on the other hand, is the result of thermal agitation and is therefore random in nature. A diffusion current will flow by virtue of a density gradient. The equation relating the gradients to the current density J is given by:

$$J_p = - q D_p \nabla P , \qquad (1)$$

where

q = charge of an electron,
D_p = diffusion constant for hole,
∇P = gradient of hole density P, and
J_p = current density due to the diffusion of holes ($J = I_p/A$).

For a one-dimensional case and with the origin as shown below the above equation reduces to:



$$J_p = - q D_p \frac{dP}{dx} \quad . \tag{2}$$

The theoretical analysis in the literature[5,8] begins by assuming that the voltage drop across the end region is zero. This allows a relatively simple analytical approach in that the diffusion equation is solved for P under the boundary conditions of interest. The diffusion current is then obtained by substitution of $\partial P/\partial x$ in Equation (2).

The justification for the above simplification is based upon the fact that the voltage drop across the diode is almost entirely equal to the voltage drop across the junction.

If the concentration of P impurities is much greater than the concentration of N, the total current can be assumed to be equal to the hole current (I_p). In Fig. 2.1-1 an idealized junction diode has been taken to illustrate the function of the barrier height in diode operation. Although the point-contact diode, basically a P-N junction diode with a small region of P under the whisker, is of major interest, the analogous junction diode allows a more manageable solution due to its simple geometry.

Figure 2.1-1 is a schematic representation of a diode under condition of equilibrium. The effect of forward and reverse bias is also illustrated. Note the effect of the external field on the barrier height.

Boltzmann's equation relates the relative concentration of carriers adjacent to the barrier region to the potential gradient. If P_{po} is the concentration of holes adjacent to the barrier in the P region and P_{no} is the concentration in the N region under equilibrium conditions, then P_{no} is related to P_{po} by:

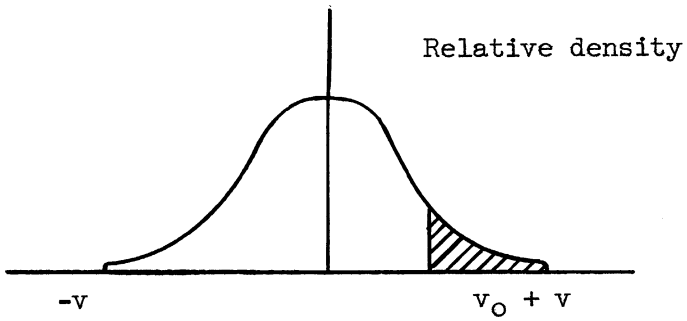
$$\frac{P_{no}}{P_{po}} = e^{-\frac{q\Delta V}{kT}} , \tag{3}$$

where

q = charge of an electron,
k = Boltzmann's factor, and
T = absolute temperature, °K.

An understanding of the derivation[10] of the above equation is basic to the understanding of the mechanism of current flow at the junction.

Consider a one-dimensional velocity distribution of the holes in the P region as a result of thermal agitation.



Since the distribution is Gaussian, it is easy to show that the probability of a carrier acquiring sufficient velocity v_o to jump the potential barrier is given by:

$$P_{po} \int_{v_o}^{\infty} P(v)dv = \frac{P_{no}}{2} \quad . \tag{4}$$

The significance of the right-hand factor is that of those holes which have crossed into the N region any that have a velocity component in the direction of the barrier are free to roll back down the potential hill. Therefore, since at equilibrium* the current from region P to N is equal to the flow from N to P, the number of holes with velocities greater than v_o is exactly equal to one-half the total number of holes in the N region.

$$P(v) = \frac{1}{\sqrt{2\pi\ kT/m}} \exp^{-\left(\frac{v^2 m}{2kT}\right)} . \tag{5}$$

The kinetic energy of an electron (hole) is related to the potential by:

$$\frac{mv^2}{2} = q\Delta V \quad . \tag{6}$$

Then:

$$-\frac{v^2}{2}\frac{m}{kT} = -\frac{q\Delta V}{kT} . \tag{7}$$

P(v) becomes:

$$P(V) = \frac{q}{2kT} e^{-\frac{2\Delta V}{kT}} \quad . \tag{8}$$

*No bias applied.

The correctness of this normalization can be checked by integrating

$$\int_{-\infty}^{+\infty} P(v)dv \quad .$$

Then:

$$\frac{P_{po}}{2}\frac{q}{kT}\int_{V}^{\infty} e^{-\frac{q\Delta V}{kT}}\, d\Delta V = \frac{P_{no}}{2} \quad ; \tag{9}$$

$$P_{po}\, e^{-\frac{q\Delta V}{kT}} = P_{no} \quad ;$$

$$\frac{P_{no}}{P_{po}} = e^{-\frac{q\Delta V}{kT}} \quad . \tag{3}$$

If P_p and P_n are the respective hole concentrations in the P and n region when the diode is biased by an external voltage source

$$E_x = -\frac{\partial V_d}{\partial x} \ ,$$

Equation (3) can be modified to relate the equilibrium concentration density P_{no} to the concentration P_n when the diode is externally biased.

Equation (3) for the forward bias condition may be written:

$$P_n = P_{po}\, e^{-\frac{q}{kT}(\Delta V - V_d)} \quad ;$$

$$P_n = P_{po}\, e^{-\frac{q\Delta d}{kT}} e^{\frac{qV_d}{kT}} \quad . \tag{10}$$

Substituting Equation (2) in Equation (10),

$$P_n = P_{no}\, e^{-\frac{qV_d}{kT}} \quad . \tag{11}$$

The hole current under steady-state conditions is proportional to the increase in minority carrier density in the N region:

$$I_p \ \alpha [P_n - P_{no}]$$

$$I_p = P_{no}\, C\left(e^{\frac{qV_d}{kT}} - 1\right) \quad . \tag{12}$$

Under back-bias conditions V_d is negative and the hole current is just equal to the intrinsic back current I_o.

$$I_p = -p_{no} C = -I_o \ ;$$

$$\therefore \quad I_p = I_o \left(e^{\frac{qV_d}{kT}} - 1 \right) \ . \qquad (13)$$

Equation (13) may be recognized as the steady-state diode equation. Although the result above applies to steady-state conditions, Equation (11) does not have this restriction. It is this relationship that forms the basis for the Ebers-Moll equations which have contributed greatly to the theoretical analysis of the junction transistor.[11]

2.1.3 The solution of the diffusion equation for reverse current as a function of time.—The presence of diode transients has been known for many years. Many individuals and organizations have contributed to both the theoretical and experimental understanding of these nonperfect switches. The forward transient may be considered to be the inability of a diode to establish the steady-state gradient in the N region instantaneously. In the same way, the reverse transient is the result of the delay in removing the stored carriers in the n region after the external field has been reversed.[5]

If some simplifying assumptions are made regarding the diode, it is possible to obtain a solution for the reverse current as a function of time.

1. Current flow in the end regions is entirely by diffusion.
2. The cross-section dimensions are much greater than the diode width.
3. If the concentration of P $\gg$ N, then it can be assumed that current flow at the junction is entirely by holes.

At the junction, current flow is by hole diffusion only and therefore Equation (2) of Section 2.1.2 becomes

$$I_B = \left| - q D_p \frac{\partial P}{\partial x} \right|_{x = 0} \ , \qquad (1)$$

where

I_B = the reverse current resulting from hole storage in the P region.

Thus, to solve for the reverse current it is then necessary to solve the continuous-flow or one-dimensional diffusion equation (18) for the proper set of boundary conditions associated with the reverse current transient:

$$\frac{\partial P}{\partial t} = \frac{P_{no} - P}{\tau_p} + D_p \frac{\partial^2 P}{\partial^2 x} \ , \qquad (2)$$

where

P = hole density in N region,
P_{no} = hole concentration in N region under conditions of no externally applied bias, and
τ_p = life-time of holes in N region.

The reverse transient is composed of times T_1 and T_2. (See Fig. 2.1-2.) After a semiconductor diode has been passing current in the forward direction for a period of time sufficient to allow the hole density P to reach its steady-state value, the concentration gradient is as shown. When the bias is reversed, the concentration gradient assumes successive conditions at times t_1, t_2, t_3, and t_4.

During T_1 the hole diffusion out of the N region is limited by the resistance of the external circuit. Thus T_1 is a function of the external circuit resistance and the previous forward current.*

Reverse-recovery time measurements have shown that for point-contact and small junction diodes $T_1 \ll T_2$. One possible reason for this would be the relatively small volume of P and N material used in the construction of the above type of diode as compared to the larger volumes used in such junction diodes as the G. E. 1N91, where T_1 does become an important factor. Since $T_1 \ll T_2$ here, we can limit our interest to the time T_2.

We are interested in solving the diffusion equation for the following boundary conditions (see Fig. 2.1-2): $P = 0$, $x = 0$, and $P = 0$, $x = L_o$ at $t = 0$, to obtain $P = f(x,t)$ $t \geq 0$.

The procedure is to solve Equation (2) for the boundary conditions given and thus evaluate two of the three resulting constants. However, to satisfy the third constant it is necessary to require Equation (3) to equal Equation (4) at $t = 0$:

$$P = f(x,t) \quad \text{for} \quad t \geq 0 \; ; \tag{3}$$

$$P = f(x,t) \quad \text{for} \quad t < 0 \; . \tag{4}$$

Equations (3) and (4) both result from the solution of Equation (2), but Equation (4) is the steady-state solution for hole density before switching bias conditions.

The mathematical steps have been omitted, as routine methods of solving partial differential equations are used:

$$P = P_{n\,max} \left[\frac{\sin h \, \frac{L_o - x}{L_o}}{\sin h \, (L_o/L)} \right] \; ; \tag{3}$$

*Sometimes reference is made to holes being swept out of the N region. It is true that those holes adjacent to the junction are "swept out," but the majority of the N region holes "die" as a result of recombination if T_1 is much less than T_2.

$$P_{n\,max} = \sum_{1}^{m} \frac{2}{m\pi} \sin \frac{m\pi x}{L_o} \left[1 + \left(\frac{L_o}{m\pi L} \right)^2 \right]^{-1}$$

$$= x \exp \left\{ - \frac{t}{\tau_p} \left[1 + \left(\frac{m\pi L}{L_o} \right)^2 \right] \right\} . \qquad (4)$$

Then from Equation (1) at $x = 0$ and $L_1/L \ll 1$,

$$I_r = - 2 q P_{n\,max} \frac{D_p}{L_o} \exp \left[\left(\frac{-t}{\beta} \right) \right] , \qquad (5)$$

where

$$\beta = \frac{\tau_d L_o^2}{\pi L^2} .$$

The diffusion constant is related to hole mobility by Einstein's relation

$$D_p = \frac{kT}{q} \mu_p . \qquad (6)$$

$$\therefore \quad \beta = \left(\frac{L_o^2 q}{\pi^2 k} \right) \frac{1}{T\mu_p} ,$$

where

$P_{n\,max}$ = maximum hole concentration on the N side of the junction under steady-state forward bias conditions,
L_o = length of N region,
$L = \sqrt{D_p \tau_p}$,
T = absolute temperature in degrees, and
k = Boltzmann's constant.

Certainly as small a β as possible is desired. Care should be taken in drawing conclusions, especially in regard to temperature effects. The model taken is quite simple, and such considerations as surface recombination have been neglected.

There are three conclusions that can be drawn:

1. Since hole mobility (μ_p) is less than electron mobility (μ_e), there would be a gain in recovery time if the current was primarily electron current rather than hole current as assumed here.

2. The hole mobility of silicon (μ_p) is less than the hole mobility, for germanium (μ_p). Therefore, diodes made from basic germanium may be superior to silicon diodes of identical construction.

3. Small dimensions are very important as L_o appears as a squared term.

There are a number of factors that affect reverse-recovery Current I_B

1. I_B is a function of the diode physics by Equation (5).
2. I_B is a function of steady-state forward current (I_f).

Notice in Equation (5) that the term $P_{n\ max}$ appears. By Boltzmann's equation governing diffusion across the junction,

$$P_{n\ max} = P_{no}\, e^{-\frac{qV_d}{kT}} \qquad (11)\ \text{(Section 2.1.2)}$$

V_d is the external forward bias, and is a function of forward current (I_f)

3. I_B is a function of pulse rate (prf).

If the pulse rate is such that the forward-current steady-state condition is not reached, then the reverse-recovery time is certainly less.

4. Reverse-recovery time has been assumed equal to T_2, but if T_1 is not negligible, circuit resistance then becomes much more important.

5. The back bias E_b also affects back-recovery time, but to a much lesser extent than would be expected.

Considering all the above,

$$I_B = f(I_f,\ prf,\ E_b,\ R_c)\ . \qquad (7)$$

The factors affecting diode back-recovery are covered in detail in Section 2.2.1.

2.1.4 Barrier capacitance[1]. —At the junction of the P- and N-type regions there is a very thin layer in which no mobile carriers exist. The width of this region is a function of the back bias. That is, as the external bias is increased, holes and electrons withdraw respectively from the fixed acceptor and donor atoms. The resulting increase in barrier charge is responsible for the increase in barrier potential.

A solution for the barrier capacitance of a step junction diode is of interest.[10]

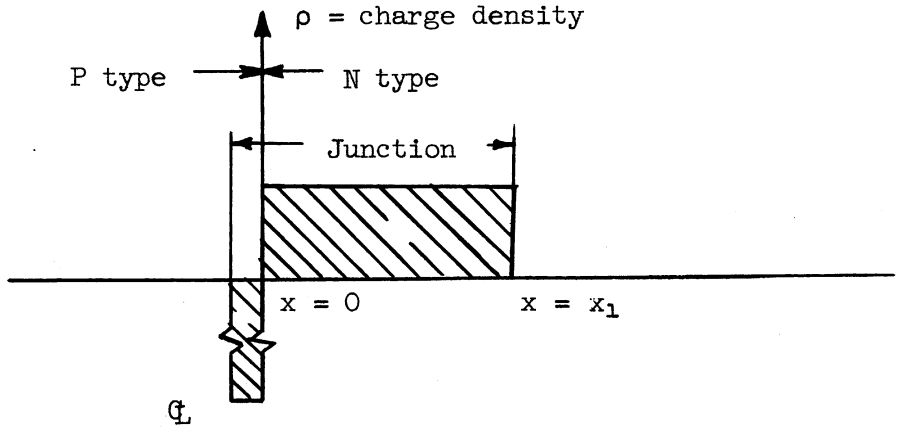
Assume that the concentration of P-type impurity is much greater than that of the N-type impurity. The width of the depletion layer in the P region is negligible compared to the width in the N region as $P \gg N$.

If ρ is equal to charge density, then:

$$\rho = q\, N_d\ ,$$

where

q = charge of an electron, and



N_d = density of donor impurities.

Solving Poisson's equation for the region,

$$\nabla^2 V = -\frac{\rho}{\epsilon} \tag{1}$$

$$\ddot{V}(x) = -K \tag{2}$$

where

$$K = \frac{qN_d}{\epsilon} \text{ , and}$$

ϵ = the dielectric constant of the depletion layer.

Integrating Equation (2) once:

$$\frac{dV}{dx} = -Kx - K_1 \text{ ,} \tag{3}$$

which is equal to:

$$\vec{E} = \frac{qN_d}{\epsilon} x + K_1 \text{ ,} \tag{4}$$

as

$$\vec{E} = -\nabla V = -\frac{dV}{dx} \text{ .}$$

Integrating (2) a second time we have:

$$V = -\frac{qN_d}{\epsilon} x^2 - K_1 x - K_2 \text{ .} \tag{5}$$

The boundary conditions are:

$$\vec{E} = V = 0 \text{ when } x = 0 \text{ .}$$

Therefore:

$$K_1 = K_2 = 0 \ ,$$

$$V = -\frac{qN_d}{\epsilon} x^2 \ . \tag{6}$$

The junction capacitance C_j is equal to:

$$C = \frac{Q}{V_1} \ , \tag{7}$$

where

$$Q = A\epsilon \frac{E}{2}\Big|_{\substack{\text{at} \\ x = x_1}} = \text{total charge,} \tag{8}$$

V_1 = the potential at $x = x_1$, and
A = effective area of the junction.

Substituting Equation (4) into Equation (8),

$$Q = \frac{A\ q\ N_d\ x_1}{2} \ . \tag{9}$$

Solving Equation (6) for x_1 in terms of V_1,

$$x_1 = \frac{\sqrt{\epsilon V_1}}{qN_d} \ . \tag{10}$$

Substituting Equation (10) into Equation (9),

$$Q = \frac{A}{2}\sqrt{\epsilon V_1 q N_d} \tag{11}$$

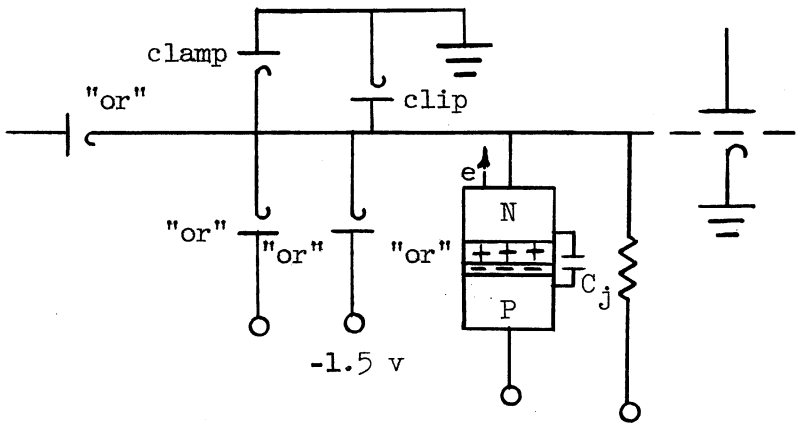
Substituting Equation (11) into Equation (7),

$$C_j = \frac{A}{2}\sqrt{\frac{\epsilon q N_d}{V_1}} \ . \tag{12}$$

The capacitance of the junction C_j requires a charging current I_j to flow into the diode when the depletion layer increases.

Consider the "or" diodes on the grid of the lower tube of Fig. 3.2-1. The nonconducting "or" diode would contribute to the total effective grid capacitance because as the grid rises in a positive direction the depletion layer becomes wider, requiring electrons to leave the N region.

Test results have shown that the contribution of barrier capacitance



of a point-contact diode to the total grid capacitance may be neglected if the grid noise clipping (back bias on the grid "or" diode) is equal to or greater than one volt. Since the barrier capacitance decreases with increased back bias, the contribution of barrier capacitance is even further reduced as the noise clipping is increased.

The preceding material will serve as a guide or basis for the remainder of the report. The point-contact diode, because of its grometry and method of manufacture, does not readily lend itself to mathematical analysis, and thus work with point-contact diodes has tended to be experimental in nature. The analogy between the two diode types is valid as the difference in transient behavior is only in magnitude and not in character.

2.2 DIODE CHARACTERISTICS

In this section the factors which affect diode transients for low current are discussed. Back and forward transient measurements, static characteristics, and experimental results of testing are included.

2.2.1 Back transients.—The recovery time as specified by diode manufacturers in their literature is not applicable to the problem at hand. In general, the manufacturers have specified reverse-recovery time as the time required to reach a particular back resistance for steady-state currents of the order of 30 ma. This is approximately three times larger than the current required in the typical gate circuit considered by this project. It has not been found feasible to extrapolate the recovery time at low currents from the data supplied by the manufacturer. Therefore, during the early phase of this project, a quantity of data was taken to supplement the manufacturers' data. The purpose of this work was first to compare diodes and second to gain insight into diode transient effects. A summary of these tests is included at the end

of this section. For the purpose of this report, however, the following transient tests have been based upon biases and currents encountered in the proposed logic circuit of Fig. 3.1-1a. The gate circuit itself has been used as a test circuit whenever possible. Equation (7) of Section 2.1.3 indicates those factors affecting reverse recovery of point-contact diodes.

$$I_B = f(I_f, E_b, R_c, \text{prf}) , \qquad (7) \text{ (Section 2.1.3)}$$

where

I_f = steady-state forward current,
E_b = back bias,
R_c = circuit resistance in series with the diode, and
prf = pulse repetition rate.

(a) Effect of Forward Current (I_f) on Recovery Time.

The reverse current in a point-contact diode is primarily a function of the forward current previous to switching. That is, the magnitude of the carrier gradient in the N region determines the amplitude and duration of the reverse current after switching.

The importance of the effect of diode reverse-transient currents can be verified by the following experiment. The test consists of observing the current flow in a pulsed diode. A 100-ohm resistance is inserted in the diode circuit between the anode and ground. Normally, a current I_f is allowed to flow in the diode. The diode is then pulsed and the transient current is observed by the voltage which is developed across the 100-ohm resistor. The data and circuit are shown in Table 2.2-I. The included photographs are the voltage wave-shapes at point (2') and can be calibrated directly in ma.

Before the positive biasing pulse was applied, the voltage drop across the 100-ohms was negative. The shaded area is then the integral of the reverse current or, as defined here, the "lost" charge. The amplitude of the input pulse was adjusted so that the back bias was equal to approximately -1.5 volts at the end of the 50 μsec pulse.

These reverse currents are of major concern in high-frequency switching as they represent losses not present in the ideal diode. For example, in the ideal diode the gate current I must supply charge to the capacitance C_1 at the "and" pull-up resistor, the capacitance C_g at the tube grid, and current to the grid pull-down resistor. In the nonideal case the gate current must supply an additional amount of charge which is lost to the grid-clamp diode. The input gate current I' to a particular pulsed "and" gate input must also be increased by an amount ϵ ($I'' = I' + \epsilon$) to supply the reverse current taken by the pulsed input clamp diode. Obviously, the number of gate drives from a package output is directly dependent upon the current required per gate input. Therefore, it is particularly important that the lost charge be a minimum.

Since the reverse current is dependent to a large extent on the previous forward current, the magnitude of the noise at the "and" gate output is intimately related to the gate current I. To increase the frequency of operation of a package by a factor of two (or to increase the grid swing by a factor of two), all currents are increased by a factor slightly larger than two. Therefore, noise resulting from the reverse current of the pulsed "and" diode* is a function of frequency of operation. The advantage, then, in the small grid signal approach to the over-all problem, as far as diode transients are concerned, is that the diode currents are comparatively small, thus minimizing the effect of diode back-current.

The lost charge is of sufficient importance to use this measurement as a basis for the diode comparison. The following table is a ranking of the diodes tested. The lost charge has been taken as indicative of the transient properties. The remainder of this report will substantiate the superiority of the Hughes 2109. Therefore, other diodes have been rated as inferior to the 2109 if they have poorer forward conduction or a larger lost charge. The Hughes 2182 and Clevite 309 have been taken as representative of diodes with high forward conduction but inferior back-transient properties.

DIODES TESTED

Diode	Inferior to Hughes 2109	
	Statically	Transient
Raytheon IN295	x	
Hughes IN191	x	
Hughes HD2108	x	
Transitron S5G	x	x
Transitron IN251	x	x
Hughes IN629	x	x
Hughes silicon junction	x	x
Hughes HD2191		x
Radio Receptor type W		x
PSI silicon diffusion computor diode	x	x
Hughes IN117	x	x
Clevite CTP309		x
Hughes IN118		x
Raytheon IN306		x
Hughes 2182		x

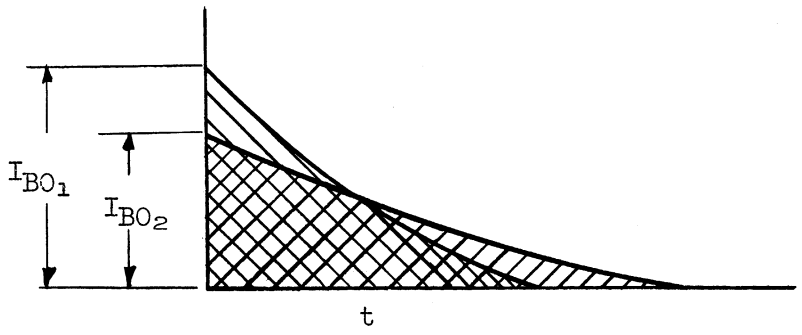
*The mechanism by which the "and" contributes to the noise at the "and" gate is considered in detail in Section 2.2.3.

(b) Effect of Back Bias on Reverse Recovery.

The simple model assumed for back-transient studies has no electric field in the end regions.* It can be seen that a reverse field would contribute to the removel of hole storage charge. That is, the initial reverse-current spike is higher for increased back bias.

If the duration of the switching pulse were much longer than the 50 μsec pulse used here, the areas under the reverse-current curves would be constant and the only effect of increased back bias would be to increase the initial reverse current I_{BO}.

$$E_{b_1} > E_{b_2} \qquad I_{BO_1} > I_{BO_2}$$



In Fig. 2.2-1 the initial back current and the current at 20 μsec after switching has been plotted for one of the Hughes 2182 diodes where the reverse current is significant and for the Hughes 2109 where it is not. Note that when the transient is significant, the initial back current increases as expected while the back current at 20 μsec becomes constant for $E_o > 6$ volts. The implication for gate operation is that the back-biased diode becomes approximately a constant current device. That is, regardless of the back bias the reverse current is essentially constant.

One definition frequently used for the recovery time of a diode is: that time required to obtain a specified back resistance for a given back-bias condition. This definition is somewhat ambiguous since the back resistance is more a function of the back bias specified than an indication of the true transient behavior. A measure of the time required for the diode to reach a back current of, say, 1 ma would perhaps be a more adequate definition of recovery time. The following tabulation for the Hughes 2182 illustrates this point.

*The end regions of a junction diode are shown in Fig. 2.1-1.

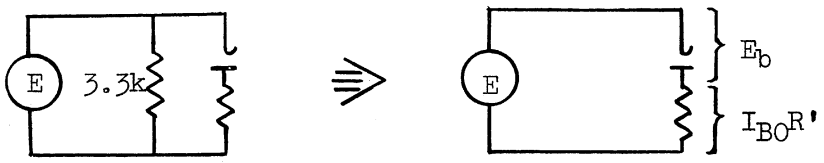
E_b	$R_B(t') = \frac{E_b}{I_B(t')}\ \Omega$
1/2	83
3	273
6	500
10	835
15	1250

$R_B(t')$ and $I_B(t')$ are the resistance and back currents respectively at 20 μsec. (See Fig. 2.1-1.)

Gate design and performance is intimately connected with the transmission of charge and therefore the most appropriate criterion of diode performance is the measurement of the "lost charge" that was discussed in connection with Table 2.2-I.

(c) Effect of Circuit Resistance in Series with a Back-Biased Diode

Another factor which can alter diode transient performance is the amount of impedance in series with the diode. In the previous sections resistance was added in series with the test diode to monitor diode currents. In some cases where relatively poor transient diodes were used (IN117), this small resistance coupled with a low back bias and large forward currents limited the reverse-current spike. The reason for this can be explained with the aid of the following circuit:



Unless $I_{BO}R' \ll E$, the series resistance may be sufficiently large to limit the reverse current. This limitation on the reverse current is quite common for junction diodes (see Section 2.1.3). The four photographs of Fig. 2.2-2 illustrate the contribution of series resistance. Note that when the back bias was increased to 4 volts, the 200-ohm resistance no longer limited the initial back current. In fact, if the scope did not mask the leading edge of the transient, the initial transient would be very large when the series resistance is zero. Certainly the series resistance then sets an upper limit on the initial transient spike.

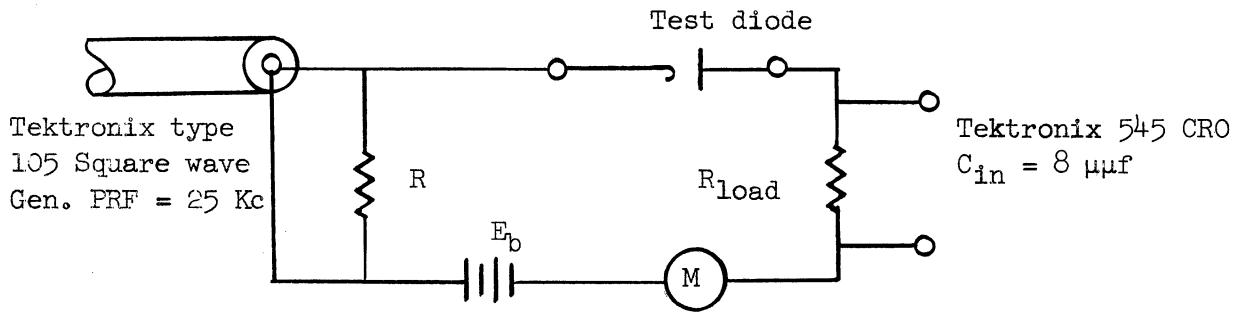
Note that in the logic circuit of Fig. 3.2-1 series resistance of the input and grid-clamp diode is zero. The series resistance of the back-biased "and" diode is to a first approximation the dynamic resistance of the unpulsed input-clamp and "and" diode in series.*

If now the diode has little or no lost charge, as is the case of the Hughes 2109, the effect of series resistance is certainly negligible. Therefore, it is reasonable to conclude for this application that the reverse current of good transient diodes is independent of series resistance even at small back-bias voltages.

(d) Back Recovery as a Function of Pulse-Repetition Rate.

The back transient is independent of the pulse-repetition frequency if the diode under test has had sufficient time to establish the steady-state minority-carrier gradient before being back-biased. If the pulse-repetition rate is such that the above condition is not satisfied, the magnitude of the reverse transient will be affected. This fact is illustrated in Fig. 2.2-3. The test circuit was pulsed with successive 50 μsec pulses at a 10 Mc repetition rate. The voltage developed across the 100-ohm resistance is indicative of the diode reverse current. Since the forward transient duration is 10 μsec or less for most diodes considered, it is possible to conduct gate tests using pulse-repetition rates lower than the basic clock frequency. This procedure is justified up to a frequency of 10 Mc.

In the preceding section the reverse transient was investigated using a 50 μsec pulse. During the initial phase of this project, the reverse transient measurements were taken on the circuit shown below. These test results have been included to augment data in the preceding section. For some diodes, the reverse transient persists for times greater than 50 μsec. Therefore, testing with a 25 Kc square wave allowed observation of the complete back transient.



A 25 Kc square wave was used as the input signal and the back bias

*The justification of this statement is included in Appendix C.

was varied by changing E_b. The forward current through the diode was varied by changing the amplitude of the input signal. An approximation of the forward current was read on an average current-reading meter. The current read on the meter is a good approximation of the forward current because the average of the reverse current through the diode over half a period is negligible compared to the average forward current. The data taken were as follows:

(a) Reverse current at t = .05 μsec.
(b) Time for reverse current to reach 5 mils.
(c) Ratio of initial reverse current to forward current (called the a/b ratio).
(d) Initial back current.

These tests were run using two different values for the back bias, namely, -1.5 and -3.0 volts, and different forward currents.

The back transient test circuit, wave shape, and results are shown graphically in Figs. 2.2-8 to 2.2-16. There is good agreement between the data in these figures and that in Table 2.2-I, with one exception. There is an apparently gross disagreement on the characteristics of the HD2182 diode. Actually this disagreement is the result of testing two different groups of HD2182 diodes. One group consistently exhibited poor transient characteristics while the other group exhibited characteristics comparable to those of the good HD2109 diode. This is a good arguing point for user tests.

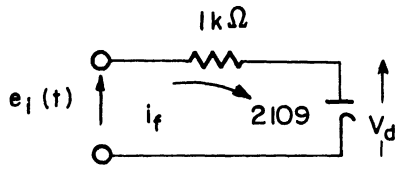
2.2.2 Forward transients.—For diodes of the quality used in typical gating circuits, the forward transients have a negligible effect. To investigate the characteristics of the forward transient, a Textronix 545 oscilloscope with a rise time of 12 mμsec was modified by bypassing the furnished vertical amplifier and using instead two cascaded distributed amplifiers (Hewlett Packard 460A and 460B), each with a band-width of 140 Mc. The overall rise time of the probe, amplifiers, and 545 CRT plates is approximately 6 mμsec.

The forward transient test circuit and the resulting data are shown in Fig. 2.2-17. The voltage developed across the load resistor is an indication of the forward current. Notice that the significant portion of the forward transient is over in less than 10 mμsec for the HD2182, CTP309, Ray 295, and HD2109. A poor forward transient diode, the Hughes 117, has been included to illustrate the contrast between good and poor transient diodes.

It follows from Fig. 2.2-17 that the HD2109 and Ray 295 will function well as grid-clip diodes. Clip, clamp, and limiter are words used interchangeably in connection with a pulsed circuit. Here (Fig. 3.2.1a) Diode F is used to clamp the grid at - 1/2 volt and Diode G clips the positive swing of the grid signal to + 1/2 volt. Figure 2.2-18 shows the various diodes used as clips (Diode G) in the package of Fig. 3.2-1a. Note the consistency of re-

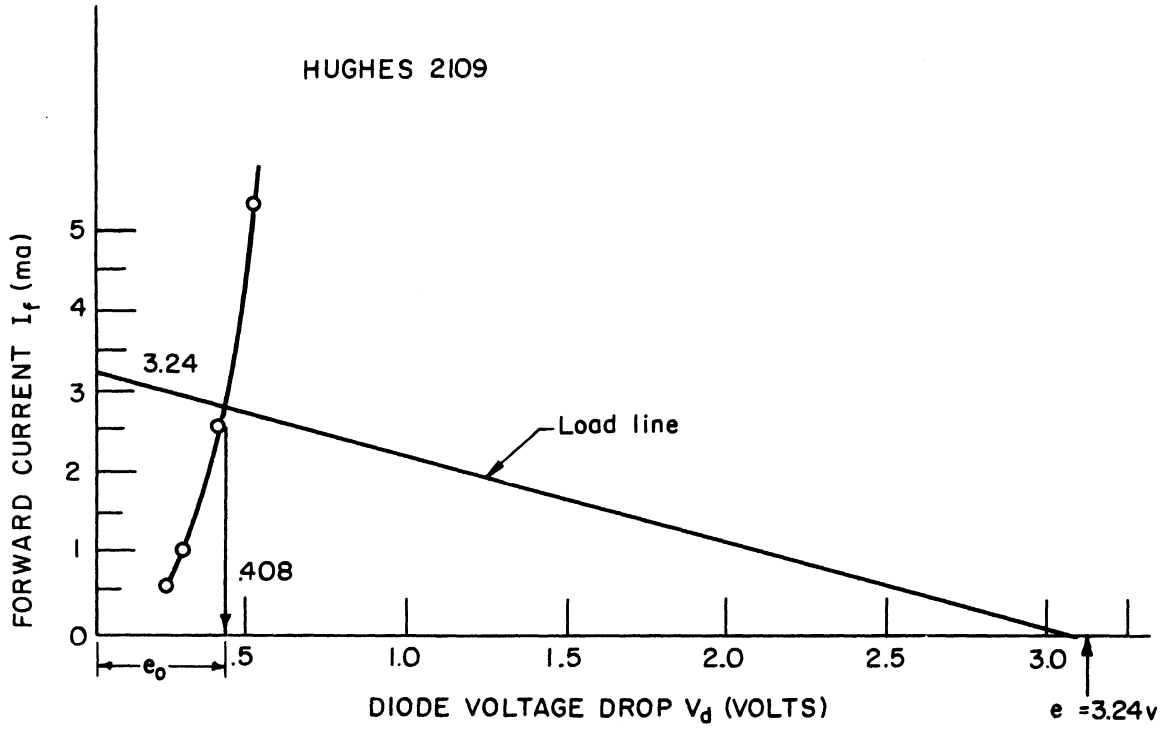
sults of Figs. 2.2-17 and -18.

A somewhat different situation is encountered when a diode is being used to clip a sine wave. It is observed that a good forward transient diode will not clip a sine wave but will only reduce the amplitude of the input signal. In Fig. 2.2-19 the dependence of the clipped wave-shape on the diode static-characteristic is shown. A sample computation for the case when the input voltage is equal to 3.24 volts is shown below. It is the nonlinear portion of the 2109 characteristic that is responsible for the rounded response. Improvement of output wave shape could be obtained by increasing either e_{in} or the series resistance or both.



$$e_i(t) = i_f R + V_d$$

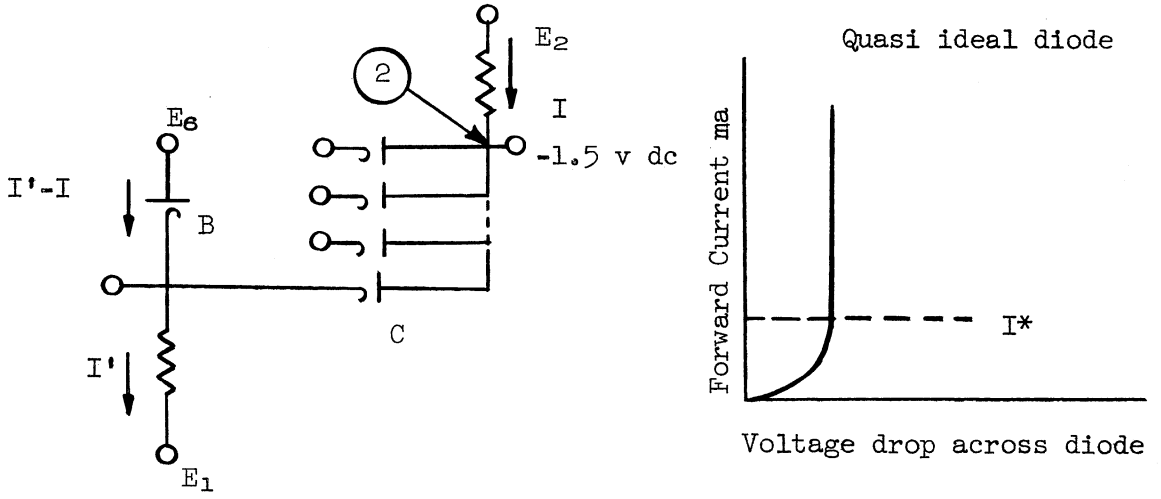
$$t = 15 \text{ μsec}, \; e_i = 3.24$$



2.2.3 Static forward characteristics.—The two major problems associated with gating structure are (1) noise when all but one of the "and" inputs are pulsed and (2) the availability of grid-capacitance charging current when all inputs are pulsed. It is necessary to consider both static and dynamic diode characteristics if noise is to be minimized. In this section the importance of static characteristics as related to static noise will be pointed out. Static noise is defined as the d-c level change in the quiescent condition at the "and" output and the dynamic noise is the component of noise resulting from the reverse-current surge from the pulsed "and" diodes.

$$\text{Total noise} = \text{Dynamic noise} + \text{Static noise}$$

Two examples, (a) and (b), will illustrate the importance of diode static characteristic to gate noise.



(a) Consider an "and" gate for which (n - 1) of the n inputs have been pulsed. The input clamp diodes have been assumed to be quasi-ideal (the quasi-ideal diode characteristic is shown above) while the "and" diodes (C) have realistic characteristics. The current through the input clamp is a minimum when all but one of the inputs are pulsed. If $I' - I \geq I^*$, the voltage drop across the input clamp will be constant.

The voltage supply E_6 necessary for point (2) to be at -1.5 volts is $E_6 = -1.5 + V_{\bar{c}}$. If (n - 1) gates are pulsed, the drop across the "and" diode will be $V_{\bar{c}} + \Delta V_c$ as the nonpulsed "and" diode is now passing the entire gate current I. The new d-c level at point (2) E_2' is given by

$$E_2' = E_6 - V_c$$

$$E_2' = E_6 - (V_{\bar{c}} + \Delta V_c)$$

$V_{\bar{c}} = -|V_{\bar{c}}|$ = voltage drop across the "and" diode when passing a current I/n.

The static noise is then the difference between E_2' and -1.5 volts.

$$\text{Static Noise} = -1.5 - E_2'$$

$$\text{Static Noise} = -1.5 - [E_6 - (V_{\bar{c}} + \Delta V_c)]$$

$$\text{Static Noise} = -1.5 - (-1.5 + V_{\bar{c}}) + V_{\bar{c}} + \Delta V_c$$

$$\text{Static Noise} = \Delta V_c$$

ΔV_c is the difference in the voltage drop across the unpulsed "and" diode when the current through it changes from I to I/n. As the number of gates approach infinity, $V_{\bar{c}}$ approaches zero and ΔV_c then is the voltage drop across the diodes when passing the gate current I. This then establishes a lower limit for the noise clipping needed for an infinite number of "and" gate inputs.

A tabulation of this minimum noise for four diodes is included below.

Minimum Noise for an n Input and Gate
(n = ∞) and gate current I(ma)

Diode	4 ma	8 ma	12 ma
309	.35V	.39V	.415V
2182	.36V	.40V	.44V
2109	.44V	.545V	.625V
295	.5V	.66V	.85V

(b) Now consider the case where the clamp diodes also have realistic characteristics. It can be shown that:

$$\text{Static Noise} = \Delta V_B + \Delta V_c \text{ ;}$$

ΔV_B = the incremental potential drop due to the finite slope of the input clamp characteristics.

If the minimum current I* (Fig. 2.2-5) is above the knee of the static curve, ΔV_B will be much less than ΔV_c when I/n is small (1 ma) even when Diodes B and C are identical. Two conclusions can be drawn regarding the effect of static characteristics on gate operation. First, the static characteristics of particularly the "and" diode contribute appreciably to the total noise when n is large. Second, it may not necessarily be desirable to reduce

the gate current I in an effort to reduce transient effects.

Figure 2.2-4 illustrates the agreement between actual gate performance and calculations made from the diode static characteristics. An estimate of the total noise was made by assuming each of the pulsed "and" diodes supplied an additional current I_{BO} to the unpulsed "and" diode. The total current to the unpulsed "and" diode during the first instant is equal to $I + (n - 1)I_{BO}$ where I_{BO} is a function of the forward current $I_f = I/n$. The requirement for the minimum input clamp current of the unpulsed "and" diode, if capacitance is neglected, is given by:

$$I' - I - (n - 1)I_{BO} \geq I^* \quad .$$

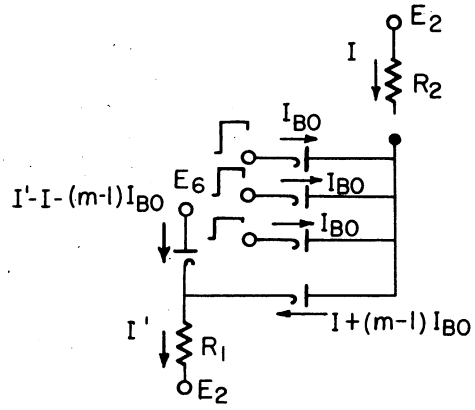
However, capacitance is certainly not negligible and a large portion of the initial back current goes into the capacitance at points (2) and (3). In fact, dynamic noise is to a certain extent reduced by capacitance at point (2). A sample computation for a five input "and" gate using 2109's as input clamps and "and" diodes is shown on the next page. The values used for $I_{BO} = f(I_f)$ were obtained from Fig. 2.2-15.

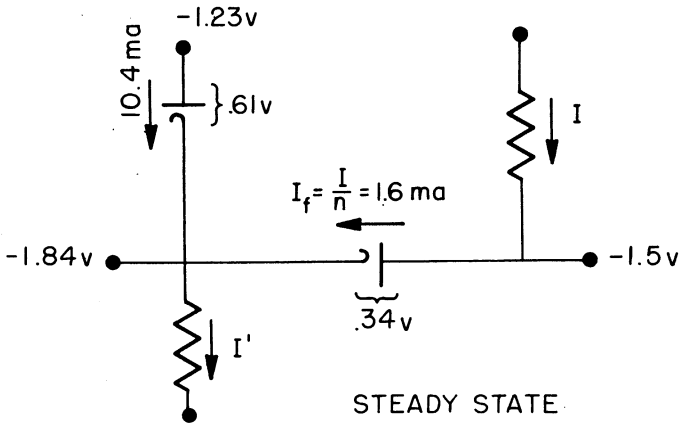
A number of diodes have been tested for static forward characteristics. Figures 2.2-5 and 2.2-7 are plots of the average characteristics. The diodes of Fig. 2.2-5 have been taken as representative of those tested both with regard to transient and static characteristics. Figure 2.2-6 gives an indication of the consistency of static characteristics within a batch.

2.3 DIODE SPECIFICATION

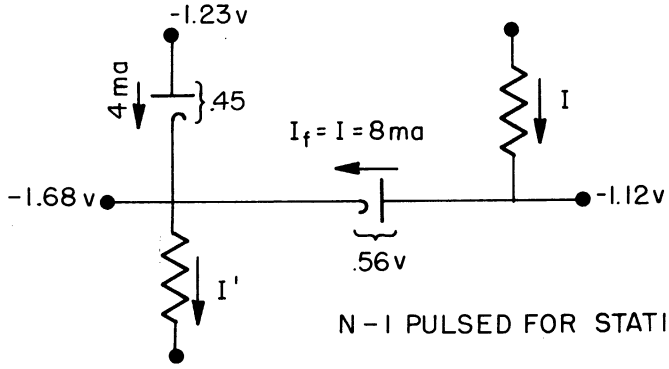
The information of the preceding sections provides a basis for predicting diode performance in any particular logical circuit. The following sections emphasize the relationship between diode characteristics and operational details of a diode gating circuit. The experimental results of testing a clocked and unclocked package are included. Finally, an experimental correlation between static and dynamic characteristics is drawn to show their close relationship.

2.3.1 Diode requirements.—In general, the two major considerations in gate design are noise and the effective use of available gate current. Both factors depend primarily on the diode back-transient characteristics. A typical "or"-"and"-"or" gating configuration is shown on page 27. The previous material on diode transients provides a theoretical basis for diode assignment to the various positions A to F. The experimental testing in the following Sections 2.3.2 and 2.3.3 substantiates these diode requirements.

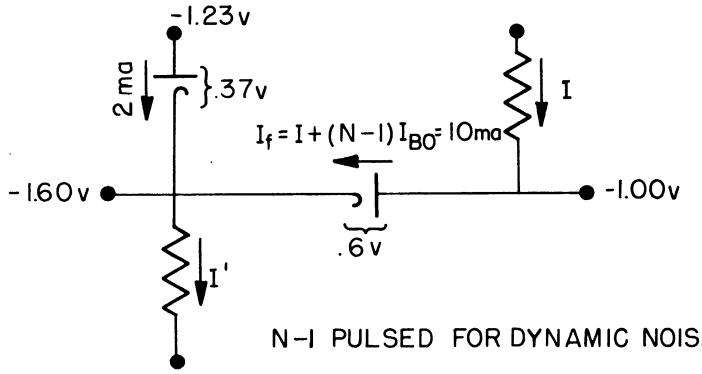




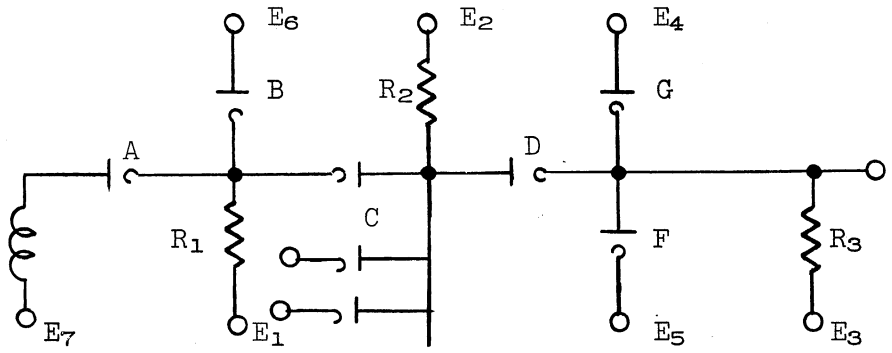
STEADY STATE



N-1 PULSED FOR STATIC NOISE



N-1 PULSED FOR DYNAMIC NOISE



(1) The "or" Diodes A and D require high forward conduction. For frequencies below 10 Mc forward transient are of negligible importance. One would anticipate that the back transient of the "or" diodes would not be objectionable. However, experimental results will show later that the grid "or" Diode D must have the best possible back-transient properties while the back transient of Diode A is not critical.

(2) It is desirable that the input-clamp Diode B and the "and" Diode C have a minimum back transient "lost charge." The importance of the static characteristics of this diode pair has already been pointed out.

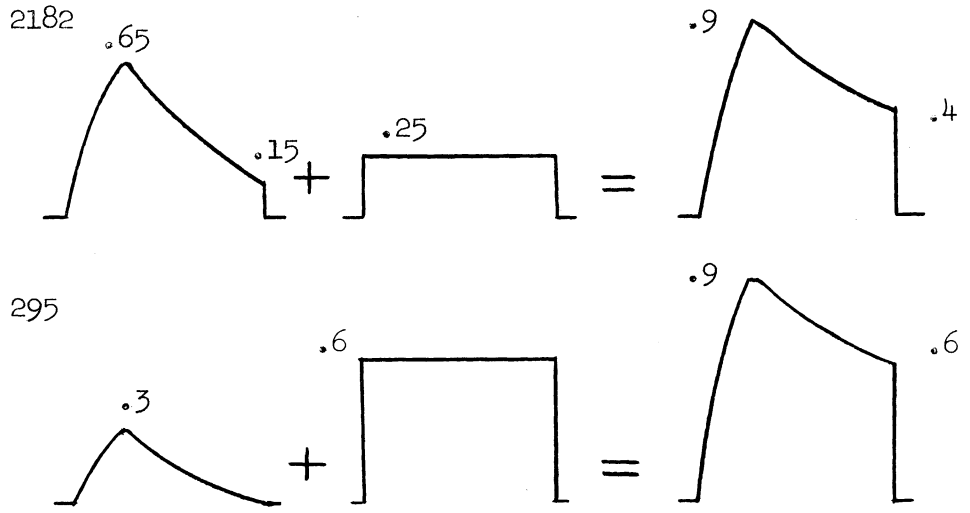
(3) The grid-clamp Diode G is required to have good back-transient properties as current lost through this diode represents a loss of grid-capacitance charging current.

(4) Diode F is required to clip the grid signal. In Section 2.2.2 it was shown that Diode F may be a good clip in this situation despite poor transient properties. In fact, the forward drop across this diode may be used to advantage to eliminate the use of the E_5 supply. What is actually desired in all cases is a diode which is as nearly ideal as possible. The following tests will outline the criteria for choosing diodes. They will point up the fact that because of the nonideal characteristics it is best in all cases to use diodes with good transient properties with high forward-conduction as a secondary consideration. Of those diodes tested the Hughes 2109 stands out as best fitting this criteria.

2.3.2 Experimental testing, unclocked.—The diode requirements outlined in the previous section may be verified by comparative testing of diode types at various positions in the package. The gate in Fig. 3.2-1a has been designed for 10 Mc operation. Fifty μsec pulses have been applied to this circuit at a 60-cycle repetition rate. The results and conclusions of comparative diode testing are summarized below.

It is desirable that the input clamp diode have both good transient and static characteristics. The Hughes 2109 best fulfills this requirement. The

best "and" diode is considered to be the one which contributes the least noise. The total noise has been defined as the additive combination of the static and dynamic noise. The results of comparative tests are shown in Table 2.2-II. Note that in the case of the 309 and 2182 diodes the experimental and computed static-noise levels differ widely. This is not surprising as these relatively poor transient diodes have considerable reverse transient current flowing at the end of a 50 μsec pulse even for small forward currents (see Figs. 2.2-9 and -10). It is possible to have the same total noise for a number of combinations of reverse current and static characteristics as shown below. Of the diodes tested, the Hughes 2109 gives the best performance.



Noise composition

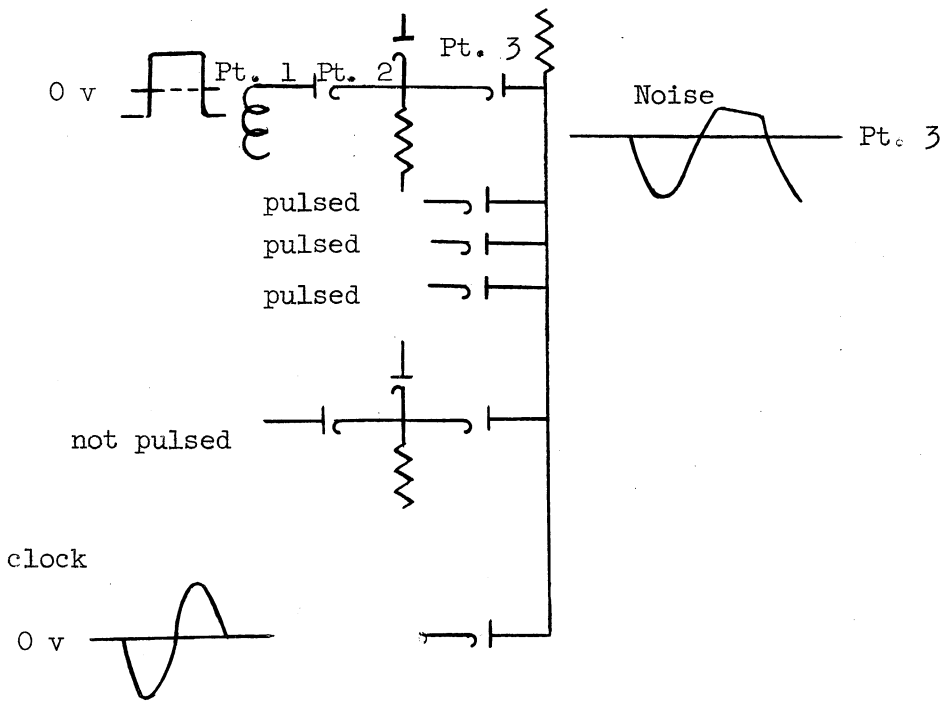
Experimental results have shown that it is necessary to increase the input gate current I' when inferior transient diodes are used in the "and" position. The surge of reverse current to the unpulsed input clamp may be sufficient to cut the n^{th} input off.

There are no situations in which a poor transient diode would intentionally be used as an "and" diode. However, the presence of the reverse current does assist in charging the grid capacitance when <u>all</u> the n inputs are pulsed.

The experimental measurements pertaining to the performance of the grid-clamp diode G are shown in Fig. 2.3-1. As previously stated, this diode must have excellent back recovery characteristics. The forward conduction is of minor importance, as the supply voltage may be adjusted to give the desired tube bias. In this particular application (Fig. 3.2-1a), it is desirable to use the steady-state drop of the 2109 to establish the grid bias of -.45 to -.5 volt by tying the diode plate to ground and thereby eliminating the E_4 supply.

The experimental results pertaining to the grid-clip Diode F were discussed in Section 2.2.2 under forward transients (Fig. 2.2-18). In the 10 Mc gate of Fig. 2.2-1a a grid swing of 1 volt was specified. The desired bias condition of -.5 to + .5 volt may be obtained by tying the cathode of the clip diode and plate of the clamp diode to ground. The 2109 has been chosen for both these diode positions because of its transient properties and not on the basis of its forward conduction for a particular application.

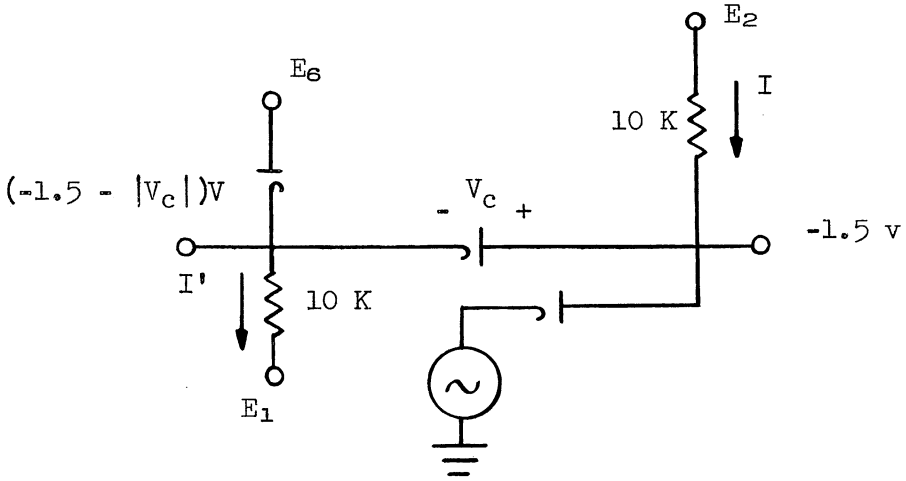
2.3.3 Experimental testing, clocked.—



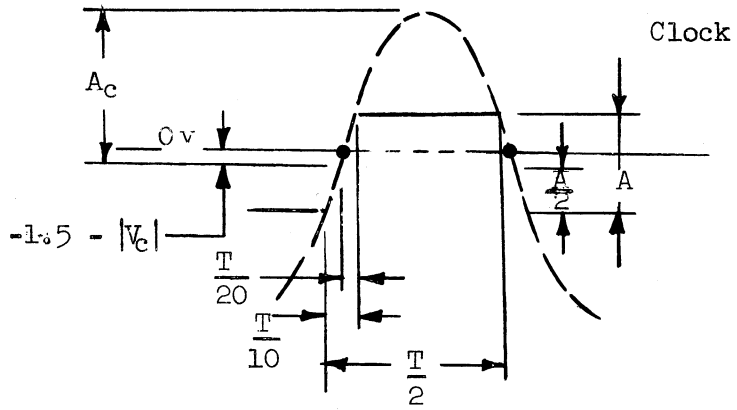
The introduction of a clock signal into the gate circuitry has the following additional features. Since a clocked system is always multiple phase, the first level logic (input "or") always reaches maximum amplitude prior to the clock-pulse-rise. Noise resulting from the reverse current of the pulsed "and" diodes is therefore completely eliminated because the pulsed "and" diodes have not experienced a forward current just prior to the pulse. The reason for this is that point (3) in the above figure has been pulled negative by the clock and has back-biased the "and" diodes. The noise phenomenon is now a function of the static properties of the unpulsed "and" diode and the reverse transient current of the clock diode.

Noise at point (3), resulting from the addition of the static noise ($\Delta V_B + \Delta V_C$) and the back-transient noise of the clocked diode, is the factor limiting high-frequency gate operation. At present the tube and transformer have placed the upper limit for practical operation at about 7 Mc, thus making a legitimate test using high pulse-repetition rates impossible above 7 Mc.

To circumvent this frequency limitation a simulated gate has been used and operated at clock frequencies from 5 to 20 megacycles. The circuit is shown below.



The clock (the voltage source shown) is an electron-coupled oscillator, operating class C. The wave shape of the clock signal with reference to the signal pulses is important for effective gating. Notice in the figure below that the steepest portion of the sine wave or clock signal is used for wave-shaping. The information pulse is required to rise and fall to amplitude A in T/10 where T is the clock period.



The amplitude of the clock pulse is given by

$$A_c \sin \frac{2\pi}{20} = A/2$$

$$A_c = \frac{A}{2} \frac{1}{\sin 18^\circ}$$

$$A_c = 1.618A \ .$$

The voltage about which the clock is centered is given by:

$$\text{Clock center voltage} = -1.5 - V_c + A/2 \ .$$

Taking the 10 Mc gate of Fig. 3.2-1a as an illustrative example, the clock centering voltage is:

$$V_c = .34 \text{ volt}$$

$$A = 3.5 \text{ volts}$$

$$\text{Clock centering} = -1.5 - .34 + 1.75 \text{ volts} = -.09 \text{ volt.}$$

There is little error in centering the clock voltage about ground as is done in the test circuit.

The amplitude of the clock is then given by:

$A_c = 1.618A = 5.67$ volts. (6.00 v used in test)

As the frequency of operation increases, the gate current I must increase to charge the circuit capacitance in the manner prescribed by Equation (2) of Section 1.3. The circuit of Fig. 3.2-1a is taken as a typical 10 Mc gate and is used as the basis for the following formulation.

Let $I' = I + 4$ ma.

Then based on the conditions given above:

$$I = \frac{4}{5} f,$$

f = clock frequency in Mc, and
I = gate current in ma.

Test results at 5 Mc (Fig. 2.2-4) show a noise voltage of .54 as compared to .55 volt (Fig. 3.2-2a) for the unclocked case at 10 Mc. The clock diode has had a forward current history (8 ma) which is roughly equivalent to the sum of the forward currents of the 4 pulsed diodes of Fig. 3.2-2a. It is anticipated then that the total resulting noise voltage will be equal for the two cases. The dynamic noise ϵ resulting from the back transient of the clock diode has been added to the computed static noise for the case where 4 or 5 inputs are pulsed. The data for the 295 show the dependence of total noise on diode static characteristics as the 2109 and 295 have equivalent back-transient properties with the 295 having inferior static characteristics.

Test results at 5 Mc (Fig. 3.2-2b) show the noise at point (3) to be approximately equal to the static drop across the unpulsed diode if the information pulse leads the clock by T/10 seconds. It is still necessary that "and" diodes have good reverse-transient characteristics but for a slightly different reason than in the unpulsed case. Consider a situation where none of the inputs has been pulsed. Each "and" diode will then send a surge of reverse current to point (3) at the termination of the clock pulse. Noise at any time during the clock cycle is objectionable. However, it is the back-transient properties of the clock diode that are particularly critical.

2.3.4 Experimentally observed correlation between static characteristics and back-transient properties.—The previous discussion has been concerned with diode characteristics; the forward conduction is measured statically and the back transients are measured dynamically. The back transient has been characterized by the amount of lost charge. It is known from manufacturing techniques that these characteristics are basically opposed. To obtain a high conduction it is necessary to use either a large junction area or high impurity concentration. Both of these factors contribute heavily to diode reverse-current. Figure 3.2-2 indicates the relationship between conduction and the reverse transient lost charge. The dynamic forward resistance $\partial V_d/\partial I_f$ vs the lost charge (for I_f = 9 ma) has been plotted for those diodes which have been tested. It should be pointed out that the number of diodes constitutes a small sample and the diodes obtained tended to represent the best available products of the manufacturers contacted.

It is obvious that the most desirable diode is that one which comes closest to realizing ideal diode properties. However, due to the aforementioned qualities of commercially available diodes, it is evident that a choice must be made between good forward conduction and good transient properties. It is the opinion of the authors that it is necessary to have back-transient properties equivalent to those shown for the Hughes 2109, giving diode static characteristics secondary consideration. The Hughes 2109 represents the best compromise of the diodes tested to date.

3. GATE STRUCTURE PERFORMANCE

In this section, the performance of two experimental packages is considered. The first is designed for 10 Mc operation and the second is an operational package for 5 Mc operation. The 10 Mc circuit of Fig. 3.2-1a has been tested on a single-pulse basis. Although a more complete test with a continuous chain of 50 mμsec and a clock would have been desirable, tube and transformer studies have shown operation at a 10 Mc repetition rate to be impractical. Figure 2.2-3 verifies the assumption that diode transients are unaltered by a 10 Mc pulse repetition rate. Therefore, the single-pulse test results are indicative of actual operation at 10 Mc.

A 5 Mc package (Fig. 3.2-1b) has been tested under legitimate operating conditions. The specification of voltage and current magnitudes and a summary of the gate performance is covered in the two succeeding sections. The remaining sections discuss the effect of tube grid characteristics upon the grid signal wave-shape and finally the upper limit of gate performance.

3.1 SPECIFICATION OF LEVELS AND CURRENTS

In this section the design specifications for a 10 Mc gate (Fig. 3.2-1a) and 5 Mc gate (Fig. 3.2-1b) are discussed.

(a) Currents - Fig. 3.2-1a.

A discussion of the input logic stage is dependent upon the tube-transformer configuration only to the extent that the bias levels and grid capacitance must be known. In this particular example, a grid swing of 1 volt and an effective total grid capacitance of 30 μμf has been used as the basis of computation. Assuming a value of 5 μμf for C_1, the gate current I can be computed from Equation (2) of Section 1.3.

$$I = \frac{(E_g + E_N)C_1}{\Delta t} + \frac{E_g C_g}{\Delta t} + I_3 \quad ,$$

where

E_g = grid swing = 1 volt,
E_N = noise clipping = 1 volt,
C_g = 30 μμf,
C_1 = 5 μμf,
$I_3 = \frac{E_g C_g}{\Delta t}$ = grid pull-down resistor current, and

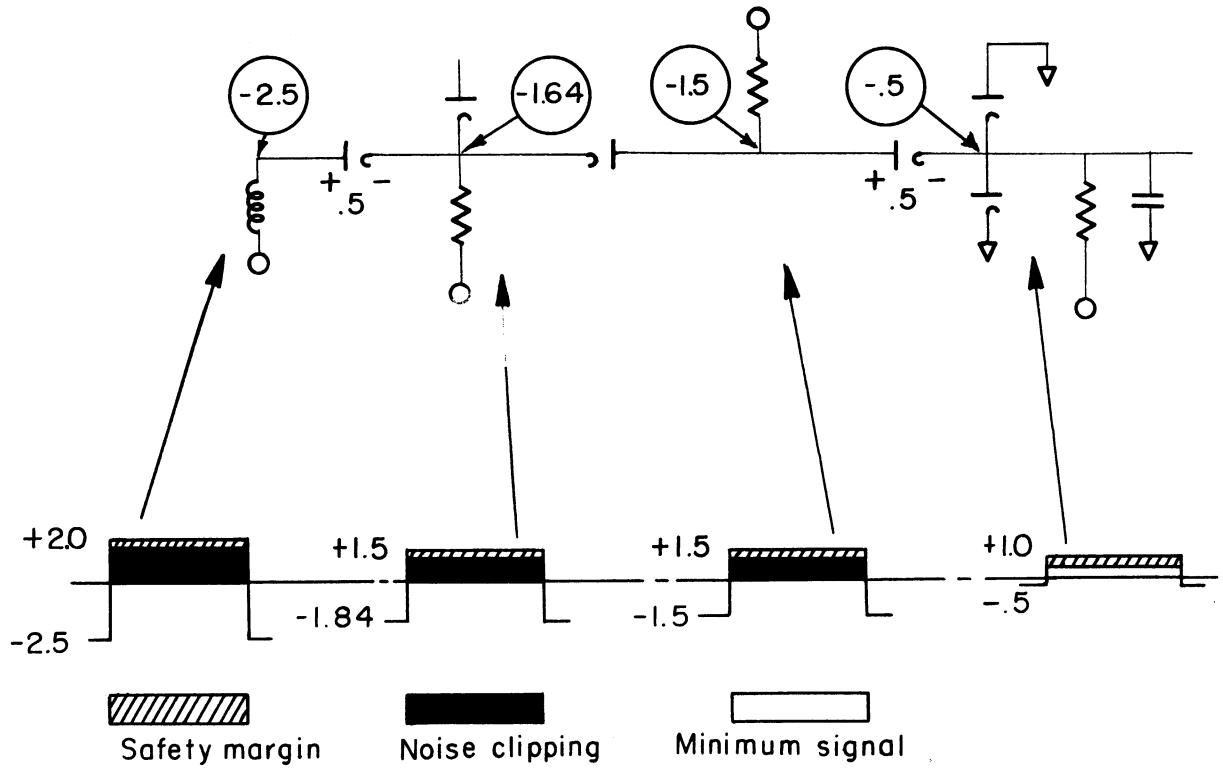
$\Delta t = \frac{T}{10}$ = 10 mμsec;

I = 7 ma.

An estimate of the average current lost in the grid-clamp diode may be made from Fig. 2.3-1 (about 1 ma). Therefore, to insure sufficient current to swing the grid, 8 ma has been used. An input gate current of 12 ma has been found satisfactory.

Levels: Fig. 3.2-1a

If "and" diode limiting is to be avoided, the level at which "and" limiting would take place must be greater than the grid clipping level by some factor of safety. Since the drop across the "or" diodes can be expected to be from .4 to .5 volt, the minimum amplitude of the gate input E_o can be established. To insure no "and" limiting of the grid signal, a .5 volt safety factor is assumed. The following sketch shows the composition of the informa-



tion pulse at the various points in the circuit. The noise clipping levels on the input and grid "or" diodes can be increased or decreased as justified by environmental tests. The levels shown have been found satisfactory in the work to date.

(b) Currents - Fig. 3.2-1b.

Figure 3.2-1b is illustrative of gate performance at 5 Mc. The 436A requires a grid swing of -2.0 to 2.0 for optimum tube-transformer performance. The effective grid input capacitance is 20 μμf. The gate current I is given by:

E_g = 4 volts
E_N = 2 volts
C_g = 20 μμf
C_1 = 5 μμf

$$I_3 = \frac{E_g C_g}{\Delta t} = \text{grid pull-down resistance current}$$

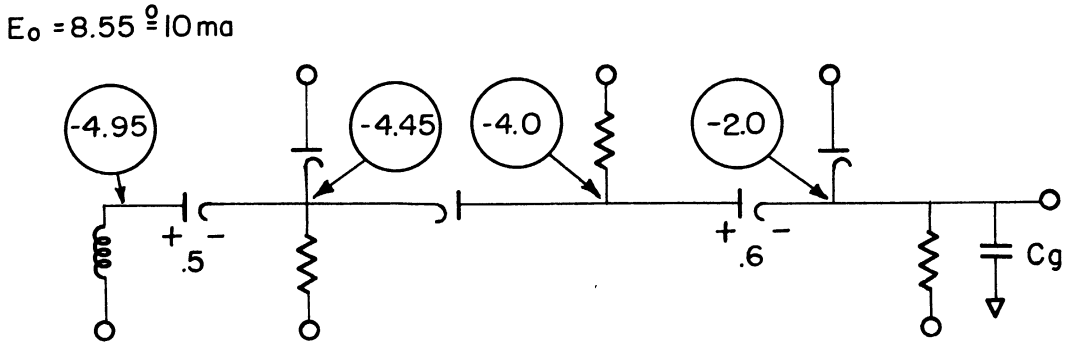
$$\Delta t = \frac{T}{10} = 20 \text{ μsec}$$

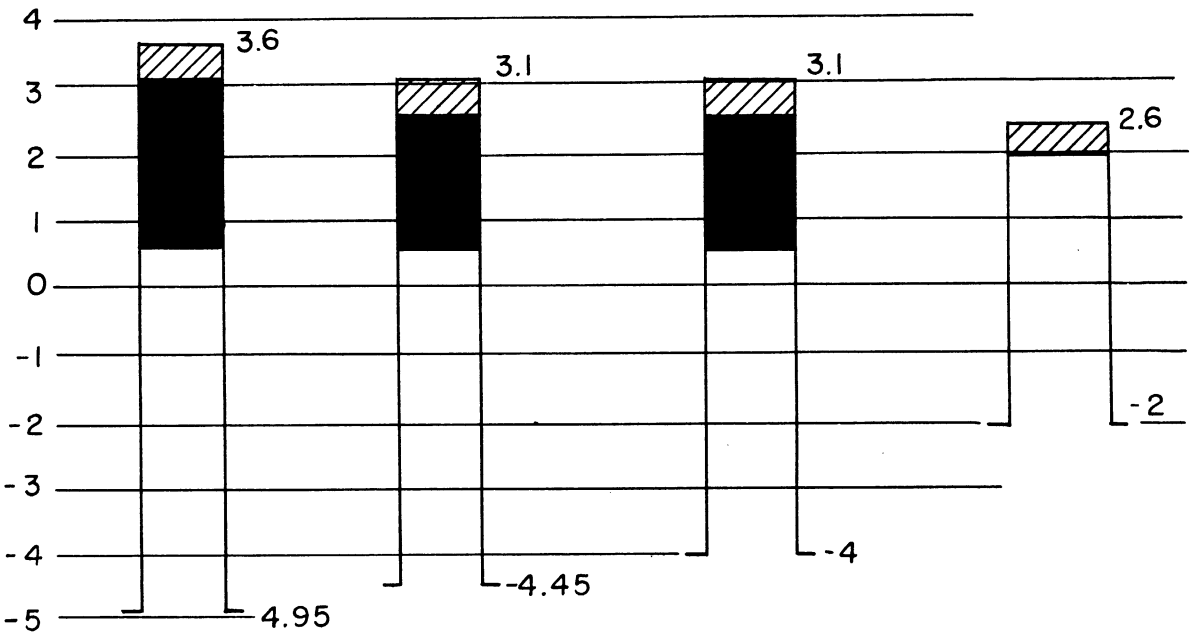
$$I = \frac{(E_g + E_N)C_1}{\Delta t} + \frac{E_g C_g}{\Delta t} + I_3$$

$I = 9.5 \triangleq 10$ ma
$I' = 14$ ma

Levels: Fig. 3.2-1b

Notice that a grid-clip diode has not been included; the 436A grid is an effective clip as the grid characteristics limit the signal at the desired level (+ 2.0 volts). It is therefore necessary that "and" diode limiting below + 2.0 be avoided. The noise clipping levels indicated are conservative and may later be reduced.





3.2 GATE PERFORMANCE

In this section the performance of a 10 Mc gate (Fig. 3.2-2a) and a 5 Mc gate (Fig. 3.2-2b) is discussed. It is desirable to assign a figure of merit or efficiency to a circuit. Let gate efficiency E be defined as the product of current efficiency A and voltage efficiency B.

$$E \equiv \frac{A\,B}{100} \%$$

$$B \equiv \frac{E_g}{E_o} \times 100 \text{ voltage efficiency}$$

$$A \equiv \frac{I/2}{I''} \times 100 \text{ current efficiency}$$

$$I'' \equiv I' + I_B \text{ (Diode B)}$$

The voltage efficiency B is the ratio of the grid swing E_g to the amplitude of the input signal required for satisfactory gate operation. The current efficiency A is defined as the ratio of current required to charge the grid capacitance C_g to the gate current necessary to drive one "and" input. The current needed to drive a gate is the "and" pull-down current I' plus the reverse current of the input clamp diode.

Figure 3.2-1a

Computation of Gate Efficiency.

E_o = 4.5 volts
E_g = 1 volt
I = 8 ma
I' = $I' + I_{B(\text{average})}$ = 12 + 2 = 14 ma
Then A = 22.2%
B = 33.3%
E = 7.4%

The term gate efficiency should be used with caution, as the same gate with different values of grid swing and capacitance will have a different efficiency. For example, consider the same circuit with a grid swing of 2 volts.

E_o = 5.5 volts
E_g = 2 volts
I = 16 ma
I'' = $I' + I_B$ = 20 + 3 = 23 ma
Then A = 36.4%
B = 34.8%
E = 12.65%

Gate efficiency is improved by decreasing grid capacitance, noise clipping, and the input current I".

Wave Shapes.

The first four photographs in Fig. 3.2-2a show the wave shape of the signal as it progresses through the unclocked package when all inputs are pulsed. The delay (4 μsec) of the pulse from the input to the "and" [point (2)] to the grid [point (4)] as shown in the next photograph. The time delay is due to the finite time required to charge the circuit capacitance. The noise resulting at the "and" output [point (3)] when different combinations of "and" inputs are pulsed is shown in the last four photographs. The negative undershoot at the termination of the noise pulse is primarily the result of the back transient from the input "or" diode. A high conduction "or" has been used to minimize the drop across the input "or" diode with little regard given to its transient properties. It is felt that the resulting negative undershoot is not objectionable and therefore the relatively poor back-transient properties of this diode can be tolerated. The effect of small variations of the input-pulse amplitude E_o and the gate current I on the noise is shown in Table 3.2-I. It is observed that the total noise is only slightly affected by an increase of E_o and I.

Figure 3.2-1b

Computation of Gate Efficiency.

E_o = 9.0 volts
E_g = 4.0 volts
I = 10 ma
I" = I' + $I_{B(average)}$ = 14 + 2 = 16 ma
A = 31.3%
B = 44.5%
E = 13.8%

Wave Shapes.

Typical pulse wave-shapes and levels are shown in Fig. 3.2-2b. The events indicated in the time sequence can be quickly summarized as follows:

(1) The output of the previous package (No. 2) arrives before the clock (No. 1) by 20 μsec.

(2) If all inputs are pulsed, point (3) rises with the clock and falls with the earliest input (No. 4). The negative swing results from the back transient of the input "or" diodes. A CTP309 has been used as the input "or" diode for its high conduction property (despite its poor back-transient characteristics). If the undershoot is undesirable, the CTP309 diode can be replaced with a Hughes 2109. The portion "A" of (No. 4) is the level of point

(3) when the clock is positive and none of the "and" diodes is pulsed.

(3) The grid signal (No. 6) rises with point (3) (a slight delay results from the 2 volts of noise clipping) and falls when the clock pulls the regenerative gate down. Notice that the grid signal did not reach + 2.0 volts because point (3) was about +1 volt during the latter portion of the pulse. "And" limiting has taken place, thus emphasizing the importance of the trailing edge of the input pulse.

(4) When point (3) falls, the "and" gate grid "or" diode experiences a back transient which pulls the grid signal slightly negative despite the effort of the regenerative gate to hold the grid up (No. 6). The back transient of an "or" diode at this time is particularly undesirable. Therefore, the 309 diode was dropped in favor of the Hughes 2109 for use as the grid "or" diode.

The delay δ' from the grid to output is 28 mμsec. This may be reduced by approximately 10 mμsec, if the grid is driven to + 2.0 volts. The package delay δ measured under this condition is 34 mμsec. All measurements were taken with a Tektronix 545.

The noise indicated in No. 9 has been obtained using Hughes 2109 diodes of the quality shown in Table 2.2-I (I_{BO} = 1 ma). A recent order of one hundred 2109's has the following distribution of initial back currents:

I_{BO} (ma)	1	2	3	4	5	6
Number of Diodes	8	37	37	13	5	0

at I_f = 9 ma
E_B = 1.5 volts.

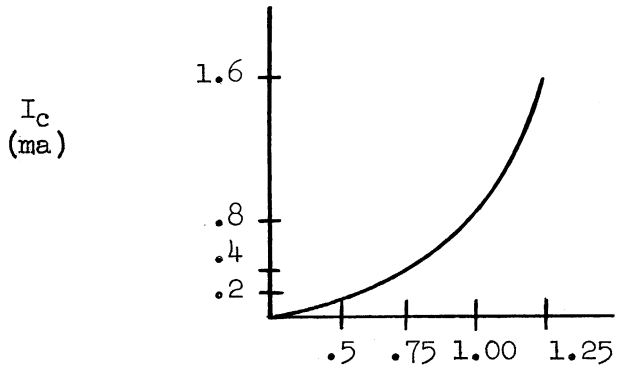
The diodes used for tests in this report have been taken from the initial shipment of 2109's received. An increase in noise of about 1.0 to 1.3 volts can be expected with inferior 2109's. It is essential that all "and" diodes and grid "or" diodes be tested with a circuit of the type used in Table 2.2-I before use in a package if the noise level is to be maintained at .5 to .8 volt.

3.3 EFFECT OF GRID CURRENT ON GRID WAVE-SHAPE

Under certain operating conditions, the tube grid can be used to clamp the grid signal. This can be brought about by driving the grid positive and drawing grid current. For example, the cascoded 437A's of Fig. 3.2-1a will clip the grid signal at +2 volts, thus eliminating the need for Diode F if it were desirable to push the grid that much positive. In Fig. 3.2-1b the grid-clip diode has been eliminated as the clip function is performed by grid to

cathode "diode" of the 436A. In any case, the gate current lost to the tube grid should be considered. In this particular case, if the grid is swung from -1/2 to + 1-1/2 volts, the grid characteristics will contribute to the clipping action. However, for a grid swing of -1/2 to +1/2 volt, grid characteristics have no effect on the grid wave-shape.

Grid characteristics for cascode 437A's



E_b = 66 volts on lower tube

3.4 UPPER LIMIT OF PERFORMANCE

Results to date indicate that the tube-transformer combination and/or delay lines will be the factors limiting high-speed operation. Therefore, it is desirable to divorce the input logic stage from the remainder of the package and outline those factors that would limit the operation of the input circuitry. Gate performance is directly related to the diodes employed and therefore any remarks must be necessarily restricted to current diode development. The factors limiting gate operation are (a) noise and (b) input gate current I".

In Section 2.3.2 noise has been measured as a function of clock frequency. It was assumed that the grid swing and noise clipping level was maintained constant as frequency of operation was increased. That is, the gate current doubled for an increase in frequency by a factor of two. The above assumptions are unrealistic for two reasons. (1) The noise clipping levels must increase as the frequency (gate current) increases due to the increased reverse current of the gate diodes, and (2) the grid swing will not necessarily remain constant. Both of these factors will result in larger gate currents than have been assumed here. It is difficult, however, to anticipate the contribution of these factors from data taken at 10 Mc. Therefore, the data in Fig. 3.2-1 represent the lower limit of noise voltage, since it has been assumed that the grid swing and the noise clip level remained at 1 volt for all frequencies.

Gate noise has been measured under two conditions at 10 Mc. In Section 2.3.2 (unclocked) the source of dynamic noise was the reverse current of the pulsed "and" diodes. In Section 2.3.2 (clocked) the dynamic noise was the result of the clock diode reverse-transient. The noise as a function of clock frequency has been replotted in Fig. 3.4-1.

It is possible to compute total gate noise from a knowledge of the diode static characteristics and measurements of the initial back current as a function of forward current. This has been done for the unclocked gate using Hughes 2109 diodes. The instantaneous input-clamp current i_b and unpulsed "and" current i_c have been derived from the following equations. The total noise has been computed from the static curves for the 2109 by the method that was used for Fig. 2.2-4.

If the 10 Mc gate is taken as a basis for computation, an equation relating gate current to clock frequency can be written [Equation (1)]. Assuming a five input "and" gate with 4 of 5 inputs pulsed, the normal steady-state current through any "and" diode is given by Equation (2).

$$I = \frac{4}{5} f \text{ ma} \tag{1}$$

f = clock frequency in Mc

$$I_f = \frac{I}{5} \text{ .} \tag{2}$$

An equation relating I_{BO} to the forward current can be obtained from Fig. 2.2-15 [Equation (3)]. Substituting Equation (2) in (3), I_{BO} as a function of gate current I is given by Equation (4). The initial current to the unpulsed "and" diode is given by Equation (5).

$$I_{BO} = .18\, I_f + .24 \text{ ma} \tag{3}$$

$$I_{BO} = .036\, I + .24 \text{ ma} \tag{4}$$

$$i_c = I + (m - 1)\, I_{BO} \qquad m = 5$$

$$i_c = 1.144\, I + .96 \text{ ma} \text{ .} \tag{5}$$

Let $I' = I + 6$ ma. A 6 ma minimum clamp current is much larger than is necessary for low frequency operation but it is necessary to avoid input clamp cutoff at 40 Mc. The current through the unpulsed input clamp is given by Equation (6). A comparison of the computed results with the experimental noise measurement at 10 Mc (Fig. 3.2-2a) shows that .1 volt should be added to the computed values to adjust the experimental results to computed data. The normalized results are plotted in Fig. 3.4-1.

$$i_b = I' - i_c$$

$$i_b = 5.04 - .144\ I \quad . \qquad (6)$$

The magnitude of the input gate current is a factor which will set a practical limit on the frequency of operation. For example, the input current to a pulsed "and" gate input at 40 Mc is equal to 38 ma plus the reverse current lost to the back-biased input clamp and pulsed "and" diode. In practice, it will be the restricted number of gate drives that will limit the frequency of operation rather than gate noise resulting from diode transients.

4. SUMMARY

The purpose of this contract was to investigate experimentally and theoretically the possibility of increasing the speed of operation of the dynamic circuitry of SEAC type computer components by at least an order of magnitude. This particular report has dealt with the design limitations of the diode gating structure. The more important conclusions are summarized below.

The speed of operation of a diode logic circuit is limited by the amount of noise which can be tolerated in the circuit and the magnitude of current required per gate input. As frequency of operation is increased, all gate currents must necessarily increase if a given grid swing is to be maintained. It is the increased gate current that is primarily responsible for the decadent performance as frequency is increased.

Noise has been shown to be the result of diode reverse-transient currents and the static characteristics of the unpulsed input clamp and "and" diodes. The reverse-transient properties have been given priority over the static characteristics. It is true that the static characteristics of the unpulsed "and" diode contribute to the static noise, but this additional .2 to .3 volt of noise is a small price to pay for a diode with really good back-transient properties. The aim of diode choice has been to obtain the best possible forward conduction without sacrificing back-transient properties. This has been the criterion for diodes in all positions in the gate with the exception of the input "or" diode.

Not only are the reverse transients important for the reduction of noise but also the reverse current of the input clamp, "and" diodes, and grid-clamp diodes represent a charge loss not present in the gate using ideal diodes. The reverse transients of two diodes, the clock diode and the "or" diodes on the tube grid, are particularly critical. The forward transients have been shown to be negligible by comparison to the reverse transient. It is recommended that all diodes be checked for forward conduction and back-transient properties before use in the gate circuit. Of the diodes tested to date, the Hughes 2109 represents the best compromise of diode characteristics.

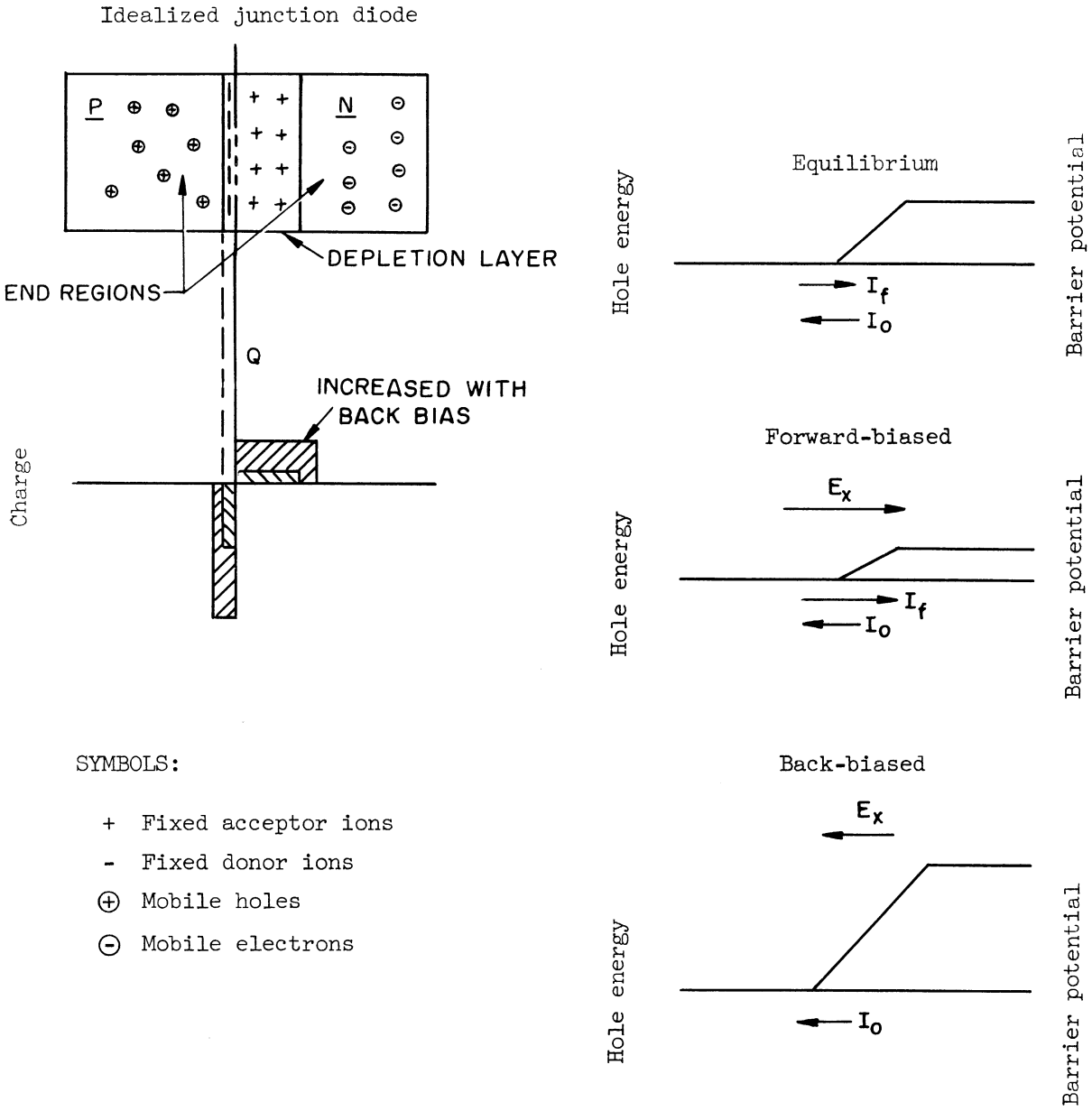
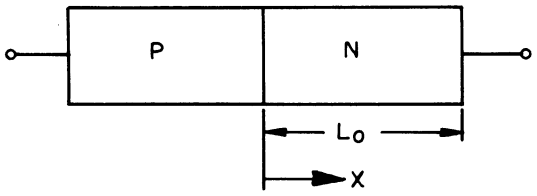
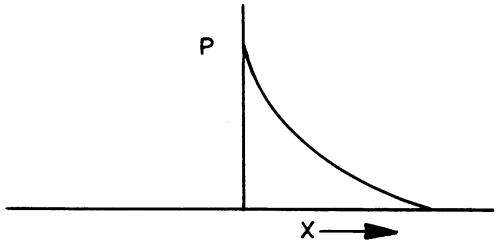


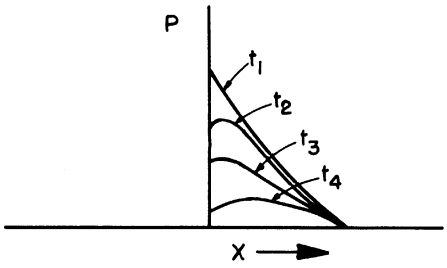
Fig. 2.1-1. Mechanism of diode conduction.



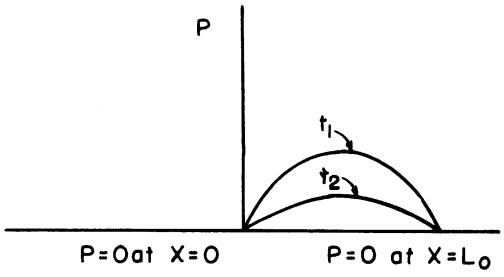
Steady-state hole concentration



Hole concentration for reverse bias condition during T_1



Hole concentration for reverse bias condition during T_2



Reverse transient for a junction diode

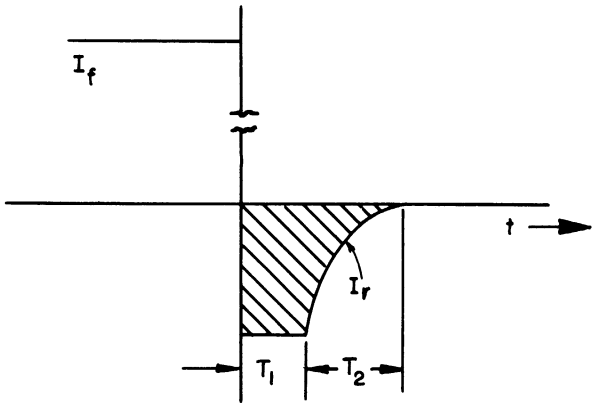


Fig. 2.1-2. Theoretical junction diode.

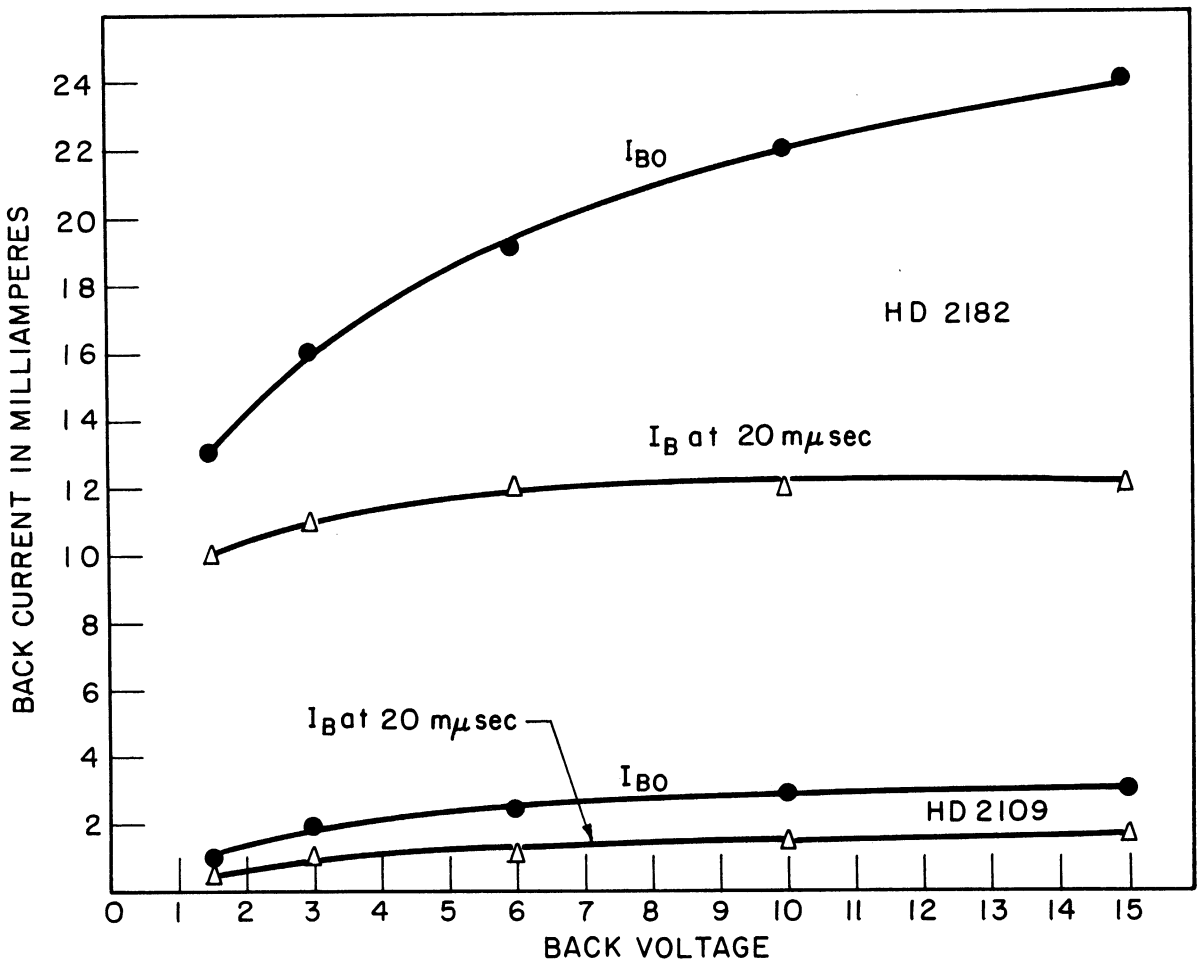
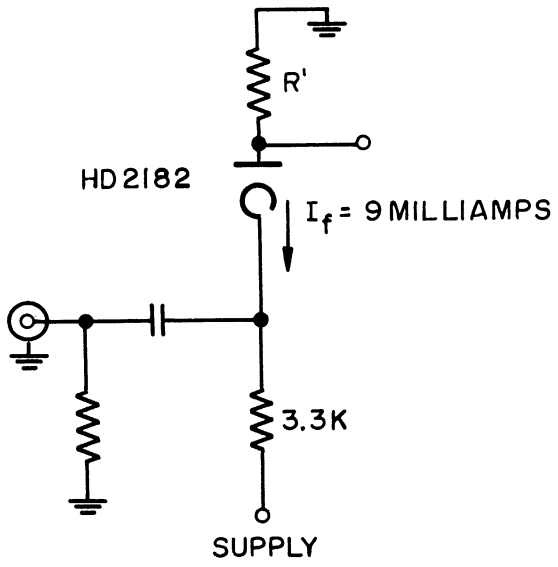
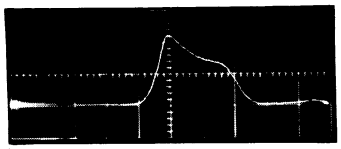
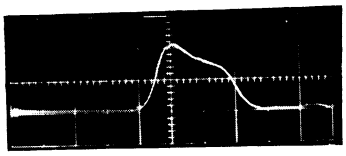


Fig. 2.2-1. Effect of back bias on back recovery.

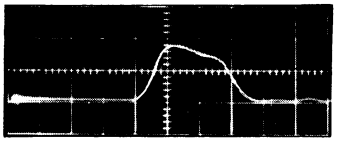




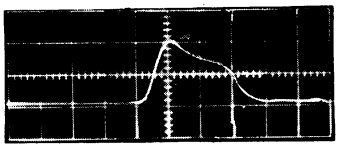
R' = 50 Ω
E_b = -1.5 v



R' = 100 Ω
E_b = -1.5 v



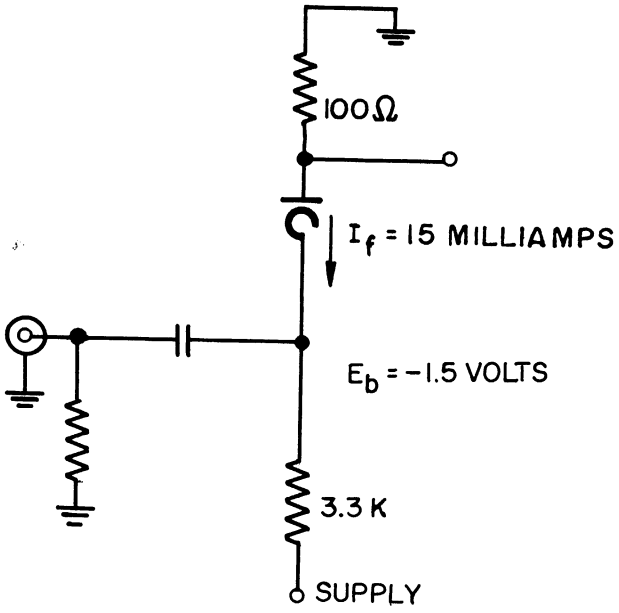
R' = 200 Ω
E_b = -1.5 v

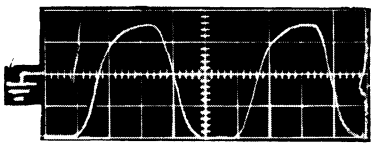


R' = 200 Ω
E_b = -4.0 v

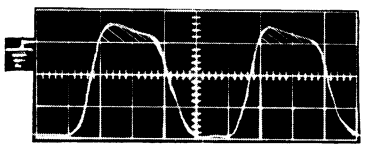
Current = 10 ma/div
Time = .02 μsec/div

Fig. 2.2-2. Effect of circuit series resistance R' on back recovery.

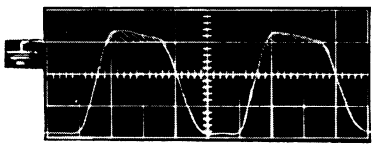




Input voltage
1 v/div
.02 μsec/div

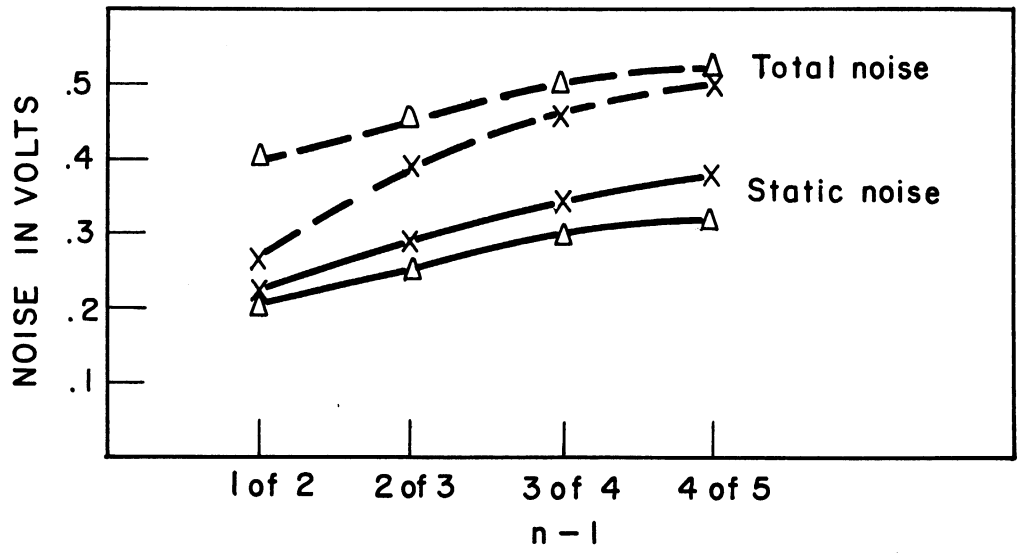


HD 2109
5 ma/div
.02 μsec/div



Ray 295
5 ma/div
.02 μsec/div

Fig. 2.2-3. Back recovery at a 10 Mc repetition rate.



Circuit: see Fig. 3.2-1a
Specifications: I = 8 ma
I' = 12 ma
Symbols: Δ = actual case
X = computed case

Fig. 2.2-4. Noise as a function of the number of gates pulsed.

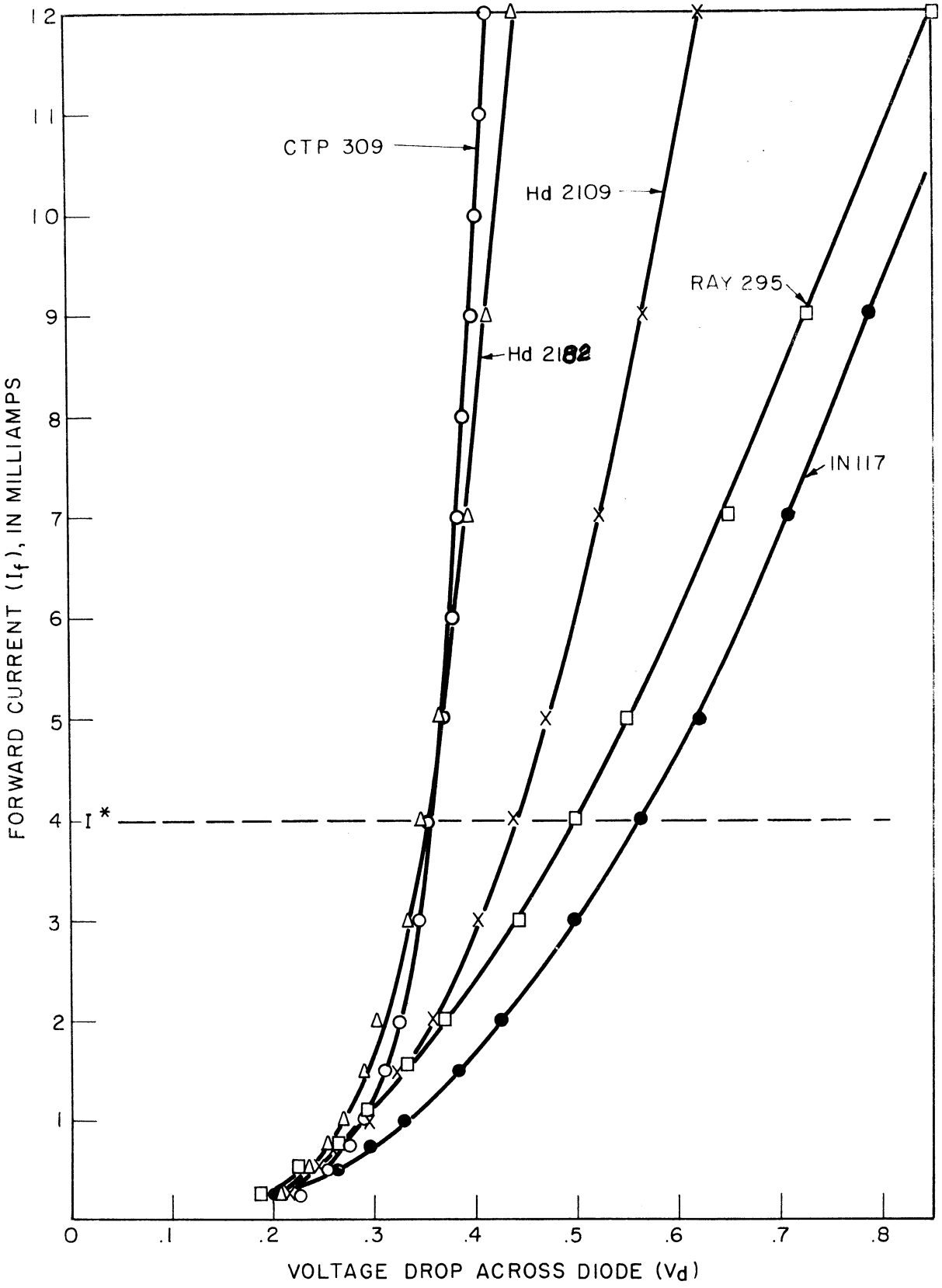


Fig. 2.2-5. Static characteristics of representative diodes.

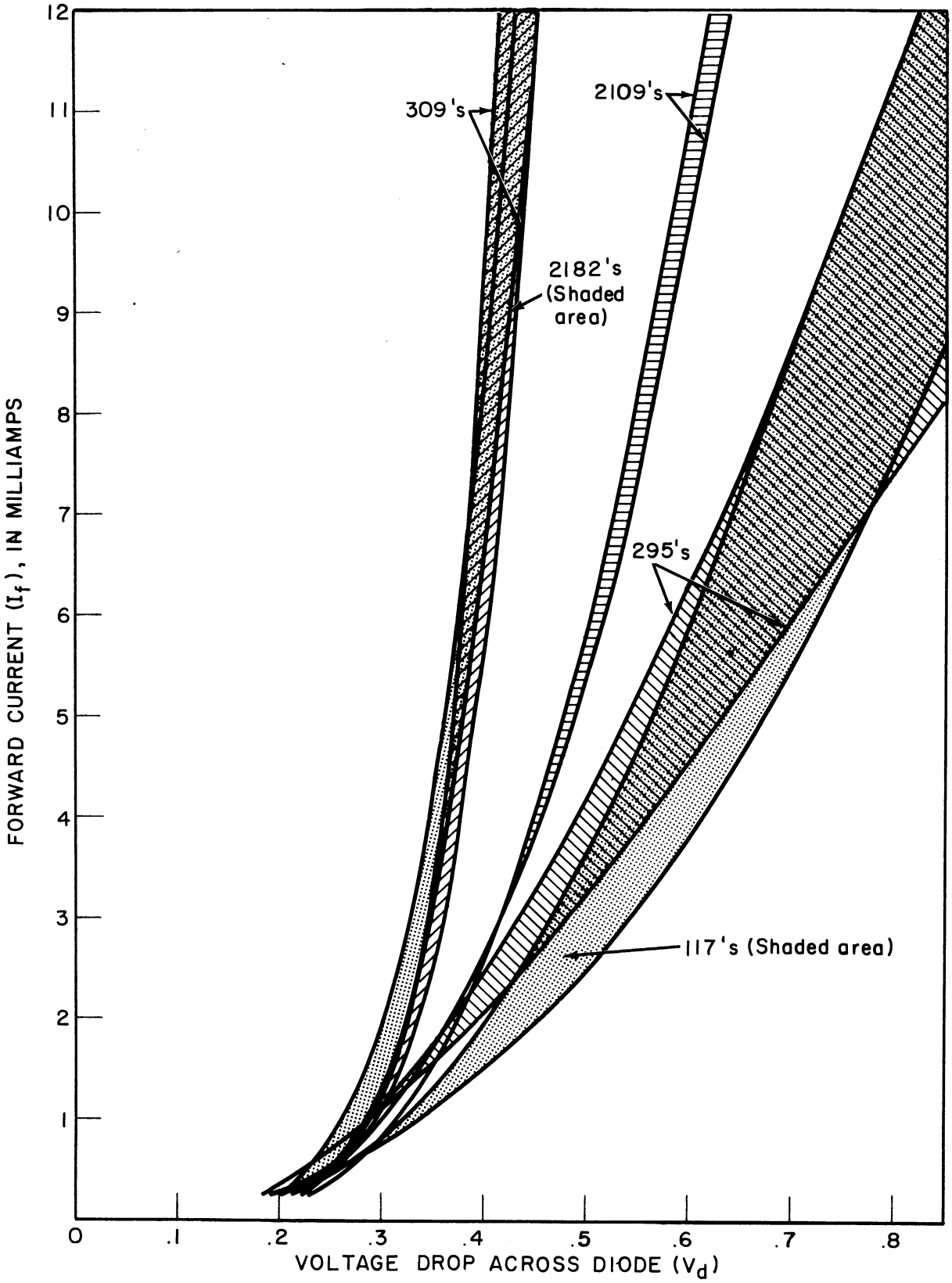


Fig. 2.2-6. Deviation of static characteristics.

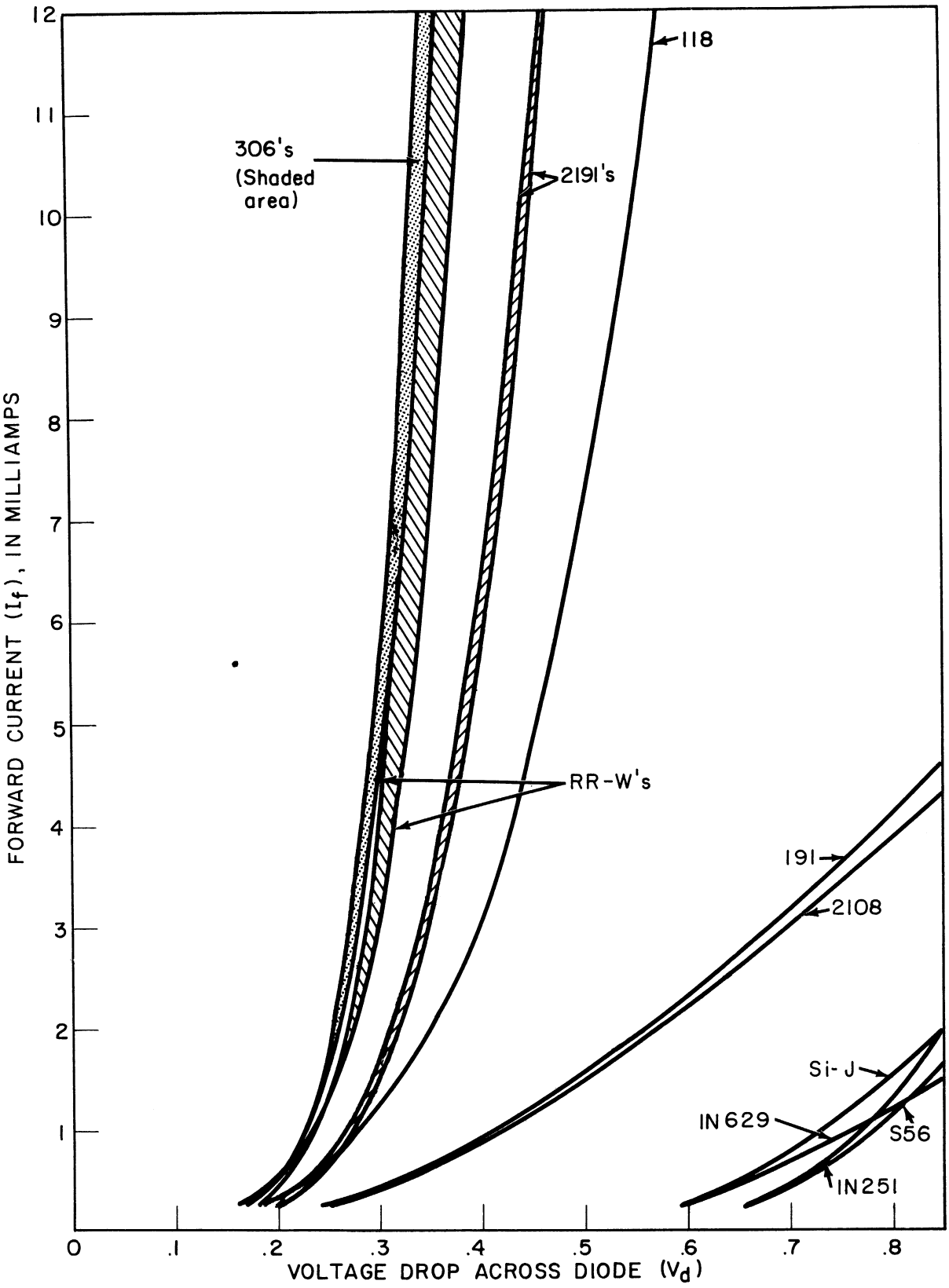
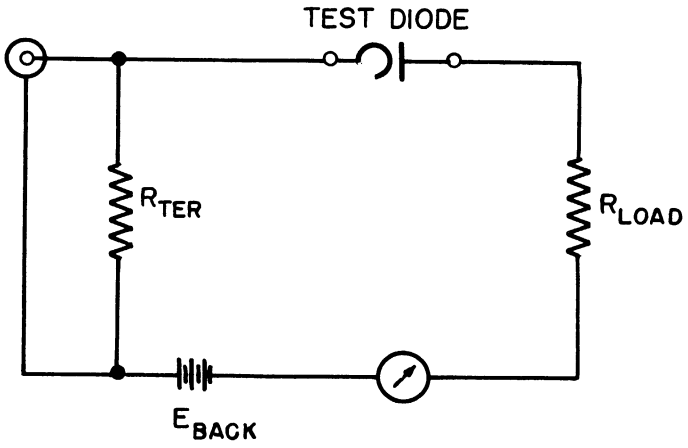
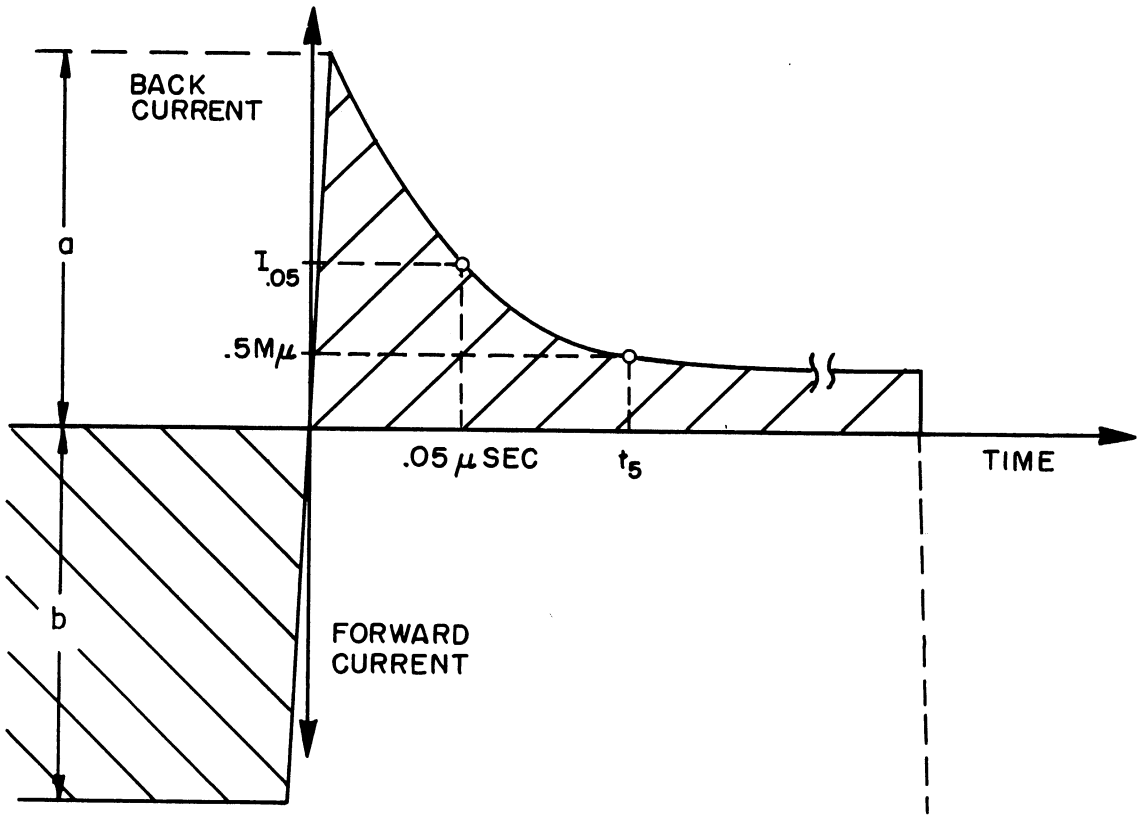


Fig. 2.2-7. Static characteristics of additional diodes tested.





Forward and reverse current at R_{load}

Fig. 2.2-8. Back transient test circuit at 25 Kc.

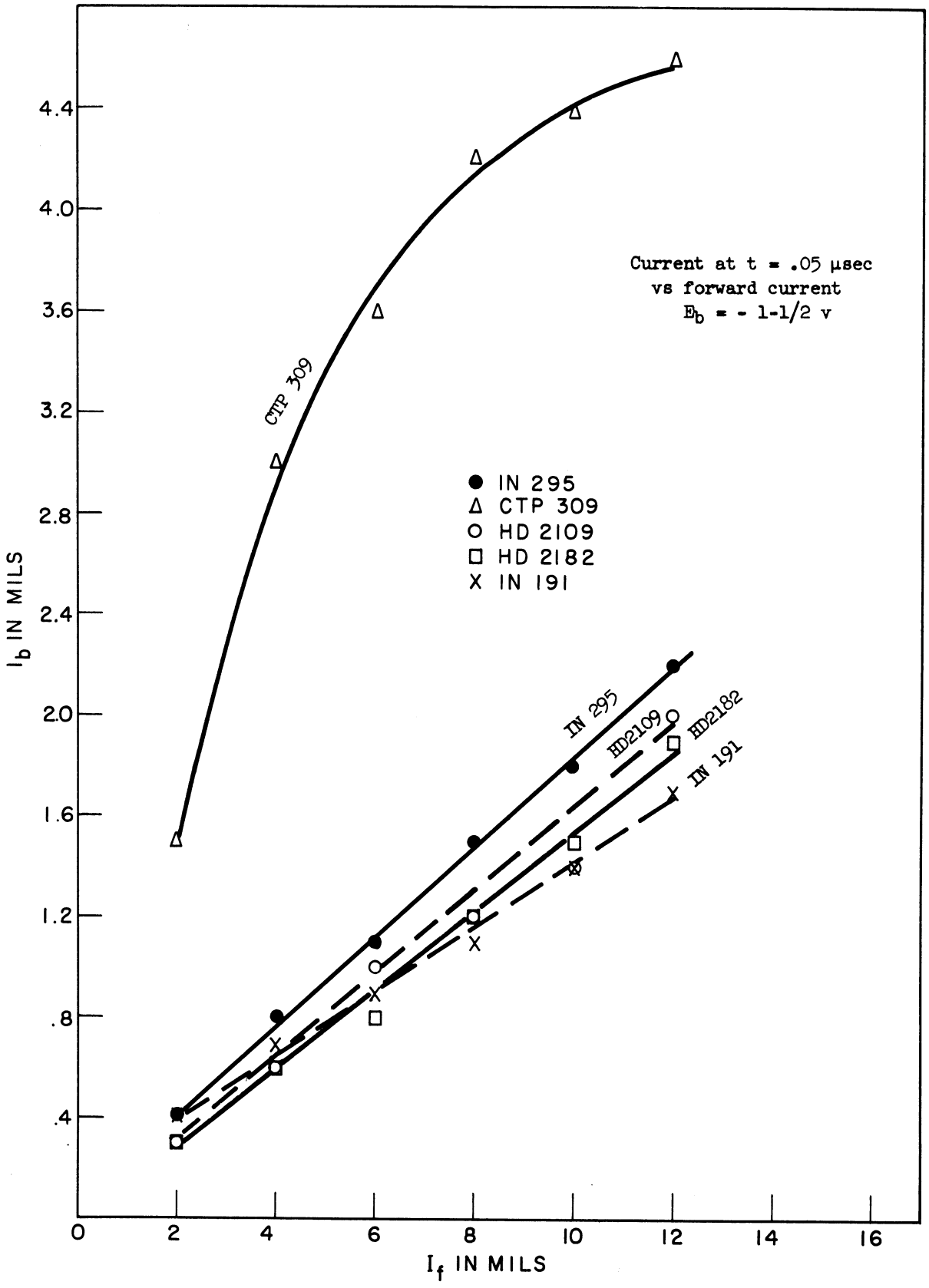


Fig. 2.2-9. Current at t = .05 μsec vs forward current, E_b = -1.5 v.

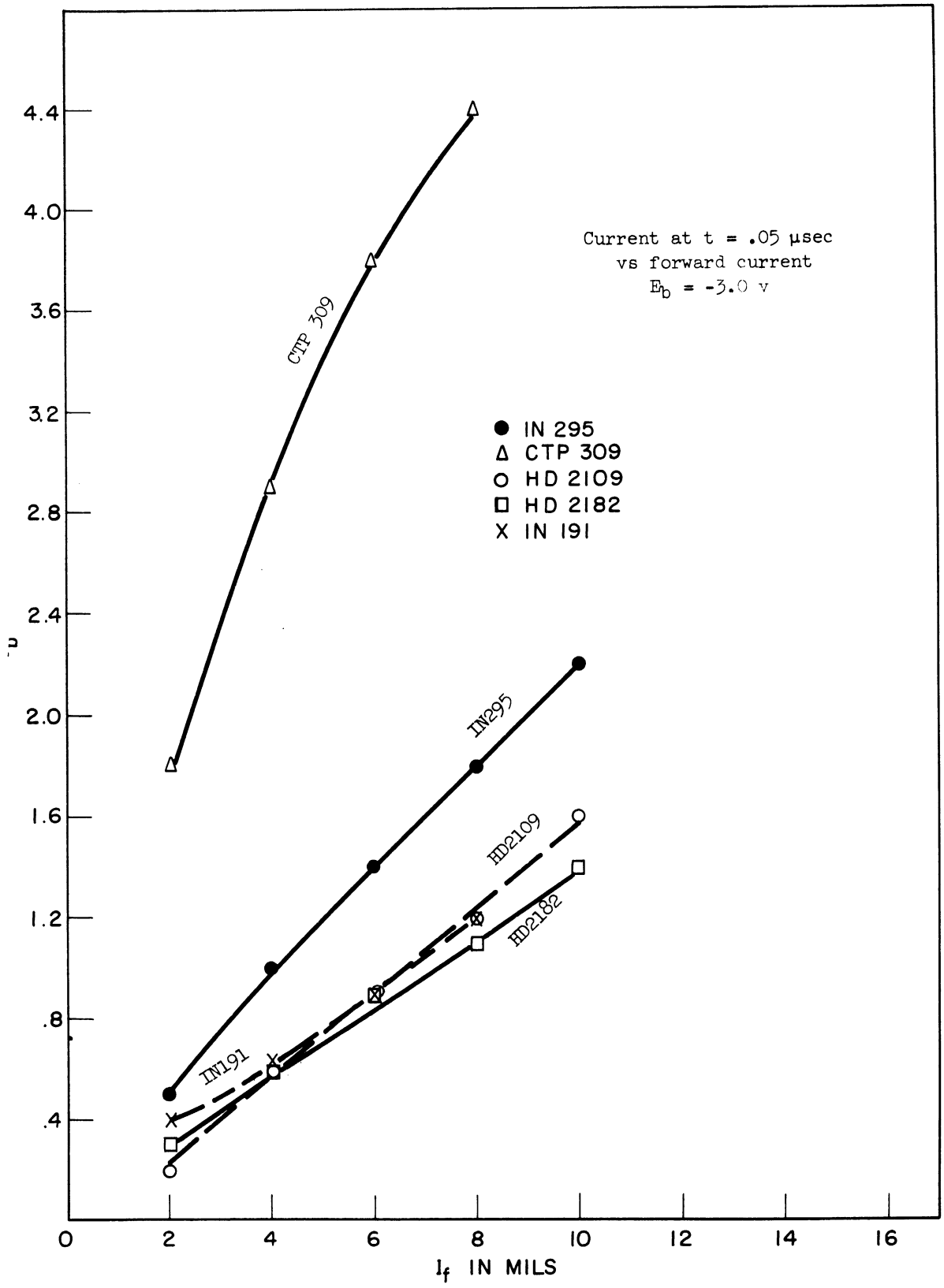


Fig. 2.2-10. Current at t = .05 μsec vs forward current, E_b = -3.0 v.

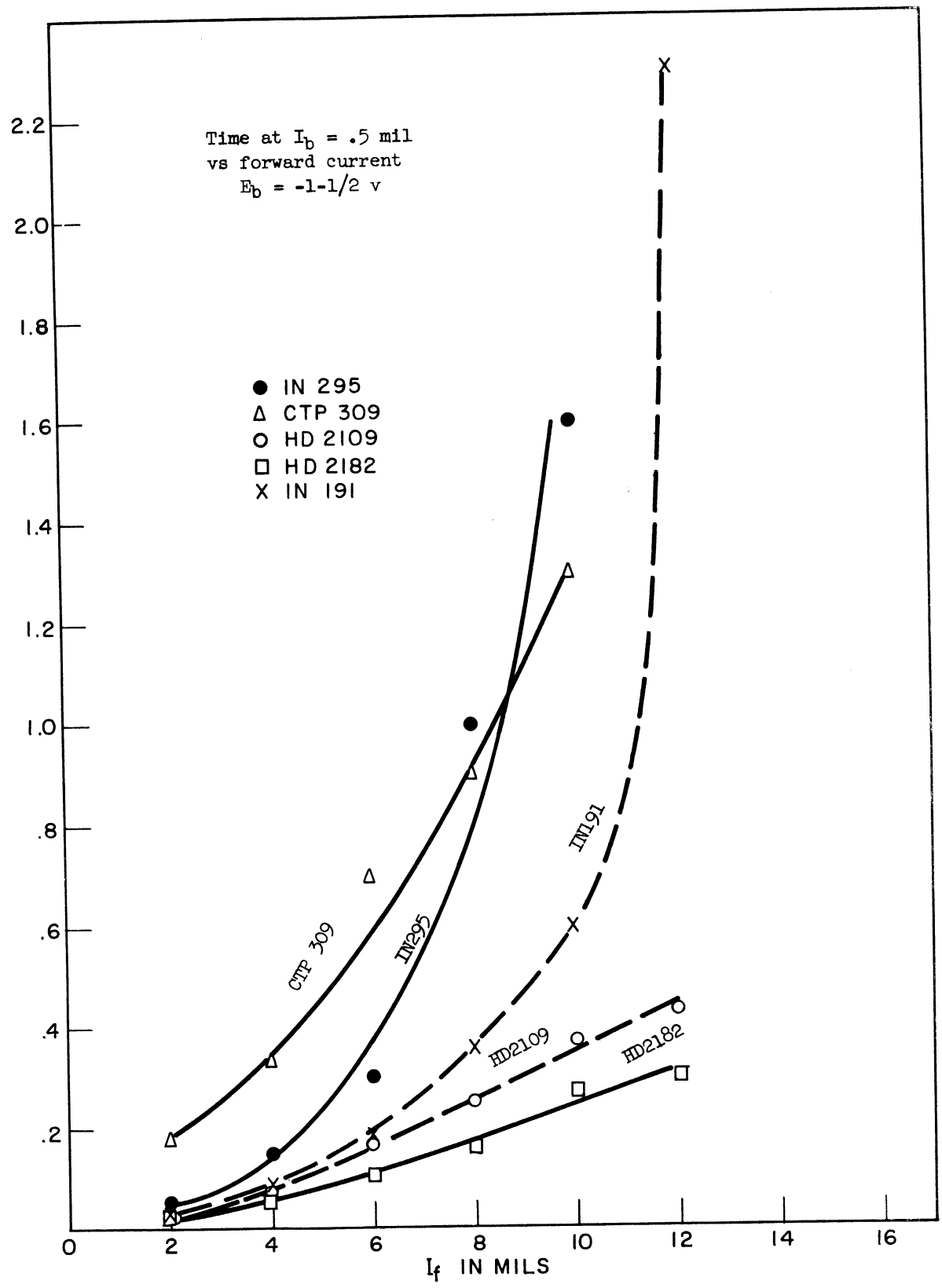


Fig. 2.2-11. Time at I_b = .5 mil vs forward current, E_b = -1.5 v.

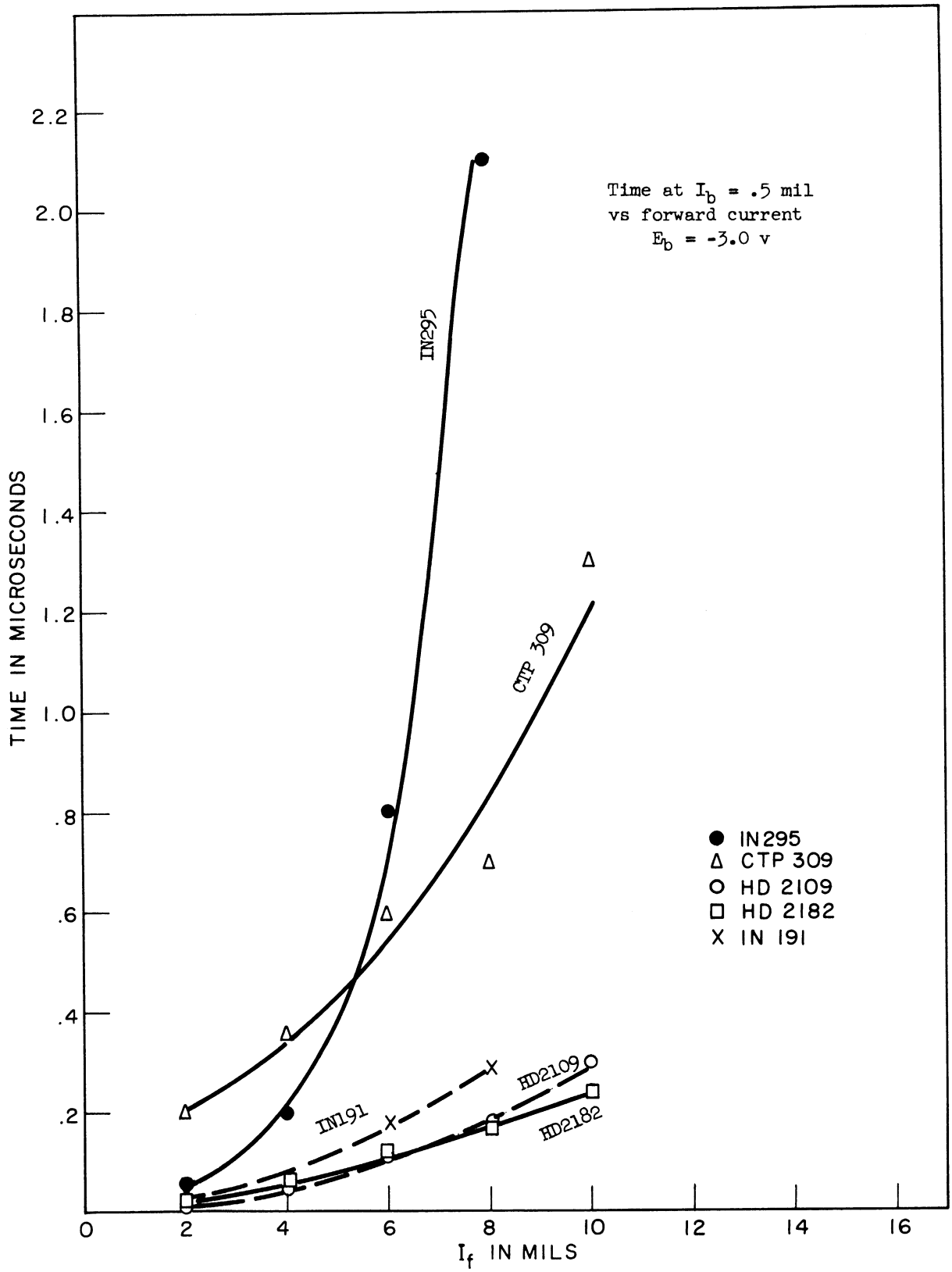
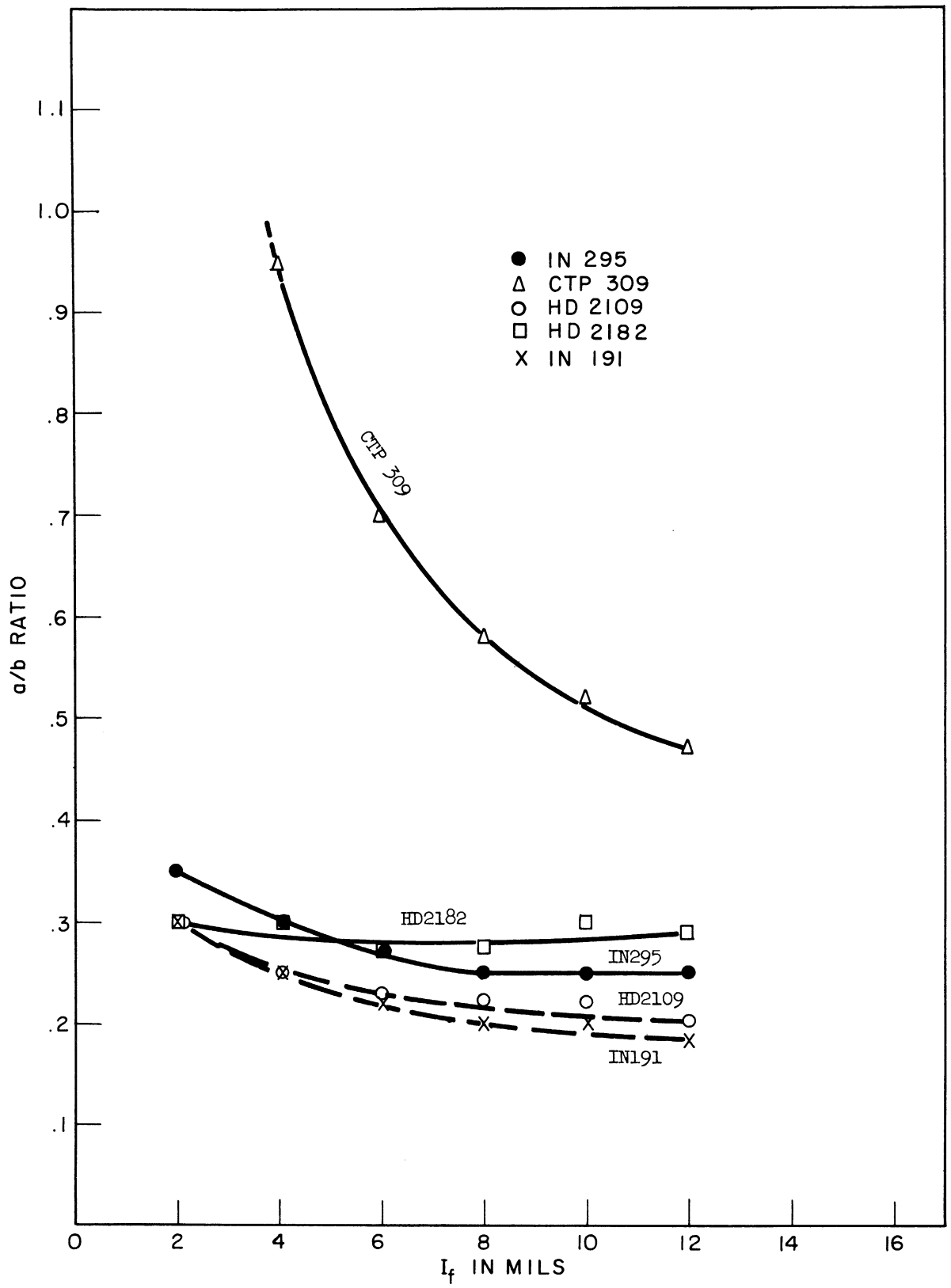


Fig. 2.2-12. Time at I_b = .5 mil vs forward current, E_b = -3.0 v.



Fib. 2.2-13. a/b ratio vs forward current, E_b = -1.5 v.

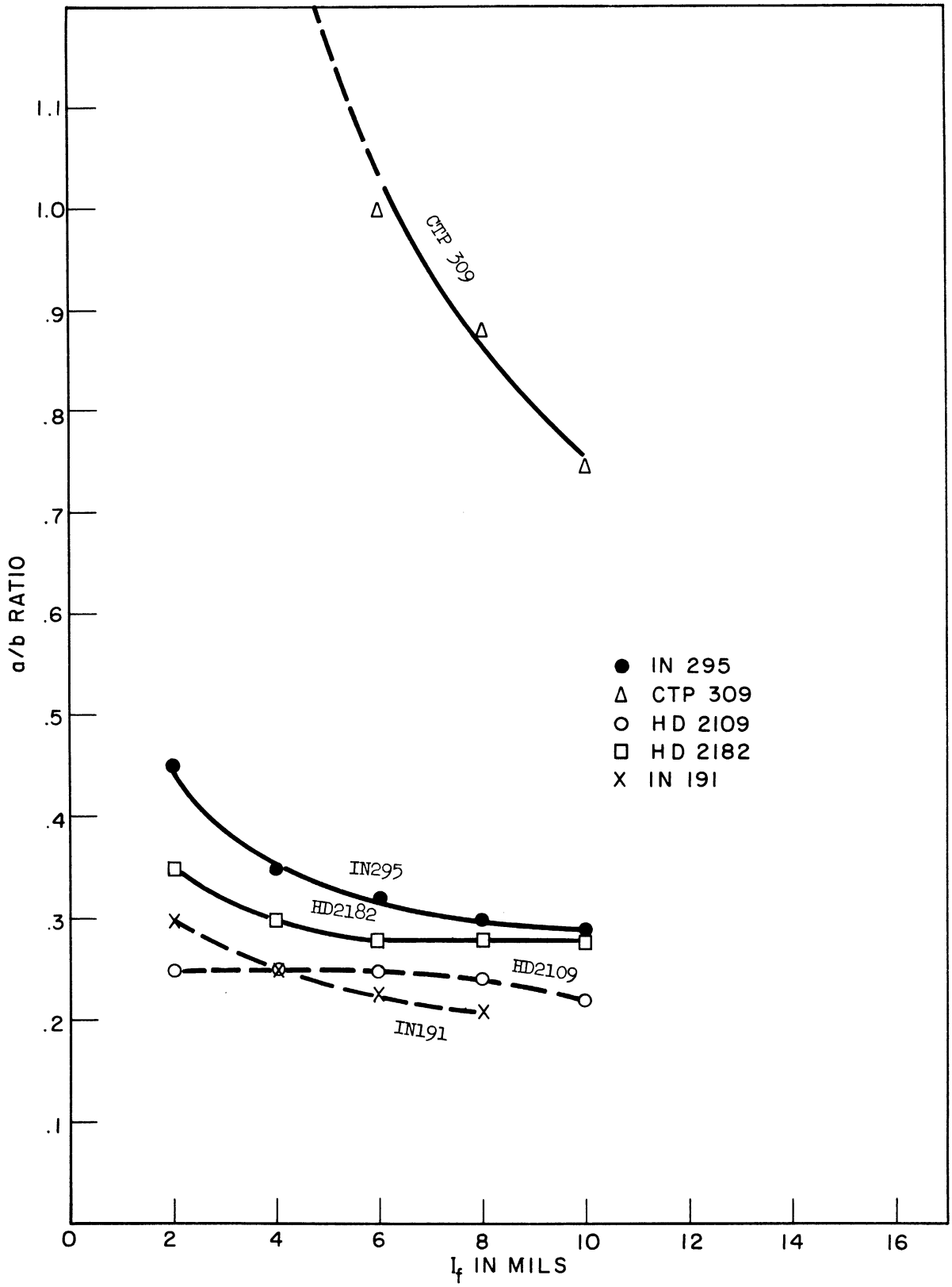


Fig. 2.2-14. a/b ratio vs forward current, E_b = -3.0 v.

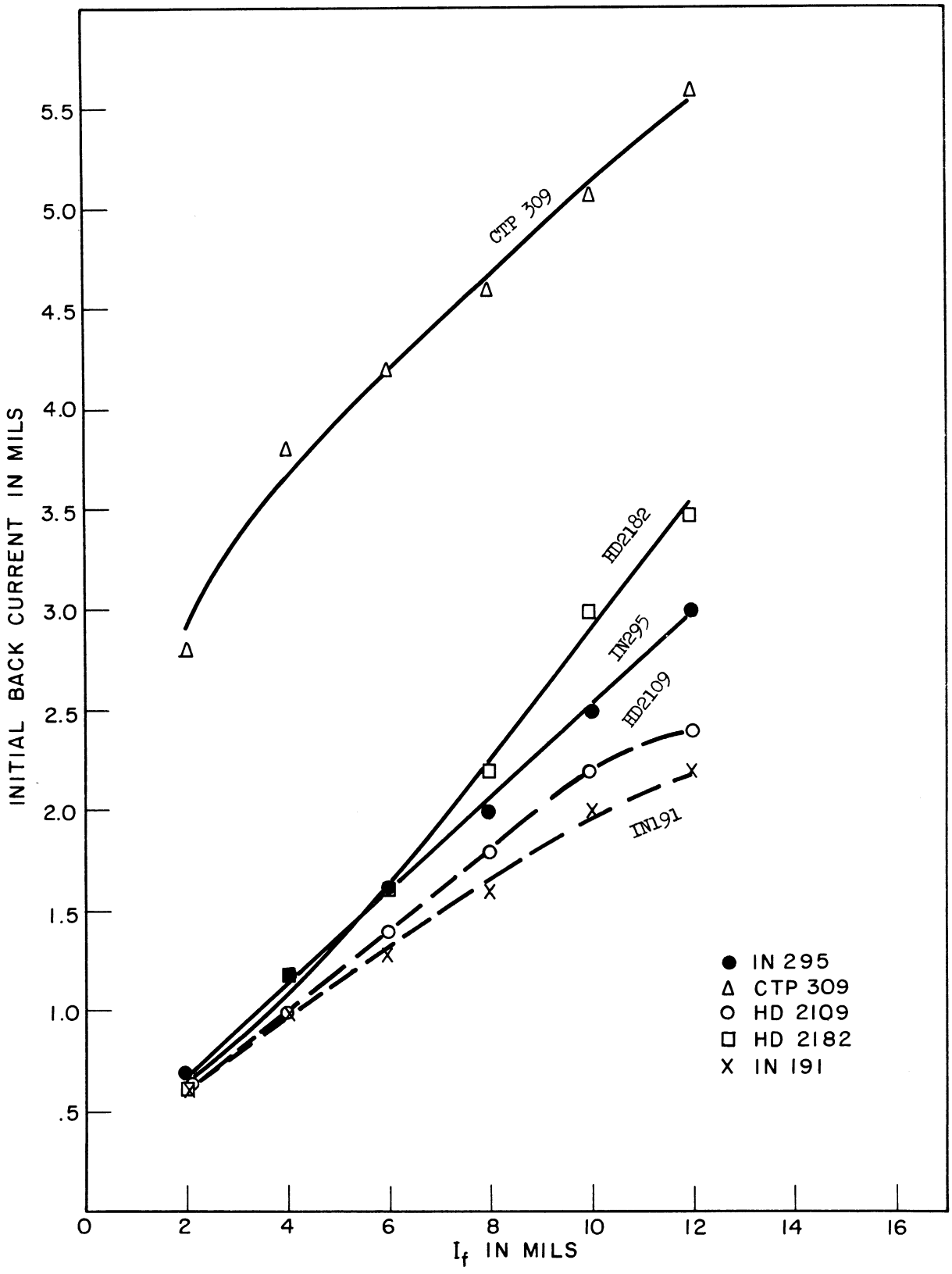


Fig. 2.2-15. Initial back current vs forward current, E_b = -1-1.5 v.

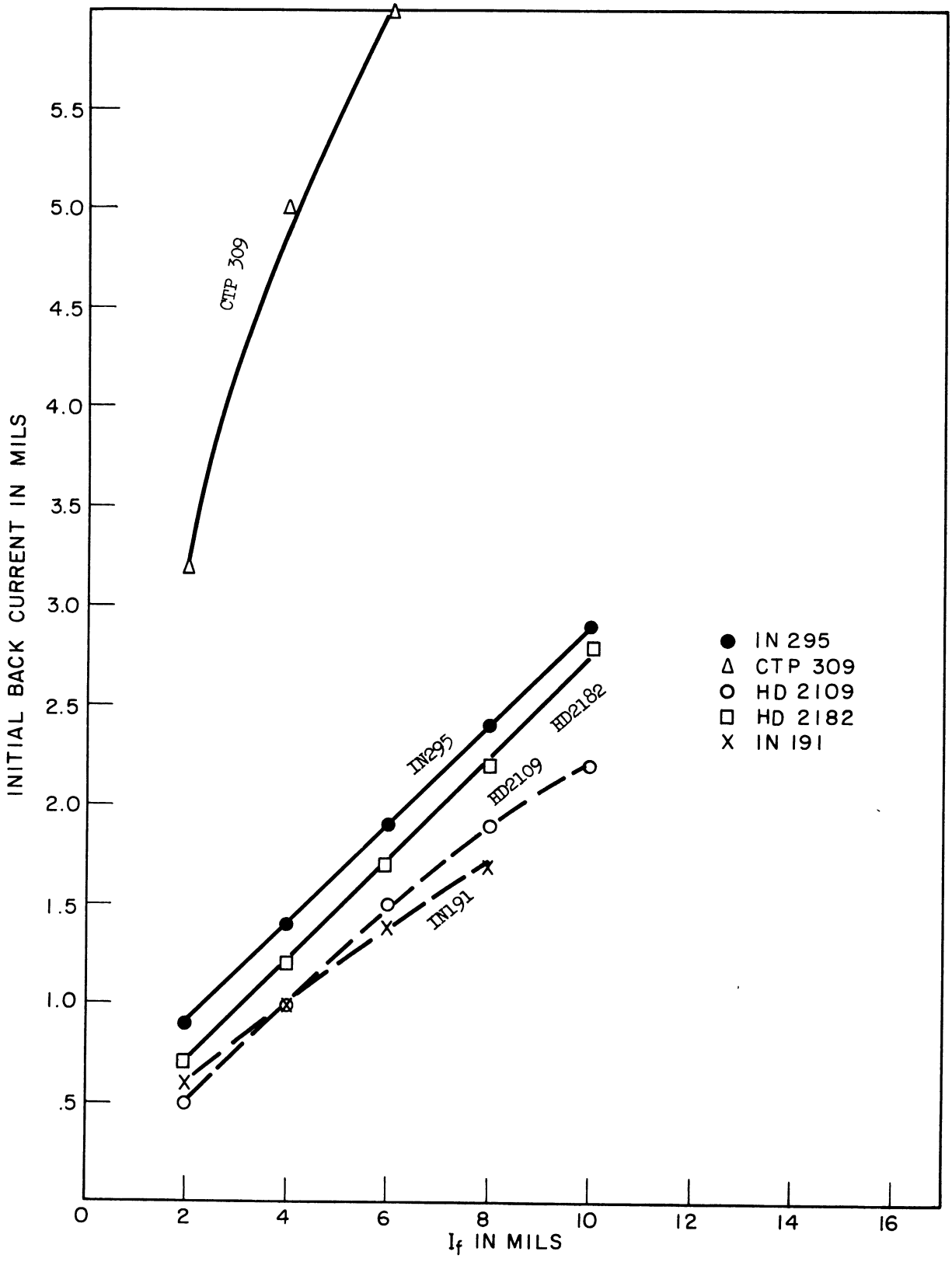
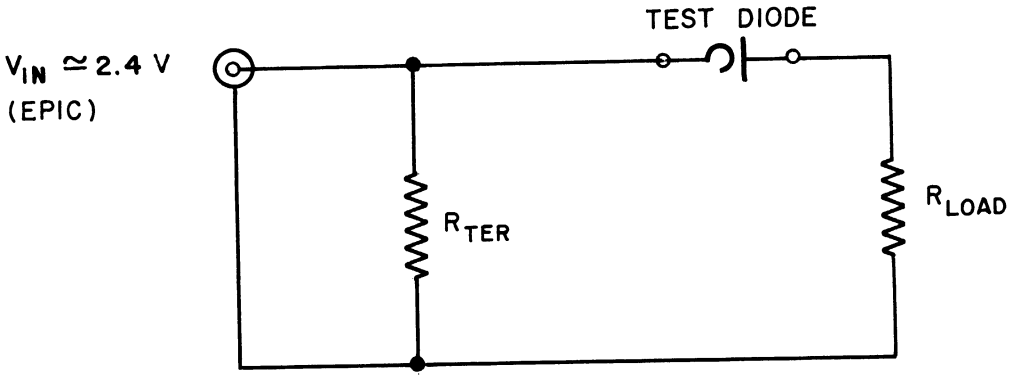
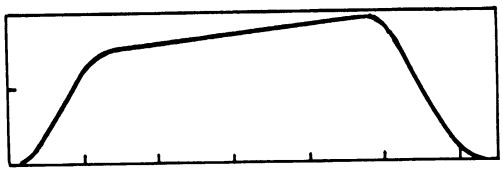


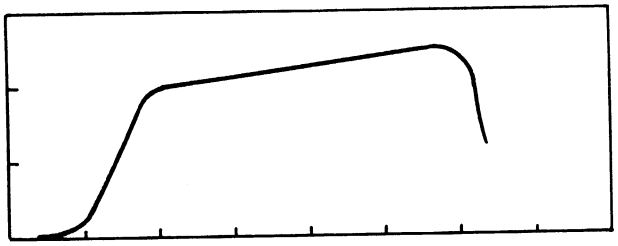
Fig. 2.2-16. Initial back current vs forward current, E_b = -3.0 v.



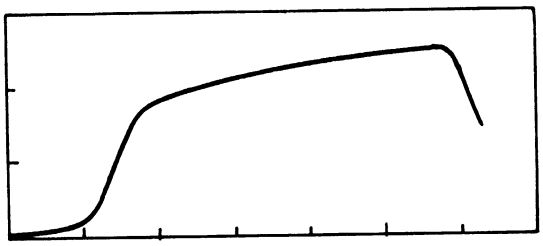
Current wave forms



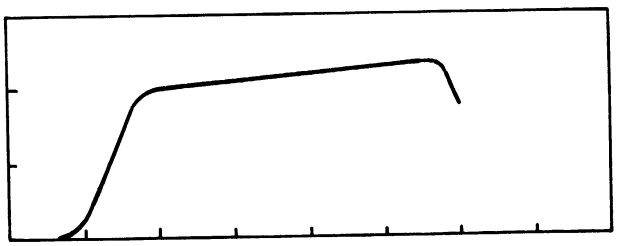
IN 117



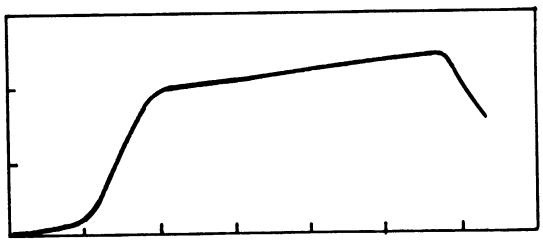
HD2182



CTP 309



Ray 295

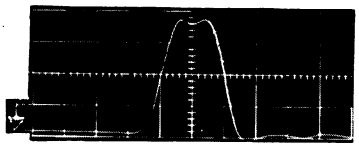


HD2109

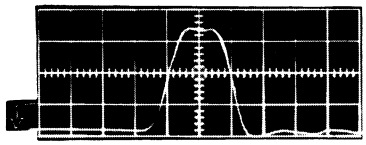
Time scale: .008 μsec/cm
Amplitude scale: .85 volts/cm

Fig. 2.2-17. Forward transients

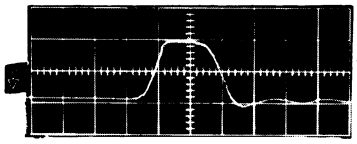
Grid signal with no attempt at clipping



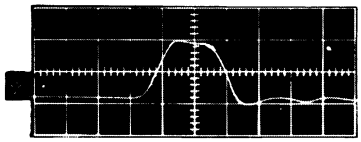
117



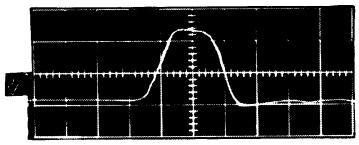
309



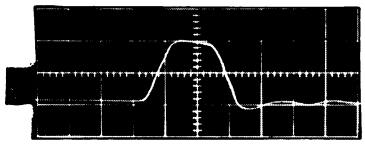
2182



295



2109



Time scale: 0.020 μsec/div
Amplitude scale: 0.5 volt/div

Fig. 2.2-18. Determination of the best clip diode (G).*

*See Fig. 3.2-1a for the circuit used.

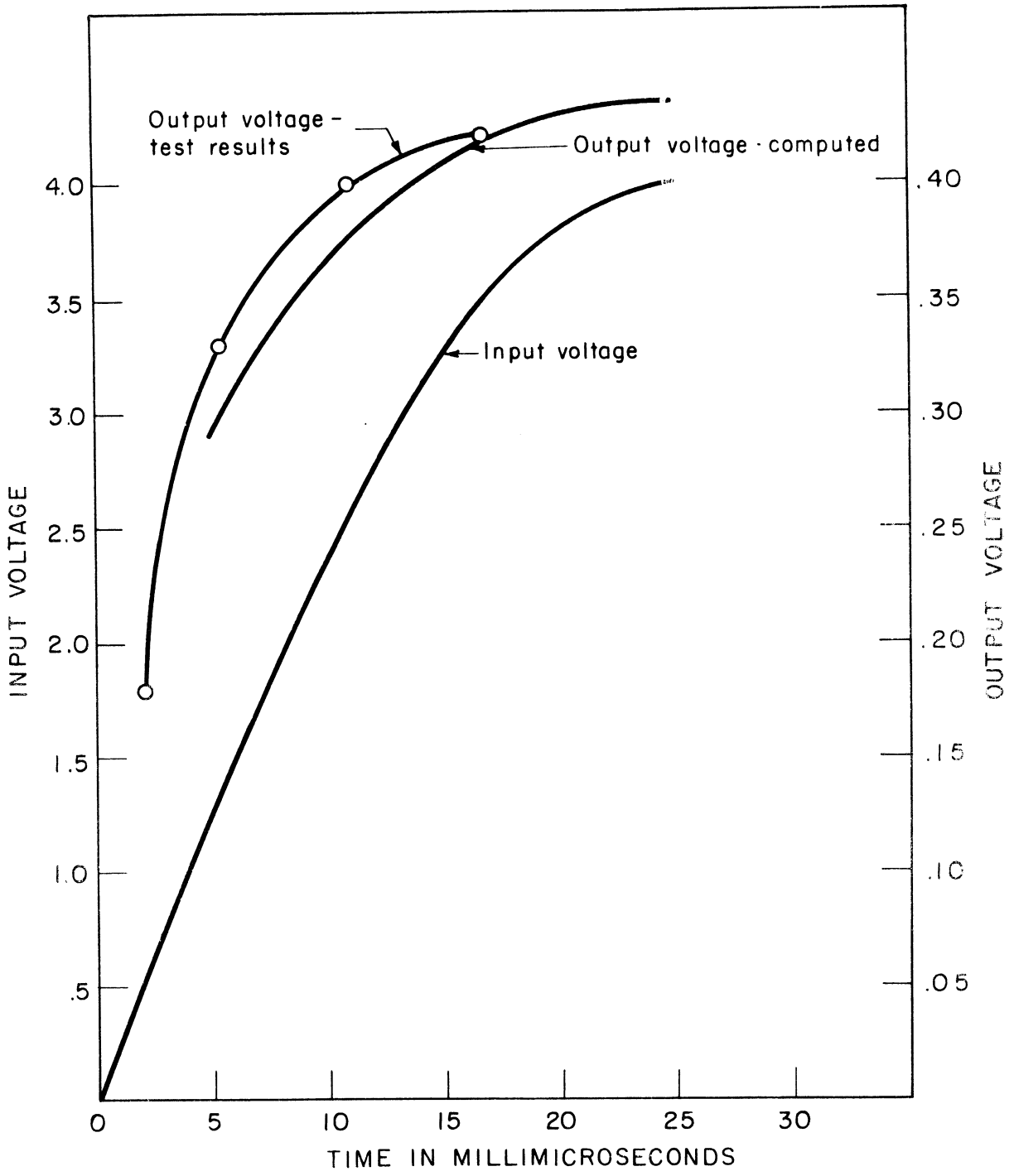
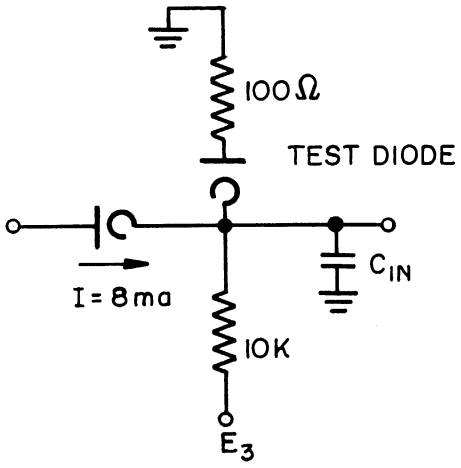
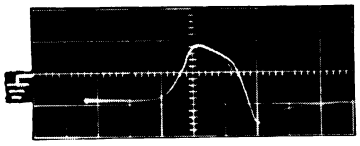


Fig. 2.2-19. Effect of static characteristics on wave shape.

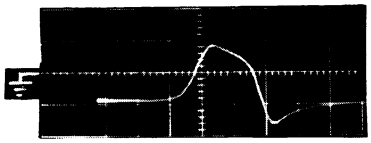
Circuit:



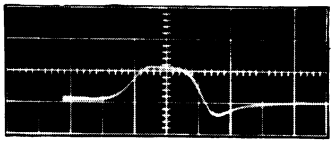
CTP 309



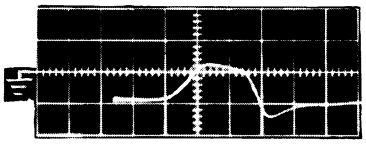
HD2182



Ray 295



HD2109



Time scale: 20 μsec/div
Amplitude scale: 5 ma/div

Fig. 2.3-1. Experimental determination of the best grid-clamp diode.

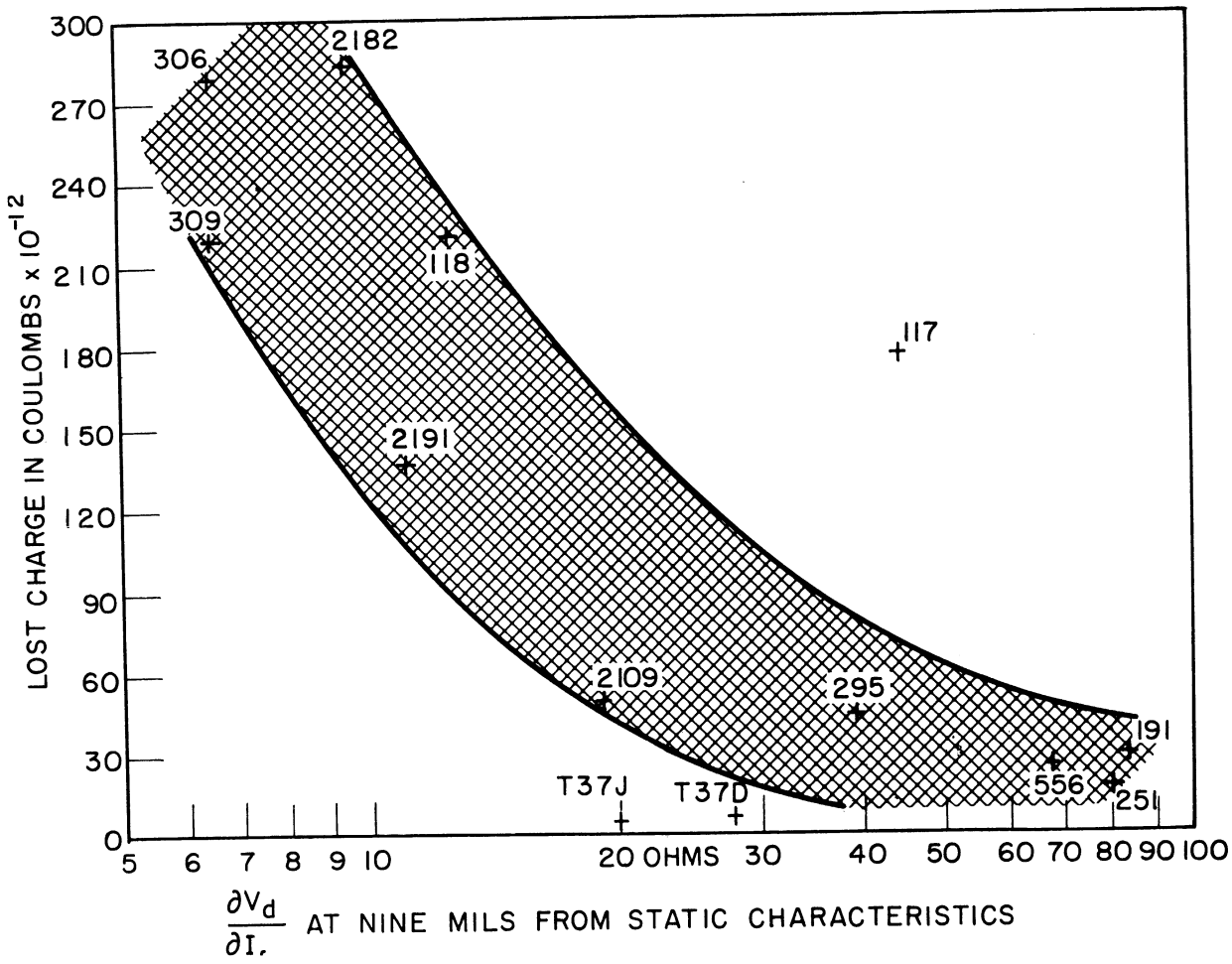
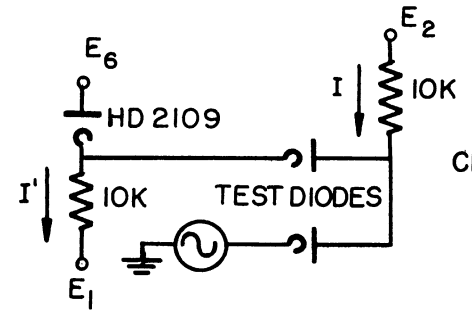


Fig. 2.3-2. Experimental correlation between static characteristics and lost charge.



CLOCK AMPLITUDE: 6 VOLTS

Frequency	I	I'	Static Noise	Clock Noise	Total Noise	Test Diodes
5 Mc	4	8	.26	.15	.41	HD2109
10	8	12	.36	.18	.54	
15	12	16	.44	.20	.64	
20	16	20	.51	.30	.81	
5	4	8	.44	.2	.64	Ray IN295
10	8	12	.49	.30	.79	
15	12	16	.67	.33	1.00	

Total noise = Static noise + Clock noise

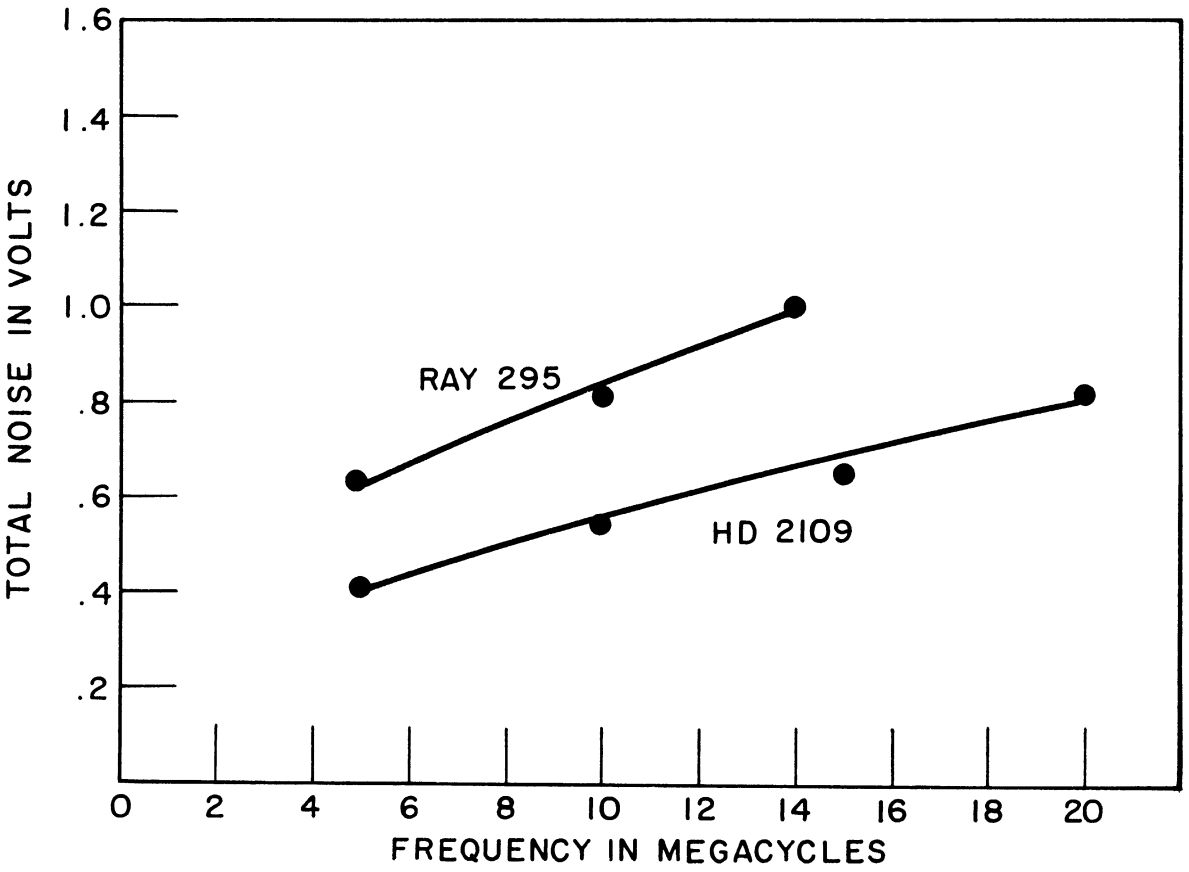


Fig. 2.3-3. Noise variation with frequency.

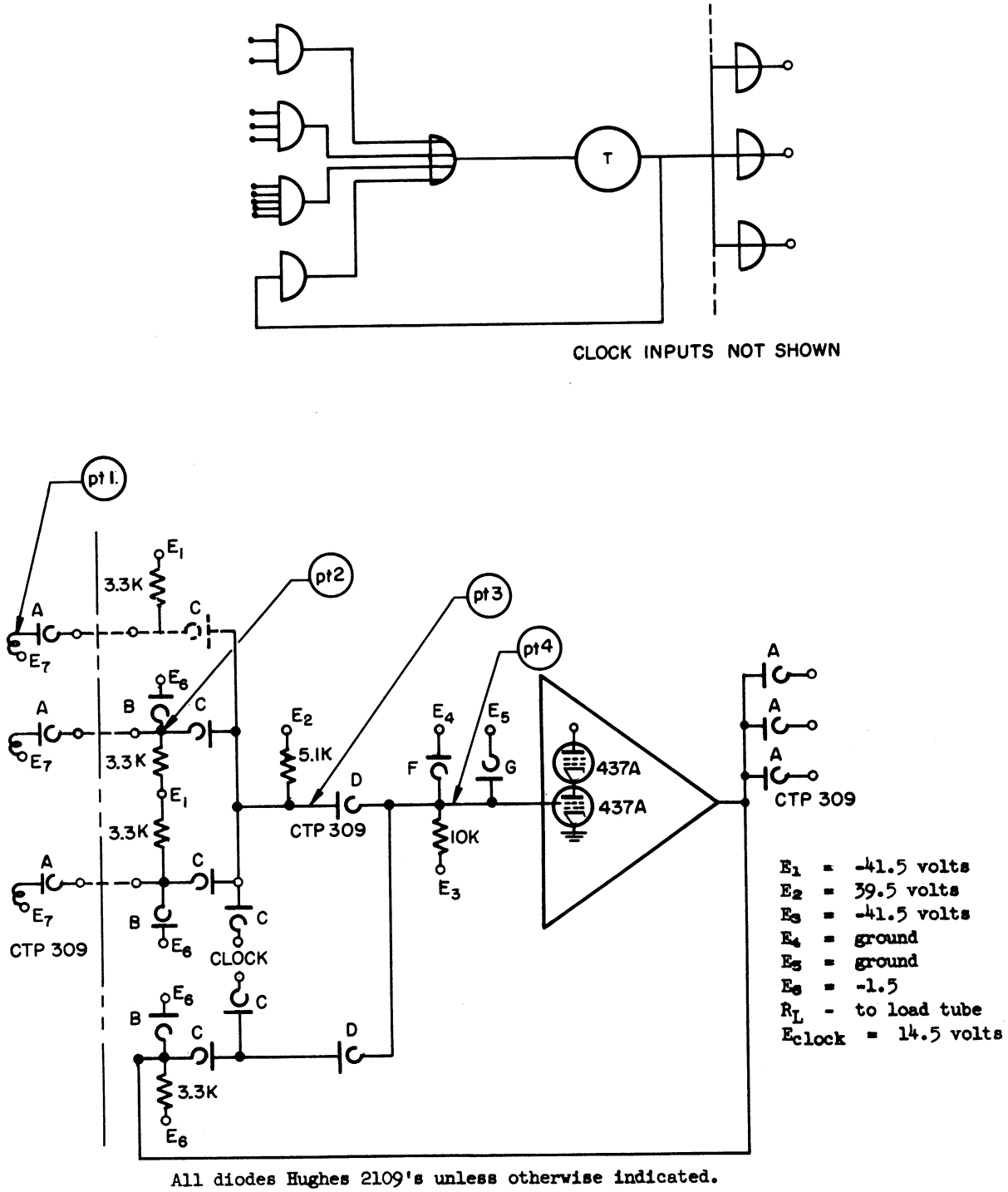
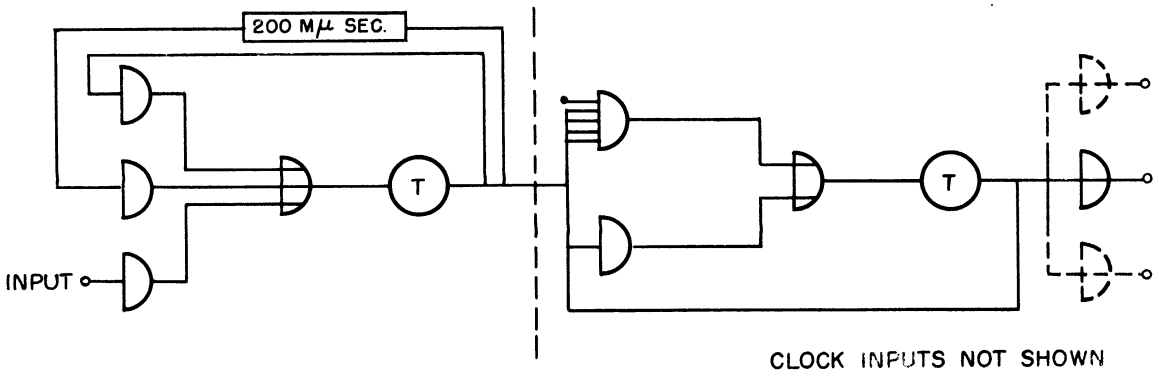
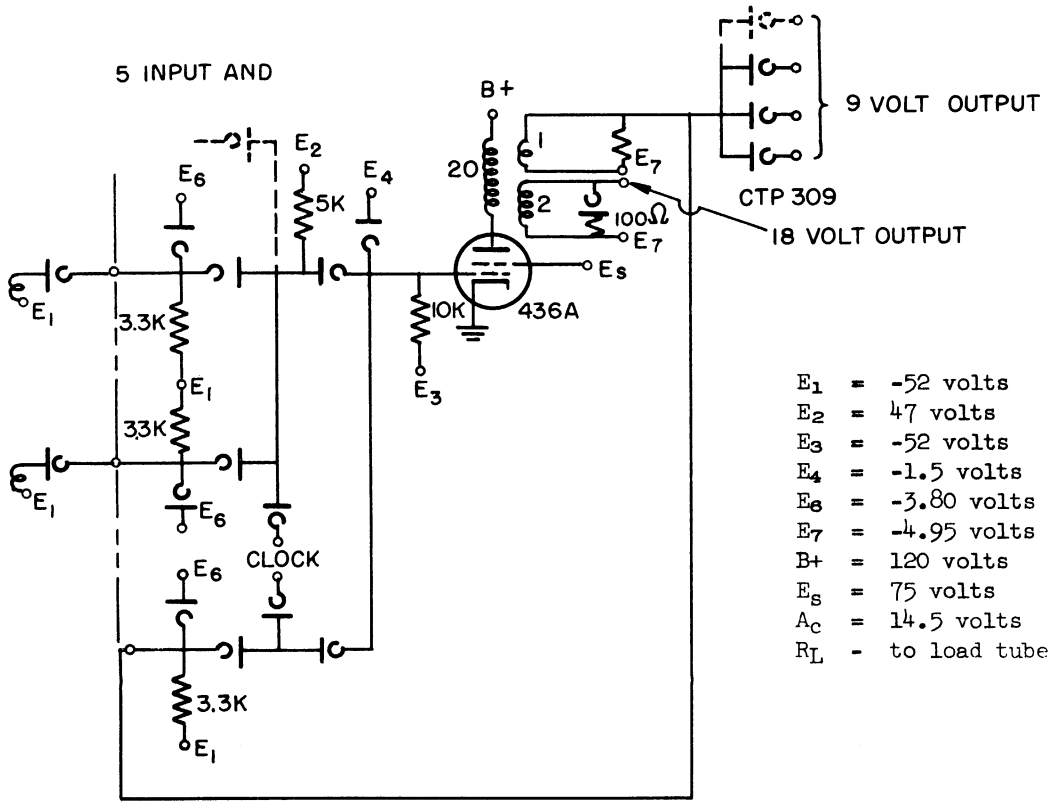


Fig. 3.2-1a. 10 Mc experimental package.

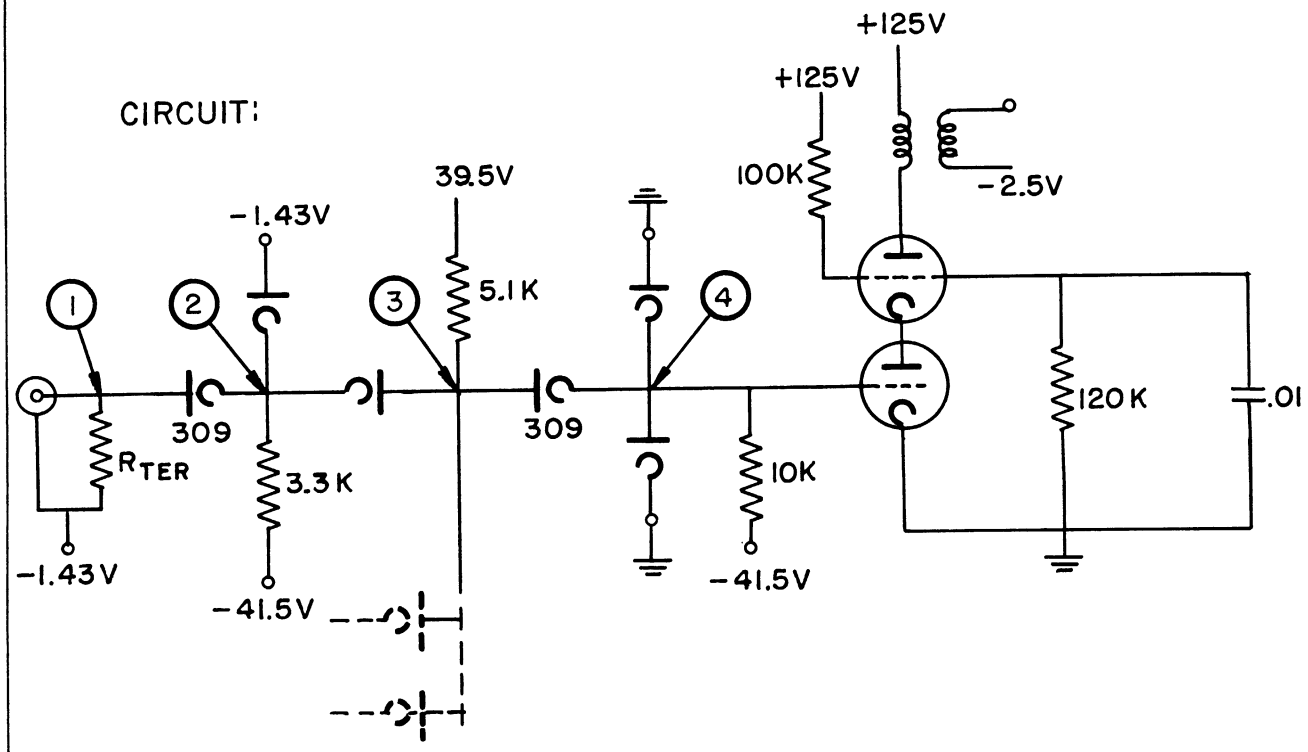




E_1 = -52 volts
E_2 = 47 volts
E_3 = -52 volts
E_4 = -1.5 volts
E_6 = -3.80 volts
E_7 = -4.95 volts
B+ = 120 volts
E_s = 75 volts
A_c = 14.5 volts
R_L - to load tube

All diodes are Hughes 2109's unless otherwise indicated.

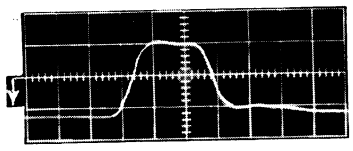
Fig. 3.2-1b. 5 Mc experimental package.



Note: All diodes 2109's unless otherwise indicated.

CONDUCTION

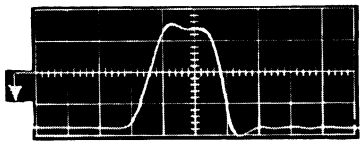
Pt 1



2 v/div

.020 μsec/div

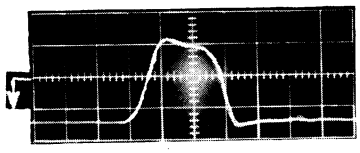
Pt 2



1 v/div

.020 μsec/div

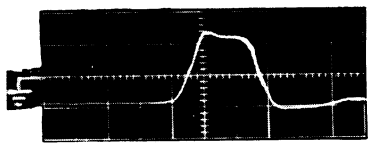
Pt 3



1 v/div

.020 μsec/div

Pt 4



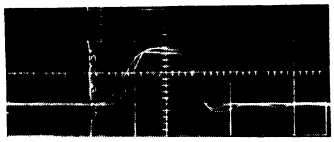
.5 v/div

.020 μsec/div

Fig. 3.2-2a. 10 Mc gate performance.

DELAY

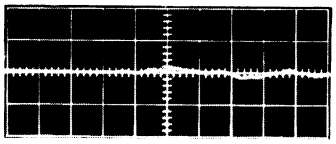
Pt 2 to Pt 4



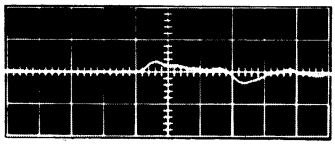
at Pt 2 2 v/div
at Pt 4 .5 v/div

Time = .020 μsec/div

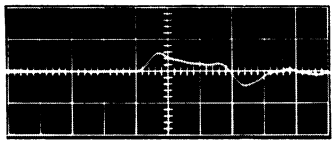
NOISE



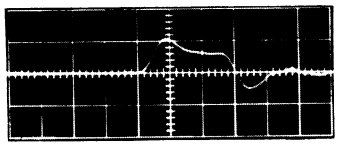
1 of 5 pulsed



2 of 5 pulsed



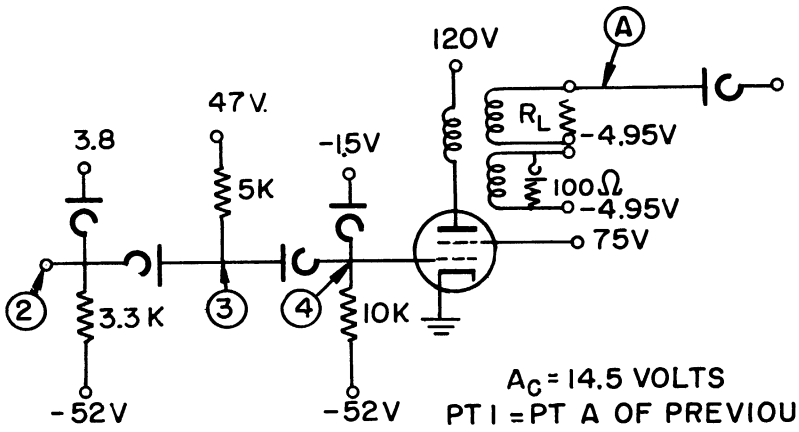
3 of 5 pulsed



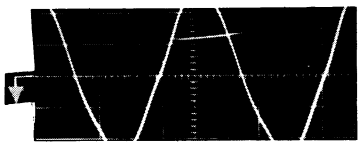
4 of 5 pulsed

.5 v/div
.020 μsec/div

Fig. 3.2-2a (Cont.).

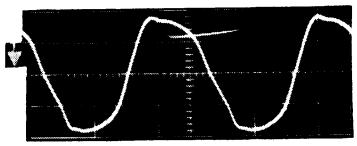


E_o = 9.0 volts
I = 10 ma
I' = 14.4 ma



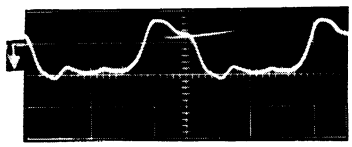
No. 1

Clock phase 2
5 v/div



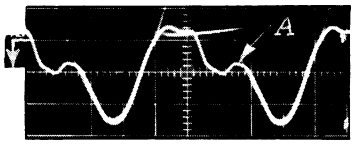
No. 2

Input-point 1
5 v/div



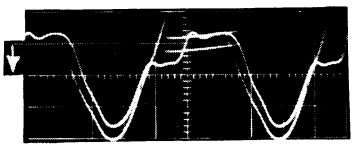
No. 3

Point 2
5 v/div



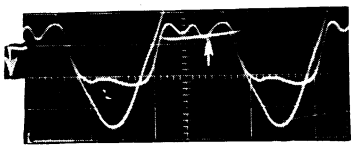
No. 4

Point 3
5 v/div



No. 5

Regen. gate
5 v/div

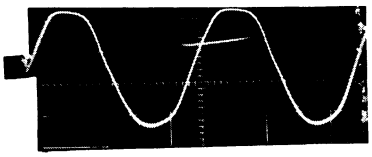


No. 6

Point 4
2 v/div

Time scale: 40 millimicroseconds/div

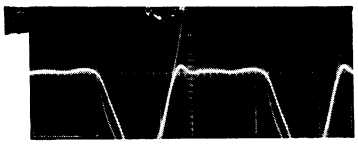
Fig. 3.2-2b. 5 Mc gate performance.



No. 7

Output
10 v/div

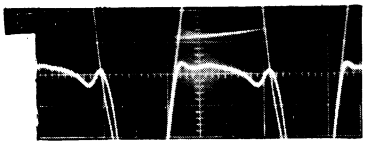
Noise



No. 8

0 of 5 pulsed
2 v/div

Noise*

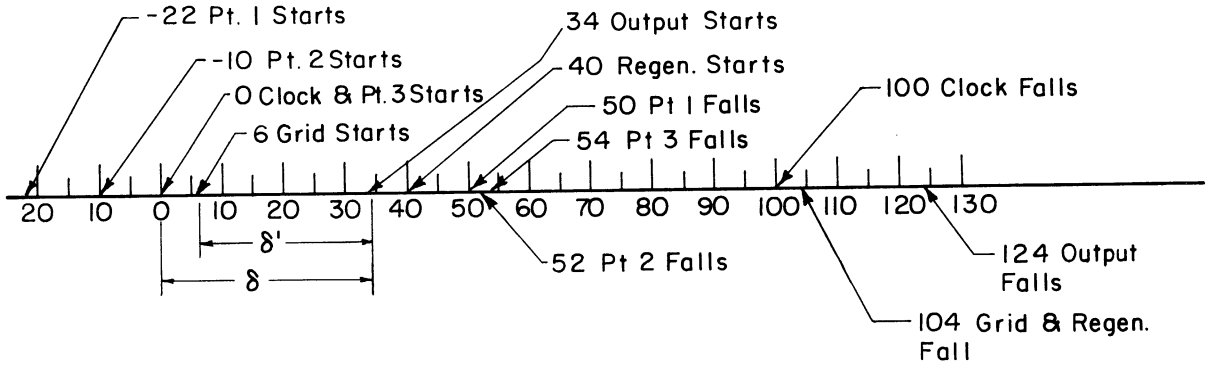


No. 9

4 of 5 pulsed
2 v/div

Time scale: 40 millimicroseconds/div

Pulse Time Sequence in Millimicroseconds



Note: Pulse "starts" when it goes through zero.
Pulse "falls" when it goes through zero.

Fig. 3.2-2b. (Cont.).

*Computed static noise is equal to .418 volt.

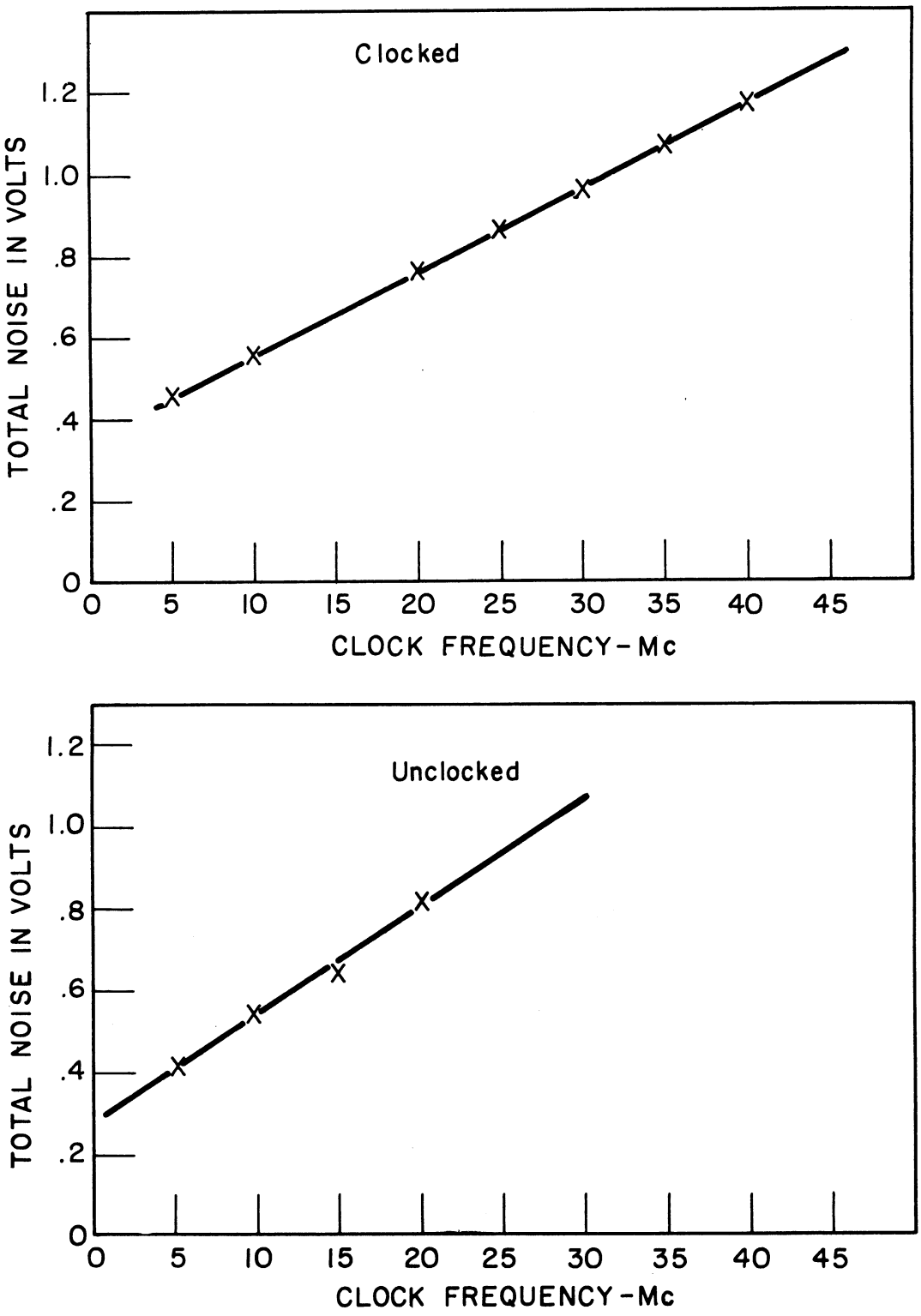
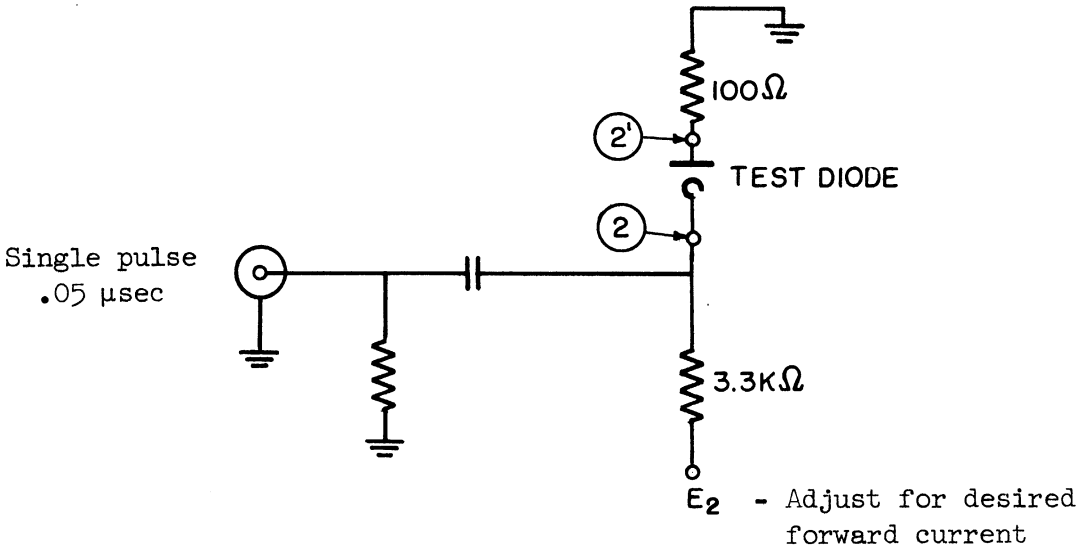


Fig. 3.4-1. Upper limit of performance.

TABLE 2.2-I

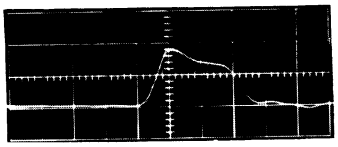
BACK RECOVERY AS A FUNCTION OF FORWARD CURRENT



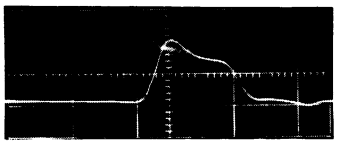
Diode	I_f Forward Current	I_{BO} Initial Reverse Current	Q_L Lost Charge	E_b Back Bias
CTP 309	3 ma	4 ma	110×10^{-12}	- 1.5 volts
	9	8	202×10^{-12}	- 1.5
	15	12	378×10^{-12}	- 1.5
Ray 295	3	1.0	18×10^{-12}	- 1.5
	9	2.0	45×10^{-12}	- 1.5
	15	3.0	77×10^{-12}	- 1.5
HD2182	3	4	104×10^{-12}	- 1.5
	9	10	252×10^{-12}	- 1.5
	15	13	402×10^{-12}	- 1.5
HD2109	3	0.5	6.5×10^{-12}	- 1.5
	9	1.5	21×10^{-12}	- 1.5
	15	2.0	36×10^{-12}	- 1.5

TABLE 2.2-I (Cont.)

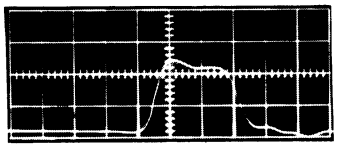
Forward Current of 9 mils in All Cases



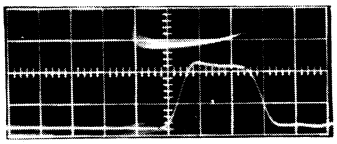
CTP 309
10 ma/div
.02 μsec/div



HD2182
10 ma/div
.02 μsec/div



Ray 295
5 ma/div
.02 μsec/div



HD2109
5 ma/div
.02 μsec/div

TABLE 2.3-II

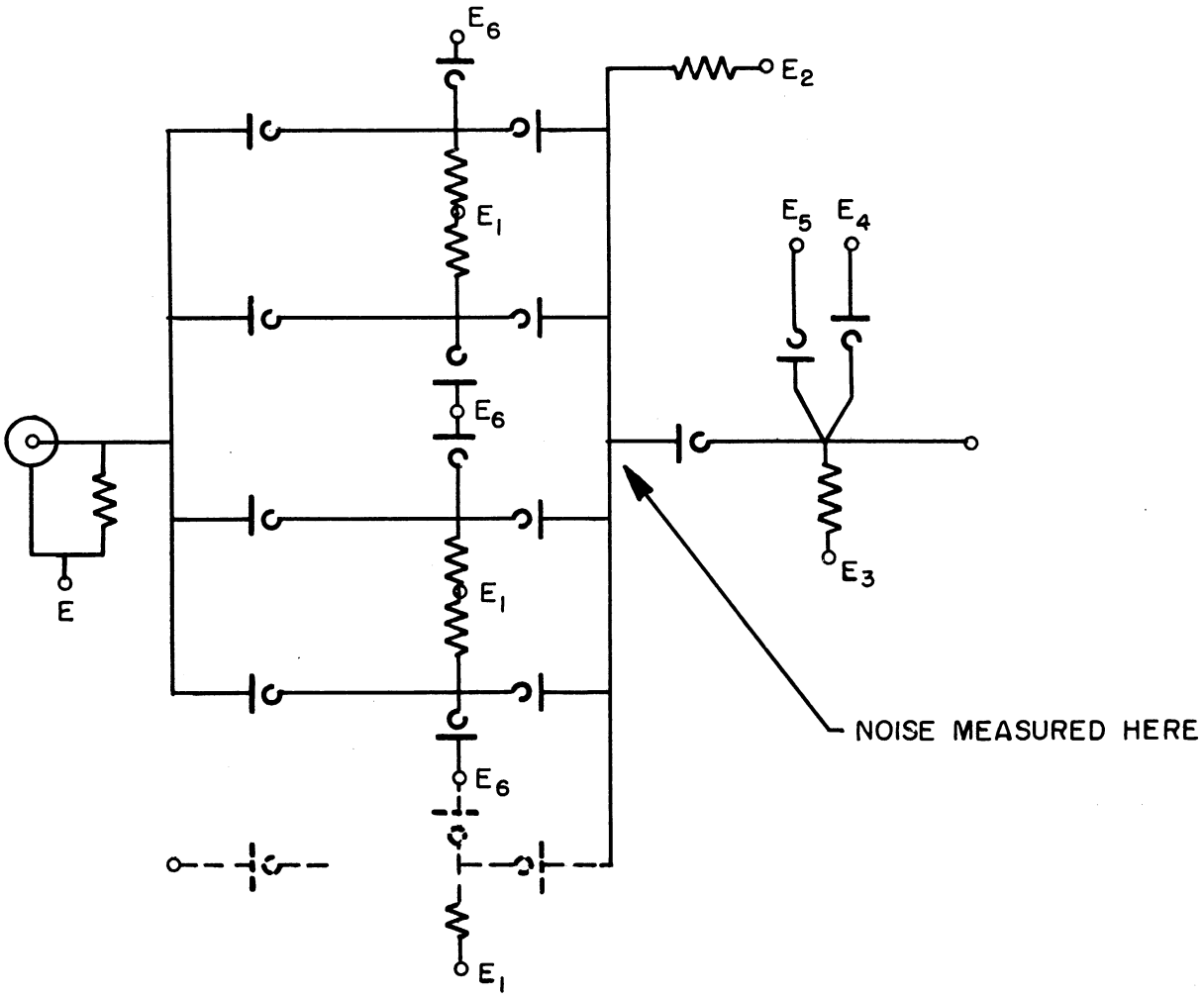
EXPERIMENTAL DETERMINATION OF THE BEST "AND" DIODE

Input Clamp Diode	"And" Diode	Total Noise	Static Noise	
			Meas.	Comp.
2109	309	.7	.35	.16
2109	2182	.9	.4	.25
2109	295	.9	.6	.61
*2109	2109	.55	.32	.38

*Best diode

TABLE 3.2-I

SECONDARY FACTORS AFFECTING NOISE



n	E_o	Total Noise	Static Noise	Currents
5	3.0	.48	.32	I = 8 ma
5	4.8	.52	.32	I' = 12 ma
5	3.0	.60	.40	I = 12 ma
5	4.8	.65	.40	I' = 16 ma

n = number of inputs to "and" gate
n-1 inputs pulsed in all cases
All diodes are Hughes 2109's.

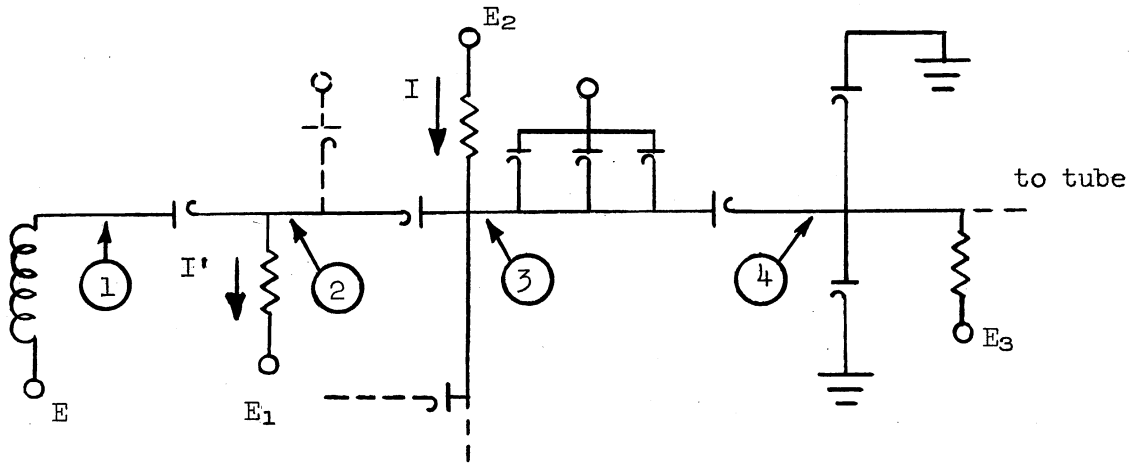
APPENDICES

APPENDIX A

OTHER LOGIC CIRCUIT CONFIGURATIONS

Two other gate configurations were considered in addition to that used in Fig. 3.2-1a. The salient features of these two gate configurations and the reasons for discarding them in favor of the one of Fig. 3.2-1a will be outlined below.

The first gate configuration is derived by placing the input clamps at the junction of the "and-or" rather than at the input of the "and." The circuit is shown in the following figure.

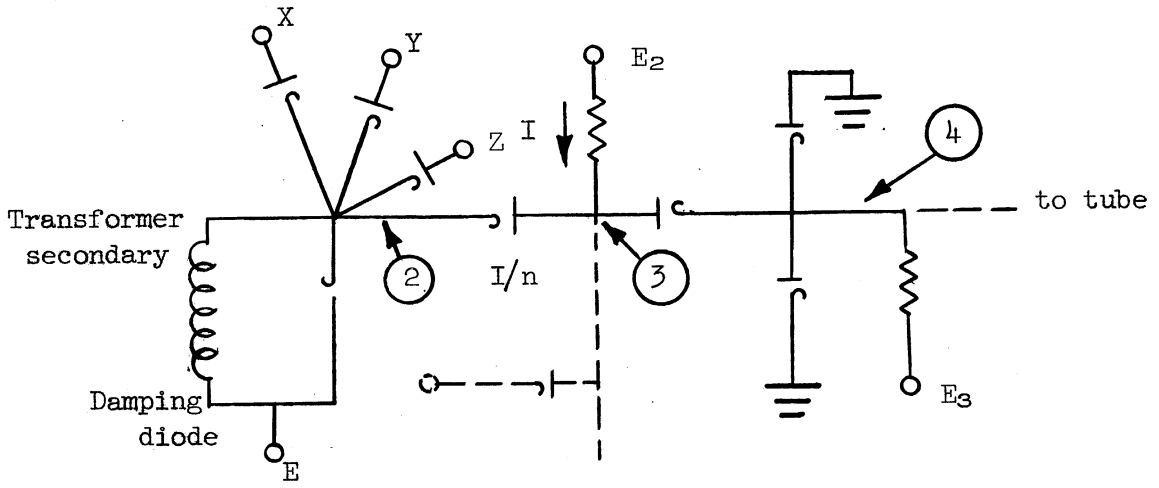


The advantage of this circuit is that it reduces the noise due to direct clamping of point (3) at point (3) rather than at point (2) as done in the circuit of Fig. 3.2-1a. The reason the noise is reduced is that the static noise due to the change in the steady-state conduction across the "and" diode is eliminated completely. The main disadvantage with this method of clamping is that there is a loss of gate current I to the clamp diodes when conduction through the gate is desired.

The second gate configuration considered could be called a "simplified secondary gate" where the need for the input clamp is eliminated completely. The circuit of this "simplified secondary gate" is shown in the following figure.

One of the theoretical advantages of this circuit is the elimination of the clamp at point (2). In addition, the current required to drive a particular gate in this circuit is I/n initially, as it is necessary to replace the

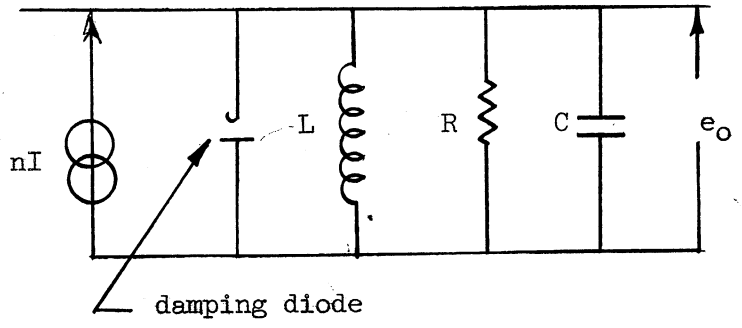
n Input "and" gate



current flowing through the "and" diode before the pulse. After the diode has been back-biased, the only load current is the current necessary to charge the capacitance at the input. The current required to drive the particular gate shown in Fig. 3.2-1a is 12 ma as against I/n for this case where n is the number of "and" inputs. Thus a substantial reduction in gate drive current can be realized.

The disadvantage of this circuit is that there is a large amount of noise developed across the transformer secondary when all the "and" gates that the unpulsed secondary would normally pulse (x,y,z...) experience the worst noise situation (n-1 gates are pulsed on a particular "and" gate).

The situation can be analyzed, assuming that a current of amplitude nI is impressed on the unpulsed secondary. A simplified representation of the impedance seen looking into the secondary of the unpulsed transformer is:



L = 10 μh
C = 10 μμf
R = 5 KΩ

Using operational mathematics to solve for $e_o(t)$ it is found that

$$e_o(t) = \frac{nI}{C\omega_o} \exp\left(-\frac{2\pi K}{T_o}\right) \sin \omega_o t \ ,$$

where

$$K = \frac{1}{2R}\sqrt{\frac{L}{C}} = \frac{1}{2Q} \ , \text{ and}$$

$$T_o = 2\pi \sqrt{LC} \ .$$

If the above equation is plotted, it is found that the maximum voltage developed across the equivalent R, L, C is

$$\text{noise} = \frac{.96\ nI}{\sqrt{C/L}} = \frac{.96\ nI}{\sqrt{10}} \text{ volts}$$

$$\cong n \times 2 \text{ volts for } I = 8 \text{ ma} \ .$$

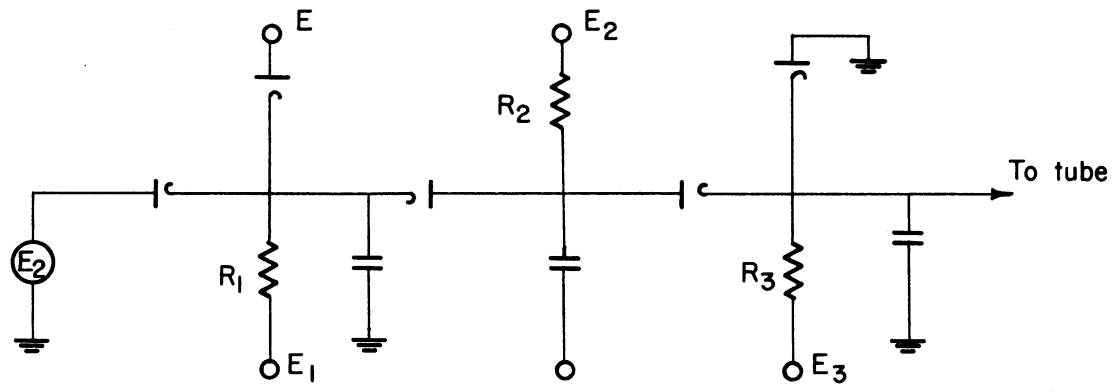
Experimental results show that the noise is of this order of magnitude, thus justifying the abandonment of this configuration.

In summarizing the disadvantages of these configurations, the poor conduction of the first and noise of the second justifies the use of the gating circuit shown in Fig. 3-2-1a.

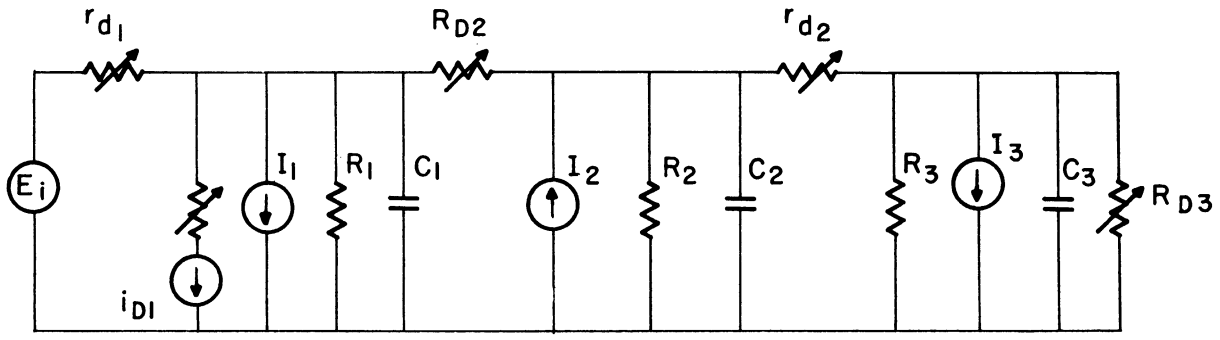
APPENDIX B

"OR-AND-OR" CIRCUIT ANALYSIS

As mentioned in an earlier report, an analytical study of an "or-and-or" gating structure has been made. The circuit that was studied is shown in the following figure. It was hoped that once a solution could be found that would define the operation of the circuit, it would be possible to vary the different parameters of the circuit to give optimum operation.



An approximate equivalent circuit of the above follows:



The analysis of the above circuit can best be done using a nodal analysis technique. The nodal equations follow.

$$I_i(t) - I_1 = (G_1 + 2G_D)\, E_1 + C_1 \frac{dE_1}{dt} - G_D\, E_Z \quad ; \tag{1}$$

$$I_2 - I_3 = -G_D\, E_1 + (G_4 + 2G_D)\, E_2 + C_4 \frac{dE_Z}{dt} \quad , \tag{2}$$

where the following assumptions and substitutions are made:

(a) $R_{D1} = R_{D2} = R_{D3} = 1/G_D$

(b) $r_{D1} = r_{D2} = 0$

(c) $i_{D1} = 0$

(d) G_1 = parallel combination of R_1 and R_{source}

(e) $G_4 = G_2 + G_3$

(f) $C_4 = C_2 + C_3$.

Now let

$$I_4 = I_2 - I_3$$

$$I'_{in}(t) = I_{in}(t) - I_1 \quad .$$

Using the above substitutions it is found that

$$I'_{in}(t) = [K_1 + f(t)]\, E_2 + [K_2 + g(t)]\, \dot{E}_2 + h(t)\ddot{E}_2 \quad ,$$

where K_1 and K_2 are constants to be evaluated.

The solution for this type of equation is rather difficult to come by. Therefore, to solve the equation the assumption is made that C_1 is small enough to be neglected. The new equations are now as follows:

$$I'_{in}(t) = (G_1 + 2G_D)\, E_1 - G_D\, E_2 \tag{3}$$

$$I_4 = -G_D\, E_1 + (G_4 + 2G_D)\, E_2 + C_4 \frac{dE_2}{dt} \quad . \tag{4}$$

Solving these for E_2,

$$\frac{dE_2}{dt} + \frac{\frac{G_1 G_4}{G_D} + 2G_1 + 2G_4 + 3G_D}{\frac{C_4 G_1}{G_D} + 2G_4}\, E_2 = \frac{I'_{in}(t) G_D + (G_1 + 2G_D)\, I_4}{C_4 G_1 + 2C_4 G_D}$$

or

$$\frac{dE_2}{dt} + f_1(t)\, E_2 = f_2(t) \quad , \tag{5}$$

where

$$f_1(t) = \frac{\frac{G_1 G_4}{G_D} + 2G_1 + 2G_4 + 3G_D}{\frac{C_4 G_1}{G_D} + 2C_4} \quad ; \tag{6}$$

$$f_2(t) = \frac{I_{in}(t)\, G_D + (G_1 + 2G_D) I_4}{C_4 G_1 + 2C_4 G_D} \quad . \tag{7}$$

There are several ways of solving this linear equation of the first order. The first is a solution of the following type:

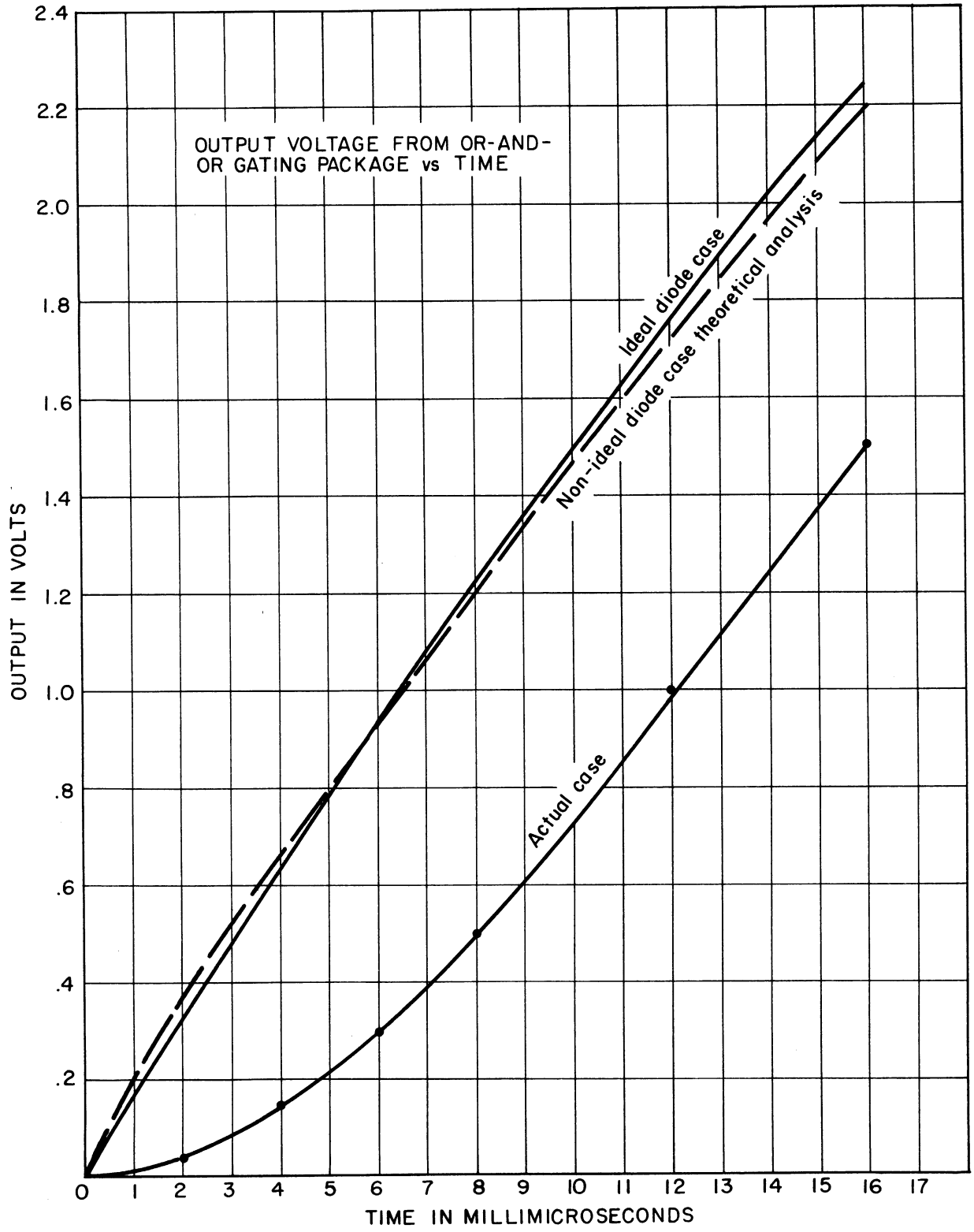
$$\frac{dy}{dx} + f_1(x)y = f_2(x)$$

$$y = e^{-\int f_1(x)dx} \int e^{\int f_1(x)dx} f_2(x)dx + ce^{\int f_1(x)dx} \quad . \tag{8}$$

Another method for getting a solution is a numerical integration of the differential equation.

The results of the two means of solution mentioned and the output from an ideal diode circuit and actual diode circuit are shown in the following figure.

Due to the amount of calculations necessary for a solution the initial objective of this phase of the work was never realized, i.e., no variance of the circuit parameters was tried.

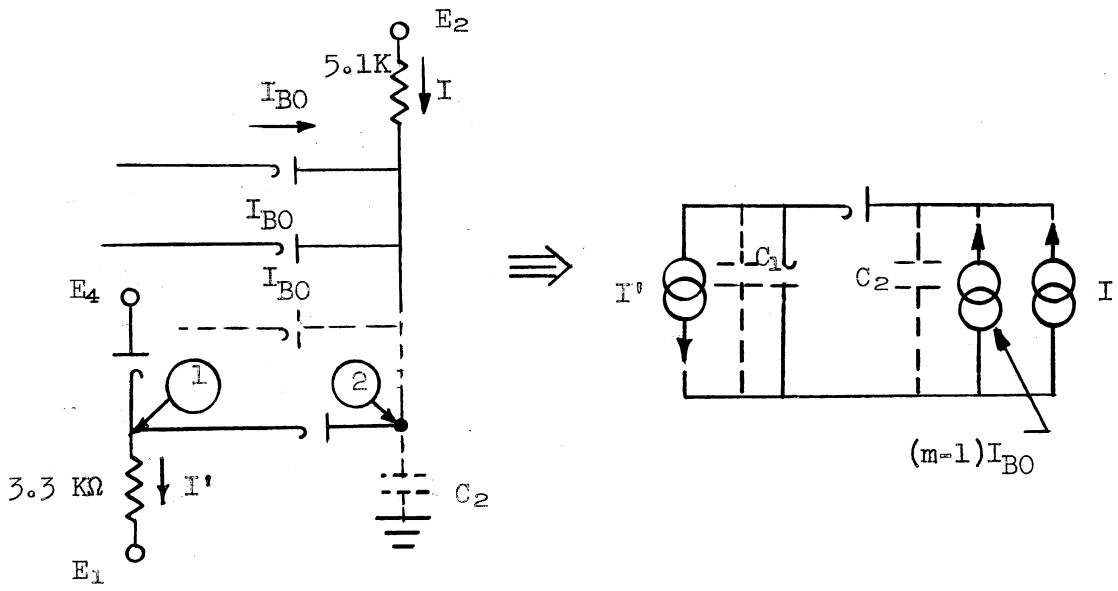

OUTPUT VOLTAGE FROM OR-AND-OR GATING PACKAGE vs TIME
OUTPUT IN VOLTS
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
.8
.6
.4
.2
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
TIME IN MILLIMICROSECONDS
Ideal diode case
Non-ideal diode case theoretical analysis
Actual case

APPENDIX C

SERIES RESISTANCE SEEN BY THE PULSED "AND" DIODE

The series resistance seen by the pulsed "and" diode is approximately the forward resistance of the input clamp diode.

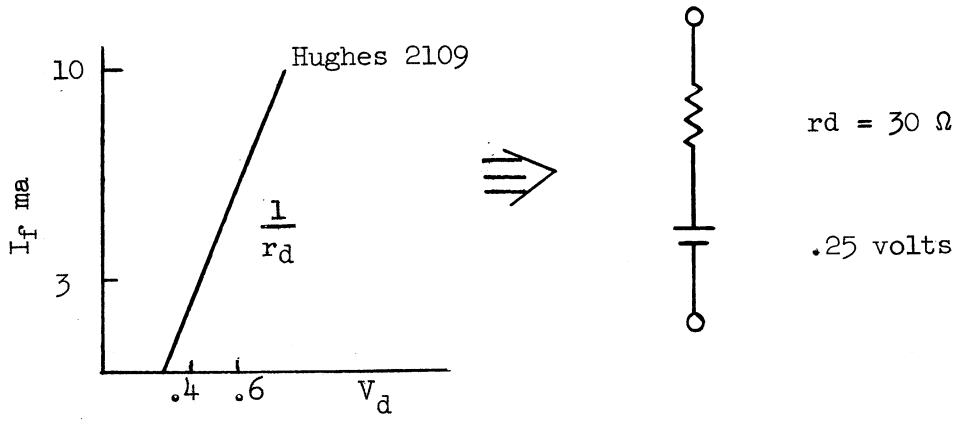
Let I_{BO} be the reverse current of a pulsed "and" diode of an "or" input gate where all but one of the inputs are pulsed.



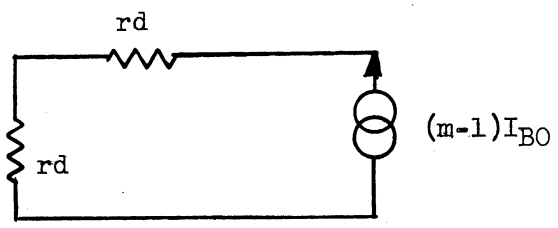
The voltage sources E_1 and E_2 in series with the large resistances may be replaced by current generators I' and I as the voltage at points (1) and (2) changes very little. The reverse currents I_{BO} of the pulsed "and" diodes can then be simulated by a current generator $(m - 1)I_{BO}$.

If a linear approximation is made for the diode static characteristic, a complete analysis of this circuit can be performed with the aid of superposition. Assume then that the input clamp is simulated by a battery and a conductance equal to the slope of the static characteristics.

If we confine our interest to the step in the process of superposition associated with the $(m - 1)$ I_{BO} current generator, we find that it sees an impedance $2r_d$. It is assumed that the internal impedance of the other current generators is infinite.



The current and voltage generator are replaced by their internal impedance, and neglecting capacitance the following equivalent circuit is obtained.

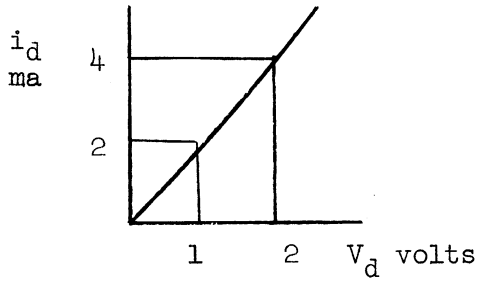


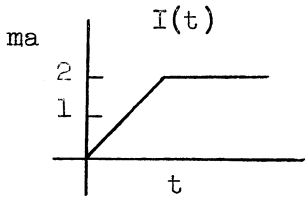
APPENDIX D

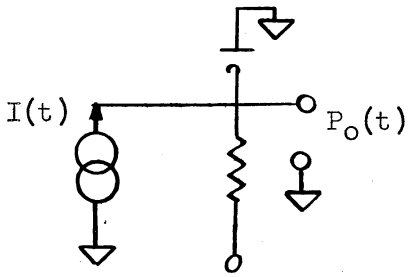
IMPEDANCE OF THE GRID-CLAMP DIODE

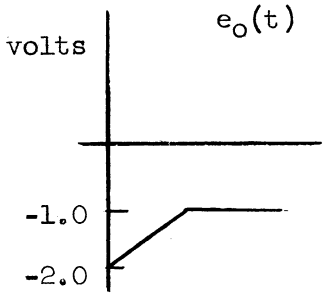
A detailed look at the grid-clamp diode (or input clamp) produces some conclusions about diode behavior in the circuit. As a first approximation the grid "or" diode and "and" pull-up can be replaced by a current source during the pulse. Also, it is reasonable to assume that a diode under pulse conditions can be described by its forward characteristics when going from two states of forward conduction. Consider a diode with a very poor static characteristic. If a current input I(t) is applied, the output will rise by one volt. Note the clamp diode has not been back-biased by this input. The disadvantage of a diode with the type of static characteristic shown in the figure below is that the output must be developed across the low impedance of the diode.

Diode Static Characteristics



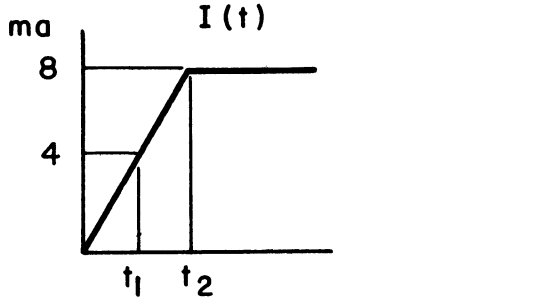




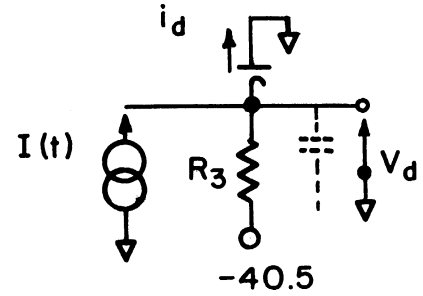


The grid-clamp diode experiences a similar problem when the grid is pulsed. Consider a ramp input of current to the grid-clamp diode. The diode

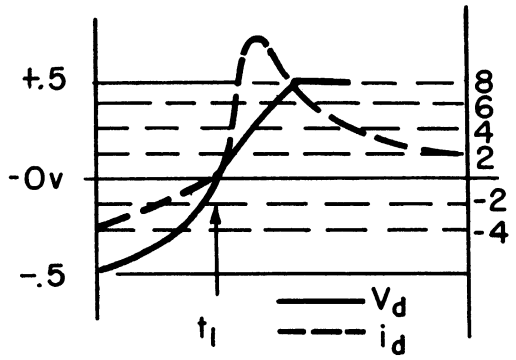
current and voltage wave-form are shown below. As the forward diode current is reduced, the dynamic resistance of the diode approaches infinity. This is certainly reasonable as low resistance about t_1 would short all input current to ground. At times $t_1(+)$ the initial reverse current is considerably greater than those measured with the Tektronics 545 (due to the limit bandwidth). The impedance after the discontinuity will be the diode end-region resistance and will increase to values in the megohm range for times much greater than t_1.

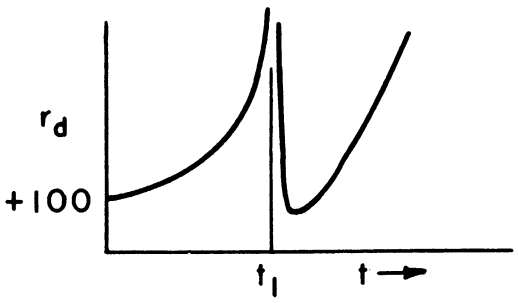


DIODE CURRENT AND VOLTAGE



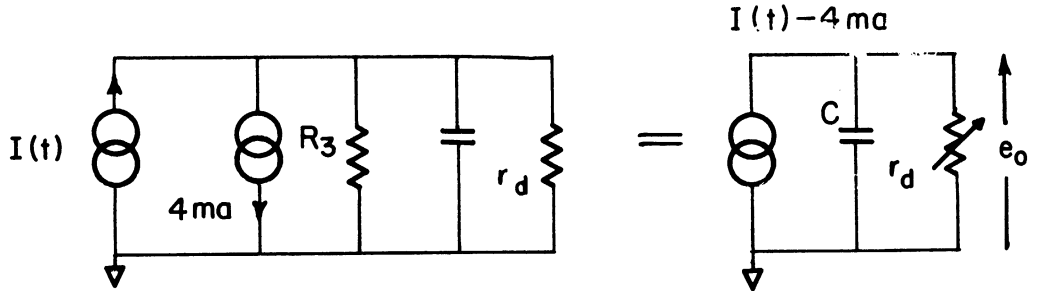
DIODE IMPEDANCE





When the diode has switched at time t_1, the output voltage is developed across a low impedance before, and for a short time after, switching. The important property of a good back-transient diode is that this impedance becomes large after a comparatively short time (15 mμsec).

An equivalent circuit can be obtained for the above clamp circuit at times of low impedance. The 40.5 volt supply and 10 K resistor can be replaced by a 4 ma current source. A diode can be replaced by an equivalent nonlinear resistance $2r_d$.


I(t)
4ma
R3
rd
=
I(t)−4ma
C
rd
eo

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