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Guest Editor's Introduction

The late 80s and early 90s ushered in the era of multimegabit memories. As the density of multimegabit RAMs is quadrupling each year and quickly pushing itself to the limit of 1 Gb by the turn of this century, major challenges are being posed to the test engineers. The complexity and cost of testing and test equipment are ever-increasing. New defect mechanisms are being caused by drastic changes in the structure and layout of the storage cell. These new defect mechanisms may potentially produce more types of faults. Some existing functional and electrical algorithms need to be speeded up significantly. Also, accurate fault and defect diagnosis have become very important for two reasons—(a) to provide feedback to the memory chip designers which will help them to improve yield, and (b) to facilitate built-in self-repair (BISR) of memory cell arrays. These issues are becoming increasingly important and we have, therefore, selected the following five papers in this special issue. These papers will familiarize the readers with these challenging problems facing the test engineers of this decade.

Cockburn's tutorial on semiconductor memory testing is very useful to a beginner in this area, because it summarizes several important papers on memory fault modeling and testing. He describes the structure and operation of SRAM and DRAM cell arrays and reviews both production testing and built-in self-testing (BIST) of memories. He provides the reader with a quick exposure to the main issues challenging the memory test engineers—possibility of new defect mechanisms as device line widths of the present-generation multimegabit memories shrink further and as storage becomes more three-dimensional, potential slowdown of existing algorithms for increasingly complex and gargantuan memories, and the necessity of making memory fault diagnosis more sophisticated.

Van de Goor and Zorian describe tests for a special class of memories that are single-order-addressed (SOA). In these memories, the address can only change in one direction. Such memories are used in FIFOs and in applications where the BIST area overhead or the delay penalty has to be minimized. The authors have described a number of march tests that detect such faults. March tests have a good fault coverage and are very attractive from the BIST point of view.

Chakraborty and Mazumder have highlighted the importance of technology and layout-related testing of static RAMs. Most conventional test algorithms for functional and electrical testing fail to achieve a high *defect* coverage. As multimegabit SRAMs become increasingly complex and humongous in size, it has become essential to detect and diagnose *cell layout defects* also in addition to the faults that they cause. Various approaches for defect and fault modeling based upon the cell technology and layout are described by the authors.

Saluja has given a good overview of BIST techniques for stand-alone RAMs. He describes techniques for speeding up well-known test algorithms. He suggests both architecture-based parallelism in which multiple cell arrays are tested simultaneously and DFT-based parallelism in which the testing scheme inherently contains some parallelizable steps, such as multiple cells being read/written in one step or multiple input shift register (MISR) being used to compress the signature from multiple cells. He then describes two efficient algorithms to test static RAMs for neighborhood pattern-sensitive faults (NPSFs). The second algorithm forms a key contribution to the literature on functional testing because it works well for *any* arbitrary manner of mapping logical addresses to physical addresses.

Kebichi, Yarmolik and Nicolaidis discuss zero-aliasing BIST for signature analysis of ROMs. The test pattern generator for a ROM BIST is an autonomous counter generating the set of input combinations exhaustively, such as an LFSR with primitive characteristic polynomial. A serious problem with fault detection for ROMs is that of aliasing during signature analysis. The authors mathematically compute the design of an aliasing free signature analyzer by examining the algebraic properties of the primitive characteristic polynomial for both bit- and word-oriented ROMs. They have also designed suitable compactors for their signature analysis scheme.

The overall aim of this special issue is to expose the most important problems that are confronted during both production testing and built-in self-testing of multimegabit semiconductor memories of this decade. Other important issues, such as low area-overhead BIST implementation, high fault coverage, simplicity and regular structure of test algorithms for ease of BIST implementation, etc., have always retained their importance and are discussed in various books, surveys, journals and conferences. They have not been emphasized in the present issue because we wish to focus on the more recently observed problems facing test engineers. Most of these problems arise from new defect mechanisms associated with drastic changes in the cell technology, innovative storage mechanisms such as three-dimensional storage, and complexities in the associated process and design. I wish to thank our reviewers for reviewing a large number of papers within a very short time to enable the quick publication of this issue. I would also like to thank Mr. Kanad Chakraborty, my Ph.D. student, for devoting a considerable amount of time to this special issue.

Pinaki Mazumder
Guest Editor
The University of Michigan
mazum@eecs.umich.edu