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# Extremely-Wide-Range Supply-Independent CMOS Voltage References for Telemetry-Powering Applications

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**Abstract.** This paper reports a voltage reference circuit in standard CMOS process. It exhibits excellent supply independency for a wide input voltage range, which is of great importance in telemetry-powered systems. This circuit is based on the well-known $V_{GS}$-reference supply-independent *current reference* circuit, but it is designed to serve as a *voltage reference*. While the reference current generated by this circuit varies with the supply voltage, a self-compensating mechanism can be found in voltage-mode operation of the circuit that results in a supply-independent reference voltage. This supply independency is well observed in the static operation of the circuit over an extremely wide input range, as well as in its dynamic behavior for high frequency ripples on the input voltage. Based on the proposed idea, a multi-output voltage reference and a CMOS DC level shifter are also designed. The proposed voltage reference circuits have been fabricated using MOSIS 1.6 $\mu$m standard CMOS process. The basic voltage reference provides 957 $\mu$V/V static supply dependency, rejects input ripples of up to 8 MHz by $60 \pm 3$ dB, and consumes only 15.8–36.9 $\mu$A when the input voltage varies in the range 2.6–12 V.

**Key Words:** voltage reference, DC level shifter, supply-independent circuits

## 1. Introduction

Telemetry powering is of interest in some advanced branches of technology like biomedical implantable micro-systems used for nerve stimulation, neuromuscular stimulation, and neural recording. Long-term and even lifelong operation without any replaceable energy source (e.g. batteries), ease of movement without being restricted by power wires, and avoiding the risk of infection and patient discomfort caused by percutaneous wires, necessitate the biomedical implantable microsystems to wirelessly communicate and be energized [1–5]. To realize this idea, the energy required for the operation of such systems is transferred from an external source to the implanted system by using an external transmitter and an internal receiver. The received waves are rectified and then regulated in order to provide the supply voltage for the implanted system. In such systems, because of transmitter or receiver movements, the distance or alignment between the transmitter and the receiver antennas varies, thus resulting in disturbances or variations in the induced voltage on the receiving antenna. To have a stable supply voltage in the presence of such input variations, the voltage regulator should be able to operate over a wide range of input voltages, and at the same time the output voltage should be highly input independent.

To serve as the voltage reference in the required voltage regulator, regular and Zener diodes have been employed in [2] and [3–5], respectively. But because of the non-negligible diode series resistance, the reference voltage would not be satisfactorily constant when the input voltage drastically changes.

Disregarding its temperature dependence, the $V_{GS}$-referenced supply-independent current reference circuit shown in Fig. 1 is a good reference circuit, although it shows much more supply dependency than its bipolar counterpart [6]. It is shown in the next section that there can be found a self-compensating mechanism in *voltage-mode operation* of the same circuit that can result in a stable *reference voltage* over an extremely wide range of input changes, provided that it is properly designed [7]. Based on this mechanism, a multi-output voltage reference [8] and also a DC level shifter will be proposed in the next sections.

## 2. Circuit Concept and Design

Assuming that $I_R$ is constant in the $V_{GS}$-referenced circuit of Fig. 1, then $V_{GS1}$ and $V_{GS2}$ are also constant. So, $V_{GS1} + V_{GS2}$ that appears at node A can be considered as a constant reference voltage:

$$V_{\text{REF}} = V_{GS1} + V_{GS2} \tag{1}$$

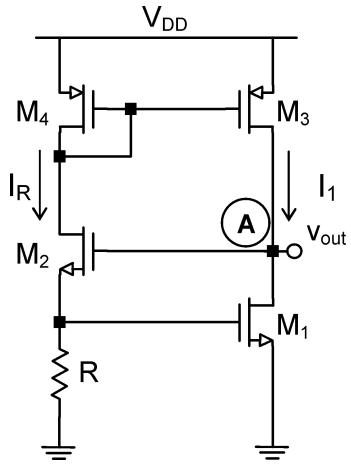


*Fig. 1.* $V_{GS}$-referenced supply-independent reference circuit.

But it is known that $I_1$, and to some extent $I_R$, vary with supply voltage and hence the above reference voltage tends to follow supply changes. When the supply voltage ($V_{DD}$) is increased, $V_{SD3}$ and consequently $I_1$ will increase. This causes $V_{GS1}$ to increase with $V_{DD}^{1/2}$, which sets the current through $R$ ($I_R$). However it seems that this will cause $V_{GS2}$ to increase with $V_{DD}^{1/4}$, but there is another factor that contributes to determining $V_{GS2}$. Remembering that:

$$V_{GS} = V_T + \{2I_D/\beta(1 + \lambda V_{DS})\}^{1/2} \tag{2}$$

$V_{DS2}$ can play a second-order role. It can be seen in the circuit that $V_{DS2}$ increases with $V_{DD}$. So, by properly setting the design parameters, it is shown that there can be found a situation that $V_{GS2}$ is so decreasing that compensates the increase of $V_{GS1}$, when $V_{DD}$ is increased, resulting in a *supply-independent reference voltage*.

Mathematically speaking, in order to achieve a supply-independent reference voltage, one should have:

$$\delta V_{\text{REF}}/\delta V_{DD} = 0 \tag{3}$$

or:

$$\delta V_{GS2}/\delta V_{DD} = -\delta V_{GS1}/\delta V_{DD} \tag{4}$$

As is derived in the Appendix, solving device and circuit equations for the above relationship leads to the following optimization equation:

$$(R\sqrt{2I_R}) \cdot (\lambda_N \cdot \sqrt{b \cdot \beta_1} - \lambda_P \cdot \sqrt{a^3\beta_2}) = b\lambda_N + a\lambda_P \tag{5}$$

which relates the proper $W/L$ ratios for $M1$ and $M2$ and resistance $R$, where $a = 1 + \lambda_N(V_{DD} - V_{\text{REF}})$ and $b = 1 + \lambda_P(V_{DD} - V_{\text{REF}})$.

It is obvious that the basic design is done for obtaining the reference voltage, by:

$$V_{\text{REF}} = 2V_{TN} + \sqrt{2I_R}.(\sqrt{b/\beta_1} + 1/\sqrt{\beta_2}) \tag{6}$$

Note that Eq. (6) is written neglecting body effect for $M2$. The only impact of the body effect would be on the value of the reference voltage, not its supply independency. In order to keep the simplicity of design Eqs. (5) and (6), the designer can solve them in order to have a rough estimate for channel sizes of $M1$ and $M2$, which play the most important role in optimizing the circuit. Then, the channel sizes can be trimmed by simulation in order to optimize the circuit considering the body effect and other second-order factors.

As a case study, the circuit of Fig. 1 is optimized for a 1.6 V reference voltage using MOSIS 1.6 $\mu$m standard CMOS process. However there are processes with smaller feature sizes available, the reason for choosing such a large feature size (the largest available through MOSIS) is as follows: In telemetry powering applications the received voltage at the input of the front-end is supposed to be high enough to result in a stable supply voltage, after considering all the voltage overheads for the rectifier, the voltage reference, and also the other blocks in the voltage regulator. So, the process with the largest possible feature size has been chosen in order to achieve the highest tolerable voltages for the transistors.

In this case, design parameters are determined to be as follow:

$$(W/L)_1 = 80\ \mu/1.6\ \mu \quad (W/L)_2 = 4\ \mu/1.6\ \mu$$
$$(W/L)_{3,4} = 4\ \mu/1.6\ \mu \quad R = 70\ \text{k}\Omega$$

Figure 2 illustrates the more important waveforms for the optimized case. As is expected, $V_{GS2}$ decreases with increasing $V_{DD}$, exactly with the same rate that $V_{GS1}$ increases, and the result is a flat $V_{\text{REF}}$ over a wide supply voltage range.

Increasing $V_{DD}$ from its minimum acceptable value of about 2.4 up to 20 V leads to a maximum deviation of 9 mV (511 $\mu$V/V) from the 1.625-V reference voltage. Over this wide supply voltage range, the current consumption of the circuit varies between 15 and 43 $\mu$A.

### *2.1. Dynamic Behavior*

Although the DC transfer curve for the voltage reference circuit is quite flat for $V_{DD}$ greater than $V_{DD}$ (min), it should be noted that it only shows static dependency of the reference voltage on $V_{DD}$ variations. However, ripples on the unregulated supply rail ($V_{DD}$) appear in an AC or dynamic nature. Simulations show that the circuit

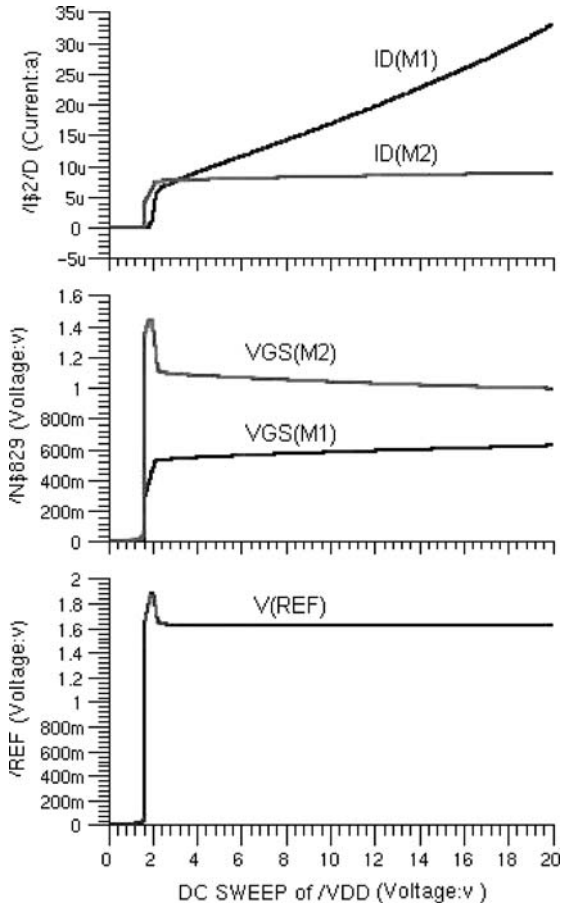


*Fig. 2.* Important currents and voltages in the optimized voltage-reference circuit.

rejects ripples by about −59 dB with 3 dB frequency of 1.5 MHz.

It is obvious that like many other supply dependent reference circuits, the circuit of Fig. 1 has two stable states and requires a startup circuit to guarantee its operation in the desired operating point.

## 3. DC Level Shifter

Theoretically, a voltage reference circuit generates a *constant voltage difference between the output node and the ground*. In another area of analog circuits there are DC level shifters whose functional behavior can be defined as providing a *constant voltage difference between the output and the input nodes*. Designing the complementary version of the circuit of Fig. 1 would result in an excellent CMOS DC level shifter, as is shown in Fig. 3.

Shown in Fig. 4 is the DC level shift as a function of the input voltage, which demonstrates excellent input independency over a very wide range of the input. The optimized behavior of the circuit in MOSIS 1.6 $\mu$m standard CMOS process is achieved by the following

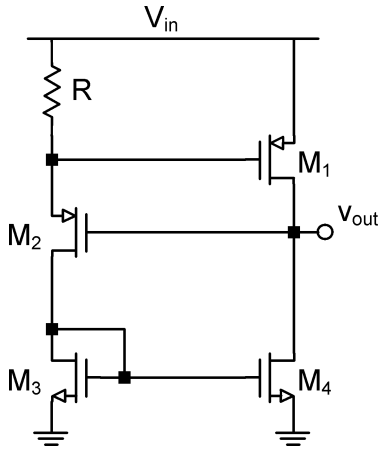


*Fig. 3.* Schematic of the proposed CMOS DC level shifter.

design parameters:

$$(W/L)_1 = 80\,\mu/1.6\,\mu \quad (W/L)_2 = 4\,\mu/4\,\mu$$
$$(W/L)_{3,4} = 4\,\mu/1.6\,\mu \quad R = 70\,\text{k}\Omega$$

In this case, the DC level shift is 3.081 V ± 8 mV when the input voltage varies from about 3.5 to 20 V. This means that the DC level shift depends on the input voltage just by less than 0.5 mV/V, and the circuit is well operating by an overhead voltage of as low as 0.42 V (in this case).

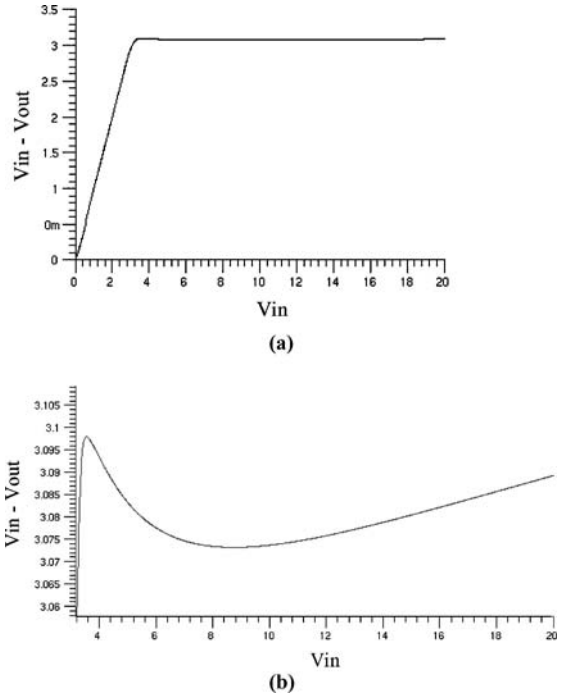


*Fig. 4.* DC level shift as a function of the input voltage (a) broad view and (b) close view.

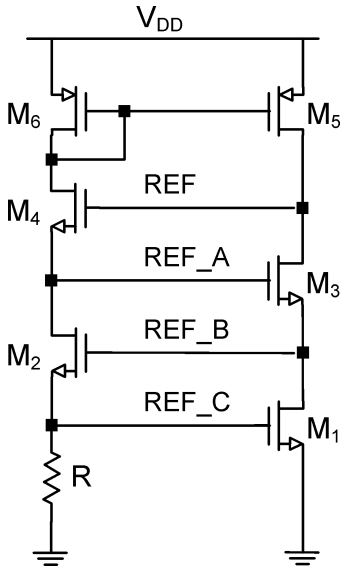


*Fig. 5.* Proposed multi-output voltage reference circuit.

## 4. Multi-Output Voltage Reference Circuit

As was described in Section 2, assuming that $I_R$ is constant in the $V_{GS}$-referenced circuit of Fig. 1, as $V_{DD}$ increases, $I_{D1}$ and $V_{GS1}$ increase with $V_{DD}$ and $V_{DD}^{1/2}$, respectively. The key point for optimizing the circuit is that transistor $M2$ should be so designed that its $V_{GS}$ should decrease with $V_{DD}^{1/2}$ with such a rate that compensates the increase of $V_{GS1}$. So, the reference voltage $V_{\text{REF}} = V_{GS1} + V_{GS2}$ would be a $V_{DD}$-independent voltage.

Now, if we stack more transistors, the reference voltage will be the summation of more $V_{GS}$ terms, and obviously at a higher voltage level. Another benefit is to achieve more reference voltages with lower values at the lower nodes. Figure 5 shows the proposed voltage reference circuit that realizes this idea. Like in the circuit of Fig. 1, the current in the right hand side of the proposed circuit increases with $V_{DD}$, and hence $V_{GS1}$ and $V_{GS3}$ increase with $V_{DD}^{1/2}$. Again, transistor $M4$ can be so sized that compensate the accumulated increase with $V_{DD}^{1/2}$ caused by $M1$ and $M3$. The reason for such a behavior is that since the drain current and drain-source voltage of transistor $M4$ are being increased, satisfying the characteristic equation:

$$V_{GS} = V_T + \{2I_D/\beta(1 + \lambda V_{DS})\}^{1/2} \qquad (7)$$

implies that there is no way for its $V_{GS}$ but decreasing.

As a case study, optimizing the circuit of Fig. 5 for a 4 V main reference voltage in MOSIS 1.6 $\mu$m standard CMOS process will result in the following design parameters:

$$(W/L)_{1,3} = 80\ \mu/1.6\ \mu \quad (W/L)_{2,4} = 11.2\ \mu/10\ \mu$$
$$(W/L)_{5,6} = 4\ \mu/4\ \mu \quad R = 70\ \text{k}\Omega$$

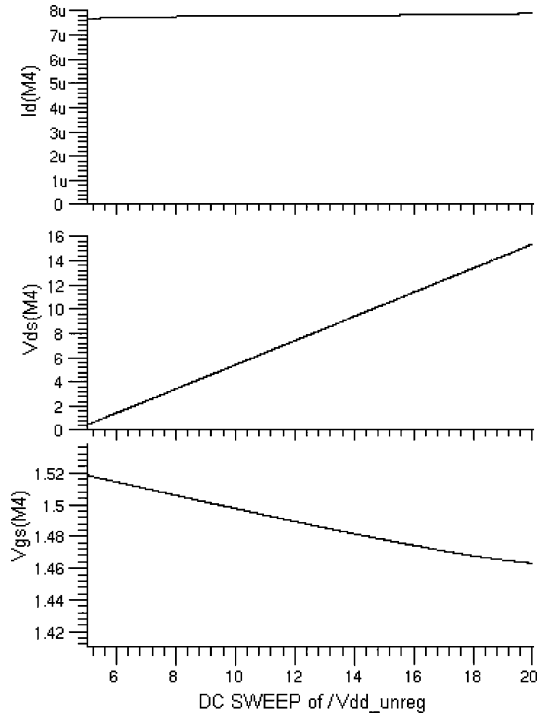


*Fig. 6.* $I_D$, $V_{DS}$, and $V_{GS}$ for $M4$, as $V_{DD}$ increases.

In this case as $V_{DD}$ increases, $I_D$, $V_{DS}$, and $V_{GS}$ for M4 will be as shown in Fig. 6.

As the result, Fig. 7(a) demonstrates how $V_{GS4}$ has been capable of overcoming the accumulated increasing behavior of the three other gate-source voltages (i.e. $V_{GS1} + V_{GS2} + V_{GS3}$). As the legends state, the traces are for $V_{\text{REF\_C}}$, $V_{\text{REF\_B}}$, $V_{\text{REF\_A}}$, and $V_{\text{REF}}$, from bottom to up. It is a great achievement that over a 15-V input range, from 5 to 20 V, the increase in the reference voltages $V_{\text{REF\_C}}$, $V_{\text{REF\_B}}$, and $V_{\text{REF\_A}}$ is only 15, 25, and 40 mV, respectively, and the above-pointed self-compensating behavior limits the deviation in $V_{\text{REF}}$ to less than 25 mV.

DC transfer curves for the four reference voltages, generated by the proposed circuit, are given in Fig. 7(b).

Simulations show that over the 15-V input range, current consumption of the circuit varies between 15 and 17 uA.

### *4.1. Dynamic Behavior*

Although the DC transfer curve for the voltage reference circuit is quite flat for $V_{DD}$ greater than $V_{DD}$ (min), it should be noted that it only shows static dependency of the reference voltage on $V_{DD}$ variations. However, ripples on the unregulated supply rail ($V_{DD}$) appear in an AC or dynamic nature. Simulations show that the circuit rejects ripples by about $-52.8$ with 3 dB frequency of 10 MHz.

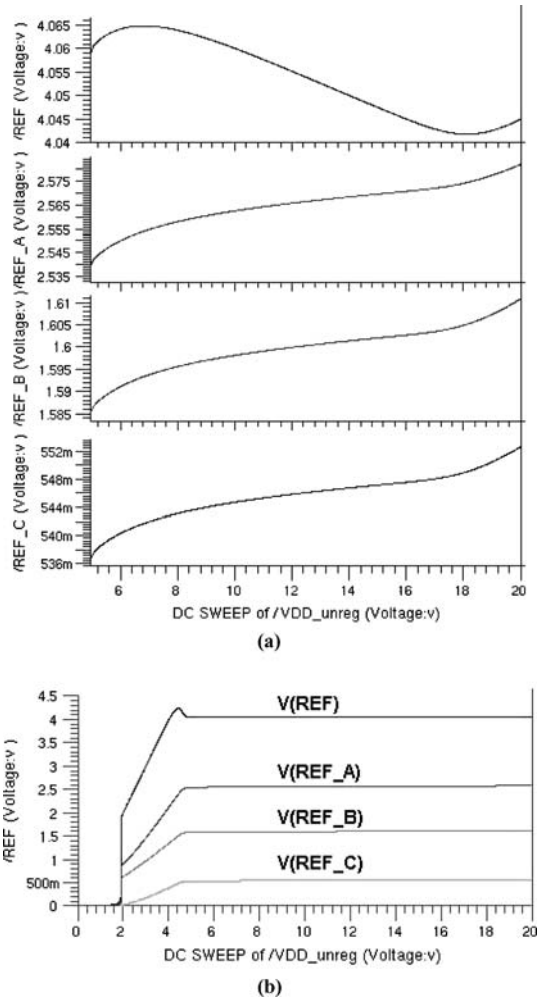


*Fig. 7.* (a) Close view, (b) broad view for the four generated reference voltages versus $V_{DD}$.

It is obvious that like many other supply dependent reference circuits, the proposed circuits have two stable states and require startup circuits to guarantee their operation in the desired operating point.

## 5. Experimental Results

### *5.1. Simple Voltage Reference*

Shown in Fig. 8 is the photograph of the proposed circuit along with its startup circuit fabricated using MOSIS 1.6 um standard CMOS process.

Figure 9 shows the simulated and measured DC transfer curves of the optimized voltage reference circuit. As can be seen, because of a slight difference between transistor threshold voltages in simulation and in practice the output voltage level has been shifted up, but it is still extremely flat over a wide range of input from 2.6 V up to as high as 12 V. This robustness (in the flatness of the input-output characteristic) against threshold voltage variations was predictable since transistor threshold voltages do not directly appear in the output flatness condition (Eq. (5)).

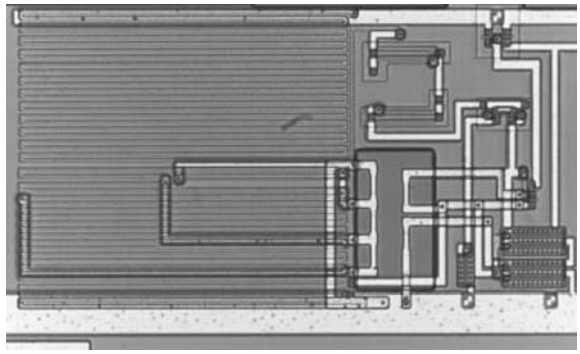

*Fig. 8.* Photo of the fabricated circuit along with its startup circuit.

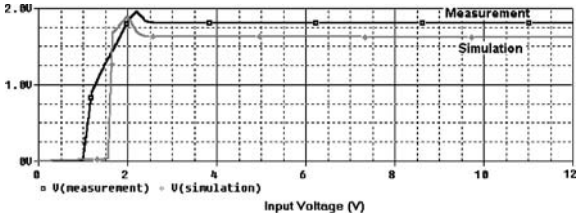


*Fig. 9.* Simulated and measured DC transfer curves for the circuit.

Although simulations show that the flatness of the DC transfer curve continues up to input voltages as high as 20 V (Fig. 2), but in practice the measurements were stopped by breakdown damages at about 10–12 V and the circuit couldn't be tested for higher voltages. However the transistors are not strong enough to tolerate very large voltages, but it should be emphasized that the optimization approach, which can be considered as the spirit of this paper, is strong enough to provide extremely robust reference voltages against very large line variations.

Figure 10 illustrates both simulated and measured Bode magnitude plots for ripple rejection ratio, which is the transfer gain from the input voltage to the generated reference voltage. The capacitance of the measuring

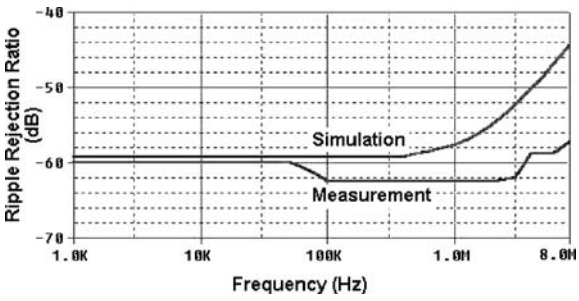


*Fig. 10.* Simulated and measured ripple rejection characteristic curves.

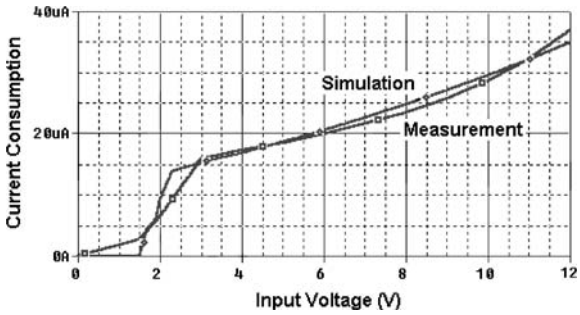


*Fig. 11.* Current consumed by the voltage reference and the startup circuits.

probe, when connected to the high-resistance output node, is the reason for achieving the measured ripple rejection curve better than the simulated one. Ripple rejection ratio for the fabricated circuit, which is a measure of its dynamic supply dependency, is within $-60 \pm 3$ dB for frequencies up to 8 MHz. This is far larger and also is valid for much wider frequency range than that of the commonly reported CMOS voltage references.

Shown in Fig. 11 are the simulated and measured current consumptions for the optimized voltage reference circuit and its startup circuit, as a function of the input supply voltage.

Table 1 summarizes the simulated and measured specifications of the voltage reference circuit, which demonstrate great performance for a wide-range supply-independent voltage reference both in simulations and experiments. Table 2 compares this optimized voltage reference circuit with three other precise voltage reference circuits reported in the literature. It is noted that the circuit reported here provides the best performance in terms of voltage stability (regulation), power consumption, and ripple rejection of all the circuits so far reported.

*Table 1.* Simulated and measured specifications of the simple voltage reference circuit.

| Specification | Simulated | Measured |
|---|---|---|
| Input voltage range | 2.4–20 V | 2.6–12 V* |
| Static supply dependency (DC) | 511 $\mu$V/V | 957 uV/V |
| Dynamic supply dependency(Ripple reject.) | −59.2 dB | −60 dB |
| Current consumption @$V_{DD} = 3$ V | 15 $\mu$A | 15.8 $\mu$A |

*Limited by breakdown.

*Table 2.* Performance comparison of this optimized simple voltage reference circuit with three other precise voltage reference circuits reported in the literature.

| Case | $I_{\text{Diss}}$ ($\mu$A) | Input range | Line regulation | |
|---|---|---|---|---|
| | | | Static | Dynamic |
| [9] | 8.6 | 1.3–3 V | 53 m V/V | – |
| [10] | 7@$3.5^V$ | 1.3–3.5 V | 45 mV/V | 34 dB |
| [11] | 89@$5^V$ | 3.3–7 V | 6.2 mV/V | 43.2 dB @1 kHz |
| This work | 18.4@$5^V$ | 2.6–12 V* | 957 $\mu$V/V | $60 \pm 3$ dB @$f \leq 8$ MHz |

*Limited by breakdown.

## 5.2. *Multi-Output Voltage Reference*

Shown in Fig. 12 is the photo of the proposed voltage reference circuit along with its startup circuit that has been fabricated using MOSIS 1.6 um standard CMOS process.

Figure 13 shows the DC transfer curves of the optimized reference circuit obtained from simulations and experiments for the main reference output. Again, the input-output characteristic curve is still extremely flat over a wide range of input from about 6 to 12 V. However simulations show that the flatness of the DC transfer curve continues up to input voltages as high as 20 V (Fig. 7) and even higher, we couldn't apply input voltages above 12 V (in some cases 14 V) since the transistors were burned out.

*Table 3.* Simulated and measured specifications of the multi-output voltage reference circuit.

| Specification | Simulated | Measured |
|---|---|---|
| Input voltage range | 5–20 V | 6–14 V* |
| Static supply dependency (DC) | 1.53 mV/V | 1.33 mV/V |
| Dynamic supply dependency (Ripple reject.) | −52.8 dB | −48 dB |
| Current consumption (voltage ref. & startup circuit) | 23 uA @20 V input | 25 uA |

*Limited by breakdown.

*Table 4.* Performance comparison of this optimized multi-output voltage reference circuit with three other precise voltage reference circuits reported in the literature.

| Case | $P_{\text{Diss}}$ | Input range | Line regulation | |
|---|---|---|---|---|
| | | | Static | Dynamic |
| [9] | 8.6 uA | 1.3–3 V | 53 mV/V | – |
| [10] | 7 uA @$3.5^V$ | 1.3–3.5 V | 45 mV/V | 34 dB |
| [11] | 89 uA @$5^V$ | 3.3–7 V | 6.2 mV/V @1 kHz | 43.2 dB |
| This work | 25 uA | 6–14 V | 1.33 mV/V | 48–57.4 dB @$f \leq 1$ MHz |

*Limited by breakdown.

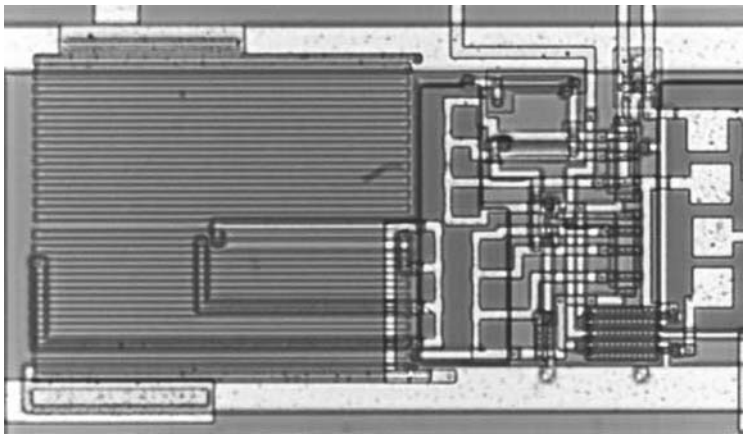

*Fig. 12.* Photo of the proposed voltage reference circuit along with its startup circuit.

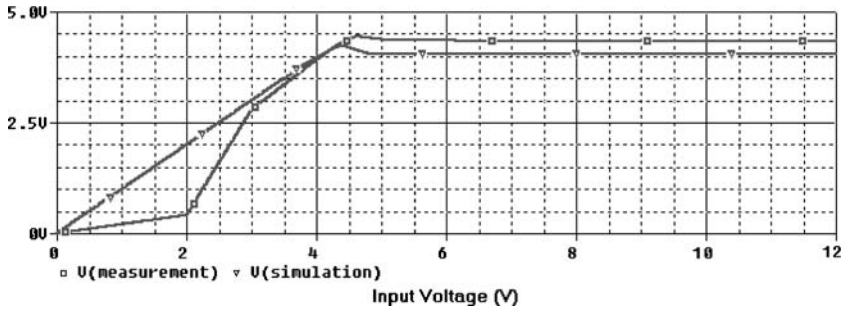


*Fig. 13.* DC transfer curves for the circuit, resulted from simulation and measurement.

Measurements show that the ripple rejection ratio of the circuit has fallen from −52.8 dB in simulations to −48 dB.

Table 3 summarizes the specification of the voltage reference circuit obtained from both simulations and measurements. Table 4 compares the optimized voltage reference circuit with three other precise voltage reference circuits.

## 6. Conclusion

A voltage reference circuit has been designed in standard CMOS process that exhibits excellent supply independency. This supply independency is well observed in the static operation of the circuit over an extremely wide input range, and also in its dynamic behavior for high frequency ripples on the input voltage. The circuit, fabricated using MOSIS 1.6 $\mu$m standard CMOS process, shows 957 uV/V static supply dependency, 60 dB ripple rejection, and consumes 15.8 to 36.9 uA when the input voltage varies from 2.6 to 12 V. **This 12-V maximum input is just the breakdown limitation that didn't let the measurements go farther, but based on the close agreements observed between simulation and experimental results, the circuit is expected to continue its highly supply independent operation for up to 20-V input.**

Based on the proposed idea, a multi-output voltage reference and a CMOS DC level shifter are also designed.

## Appendix

From the circuit we have:

$$V_{GS1} = V_{TN} + (2I_1/\beta_1)^{1/2} \quad \text{(A.1)}$$

$$V_{GS2} = V_{TN} + [2I_R/\beta_2(1 + \lambda_N V_{DS2})]^{1/2} \quad \text{(A.2)}$$

$$I_1 = I_R \cdot [1 + \lambda_P V_{SD3}] \quad \text{(A.3)}$$

$$I_R = V_{GS1}/R \quad \text{(A.4)}$$

Considering (3), and also approximating $\delta V_{DS2}/\delta V_{DD}$ to 1 for more simplification, we will have:

$$(\delta V_{GS1}/\delta V_{DD}) \cdot [\sqrt{2b\beta_1/I_R} - b/(RI_R)] = \lambda_P \quad \text{(A.5)}$$

$$\sqrt{2a^3\beta_2 R V_{GS1}}(\delta V_{GS2}/\delta V_{DD}) = [a \cdot (\delta V_{GS1}/\delta V_{DD}) - \lambda_N V_{GS1}] \quad \text{(A.6)}$$

where $a = 1 + \lambda_N V_{DS2}$ and $b = 1 + \lambda_P V_{SD3} = 1 + \lambda_P(V_{DD} - V_{\text{REF}})$.

Now, in order to have a supply-independent reference voltage, Eq. (4) helps us to rewrite (A6) as:

$$(\delta V_{GS1}/\delta V_{DD})(a + \sqrt{2a^3\beta_2 R V_{GS1}}) = \lambda_N V_{GS1} \quad \text{(A.7)}$$

and using (A4), (A7) can be rewritten as:

$$(\delta V_{GS1}/\delta V_{DD}) \cdot (a/RI_R + \sqrt{2a^3\beta_2/I_R}) = \lambda_N \quad \text{(A.8)}$$

Dividing (A8) by (A5) and rearranging the resulted equation leads to:

$$a/RI_R + (\lambda_N/\lambda_P)b/RI_R = (\lambda_N/\lambda_P)(2b\beta_1/I_R)^{1/2} - (2a^3\beta_2/I_R)^{1/2}$$

and

$$a + (\lambda_N/\lambda_P)b = R(2I_R)^{1/2}[(\lambda_N/\lambda_P)(b\beta_1)^{1/2} - (a^3\beta_2)^{1/2}]$$

and eventually:

$$(R\sqrt{2I_R})(\lambda_N\sqrt{b \cdot \beta_1} - \lambda_P\sqrt{a^3\beta_2}) = b\lambda_N + a\lambda_P \quad \text{(A.10)}$$

In order to introduce (A.10) as a design equation, $a$ and $b$ should be defined in term of known quantities. So,

$$\begin{aligned} a &= 1 + \lambda_N V_{DS2} \\ &= 1 + \lambda_N(V_{DD} - V_{SG4} - V_{GS1}) \\ &= 1 + \lambda_N(V_{DD} - V_{\text{REF}}) + \lambda_N(V_{GS2} - V_{SG4}) \\ &\cong 1 + \lambda_N(V_{DD} - V_{\text{REF}}) \quad \text{(A11a)} \\ b &= 1 + \lambda_P V_{SD3} = 1 + \lambda_P(V_{DD} - V_{\text{REF}}) \quad \text{(A11b)} \end{aligned}$$

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