Basic Circuitry of the MIDAC and MIDSAC

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FOREWORD

During the years 1951 to 1953, several digital computing equipments were developed at the University of Michigan, Willow Run Research Center (WRRC), under sponsorship of the United States Air Force. These included the Michigan Digital Automatic Computer, MIDAC, which is a general purpose electronic calculator (Ref. 1, 2, and 3), and the Michigan Digital Special Automatic Computer, MIDSAC, designed for real-time operation as an element of an automatic control system (Ref. 4). One aspect of the computer program concerned the development of a flexible and highly standardized set of electronic computing circuits which served as the principal building blocks for both computer designs. This report describes the results of that work.

The computing circuits consist of a group of pulse circuits which operate at a 1-Mc pulse repetition rate. The circuits provide, in conveniently packaged form, the functions of logical switching, pulse amplification, and delay storage. Each of the computers mentioned above uses more than one thousand of these packages to implement all computer functions with the exception of the memory and the input-output functions.

At the outset of the development program, it was apparent that several research laboratories had independently developed computing circuits which were potentially capable of meeting the requirements of the projected Michigan computers. Rather than repeat the initial work of these laboratories, it was decided that the University of Michigan group should select the existing circuit techniques which showed the most promise of quick and reliable operation, and devote its energies to the engineering improvement of these techniques.

After preliminary studies, the computing circuits developed by the National Bureau of Standards for use in the SEAC computer were selected as most appropriate to the present needs (Ref. 5). A cooperative development program was initiated involving WRRC and the National Bureau of Standards Electronic Computers Laboratory. A research and development group at the Air Force Missile Test Center at Cocoa Beach, Florida,

was also interested in furthering the NBS techniques, and constituted a third party in the cooperative effort.

This report describes the final packaged circuitry as used by WRRC in the MIDAC and MIDSAC computers. The report is in four parts. Part I describes the function, operation, and design of the packages, and includes a set of rules governing permissible interconnections between packages. Part II contains several examples of functional units within a computer which may be implemented by using the packaged circuits. Part III describes a simplified serial-binary arithmetic unit which can be assembled using the basic functional building blocks described in Part II. Part IV describes the constructional features of the packages and of the chassis and racks in which the packages are mounted.

In addition to the listed authors of this report, many other persons contributed to the circuit development at WRRC. Circuit design work was primarily carried out by J. Kaufman with assistance from R. Hock and B. Smith. Mechanical design was done by H. Bethel with assistance from W. Sutton. H. L. Garner was primarily responsible for the preparation of this report. The development program was under the technical supervision of J. E. DeTurk.

I

DESCRIPTION OF COMPUTER PLUG-IN CIRCUITS

1.1 FUNCTIONAL ORGANIZATION OF CIRCUITS

Three functional types of equipment are generally required in the design of an electronic digital computer. These are the memory equipment, which is employed to store large quantities of numerical or instructional information for indefinite periods; the input-output portions, which provide a means for communication between the computer and the persons who operate it; and, finally, the pulse switching circuits, which govern the flow and manipulation of information within the machine. The packaged electronic circuits described in this report are of the third category; i.e., they perform elementary switching functions which can be compounded to yield the arithmetic, control, and timing operations which are essential to a digital computer.

Two theoretical requirements apply to circuitry for this purpose. The first is a requirement for logical completeness; i.e., enough different types of switches should be employed so that any conceivable logical structure can be implemented. The second theoretical requirement makes it necessary to store, or remember, an event (pulse) over some part of the computation time. In the circuits to be described, the logical operations "and", "or", and "not" are used to provide completeness. The physical circuits which implement these functions are called gates; the three types of gates employed are shown symbolically in Figure 1-1. The second essential property, that of memory, is obtained by means of electrical delay line.

In addition to the theoretical requirements, several practical considerations affect the design of computer circuitry. Imperfections in the physical structures which implement the logic cause pulse deterioration in the form of amplitude attenuation, pulse shape distortion, and variations in pulse timing. Thus there is a need for complete re-standardization of the power level, shape, and timing of every pulse after the pulse has passed through a few logical structures. In the MIDAC circuits, a maximum of three cascaded levels of logical switching operation and one level of logical

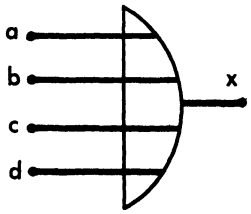
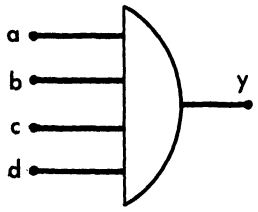
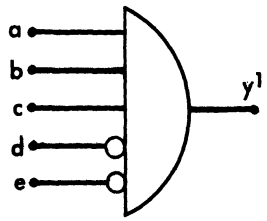
Symbol	Boolean Identity	Meaning
	$a+b+c+d=x$	Signal x occurs when a or b or c or d is present.
Or - Gate		
	$a \cdot b \cdot c \cdot d = y$	Signal y occurs when a and b and c and d are present.
And - Gate (with only positive inputs)		
	$a \cdot b \cdot c \cdot \bar{d} \cdot \bar{e} = y^1$	Signal y^1 occurs when a and b and c and not $-d$ and not $-e$ are present
And - Gate (with three positive and two negative inputs)		

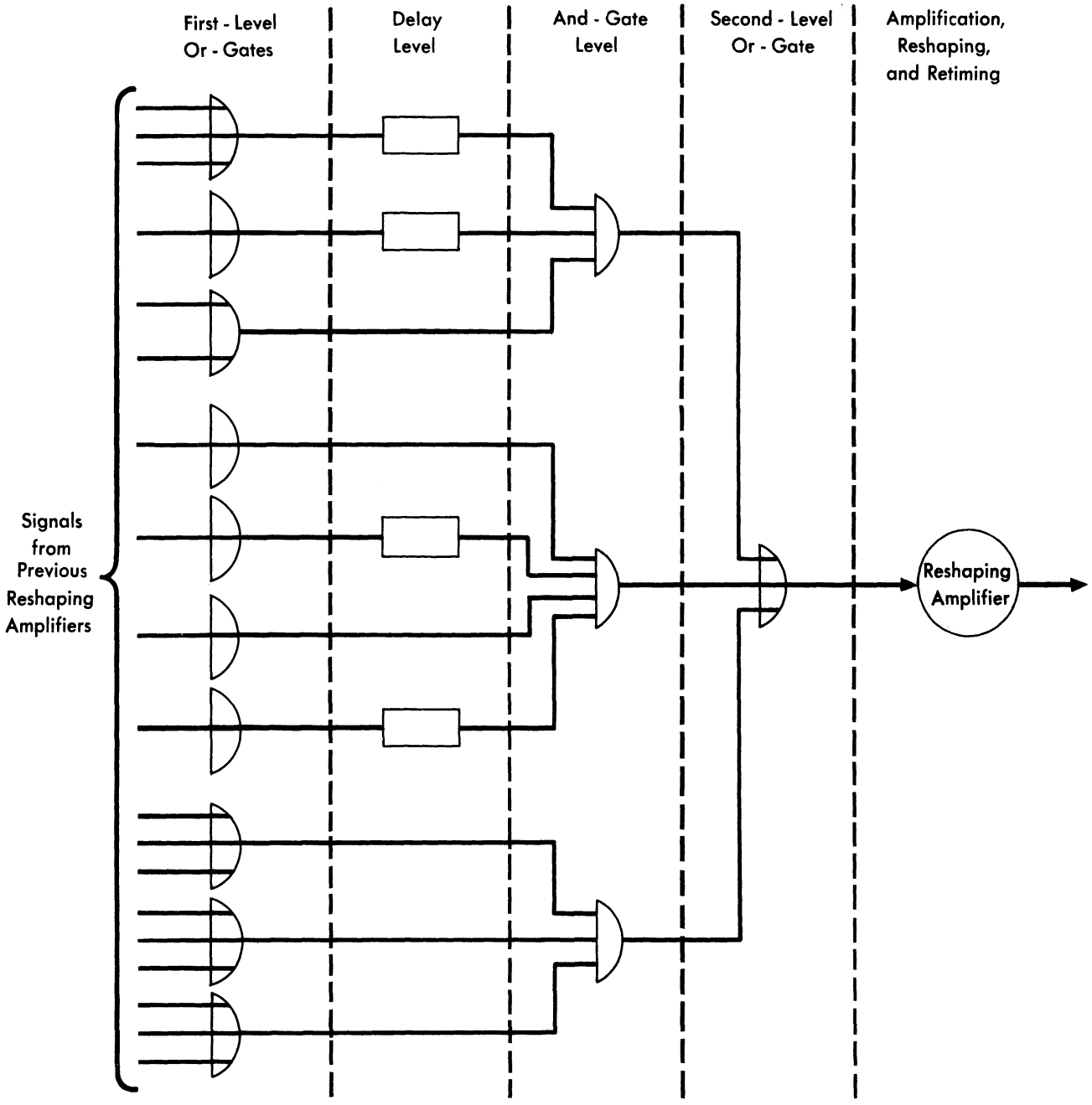
FIG. 1-1 SYMBOLIC REPRESENTATIONS OF GATES

delay are permitted before pulse amplification, retiming, and reshaping occur. Figure 1-2 (a) suggests the type of configuration in which these levels are assembled. (In a given configuration, the delay level may sometimes be omitted.) Circuit design factors require that the and-gate level and the two levels of or-gates occur in all but a few situations. Figure 1-2 (b) illustrates a situation where each gate associated with an amplifier is degenerate (has only one input).

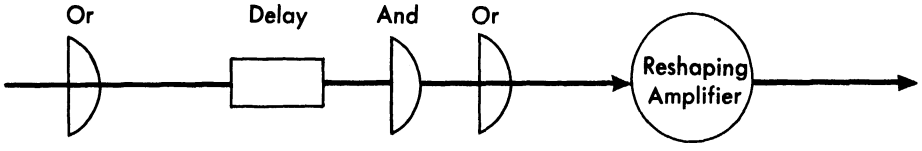
Some unavoidable delay occurs as a pulse is propagated through switching and amplification circuits. To avoid an uncontrolled accumulation of delay in a large ensemble of circuits, each configuration is operated so as to have a standardized delay of 1/4 microsecond, exclusive of the delay due to the logical delay elements. This delay is controlled by synchronizing each circuit with a master clock which operates continuously at 1 Mc. The master clock provides separate outputs at four equally spaced phases (i.e., at one-quarter-microsecond intervals), and successive circuits are synchronized with progressively advanced clock phases.

Five basic types of plug-in units are designed to implement configurations of the type shown in Figure 1-2. An amplifier package (Fig. 1-3) contains a second-level or-gate, an amplifier, and a degenerate, first-level or-gate (the latter gate is not always used). An and-gate package (Fig. 1-3) contains all functional and-gates which may be associated with a given amplifier. The and-gate package design has several variants, differing in the number of gates included (from one to four) and in the number of signal inputs to each gate (from one to seven). One amplifier package and one and-gate package plug together to form an integral plug-in unit, and are always used in this combination. Such a combined unit is called a gate-amplifier package. Smaller packages, called "penthouses" (Fig. 1-3), are sometimes plugged into the amplifier package to augment the current capability of the degenerate or-gate at the amplifier output.

A delay package (Fig. 1-4) contains several pieces of electrical delay line which are used to delay pulses by discrete time intervals. A delay termination package (Fig. 1-4) consists of several terminating networks used to provide proper terminating impedances for the delay lines in delay



(a) General Case



(b) Degenerate Case

FIG. 1 - 2 THE LEVELS OF LOGICAL FUNCTION ASSOCIATED WITH ONE PULSE AMPLIFIER

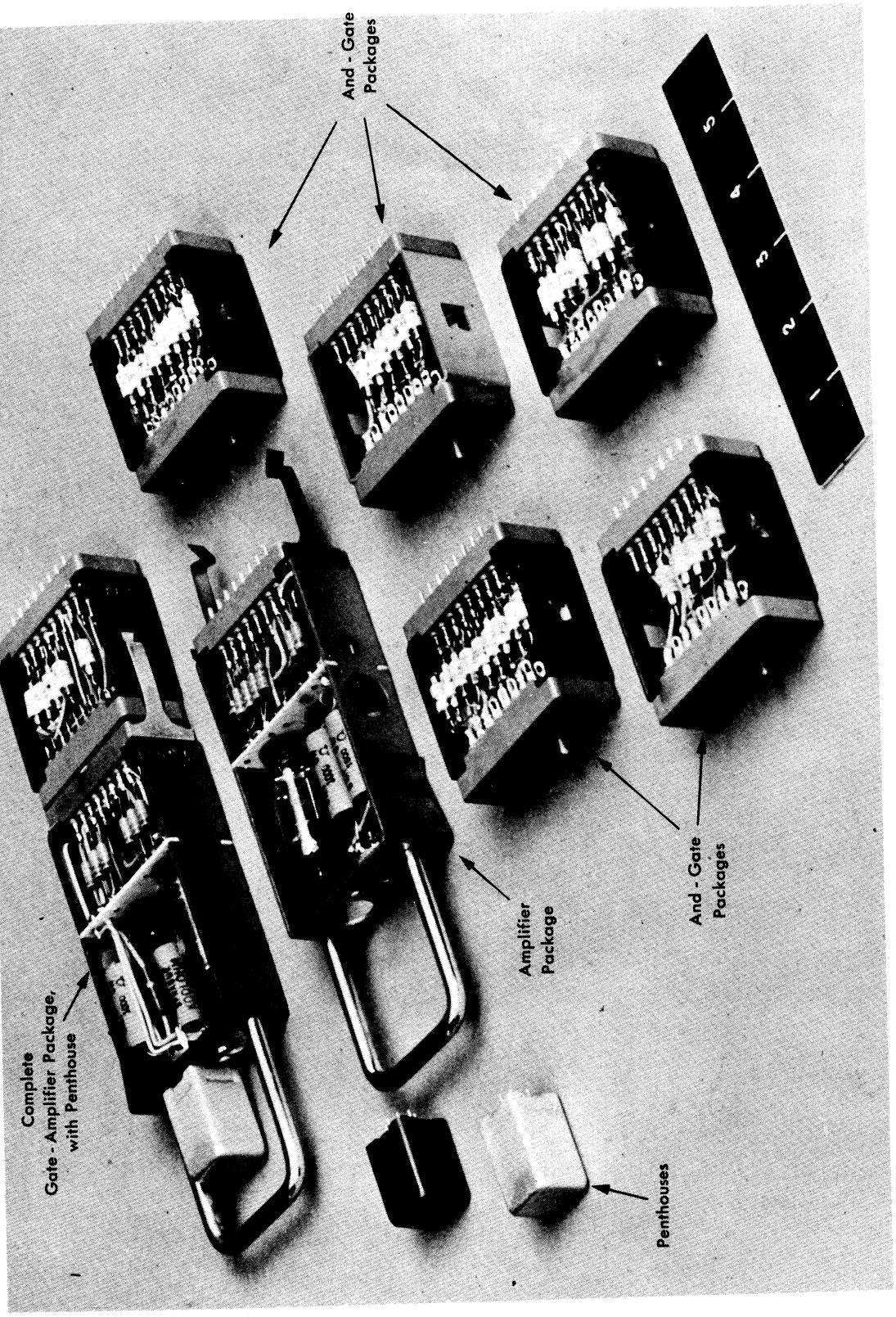


FIG. 1-3 GATE-AMPLIFIER PACKAGE

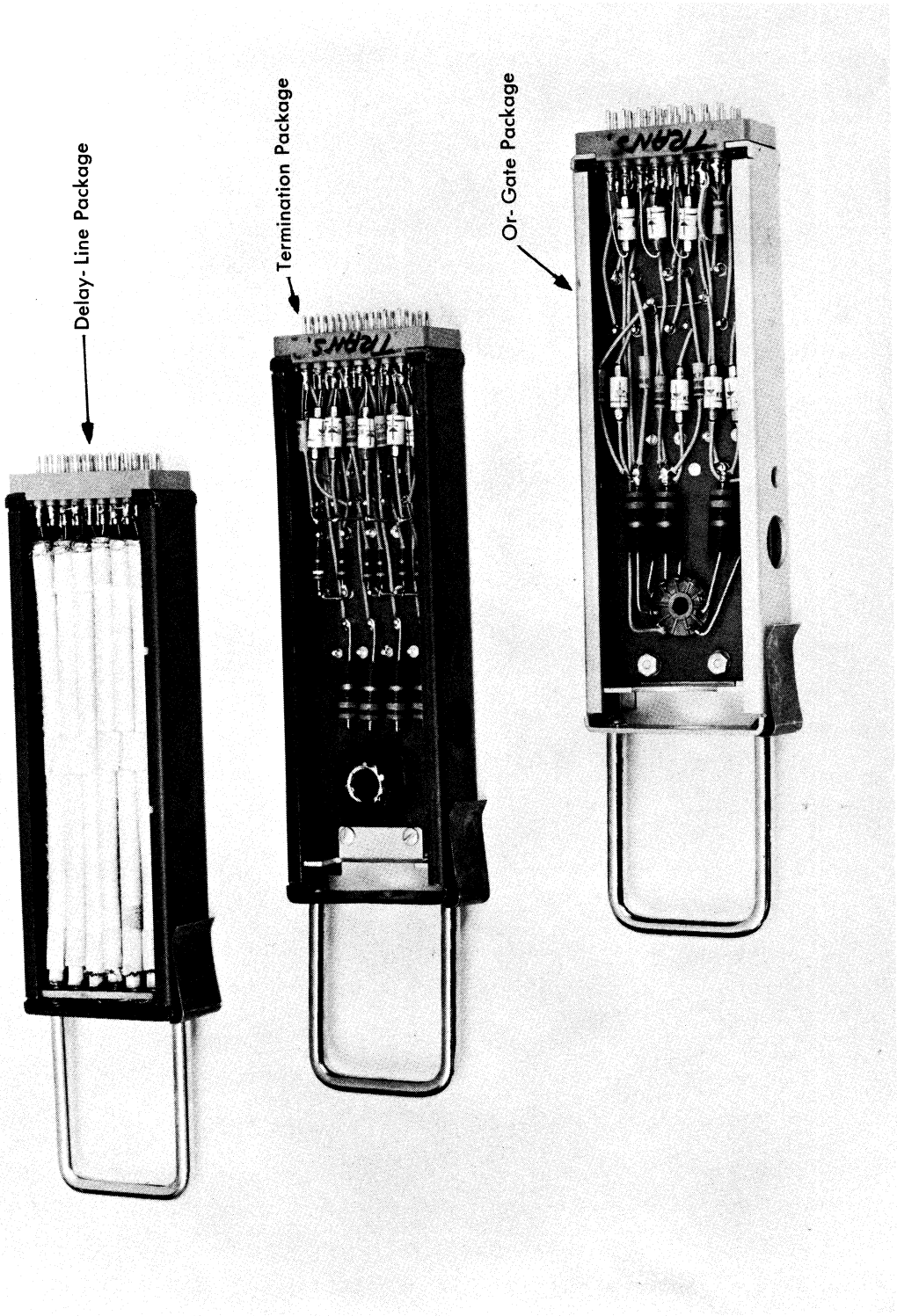


FIG. 1-4 DELAY-LINE, TERMINATION, AND OR-GATE PACKAGES

packages. An or-gate package (Fig. 1-4) consists of several or-gates which may be used as needed to provide first-level or-gates.

1.2 DESCRIPTIONS OF PACKAGE TYPES

1.2.1 Gate-Amplifier Package

Figure 1-5 shows a symbolic representation of the gate-amplifier unit. The gates are implemented by passive networks consisting of germanium diodes and resistors. The amplifier is a single-tube pentode pulse amplifier with transformer-coupled output. Both positive and negative outputs are provided, and the positive output may be obtained either directly or through the degenerate or-gate.

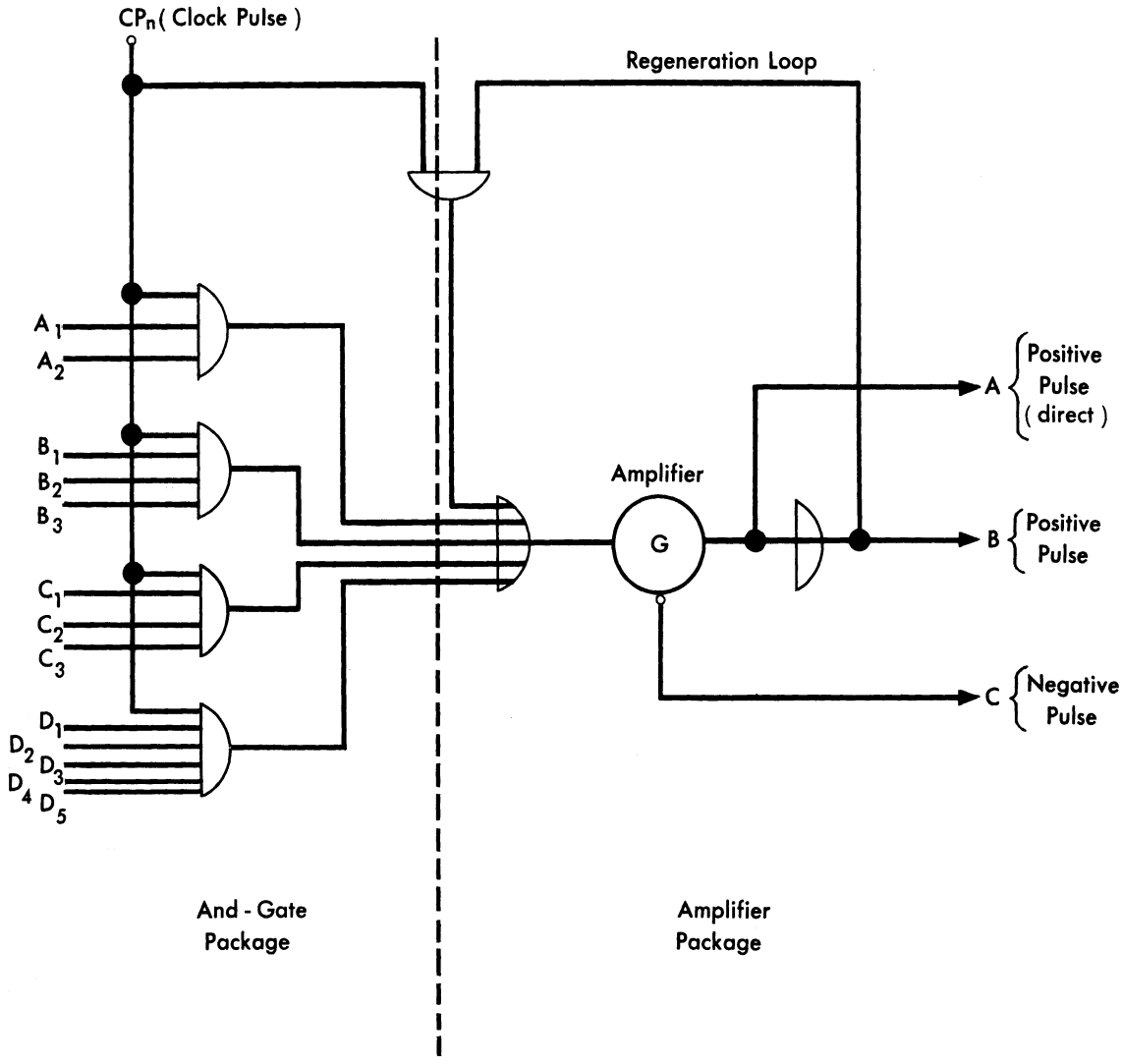
Two features of this circuit provide for the standardization of the output pulse shape and the amplifier time delay. First, the clock signal is applied to one input of each and-gate; this procedure ensures that the leading edge of the amplifier excitation pulse cannot occur before the leading edge of the clock pulse. Second, the output of the amplifier is coupled to its own input through an and-gate which is clocked with the same clock phase. The resulting regeneration loop ensures that the excitation pulse, if once initiated, will continue for the entire duration of the clock pulse.

The clocking and regeneration action allows the package to produce a standardized output signal even though the signal inputs to the package are distorted in shape and are not precisely timed. Figure 1-6 illustrates the time relationships between two cascaded gate-amplifier circuits.

1.2.1.1 Package Variations

There are no variations of the amplifier package. There are five variations of the and-gate package, as indicated in Table 1-1.

The letters in the first column of the table identify each and-gate package type. The second column describes the package types in terms of the number of and-gates and the number of permanent inputs on each gate; for example, "5, 3" in the second line means that the Type C package contains two and-gates with five and three inputs respectively. As indicated in the third column, each package contains some "free diodes" which



$$(A_1 \cdot A_2) + (B_1 \cdot B_2 \cdot B_3) + (C_1 \cdot C_2 \cdot C_3) + (D_1 \cdot D_2 \cdot D_3 \cdot D_4 \cdot D_5) = A$$

FIG. 1-5 GATE - AMPLIFIER PACKAGE

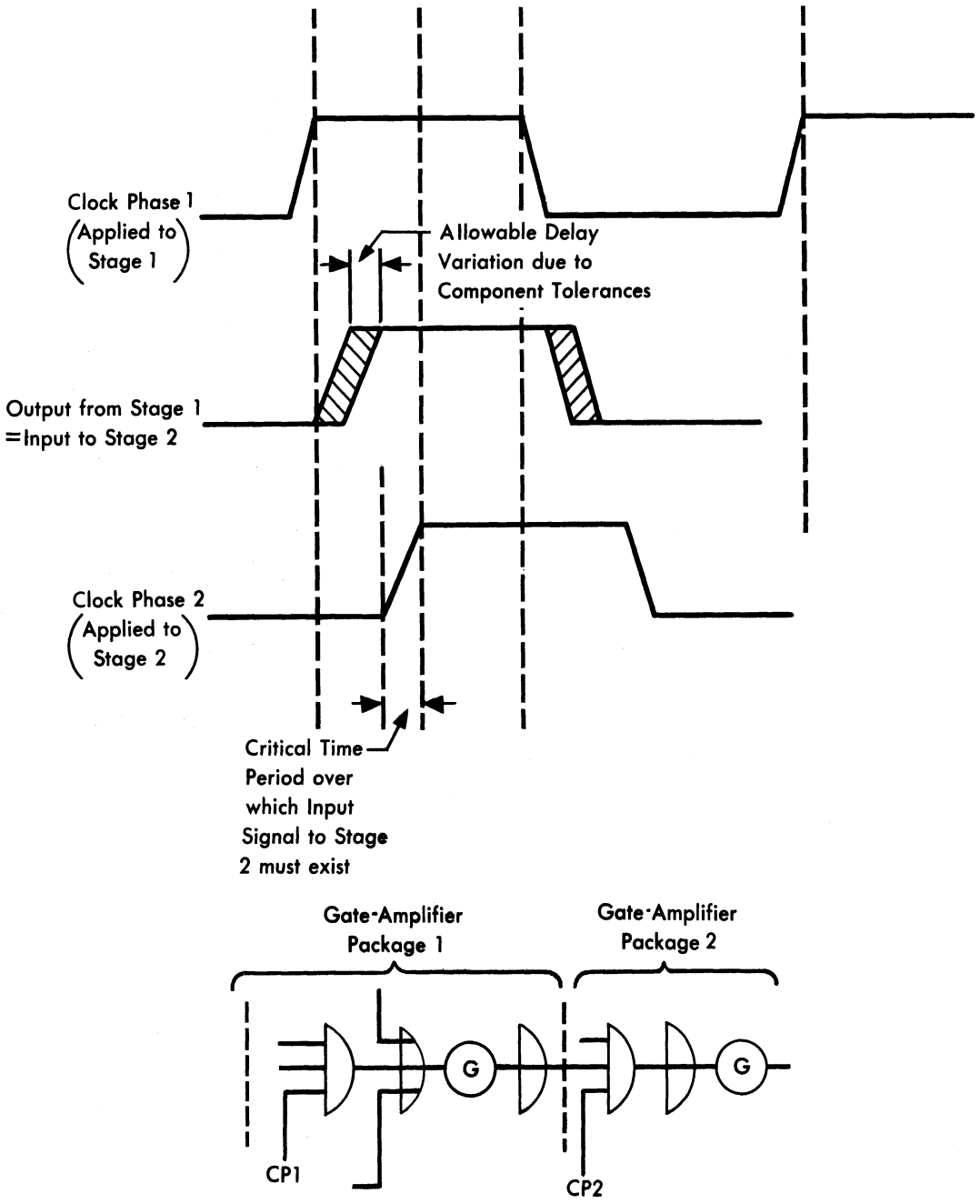


FIG. 1-6 USE OF MULTI-PHASE CLOCK TO STANDARDIZE DELAY IN CASCADED CIRCUITS

TABLE 1-1

TYPES OF AND-GATE PACKAGES

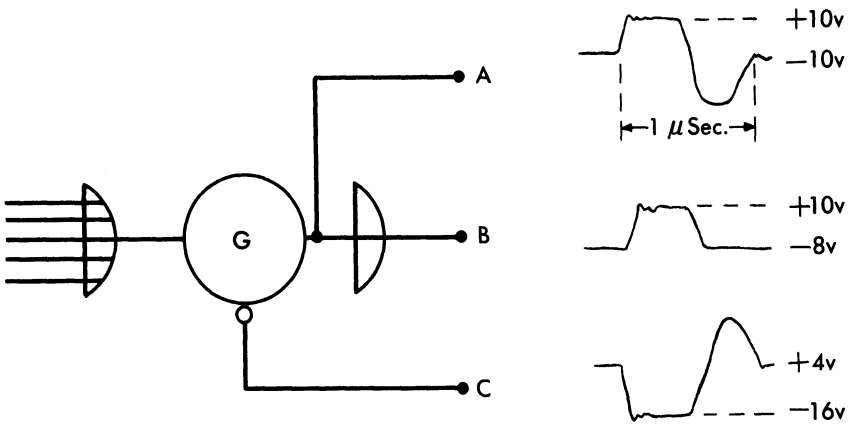
Package Type	Permanently Connected Gate inputs	Free Diodes	Maximum Number of Gate inputs
A	3	3	6
C	5, 3	3	7, 6
D	2, 2, 2	3	6, 6, 6
E	5, 4, 3	2	7, 7, 6
F	5, 3, 3, 2	1	7, 6, 6, 6

are not connected directly to the gate circuits, but are, instead, independently connected to the package base pins. By means of jumper wires on the package receptacles, these diodes may be used to augment the number of signal inputs to the and-gates, at the rate of one diode for each added input. Column four indicates the maximum number of inputs which can be tolerated on each and-gate. When free diodes are used to augment gate inputs, they should be located in the same package as the gate (or in adjacent packages); otherwise excessive wiring capacitance will prohibit using the maximum number of inputs listed.

In addition to the listed components, the Type A package contains a positive delay-line termination network.

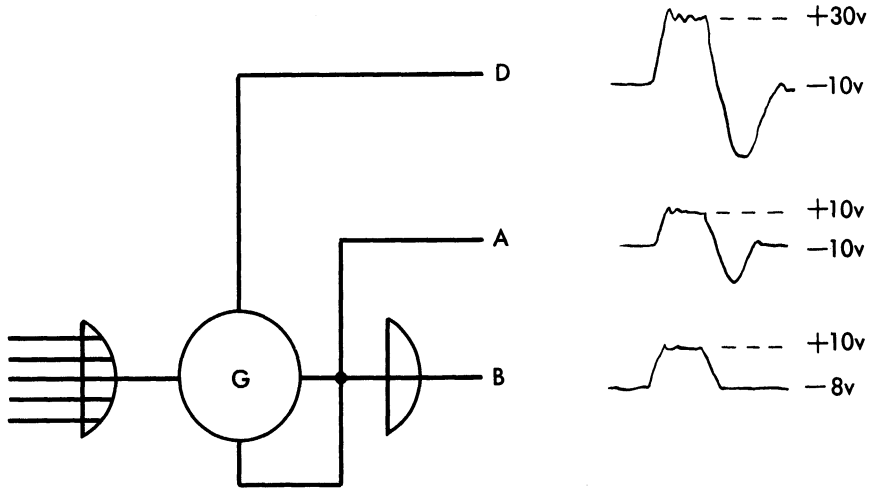
1.2.1.2 Amplifier Package Outputs

The output terminals of the amplifier package may be connected in either of two ways. The usual manner of connection provides three types of output signals, as illustrated in Figure 1-7 (a). The second type of connection, shown symbolically in Figure 1-7 (b), causes the two transformer output windings to be connected in series aiding. This connection makes available a positive pulse output, D (which has twice the amplitude of the normal positive output) in addition to the two positive outputs of normal amplitude. Note that with this connection the negative pulse output is not available.



A. Positive Pulse (Direct)
B. Positive Pulse Through Degenerate Or-Gate
C. Negative Pulse

a. NORMAL OUTPUT LINES AVAILABLE FROM AMPLIFIER PACKAGE



D. Double Amplitude Positive Pulse
A. Positive Pulse (Direct)
B. Positive Pulse Through Degenerate Or-Gate

b. OUTPUT OF AMPLIFIER PACKAGE USING SERIES CONNECTION OF SECONDARIES

FIG. 1-7 OUTPUTS OF AMPLIFIER PACKAGE

Each of these outputs is used to drive a particular type of load. Output A is used to drive positive short-delay lines[1] and first-level or-gates. Output B is used to drive and-gates directly. Output C is used to drive negative short-delay lines and inhibit inputs to and-gates. Output D is used exclusively for driving positive long-delay lines.

For convenience, the amplifier power output requirements for all types of loads are expressed as integral multiples of a unit called an equivalent gate load. One equivalent gate load is a load which requires the same current as a single and-gate input. Table 1-2 shows the equivalent gate load ratings of the inputs to various circuits.

TABLE 1-2

EQUIVALENT GATE LOAD RATINGS

Type of Load	Number of equivalent gate loads
Single and-gate input	1
Positive (or negative) short-delay line	2
Long-delay line	8
Positive (or negative) or-gate driving a single and-gate input	1
Positive (or negative) or-gate driving a short-delay line	2

The amplifier package is capable of driving a maximum of sixteen equivalent gate loads from the combination of all output terminals. The degenerate or-gate output, B, is normally capable of driving only four and-gate inputs, leaving twelve equivalent gate drives for outputs A and C or A and D. The addition of one of two types of "penthouse" units (described in the following paragraph) increases the drive capability of terminal B to either ten or sixteen drives, leaving either six drives or no drives available at A or C.

[1]Short-delay lines provide from 0.25 microseconds to 2.00 microseconds delay, and long-delay lines provide from 2.25 microseconds to 4.00 microseconds delay.

1.2.1.3 Penthouse Units

Penthouses (Fig. 1-3) are external plug-in units which are added to the amplifier package when more than four equivalent gates are to be driven from output B. A penthouse contains additional diodes which augment the current-carrying capacity of the degenerate or-gate output. A type P_1 penthouse is used when five to ten equivalent gate drives are required, and a type P_2 penthouse is used when eleven to sixteen equivalent gate drives are required.

1.2.2 Delay Package

The delay package (Fig. 1-4) contains sixteen "sticks" of distributed-parameter delay line. Each delay line stick provides a pulse delay of 0.25 microseconds. There are four variations of this package, differing only in the way the delay line sticks are pre-connected. Table 1-3 lists the delay combinations in the four types of delay packages.

TABLE 1-3

TYPES OF DELAY PACKAGES

Package Type	Number of 1/4-microsecond delays	Number of 3/4-microsecond delays	Number of 4-microsecond delays
L_1	7	3	0
L_2	1	5	0
L_3	4	4	0
L_4	0	0	1

1.2.3 Termination Package

Each termination package (Fig. 1-4) consists of ten sets of diode-resistor networks. Each set provides the proper electrical terminations for both the input and output of one delay line. The termination networks contained in any package are of two types, one for positive pulses and the

other for negative pulses. There are two variations of the termination package. The T_1 package contains eight sets of termination networks for positive pulses and two sets for negative pulses. The T_2 package contains five sets of termination networks for positive pulses and five sets for negative pulses.

A portion of the termination network consists of a degenerate or-gate which drives the delay line input. The number of signal inputs to this or-gate can be augmented by free diodes, thus providing the ability to drive a single delay line from several independent packages. This augmentation applies to both positive and negative termination networks. Positive termination networks can also be converted to multiple-input, first-level or-gates suitable for driving and-gates.

1.2.4 Or-Gate Package

The or-gate (Type R) package is employed when termination networks or free diodes are not available for constructing first-level or-gates. An or-gate package contains six two-input or-gates for positive pulses, and six free diodes; the free diodes may be used to augment the number of gate inputs.

1.3 INTERCONNECTION OF PACKAGES

The permissible ways in which packages may be interconnected are illustrated in Figures 1-8, 1-9, 1-10, and 1-11.

Figure 1-8 illustrates important rules concerning the application of negative pulses to and-gates in order to realize the "not" function. Figure 1-8(a) shows a desired logical function involving inhibition of two and-gates of different clock phases. Parts (b) and (c) of Figure 1-8 show two different methods for using the packaged circuits to realize this function. In Figure 1-8(b), each and-gate to be inhibited requires two separate paths from the driving package to two separate inputs of the gate. One of these paths is the functional path shown in part (a) of the figure. The other path contains an additional delay of 1/4 microsecond. The effect of the delay path is to increase the duration of the negative signal at the driven gate, thus ensuring that reliable inhibition occurs.

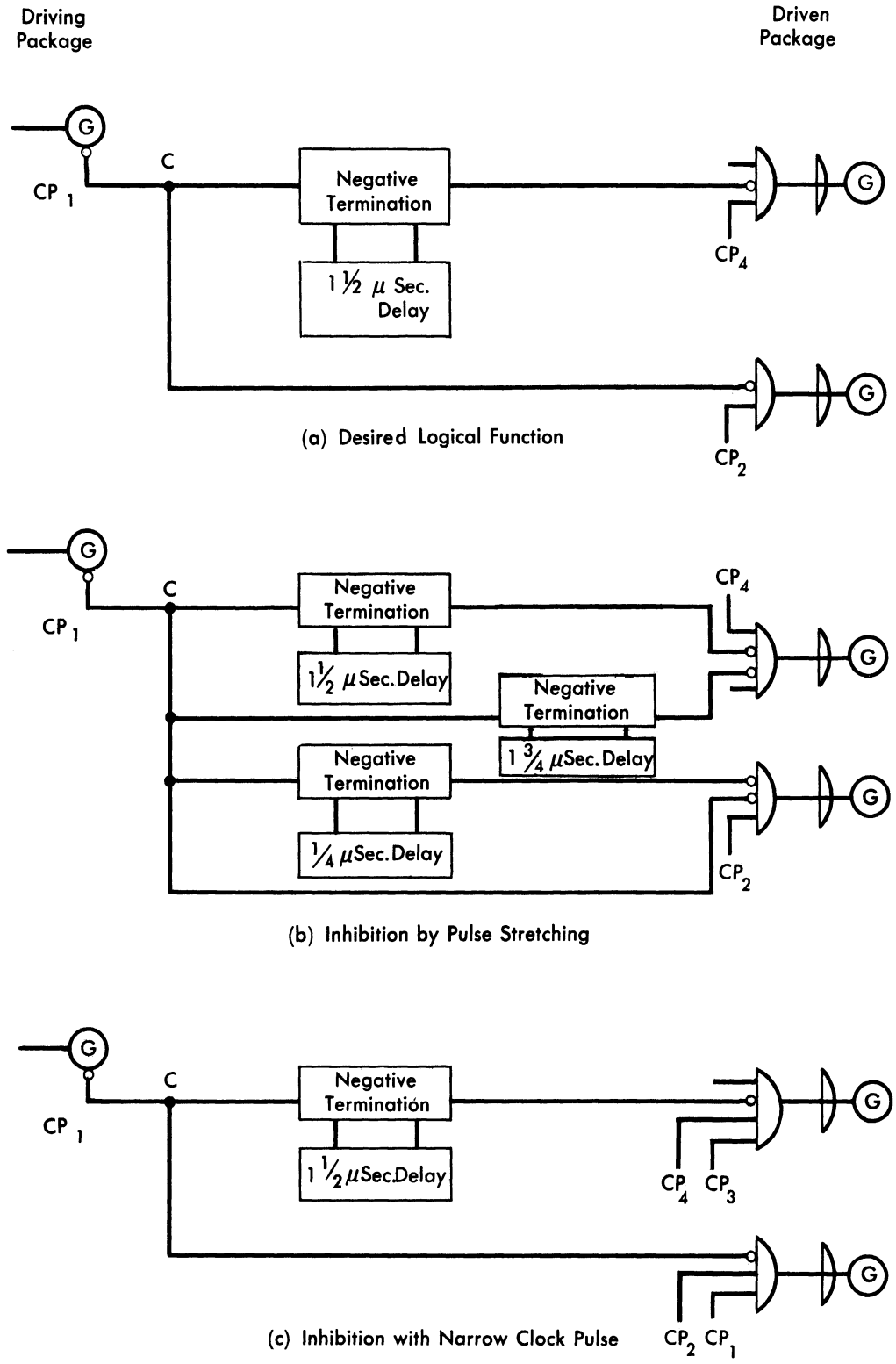


FIG. 1-8 EXAMPLES OF AND-GATE INHIBITION

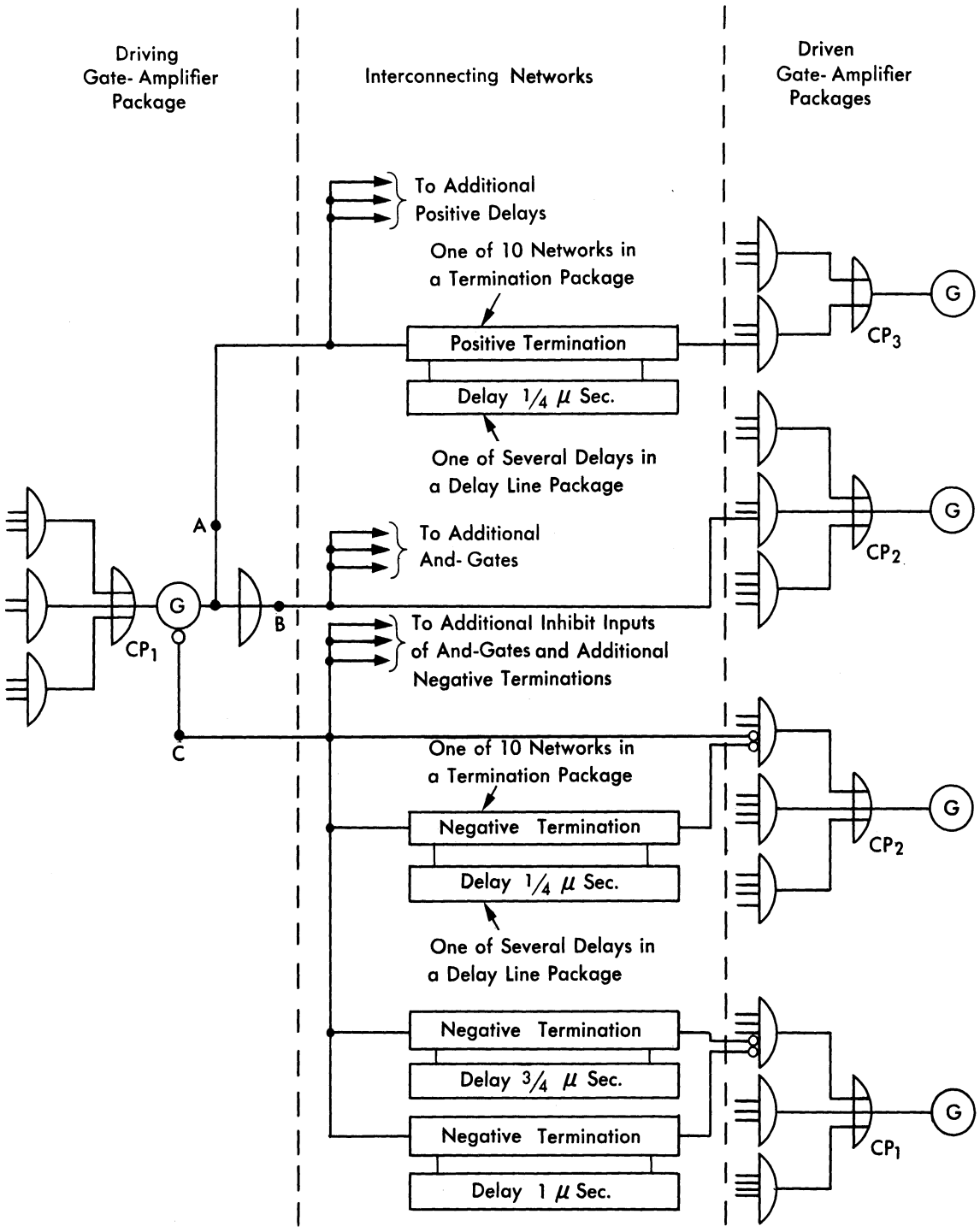


FIG. 1-9 INTERCONNECTING NETWORKS WITH DEGENERATE FIRST-LEVEL OR-GATES

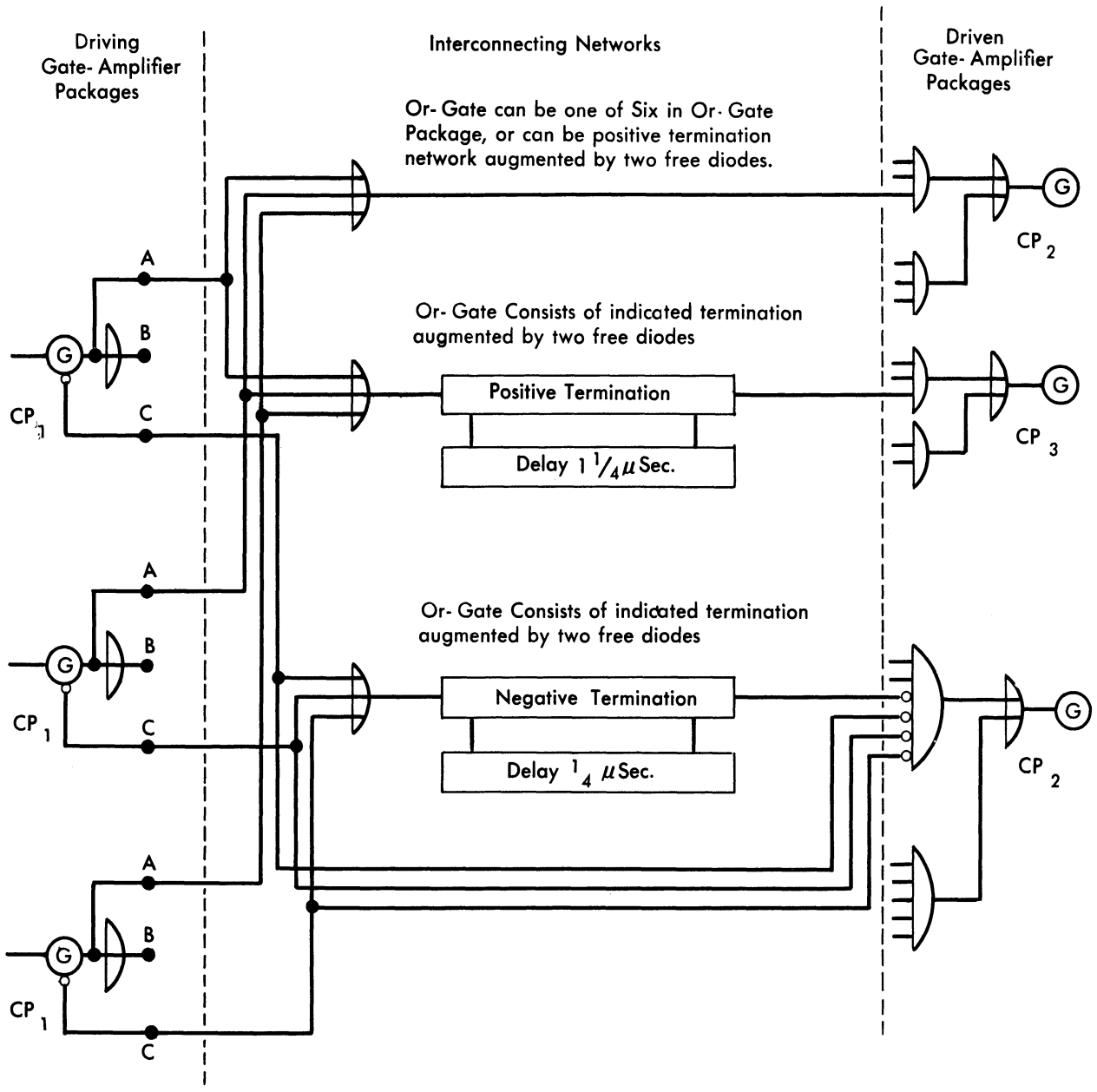


FIG. 1-10 INTERCONNECTING NETWORKS WITH NON-DEGENERATE FIRST-LEVEL OR-GATES.

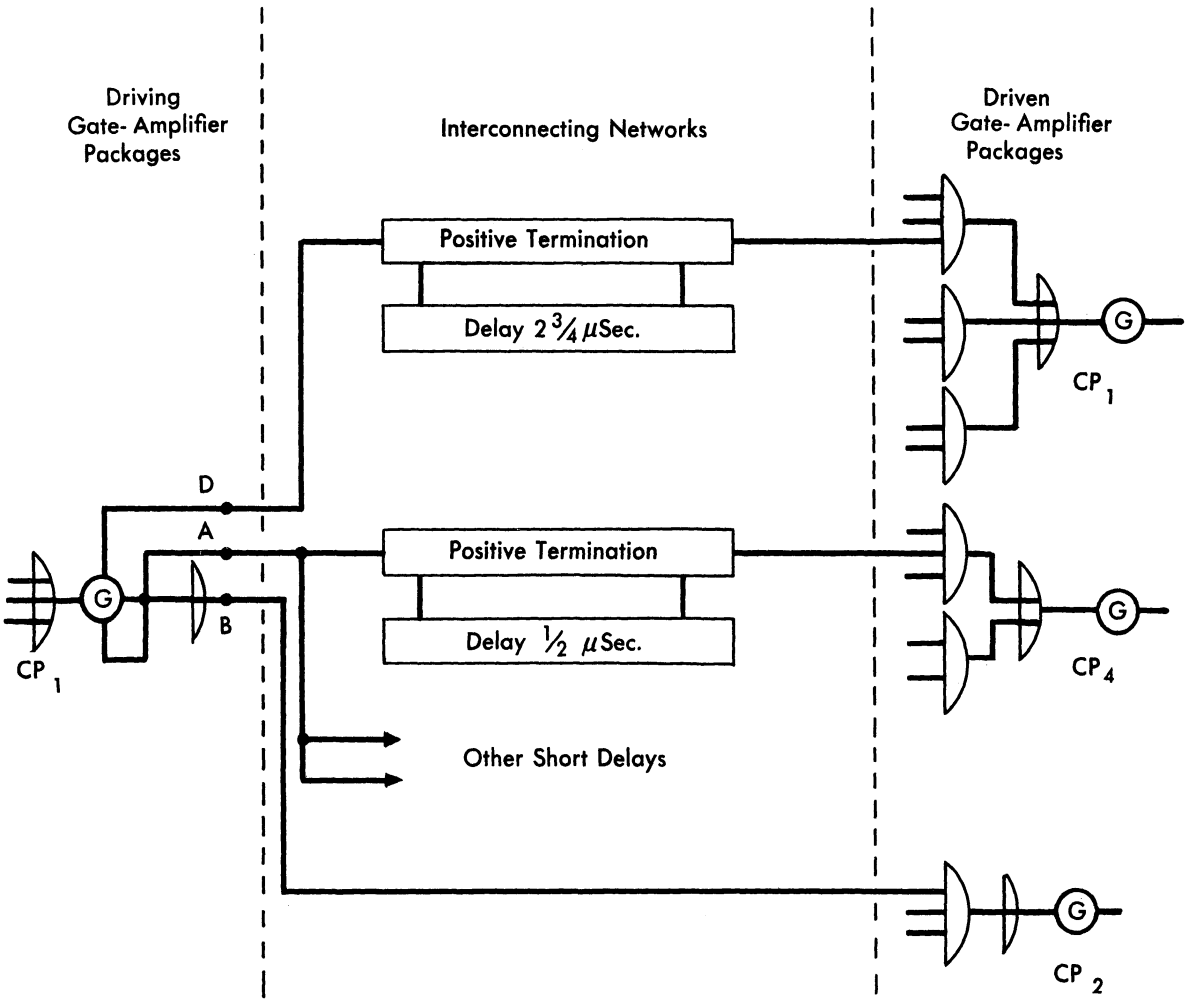


FIG. 1-11 INTERCONNECTING NETWORKS USING LONG DELAY LINES

Figure 1-8(c) shows an alternative method for achieving the functions shown in part (a). Here, each gate to be inhibited is clocked with two adjacent clock phases. One clock input is the normal clock input to all gates of the package. The second clock input is to the particular gate being inhibited. The effect is to decrease the period during which the gate is sensitive, thereby ensuring that reliable inhibition occurs.

Figure 1-9 shows examples of interconnections in which first-level or-gates are degenerate and delays are two microseconds or less. Figure 1-10 shows examples of interconnections in which non-degenerate, first-level or-gates occur and delays are, again, two microseconds or less. Figure 1-11 shows examples of interconnections in which long-delay lines occur. These figures illustrate most of the rules for interconnecting packages. They also illustrate correct usage of the clock pulses, and indicate the methods for obtaining first-level or-gates.

There are restrictions on the length of signal wires which can be used to interconnect packages. Consequently the computer designer must exercise skill and judgment in planning the location and utilization of packages. Important factors influencing package groupings are:

1. Signal wires should not be shielded,
2. The wires connected to the output terminals of an amplifier package can be up to fifty feet in length,
3. All other signal wires should be short,
4. Free diodes should be located in the same package as the gate which they are used to augment, or in an adjacent package,
5. A delay line package should be adjacent to the package containing its terminations,
6. The signal wire from a delay line output to the and-gate which it drives should be not more than one or two "inter-package" distances in length.

1.4 CIRCUIT OPERATION

Figure 1-12 shows schematically the circuit of the gate-amplifier package which was symbolically represented in Figure 1-5. Elements to the left of the dashed line are located in the and-gate package and those to the right are in the amplifier package.

1.4.1 The Diode Gates

An and-gate is shown in Figure 1-13. If the diodes are assumed to be ideal and the circuit is assumed to have no external load or shunt capacitance, then the output voltage e_a is equal to the most negative of the several input voltages. An output pulse will occur only when all inputs are simultaneously pulsed positive. The waveforms on the figure illustrate the operation of the gate under actual conditions. With the gate closed, the output follows the clock voltage during negative half-cycles of the sinusoidal clock signal. During positive half-cycles of the clock, the output is prevented from rising above -8v in the absence of positive pulses at other signal inputs. When positive signals are present at all signal inputs, the gate output tends to follow the positive half-cycle of the clock voltage. It is prevented from rising above +2v by a bumper diode not shown in Figure 1-13.

Under ideal conditions, the output signal of the or-gate of Figure 1-14 is always equal to the voltage of the most positive input. A positive pulse on any input will appear as a pulse at the output. The or-gate output is clamped at -5v, which is three volts positive with respect to the most positive input expected under no-signal conditions with ideal components. Thus 3v of spurious signals or noise, due to imperfections in the and-gate or stray couplings between signal wires, can be tolerated. A bumper diode at the or-gate output limits the signal to a peak value of +2v.

1.4.2 Amplifier

The amplifier uses a type 6AN5 high-transconductance pentode in the circuit shown in Figure 1-15. The two piece core of the pulse transformer is a miniature pot type made from a manganese-zinc ferrite material, and is designated as Part No. 7F160 by its manufacturer, Ferroxcube Corporation of America. The windings are on a ring-shaped nylon

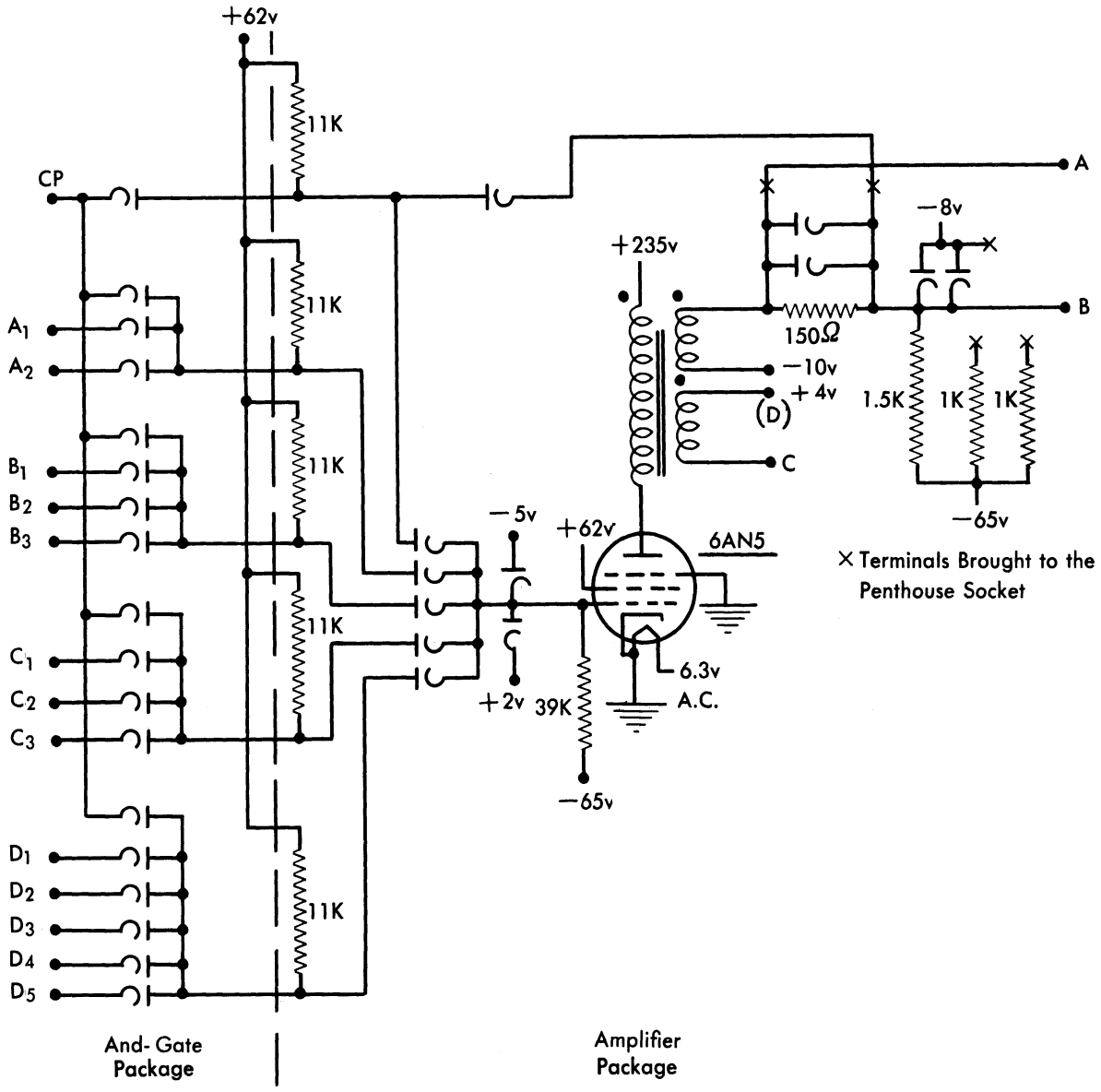
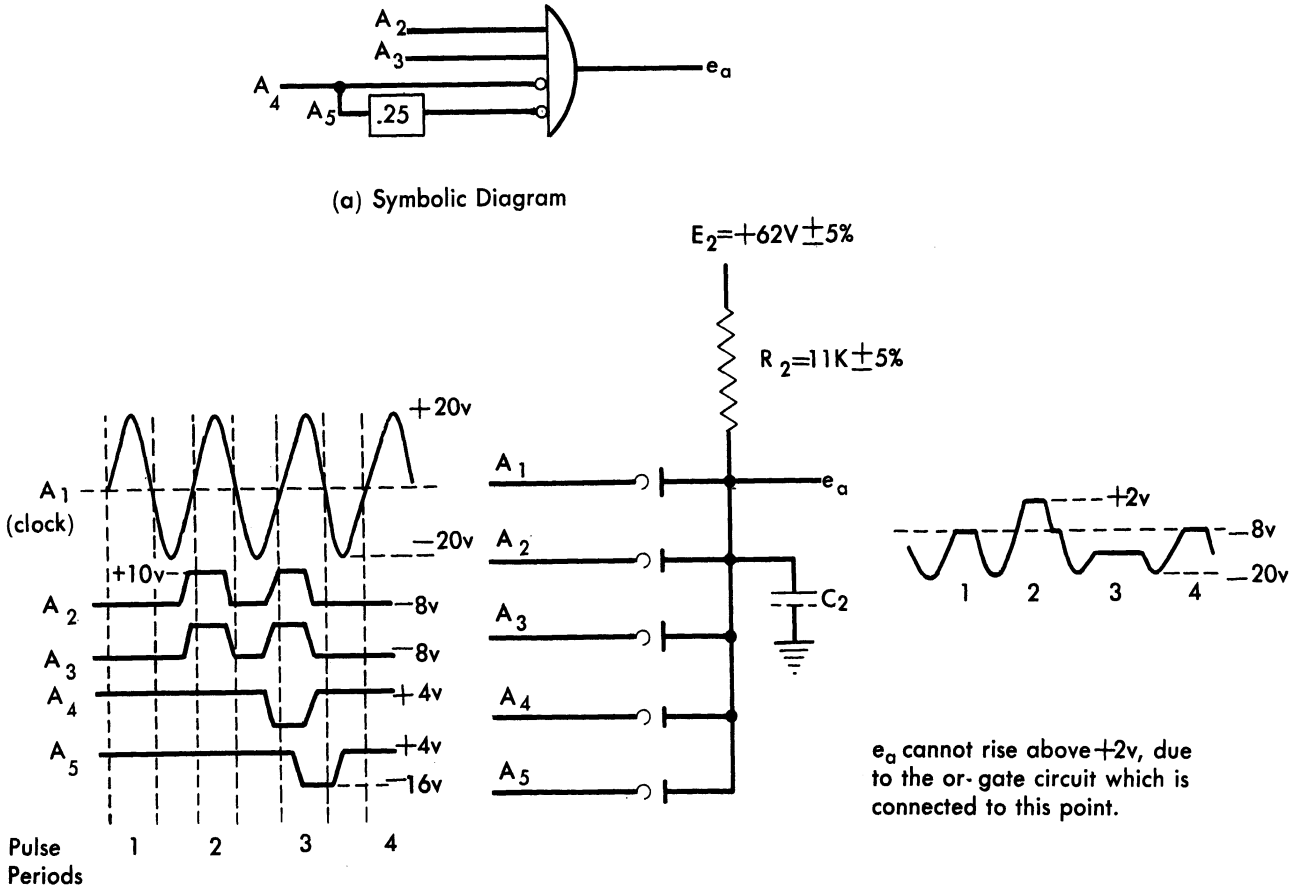
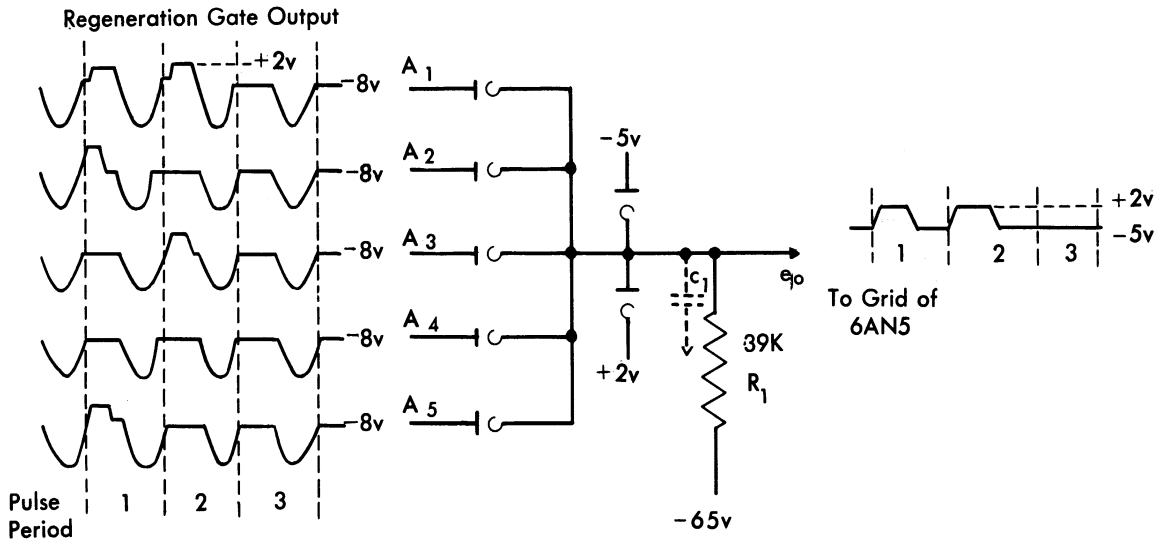


FIG. 1-12 CIRCUITS OF GATE-AMPLIFIER PACKAGES



Gate is activated during pulse period 2 when A_2 and A_3 have coincident pulses. Gate is inhibited during pulse period 3 when A_4 and A_5 are pulsed.

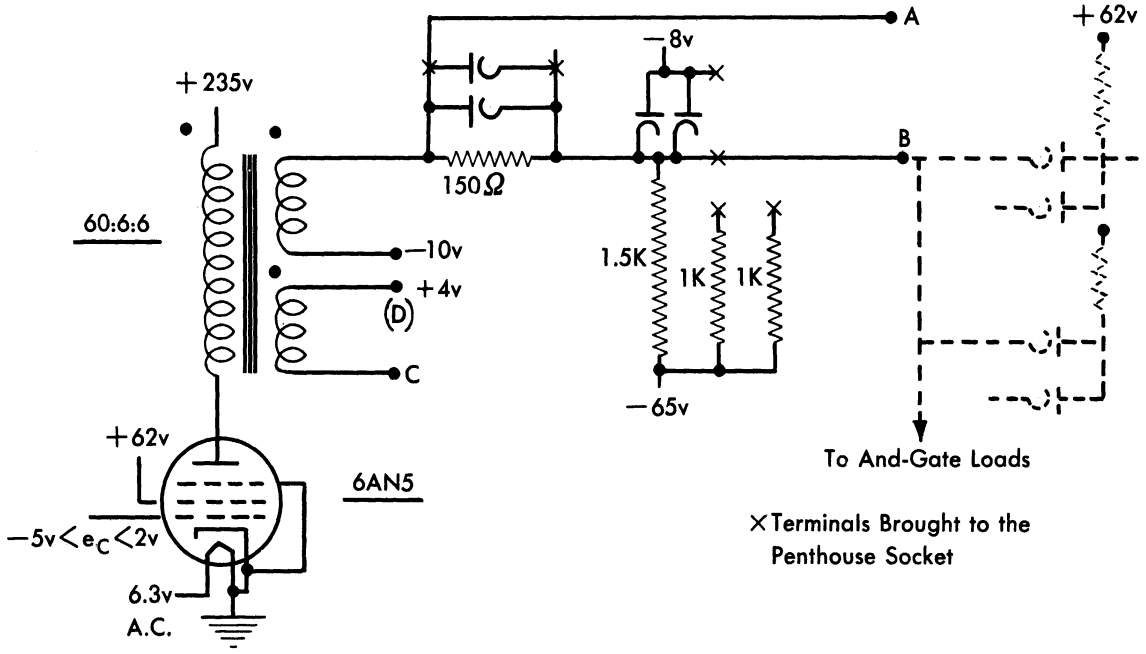
FIG. 1-13 OPERATION OF AND-GATE



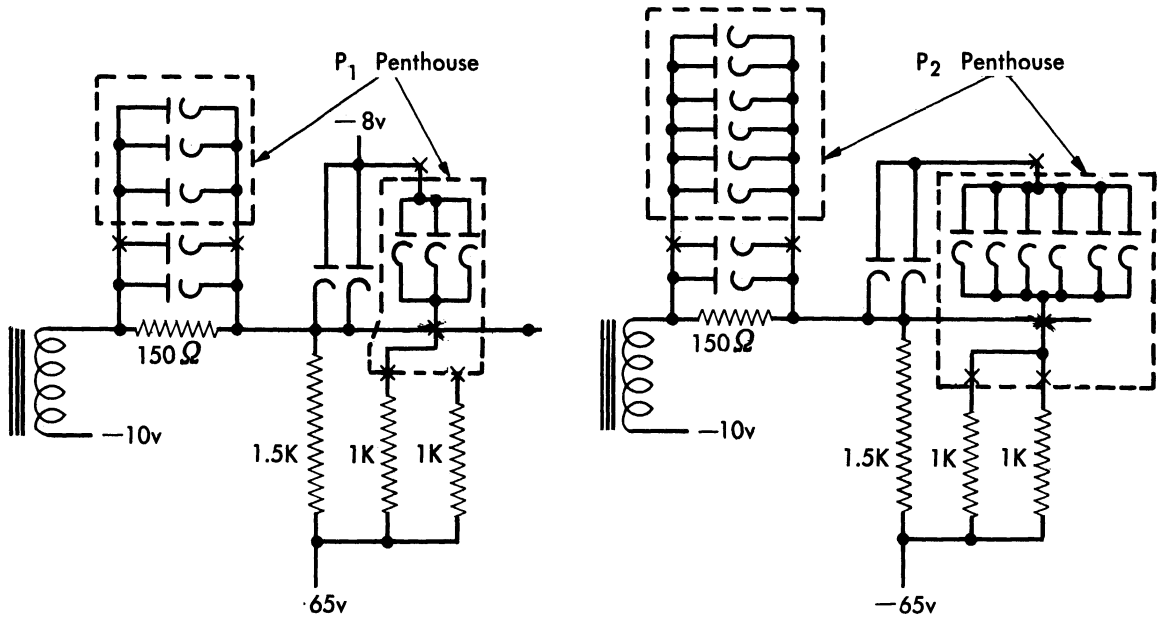
Or-gate pulses during time 1 and 2, due to pulses on A_2 and A_5 at time 1, and pulses on A_3 at time 2.

A_1 is the output of the regeneration gate which spreads the output pulse e_o to a full pulse width.

FIG. 1-14 OPERATION OF OR-GATE



a. AMPLIFIER AND OUTPUT BUFFER



b. OUTPUT BUFFER WITH P_1 PENTHOUSE ADDED

c. OUTPUT BUFFER WITH P_2 PENTHOUSE ADDED

FIG. 1-15 AMPLIFIER OUTPUT CIRCUITS

bobbin which has a slot for each of the three windings. The primary winding consists of 60 turns of No. 38 A. W. G. triple Formax coated wire. The two secondaries each have 6 turns of No. 31 A. W. G. triple Formax coated wire. The primary inductance is between 3 and 4.5 millihenries (measured at 250 kc). The Q averages about 52, and must be at least 35. The ferrite core has very low core loss and high effective permeability at 1 Mc. The method of construction of the pulse transformer keeps the leakage inductances at a minimum.

The circuit parameters of the amplifier stage are chosen so that the tube operates along a load line giving optimum power output. Maximum power output would be obtained by choosing the operating point of the tube at the knee of the plate characteristic. The actual operating point is chosen so that low-limit[1] tubes in conjunction with a three-millihenry primary inductance will operate just at the knee. Thus, all tubes will bottom, i.e., operate with plate voltage swinging below the knee.

The turns ratio was chosen to deliver maximum current to the load, consistent with the required rise time of 0.1 microsecond and a voltage swing of 20v. The largest resistance which loads the secondary is 1500 ohms, the value of the pull-down resistor in the output buffer. If a P_2 penthouse is used, this resistance is decreased to 375 ohms. The corresponding maximum load is a peak positive current of 160 ma. The capacitive load on the secondary may be as much as 300 micromicrofarads for a maximum and-gate load.

At the completion of a positive pulse, the plate current drops to a very small value and the plate resistance of the tube becomes essentially infinite. In addition, the load impedance on the secondary is decoupled by the diodes of the output buffer. The magnetizing current left in the transformer now excites an oscillation of the open circuit inductance and the plate capacitance. This oscillation carries the pulse to a negative peak of about -40v. The period of this oscillation is slightly longer

[1] A low-limit tube is one which conducts 45 ma of plate current when $E_{plate} = E_{screen} = +62v$, $E_{grid} = +2v$, and $E_{fil} = 5.7v$ (Sec. 1.5.2).

than 1 microsecond. If the oscillation were permitted to go unchecked, a spurious positive pulse would be picked up through the regeneration gate, which would broaden it to an almost full-sized output pulse. A damping resistor placed across the output buffer diodes is used to prevent such spurious outputs from occurring. The damping resistor is chosen so that the pulse is slightly underdamped instead of critically damped, allowing a small positive bump to appear following a single pulse. However, the bump is never enough to trigger the regeneration loop, since at least a 2v pulse is required to decouple the bumper diodes at the output buffer.

If the damping resistance in series with the bumper diodes of the output buffer is too low, then at the next pulse time the over damped transformer will have a magnetizing current which subtracts from the charging current available at the beginning of the next pulse. Since the open circuit inductance of the transformer is allowed to vary from 3.0 to 4.5 millihenries and the damping impedance depends on the characteristics of the diodes of the output buffer, it is obvious that it is not always possible to have zero magnetizing current at the beginning of the next pulse. In a train of pulses, the residual magnetizing current at the beginning of each pulse increases with each pulse until it approaches a stable value. The leading edge of the Nth pulse is then delayed by a measurable amount when N is larger than five or six (Sec. B.3.4 of Appendix B). The output pulse suffers additional delay due to the time necessary to charge the plate and load capacitance and also due to the effect of the leakage inductance.

1.4.3 Output Buffer

The normal method of driving and-gates from the output of the amplifier package is through the output buffer. An important consideration in the design of the buffer is the value of the pull-down resistor. The resistor value must be chosen low enough to give the output pulse a fall rate of at least 75v per microsecond. Since the normal load is the and-gates of other packages, the capacitive load is the wiring capacity of the leads to the and-gates as well as the stray capacity, C_2, at the and-gate itself. With no penthouse added, the pull-down current is approximately 40 ma. And-gates which the buffer drives require somewhat less

than 10 ma per input, and the pull-down current is enough to accommodate a four and-gate load as an external load in addition to the and-gate associated with the package internal regeneration loop. A P_1 penthouse increases the pull-down current to 100 ma; when a P_2 penthouse is used instead, it increases the pull-down current to 160 ma. As shown in Figure 1-15, the diodes added to the output buffer by the penthouse units are to accommodate the additional forward current when more than four gates are to be driven.

1.4.4 Pulse Delay Units

Pulse delays in integral multiples of 0.25 microsecond up to a maximum of 4.00 microseconds are obtained through the use of the delay line and termination packages. Each delay line package contains sixteen sticks of electrical delay line, each with 0.25 microseconds delay. Because of the frequent occurrence of certain delay times, the 16 sticks are preconnected within the package to provide the four package types described in Section 1.2.2.

The delay-line sticks are cut from a continuous roll of distributed-parameter delay line manufactured by the James Millen Company. The distributed inductance is formed by a single layer helix of fine Formax insulated wire which is wound on flexible plastic tubing. Covering the helix is a layer of thin Teflon tape, and surrounding this is a wire braid. The distributed capacity is that between the helix and the braid. In addition, the helix is covered by a thin layer of aluminum paint, which introduces mutual capacity between coils to compensate for the inductance lost as frequency increases. The wire braid is grounded through a loop of wire soldered around one end of the braid. Care must be taken not to ground the braid at other points, for this will affect the characteristics of the line. At one end of the delay-line stick, the grounded braid is cut back so that a section of the helix is exposed. The exposed helix forms a small inductor which tends to compensate for the wiring capacity of the long lead-in wire at this end.

The 0.25-microsecond delay-line sticks are calibrated to an accuracy of ± 0.003 microsecond. Thus the maximum error for four microseconds of delay is ± 0.048 microsecond. The characteristic impedance of the

line is 1350 ohms and the length of a 0.25-microsecond stick is approximately 5-3/4 inches.

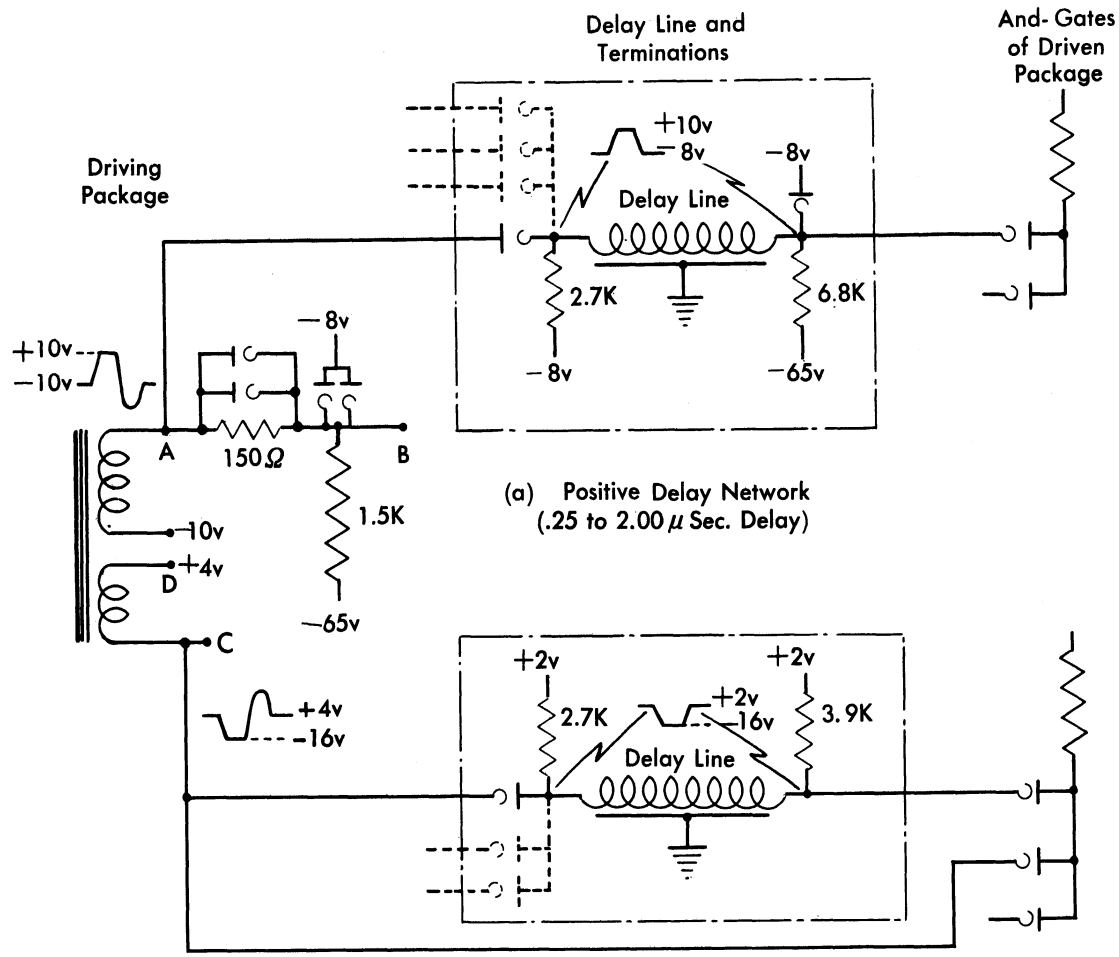
Figure 1-16 shows the circuits used to terminate delay lines and delay-line interconnections to the gate-amplifier packages.

For positive pulses, the output termination is a 6.8K resistor to -65v. Reflections which occur due to the impedance mismatch at the output end of the delay line are attenuated in the line and almost completely absorbed in the 2.7K input termination resistor. This resistance should be as large as possible, consistent with minimizing reflections, so that unnecessarily large driving currents are not required. A buffer diode at the input disconnects the pulse transformer during the negative backswing. The input termination may be used as an or-gate by the addition of free diodes as indicated by the dotted lines in Figure 1-15(a).

For negative pulses, a 3.9K resistor is used as an output termination. Again, any returning reflections are sufficiently absorbed in the 2.7K input termination. A buffer diode at the input disconnects the pulse transformer during the positive backswing. An or-gate for negative pulses may be made by adding free diodes to the input termination as shown by the dotted lines in the figure.

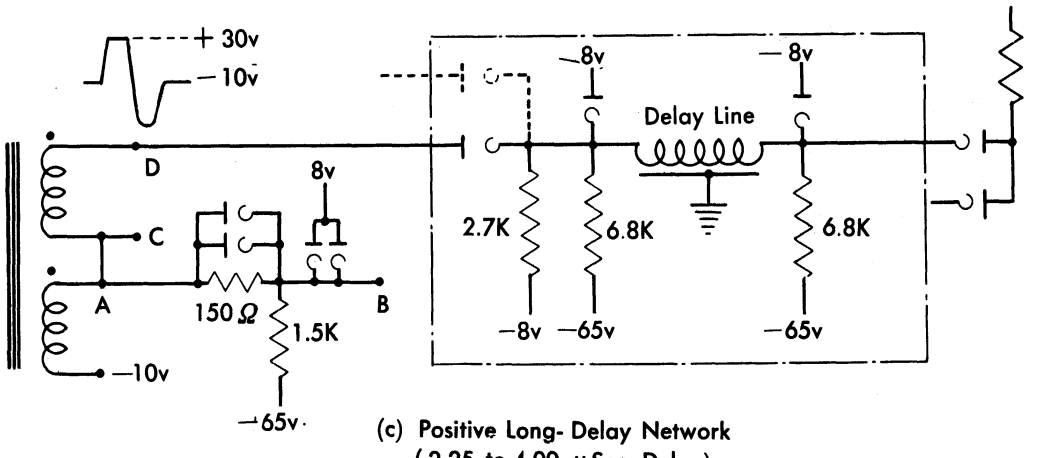
For positive pulse delays greater than 2 microseconds, the pulse attenuation becomes too great to allow the use of pulses of normal amplitude. A series connection of the two-pulse transformer secondaries in the driving package is then used to provide a pulse of twice the normal amplitude. This connection, Figure 1-16(c), provides sufficient drive for delay lines whose delay is between 2 and 4 microseconds.

Attenuation, distortion, and the accumulation of time delay errors become larger as the length of a delay is increased. These factors limit the maximum permissible delay between any two amplifier packages to 4.00 microseconds.



(a) Positive Delay Network
(.25 to 2.00 μ Sec. Delay)

(b) Negative Delay Network
(.25 to 2.25 μ Sec. Delay)



(c) Positive Long-Delay Network
(2.25 to 4.00 μ Sec. Delay)

FIG. 1-16 PULSE DELAY CIRCUITS

1.5 ELECTRICAL SPECIFICATIONS

1.5.1 Voltage and Current Requirements of Packages

Nine voltages are required to operate the gate-amplifier package. The maximum current requirements (Table 1-4) occur when an F package is used in conjunction with an amplifier package. These current values are taken with the package either pulsing continuously or not at all, depending on which condition draws the greater current. All supply voltages must be within ±5 per cent of the values given in Table 1-4.

TABLE 1-4

MAXIMUM POWER REQUIREMENTS OF GATE-AMPLIFIER PACKAGES

	6.3v a-c	-65v	-10v	-8v	-5v	+2v	+62v	+235v	Total Power
	(milliamperes)								(watts)
No penthouse	450	42	40	80	1.4	10	52	24	15.8
P_1 penthouse	450	100	6.2	110	1.4	10	50	27	20.1
P_2 penthouse	450	160	-30	130	1.4	10	48	30	25.0

The negative output winding of the pulse transformer is usually returned to +4v. If the maximum load is applied to this winding, a maximum current of 50 ma is required; and, if no load is applied, the current is zero. For this reason the requirement on the +4v supply is not included in the table.

The delay line package requires only a ground connection. The termination packages require -8v, +2v, and -65v, and the or-gate package requires -8v and -65v. Approximate maximum current requirements for these packages are shown in Table 1-5. These values are for a continuous train of pulses.

TABLE 1-5

POWER REQUIREMENTS OF TERMINATION AND OR-GATE PACKAGES

	-8v	+2v	-65v
	(milliamperes)		
Package Type T_1	70	11	90
Package Type T_2	44	27	55
Package Type R	44	0	55

1.5.2 Component Tolerances

All resistors must be ±5 per cent grade and should be rated at twice the operating power dissipation.

The 6AN5 tubes must, when operated with +62v on both screen and plate, pass the following tests:

1. Plate current must be more than 45 ma when the grid is at +2v and filament at 5.7v,
2. The difference between the plate current with the grid at +2v and filament at 5.7v and the plate current with the grid at -6v and filament at 5.7v must be more than 42 ma,
3. The plate current must not exceed 10 ma with the grid at -6v and the filament at 5.7v,
4. The difference between the plate current with the grid at +2v and the filament at 6.3v from the plate current with the grid at +2v and the filament at 5.7v must not be greater than 6 ma. However, if the plate current in the first test is greater than 55 ma, a decrease of 8 ma is permissible.

The diodes must pass the following tests:

1. The voltage drop with 20 ma of forward current must be less than 2v before soldering into the circuit and less than 2.2v after soldering,

2. With 40v of inverse voltage, the current must not be greater than

   a. 250 microamperes before soldering,

   b. 300 microamperes after soldering into package,

   c. 350 microamperes in operational use.

The pulse transformer must have a primary inductance not less than 3.0 nor more than 4.5 millihenries and must have a Q greater than thirty-five.

II

ASSEMBLY OF STANDARD PACKAGES TO OBTAIN FUNCTIONAL UNITS

The purpose of this section is to illustrate how functional structures of a computer are constructed from the basic packaged circuits described in the previous section. These include and-gates, or-gates, delay lines, and amplifier packages.

The symbolism which is employed in this section is similar to that of Section I. For brevity, the regeneration loop between the amplifier output and input is not shown in any of the diagrams in this section. However, it is to be understood that this loop always exists. For further simplification, both positive and negative amplifier outputs are represented by one line. This should cause no confusion since only an output which drives an inhibit input to a gate must be the negative output of the amplifier. It is also to be understood, but not indicated, that delay lines longer than 2 microseconds are driven with double-amplitude pulses. A rectangular symbol is used to indicate a delay line and its termination networks. The number inside the rectangle is the delay in microseconds. The general rules stated in the previous section, concerning maximum gate-drive capabilities and timing, are applicable to the following discussion and indeed must be rigidly adhered to.

In presenting the basic circuits, the logical symbols "and" and "or" (Fig. 1-3) are used, since this type of presentation provides a concise and compact representation of the circuit function. Because a delay of one clock phase occurs in each amplifier package the notation CP_n (n = 1, 2, 3, 4) is used at package inputs and outputs to indicate relative pulse times. The simpler circuits are discussed first; then combinations of the simple circuits are used to obtain more elaborate functional units.

2.1 STORAGE LOOP

A storage loop provides for the recirculation of N information pulses in a closed loop N microseconds long at a pulse repetition frequency of one megacycle. The ability to read out, read in, or modify stored

information is also provided. Electromagnetic delay lines are used as the storage elements. The other requirements are obtained by proper configurations of and-gates and or-gates. An amplifier is required because of the losses encountered in the gates and the delay line.

The basic storage loop is shown in Figure 2-1. Pulses in the storage loop (composed of the delay line, the amplifier, and gate 2) continue to circulate unless an inhibit pulse is applied on line $\underline{c}$ at phase CP_{n-1}. The information in the loop is available at the output of the amplifier at CP_n. Modification of stored information is accomplished by applying information pulses on $\underline{a}$ at CP_{n-1} and simultaneous inhibit pulses on $\underline{c}$.

If N = 1 (for which case a .75-microsecond delay line is used), the simple storage loop becomes a "dynamic flip-flop". This flip-flop is set to its pulsing state, called its "one" state, by a pulse on $\underline{a}$ at CP_{n-1}. The output is then a train of pulses at CP_n. The flip-flop is reset to its quiescent state, called its "zero" state, by an inhibit on $\underline{c}$ at CP_{n-1}. In this state the output provides no pulses. Thus the flip-flop has two stable states, the output being either a train of one-megacycle pulses or no pulses.

An example of a flip-flop is shown in Figure 2-2. This flip-flop is set to its "one" state by $(t \cdot s \cdot r) + (b \cdot \bar{a})$ at CP_{n-1}, and is reset to its zero state by $(\bar{e} + d)$ at CP_{n-1}.

Figure 2-3 is an example of a long storage loop. Information is entered into the loop at gate 1. An information pulse is erased from the loop by a pulse on $\underline{d}$ at CP_{n+1}. The length of the loop is either 11, 12, or 13 microseconds, depending on the control pulses on $\underline{b}$ and $\underline{c}$. Such provision for shortening or lengthening the loop permits information in the loop to be shifted right or left relative to some set of timing pulses.

2.2 TIMING-PULSE GENERATOR

In serial computing systems it is necessary to be able to identify specific digits within a word. This is accomplished by providing a unique timing pulse corresponding to each digit position. Such pulses are provided by a timing-pulse (T-pulse) generator.

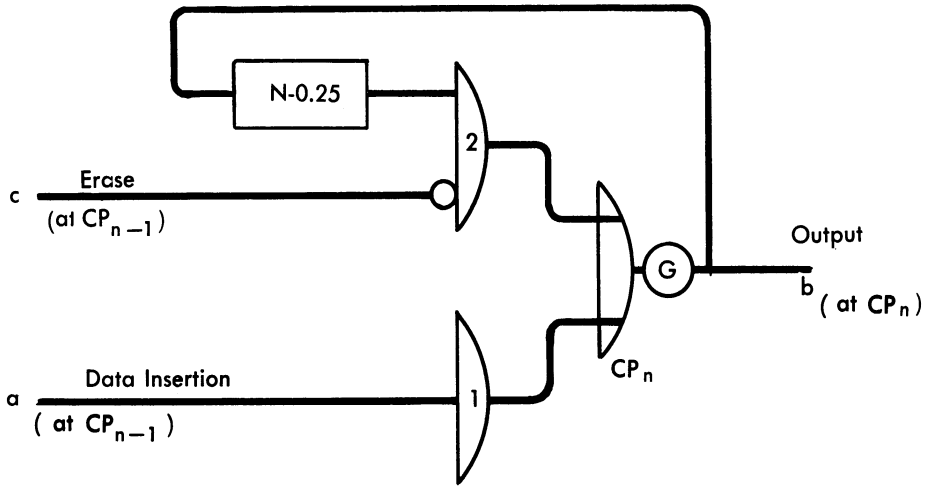


FIG. 2-1 SERIAL STORAGE LOOP FOR N PULSES

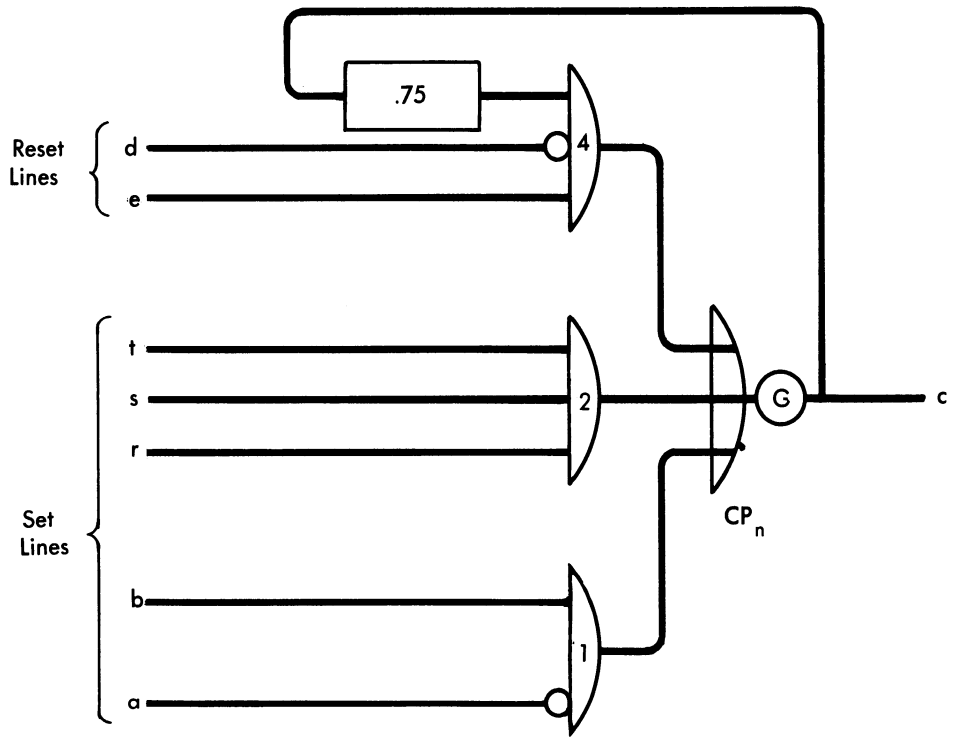


FIG. 2-2 FLIP-FLOP

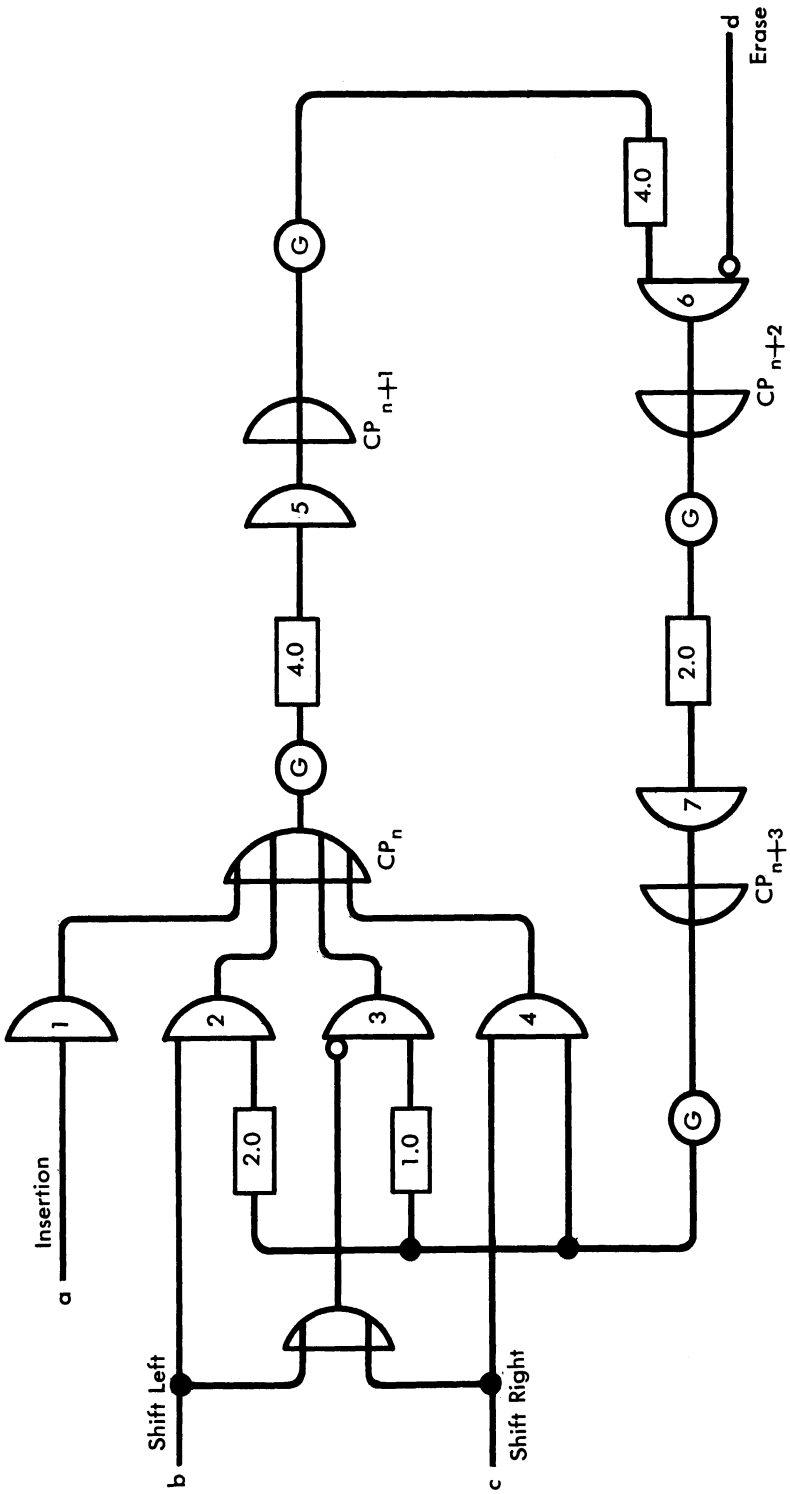


FIG. 2-3 LONG STORAGE LOOP

As an example of a timing-pulse generator we shall discuss a generator having a 12-microsecond period. An economical method for obtaining these pulses uses a 3-microsecond count-down loop in conjunction with a 4-microsecond count-down loop. Specific outputs of the two loops can be combined in and-gates, to provide a T-pulse at any pulse time in the 12-microsecond period. The package containing the and-gate used in this manner is referred to as a "T-blender".

Figure 2-4 shows the logic of the count-down loops, and the T-blender packages. The operation of the 3-microsecond count-down loop is as follows. Initially there are no pulses in the loop, and gate 1 is not inhibited. Therefore, the first stage of the loop produces, on line A_1, a pulse at a time denoted by the symbol $1CP_n$. One microsecond later, at a time called $2CP_n$, a pulse appears on A_2, while the previous output, A_1, which has been delayed, inhibits gate 1. At time $3CP_n$, a pulse appears on A_3, and the delayed pulse A_2 inhibits gate 1. The inhibiting of gate 1 ends at $3CP_n$ so that at $4CP_n$ a pulse again passes gate 1 and appears on A_1. The cycle then repeats. The 4-microsecond count-down loop is similar in operation, except that it starts a new cycle every four microseconds rather than every three. Figure 2-5 shows the time relationships of the A_n and B_m pulses.

T-pulses are generated by coincidences between selected A_n and B_m pulses in the T-blenders, as shown in Figure 2-4. The method of determining the proper combination of A_n and B_m to provide T_j is as follows:

$$n = j \text{ modulo } 3$$

$$m = j \text{ modulo } 4 \ .$$

For example, consider T_9:

$$n = 9 \text{ modulo } 3 = 3$$

$$m = 9 \text{ modulo } 4 = 1$$

$$\therefore T_9 = A_3 \cdot B_1 \ .$$

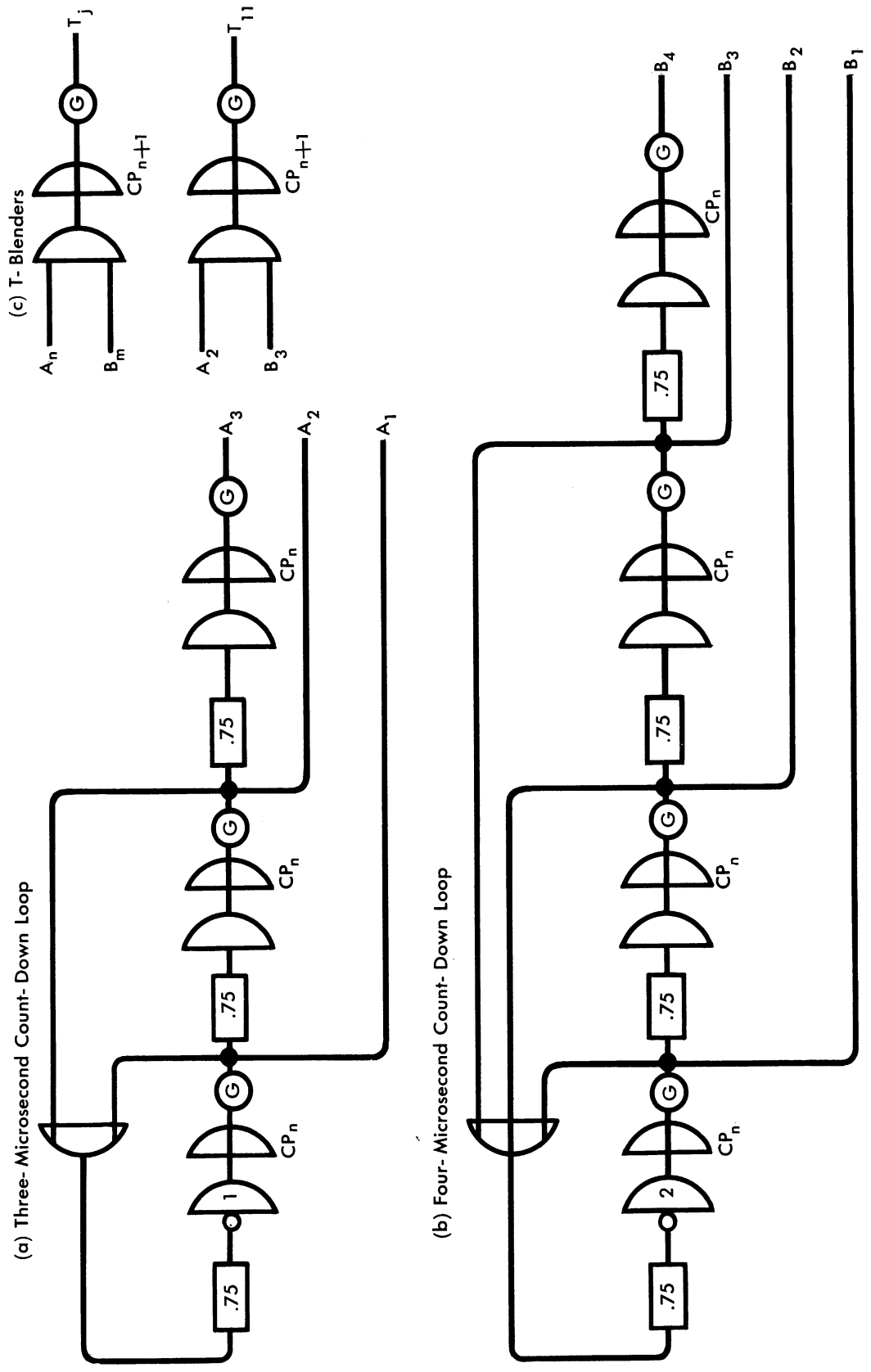


FIG. 2-4 12- MICROSECOND TIMING- PULSE GENERATOR

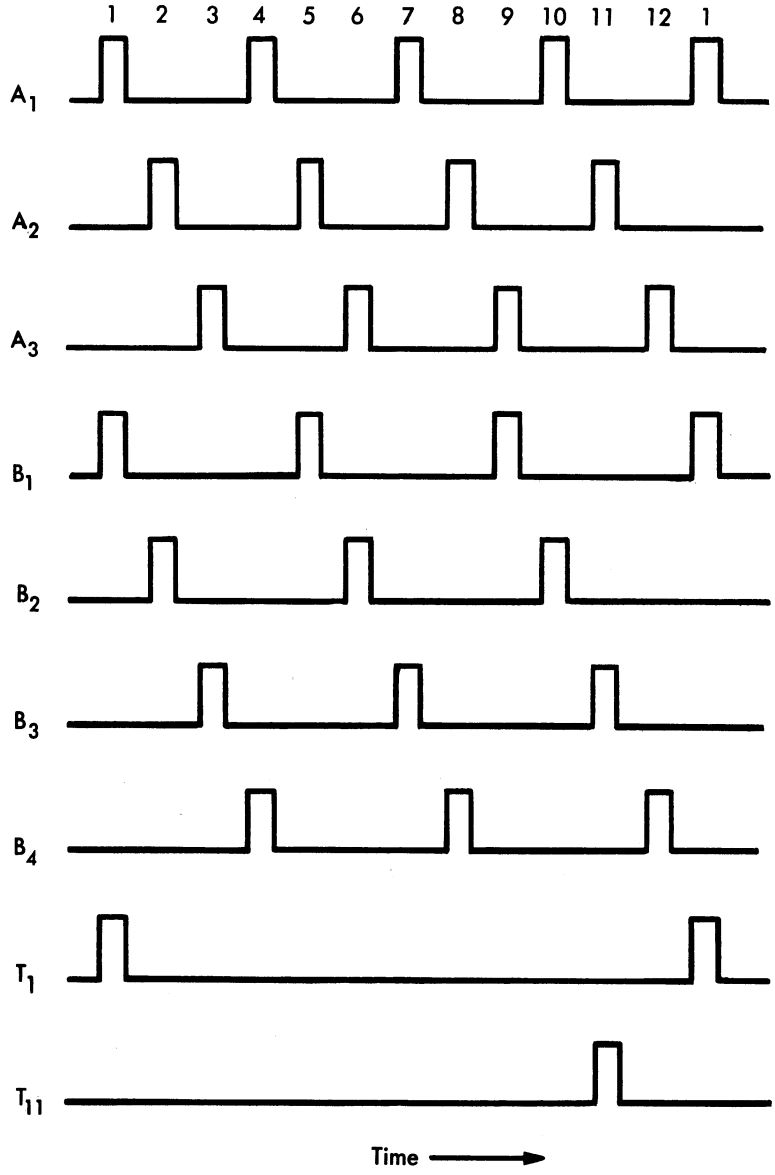


FIG. 2-5 T-GENERATOR SIGNALS

For T_{11}:

$$n = 11 \text{ modulo } 3 = 2$$

$$m = 11 \text{ modulo } 4 = 3$$

$$\therefore T_{11} = A_2 \cdot B_3$$

2.3 SHIFT REGISTER

Transfer of information frequently requires either a change in data rate or a serial-parallel conversion. These operations may be accomplished by the use of a shift register.

The logic of a typical three-stage shift register is shown in Figure 2-6. Gates 1 and 2 of each stage, in conjunction with the amplifier and delay line, form a dynamic flip-flop. Gates 3 and 4 in each stage are used to shift the information in each flip-flop to the right or left. The shift register is characterized by the following features:

1. Information can be inserted or extracted in serial or parallel fashion.
2. Information can be inserted or extracted serially from either end of the register; i.e., left or right shift.
3. Information can be inserted or extracted at any rate up to one megacycle per second.

Any movement of information to, from, or within the shift register must be accompanied by a sync pulse on the appropriate line; that is:

1. Parallel insertion of information on the lines P_1, P_2, and P_3 must be accompanied by a signal on line a .
2. Insertion of information on line d must be accompanied by a signal on line b .
3. Insertion of information on line e must be accompanied by a signal on line c .

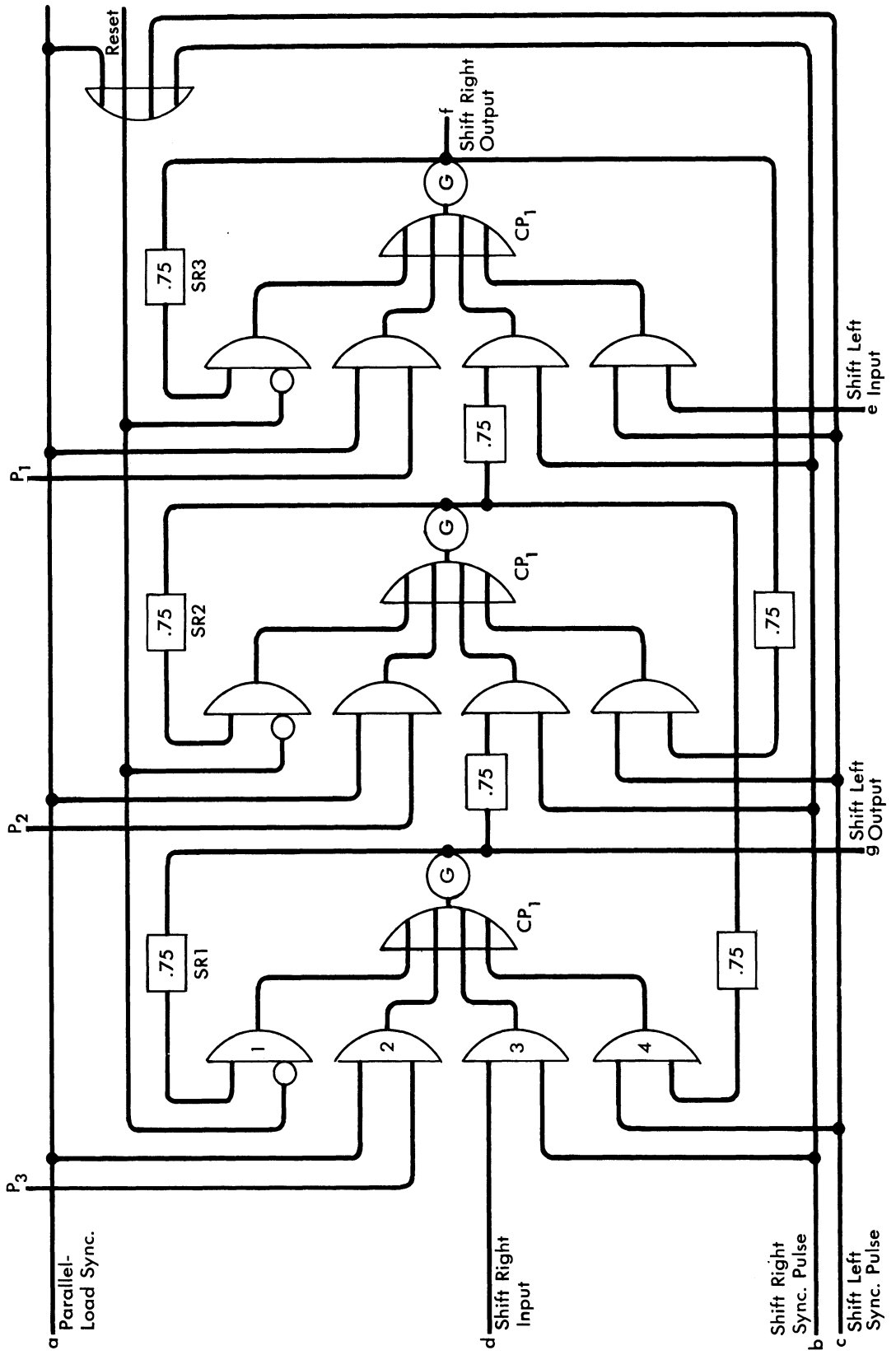


FIG. 2-6 SHIFT REGISTER

2.4 COMPARATOR

It is often necessary to compare the magnitudes of two numbers to determine whether equality or inequality exists. Figure 2-7 shows the logic of a simple comparator. This circuit provides an output on inequality and no output on equality, since the output C is given by:

$$C = (a \cdot \bar{b}) + (\bar{a} \cdot b).$$

To detect the inequality of two words, each consisting of several serial pulses, the comparator is used to test the digits of the two words sequentially, and a dynamic flip-flop is incorporated to serve as a memory device. This is most conveniently accomplished by the method shown in Figure 2-8. Before comparison begins, input c is pulsed to clear the dynamic flip-flop. The two words are then compared digit by digit. If equality exists for each digit pair, the flip-flop is not set. However, if an inequality exists for any digit pair, the flip-flop is set and a series of ones appears at output d until the circuit is reset at input c.

Figure 2-9 shows the logic of a serial equality comparator. The circuit is basically a dynamic flip-flop which is set by input c before the start of a comparison operation. An inequality existing at inputs a and b resets the dynamic flip-flop by stopping the recirculation of the stored "one".

2.5 COMPLEMENTOR

In digital computation a negative number is often represented by the complement of its absolute value. In binary arithmetic, two types of complements are frequently employed. The "diminished radix" or ones-complement of a number x is defined by

$$y = N - |x|$$

where N is the maximum value which x can take. An examination of the definition reveals that the ones-complement is obtained by changing all zero digits of x to one, and all one digits to zero. The basic comparator circuit shown in Figure 2-7 performs ones-complementation of one input if a sequence of pulses is applied to the other input.

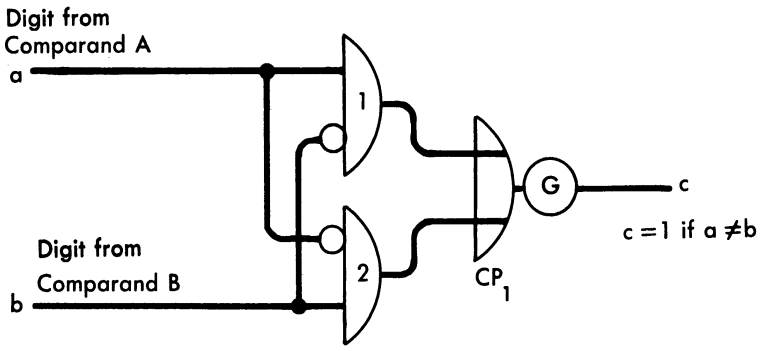


FIG. 2-7 SIMPLE COMPARATOR

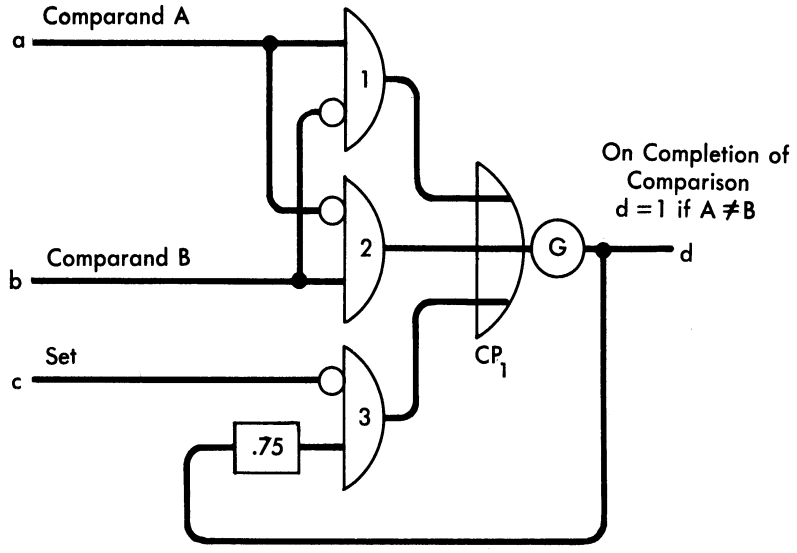


FIG. 2-8 COMPARATOR (INEQUALTY)

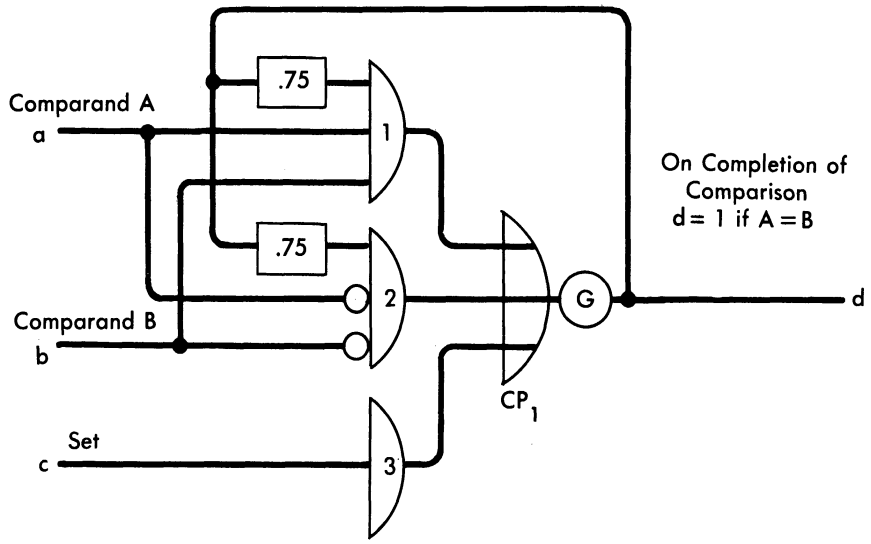


FIG. 2-9 COMPARATOR (EQUALTY)

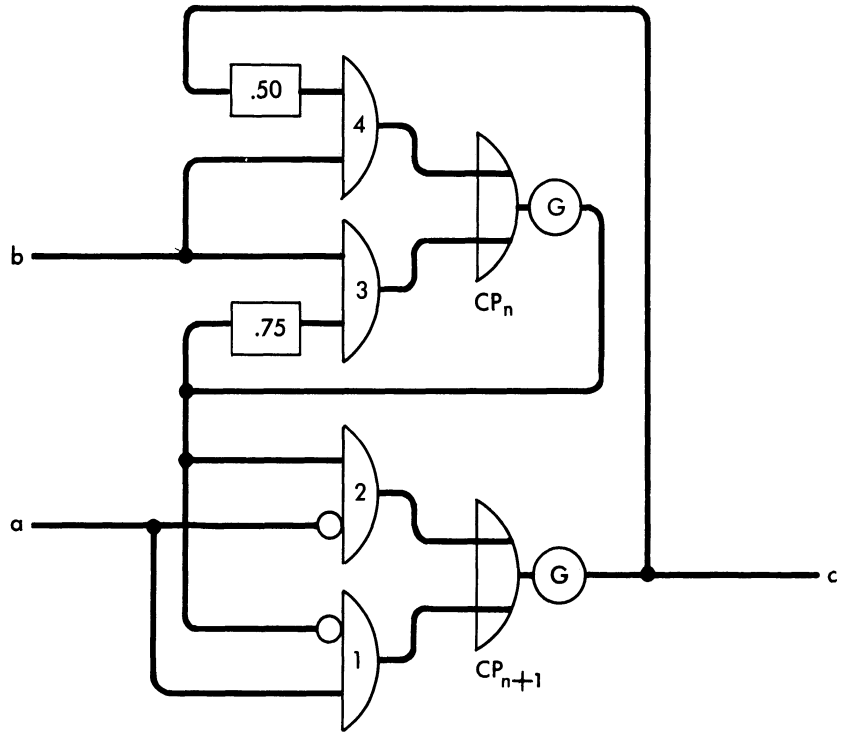


FIG. 2-10 TWOS-COMPLEMENTOR

The "radix complement" or twos-complement is defined by

$$y = N + 2^p - |x|$$

It may be obtained by the following procedure.

The low order digits are observed first, but no digits are changed until a "one" is encountered. The first "one" digit is not changed, but the remaining digits are ones-complemented. The logic of a twos-complementor for serial numbers is shown in Figure 2-10. It can be seen that gates 1 and 2 form a basic comparator circuit used as a ones-complementor while gates 3, 4, the associated tube, and the .75-microsecond delay line form a flip-flop which stores the fact that a one digit has occurred. To form the twos- complement of a number, pulses are fed to input b. The number to be complemented is fed to a. Gates 1 and 2 form no complements until the flip-flop is set. The flip-flop is set by the first one digit and thereafter gates 1 and 2 form the ones-complement. The twos-complement of the number appears serially at c.

2.6 ADDER

The rules for binary addition may be expressed simply by use of a "truth" table. The correct logic for operation on each digit pair is shown in Table 2-1.

TABLE 2-1

TRUTH TABLE FOR HALF-ADDER

Addend (a)	Augend (b)	Partial Sum (S')	Partial Carry (c')
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

The circuit which implements this truth table is termed a half-adder. The half-adder provides no means for operation on the carry digits to produce the true sum. It may be seen from Table 2-1 that the basic half-adder consists of a simple comparator (Fig. 2-7) and a two-input and-gate. The comparator logic produces the partial sum while the two-input and-gate determines the partial carry digit.

A complete two-input adder may be formed from two half-adders, as shown in Figure 2-11. This two-input adder gives the complete sum.

Among the many other designs for serial adders is the so-called "three-input adder" shown in Figure 2-12. The operation of this adder is essentially the same as that of the two-input adder.

For the sum S to be correct, either adder must satisfy the eight possible combinations of two input digits and one carry digit, as shown in Table 2-2. The subscript refers to the j-th digit of an N-digit number. The columns at the right indicate the gates used in each case.

TABLE 2-2

DIGIT COMBINATIONS

	$a_j + b_j + c_{j-1} = S_j$ and c_j					Gates Fig. 2-11	Gates Fig. 2-12
1	0	0	0	0	0	---	---
2	1	0	0	1	0	1·4	1
3	0	1	0	1	0	2·4	2
4	0	0	1	1	0	5	4
5	1	1	0	0	1	3	5
6	1	0	1	0	1	1·6	6
7	0	1	1	0	1	2·6	7
8	1	1	1	1	1	3·5	3·5·6·7

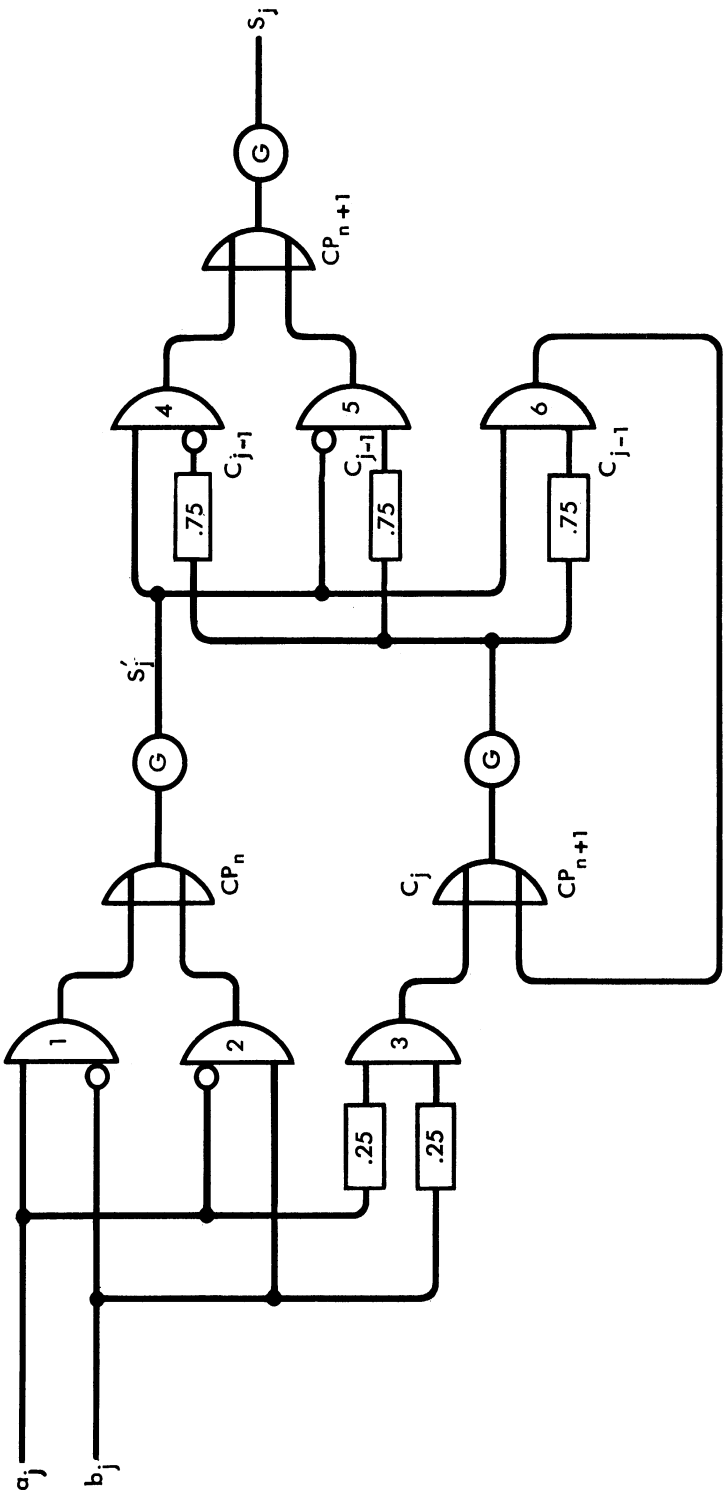


FIG. 2-11 ADDER

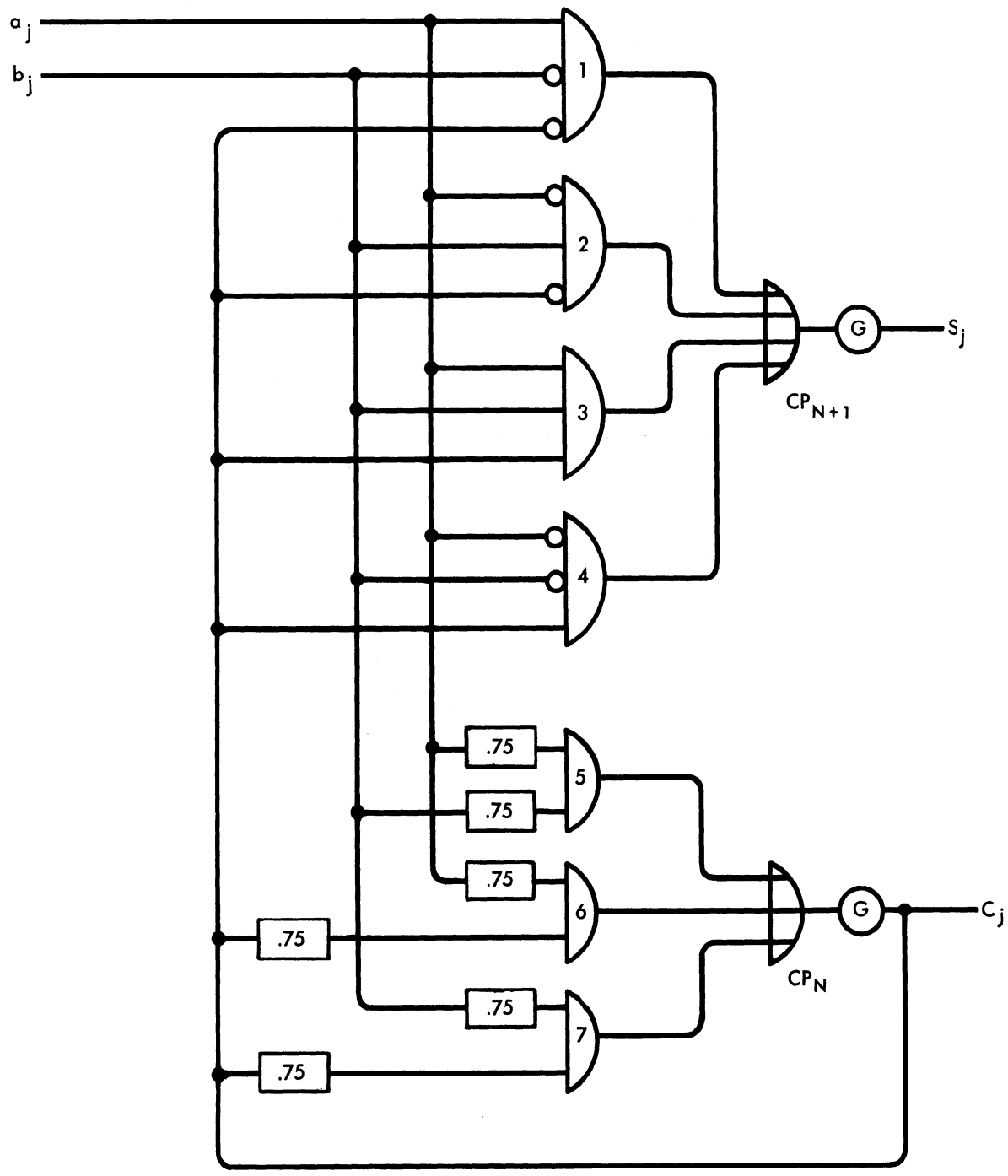


FIG. 2-12 THREE-INPUT ADDER

2.7 COUNTER

It is often necessary to count the occurrences of some signal in a computer in order to know when some other process or event should be initiated.

An economical counter structure makes use of a circulating storage loop, in which the binary count is stored. The circulating loop includes a circuit capable of adding unity to the stored count once during each circulation. The maximum counting rate for such a device is the reciprocal of the circulation time. Thus,

$$f_{max} = \frac{10^6}{\log_2(N+1)}$$

where f_{max} is the maximum counting rate in counts per second and N is the maximum count which can be registered.

Figure 2-13 illustrates such a circuit for the case N = 7 in which a 3-microsecond loop is employed.

The input to the counter is on line a, and must satisfy the condition that its period is some multiple of 3 microseconds, though not necessarily always the same multiple. Pulses to be counted on line a, must be in time synchronization with the least significant digit of the stored count if the circuit is to operate properly. The counter is reset by means of line b. Line b must remain on for at least 3 microseconds to ensure full reset. This serial-type counter is especially useful where the count in the counter is fed to a serial comparator to be compared with a control parameter.

The multi-stage flip-flop counter of Figure 2-14 requires more equipment but is capable of handling counting rates up to 10^6 counts per second. This counter is made up of identical flip-flop stages and can be extended to as many stages as desired. The input is applied to line a. An output signal is sent to the next stage each time a stage is reset from one to zero. The reset signal is generated by gates 1 and 2 in the two-stage counter

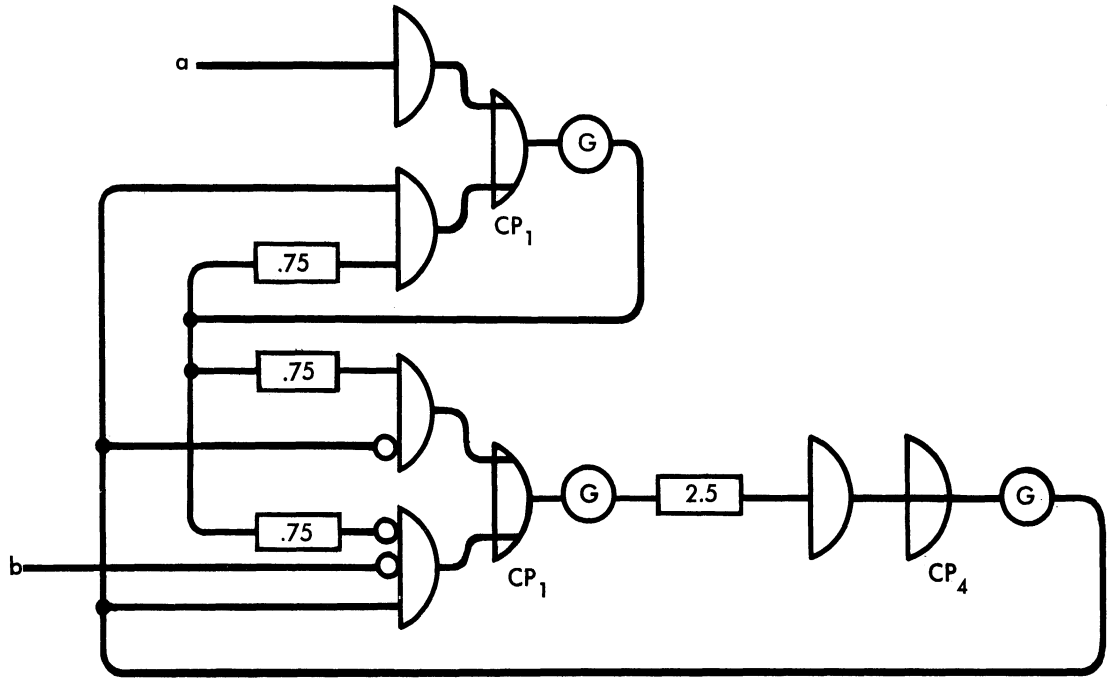


FIG. 2-13 COUNTER

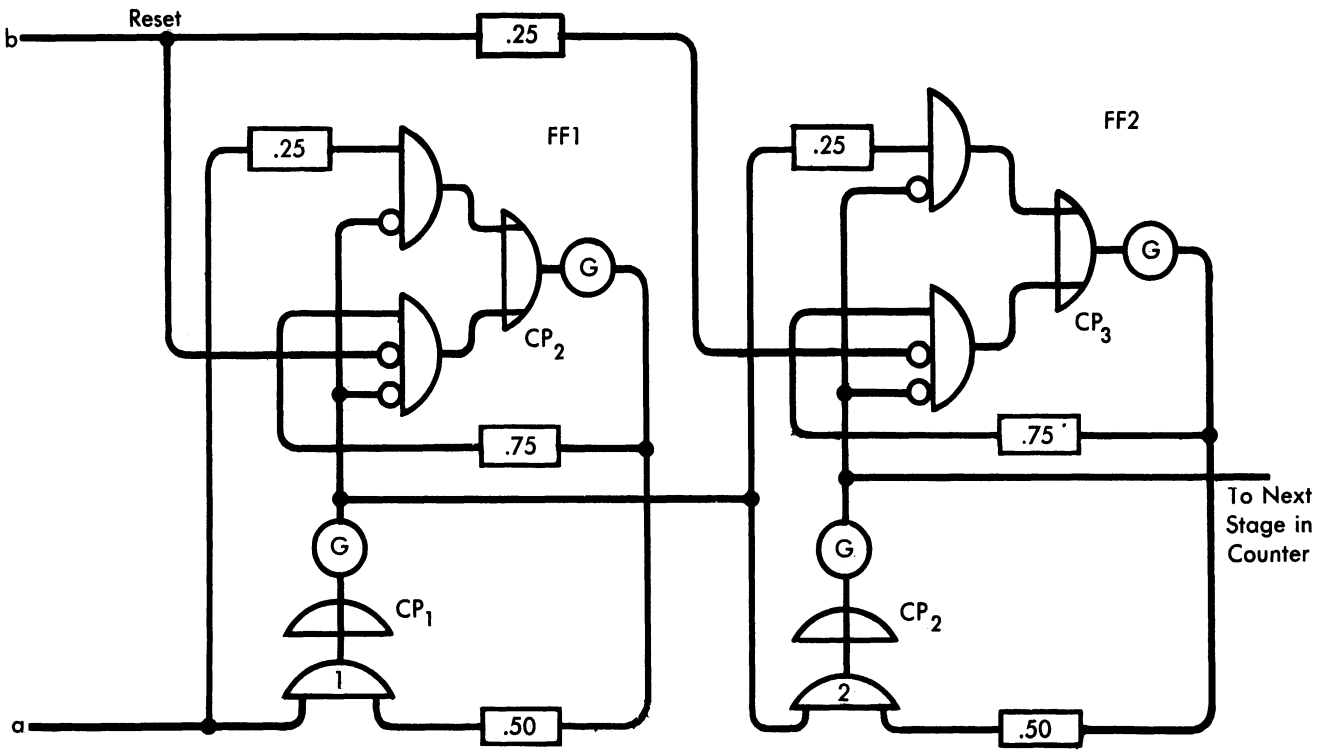


FIG. 2-14 MULTISTAGE FLIP-FLOP

shown. The count stored in the counter is indicated by the condition of the flip-flops (FF1 and FF2) in the various stages. Particular counts can be sensed by means of and-gates not included in Figure 2-14; e. g., a count of three would be sensed by feeding the outputs of FF1 and FF2 into an and-gate. A change of state propagates through the stages of the counter at a rate of one stage for each quarter-microsecond. In sensing the accumulated count, care must be exercised to avoid erroneous sensing during a change of state.

III

EXAMPLE OF A COMPUTER SUBSYSTEM: A SERIAL ARITHMETIC UNIT

This section illustrates how the functional units described in Section II may be interconnected to function as a subsystem of a complete computer. The example used is a serial arithmetic unit that can add and subtract ten-digit binary numbers.

3.1 INPUTS AND OUTPUTS

Each time the arithmetic unit is to operate, it receives two numbers, $\underline{a}$ and $\underline{b}$, as operands. It may perform either an addition or a subtraction upon those operands, in obedience to an add-subtract signal supplied to it on another line. Its output, $\underline{c}$, may then be either $\underline{c} = \underline{a} + \underline{b}$ or $\underline{c} = \underline{a} - \underline{b}$. The numbers $\underline{a}$ and $\underline{b}$, each specified by ten binary digits, enter the arithmetic unit as serial information . The first pulse (P_1) of each number denotes the sign of the number. The others (P_2 through P_{10}) give the absolute value of the number in standard binary form; i.e., if $P_n = 2^m$, then $P_{n-1} = 2^{m-1}$, where $\underline{m}$ can take either positive or negative integral values.

Twelve T-pulses (T_1, T_2, . . . T_{12}) are available in the system, though not all of these are needed by the arithmetic unit. The 12-microsecond period between successive T-pulses of the same number is called a minor cycle. Pulses in the arithmetic unit may occur at any of forty-eight discrete times within any minor cycle, since pulses derived from any T-pulse may be clocked, in successive packages, by each of the four phases of the clock signal.

The two operands appear on the information line in different minor cycles. The first pulse of either operand appears at time T_1 of its own minor cycle. Two control lines are also provided, one for each of the operands. A control signal appears on one of these lines while the related operand appears on the information line. These lines are identified as the "$\underline{a}$-control" and "$\underline{b}$-control" lines. A reset signal is furnished before each

add or subtract operation. The a-control, b-control, reset, and subtract signals are trains of pulses one minor cycle long, the first pulse of each occurring at time T_1. The first bit of the result appears on the information output line, c, at T_1 of the first minor cycle after the minor cycle in which the second operand was inserted.

3.2 FUNCTIONS OF SUB-UNITS

The method used in this arithmetic unit to add operands of opposite sign is to complement negative numbers and then add. The method used to perform subtractions is to change the sign of the subtrahend and then perform an addition; that is, positive subtrahends are treated as negative addends, and negative subtrahends are treated as positive addends. Correct operation of the arithmetic unit is not dependent on the position of the radix point in the operands. For the sake of simplifying the explanation, we assume the binary point to be at the extreme left end, making the magnitude of each number less than one.

A block diagram of the arithmetic unit is shown in Figure 3-1. The input complementor activating flip-flop (ICAFF) determines whether to complement the incoming information on the basis of the operand (a or b), the operation, and the sign of the operand. The input complementor (IC), when activated by the ICAFF, forms the ones-complement of the incoming information. The adder forms the sum of the two operands. The accumulator stores by recirculation the first operand until the second operand arrives. After the second operand appears, the accumulator stores the sum. A reset signal is used to erase the contents of the accumulator.

The sign storage flip-flop (SSFF) determines the sign of the sum or difference on the basis of whether or not the operands have been complemented and on the basis of the magnitude of the result in the accumulator. The output complementor (OC) forms the twos-complement of the information in the accumulator. The OC operates only if the sign of the result is negative. The output gates combine the sign and magnitude of the result in the required serial form.

3.3 OPERATION OF SUB-UNITS

The complete logical diagram of the arithmetic unit is shown in Figure 3-2. Gate 1 of the ICAFF is the recirculation gate for the flip-flop,

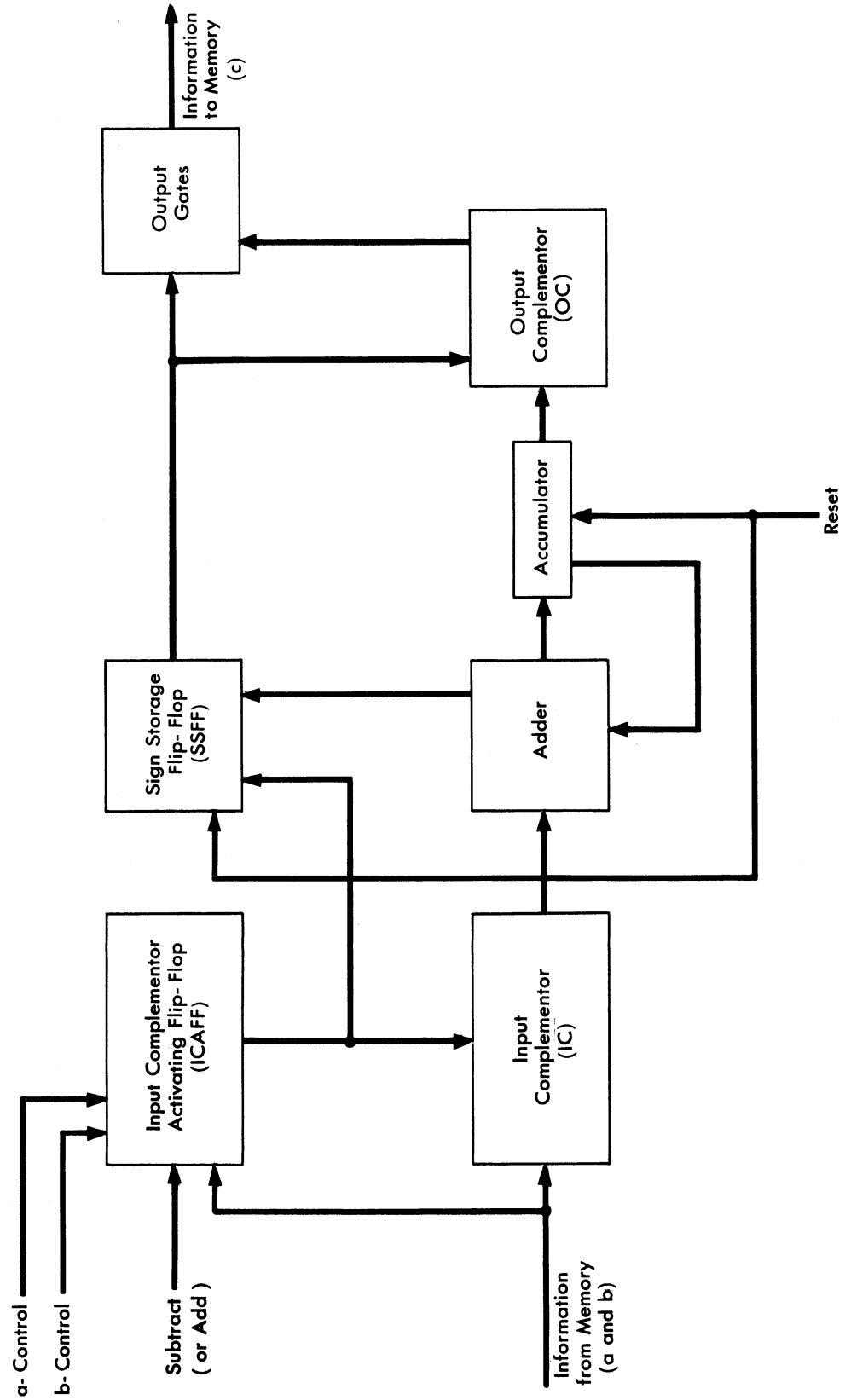


FIG. 3-1 BLOCK DIAGRAM OF ARITHMETIC UNIT

and is timed so that if the flip-flop is activated, its last pulse is put out at T_{10}. Gate 2 senses the sign of $\underline{b}$ for a subtract operation; if the sign is negative, the flip-flop is not turned on, so $\underline{b}$ is not complemented by the IC. Gate 3 senses the sign of $\underline{b}$ for an add operation; if the sign of $\underline{b}$ is negative, the flip-flop is turned on and $\underline{b}$ is complemented by the IC. Gate 4 senses the sign of $\underline{a}$ during either an add or a subtract operation; if the sign of $\underline{a}$ is negative, the output of this gate turns on the flip-flop and $\underline{a}$ is complemented.

The adder used here is the same as the unit described in Section 2.6, except for gate 19. This gate is used, when the ICAFF is on, to insert a digit (coincident with the low order digit of the result) into the carry loop of the adder. This added digit changes the ones-complement to a twos-complement. The accumulator is similar to the long storage loop described in Section 2.1. The information stored in the accumulator (the result of the operation) is defined as C_A. The OC differs from the unit previously described (Fig. 2-10) in that it has an additional reset input, T_{10}. The OC operates only when the SSFF is on.

The condition of the SSFF after an operation has been completed indicates the sign of the result and whether or not C_A is to be complemented before it is sent to the memory. When the SSFF is found to be off at the end of its operation, the result, $\underline{c}$, is positive and is correctly represented by C_A. When the SSFF is found to be on, the result is negative; C_A is the complement of the desired result $\underline{c}$ and must be complemented before leaving the arithmetic unit.

To understand when the SSFF should be on, we look for the conditions under which the result is negative. If both operands are positive, the result is positive and no complementation is needed. Similarly, if both are negative, the result is obviously negative. In the latter case, the arithmetic unit complements $|\underline{a}|$ before receiving the information that $|\underline{b}|$ is also negative, so it must complement $|\underline{b}|$ also, and then complement C_A to produce $|\underline{c}|$. When the operands are of opposite sign, the sign of the result depends on which operand has the larger absolute value; thus the sign cannot be decided until the adder has performed its operation, indicating which is the larger. If the positive operand has the larger absolute value

(so that the result is positive), the addition of the complement of the negative operand gives a C_A which is greater than one; thus C_A contains an "overflow" digit (one which has been carried into the P_{11} position). If, instead, the negative operand has the larger absolute value (so that the result is negative), the addition of its complement to the positive operand gives a C_A which is less than one, and which thus has no overflow digit. The absence of an overflow digit is seen to be sufficient to signify the need to complement C_A in cases where the operands have opposite signs. Since the overflow digit in C_A has the above-mentioned use in the internal operation of the arithmetic unit itself, a position is provided for it in the accumulator. However, an overflow digit is not a proper part of the arithmetic unit's output, and is not transmitted upon completion of the operation.

The SSFF is started by the output of gate 8, and stops only when all three gates (5, 6, and 7) are simultaneously inoperative. Because of the T_{11} input to gate 8 and the T_{11} inhibit to gate 5, starting and stopping of the SSFF occur only at the time the overflow digit may appear. The starting conditions are that the operand is negative and there is no carry digit in the overflow position; since the first operand's entry into the accumulator gives rise to no carry digits, a negative $\underline{a}$ always starts the SSFF. Assuming the reset input to be inactive, gate 7 is inoperative only when a carry digit enters the accumulator; this cannot occur until the second operand is in the adder. Gate 6 is inoperative only if the operand just received is positive. The combination of gates 5, 6, and 7 therefore shuts off the SSFF only when $\underline{b}$ is positive and there is a carry digit in the overflow position.

Table 3-1 shows how the requirements developed in the next-to-last paragraph above are matched by the SSFF performance rules given in the last paragraph above. The first three columns of the table show the input conditions which define each case; the next three show the three conclusions developed in the requirements paragraph; and the last three show the SSFF actions determined by the entries in columns 1, 2, and 6. The agreement sought is that among columns 4, 5, and 9.

TABLE 3-1

OPERATION OF SIGN STORAGE FLIP-FLOP

(1) Sign of $\underline{a}$	(2) Sign of $\underline{b}$	(3) Relative Magnitudes	(4) Sign of $\underline{c}$	(5) Output Complement Needed	(6) P_{11} Carry	(7) SSFF Action After Entry of $\underline{a}$	(8) SSFF Action After Entry of $\underline{b}$	(9) Final SSFF State
+	+	----	+	No	Maybe	Does not start	Does not start	OFF
-	-	----	-	Yes	Maybe	Starts	Does not stop	ON
+	-	$\|a\|>\|b\|$	+	No	Yes	Does not start	Does not start	OFF
		$\|a\|<\|b\|$	-	Yes	No	Does not Start	Starts	ON
-	+	$\|a\|>\|b\|$	-	Yes	No	Starts	Does not stop	ON
		$\|a\|<\|b\|$	+	No	Yes	Starts	Stops	OFF

IV

MECHANICAL DESIGN

The mechanical design of the computer was undertaken with the following aims in view:

1. Ease of maintenance.
2. Wherever possible, sub-assemblies should be removable to facilitate construction and subsequent test or modification.
3. Economical construction without sacrificing quality or reliability.

Each package of the computer is a self-contained plug-in unit. To perform various logical functions, such as those described in Section II, a number of packages are plugged into a chassis, where permanent wiring interconnects the package sockets. Chassis are mounted in racks, and connected together with patch cords. This manner of using plug-in packages has distinct advantages over the method in which an entire logical function, such as a shift register, is permanently wired on a standard chassis. The advantages are as follows:

1. Computer reliability is increased because computer packages can be removed and checked at regular intervals and any marginal components can be replaced.
2. The checking of individual packages can be done on a package tester suitable for all packages of one type, whereas the checking of a large logical unit permanently built on a chassis is more difficult.
3. Initial construction of the computer is simplified because the standard packages can be mass produced.
4. Maintenance of the computer is simplified because defective plug-in packages may be quickly removed and components within the packages replaced.
5. Because few different types of equipment are employed, a minimal amount of spare equipment must be stocked.

4.1 GENERAL DESCRIPTION

Figure 1-3 (Sec. 1.1) shows the parts of the gate-amplifier packages used in the computer. The small and-gate packages are always used clipped to an amplifier package, as shown at the top of Figure 1-3. Figure 1-4 (Sec. 1.1) shows the delay and termination packages. Figure 4-1(a) shows a group of packages installed in a chassis. There are spaces for 32 packages in each chassis. Figure 4-1(b) shows the chassis from the rear. Figure 4-2 is a rear view of two racks in which the chassis fit. There is space for 10 chassis per rack. Figure 4-3 shows the base of a rack, including the blowers that send air up vertical air ducts (which form the sides of each rack) to the several chassis. Figure 4-4 shows the complete MIDAC rack assembly.

4.2 DEVELOPMENT

4.2.1 Packages

The following rules were adopted to govern the mechanical designs of the basic packaged circuits:

1. All package types should be mechanically interchangeable.
2. It must be possible to isolate each component in a package from the others in the circuit without unsoldering any leads, so that each component may be tested individually.
3. Stray capacity at critical points must be kept to a minimum.
4. The package must be as small as possible, giving due consideration to the proper separation of components and to heat dissipation.
5. The circuits must be arranged so that the following conditions are satisfied:
   a. The number of basic packages used is minimized.
   b. The number of applications served by each basic package is maximized.
   c. The number of unused components in the computer is kept at a minimum.

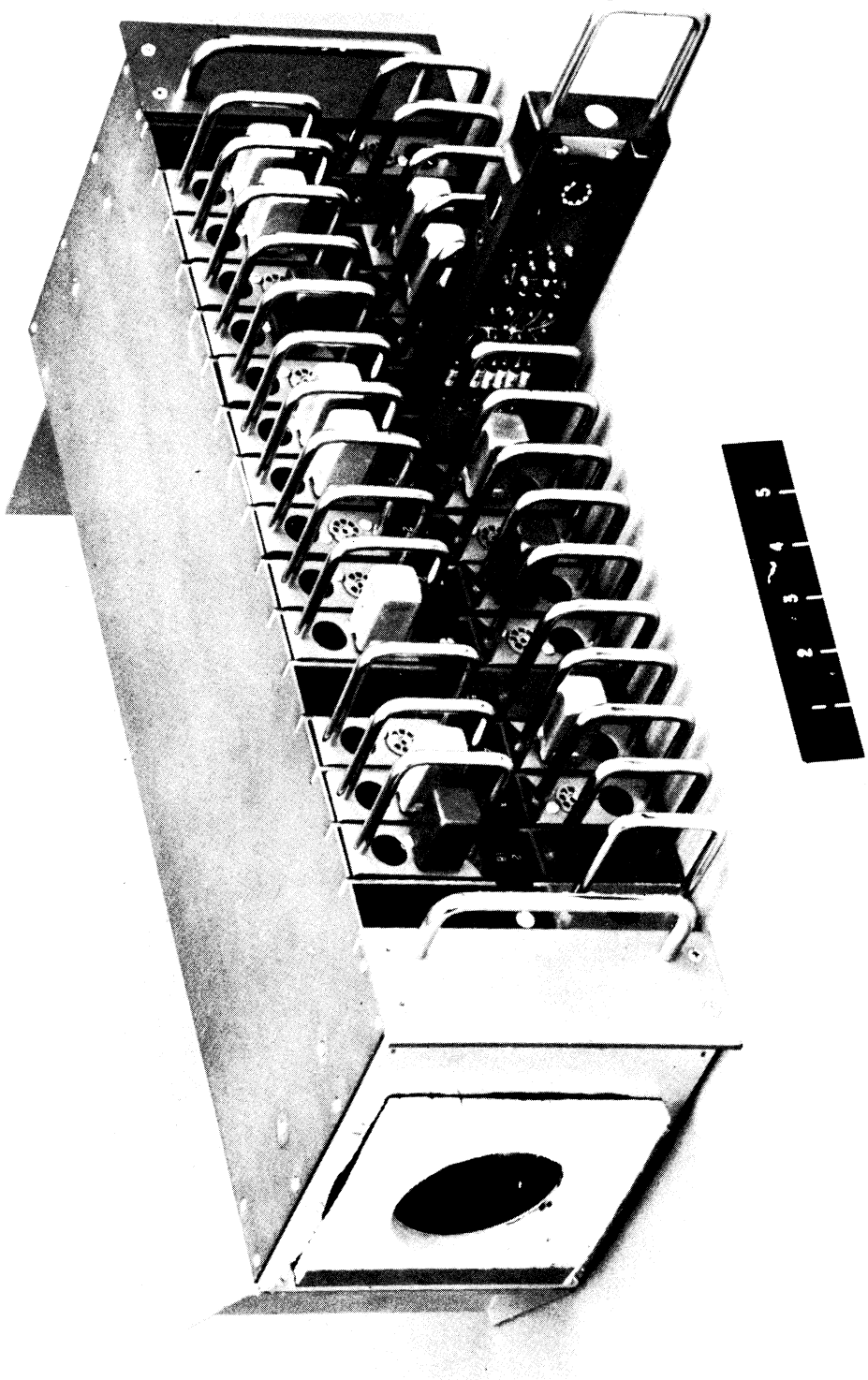


FIG. 4-1A CHASSIS (FRONT VIEW)

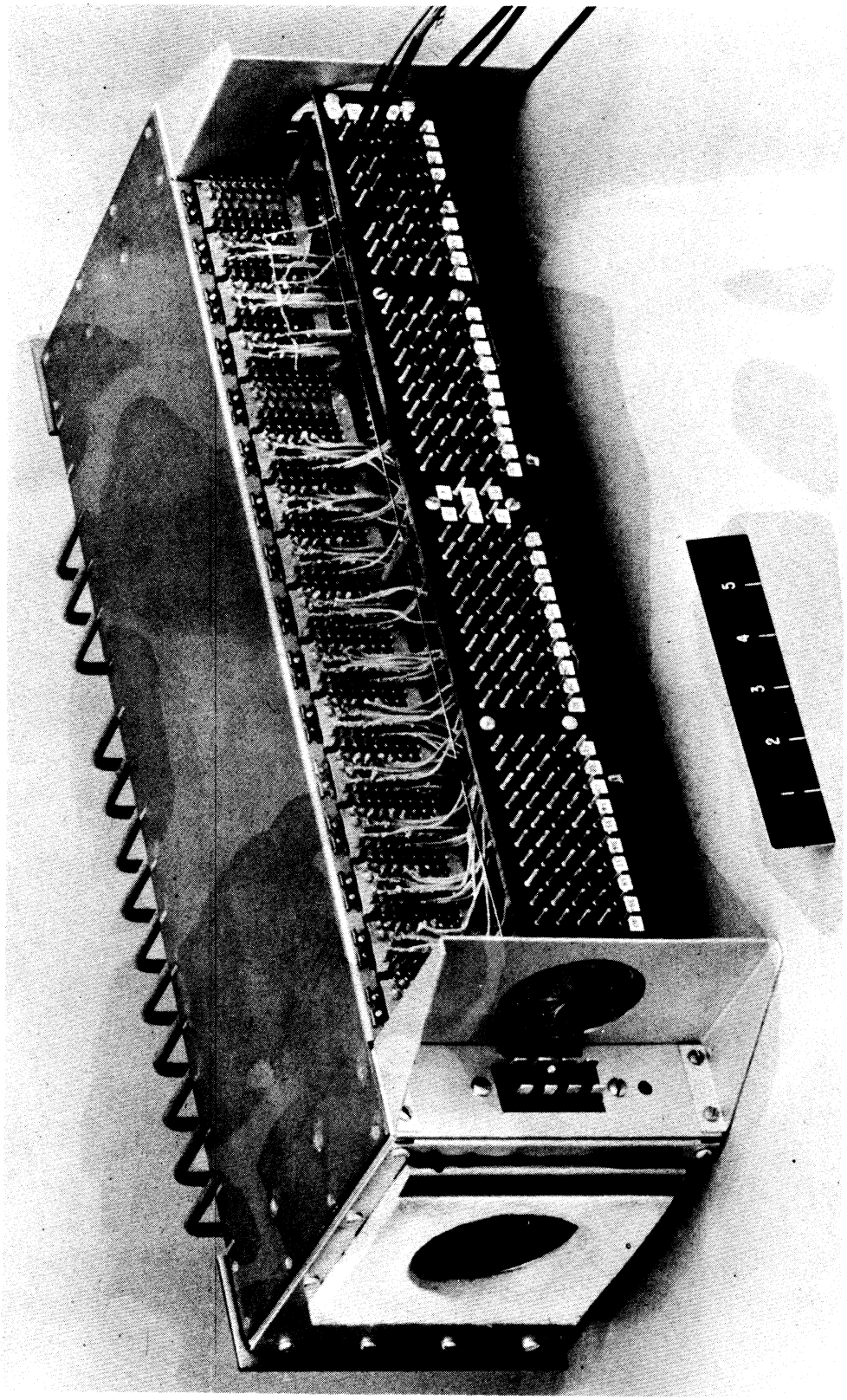


FIG. 4-1B CHASSIS (REAR VIEW)

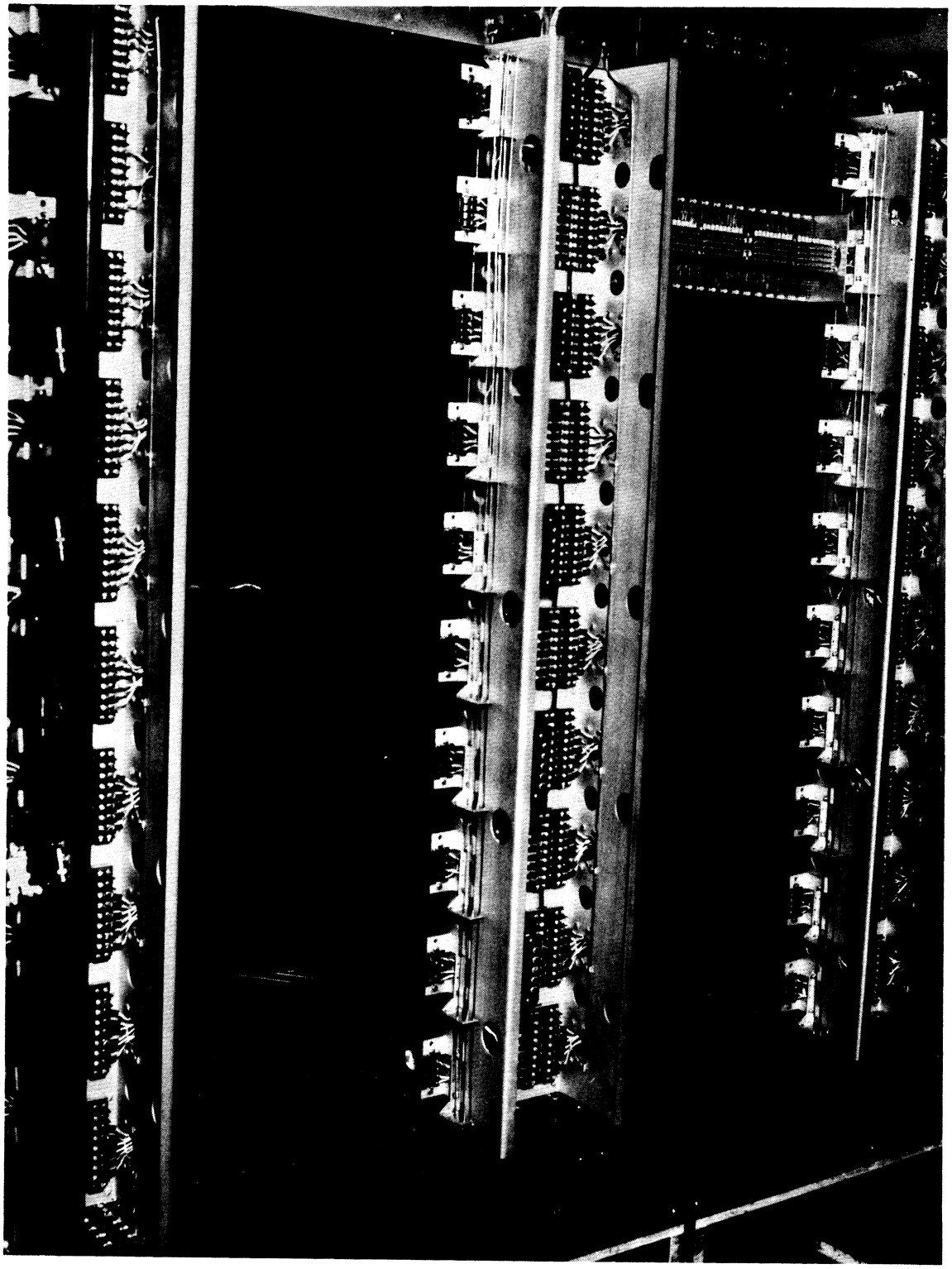


FIG. 4-2 RACK (REAR VIEW)

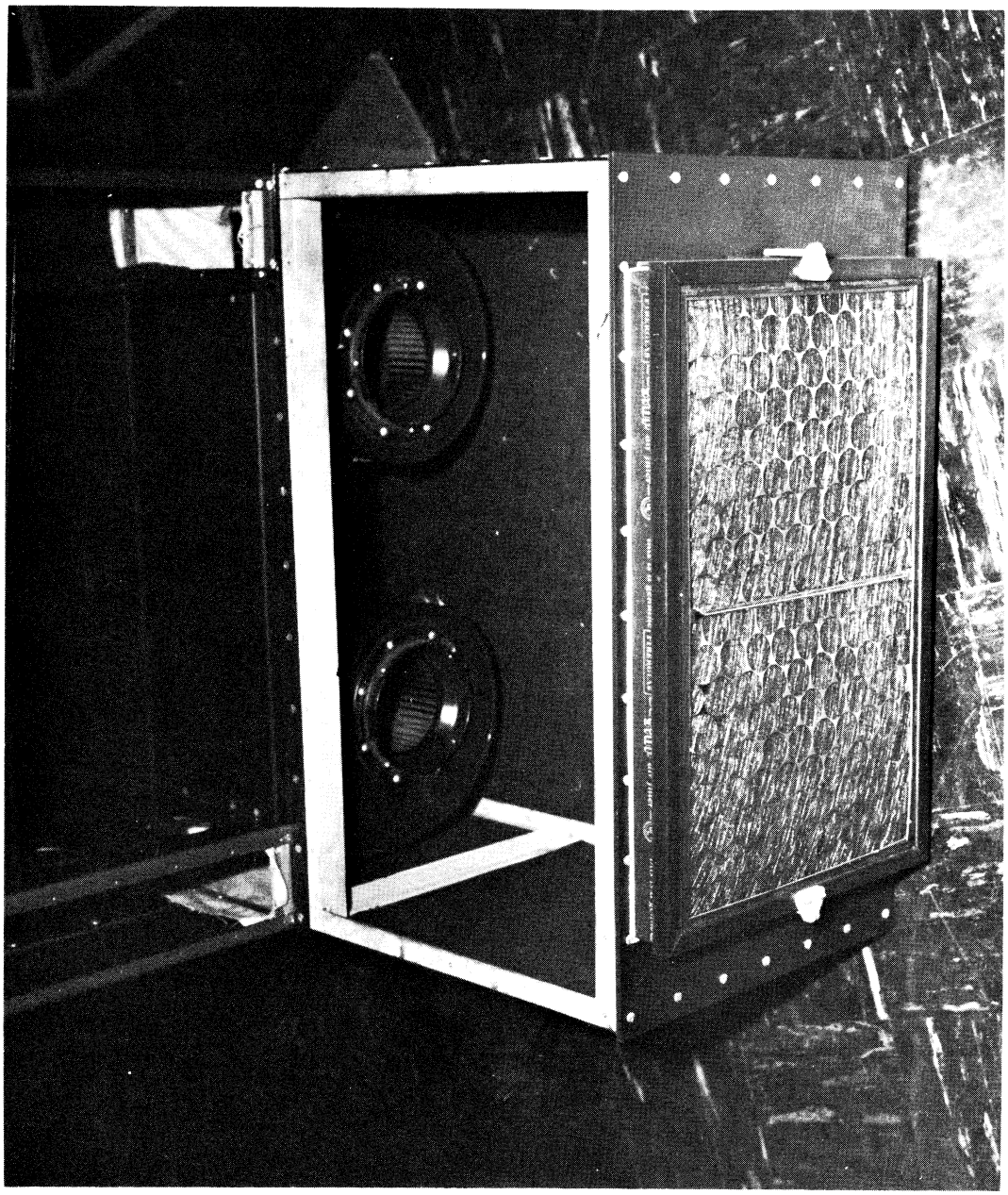


FIG. 4-3 BASE OF RACK, SHOWING BLOWERS AND FILTER

FIG. 4-4 COMPLETE MIDAC RACK ASSEMBLY

From a maintenance standpoint, the most expedient method of checking components is to plug the package into some form of checker that allows rapid switching of the test circuits from component to component. Thus all terminals of every component must be available at the connector pins.

In considering the stray capacity at critical points, it is noted that, in general, the basic circuits are connected as in Figure 4-5. Each amplifier is usually used to drive several circuits. Because the output of the amplifier is less disturbed by stray capacity than are other points in the circuit, the long leads to other packages are inserted at this point. The termination package is customarily located as close as possible to the delay line package with which it is associated.

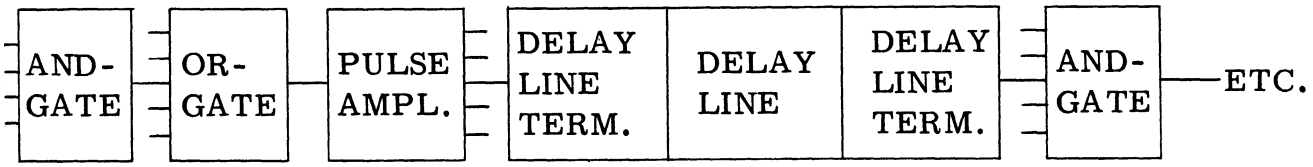


Fig. 4-5 CONNECTION OF BASIC PACKAGED CIRCUITS

The minimum size of the package is determined by the unit length of delay line in the delay line packages and by the size of the 35-pin connector. The unit of delay is .25 microseconds and requires approximately six inches of 1350-ohm delay line. The connector is 2-1/4 inches by 1 inch. The standard package is, therefore, 1 inch wide, 2-3/8 inches high, and 7-1/16 inches long.

The gating-amplifier package is separated into two sections. A single type amplifier package is employed, together with six types of and-gate packages, as described in Section I (Table 1-1). The two parts of the gating-amplifier package are held together by spring clips, so that they do not become separated during removal from the chassis.

The frames of all packages are aluminum stampings, and are colored during anodizing to provide an identifying color for each type of package.

The color code used in MIDAC is as follows:

Package	Color
And-gate type A	Red
And-gate type C	Yellow
And-gate type D	Green
And-gate type E	Blue
And-gate type F	Violet
Amplifier	Gold-Yellow
Delay Line	Green
Termination	Red
Or-gate	Silver

The packages are cooled by moving air. The air enters the side of each package through a hole in its frame, passes first over the diodes and then over the warmer resistors and tube, and leaves the package through a hole in the front. Packages are held against the air duct in the chassis by beryllium copper clips.

4.2.2 Chassis

One chassis holds 32 packages. The full chassis is small enough to be handled easily by one person, yet is not so small that the computer is split up into a large number of parts.

The chassis structure (Fig. 4-1) consists of two end boxes connected by an upper and a lower skin and a central horizontal air duct, all of which fasten to the end boxes. The back of the air duct consists of a sheet of insulator board (Fig. 4-6), on which are mounted the power distribution busses and lugs for use in connecting the package socket pins to the power busses. The lugs on the power strip are so arranged that any of the ten supply voltages may be easily connected to any package pin. Connectors at the ends of the chassis are used to bring power from the rack to the power distribution board.

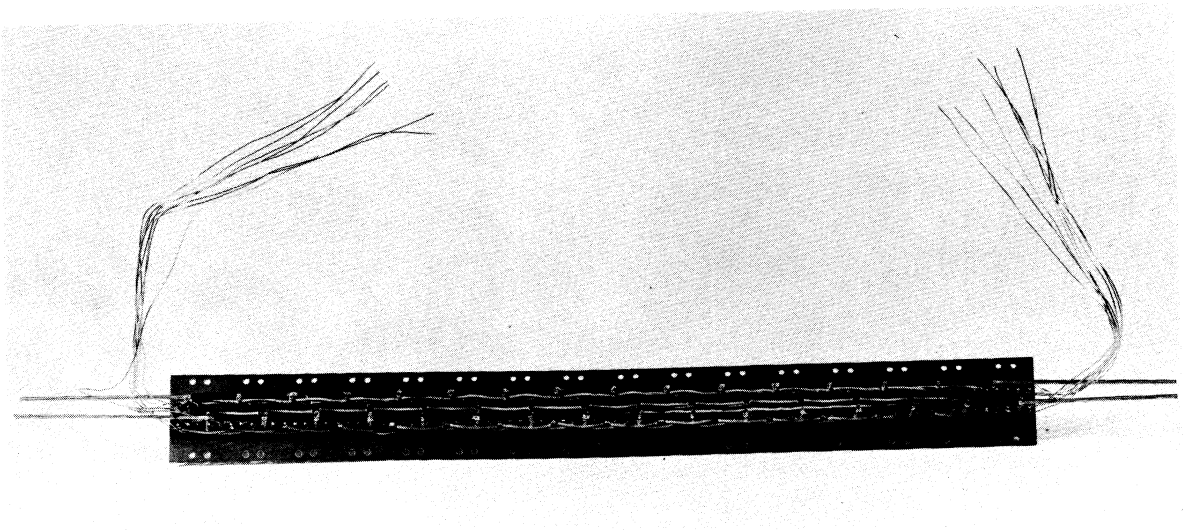


FIG. 4-6 REAR PLATE OF HORIZONTAL AIR DUCT

A patch panel of 204 pins is mounted on stand-offs behind the power strip. The stand-offs also carry the busses for the four clock phases. The patch panel is used to connect inter-chassis signal wires. Signal wires between packages within a given chassis are permanently wired to the package sockets. As shown in Figure 4-1(b) permanent wiring is also installed from the power strip and the patch panel to the package sockets.

In addition to the chassis for packages, a second chassis of the same over-all dimensions was designed. Circuits not in package form may be installed in one of these chassis and plugged into the rack at any desired location. An example of such a chassis is the one in which the clock is mounted; this may be seen in Figure 4-4.

4.2.3 Rack

Figures 4-2 and 4-4 show the vertical columns at each side of each rack. These are the vertical air ducts which act as plenum chambers to supply the ends of each chassis with forced air for cooling. The top of

the rack is a horizontal cable channel of the same form as the vertical duct. Felt insulation is applied to all inside surfaces of the vertical air ducts to prevent "sweating" when the air on the inside is cooler than the air on the outside.

The power voltages are brought into the rack through the horizontal cable channel and are connected to Jones sockets mounted in the back of the cable channel. Power harnesses run down the back of the air ducts and plug into the Jones sockets at the top, as shown in Figure 4-2. Voltages are distributed from the harness to the chassis through a fuse block. The fuses are of the indicating type and are connected to an interlock system which cuts off the power when any fuse is blown. Filament voltage is kept as uniform as possible throughout the computer by providing a filament transformer for each two chassis and mounting these transformers on the air duct next to the chassis they serve.

All signal connections to and from each chassis are made to the patch panel strip of the chassis. Signal connections between any two chassis are made by connecting patch cords between the appropriate patch panel pins. Patch connections between chassis in the same rack are made directly, but connections between chassis in different racks are made through two-inch phenolic tubes running through the five pairs of holes shown in the vertical members in Figure 4-2. Connections to units outside the racks are made by patch cords to the patch pins in the cable channel at the top of the rack and then by cable out of the rack.

The base unit of each rack houses the blowers and air filters and serves as a catwalk for work on the computer. The base unit in Figure 4-3 is uncovered to show the blowers used to force air into the vertical ducts. The choice of blowers was made after a study of the cooling requirements of the computer.

The required air flow, in cubic feet per minute, is

$$CFM = \frac{BTU/Hr}{1.08 \times \Delta t} ,$$

where BTU/Hr is the power dissipated and Δt is the maximum permissible temperature rise, in Fahrenheit degrees. For reliable operation, diodes should not operate at more than 100° F. If room temperature is considered to be 75° F, Δt is then 25° F. The hottest package combination, including a Type F and-gate and a P2 penthouse, dissipates 22 watts, or 75 BTU/Hr. Then for the case of an entire rack completely filled with such packages, the required flow is 860 cu. ft./min. Two ILG B-12 blowers, operating in a typical rack, supply 870 cu. ft./min. with a static pressure difference of 3/4 inch of water between blower inlet and outlet.

The heat is finally removed from the room by a 10-ton capacity air conditioner. An air conditioner was chosen over several other methods of heat removal because it allows control of humidity, is fairly economical, and can be moved with reasonable ease.

4.3 SUGGESTED IMPROVEMENTS

4.3.1 Packages

While a rack and 10 chassis can be made for less than $5000, enough packages to fill a rack, at an average cost of $100 each, cost $32,000. A means of reducing the cost of the individual package is clearly desirable.

Printed circuitry was examined with a view to cost reduction. In addition to cost reduction, the following factors point toward printed circuits:

a. Production rate may be greatly increased with only unskilled labor required for assembly.

b. Maintenance is simplified, as all components are easy to replace.

c. Visual inspection of the finished product is simplified.

d. Computer reliability is increased because wiring shorts are eliminated, components are not stressed by wrapping procedures, and components are protected against damage in handling.

Figures 4-7 and 4-8 show etched-circuit package design possibilities. The removable panel is the interchangeable and-gate section.

4.3.2 Chassis

The pre-wiring of chassis sockets is a desirable feature, and is made possible by a chassis (Fig. 4-9(a)) designed to hold etched-circuit packages. The chassis consists of four identical extruded angles bolted to a plate at each end. Sockets that have been pre-wired in a jig may be inserted separately in the angles. The power strip in this chassis has been simplified and consists merely of power bus wires inserted in insulated spacers. Connection is made directly to the bus wire instead of to a lug, as in the present chassis. Figure 4-9(b) shows a rear view of the new chassis design. All patch pins are in the Cinch plugs on the ends instead of being along a patch board across the back of the chassis. The improved system permits easy removal of the chassis if necessary. Under the present system, a large number of patch cords must be labeled and removed before a chassis can be removed from the computer. In the improved design, the power wiring connection of the rack is located at the front of the chassis.

4.3.3 Racks

The general organization of the rack may be changed to reduce the congestion at the back of the racks. The power harness, fuses, filament transformers, etc., could be moved to the front of the vertical air ducts. The air filter could be mounted in the front of the base unit and the extension of the base unit at the back of the rack could be reduced to provide easier access to the chassis at the bottom of the rack.

The construction of the vertical air ducts can be simplified and improved. Figures 4-10(a) and 4-10(b) show a segment of the suggested improved rack. The vertical air ducts consist of front and back U-channels held together by removable plates. The plates on the inner side of the air duct are arranged so that the horizontal air duct required for each package chassis can be put in if a package chassis is to be used, but left out if a non-standard chassis is to be used. The outer sides of the duct are also removable so that baffles may be inserted to equalize air flow and eliminate hot spots.

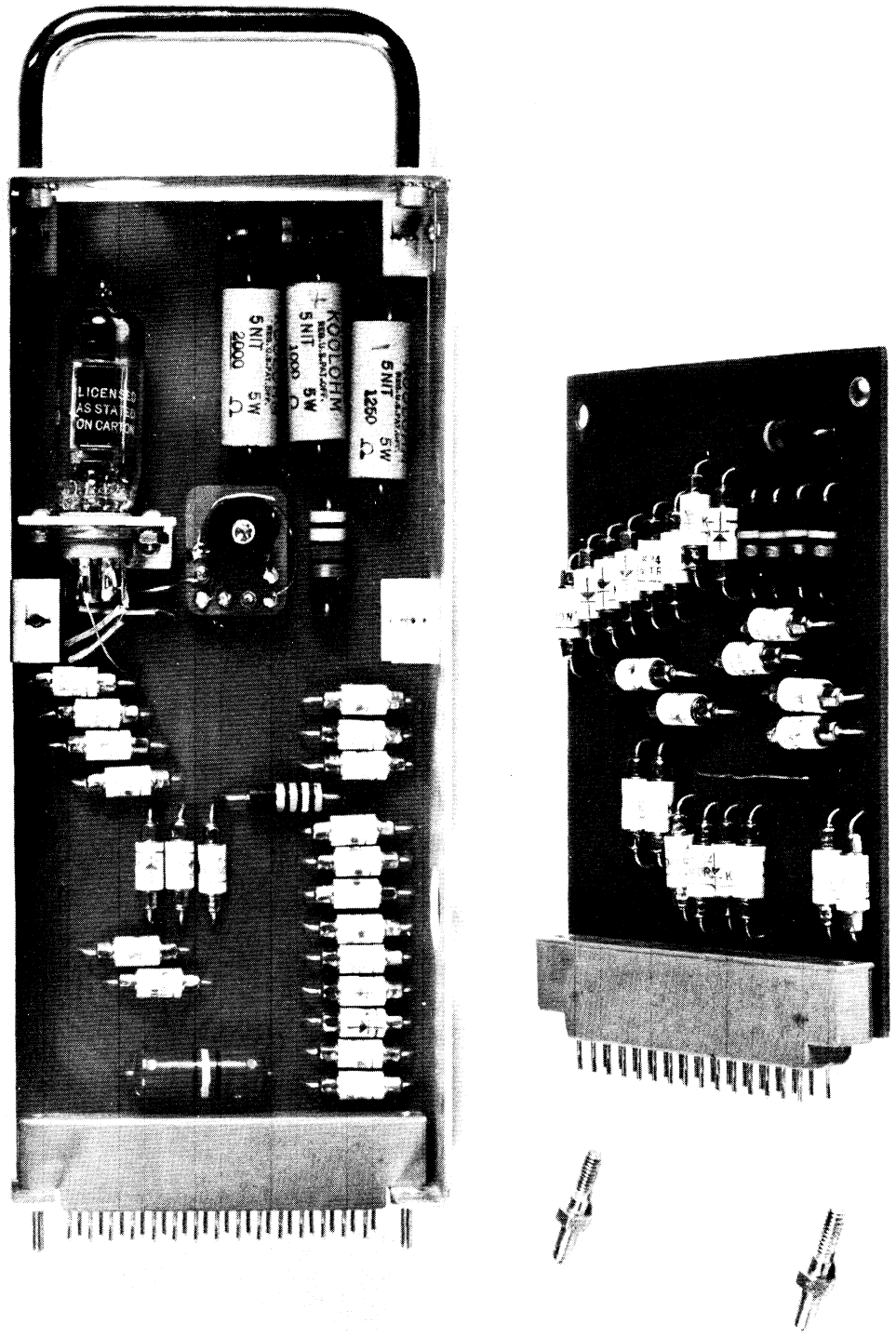


FIG. 4-7 INTERIOR OF PRINTED CIRCUIT PACKAGE

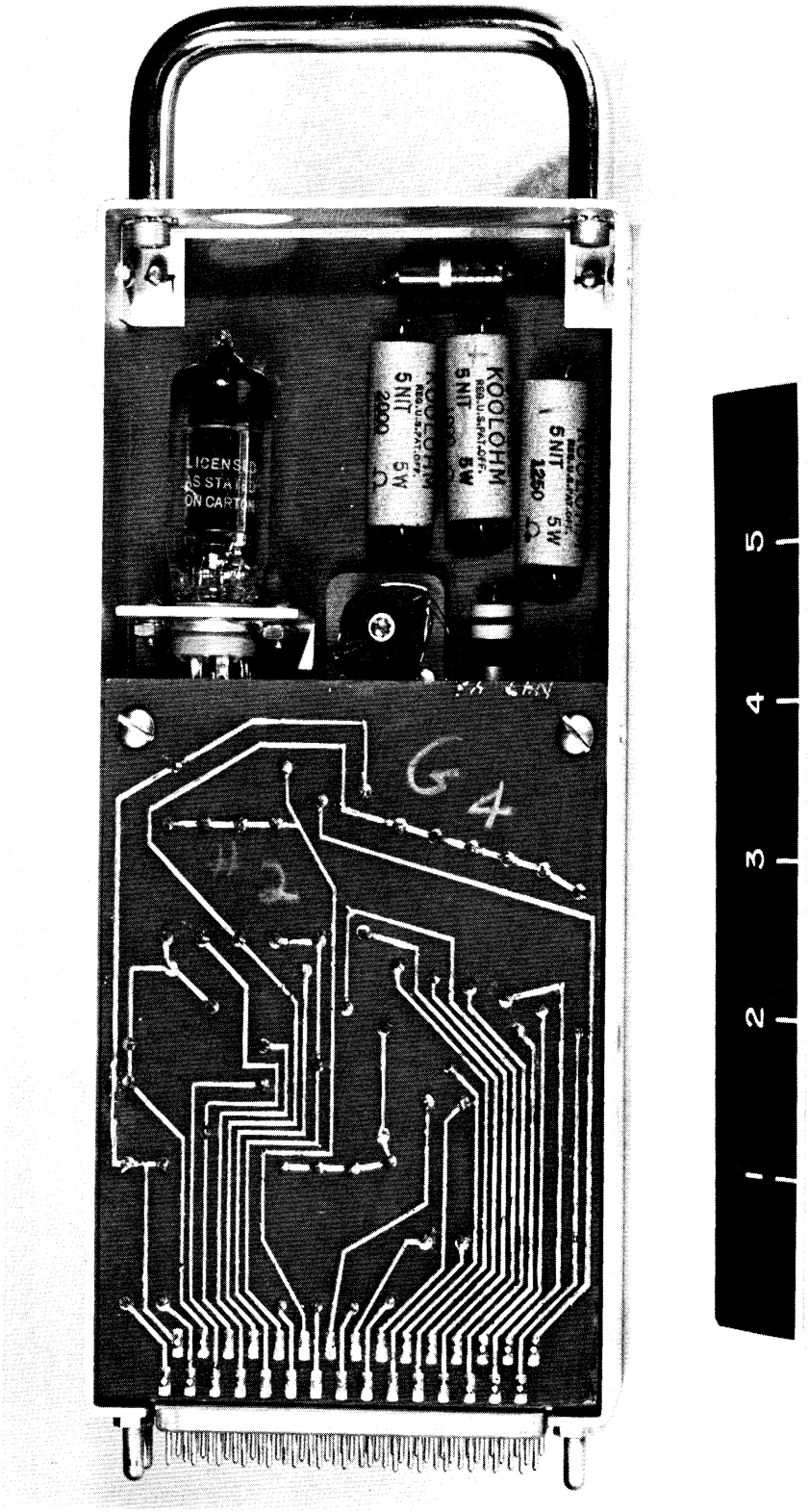


FIG. 4-8 ASSEMBLED, PRINTED CIRCUIT PACKAGE

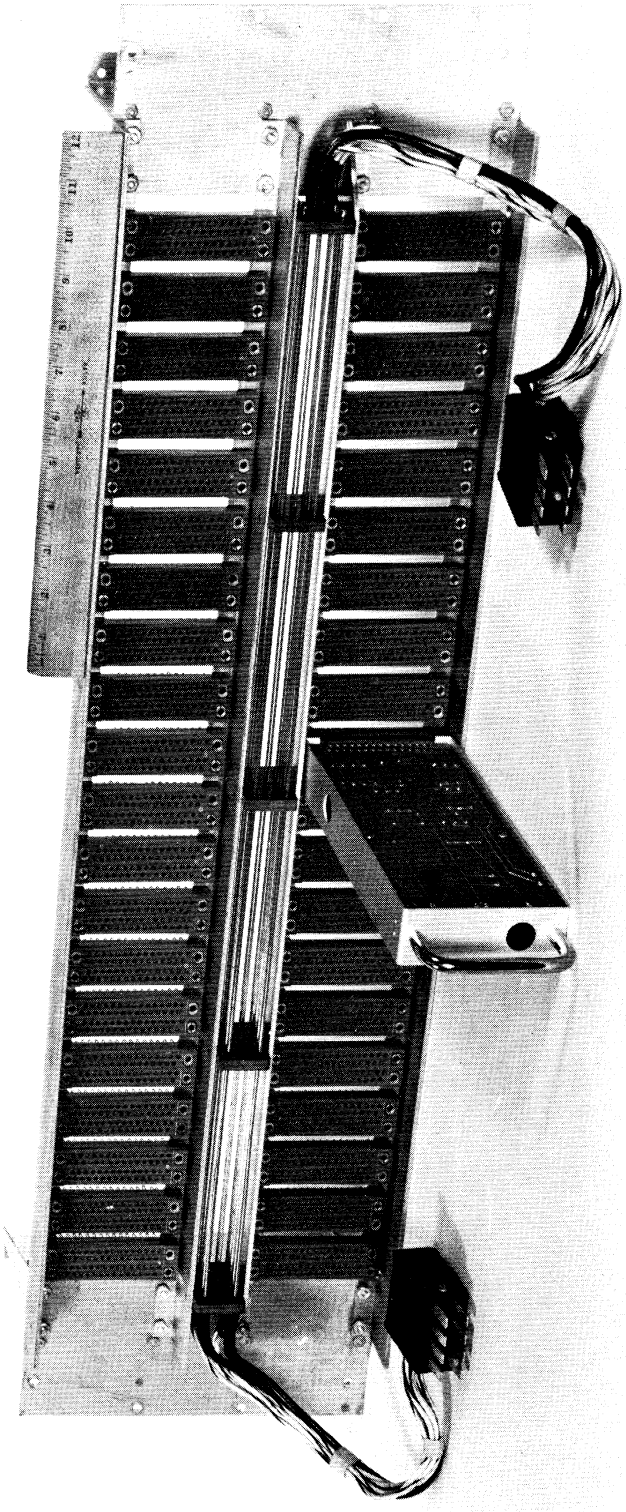


FIG. 4-9A IMPROVED CHASSIS (FRONT VIEW)

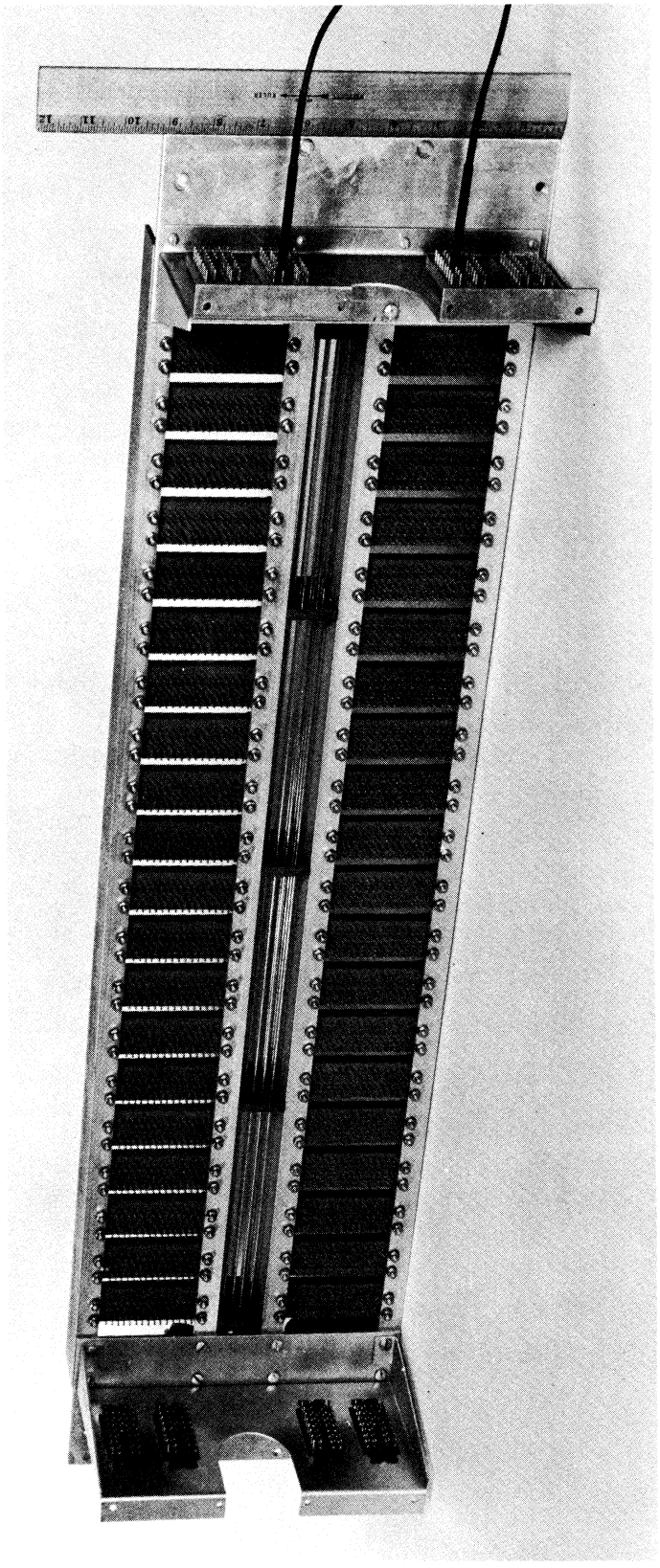


FIG. 4-9B IMPROVED CHASSIS (REAR VIEW)

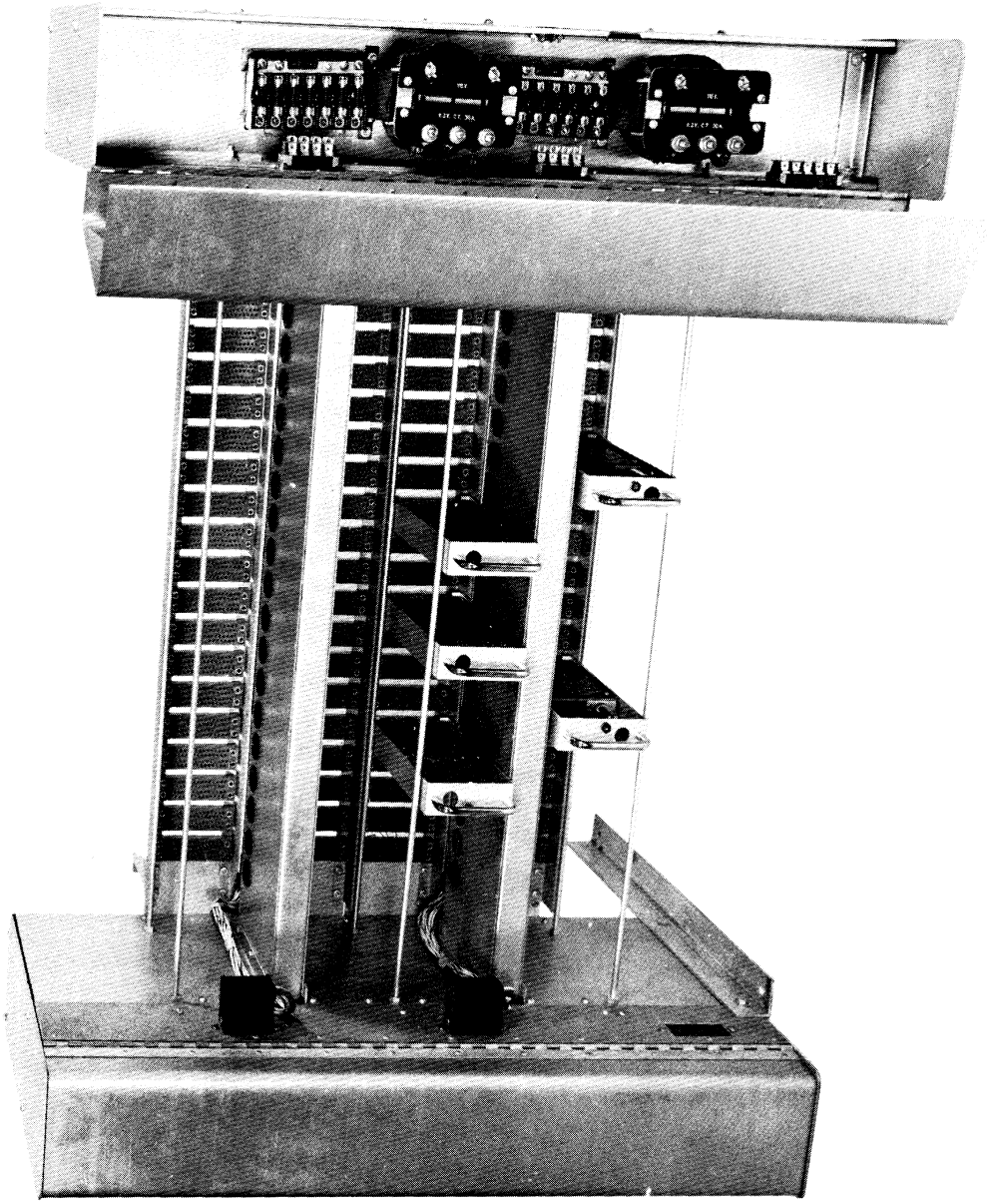


FIG. 4-10A MODEL SHOWING IMPROVED RACK CONSTRUCTION (FRONT VIEW)

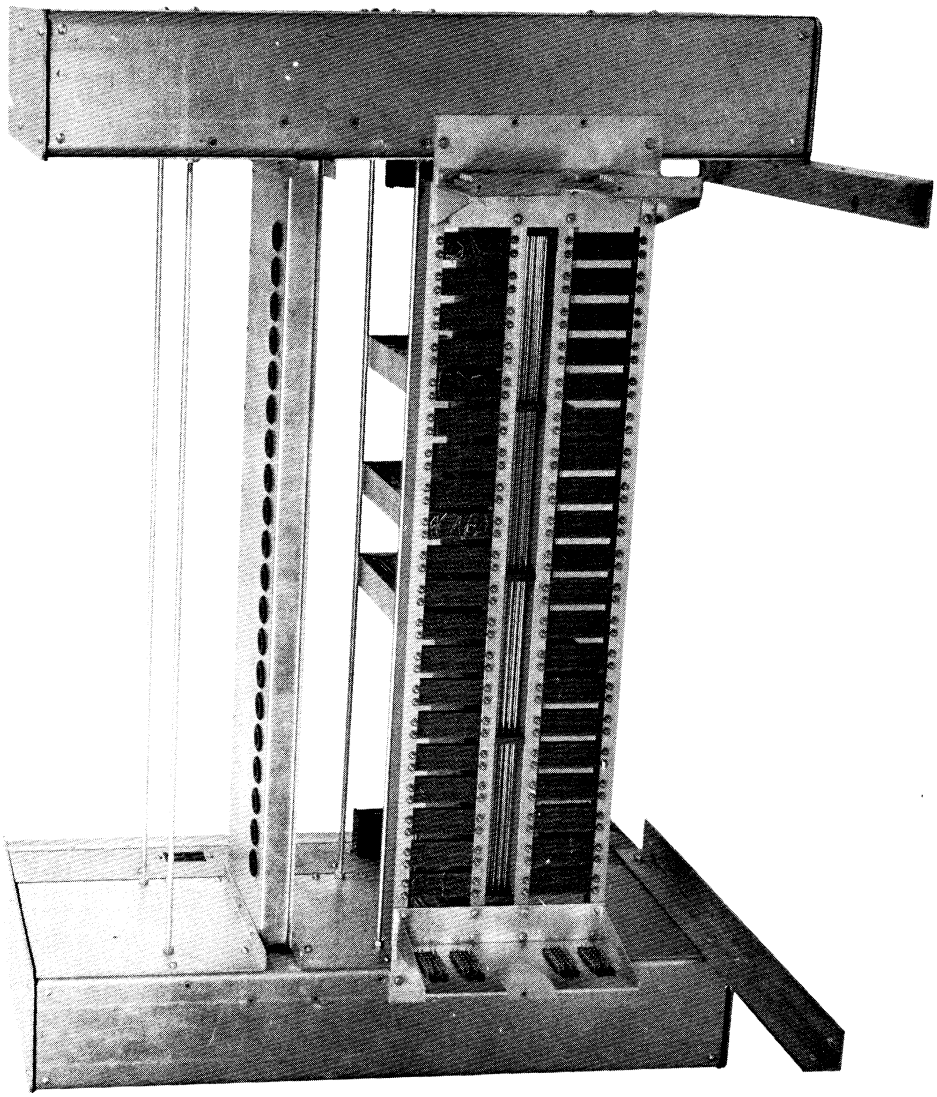


FIG. 4-10B MODEL SHOWING IMPROVED RACK CONSTRUCTION
(REAR VIEW)

APPENDIX A

RULES AND DATA FOR USING PACKAGES

A.1 GENERAL RULES

a. The path of a pulse is through the following elements in sequence: first-level or-gate, logical delay element, and-gate, second-level or-gate, pulse amplifier, another first-level or-gate, another logical delay element, etc. Any logical delay element can be omitted. The possible physical locations of first-level or-gates are given in Table A-1.

b. Signal wires connected to the output of an amplifier may be as long as 50 feet; all other wires should be kept short.

c. When a pulse passes from an amplifier clocked with CP_r (r = 1, 2, 3, or 4) to another amplifier clocked with CP_s (s = 1, 2, 3, or 4), the relationship between clock phases r and s is given by

$$s = (r + d + 1) \text{ modulo } 4,$$

where d is the logical delay between packages, measured in quarter-microseconds.

A.2 PACKAGE DATA

Tables A-2 through A-7 give additional data on the use of packages, including pin numbers.

TABLE A-1

PHYSICAL LOCATIONS OF FIRST-LEVEL OR-GATES

Signal Polarity	Used to Drive	Number of Or-Inputs	Possible Location of First-Level Or-Gate
Positive	One or Many And-Gates	One	Amplifier output B, or positive termination connected to amplifier output A.
		Many	R package connected to amplifier output A, or positive termination augmented by free diodes connect to amplifier output A.
	Single Delay Line	One	Positive termination connected to amplifier output A.
		Many	Positive termination augmented by free diodes connected to amplifier output A.
Negative	Single Delay Line	One	Negative termination connected to amplifier output C.
		Many	Negative termination augmented by free diodes connected to amplifier output C.

TABLE A-2

OUTPUT CAPABILITY IN EQUIVALENT-GATE DRIVES

Terminal Output	No Penthouse	P_1	P_2
Pin 18 (positive pulse through degenerate or-gate)	4	10	16
Pins 14 (direct positive pulse) and 15 (negative), or pins 14 and 23 (double-amplitude positive pulse).	12	6	0

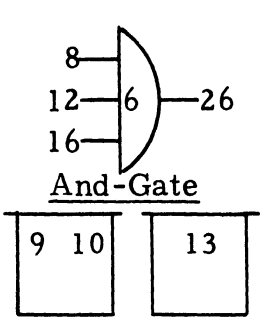
Notes:

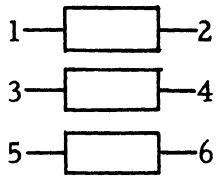
1. For negative output, pin 23 is connected to +4v.
2. For double-amplitude output, pin 14 is connected to pin 15 to obtain series-aiding transformer connection.

1947-2-T

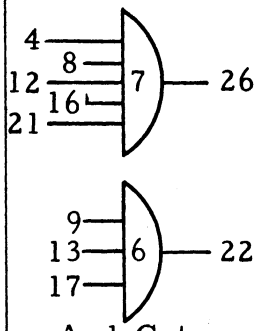
TABLE A-3

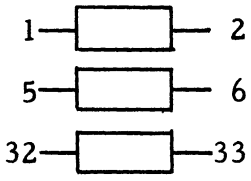
CONTENTS AND PIN CONNECTIONS OF AND-GATE PACKAGES



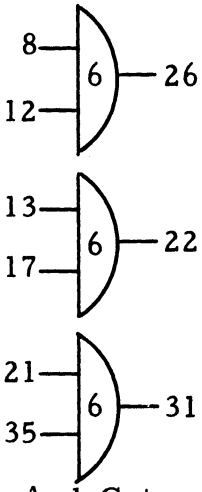


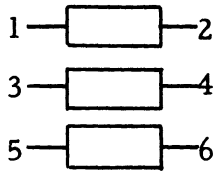
"A" Package (Red Frame)



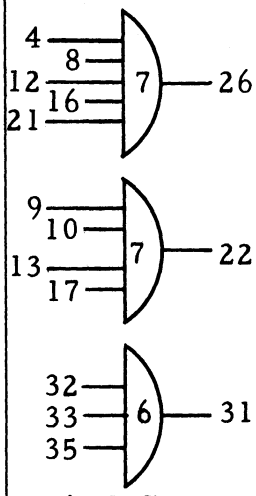


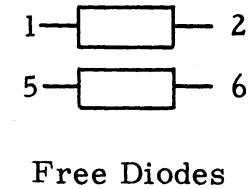
"C" Package (Yellow Frame)



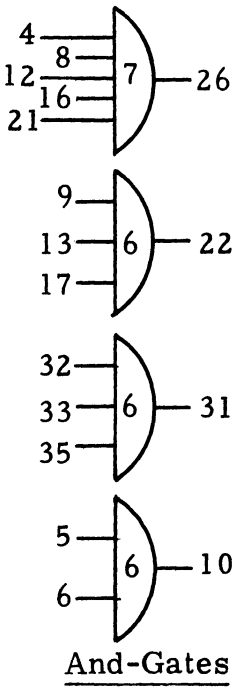


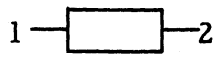
"D" Package (Green Frame)





"E" Package (Blue Frame)





"F" Package (Violet Frame)

Notes:

1. Number inside gate is maximum number of inputs allowed on gate.
2. High pin number of free diode is always the anode.
3. To add an input to a gate, connect anode of diode to gate output.
4. On each package type, the clock voltage is connected to pin 25.

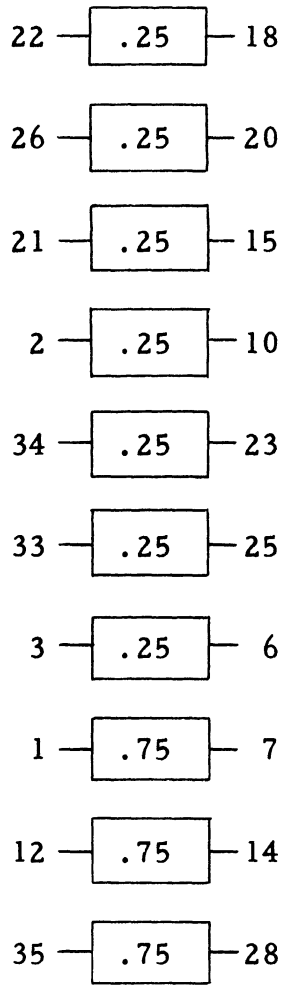
TABLE A-4

POWER CONNECTIONS TO GATE-AMPLIFIER PACKAGE

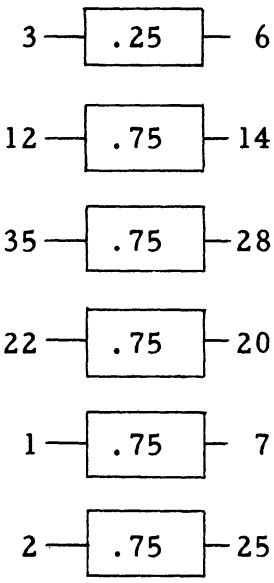
Pin	Voltage
7	-8v
11	+62v
19	+235v
20	-10v
24	6.3v ac
28	+2v
29	Ground
30	-65v
34	-5v

TABLE A-5

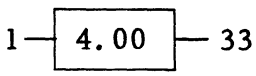
CONTENTS AND PIN CONNECTIONS OF DELAY LINE PACKAGES



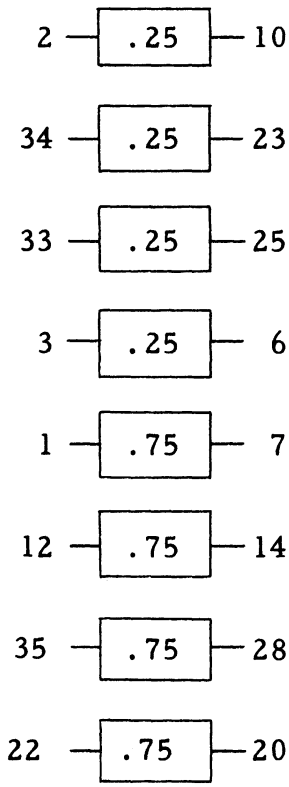
L_1 Package



L_2 Package



L_4 Package



L_3 Package

Notes:

1. Ground to pins 5 and 31.
2. Delay units expressed in microseconds.
3. Delay packages have green frames.

TABLE A-6

CONTENTS AND PIN CONNECTIONS OF TERMINATION PACKAGES

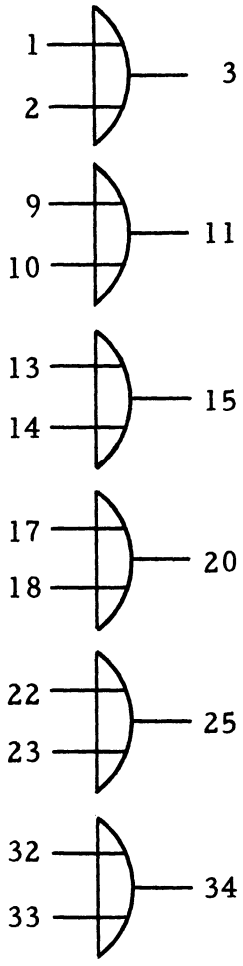
a	b	c	Polarity of Termination T_1 Package	Polarity of Termination T_2 Package
1	2	5	P	P
4	3	8	P	P
9	10	13	P	P
12	11	16	P	P
17	14	22	P	P
21	15	26	P	N
27	18	32	P	N
31	20	35	P	N
33	29	19	N	N
34	24	25	N	N

Power Connections
Ground to pin 6
-8v to pin 7
+2v to pin 28
-65v to pin 30

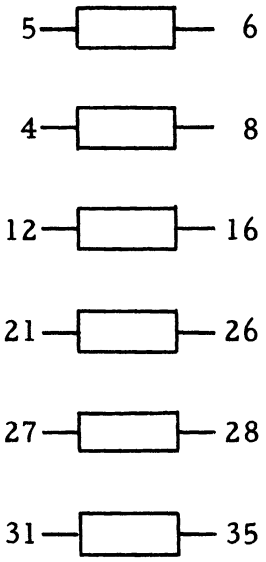
Notes:
1. Termination packages have red frames.
2. Signal input goes to pin a; delay line is connected between pins b and c; and the delayed signal output appears at pin c.

TABLE A-7

CONTENTS AND PIN CONNECTIONS OF OR-GATE PACKAGE



Positive Or-Gates



Free Diodes

Power Connections

-8v to pin 7

Ground to pin 29

-65v to pin 30

Notes:

1. High pin number of free diode is always the anode.
2. Or-gate packages have silver-colored frames.

APPENDIX B

SOME DESIGN FACTORS AND EFFECTS OF COMPONENT TOLERANCES

B.1 DIODE GATE DESIGN PROCEDURE

The diode gate structure is shown in Figure B-1.

The first-order design procedure for the diode gates made use of the following assumptions:

1. The grid swing desired on the 6AN5-tube is from -5v to +2v.
2. Diodes have zero forward resistance and a lowest permissible back resistance of 90,000 ohms.
3. The minimum tolerable rate of potential rise and fall at the grid of the tube is 75 volts per microsecond.
4. Because of diode manufacturers' ratings, the maximum power supply voltages for diode returns are in the neighborhood of 65 volts. Values of +62v and -65v were chosen.
5. Unwanted signals at the output of an and-gate should not exceed 3 volts.

The design procedure first required that the stray capacitances C_1 and C_2 be measured using the actual circuit structure. These were found to be 18 micromicrofarads and 19 micromicrofarads respectively.

B.1.1 Calculation of R_1

Assume that the tube has been pulsed and that the input voltages to the or-gate are then removed at a rate in excess of 75 volts per microsecond. The required minimum rate of discharge of C_1 must be 75 volts per microsecond. The rate will be minimum as the grid approaches -5v, with R_1 at its maximum value (105 per cent of nominal), and the negative supply voltage, E_1, at its minimum value (95 per cent of nominal).

$$75 \times 10^6 \ \frac{\text{volts}}{\text{sec}} = \frac{(0.95)\,E_1 - (5)}{(1.05)\,R_1 C_1}$$

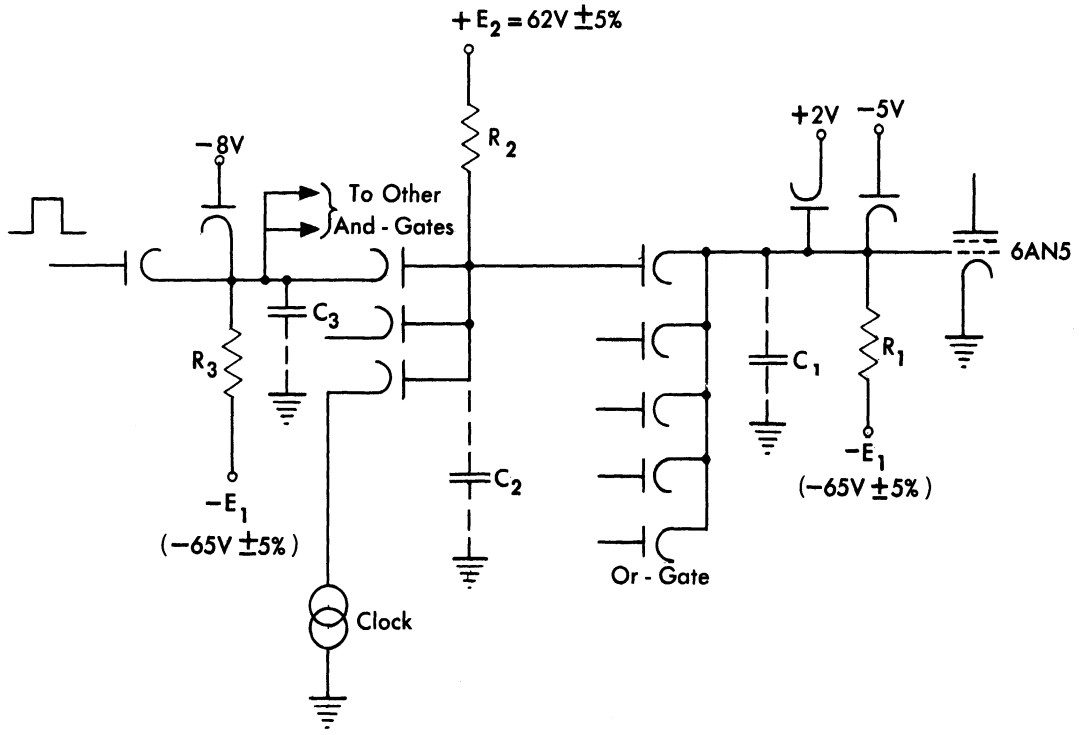


FIG. B-1 DIODE GATE STRUCTURE

Substitution of numerical values for E_1 and C_1 gives R_1 = 40,000 ohms. The nearest standard resistor value is 39,000 ohms.

B.1.2 Calculation of R_2

Assume that the inputs to the and-gate are elevated at a rate greater than 75 volts per microsecond. The minimum rate of charging of C_1 and C_2 must be 75 volts per microsecond. This minimum rate will occur as the grid signal approaches +2v and when:

1. E_2 is at its minimum value (95 per cent of nominal),
2. R_2 is at its maximum value (105 per cent of nominal),
3. E_1 is at its maximum value (105 per cent of nominal), and
4. R_1 is at its minimum value (95 per cent of nominal).
5. Only one diode is conducting, the remaining four being cut off.

The value of R_2 is given by:

$$75 \times 10^6 = \frac{I}{C_1 + C_2} ,$$

where,
$$I = \frac{(0.95)E_2 - (2)}{(1.05)R_2} - \frac{(1.05)|E_1| + (2)}{(0.95)R_1} - \frac{10}{R_b'} ,$$

R_b' being the back resistance of four or-gate diodes in parallel. Substituting numerical values gives R_2 = 10,600 ohms. The nearest standard resistor value is 11,000 ohms.

B.1.3 Calculation of R_3

The capacitance C_3 consists of the shunt wiring capacitance at the output of an amplifier package. The value of C_3 depends upon the number of circuits a given amplifier is driving and the length of wire used to make the connections. Because the capacitance load is variable, it is impossible to choose a single fixed value for R_3. In designing the packages, it was found that two additional values of R_3 could be provided

through the use of the standard plug-in penthouse packages. This variety of values accommodates the necessary range of output loads.

B.2 EFFECT OF NON-IDEAL DIODE CHARACTERISTICS

Several factors tend to compromise the ideal operation of the gates.

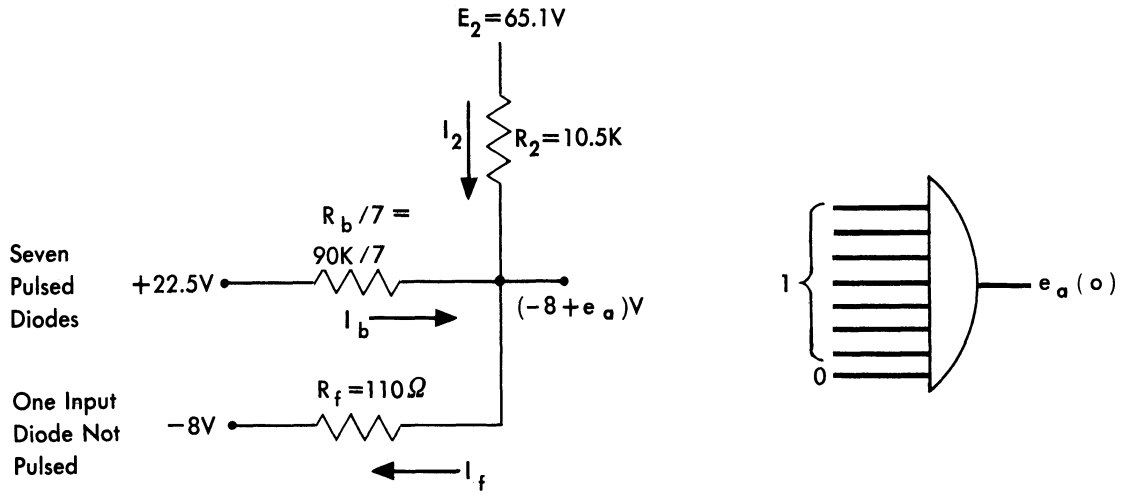
The non-zero forward impedance of diodes causes unwanted signals to appear at the output of an and-gate.

The situation which is most critical exists when one input alone must keep the gate inoperative. The equivalent circuit for this condition is shown in Figure B-2(a). It is assumed that all circuit parameters are at their maximum values in the direction which produces the largest leakage signal. These are:

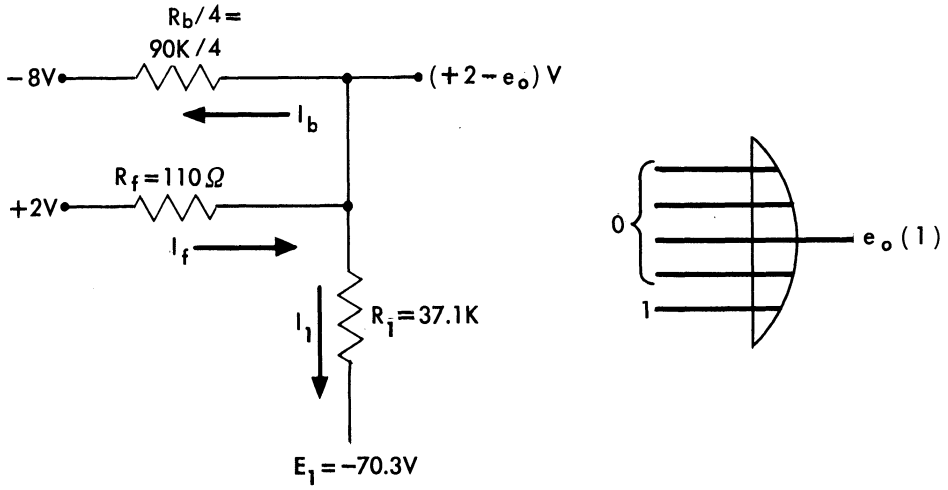
1. Maximum leakage current from input diodes:
   a. Maximum number of input diodes (8),
   b. All inputs except one at the most positive voltage level, (+22.5v),
   c. All input diodes at their minimum allowable back resistance (90K).
2. Maximum pull-up current:
   a. Pull-up resistor at its minimum allowable value (10.5K),
   b. Pull-up voltage at its maximum allowable positive value (65.1v).
3. Maximum allowable forward resistance for the conducting diode (110Ω).

The leakage signal amplitude, e_a, measured from the -8v input level, is equal to the voltage drop across the conducting diode due to the leakage current I_b and the gating current I_2.

$$I_b = \frac{22.5 + (8-e_a)}{\frac{R_b}{7}} = \frac{30.5 - e_a}{13000} = \left(2.3 - \frac{e_a}{13}\right) \text{ milliamperes}$$



(a) EQUIVALENT CIRCUIT OF 8-INPUT AND-GATE.
(ALL CIRCUIT PARAMETERS ARE AT THEIR EXTREME VALUES, IN THE DIRECTION WHICH ALLOWS THE LARGEST LEAKAGE SIGNAL e_a)



(b) EQUIVALENT CIRCUIT OF 5-INPUT OR-GATE.
(ALL CIRCUIT PARAMETERS ARE AT THEIR EXTREME VALUES, IN THE DIRECTION WHICH CAUSES THE LARGEST REDUCTION e_o)

FIG. B-2 EQUIVALENT CIRCUITS FOR CALCULATION OF LEAKAGE SIGNALS

$$I_2 = \frac{65.1 + (8 - e_a)}{R_2} = \frac{73.1 - e_a}{10500} = \left(7.0 - \frac{e_a}{10.5}\right) \text{ milliamperes}$$

$$e_a = (I_2 + I_b) R_f = (9.3 - 0.2\, e_a)\, 110 \cdot 10^{-3} \text{ volts} = 1.0\text{v}.$$

Thus the maximum d-c leakage signal of an and-gate is about one volt.

Under pulse conditions the transient response of the pulsed diodes may increase the leakage signal slightly, since the combined R_b of the pulsed diodes tends to remain low for a short period of time. However, the signal lines are always pulsed well before the clock pulse occurs. Thus, by the time the clock diode is pulsed, the back resistance of the signal diodes has had a chance to approach its d-c value. In addition, the assumed maximum +22.5v level at a pulsed input line is characteristic of only the clock input line while the average information pulse has a maximum level of +10v.

Non-ideal diodes in the or-gate may reduce the amplitude of a signal at the grid. The worst case exists when only one input diode is pulsed; this situation is shown in Figure B-2(b). The circuit parameters which make this effect most pronounced are:

1. Maximum leakage current drawn by the "off" diodes:
    a. Maximum number of off diodes (4),
    b. All off inputs at their most negative level (-8v),
    c. All off diodes at their minimum allowable back resistance (90K).
2. Maximum pull-down current:
    a. Pull-down resistor at its minimum allowable value (37.1K),
    b. Pull-down voltage at its most negative value (-70.3v).
3. Maximum allowable forward resistance of the pulsed diode (110 Ω).

The reduction e_o of the output signal amplitude from the +2v-input level is equal to the voltage drop across the conducting diode.

$$I_b = \frac{-8 - \left(2 - |e_o|\right)}{R_b/4} = \frac{-10 + |e_o|}{22,500} = \left(-0.45 + \frac{|e_o|}{22.5}\right) \text{ milliamperes}$$

$$I_1 = \frac{-70.3 - \left(2 - |e_o|\right)}{R_1} = \frac{-72.3 + |e_o|}{37,100} = \left(-1.95 + \frac{|e_o|}{37.1}\right) \text{ milliamperes}$$

$$e_o = (I_b + I_1) R_f = -\left[2.4 - |e_o| \left(\frac{1}{22.5} + \frac{1}{37.1}\right)\right] 110 \cdot 10^{-3} \text{ volts}$$

$$e_o = -0.26\text{v.}$$

This drop in signal level is not significant since the grid is driven back to +2v when the regeneration gate is pulsed.

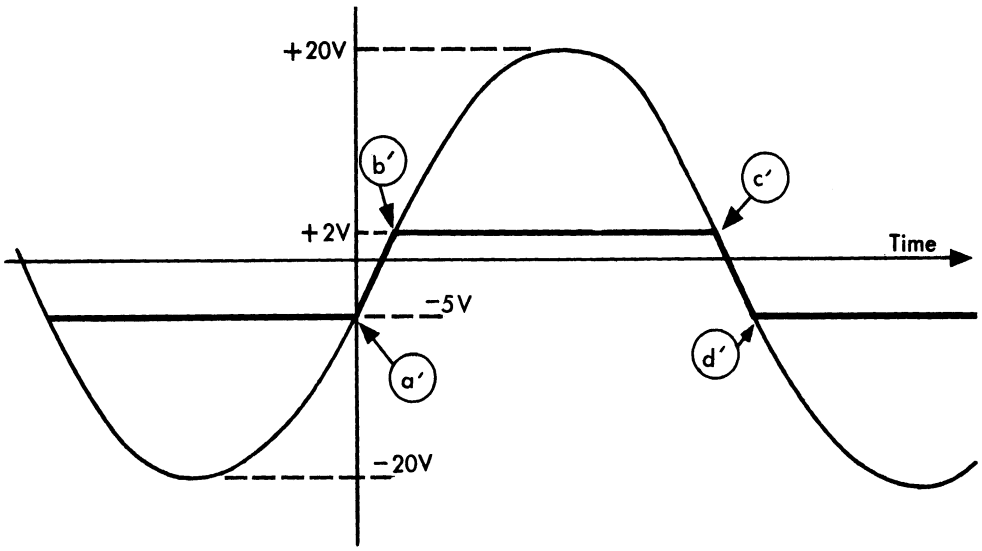
The leakage current through the -5v bumper diode has not been included in the above calculations because it is several orders of magnitude smaller than the other currents involved.

B.3 LABORATORY MEASUREMENT OF EFFECT OF COMPONENT TOLERANCES

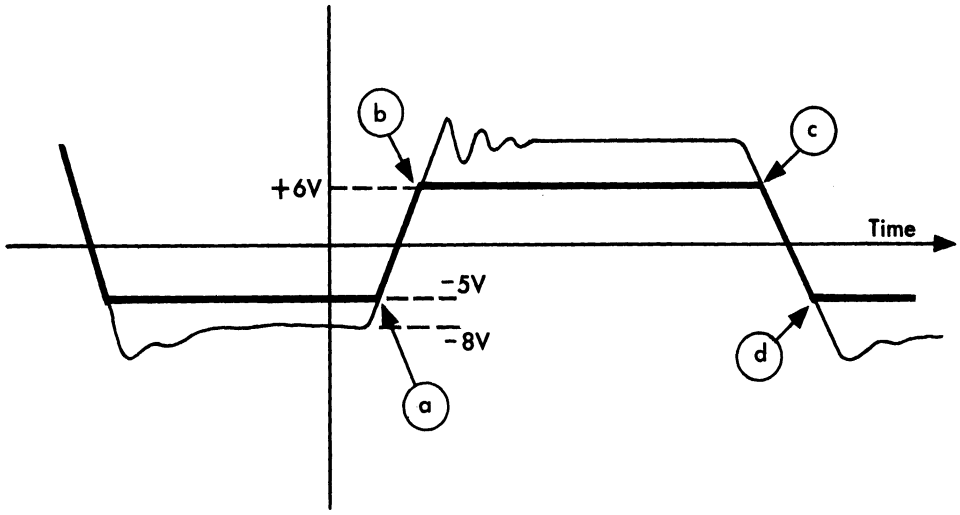
B.3.1 Timing Numbers

To provide a basis for measuring the effects of combinations of circuit tolerances, a notation has been devised to express precisely the relative shape and timing of computer pulses. This notation makes use of four critical points on a voltage pulse -- two define the leading edge, and two define the trailing edge, as shown in Figure B-3.

For this purpose, time is conveniently measured in hundredths of microseconds. The first timing point of a clock-pulse of phase one (CP_1) is arbitrarily chosen as time zero. The four numbers which specify the timing points of any pulse are called the timing numbers and are



LOCATIONS OF TIMING POINTS ON CLOCK "PULSE"



LOCATIONS OF TIMING POINTS ON AMPLIFIER PULSE

FIG. B-3 TIMING POINTS

written in a block of two lines and two columns. The timing numbers for each of the four clock phases are as shown in Table B-1.

TABLE B-1

TIMING NUMBERS OF CLOCK PULSES

	CP_1	CP_2	CP_3	CP_4
b' | c' / a' | d'	6 | 53 / 0 | 59	31 | 78 / 25 | 84	56 | 103 / 50 | 109	81 | 128 / 75 | 134

A circuit which delays and distorts a pulse can be described in terms of an operator consisting of four numbers in a bracket:

$$\left[\begin{array}{c|c} b & c \\ \hline a & d \end{array}\right]$$

When this operator is applied to the timing numbers of the circuit input pulse, the result is the timing numbers of the output pulse:

$$\begin{array}{c|c} b' & c' \\ \hline a' & d' \end{array} \left[\begin{array}{c|c} b & c \\ \hline a & d \end{array}\right] = \begin{array}{c|c} b'+b & c'+c \\ \hline a'+a & d'+d \end{array}$$

B.3.2 Rules of Coincidence

A pulse at the input of an and-gate is said to be coincident with the clock pulse at this and-gate if it obeys the following four rules:

Rule 1. An input pulse must not occur so early as to gate with the last part of the previous clock pulse. Specifically, it must not rise above -8v while the previous clock pulse is above -5v.

Rule 2. The input pulse must be at full gating voltage (+2v) before the clock pulse reaches this voltage, so that the input pulse always encompasses the leading edge of the clock pulse.

Rule 3. The regeneration gate must be activated for at least 0.05 microseconds before an input pulse ceases. Therefore, the input cannot be allowed below +2v before the package output has been at or above this level for .05 microseconds.

Of course the input pulse must not last so long that it gates with the clock pulse following the one with which it is intended to coincide. However, this is a trivial statement, since normal information pulses are always much less than 1 microsecond.

If it were not for the regeneration loop, the output pulse of a tube package would be a pulse which has a duration only as long as the longest time of coincidence at any one of the and-gates. Since Rule 2 states that input pulses always occur before the clock pulse with which they are gated, then the time of coincidence is always less than the duration of a clock pulse. The regeneration loop stretches the output pulse, so that it lasts as long as the clock pulse. This loop consists of a two-input and-gate which has a clock pulse as one input and the output of the package as the other. Once this gate is activated (Rule 3), the duration of the output pulse is controlled by the clock pulse, and is independent of the conditions present at the other and-gate inputs. Thus a full length output pulse from the package is guaranteed.

Rule 4. The output pulse must not last so long as to gate with the next clock pulse. Therefore, the output voltage must be below -8v before the clock pulse goes above this value.

B.3.3 Rules of Inhibition

The previous discussion has been concerned with positive pulses only. A negative pulse is used to inhibit an and-gate. The base line of this pulse is at +4v. Complete inhibition of an and-gate requires that the negative inhibit pulse completely encompass any coincidence event. Four timing rules apply to the inhibition of and-gates.

Rule 1. The inhibit pulse must not occur so early as to interfere with the previous clock pulse. Specifically, it must not fall below +2v while the previous clock pulse is above -5v.

Rule 2. The inhibit pulse must be below -5v before the clock pulse rises above this level.

Rule 3. The inhibit pulse must remain below -5v for the total duration of the clock pulse.

Rule 4. A delayed inhibit pulse must not inhibit part of the clock pulse following the one to be inhibited. Specifically, the delayed inhibit pulse must be more positive than +2v by the time the next clock pulse reaches -5v.

B.3.4 Worst Timing Numbers

The eight rules stated in the two previous sections represent a set of conditions which, when obeyed, result in the proper operation of the gate-amplifier package. The obedience of a circuit to the above rules may be checked by means of the timing numbers previously defined.

A useful concept is a set of numbers which, when added to the timing numbers of a clock pulse, represents the "worst" possible timing configuration. The worst timing is that which comes nearest to violating the timing rules in any gating configuration. The worst timing condition must be found by experiments in which a great many circuits parameters are allowed to vary within stated tolerances. The worst timing numbers of a package output pulse have been found to be:

b' + 14	c' + 1
a' + 6	d' + 8

For example, the worst timing numbers of an output pulse of a package which is clocked with CP_1 are:

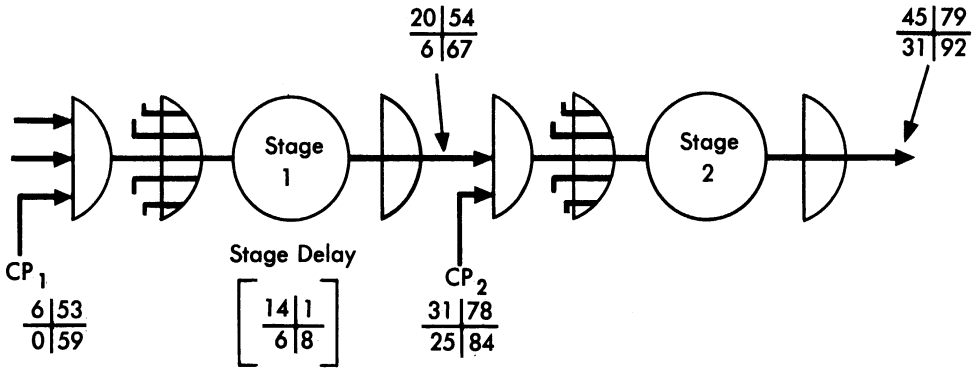
$$\begin{array}{|c|c|} \hline b & c \\ \hline a & d \\ \hline \end{array} = \begin{array}{|c|c|} \hline 20 & 54 \\ \hline 6 & 67 \\ \hline \end{array}$$

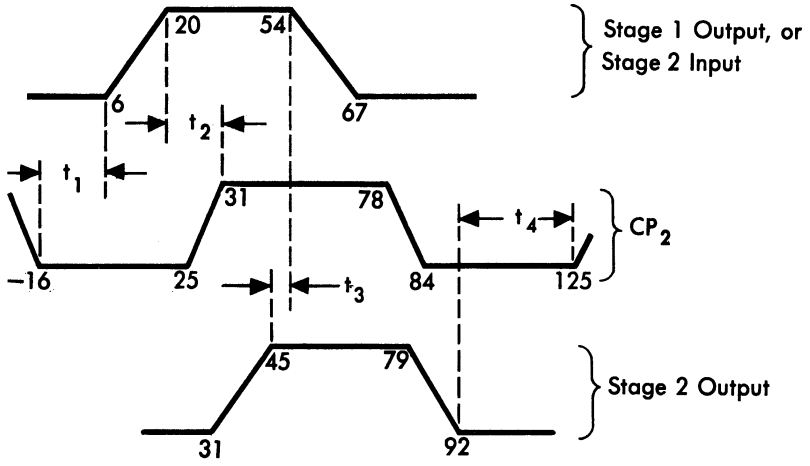
The use of the four clock phases is now apparent. If only one clock phase were available, the output of a package would have to be delayed on the order of .75 microsecond so that it could properly gate a following and-circuit. However, if the second and-circuit is clocked with

CP_2, no external delay is required and the four timing rules of coincidence are obeyed. This is illustrated in Figure B-4. The conformance to the appropriate timing rules is determined by the timing tolerances t_1, t_2, t_3, t_4 given in the figure. The subscript of a timing tolerance indicates the number of the applicable rule of inhibition or coincidence. If any timing tolerance becomes zero or negative, a rule has been violated. Two additional examples of timing numbers are given in Figures B-5 and B-6, which show two methods of inhibition.

Nine parameters were varied to obtain the worst timing numbers. These parameters were:

1. Clock pulse amplitude:
   a. "Fast" clock - maximum amplitude - 45v peak to peak,
   b. "Slow" clock - minimum amplitude - 30v peak to peak.
2. Capacitive load (after output buffer):
   a. Maximum - 300 uuf,
   b. Minimum - no external capacity.
3. Resistive load:
   a. Maximum - P_2 penthouse,
   b. Minimum - no penthouse.
4. Grid pull-down current:
   a. Minimum - pull-down resistance 5 per cent high and pull-down voltage 5 per cent less negative than design center,
   b. Maximum - pull-down resistance 5 per cent low and pull-down voltage 5 per cent more negative than design center.
5. Number of and-gates used:
   a. Minimum - 1,
   b. Maximum - 4.
6. Speed of and-gate:
   a. Slow - seven-input and-gate representing maximum capacity

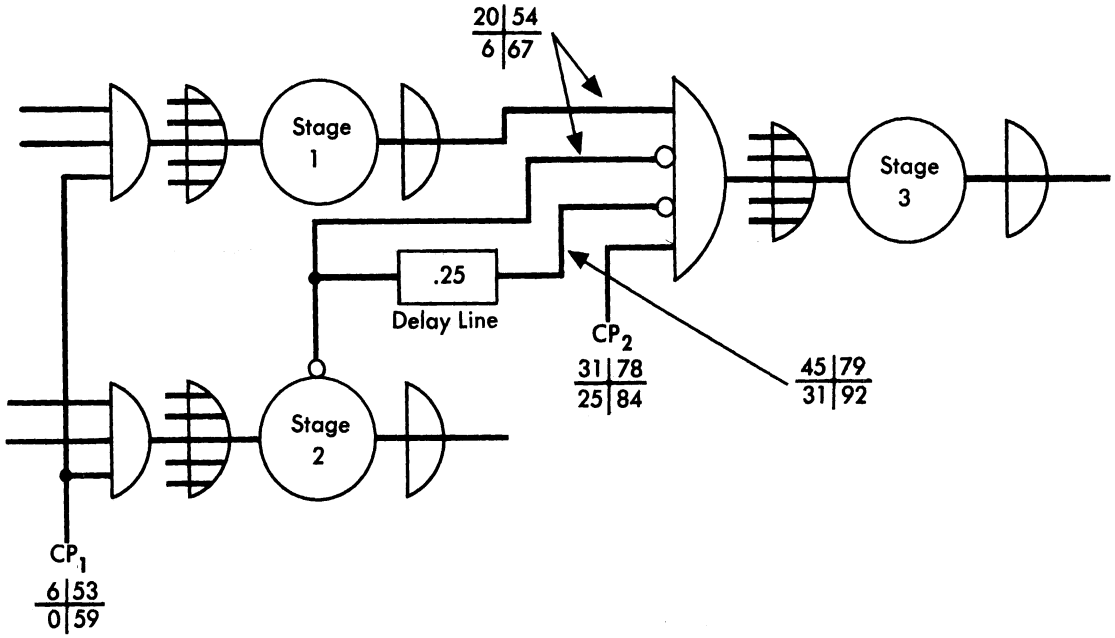


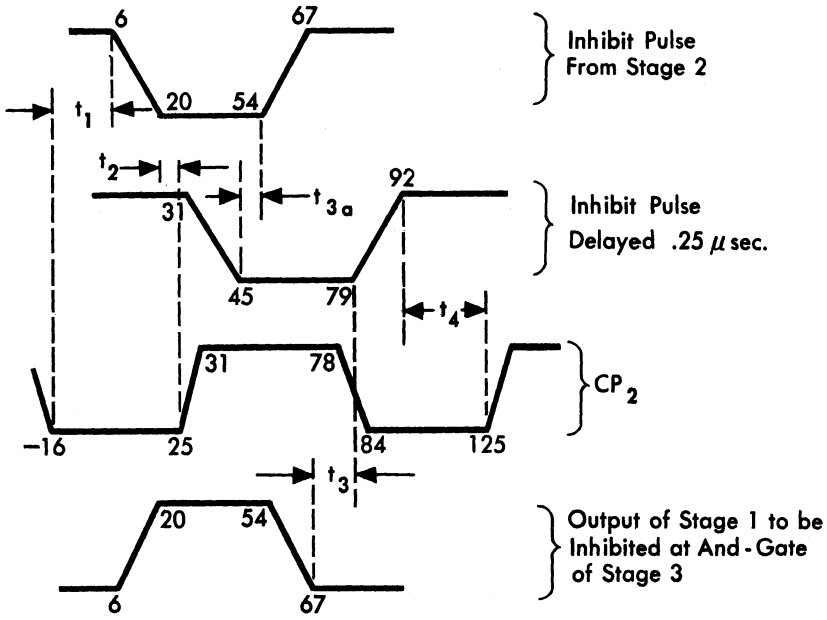


The Output Pulse of Stage 1 is shown to be coincident with CP_2 in accordance with the 4 Rules of Timing. The Timing Tolerances for this configuration are:

$$t_1=22,\ t_2=11,\ t_3=9,\ t_4=32.$$

FIG. B-4 TIMING OF POSITIVE PULSES

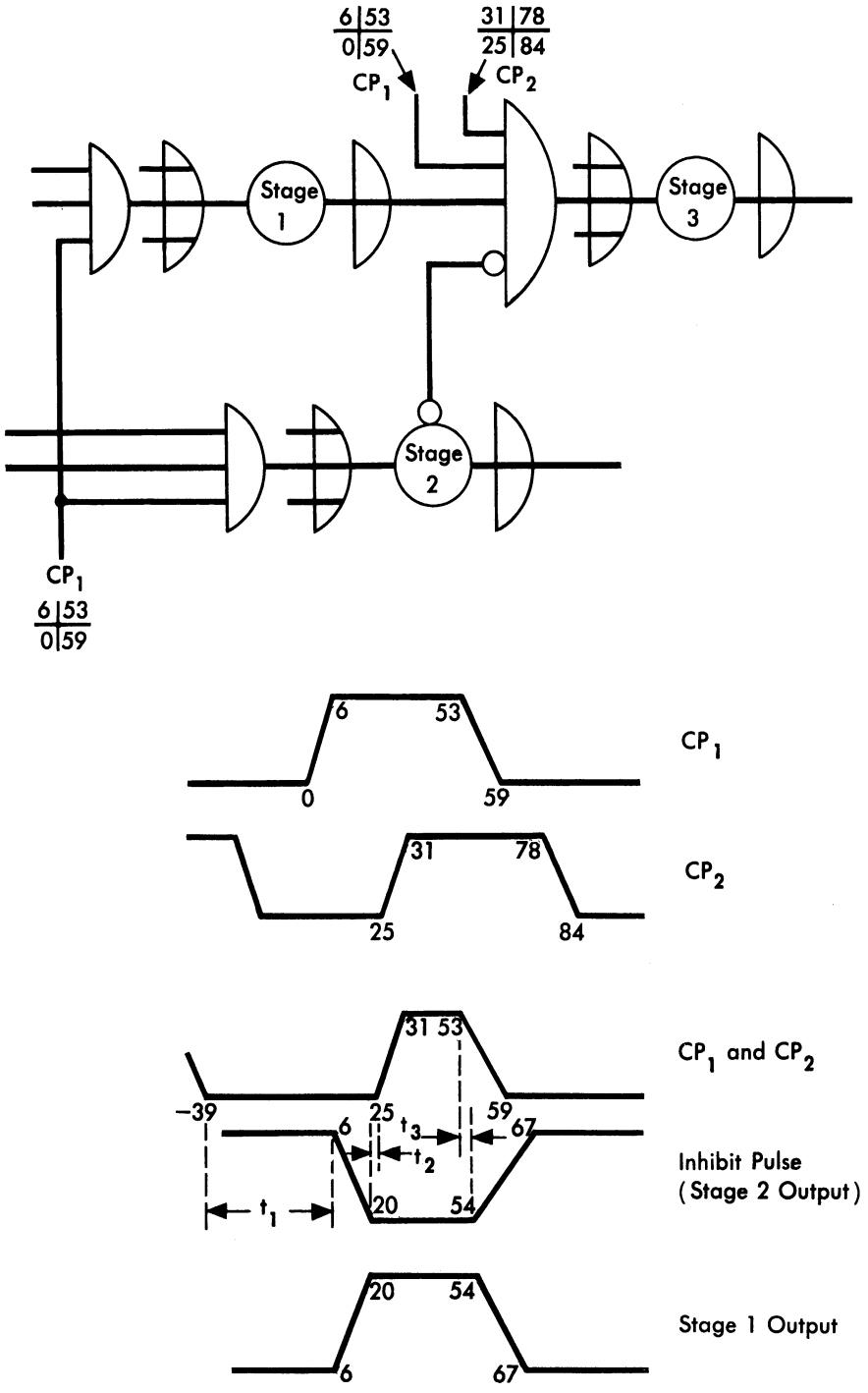




The And-Gate of Stage 3 is inhibited by the pulse from Stage 2.
The Timing Tolerances are:

$$t_1 = 22,\ t_2 = 5,\ t_3 = 12,\ t_{3a} = 9,\ t_4 = 33$$

FIG. B-5 INHIBITION BY PULSE STRETCHING



Stage 3 is Inhibited by Stage 2. The Timing Tolerances are:

$t_1 = 45$, $t_2 = 5$, $t_3 * = 1$

$*t_3$ cannot become Zero or Negative, because a "Cause" must always precede an "Effect".

FIG. B-6 INHIBITION BY CLOCK PULSE SHORTENING

C2, pull-up resistor 5 per cent high and pull-up voltage 5 per cent less positive than design center,

b. Fast - one-input and-gate representing minimum C2, pull-up resistor 5 per cent low and pull-up voltage 5 per cent more positive than design center.

7. Tube:

   a. Hot tube - draws more than 75 ma of plate current with +2v on grid, +62v on screen and plate, 5.7v on filaments.

8. Pulse transformer primary inductance:

   a. High - 4.5 millihenries,

   b. Low - 3.0 millihenries.

9. Pulse condition:

   a. First pulse - an output pulse every 4 microseconds,

   b. Nth pulse - a continuous train of pulses.

The combination of parameters which by experiment had the greatest effect on specific timing members are given below in order of their importance.

1. Parameters giving smallest Δa (.06 microsecond):

   a. First pulse

   b. Minimum capacitive load

   c. Minimum resistive load

   d. Four pulsed and-gates

   e. Slow clock

   f. High inductance (small effect)

   g. Hot tube

   h. Fast grid pull-down (negligible effect)

2. Parameters giving largest Δb (0.14 microsecond):
   a. Maximum capacitive load (very large effect)
   b. Nth pulse (large effect)
   c. Maximum resistive load
   d. One pulsed and-gate; seven-input
   e. High inductance (small effect)
   f. Cold tube
   g. Fast clock
   h. Fast grid pull-down (negligible effect)
3. Parameters giving smallest Δc (0.01 microsecond):
   a. Cold tube (large effect)
   b. Low inductance
   c. First pulse
   d. Maximum resistive load (small effect)
   e. Maximum capacitive load (very small effect)
   f. Four pulsed and-gates (negligible effect)
   g. Fast grid pull-down
   h. Clock amplitude (no effect)
4. Parameters giving largest Δd (0.08 microsecond):
   a. Maximum capacitive load (large effect)
   b. Hot tube
   c. One pulsed and-gate; seven-input
   d. Minimum resistive load
   e. Slow grid pull-down
   f. Nth pulse (no effect)
   g. Inductance (no effect)
   h. Clock amplitude (no effect)

REFERENCES

Number	Title
1.	UMM-101, "MIDAC - Automatic Computer", University of Michigan, Willow Run Research Center (June 1953).
2.	WRRC-13-T, "The MIDAC Computer", University of Michigan, Willow Run Research Center (to be published).
3.	WRRC-14-T, "A Programming and Operating Manual for MIDAC", by J.W. Carr, University of Michigan, Willow Run Research Center (to be published).
4.	1947-3-T, "The MIDSAC Computer", by W.G. Brown, J.E. DeTurk, H.L. Garner, and E.M. Lewis, University of Michigan, Willow Run Research Center (April 1954).
5.	"Dynamic Circuit Techniques Used in SEAC and DYSEAC" by R.D. Elbourn and R.P. Witt, Proc. of the IRE, Vol. 41, No. 10 (October 1953).

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