THE DEVELOPMENT AND CHARACTERIZATION OF SELF-PACKAGES USING MICROMACHINING TECHNIQUES FOR HIGH FREQUENCY CIRCUIT APPLICATIONS

by

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The Serenity Prayer

God,
Grant me the Serenity
to Accept the Things that I cannot Change,
The Courage,
to Change the Things that I Can,
And the Wisdom to know the Difference.

Author Unknown

To my loving husband, Marcus
My inspiring parents, Elvin and Ann Franklin
and In memory of my grandmother, Yolande.

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PREFACE

This thesis presents with the development and characterization of a novel packaging structure that is realized for high frequency circuit applications using silicon micromachining techniques. This self-packaged topology results from the merger of two technologies, silicon micromachining and high frequency circuit design techniques used in microwave and millimeter wave applications. Extensions of the technology have been used to explore its potential to improve the performance of microstrip antennas, such as the rectangular patch, in order to provide an alternative means for reducing surface wave excitation in high index materials. The design, fabrication and testing procedures are discussed herein, and measured results are shown for representative planar circuits and antenna elements typically used in high frequency applications.

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CHAPTER I

INTRODUCTION

1.1 PACKAGING IN HIGH FREQUENCY APPLICATIONS

Since the 1950's, packaging has played an increasing important role in the advancement and direction of circuit designs in the electronics industry. Packaging for low frequency (LF) circuit applications have advanced significantly to accommodate high volume cost effective circuits used in commercial applications below 1 GHz. On the other hand, packaging for high frequency (HF) applications has experienced limited growth due to high performance, low volume design requirements. Electrical performance improvements are significantly impacted by the present limitations in HF package development. Processing technologies used to make LF circuits and design/analysis (D/A) techniques used in HF circuits can be combined to realize novel packaging concepts for planar monolithic and microwave integrated circuits (MICs and MMICs). At high frequencies, research on optimum device and component performance were given the highest priority. This resulted in the development of sophisticated D/A tools and an extensive circuit design library. In the last few years, packaging effects are now identified as one of the most important parameters affecting substantial performance improvements in many HF circuits.

Several packaging approaches have been implemented thus far in high frequency applications. Multi-function circuits and arrays use STRATEDGE^{TM} [1] and WAFFLE-LINE [3] for example to accommodate MIC and MMIC designs. Quartz hermetic pack-

ages have been successfully developed for multi-chip-modules (MCM) at millimeter wave frequencies [2]. Common to each of the aforementioned approaches is the incorporation of packages at the last phase of product development. Since package integration does affect circuit performance, several design iterations are usually implemented before design requirements are satisfied. Monolithic packaging is a novel approach that provides integration at the circuit design level which offers several advantages. First, the packaging parameters extend the number of design variables to enhance design flexibility. Second, circuit evaluation is inclusive since the package has been integrated simultaneously in the fabrication procedure.

Silicon micromachining techniques can be used toward the development of monolithic packages. To date several micromachined circuits which consist of antenna elements, TM_{01} waveguide structures, and planar designs have been implemented using this technique. Rutledge et. al [5] introduced a pyramidal horn antenna with a planar dipole integrated monolithically onto a thin membrane[1] dielectric in the millimeter-wave region. Soon thereafter, one waveguide structure was developed using similar techniques [10] for W-band applications. Since that time, high performance planar transmission lines such as the microshield have been investigated [6] using membrane supported technology.

The planar circuits can be improved significantly by reducing loss mechanisms common to many planar topologies: (a) dielectric and (b) radiation loss. Complete elimination of dielectric losses is achieved through substrate removal that produces planar lines supported on membranes. Demonstrations have been shown for components that include filters to power dividers for frequencies between tens of gigahertz (X-Band) to hundreds of gigahertz (above W-Band). In fact, an extensive collection of planar lowpass to bandpass filters exist based on tuning stubs [6], couples lines [7-8], and lumped elements[9]. An alternative that reduces the loss mechanisms associated with the dielectric can be achieved

1. Membrane is a tri-dielectric layer consisting of silicon dioxide/ silicon nitride/ silicon dioxide having thicknesses of 7500Å/3500Å/4500Å.

by controlling the excitation of substrate modes in the form of surface waves and higher order modes.

Both radiation and dielectric loss are addressed in the development of self-packages that incorporate a monolithic shielding package around planar circuit elements using micromachining techniques. Typical to many planar circuits are the excitation of substrate modes, parasitic radiation and package resonances. Together, each of these mechanisms can severely degrade the electrical performance of planar circuits. As the frequency of operation increases to millimeter waves and above, the use of conventional planar transmission lines is diminished since the losses are very high in comparison to the signal strength propagating though the circuit. In order to benefit from existing circuit designs to develop high frequency systems, novel solutions are required to minimize the aforementioned unwanted properties that are inherit to conventional planar designs.

To reduce substrate modes effects, the formation of the lower cavity regions isolates the dielectric medium propagating the undesired mode from the continuity in the substrate Once metallized this shielding can reduce or eliminate unwanted electromagnetic effects that oftentime decreases the amount of useful power available in the circuit. This dimension can be chosen such that any resonance occurs outside of the desired frequency range of operation. Since this type of excitation is detrimental for both planar circuit and antennas elements, use of silicon micromachining technology can open an entirely new arena in high frequency design with an unlimited number of potential applications. To address radiation issues, individual shielding to circuits can offer improved circuit performance by isolating the circuit from neighboring circuits and by reducing interference of random electronic signals.

In addition to decreasing radiation, this approach addresses a number of problems associated with high frequency package design. There are a number of problems that arise from poorly designed electronic packages at high frequencies. One of them, mentioned above, is caused from parasitics in planar transmission lines while the other is associated

with the package layout and configuration. Planar circuits are lightweight, low cost, and conformal and many are easily integrable with active elements. Unwanted parasitics, however, are the cause of many problems in circuit performance and occur whenever discontinuities arise in a circuit design to cause radiation. Package layout and the configuration issues on the other hand influence proximity (or near neighbor) coupling and package resonances that also contribute to performance degradation. Resolution to these problems can be addressed in a variety of ways, either through improved circuit designs or though packaging. The investigation of this novel packaging concept is the subject of the work presented herein.

1.2 OVERVIEW

In this work, a novel approach is proposed that considers the package as an additional parameter to the circuit design and allows monolithic integration with the circuit. This approach presents for first time a monolithic package that has been extensively characterized for microwave and millimeter wave applications. With the use of advanced processing techniques that have been traditionally associated with sensor technology and high frequency circuit design techniques, this packaging concept can be realized and applied to a number of basic circuits that are commonly used in many high frequency applications.

This dissertation is organized into two main sections, the development/characterization and evaluation of the micromachined self-package and circuits. The packaged configuration is described by its cross-sectional geometry and categorized as partial or completely shielded. Next, extensions of this two dimensional topology can be in a straight (linear) or bending (non-linear) direction which is referred to as "in-line" or "conformal" packaging. The conformal package can also be used with multiple input paths to a circuit. Three techniques are required to completely develop and characterize the structure: fabrication, measurement and theoretical.

Chapter 2 presents the fabrication techniques required to develop this structure and various phases of the self-packaged circuit topology are discussed with the merits and problems associated with each design. In Chapter 3, the measurement and theoretical techniques utilized to characterize the package and circuit are discussed with a summary of the factors contributing to measurement error. Next, demonstrations of the concept is applied for various packaging configurations.

The results presented in Chapter 4 indicate the performance of stubs and filters indeed show improved performance over conventional open structures of similar design due to the reduction of parasitic radiation. Basic designs such as a detector circuit and double right angle bend have also been evaluated to show the flexibility of using micromachining as a conformal package. While many issues of planar circuit performance are significantly impacted by the excitation of substrate modes, this packaging approach has been extended to include planar radiating elements such as the microstrip patch. In Chapter 5, the micromachining approach is applied to an antenna problem where the effective dielectric constant is reduced underneath the antenna while maintaining the feeding networks on high index substrates for design compactness. Chapter 6 concludes this work with a summary and suggestions for future work in this area.

CHAPTER II

DEVELOPMENT OF MICROMACHINED PACKAGES

2.1 INTRODUCTION

For millimeter and sub-millimeter wave applications, system development is required with transmission and radiating elements as well as sources and respective circuitry in order to communicate with existing hardware. Waveguide and aperture based systems have been successfully implemented at these frequencies since these structures only require scaling of dimensions and rely on existing manufacturing technologies. An alternative approach for an aperture-based system that was observed in the late eighties were a monolithic integrated horn array [5] and a monolithic waveguide structure [10]. At that time, one of the main limiting factors in the realization of high frequency systems was the availability of adequate planar transmission line geometries. Since loss mechanisms found in traditional planar circuits in the form of radiation and parasitic coupling cause extreme performance degradation at higher frequencies, a need existed for exploration and development of novel circuit geometries that overcome these mechanisms. This motivated a large scale investigation into alternative methods that offer improved characteristics. One approach focuses on the use of silicon micromachining techniques to provide an alternative method for the development of such geometries and is the topic of this work.

In many circuit and array applications, design flexibility is extremely important therefore novel transmission line geometries that offer generic shapes and an increase design parameters are desirable in order to develop circuits with optimum performance. Many

limitations observed in specific circuit designs can be attributed to the inherit behavior of a planar line along with those effects caused by the surrounding environment. Existing planar lines, such as microstrip and stripline, have well known electromagnetic behavior. As a result, extensive geometry libraries are currently available for circuit realization. In recent years, however, monolithic integration of active and passive elements motivated interest in the use of coplanar waveguide lines since these provide more flexibility in accommodating design requirements. While each of the above lines provides certain advantages to high frequency applications, all of these suffer from losses associated with the dielectric and conductor, which ultimately limits their use for frequencies at and above the millimeter wave region. In addition, external factors associated with proximity coupling to neighboring circuits and electronic package resonances can also result in detrimental effects on electrical performance.

Circuits that geometrically and physically resemble coplanar transmission line technology and have cavity shielding on one side of the circuit were first proposed by Katehi and Dib [10-12] in 1991. In a comparison to the conventional coplanar waveguide (CPW) in an open medium, these geometries, which can exist with or without the substrate underneath the conducting line (Figure 2.1a), offer the advantage of lower radiation, thereby providing an alternative topology with improved performance. Of the two proposed solutions, one performs optimally as a result of the removal of material underneath the conducting line. This eliminates dielectric loss such that a membrane-supported line propagates a purely TEM mode and offers a non-dispersive behavior up to the terahertz frequency range [13]. The other solution is a topology that results in improved performance by providing shielding around the transmission line to form a microcavity (Figure 2.2). This reduces the radiation effects caused by parasitic coupling and substrate mode excitation while providing additional design parameters that can used to enhance circuit design flexibility.

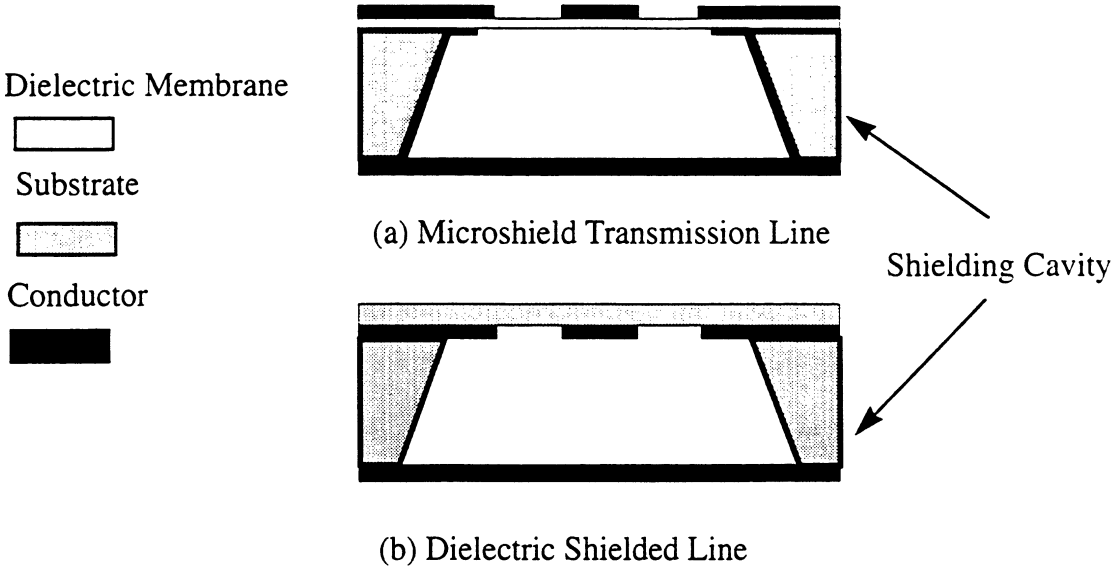


Figure 2.1 Novel Geometries for Microwave and Millimeter-wave Technology. (a) Dielectric membrane supported transmission line, called the microshield. The metal conductors are supported by the membrane and a lower shielding cavity is below the conducting line. (b) Dielectric shielded line has conductors supported by the substrate while a shielding cavity is mounted above the conducting line.

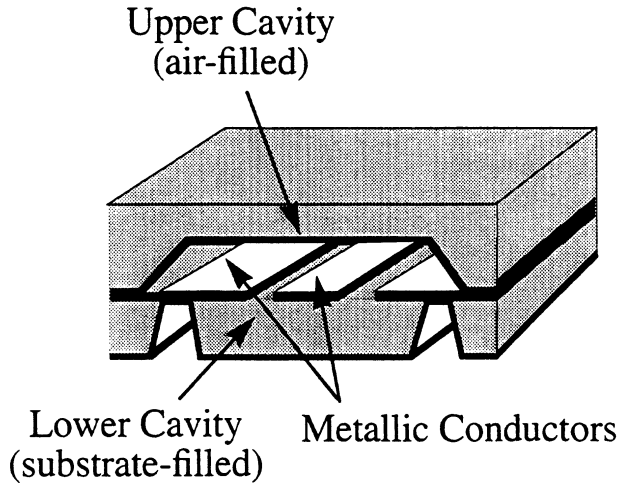


Figure 2.2 Self-Packaged Circuit Topology. Constructed out of two silicon substrate wafers. The upper wafer has an air-filled cavity that is mounted over the metallic conductors. The bottom wafer has a silicon-filled cavity is defined by the sidewalls of the v-grooves below the outer conductors.

In planar circuit designs, this micromachining technology has provided a flexible approach to the development of very low loss transmission lines [13] as well as micro-packages that provide self-packaging to individual planar circuit components. Investigation of the latter novel structure, the micropackage, is the primary focus of this dissertation which is intended to address the requirements of low-cost lightweight circuits in applications such as communication systems. In this study of an alternative packaging approach, the following topics are of interest in order to evaluate its potential to high frequency design. The primary issues include:

- characterization of micromachined topologies on CPW based circuits,
- demonstration of the shielding effects on simple high frequency planar elements,
- realization of a package that conforms to the shape and path of the electrical signal line, and
- integration capability with designs that include active elements integrated either hybridly or monolithically.

Before addressing the above topics, however, this chapter will present the evolution of the "self-packaged" circuit shown in Figure 2.2 and will discuss the critical factors associated with the development and fabrication of micropackaged topologies using silicon micromachining.

2.2 MOTIVATION AND OBJECTIVES

In the past, machine milling technology has been the primary method for developing metallic structures such as waveguides and test fixtures. To date, the smallest standard rectangular waveguide produced is WR[1]-3 while custom designs can be as small as WR-1 [13]. While this represents one approach for the development of small cavities that can be

1. Rectangular waveguide is denoted WR by the Electronic Industry Association (EIA) and represents the inside width of the rectangular waveguide dimension in english units of mils.

used to shield individual circuit components, there are fundamental limitations to this method regarding product development. As applications require size and space reduction, these metallic structures can add considerably to the overall weight and volume. The fabrication of specific circuit designs using this approach may be limited to low-volume applications, however it requires the cavity and planar circuit to be manufactured then tested separately, followed by additional re-evaluation. This method is extremely time intensive and costly in the fabrication and testing of prototype designs. An alternative approach will be presented in this chapter that addresses the need to develop low-cost lightweight circuits that exhibit improved performance over conventional planar circuits. This exploration focuses on the use of silicon micromachining to implement multiple package topologies that address the requirements of high frequency planar circuit designs.

While several factors motivated the investigation of high frequency packaging techniques, planar designs for use in millimeter and submillimeter applications will be tremendously impacted by the outcome. The investigation depends on identifying and addressing fabrication issues as well as circuit performance characterization which must be considered during the initial planning phases of this study. Moreover, accurate evaluation of circuit performance is best obtained using high performance circuits and testing methods. In order to achieve such accuracy, a state of the art on-wafer probing measurement system for high frequency characterization will be employed. The various calibration techniques available will be discussed in Chapter 3, however, it is important to introduce the subject of the measurement tool at this time since it has an essential role in the geometrical evolution of the packaged topologies discussed herein.

High frequency planar circuit characterization results from a combination of good design techniques and accurate measurement techniques. Since many calibration methods rely on the use of several circuit elements which vary in line lengths, a flexible measurement apparatus must be employed. While commercially available test fixtures can be used, the flexibility to measure novel complex three-dimensional structures such as planar cir-

cuits with shielded environments becomes more challenging. Custom-made fixtures may be designed to measure the specific circuit topologies of interest, however this may require additional time for test fixture development and evaluation. This may ultimately impact overall cost depending on the number of design modifications required to meet the circuit requirements. If separate fixtures are needed to accommodate each circuit, for example, many coaxial connectors may be required which can introduce measurement inaccuracies due to unreliable connector repeatability and increased cost.

One simple solution that is both cost effective and very accurate is to use measurement techniques such as on-wafer probing [14] which allow for testing of many circuits on a single wafer. This probing technique is the most accurate method for evaluating large numbers of planar circuits and can accommodate a variety of planar line geometries that have operating frequencies from dc to W-band [15]. Finally, testing time requirements are reduced significantly since the measurements can be made manually or automatically in industrial testing facilities.

Alternative methods for development of potentially inexpensive packaging schemes for high frequency circuits are discussed using fabrication techniques that are standard **m**onolithic and **m**icrowave **i**ntegrated **c**ircuit*s* (MICs and MMICs) processing. The following sections highlight the evolution of the "self-packaged" circuit shown in Figure 2.2 starting with the first version of the upper shielded cavity, which is a monolithic version of the machine-milled cavity mount, used to provide an initial understanding of the shielding effects on planar circuits [16]. This micromachined version addresses the monolithic integration of a multiple cavity wafer that is mounted over several circuits. Since the upper shielded circuits exhibit reduced radiation, additional minimization of other unwanted electromagnetic effects, mainly those observed in circuits measured on ground planes, is needed. This reduction of substrate mode excitation occurs with the development of lower shielded circuits that provides isolation between neighboring circuits residing in the same substrate material. Integration of both upper and lower shielded circuits result in the for-

mation of the first "self-packaged" circuit. The discussions will include specifications for each package design and measurement condition requirements, as well as, detailed discussions of the fabrication processes employed to realize the specific three-dimensional geometry. Lastly, current self-packaged configurations [17-18] will be discussed and extensions for the development of simple conformal packages are highlighted. Realization of simple basic planar circuit components that are based on these fabrication procedures are described in the following section and measured data will be presented in Chapter 4 on electrical performance.

2.3 GENERAL FABRICATION METHODOLOGY

The micromachined packaged circuits are comprised of a two-silicon (Si) wafer system having a <100> orientation and rely primarily on silicon micromachining processes. In sensor applications, this process is well-established and is frequently utilized in MEM structure development, however, these processes are relatively new to high frequency circuit design. Therefore, a discussion of the fabrication procedures required for the development of micromachined packaged circuits as it pertains to the planar circuit realization and specific cavity formation will be given.

While a variety of transmission line configurations can be used, the circuits in this work are based on coplanar waveguide (CPW) lines since these offer the advantage of having the signal and ground lines on the same plane. The shielding of the circuit is attained by miniature cavities that have been developed monolithically to reside in either or both upper and lower surrounding regions. In general the cavity geometry may consist of air or any dielectric material, however the standard convention used in this work will have air-filled upper cavities located above the planar geometry and substrate filled ones below. Typically high frequency circuits are developed on materials that provide reasonably low loss, therefore the following planar circuits are printed on high resistivity n-type silicon, $\varepsilon_r = 11.7$, with resistivity values in the range of 2000-3000 ohm-cm which is ade-

quate to achieve minimal loss effects in the substrate [19]. Since the upper cavity provides grounding to the circuit described, the value of resistivity is less important and are in the range of 6-10 ohm-cm.

While most of the discussions that follow involve the fabrication procedures employed, the factors associated with the testing apparatus will be commented on next since this ultimately influences the circuit design. There are three primary factors, illustrated in Figure 2.3, that influence the accuracy and physical measurement of these circuits in a probe station environment. The first deals with construction of the planar geometry with the shielding cavity while the second and third address excitation of the circuit on the probe station set-up. Configurations having an upper and/or lower cavity region must provide ground plane equalization between the shield and the CPW circuit. As a result the incorporation of mechanisms for the alignment of several wafers is required. In order to measure the circuits, however, access to the shielded region is necessary and achieved by incorporating windows that allow entry of the high frequency probe to the circuit input line. Lastly, transitions between the open and shielded region, which will be discussed in more detail in Chapter 3, are needed for appropriate excitation of the shielded geometry.

The remaining sub-sections concentrate on the evolution of the various packaging configurations and are organized into three main parts: (1) half shielded, (2) self, and (3) conformal packaging. The development of half-shield circuits with upper or lower cavities has produced fundamental knowledge for package development. Packages (2) and (3) are based on a combinations of upper and lower cavity sections and are modified to accommodate the appropriate design requirements while providing the basic foundation for extensions to a variety of complex circuit designs that may be used in high frequency designs.

2.3.1 Air-Filled Upper Shielded Circuits

There were many fundamental concerns regarding fabrication and construction of shielded circuits initially; therefore a review of some of the issues pertaining to substrate

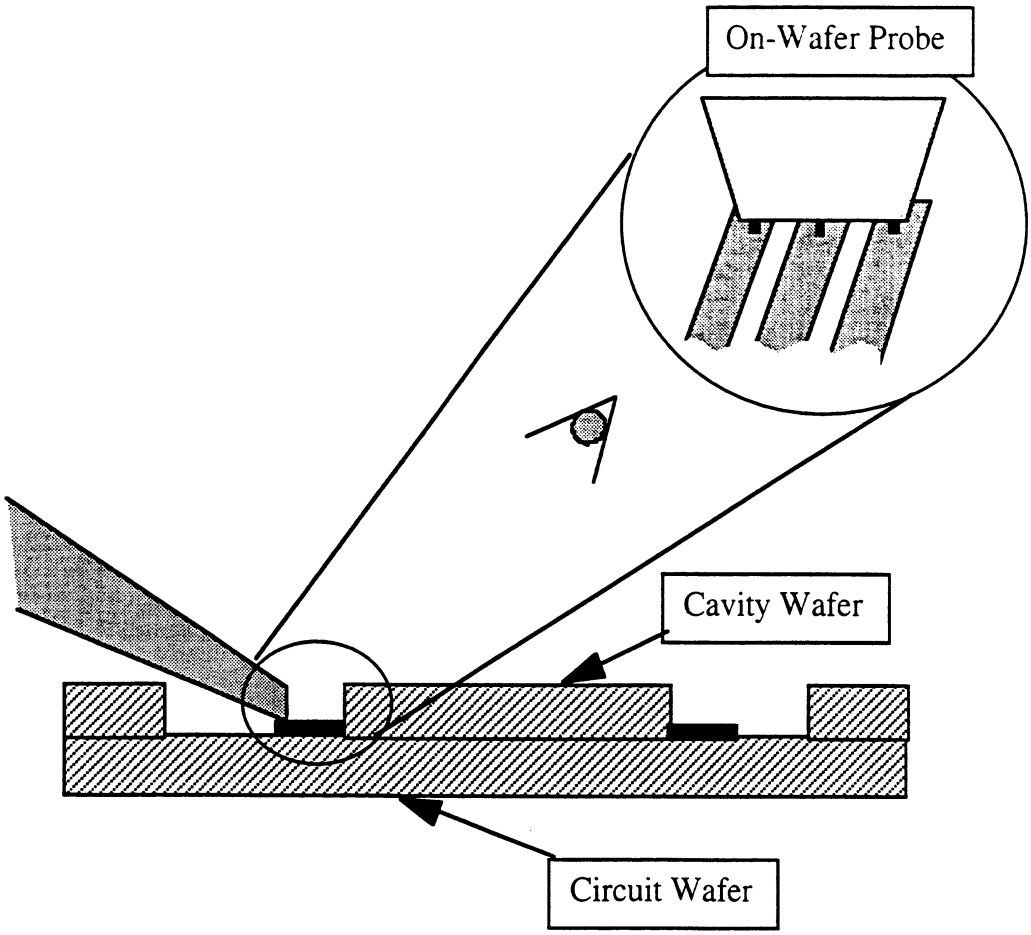


Figure 2.3 The probe window needed to measure a circuit on-wafer.

material selection and appropriate fabrication technique identification is given. Although high frequency devices and MMICs are usually realized on GaAs substrates, the vision of this work is to provide packaging alternatives for dense complex circuit layouts that produce improved electrical characteristics using reliable fabrication techniques. Therefore compatibility to existing MMIC processes and cost effective solutions are important goals. Silicon substrates have become an essential part of the microelectronics industry and a wealth of knowledge is available that can be used in the development of novel solutions to packaging high frequency circuits. Sensor applications, which rely heavily on silicon micromachining, make extensive use of advanced etching techniques. With the availabil-

ity of high resistivity substrates at reasonably low cost, Si invariably is the first choice in which these novel packaging schemes will be explored. In addition, planar circuit designs and high power devices, currently being developed with Si-germanium technology, show promise in high frequency circuits applications. Silicon substrates are used here, even though these topologies can be developed in other materials such as GaAs so long as appropriate modifications are used to realize the appropriate cavity geometry and similar electrical behavior.

Two main issues that were considered carefully are the etchant type and selectivity between wet and dry etches and its respective isotropic or anisotropic behavior. Repeatability and consistent process control are typically achieved using dry etchants, however, high selectivity between metal and dielectric masks is difficult [20]. On the other hand, certain wet anisotropic etchants used in micromachining are quite successful since selectivity ratios between specific crystal plane orientations depend on the anisotropic etch chosen. From research, etch rates have been determined for bulk silicon that are reliable for micromachining using well-controlled bath conditions for potassium hydroxide (KOH) and Ethlylenediamine pyrocatechol (EDP) wet etchants. With appropriate masking dielectrics, such as silicon dioxide and silicon nitride combinations, cavity configurations can be formed which have an etch profile of 54.75° with respect to <100> plane.

2.3.1.a Version One: Basic Cavity

The primary objective in the development of the first generation of air-filled shielding cavities is to produce a micromachined version of a machined-milled cavity. A planar circuit shielded by a machine milled cavity has produced a desired circuit response for coplanar based lines and has shown reduced losses for discontinuities after careful determination of the planar line geometry and cavity dimensions [16]. Since many circuits can be realized on a single substrate sample, batch processing techniques are employed to produce a variety of circuits that have consistent physical similarities. The circuit layout

consists of at least three calibration standards and a variety of circuit elements which occupy at most one-quarter of a three inch section wafer in the approach used in this methodology. The cavities are included in the layout to correspond to the various circuits and have been oriented to form vertical column alignment. Each column contains cavities that have been separated with similar spacing to the circuits on which they are to be aligned. Since the cavity lengths vary in some cases, one edge has been held constant for each cavity while the other edge accounts for the length variation (Figure 2.5). The cavity depths in this design are approximately 200 microns and are determined so that they provide appropriate shielding to each circuit while maintaining a 50 ohm impedance for the coplanar line. If the cavity shield is placed in close proximity to the transmission line, disturbances to the electric field distribution in the slots of the coplanar waveguide will occur, causing undesired line characteristics.

To facilitate the placement of the cavities over the lines, alignment of the cavities to the circuit wafer is achieved by including rectangular window openings. Each window is aligned to the metallic marks on the circuit surface and as shown in Figure 2.4 in the final version of the cavities shown mounted over the various planar circuits. To produce the design, a two-step etch procedure is employed and requires a layout that requires the inclusion of alignment windows, scribing marks, and cavity regions as shown in Figure 2.5. The following section will focus more on the general procedures used to fabricate the cavity structure.

1. A three dielectric layer consisting of silicon dioxide/silicon nitride/silicon dioxide ($SiO_2/Si_3N_4/SiO_2$) has thicknesses of 4500 Å /3500 Å / 7500 Å and each layer functions as a mask. Using standard optical lithography processing techniques to pattern the wafer, the two outer dielectrics are removed from all regions to be etched using buffered hydrofluoric acid (BHF) for the oxide (SiO_2) layers and CF_4+O_2 in the plasma etcher for the nitride (Si_3N_4) layer.

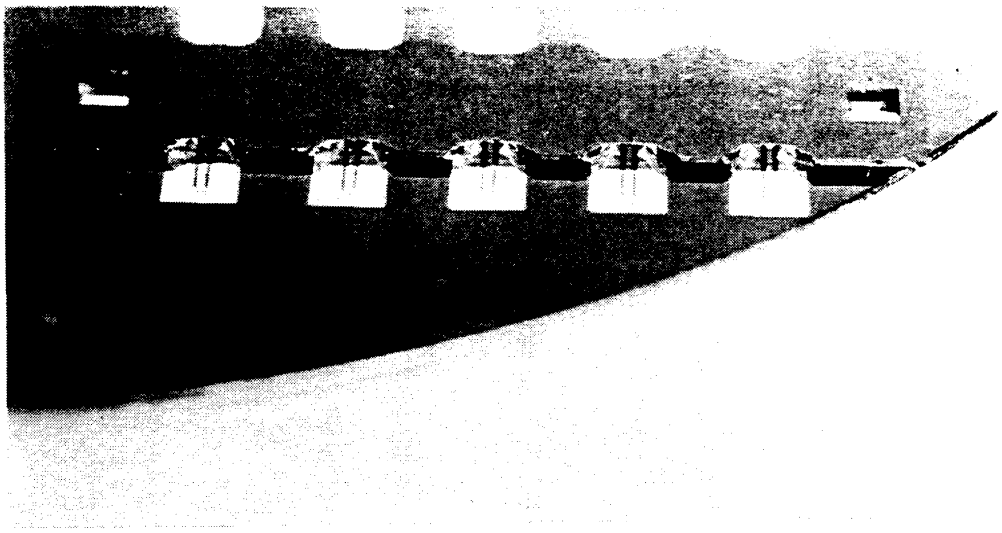


Figure 2.4 Photograph of the circuit with the single-strip cavity over the circuits.

2. After repatterning to protect the lower oxide in the cavity area, the sample is placed into the KOH bath solution where the alignment windows are etched approximately half way through the wafer.

3. The sample is then removed from the bath and the silicon surface in the cavity region is exposed using BHF etchant and returned to the KOH etch to remove the desired cavity depth of 200 microns. For the KOH recipe used in this process, the etch rate was approximately 29.6 microns/hour, which required approximately 13 hours to etch completely through a 390 micron wafer in this process.

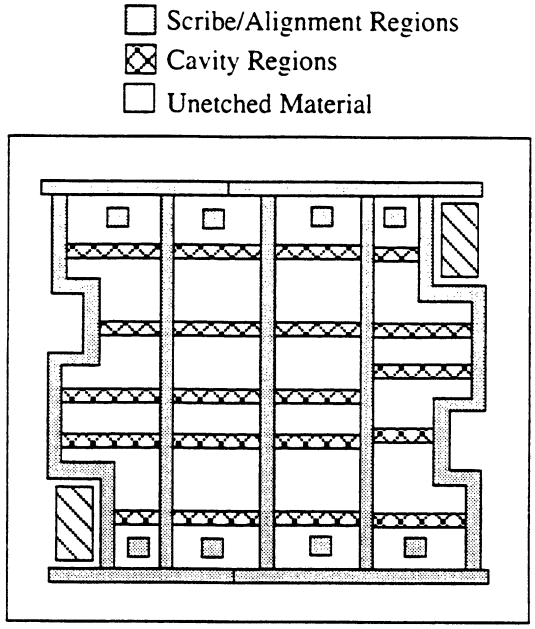


Figure 2.5 This represents the upper cavity wafer for the single strip cavity approach shown in Figure 2.4. The Crossed areas represent the region where the cavity is formed. The Hatched are is where the etch rulers are incorporated. Finally the dark regions are where the cavity strip it detached from the larger wafer area using chemical scribing.

4. Since the scribe lines are completely etched through, each vertical column section will be separated. The cavity structure is then cleaned and metallized with evaporated Cr/Al/Cr/Au to achieve a thickness of 1.5 microns.

This procedure proved to be the best method even though many other approaches were investigated. Initially a 1.2 micron oxide layer was used as a mask, however, this thickness is insufficient to accommodate the extremely long etch times. The thickness issue is compounded by the post-KOH oxide etch, which removes additional dielectric from the other masked areas leaving an inadequate amount of oxide for remainder of the cavity etch time. To overcome this problem, several other approaches were implemented to provide an additional masking layer as protection during the removal of the material in the cavity region. Alternatives masking layers based on metal systems such as chrome-gold (Cr/Au)

and chrome-aluminum (Cr/Al) were tested, however these also produced poor results. The main reason is due to adhesion problems associated at the metal/oxide interface since thin metal layers of approximately 2000Å are thermally evaporated on to the surface. These adhesion problems were not noticeable during the first etching step, however after the second oxide etch small pockets of solution were observed on the surface of the wafer in the metal areas after the samples where submersed into the KOH bath. These problems are related to thermal issues as a result of long etch times in temperatures ranging from 55° to 60° C. Problems in adhesion can result from metallic pinholes which become noticeable after the oxide etchant since the bare silicon surface is exposed and subjected to the KOH. Other adhesion metals such as titanium were investigated, however similar results were also observed which motivated modification of the process and selection of a different masking material.

The tri-layer dielectric materials mentioned above, sometimes referred to as a membrane, allow for successful development of the cavity structure in the KOH solution. The nitride layer in particular is very resistent to many acidic solutions therefore it provides additional protection to the wafer surface during the removal of the lower oxide layer in the cavity regions. This resulted in good masking capabilities, and the problem of metal adhesion is now eliminated since it is no longer required as an additional mask. There is, however, another problem that arose regarding the use of membrane which impacts the successful reliability of the above process. Membranes have been successfully etched in KOH solutions at the University of Michigan by Ling [21] and Ali-Ahmad [23], however a varnish is applied to the front side of the dielectric to serve as a protective layer for the upper surface since backside wafer processing is required to make free-standing membranes. In this case a protective layer is not compatible with the desired design requirements and cannot be used. The nitride tensile stress can be counter balanced by adding even though oxides layers unless low-stress nitrides are used. In long continuous etching cycles, this problem seldom occurs since a photoresist mask protects the entire wafer dur-

ing the dielectric removal. Even though these cracks may be present, the outer oxide layer is protected by the resist during the dielectric removal. On the other hand, when this procedure requires an additional oxide etch after the Si material has been partially removed by the KOH etchant, any imbalance of stress in the dielectric layer will produce membranes in compression or with low grade stress cracks that become more pronounced as in the process described above. These cracks allow for severe surface damage from the KOH across the entire surface of the wafer. Therefore, since a testing procedure and calibration on the appropriate membrane tensile stress compositions was not available, other etchant solutions were investigated.

To summarize the above discussion, the first generation of upper cavities are realized using tri-layer dielectric combinations as masking layers in a KOH chemical solution. The procedure works in general even though there are some issues regarding membrane tensile stress which can be alleviated with the appropriate choice of dielectric layer thicknesses. Tensile stress tests are described in the appendix of Ling's thesis [21] and can aid in the determination of the appropriate thickness needed for a given wafer size.

2.3.1.b Version Two: Cavity with Access Windows

In this phase, the issue of aligning multiple cavities with more reliability is addressed along with minimizing the sensitivity of the dielectric masks in the etching solution. The shielding cavity structure in the first version was developed where single strips are used to represent cavities having similar or varying lengths. This arrangement validated the realization of the micromachined structures, however it has limited alignment repeatability since the cavities are not mounted simultaneously. To alleviate this problem, large windows have been incorporated that attach the various cavity columns in order to align all of the cavities to the circuit wafer. The requirements for the windows are to provide probe entry access to each circuit while concurrently providing a mechanism for alignment of all

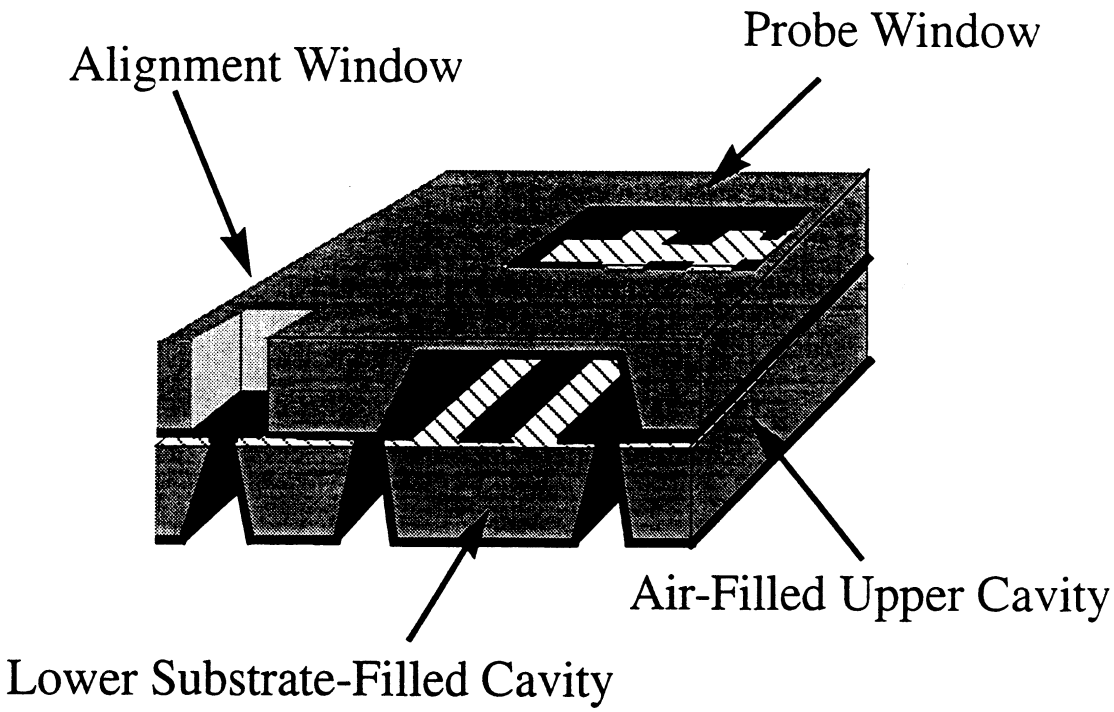


Figure 2.6 Completely shielded micropackaged circuit with lower and upper wafer alignment.

cavities in the same relative position of each circuit. Any misalignment at this point can be accounted for in the calibration which improves the accuracy of the characterization.

Initially, KOH solution was investigated, however, due to the long etch time requirements and problems discussed above in the first version, EDP anisotropic etch is used the remainder of this work. Probe and alignment windows are incorporated and etched entirely through the wafer while the cavities are etched partially. The use of EDP in this case has reduced the etch time to about 5 hours for a 390 micron thick wafer and the issue of tensile stress has been eliminated. The following description highlights the fabrication procedures implemented:

1. The first two dielectric layers, silicon dioxide and silicon nitride, are removed from all areas to be etched as before.

2. The wafer is then repatterned to protect the cavity region and the lower oxide layer is removed in the probe and alignment windows.

3. Since the desired cavity depth is approximately 200 microns, all windows are etched to ≈150 microns before the last layer of the oxide is removed from the cavity region.

4. The oxide is then removed using buffered hydrofluoric acid (BHF) and the sample is returned to the EDP solution to remove the additional 200 microns of silicon in the remaining areas and the cavity region.

Although the above procedures represent the general form of the process, some concerns did arise regarding the realization of the geometry. While attempting to achieve the desired cavity formation, severe lateral etching was observed in the cavity region as a result of the rapid etch. This is a problem since the etch depth and cavity upper wall depend on the etch used in the fabrication procedure. Many alternatives were investigated to reduce this effect of lateral etching at the entrance of the cavity. The first objective is to determine the difference between the EDP and the KOH used previously. Since all of the probe windows are etched entirely, removing large cross-sectional areas produces uneven etching across the surface due to the selectivity of the etch ratio between <111> and <100> plane. In a large rectangular area, the centers of the surface are not removed at the same rate as the sidewall and result in the inverted bowl profile shown in Figure 2.7. In order to completely remove this material from the center region, etching continues along the cavity edge which causes lateral etching in the cavity upper roof. This results in a narrow horseshoe shaped openings in the upper surface of the cavity entrance regions compared to the straight edge obtained in the KOH etch. To minimize this effect, a channel is etched along the perimeter of the desired rectangular window completely through. Once the channels are etched entirely, the center sections separate apart from the remaining wafer which reduces the edge exposure of the cavities and results in less sever overetching.

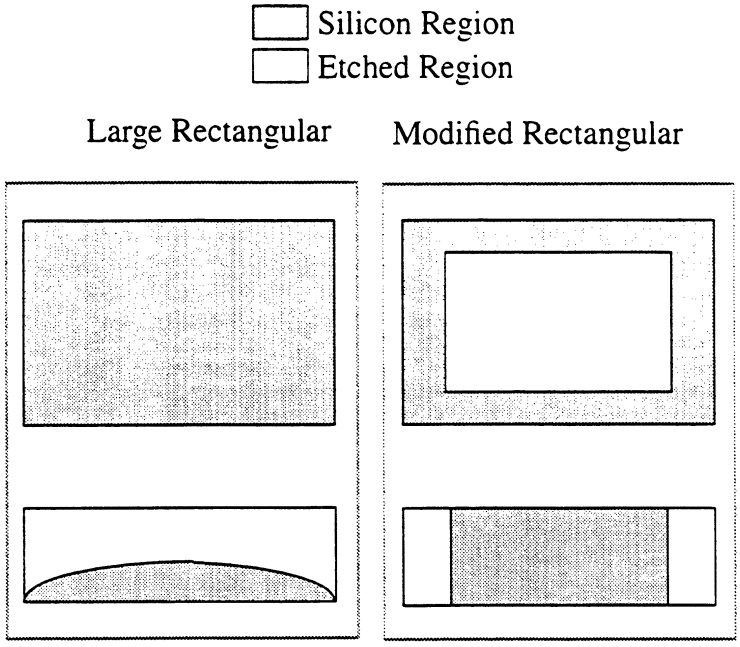


Figure 2.7 Etching profile of the probe window area and the cavity region.

While the cavity formation and accurate reproduction of the desired dimensions is fundamentally important, wafer strength is equally important since these cavity wafers are handled during cleaning, metallization and mounting steps. Single side processing resolved the alignment problems for the multiple column circuit layout, however wafer strength is seriously compromised by the probe windows which emphasizes the inherit weaknesses of the cavity regions. Approximately 150 microns remain in this region, the bulk of the wafer handing on the perimeter of the wafer cause forces to propagate directly to the cavity regions which result in breakage, usually within the cavity columns. This is especially true when the cavity lengths vary in the particular column. These problems have motivated the use of support bars within the probe windows to provide additional support to the wafer. It effectively shortens the cantilever length created by the column such that forces caused by lifting and handling the wafer are minimized in the cavity

regions. Improvements of wafer strength and handling are the primary goals of the next version and are achieved with support bars and double-sided etching.

2.3.1.c Version Three: Cavity with Access Windows based on a Double Side Etch

The final version of the upper shielded structure represents the basic foundation for future designs and provides the most reliable process technology for developing these shielding configurations in EDP etch solution. A combination of design practices and fabrications techniques are established to address the development issues associated with the upper cavity and these can be adjusted to meet the requirements of any etching technique. The main component is the use of double-sided etching techniques in regions that must be etched entirely while providing additional protection to accommodate the single-side etched sections. This offers the advantage of using a single layer dielectric of oxide which reduces processing time. Ideally, the probe window should allow probe entry to a single circuit, however, the probe window must be sized to meet the physical constraints of the measurement probe. For the majority of this work, a triangular shaped probe head by Cascade Microtech WPH-150-K is used with very large windows that enable multiple circuit access in a probe window strengthened by a mechanical support bar. Air-coaxial CPW probes are available which allow for single window access to each circuit since the probes are smaller. This eliminate the need for the support bars.

The following is a description of the development of this upper wafer topology which contains both upper cavities and alignment marks that are formed by etching from both sides of the wafer. Since these cavities provide ground plane equalization and shielding without interfering with the signal path, it is not necessary to use high resistivity Si. The upper shielding in this work is developed using 500 micron thick low resistivity Si with 7500Å of thermally grown oxide on both sides (See Figure 2.8).

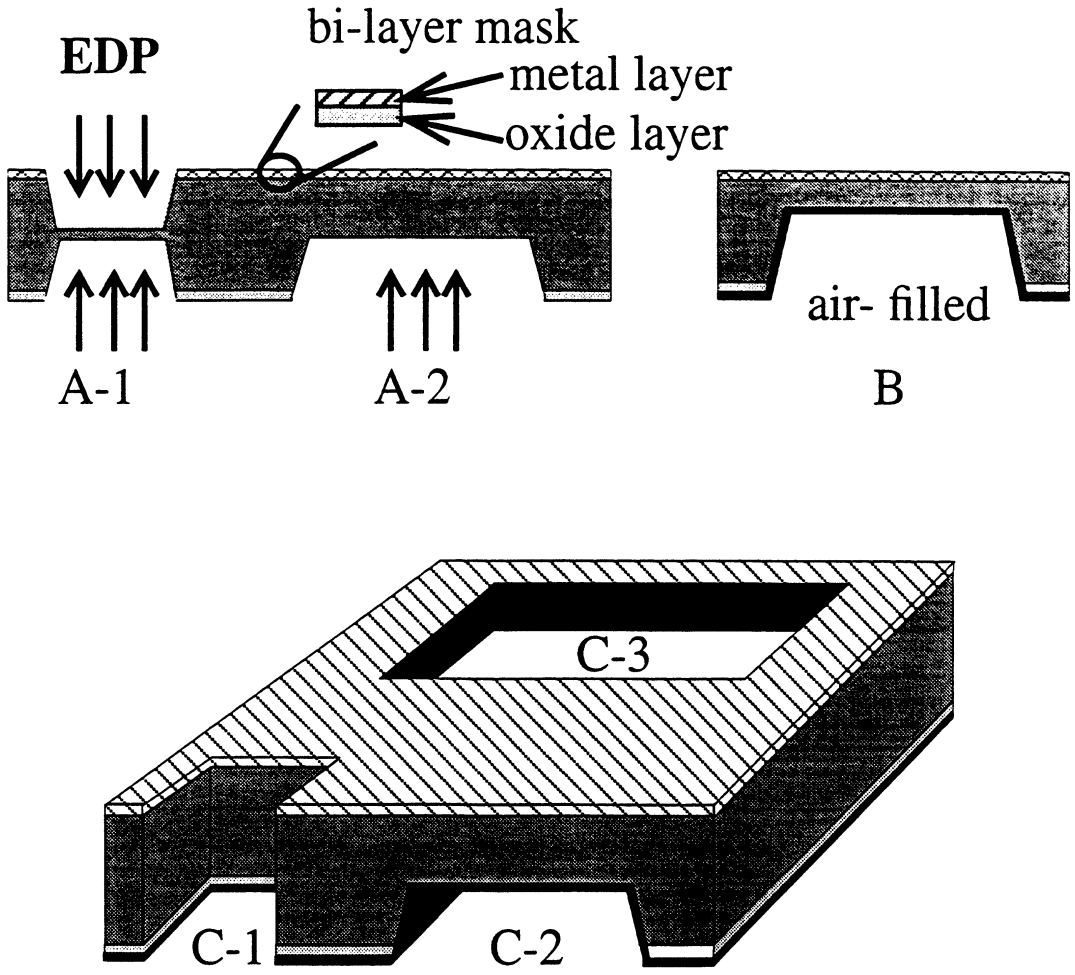


Figure 2.8 Upper Wafer Development. A. Probe windows and alignment marks (A-1) are etched from both sides while the upper cavity (A-2) is etched from one side only. B. The upper cavity is then metallized. C. The upper wafer sectional view after processing with the alignment marks (C-1), upper cavity (C-2) and the probe window (C-3).

1. After defining the probe window and alignment marks using photolithography, a metal lift-off procedure is employed to open the areas to be etched and to provide an additional masking layer of Ti/Au metal on

the backside of the wafer. This layer serves two purposes: it offers protection on the back of the cavity regions and it acts as a mask during backside IR alignment.

2. On the lower side, the cavities are defined and the oxide is removed to expose the silicon surface. The patterns are then etched in EDP to a desired depth that is monitored using "etch rulers", which consist of rectangular widths corresponding to specific etch depths.

3. Since this wafer must be handled frequently after etching the multiple cavities and windows, additional mechanical strength can be provided by including a "structural beam", located in the middle of the probe window.

In this scheme, a metal mask is required for the infrared alignment procedure. Since the oxide etch is performed prior to etching and the metal surface is protected and doesn't exhibit pinholes during the EDP procedures.

2.3.2 Self-Packaged Circuits

The self-packaged circuits results from a combination of the upper half shielded cavities described in Section 2.3.1 and a lower shielded substrate filled cavity described here. Since the upper cavity has been investigated thoroughly, the requirement for self-packaged circuits depends on the development of the lower shielding cavity which is emphasized in this section and discussed below.

The *lower wafer scheme* shown in Figure 2.9 is fabricated on a high resistivity, single-side polished, 350 micron thick silicon substrate having a dielectric mask of silicon dioxide that has been thermally grown to 1.2 micron thickness or a membrane tri-layer dielectric. The fabrication of these circuits is described below:

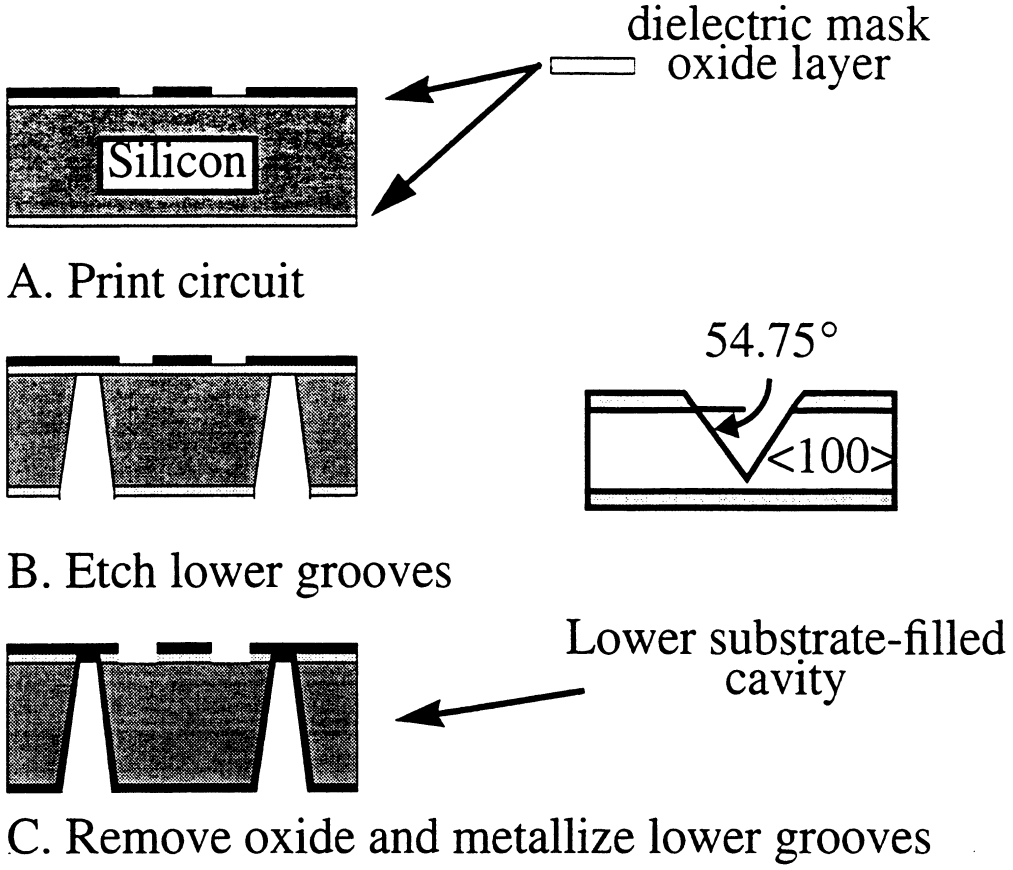


Figure 2.9 Lower Wafer Development. A. Transmission lines are printed on the top surface. B. Lower cavity is formed by etching v-grooves. C. Lower cavity grooves are metallized below the line forming direct contact to the upper ground planes.

1. Since this wafer contains the planar circuits and lower cavity region of the circuit, dielectric is removed on the upper surface. This will allow ground plane on the upper surface to be in contact with the outer shield after the lower cavity is formed.

2. The planar circuits are then defined using standard photolithographic techniques and electroplated to the desired metal thickness after evaporating a seed layer of titanium/gold/titanium (Ti/Al/Ti).

3. Once the circuits and alignment marks have been printed, the lower side of the wafer is patterned photolithographically and regions needed to form the lower cavity are defined using an infrared (IR) alignment procedure.

4. Prior to anisotropically etching the silicon, the dielectric is removed on the backside of the wafer in the areas that define the cavity sidewalls. Using the EDP etchant, the cavity formation has pyramidal sidewalls [25] as seen in Figure 2.9B, where the lower cavity is the substrate-filled one shown with its widest dimension at the upper surface and narrowest dimension at the bottom of the cavity (Figure 2.9 c), simulating an inverted pyramid.

5. The lower cavity shielding formation is complete after a seed layer of Ti/Au is evaporated and electroplated on the backside of the wafer or after a Ti/Al/Ti/Au system is employed for a thickness of $\approx$ 2 microns.

After fabrication of both wafers, the upper cavity wafer is aligned to the planar circuits that are printed on the lower substrate-filled cavity. The two wafers are then bonded together to finalize the formation of the micropackage Figure 2.6. The bonding is either photoresist which is a temporary bonding solution or silver epoxy which is a permanent one. Although the above procedures presents the development of a completely shielded or self-packaged configuration, partially shielded structures can also be obtained by implementing procedures presented in either the upper or lower wafer development scheme.

2.3.3 Conformally Packaged Circuits

Although planar high frequency circuits may be in the form of straight, curved, or right angle shapes, many times layout constraints require modifications of specific element placement within the design to accommodate the space limitations. This results in undesired electrical performance due to the proximity coupling between neighboring lines and

resonances that arise due to large package layouts. In order to meet designs requirements and minimize the layout effects, the concept of "in-line" packaging can be extended to that of conformal packaging which can follow the direction and path of specific circuit components. This section will highlight briefly the implementation of such concepts for cross-tee junction and right-angle bend configurations. Comments are made regarding fabrication issues pertinent to the realization of such topologies. In one case, a packaging structure is developed that shields a planar circuit with active elements while the other will illustrates the development of a cavity package that has right angle bends. The two designs are part of the foundation for establishing basic building blocks for a packaging library that may be instituted in a design based on micromachining techniques.

The conformal packages in this work are the foundation for the types of circuits and geometries that may be implemented in a variety of high frequency components and systems. The self-packaged circuits described earlier focus on the development of straight longitudinal packages where the cross-sectional effects of a package having an air-filled cavity in one region and a substrate-filled one in the other were the primary concern. Conformal packaging techniques additionally must address package designs that follow the path of the line around corners to provide overall shielding of a specific geometry. The fabrication process steps are very consistent with those described before, and will not be expounded upon in this section although specific issues regarding the development of the conformal package will be highlighted briefly.

The conformal package development starts with investigation of two basic geometries, the cross-tee and the right angle bend which consist of the two types of corners that must be addressed when using anisotropic etchant, concave inward and concave outward. Concave inward corners will naturally maintain their shape since the side wall intersect along the <111> plane that serves as an etch stop. Concave outward corners are etched since the crystal planes are not well defined at a corner edge. As a result, compensation techniques are required to address these problems and require modifications to the shapes at the cor-

ners so that the etch rate is comparable to those needed to achieve the desired cavity depth [22-23].

For the cross-tee, the exactness of concave outward corners has less importance since it is located under the ground plane of the planar line. However, minimization of the package resonances that could arise from a wide upper shielding cavity is critical. In this case (Figure 2.10), squares with a typical length of 200 microns are centered at the corners of the bend. After etching, corner rounding does occur that is not as severe as the corner without compensation. For the double right angle bends, a 400 micron square was incorporated in a similar manner and results in good shape replication of the corners for etch depths of 350 microns.

Overall, conformal packages for cross-tee junctions and right angle bends have been demonstrated. Since these represent entry level attempts to develop conformal packages, design rules are still needed in order to be determine the appropriate parameters required to achieve a specific shapes at the corners in a particular design. This entails investigating the effects of various geometries and also the types of etchants that should be used for successful replication of a desired shape. In this work, however the most important issue has been addressed which is to provide a demonstration of the use of self-packaging as a basis for conformal shielding of a given circuit geometry.

2.4 SUMMARY AND FUTURE WORK

This chapter has highlighted the development of micromachined packaged circuits that provide partial-shielding either above or below the planar circuit. Completely shielded circuits that form self-packaged planar components and conformal packages can be used to develop cross junctions and right angle bends. These techniques have resulted in a novel packaging technology that provides solutions to many high frequency problems. The fabrication processes presented utilize wet chemical anisotropic etchants such as KOH and EDP, though they are not limited to these. The methodology described in this

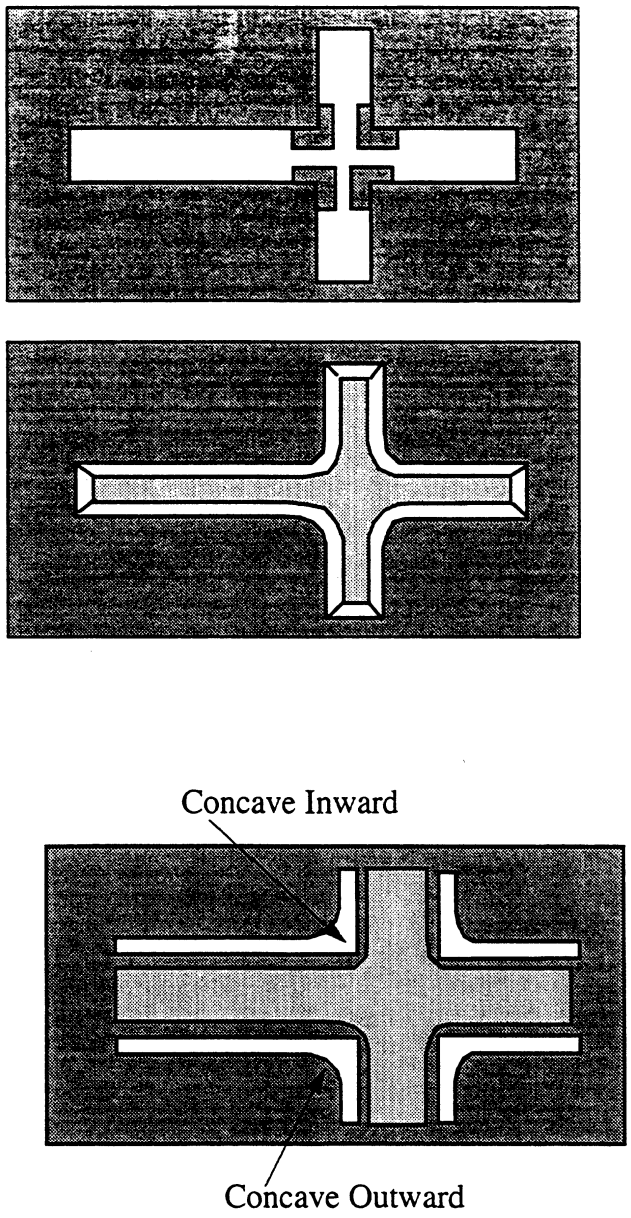


Figure 2.10 Cross-Tee Fabrication Layout for Conformal Package Development. The top View shows the effect of etching the upper cavity with compensation. The etched depth is 350 microns and the corners are slightly curved. Bottom View shows the lower wafer where the white slots represent the section that is opened on top for the dc contact and the dashed line is the section that is etched underneath. The curvature in both of the view result from the concave outward corners.

chapter represents one phase in the development of packages around planar circuits. Subsequent chapters will illustrate the other phases that lead to complete characterization of these topologies.

Some of the issues that are of immediate concern are the development of design rules that provide (1) more precise etch depth determination, (2) compensation design rules to produce a variety of geometries, (3) determination and completion of recipes for etching a variety of substrates (such as silicon and gallium arsenide) which include etch profile and surface roughness information.

CHAPTER III

THEORETICAL AND EXPERIMENTAL CHARACTERIZATION TECHNIQUES

3.1 INTRODUCTION

High frequency circuit characterization requires theoretical modelling and experimental testing in order to evaluate circuit performance. At low frequencies, analytic solutions based on static models are suitable to describe the electrical behavior of lumped element circuits. However, as the frequency of operation increases to the lower microwave range, lumped elements can no longer be used in circuit design since the dimensions are large compared to the wavelength of operation which results in distributive effects. Such behavior can be resolved by using planar circuits that are evaluated with quasi-static models. Within the last 50 years, modelling techniques which accurately describe the physical phenomena associated with high frequency planar waveguiding structures have expanded from basic quasi-static to full-wave analysis techniques. The behavior of many planar circuits are initially described using quasi-static approximations in order to determine the capacitance thereby leading to the characteristic impedance and propagation constant. These models, however, do not take into consideration the hybrid nature of guided modes associated with many quasi-TEM planar lines. Therefore, full-wave analysis techniques are required to address the dispersive nature of these circuits especially at the higher frequencies. Classification of these methods include spectral domain, method of lines, finite element, integral equation, etc., which provide complete characterization of the planar designs by accounting for the dispersion along with coupling and parasitic effects.

Self-packaged circuits require characterization of a structure that is comprised of a planar circuit and its shielding package. Several of the methods mentioned above can be employed to determine the design parameters and to accurately evaluate the electrical performance. It is important to note that successful evaluation of any novel circuit topology is a function of the interdependent relations between the design, fabrication, analysis and testing capability of the said structure. In this chapter, a summary is presented of the various models utilized in the design and analysis of the micromachined circuit. In addition, the measurement techniques used to evaluate the behavior of circuits are examined. In some cases, as will be seen in the next chapter, there may be discrepancies between the measured results and the modelled structure. Many of these differences can be attributed to various aspects of the development procedure; however, the fabrication methodology and the analysis techniques tend to have the most significant impact. While full-wave techniques in and of themselves are accurate, correct implementation of these techniques depends on the identification of the model assumptions and the establishment of its appropriateness to the particular design. Therefore, pre-knowledge of this information will enhance the evaluation of the design problem.

This chapter will present the methodology that should be taken to effectively utilize design and analysis tools that are available for circuit realization. A brief discussion of the software tools employed and respective assumptions which may aid in the interpretation of theoretical and measured results is given. The design tools are quasi-static models based on conformal mapping and spectral domain techniques. The analysis tools are full-wave techniques based on space domain integral equation (SDIE) method and finite difference time domain (FDTD) method. Lastly, discussions regarding the experimental set-up and the respective calibration procedures considered to evaluate the circuit performance will be described and discussed.

3.2 CIRCUIT DESIGN AND ANALYSIS TOOLS

High frequency micromachined circuit development occurs in two phases: (1) design and analysis and (2) fabrication and measurement. This section will discuss the design and analysis phase where the primary objective is to discuss the approach and tools used to determine the parameters required to realize a particular circuit design and evaluate its performance. The reader is referred to Chapter 2 for a detailed discussion of the fabrication issues and processes employed to develop these micromachined packaged circuits and Chapter 4 for specific circuit performance evaluation.

Theoretically, while full-wave analysis techniques offer the most accurate model predictions, they are inappropriate for use as design tools due to their complexity and time intensive computer requirements. As a result, initial circuit design is best achieved using simpler quasi-static models that are based on transverse electric and magnetic field (TEM) or quasi-TEM approximations. Once an entry level circuit design is complete, the specific geometry is realized in the appropriate topology which can then be analyzed using full-wave analysis techniques for performance verification. Since these models require specification of the exact geometry, highly accurate predications of the circuit response can be obtained for the modelled circuit. Performance improvements can be gained through an iterative approach to fine tune specific circuit dimensions to meet the given design requirements. After an optimum design has been determined, the circuit are fabricated and evaluated.

3.2.1 Design Procedure

A flow chart illustration for circuit development is shown in Figure 3.1. The first goal in the design of high frequency circuits is the determination of the physical geometry corresponding to specific electrical parameters. Typically, CAD tools, based on quasi-static or semi-empirical formulations, are employed to achieve the desired circuit response in terms of electrical parameters. While a wide variety of commercially available computer-aided

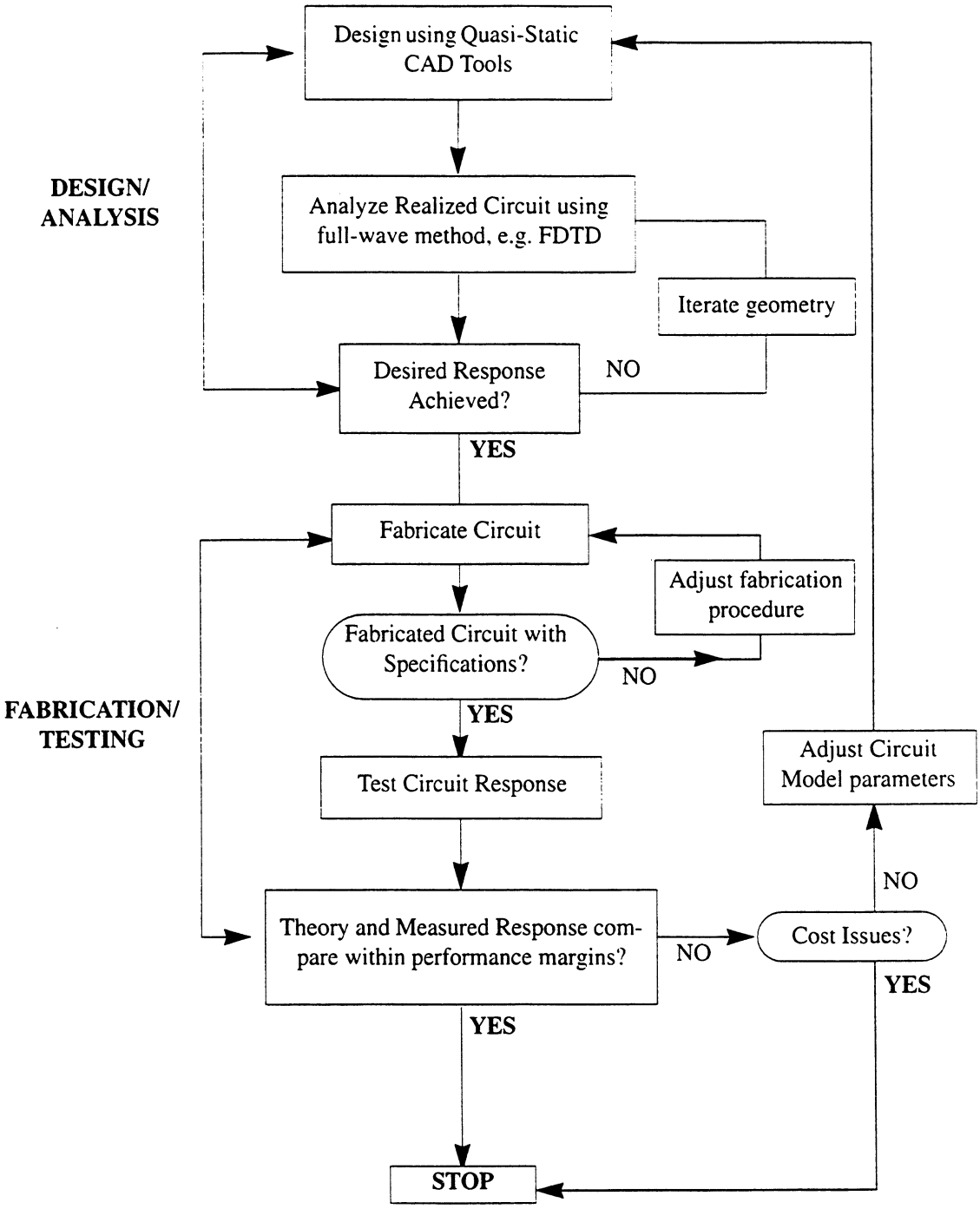


Figure 3.1 Design Procedure for Micromachined Circuits

design (CAD) software exists, the amount available for high-frequency design is relatively nonexistent. However, there are a number of high frequency circuit simulation tools in the market that indirectly aid in circuit design to produce satisfactory results. Due to the nature of the methods involved, however, very long design cycles and extensive computation times are typically required. Once the appropriate response is obtained, the circuit geometry is determined and then an analysis is performed using full-wave techniques such as the SDIE or FDTD method. During the detailed analysis phase, while the circuit response is being evaluated, changes are made iteratively to the geometry dimensions to improve the response. The final design of a circuit is then fabricated and the response is measured using an appropriate experimental set-up.

Once both theoretical and experimental results are available, comparisons are made to validate the circuit response. If the electrical response is within an acceptable performance margin, the procedure is complete. If the response is unacceptable, design objectives must be reconsidered. In the case of high performance applications, discrepancies between theory and experiment mainly arise from fabrication tolerances and approximations that may be used to determine the model parameters for the code. If design errors must be minimized, two options exist. The first involves modifying the steps in the fabrication procedure to reduce the geometrical deviations between the theoretically modelled and the measured circuit. In instances where prototype cost is a critical issue, the second option involves modifying the circuit designs such that sensitivity to fabrication tolerances is reduced while simultaneously preserving the desired electrical performance.

3.2.2 Theoretical Model Techniques

Several comments can be made regarding the theoretical techniques implemented in the modelling of micromachined circuits. Before a design can be realized, geometrical parameters must be determined. If the structure has a non-traditional topology, models must be employed that are designed specifically for the structure or that approximate it

reasonably well. In this case, electrical parameters such as the characteristic impedance are determined by evaluating the dimensions using the quasi-static model shown in [26]. This model uses conformal mapping to produce results that compare well to quasi-TEM point-matching methods with the advantage of reduced computational time. For dispersion characteristics such as the propagation and effective dielectric constants, a spectral domain technique (SDIE) presented in [27] can be used. This development is required in order to design appropriate feeding lines that are compatible with the measurement system and specific calibration procedures.

Commercially available software can also provide these parameters; however at the beginning of this work in the early 1990's, most were valid for open structures and could not easily accommodate the various shielding topologies discussed. Models that can address these geometries were developed for specific applications and are difficult to obtain. Programs such as PUFF [28] are based on ideal transmission line theory and are geometry independent if the design is evaluated in terms of the electrical parameters only. However, specialized full-wave programs are still required to evaluate a specific structure if the propagating modes are not TEM or quasi-TEM in nature which is the case whenever circuits exist in inhomogeneous environment. These static models become inadequate and the use of full-wave techniques is required for circuit analysis. While many techniques are available, the ones used here are based on SDIE and FDTD methods and are applied to the three-dimensional geometries described previously in Chapter 2. FDTD offers the most versatility in modelling near - exact shapes and dimensions of the realized planar lines and cavities (see Figure 3.1). Given the complexity of these techniques, a brief discussion is merited on the their implementation will be included.

3.2.2.a Space Domain Integral Equation Method

At the earlier stages of this work, the space domain integral equation technique (SDIE) was employed with the method of moments for the analysis of coplanar waveguide topol-

ogies with half-shielding using codes previously developed in [29]. In this boundary value problem for the coplanar waveguide circuits, the region is divided into two simpler ones

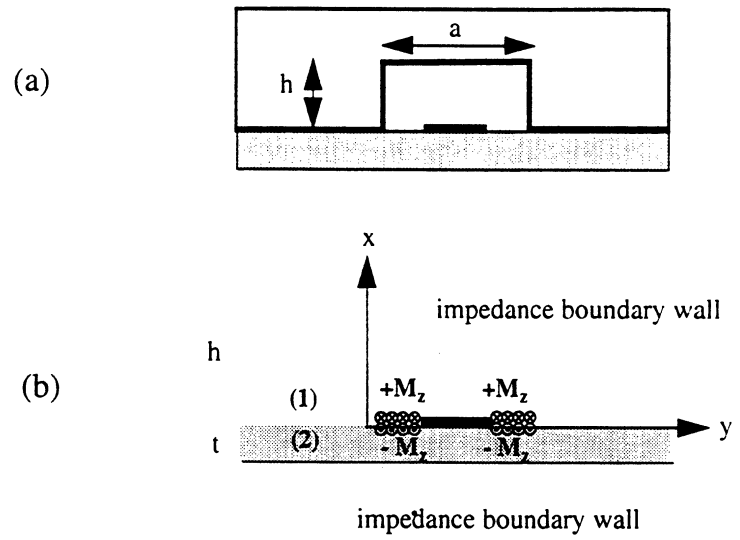


Figure 3.2 Half-Shielded geometry of Coplanar Waveguide Circuit and the Equivalent current representation for modeling using Space Domain Integral Equation.

where an equivalent surface magnetic current M_S is introduced on the slot apertures. These currents radiate into the full space region above and below the slot such that the boundary conditions of the tangential electric field on the surface of the slots are satisfied. Since the tangential component of the magnetic field is continuous on the surface of the aperture, an integral equation can be formulated as

$$\hat{n} \times \iint_S \left[\overline{\overline{G}}_0^h \langle \mathbf{r}|\mathbf{r}' \rangle + \overline{\overline{G}}_1^h \langle \mathbf{r}|\mathbf{r}' \rangle \right] \cdot \mathbf{M}_S(\mathbf{r}')\, ds' = \overline{J}_s \tag{3.1}$$

where $\overline{\overline{G}}_{01}^h \langle \mathbf{r}|\mathbf{r}' \rangle$ represents the Green's functions in the regions above and below the slots and J_S is the ideal current source feeding the circuit [31]. For the free-space Green's func-

tion, Sommerfeld integrals in the space domain are used in the open structure side while double summations are used in the shielding cavity regions. Excitation of higher order modes can be ignored since the cavity dimensions are very small in the frequency range of interest. After the SDIE (Equation 3.1) is solved using the method of moments where the unknown magnetic current is expanded in terms of rooftop basis functions, Galerkin's method is applied to reduce the above integral equation into a linear system of equations in terms of an admittance matrix.

$$\begin{pmatrix} Y_{yy} & Y_{yz} \\ Y_{zy} & Y_{zz} \end{pmatrix} \begin{pmatrix} V_y \\ V_z \end{pmatrix} = \begin{pmatrix} I_z \\ I_y \end{pmatrix} \tag{3.2}$$

Then, the electric field in the slots is obtained after matrix inversion for the equivalent magnetic current distribution. At points away from the slot discontinuity, the fields in the slots form standing waves which are used in the derivation of the scattering parameters. In this model, the radiation loss is evaluated in terms of frequency and other parameters for this half-shielded structure.

While this method provides very accurate results, there are several limiting factors that should be identified. First, the method provides single frequency data points per excitation, and second the code is topology specific. As a result, any physical changes in the geometry require redevelopment of the program. Computed data from this method will be presented in Chapter 4 for the scaled model version of the micromachined half-shielded circuit, referred to as the machine-milled half-shielded circuit and for the completely shielded circuit. Given the topology restriction of the SDIE method, a more flexible full-wave technique is needed to examine novel geometries not previously considered in [32].

3.2.2.bFinite Difference Time Domain Method

As mentioned in Section 3.2.2, the finite difference time domain technique offers flexibility since an arbitrary geometry can be evaluated primarily by appropriate discretiza-

tion. In this method, Maxwell's curl equations are first expressed in discretized space and time domains and, then are used to simulate the propagation of the initial excitation using a "leapfrog" approach [30]. In order to characterize any planar discontinuity, the propaga-

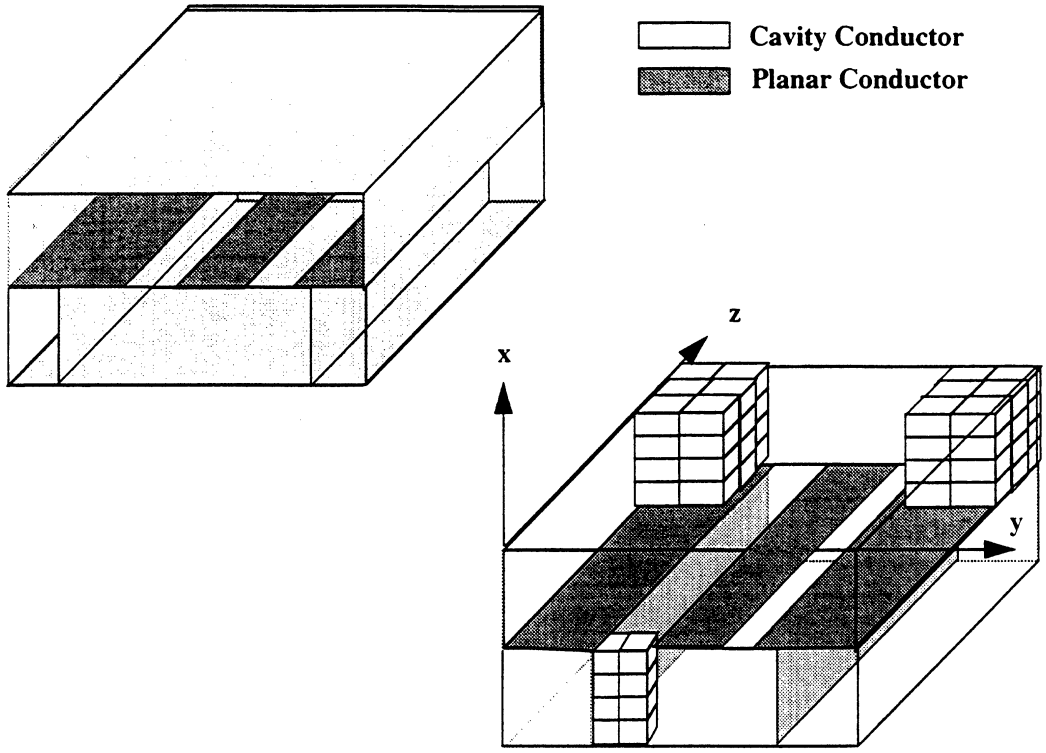


Figure 3.3 Illustration of the discretization of a shielded circuit using finite difference time domain method. The top view shows the side walls for the self-packaged circuit and the lower view shows random discretizations of with in x, y, and z directions with the cube elements.

tion of a specific time-dependent function through the structure is simulated using the FDTD technique. Although the time dependence of the excitation can be chosen arbitrarily; a Gaussian pulse is often used because it varies smoothly in time and has a Fourier transform that is also a Gaussian function centered at zero frequency. After discretization of time and space for the electric and magnetic field components, Maxwell's equations

being represented by FDTD equivalents are then used to update the spatial distributions of these components at alternating half time steps [30]. The space steps (Δx, Δy, and Δz) are carefully chosen such that an integral numbers of them can approximate the various dimensions of the structure. As a rule of thumb and to reduce the truncation and grid dispersion errors, the maximum step size is chosen to be less than 1/20 of the smallest wavelength, which corresponds to the highest frequency of interest represented in the pulse within the computational domain. To insure numerical stability, the Courant stability criterion is then used to select the appropriate time step.

This model assumes that the electric conductors are perfectly conducting with zero thickness and are treated by setting the tangential electric field components to zero at all time steps. For the electric field components lying on the dielectric-air interface, the average of the two permittivities is used in the FDTD equations. To terminate the FDTD discretized structure at the front and back planes, the super-absorbing first-order Mur boundary condition [33-35] is utilized to simulate infinite lines. The interested reader may refer to [30, 36 ,37 ,38] for a detailed description of the FDTD method.

Compared to other techniques, the FDTD method is relatively easy to implement for basic and complicated geometries. The only requirements are simple arithmetic operations in the solution process and it has the advantage of being flexible in both time and frequency domain analyses. By applying a Fourier transform on the time response of the discontinuity, frequency characteristics can then be obtained and the response represents a wide range of frequencies that include DC. This is important since it is based on one pulse simulation as opposed to the single frequency domain output from full-wave techniques. In addition, these have restriction on application at very low frequencies due to the long feeding line requirement that is no longer an issue in the time-domain.

3.3 HIGH FREQUENCY MEASUREMENT TECHNIQUES

This section will present the methodology utilized to characterize the micromachined circuits presented in this work. Several approaches were investigated to evaluate the performance of the scaled model version in a test fixture configuration and the micromachined version that has been characterized using on-wafer probing techniques. The test set-up and required calibration techniques will be presented in the next section for the planar circuits shown in Chapter 4. In general this approach is used for all passive circuit characterization measurements unless otherwise indicated. The primary objective of this section is to give the reader an understanding of the testing environment employed in this work and comment on the advantages and limitations posed in this measurement system that may lead to error within the measurements.

3.3.1 Test Set-Up and Measurement Probes

Characterization of planar circuits was originally began via test fixtures using coaxial feeds for microstrip based designs. This requires transitions that have a minimum return loss of -10 dB in order to effectively calibrate the connector out of the measurement system. One of the first coaxial connectors used in the measurement of planar lines is the Eisenhart connector [45]. While there are number of connector types available today for microstrip based designs, connectors for coplanar waveguide based designs are somewhat limited. The low frequency microwave model used in this work uses a fixture that requires a coaxial to coplanar waveguide transition. Flange mount tabs by Omni Spectra were used, however, modifications were necessary since this is traditionally a microstrip connector. Brass tabs were attached to the outer ground of the flange and offered the contact point for the grounding from the system to the planar circuit upper ground plane. A description is given in Chapter 4.2.2 for the modified connector with a illustration in Figure 4.2. This required modification limited the repeatability of the measurement since each connector is no longer identical, there the calibration of the system was very difficult.

Effective calibrations assume that the measurement system has identical transitions, which is not possible since each tab is modified separately. Therefore, one source of error due to the connector is associated with connector repeatability. Since this approach, worked very well for frequencies below 15 GHz. However, above 15 GHz parasitic effects and multi-moding were more prevalent resulting in failure to calibrate effectively in the higher band. Since this model, represents the predecessor of future high frequency measurements that go up to 40 GHz, this approach was not feasible and stimulated the use of on-wafer probing measurements.

Accurate characterization of planar circuits can be achieved from dc to W-band [43-44] using state of the art on-wafer probing techniques. In the past, probe stations were primarily used for dc testing, however, in recent years they are also used for high frequency testing as well. As the trend to develop higher frequency devices using MMIC processing techniques increases, a more flexible approach is required to take advantage of coplanar waveguide features for planar signal lines. Earlier high frequency probe designs were primarily based coplanar waveguides geometries that are printed on alumina substrates and mounted in the holder. Recently, a variety of designs are being that transition from air coaxial to air coplanar waveguide excitation.

In the diagram shown in Figure 3.4, the measurement set-up of the circuit is based on an HP Network Analyzer that is connected to an on-wafer probe station. The network analyzer operates up to 40 GHz and consists of a HP 83624A Synthesized Sweeper, HP 8516A S-parameter Test Set and HP 8510 processor while the on-wafer probing station is an Alessi REL- 4300 with Cascade Microtech ground-signal-ground (GSG) probes. The pitch, defined as the separation between the signal line and the ground plane of the coplanar GSG probes, of the probes used in this work are 150, 200, and 250 microns. Since the probes are delicate, it is imperative that the cables connecting the probes to the measurement system. In Figure 3.5 , an illustration of the two types of probes currently available for high frequency design are shown. Note that the structure of each probe design has sig-

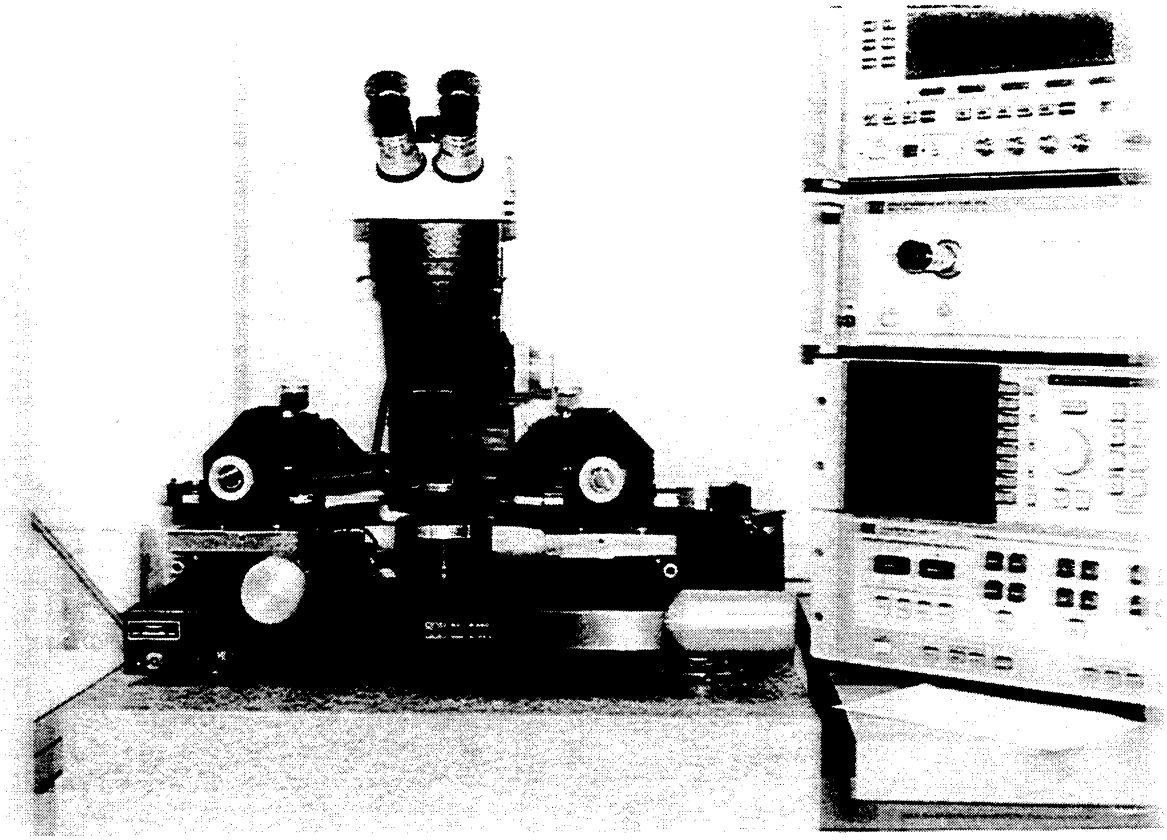


Figure 3.4 Photograph of the Network Analyzer and Probe Station.

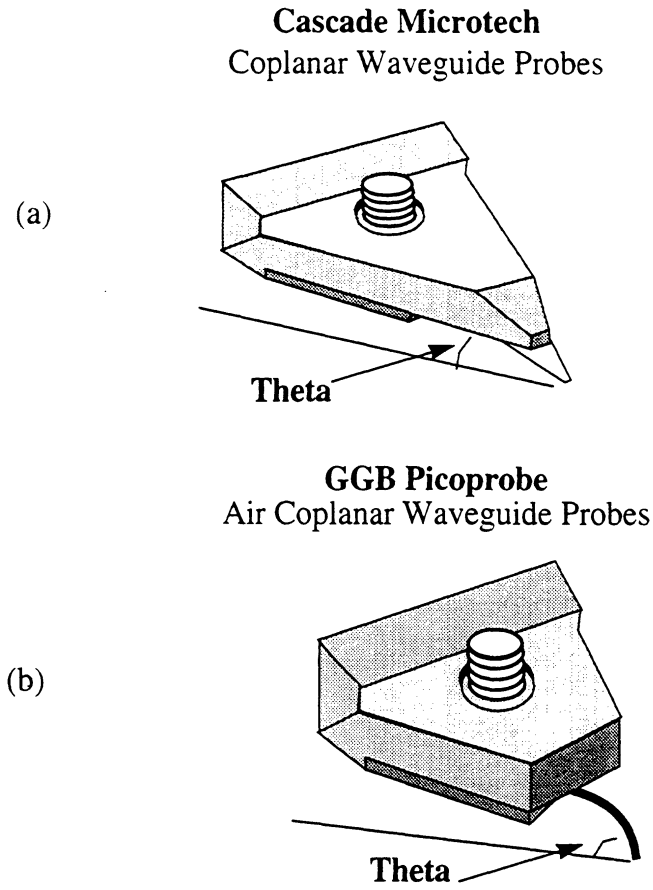


Figure 3.5 Cascade Microtech and GGB High Frequency Coplanar Waveguide On-Wafer Probes. (a) Model WPH-150-K with Theta of 11 degrees and probe widest width, w= 4 mm (b) Model 40A-GSG-150-C with Theta of 30 degrees and probe widest width, w= 1.5 mm.

nificant influence on the type of probe window design used in the shielded structures and must be decided prior to design and testing.

3.3.2 Calibration Methods

Evaluation of element performance occurs through the measurement of individual devices or circuits which are then modelled using appropriate software analysis tools. Unlike low frequency lumped element designs whose evaluations depend on voltage and

current measurements, planar circuits are typically evaluated in terms of scattering parameters. These parameters are transformed to an equivalent impedance matrix that varies with frequency and describes the electrical behavior of an unknown device under test (DUT). Circuit parameters are then extracted to develop an equivalent model that can be used to incorporate a specific planar circuit into a system level design. Therefore, accurate determination of the circuit response is important in order to develop accurate equivalent circuit models of planar lines and discontinuities. These parameters are the basis of all circuit design such as filters, couplers, and mixers.

Accurate characterization needs to remove all excess losses caused by cables and connectors that interface the DUT with the measurement system. Typically these losses are quite large in comparison to the signal response of many circuits and require very accurate calibration methods to extract the DUT response from the system response. This is a great challenge for planar circuits characterization, since the calibration techniques are more complex and less standard.

Several calibration techniques exist for automatic network analyzer (ANA) systems and the approach is typically characterized as one or two tier de-embedding techniques. The one tier method, primarily used in this work, allows the measurement reference plane to be transferred from a known location at test set interface to a predetermined location. The two tier method, decomposes the procedure into two preliminary calibrations and shifts the reference plane from ANA test set interface to the cable connector and then to the final desired location.

Resident on the network analyzer is calibration software for one-port and full two-port circuits that require the use of known standards, such as a short, open, load (50 ohm) and thru. This method, known as SOLT, is used for two- port devices and shifts the reference plane to a known location at the end of the test cables. Since the test set-up contains various connections between network analyzer and the DUT, any loss due to cables, connector transitions, or known discontinuities must be evaluated and extracted in order to accu-

rately characterize the DUT. In essence, the SOLT method effectively compensates for the cable and connector effects by mathematically determining calibration coefficients that provide the appropriate phase shift and attenuation in the scattering parameters to a reference plane at the end of the connectors.

During planar circuit characterization the SOLT calibration can be applied to the coaxial system and the planar circuit as long as known standards are used. Circuits that are non-coaxial are usually mounted on a test fixture and require other methods to characterized the effects associated with this transition probe to circuit transition. A variety of methods are available for probe tip calibration and several are employed here for the on-wafer testing of the micromachined circuits. For reference planes at the probe tips the methods includes an equivalent (SOLT) approach, line-reflect-match (LRM), line-reflect-line (LRL) and thru-reflect-line (TRL) [46-47]. The first two are very exact for evaluating the probe parameters since they are based on known standards and the load or match is usually a trimmed using laser techniques to a 50 ohm thin film resistor. The latter two techniques are useful for measuring circuits that have unknown standard characteristics and establishes a normalized reference impedance based on this unknown value. The SOLT and the TRL standards will be incorporated in these circuit designs for the characterization of the micromachined circuits.

The TRL calibration requires three lines that represent a thru, reflect, and line. All have exactly the same basic physical geometry which includes upper and/or lower shielding that is identical to those in the DUT circuit. A two tier de-embedding technique is used for the coaxial fed machine-milled circuits while a one tier de-embedding technique is used for most of the on-wafer measurements of the micromachined circuits. In the shielded circuit case, the reference plane is typically established inside the shielded section of transmission line so that the edge effects of the shield have been calibrated out. Characterization of all transitions between the test set interface and the DUT have been

accounted for and extracted such that the measurement response represents the specific line or discontinuity (Figure 3.6).

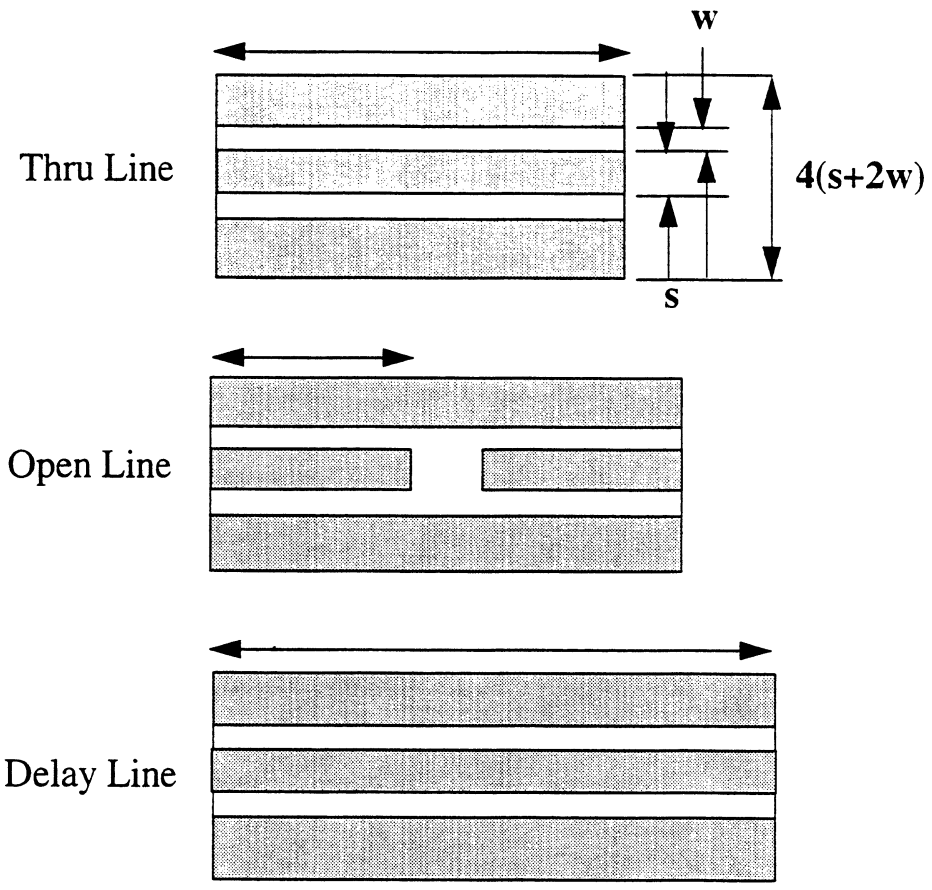


Figure 3.6 Thru-Reflect-Line calibration standards for coplanar waveguide based circuit designs.

The data presented in the next chapter are for micromachined circuits that are partially or completely shielded. Characterization of this packaging concept occurred in two parts; first, the upper shielded circuits are evaluated where the cavities are mounted on coplanar waveguide based (CPW) circuits and the entire structure is then placed on a duroid substrate with ε_r = 2.2 and thickness of 3.175 mm. The duroid substrate provides isolation between the probe station chuck and test circuit which prevents parallel plate waveguide

mode formation under ground planes of the CPW and the wafer chuck. Next, since SDIE analysis tools are available for predefined circuit geometries, several variations are implemented to evaluate the performance of the micromachined circuit and the microwave modelled one. The second part of this investigation deals with the characterization of completely shielded circuits and again various circuit geometries are investigated. Since the circuits under test are isolated from the outside environment with type of shielding, they are placed directly onto the probe station wafer chuck in the measurement set-up. The FDTD method is employed in the analysis since this provides more flexibility in evaluating the cross-section of the structure and the specific planar circuit design.

The TRL calibration technique that is provided by the HP ANA has been applied to the micromachined circuit topologies. In instances where the line a particular circuit is being evaluated with the feedlines included, the SOLT calibration has been used on the alumina calibration substrate that is used with the specific probes. The particular probes requires a specific calibration substrate which can typically be obtained from the manufacturer. This substrate and probe combination are equivalent to the calibration kit of very accurate well known standards used for coaxial systems. Without this substrate, each geometry will require TRL or equivalent calibration standards to be included on each substrate and the performance of the circuits will rely heavily on having appropriately designed calibration circuits. From experience, this is an easy step to include when the circuits are simple as in the ones included above, however, if there are several transitions and unique geometries to be considered, designing calibration standards can be as difficult as designing a suitable test fixture. In addition, without a good set of calibration standards, the accuracy of the DUT measurement is questionable.

The accuracy of high frequency measurements has been extensively researched in the past few years since the ANA became available in the mid seventies. The accuracy of planar circuit evaluation for passive and active elements is critical since circuit design models depend on the ability to evaluate the device independent of the testing environment. The

primary organization that has focused specifically on enhanced methods of calibration are at the National Institute of Standards Technology (NIST) by researchers Marks and Williams [48-52]. This published software is available for public use and is considered one of the most accurate software tools available for evaluating high performance planar transmission lines. Many of the earlier versions are useful for circuits implemented on low loss or nearly lossless substrates such as alumina, gallium arsenide, or membranes materials. There are also versions of the software, that can handle lossy substrates such as silicon and were not available for public use outside of the consortium at the time of this work. Currently, this software is available with the calibration probes described above from Cascade Microtech for high frequency planar circuit characterization.

3.3.3 Measurement Errors

This section presents a discussion on the circuit characterization by addressing measurement error, accuracy and precision for the results obtained herein. The characterization of a circuit is influenced by three techniques: fabrication, measurement, and theoretical. The discussion proceeding will be primarily qualitative since an extensive error analysis study has not been included in this work. By definition, measurement error is the difference between the true or best accepted value of some quantity and the measured value. A measurement is accurate when the error is small, therefore the accuracy refers to a comparison of the measured and accepted, or "true," value. Precision, on the other hand, is a measure of the repeatability of a series of data points taken in the measurement of some quantity [53].

The fabrication process used has been described extensively in Chapter 2. The associated errors exist in the mask making procedure and actual fabrication. Of the two, the mask making accounts for the largest amount of inaccuracy since the quality of the mask effectively determines the accuracy of design reproduction. Reductions ranged from 17 to 32 times; however, the masks were at 25 times reductions on average in order to produce

the largest number of circuits on a single quarter of a 3 inch wafer. Higher reduction capability is available that yields accurate features as small as 10 microns. The number of circuits per mask is limited, however, to a single design for circuits that perform in the 10 to 30 GHz. The accuracy ranges from 95% for dimensions larger than 100 microns to 78% for dimensions in the 10 to 15 micron range. The mask making process is based on optical transfer of the rubylith image to a glass mask. Distortion at the edges of the lightboard also introduce variation across the circuit dimensions depending on the location of the circuit on the rubylith mask. The second source of error occurs in the process phase. Photolithography contributed less than 5% error for features above 200 microns, and about 13% for those less than 15 microns. However, these effects can be compounded when several layer are required to fabricate the circuit. The circuits of interest have a large contrast between the x and y dimensions since the planar lines have lengths on the order of millimeters and slot or line widths as small as 20 microns. As a result, the smallest feature realized in this work using the given rubylith-CAD system is 20 microns for 25 times reduction.

The errors associated with the measurement system can be described as systematic or random. Systematic effects such as leakage, test port mismatch and frequency response, etc., produce uncertainties in the measured response. Random errors, on the other hand, are unpredictable and generally very small and caused by electrical noise, leakage currents and drift. Automatic vector network analyzers today are very accurate instruments since a calibration model based on a 12-term error model is used to greatly reduce the sources of systematic errors. Previously, external calibration models were discussed from the National Institute of Standards and Technology. The largest contributor to measurement error in the set-up is connector repeatability and error associated with improper calibration. Precision calibration standards exist for coaxial systems that allow for the use of Full 2-Port calibrations. Such standards are not available for non-coaxial systems, therefore the design of appropriate non-coaxial standards has a significant impact on the accuracy of a calibration. In this work, the low frequency models test fixture uses a microstrip connec-

tor, therefore, issues of repeatability were of concern. Additionally, since this design required modifications to the microstrip connector to accommodate coplanar waveguide transmission lines, connector similarity and repeatability have a role in the measurement error. The response was limited to 15 GHz maximum as the parasitics and excitation of higher order modes tend to effect the ability to calibrate the system well repeatably. This motivated the measurement of the micromachined circuits using on-wafer probing techniques which provides excellent repeatability to planar circuits of coplanar waveguide type. In addition, the on-wafer probing techniques utilize well-establish calibration techniques that are based on the 12-term error model.

The theoretical models employed can be divided into quasi-static and full-wave analysis techniques. The latter represents the most accurate approach to model the electromagnetic behavior of microwave circuits. The source of error using the SDIE and FDTD methods can be identified by the approximations made to the actual test circuit dimensions, dielectric composition, and geometry. For example, the programs are designed to handle integer multiples of specific dimensions, which in reality are not always consistent with the final dimensions. The trade-off comes in knowing which parameter is less sensitive to this inaccuracy. Since the computational time and space can be a limiting factor, compromises must be made to maximize the power of the particular method while also maintaining the integrity of the test circuit. This is especially true when determining the smaller dimensions of 10 microns in the same direction with lengths of 433 microns. To get the finer resolution implies that the size of computational matrices is very large. Secondly, the packaged circuits evaluated in this work have angled sidewalls, however the models have assumed vertical sidewalls. In particular, SDIE programs are geometry specific and require that the upper and lower cavity also have similar widths even though in reality there may as much as a 400 micron difference between the two cavity regions. Lastly, all of the circuits have approximately a 1.2 micron thick silicon dioxide dielectric that has not been accounted for in any of the models. The FDTD provided the most flexi-

ble option since it is geometry independent and many of the results gave similar trends as the measured ones except for a frequency shift, which are due to a combination of the issues previously described above.

In summary, there are many contributions to the differences observed between measured results and modelled ones. These differences can be decomposed into the fabrication, measurement and modelling errors. Each technique contributes a certain amount to the overall inaccuracy of the data, however, a good estimation of the expected response is achievable through the modelling of designs prior to testing. The testing and modelling can therefore serve as a dual validation tool as long as the assumptions of the models and test circuit are identified.

3.4 SUMMARY

The discussion in this chapter has established a foundation for the reader on the various measurement phases used to evaluate micromachined circuits. Many of the planar circuits are evaluated on the probe station, however, some designs require very specific testing set-ups. These special test circuits will be described in Chapter 2. The types of resources available to evaluate micromachined circuits will become increasingly important. For this work, the theoretical tools and measurement tools represent state of the art for this time. With increasing interest in the development of the high frequency micromachined circuits, there will be more opportunities to develop or modify techniques from other areas that can function as excellent tools to determine the electrical behavior and characteristics of these circuits.

CHAPTER IV

CHARACTERIZATION OF MICROMACHINED PACKAGES

4.1 INTRODUCTION

Systems such as radar and satellite communications, increasingly rely upon development of high frequency planar circuits that have optimum performance at microwave and millimeter-wave frequencies. Hybrid or monolithic microwave integrated circuits have had a tremendous impact on the development of high performance circuits. Several of the advantages observed in a single circuit design having broadband performance include lower cost, smaller size and weight, enhanced circuit design flexibility and in addition to multi-function operations. The hybrid circuits, known as microwave integrated circuits (MICs), can be categorized by the transmission line media or the active device. Some of the advantages include improved performance compared to traditional low frequency design methods, lighter weight compared to conventional waveguiding systems, and reduced cost due to the fabrication processes [55]. However, hybrid MICs typically require wire bonds for electrical connections of the various components in the system which is problematic in large system applications such as spaceborne phased arrays [56]. The above concern enhanced the development and use of monolithic MICs which offer the advantages of wire bond elimination and large volume production of identical chip components. Therefore by the eighties, two options existed for high performance circuits, MICs which include individual passive or active elements that are connected using hybrid mounting techniques and MMICs which provide monolithic integration of active and pas-

sive elements on the surface of semi-insulating materials to improve the circuit performance [61].

Passive transmission lines, such as microstrip, stripline, slotline, coupled strips, and coplanar waveguide (CPW), have provided the circuit designer with an extensive library to achieve high performance planar circuits that can be implemented into a variety of design configurations. Since the mid 1960's microstrip [57-58] and stripline [58-59] configurations have been explored and are commonly utilized in today's MIC and MMIC designs. These technologies, however, are more difficult for active device integration, either in hybrid or monolithic form since they require ground and signal line connections between the various configurations. As communication system design requirements increase in frequency, high performance planar circuit topologies are required for performance needs at millimeter and submillimeter-wave frequencies.

In response to the problems associated with passive element and active device integration, coplanar waveguide began to gain more popularity. It was first developed and practically implemented in the late 1960's by C. P. Wen [61]. The main problem that limited its use in earlier work arose from higher losses observed than microstrip line. However, the need to provide easy solutions for the integration of multiple components which operate with varying functions quickly outweighed these concerns. Coplanar waveguide, having both the ground and signal line on the same surface, inherently offers the feasibility of active device integration into monolithic designs to improve the overall planar circuit performance. In the last decade basic research in this area has focused on extending the planar circuit design library to include passive components such as filters, couplers, and switches that are based on this technology, in addition to, exploring monolithic system development in the form of receivers and mixers that operate in the submillimeter wave range [23],[61].

Even though much effort has been focused on the integration and improvement of passive circuit and active device performance, packaging issues are at the forefront of electronic research topics and have been found to significantly influence the overall

performance of a high frequency circuit design. Experts in the fields of device and component development began to realize that the packaging area was progressing at a much slower rate than the devices themselves [39]. As a result, many problems such as parasitic coupling and package resonances have been observed in diagnostic testing of planar circuits at these frequencies and are being attributed to the close proximity in the layout and package housing size. Circuit designs for microwave and millimeter-wave frequencies that have monolithically integrated shielding packages (micropackage) are being explored. The micropackage is integrated using silicon micromachining techniques from MEMs community. This type of package topology has not been explored extensively from a experimental perspective even though a large body of information exists theoretically and experimentally for planar circuits.

This dissertation explores a high frequency package design that is based on a combination of silicon micromachining and MMIC processing techniques for high frequency circuit design. The advantage of this approach results in the ability for the first time to resolve unwanted physical electromagnetic phenomena in planar circuits that result in novel planar topologies that operate with superior performance to conventional planar technologies.

The final application of silicon micromachining techniques to traditional high frequency planar circuit designs must addresses several issues. First, this novel package must utilize fabrication techniques that are compatible with standard MIC and MMIC processes; and the topology must be testable using current state of the art high frequency measurement techniques. Second, the package effects must be evaluated on a variety to basic geometries that represent fundamental elements to high frequency passive component design. Lastly, this structure must accommodate a variety of configurations which may extend in linear and nonlinear directions as well as handle single or multiple inputs paths to a single line within the circuit and layout requirements. This variation in planar

line shapes and directions require "conformal" packages to provide basic understanding of the shielding effects introduced by packaging approach.

In this chapter, the characterization of micromachined circuits using the micropackaging technology described in Chapter 2 is presented. The micropackaged circuits are classified into three main categories: (1) partially shielded, (2) completely shielded or self-packaged, and (3) conformally packaged circuits. In each category the discussion begins with the motivation of the work followed by a description of the design objectives and testing requirements. The last part section will be concluded with a brief summary of the findings. Circuit performance of basic elements is presented for a variety of topologies and comparisons to either theoretically modelled data or measured unshielded (open) circuits having similar geometries are shown. Initial investigation of the upper shielded circuit begins with the presentation of a microwave model and establishes the basis for the first micromachined upper shielded package. The evaluation of the completely shielded or self-packaged circuit is obtained through basic transmission line characterization shown for half and completely shielded configurations. Lastly, illustration of conformal packages are shown which extend the basic idea of self-packaged circuits into more complex circuit designs.

4.2 MICROMACHINED PACKAGE AND CIRCUIT EVALUATION

Structures residing on continuous substrates and in open environments exhibit poor electrical performance due to free-space radiation and substrate mode excitation. Shielded structures have the added problem of package resonances. The open environment described refers to circuits which are printed on a dielectric substrate and are free to radiate into space. The term "shielded geometries" means circuits which may be partially or completely shielded through cavities in the upper and/or lower regions. Since substrate modes occur in the dielectric substrate, the introduction of physical alterations to the substrate itself can result in elimination of these parasitic waves and an improvement of cir-

cuit performance. The following sections outline the steps required to design circuits that reside in partially or completely shielded environments and extensively describes the silicon (Si) fabrication processes required for their development.

4.2.1 Micromachined Circuit Modelling Issues

While the geometrical parameters are determined to provide the desired electrical response, the issue of package resonances and substrate mode excitation are also being addressed. As has been described in the literature [40-41], electrical packages can greatly affect circuit performance either through package resonances or through proximity coupling. The first effect is mostly related to the dimensions of the package while the latter is due to cross-coupling of neighboring circuits. These two mechanisms require contradicting measures for correction or elimination and this leads to design trade-offs. Ideally, a given circuit has an optimum package size that is small enough to eliminate resonances within the range of operating frequencies and that is physically far enough from the circuitry so that it does not interfere with the circuit's electrical performance. Although circuits in open environments do not encounter these problems, they are prone to parasitic radiation losses which is mostly associated with the excitation of substrate modes. Since the excitation of these modes is mostly dependent on the operating frequency and the physical thickness of the substrate, careful layout configurations in less dense circuit environments can sometimes reduce such parasitic radiation, provided there is flexibility in circuit placement. In practical applications, however, circuit requirements greatly limit the flexibility in rearranging the location of the various circuit components such that any layout modifications, at best, can only weakly reduce such parasitic loss [42].

During the characterization, preliminary findings indicate that substrate modifications alone may have a substantial impact on substrate mode excitation. Since the late seventies researchers have been aware of these problems in hybrid and monolithic planar circuit design, however, the technology at that time could not provide alternative solutions to

reduce the substrate mode excitation. Recent advances in silicon micromachining techniques, however, allow for unique, yet simple practical solutions. In the development of micropackages, dimensions can be chosen simply by using waveguide and cavity models to predict geometrical dimensions that avoid unwanted resonances. In addition, the shape of the cavity can be designed so that it follows the circuit and does not physically affect its performance. For open circuits, substrate modifications using micromachining can be implemented to eliminate these unwanted substrate modes entirely, resulting in improved circuit performance.

4.2.2 Existing Machine-Milled Shielded Circuits

4.2.2.a Motivation

Planar line structures which have a metallic shielding over the conducting line and very thin substrates or no substrate could be used to provide novel generic shapes that offer improved circuit performance [26]. Geometries of this form are beneficial to high frequency circuit and array applications operating at frequencies ranging from Ka-Band to the terahertz region. Since the parasitic radiation and other inherent loss mechanisms found in traditional planar lines are especially detrimental to the electrical response of circuits at higher frequencies, novel geometries that offer solutions to these problems are warranted. From the analysis, circuits with coplanar waveguide lines and shielding on one side of the circuit surface tend to radiate less than the conventional coplanar waveguide (CPW) due to improved field confinement into the substrate.

To study this behavior experimentally, circuits on unaltered substrates have coplanar-type lines with a cavity mounted over the circuit surface. Geometrically, this shielded circuit can be made so the cavity structure totally shields one side of the inner conductor strip to form a microcavity (Figure 4.1). This geometry establishes the basis for studying the effects of the shielding package on planar circuits. This structure can also be made mono-

lithically by incorporating dielectric etching and metal deposition techniques as well as silicon micromachining technology to form the cavity region. Since theoretically a number of advantages have been shown in [12] for the shielded structure, experimental characterization of this structure is merited to validate the reduction in radiation loss and electromagnetic interference. In addition, the potential to integrate this type of structure with existing antennas of microstrip and aperture type [62] are promising. Section 4.2.2.b will focus on a simple microwave model characterization that is based on a machine-milled upper cavity mounted over coplanar waveguide circuits.

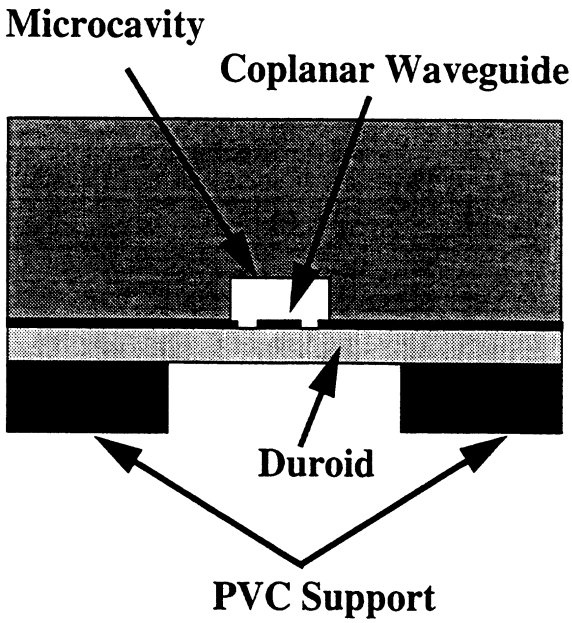


Figure 4.1 Microwave Shielded Transmission Line Structure made of an aluminum block mounted over the planar circuit on duroid substrate having $\varepsilon_r = 2.2$. The substrate is supported by a PVC block that has been cored out in the middle.

4.2.2.b Circuit Design and Fabrication Considerations

The first step in studying package effects requires evaluating the upper shielding cavity in the presence of standard circuit designs. An understanding of these mechanisms provides useful information for high frequency applications. To characterize the performance of circuits for higher frequency applications (in some cases even to sub-millimeter-wave frequencies), a low frequency model is first evaluated. In high frequency measurements, scattering parameters are used to evaluate the performance of a circuit and can be converted with an appropriate model to lumped element equivalence. Experimentally, a scaled model of the shielded line is measured to determine the circuit performance and the total loss of the system is found. The electrical response and associated losses can be scaled linearly to high frequencies except for those associated with the conductor. However, the amount of conductor loss in coplanar waveguide lines can be obtained from a number of references in the literature for experimental and theoretical data. With the additional design parameters provided by the shielding cavity to the planar line, a wide variety of characteristic impedances can be obtained depending on the specific cavity and the planar geometry dimensions. The upper shielding offers an alternative to airbridges or via holes, since the center conducting line is in such close proximity to the microcavity and the ground planes of the line are tied together via the shielding cavity. The result is radiation loss that is significantly lower than those of the conventional CPW or microstrip mainly due to the microcavity enclosure.

The microwave model of the partially-shielded circuit consist of a coplanar waveguide based transmission line circuit that has an aluminum cavity mounted over the center conducting line with the bottom of the substrate elevated on a cored PVC non-conducting block. This structure is used to develop an understanding of the nature of a cavity structure on a planar transmission line. The choice of coplanar waveguide is due to the inherit advantages of its physical properties for mounting active devices and ease of probe measurements. In order to characterize the behavior of the upper shielded configuration, cir-

cuit parameters must be obtained that correspond to desired the characteristic impedances. These are calculated using quasi-static models to generate the range of impedance values available for the design parameters [26].

The design criteria for the fixture requires matching of the fields at the discontinuity between coaxial excitation and transmission line. Thus, the resulting characterization is a three step process. First, various transitions are evaluated to provide maximum excitation to the line. Second, the circuits are evaluated to determine the minimum thickness and dielectric constant of the substrate which are feasible for accurate characterization of the line. Third, the results of the above processes are combined to evaluate the overall performance of the line. The test fixture is designed so that a microcavity encloses the conducting line. This cavity is machine-milled into an aluminum block and then a conducting line, which is printed on the substrate, is centered and aligned to the cavity. Center positioning of the conducting line ensures excitation of the CPW mode (odd mode) and suppression of the slotline mode (even mode) in the line. The back of the circuit substrate is then supported by a cored non-conducting PVC block which offers mechanical strength to the substrate surface and support for the coaxial connectors. After mounting the circuit, the connectors are placed on the circuit and secured for measurement.

The circuits described in this work are designed for 10-15 GHz operation on a duroid with dielectric constant, ε_r, of 2.2 and substrate thickness of 0.762 mm. While thinner substrates have been tested, flexibility in the dielectric backing resulted in poor ground plane contact. This leads to leakage and poor measurement repeatability. Ground planes are included on the circuit surface to ensure contact of the cavity ground to the CPW ground. While this enhanced the performance, it is observed that a substrate thickness of 0.762 mm provides the most repeatable measurements for characterization since the supporting PVC material is cored in the center. To ensure excitation of the CPW mode, the ground planes of the CPW line are extended inside the cavity. Connections between the coaxial line and the CPW line are obtained by field matching rather than impedance

matching. It is observed that a CPW line of 72 ohms matches optimally to coaxial line of 50 ohms [63]. Implementing the above considerations results in a fixture that is easily characterized during calibration.

The planar circuits are fabricated using standard photolithography and wet etching techniques employed for the duroid laminate substrates. Initially, the cavity is represented by an aluminum block that is milled to the desired depth and width corresponding to a 50 ohm input impedance. In this case a 50 ohm line is achieved by having a cavity width, w_c, and height, h_c, dimensions of 2.5 mm and 1.27 mm, respectively with CPW slot, w, and conductor, s, dimensions of 0.5 mm and 1.52 mm. Since the circuits are coplanar waveguide, excitation is obtained using the Omni Spectra flange mount tab coaxial connectors. These connectors have a Teflon diameter of 187 mils and a tab width of 1.52 mm and are designed to be mounted in a fixture environment. Since these connectors are typically used in microstrip designs, modifications have been incorporated in order to maintain electrical continuity between the system ground through the connector and the planar circuit ground of the coplanar waveguide. Figure 4.2, shows how brass tabs have been sol-

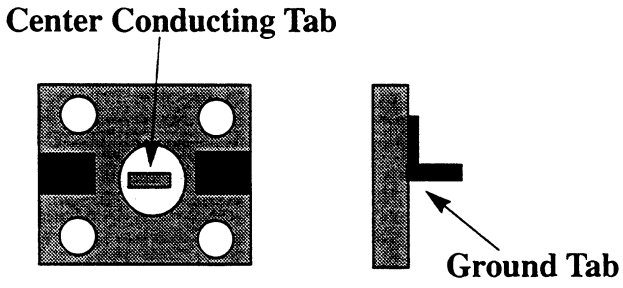


Figure 4.2 Illustration of the modified conducting tab to connect the coaxial connector to the coplanar waveguide transmission line.

dered to the gold-plated connector at a 90 degree angles to provide a physical connection

between the circuit and the connector. Alignment pins are also used to provide appropriate alignment between the three layers of the aluminum cavity, the circuit surface, and the PVC mount (Figure 4.3) Once the mount has been attached, the center conductor tabs are

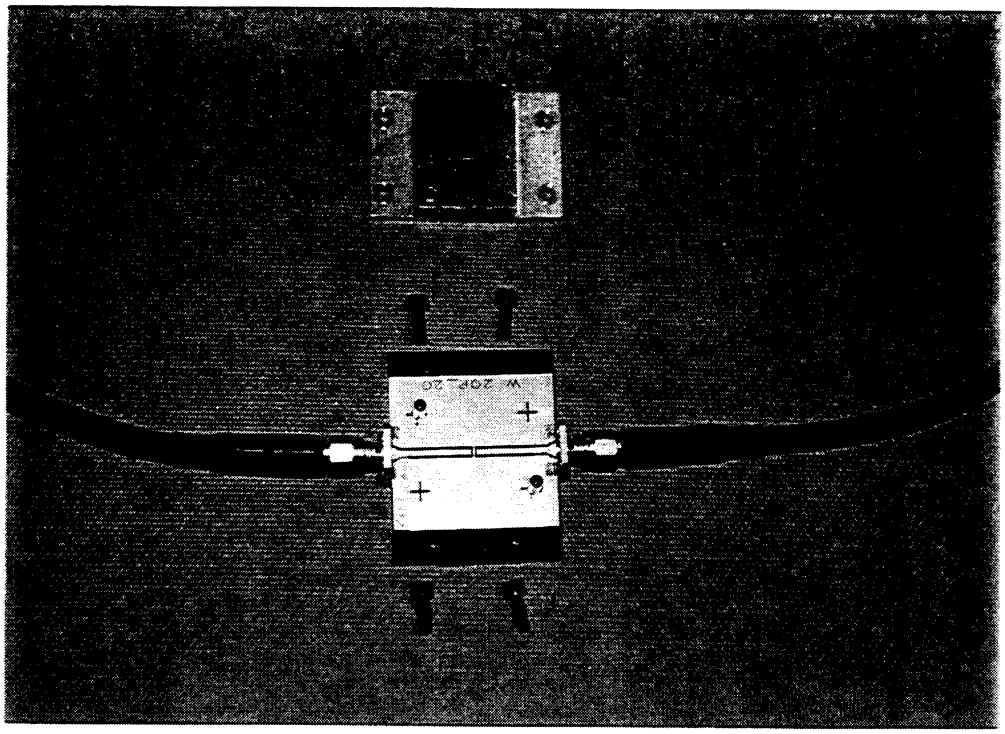


Figure 4.3 Photograph of the Microwave Model of the Half Shielded Transmission Line

brought into contact with the circuit and silver paint is applied to ensure good electrical contact.

4.2.2.c Microwave Model Measurements

Characterization of the fixture and discontinuities are obtained using the Thru-Reflect-Line (TRL) calibration technique which eliminates the effects of the connector discontinuities from the measured data. Since precision calibration standards of the half shielded circuits are not standard and readily available, a non-coaxial de-embedding technique is utilized to characterize the line [64-65]. In a two-tier de-embedding technique is employed, the ANA is first calibrated using precision coaxial standards. The test fixture is then calibrated with appropriate planar standards that offer field transitions between the coaxial connector and the linearly tapered input planar line of the specific line.

Experimentally, the propagation constant of the line is obtained from the measurement of phase information of a long delay line (Figure 4.4). For the characterization of disconti-

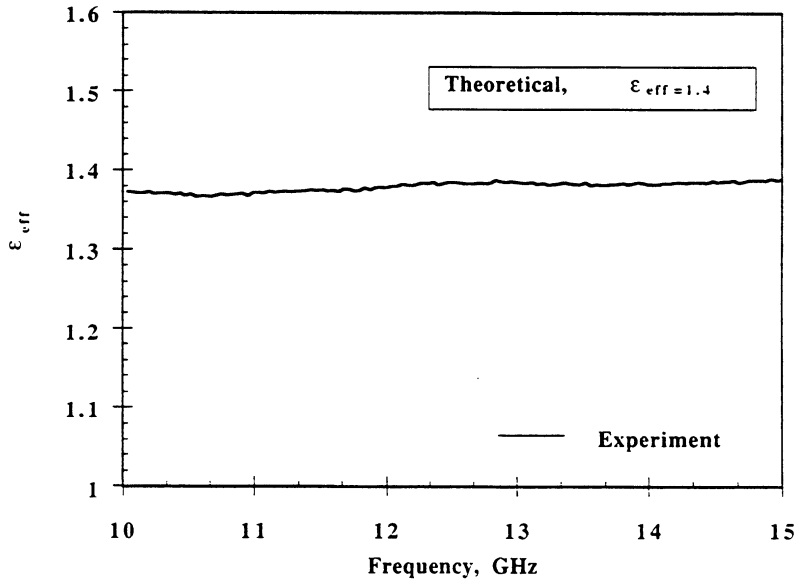


Figure 4.4 Effective Dielectric Constant of the Microshield Microwave Model. Graphs shows the calculated effective dielectric constant which was determined theoretically to be 1.4.

nuity effects, a two-coupled open-end line is measured and scattering parameters are shown in Figure 4.5 for the magnitude and phase of the circuit. The calculated radiation loss factor is shown in Figure 4.6. In general the comparison between theory and experiment is in very good and the ripple seen in the measured data is attributed mainly to the very small coupling that exist between the two slot line which intensifies the effects of connector repeatability.

4.2.2.d Summary and Conclusions

During the first phase of experimental characterization in this study, the results from upper shielded machine-milled circuits formed the initial groundwork for investigation of monolithic versions of the circuit. The performance thus far has indicated lower radiation compared to conventional coplanar waveguide (CPW) lines in frequency range. Since a number of difficulties can occur in achieving a good fixture design that can be accurately characterized for coplanar waveguide based circuits, future measurement data will be obtained using on-wafer probing techniques for characterization. The size and bulkiness of the aluminum cavity as well as alignment accuracy can be improved by developing a similar structure on lightweight materials such as silicon, where the cavity is formed monolithically using micromachining techniques. In the next section measured data will be presented for the cavity structure implemented in a silicon based system.

4.2.3 Micromachined "In-Line" Packaged Circuits

The characterization of partially as well as completely shielded circuits can provide a very comprehensive understanding of the effect of micropackaging on circuit performance. Results have been obtained from a theoretical and experimental investigation of a variety of circuits. These circuits are grouped into three categories: (a) circuits with upper shielding (US), (b) circuits with lower shielding (LS), and (c) circuits with complete shielding (CS) or self-packaged.

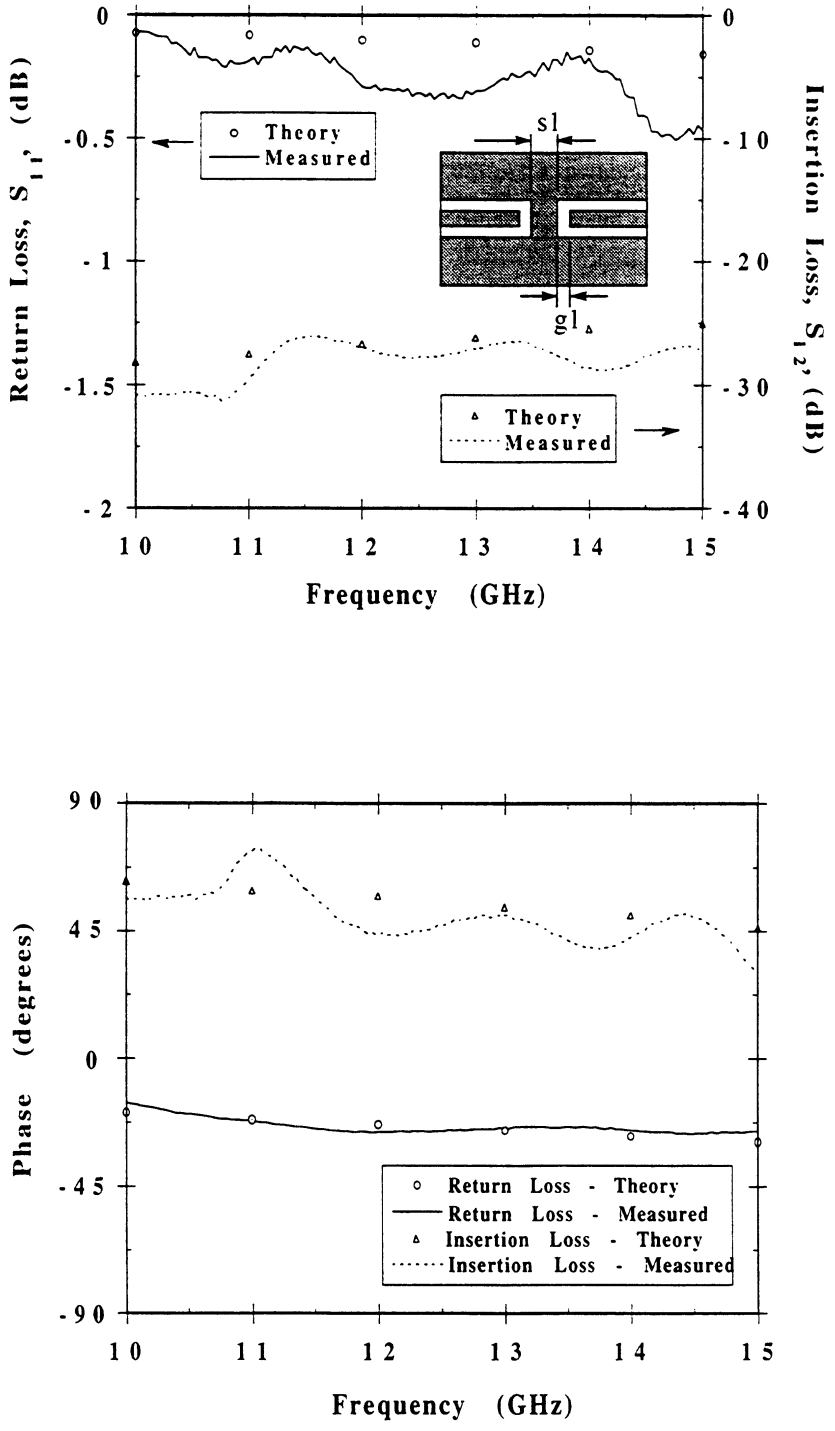


Figure 4.5 Two Coupled Open End Line Scattering Parameter Magnitude and Phase (S1=20 mils and g = 10 mils)

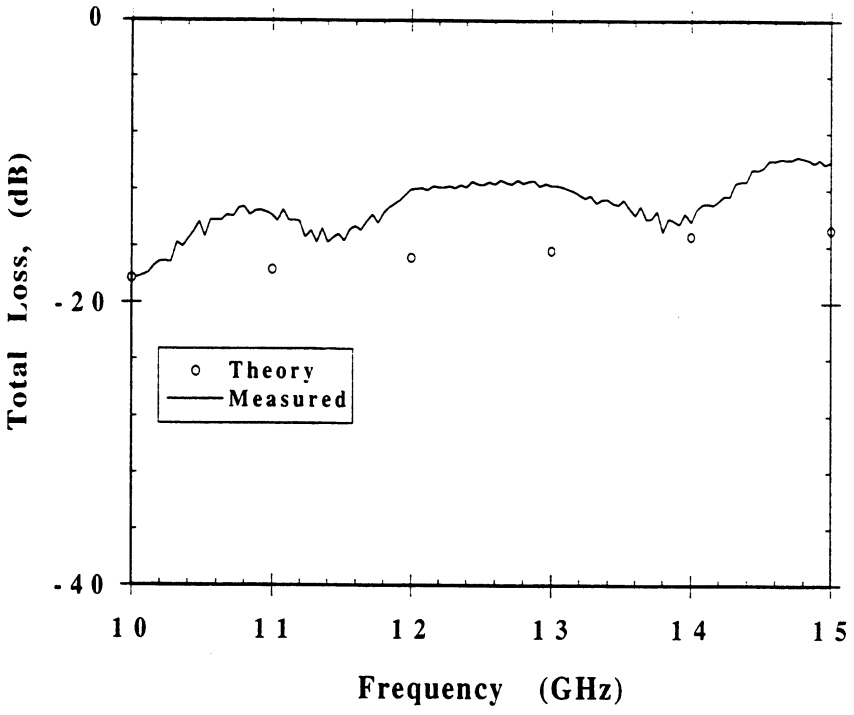
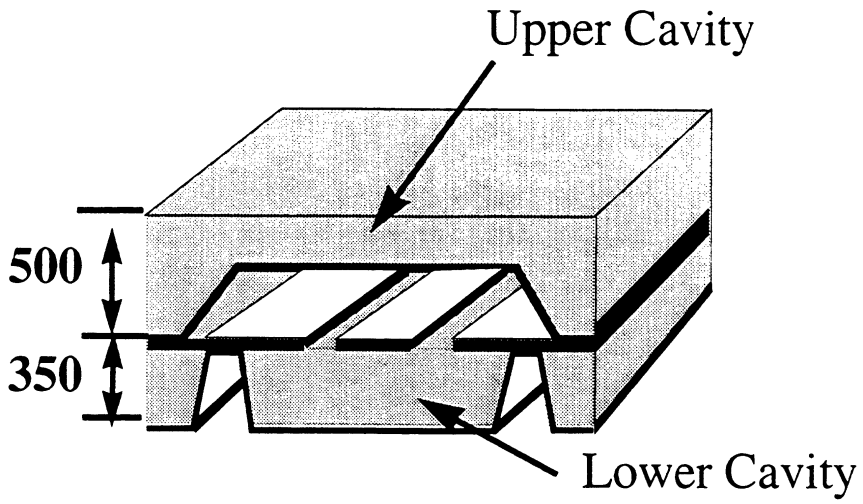


Figure 4.6 Two Coupled Open-End Line Radiation Loss Factor, (S1=20 mils and g = 10 mils)

4.2.3.a Self-Package Circuit Characterization

To accurately characterize the micromachined geometries presented, the first issue to address is the development of feeding lines that provides appropriate excitation to the circuit. Since the measurement system reference impedance is 50 ohms, the feedline dimensions are determined to meet this requirement. For the circuit components presented in this paper, the feedlines were designed using CAD tools available at the University of Michigan [66]. For the on-wafer probe station, coplanar waveguide input feedlines were designed to have a 100 micron center conductor width and a 60 micron slot width, which were determined using design equations from Ghione et. al [67]. For matching 50 ohm impedances in the shielded region, the planar line tapers outward to dimensions of 180 and

130 microns for the center conductor and slot widths, respectively. The cavity dimensions used in this case are shown in Table 4.1 of Figure 4.7.



Cavity	height	width-max	width -min
Upper	280	1200	800
Lower	350	950	500

Table 4.1 Cross Sectional Dimensions of Shielded Circuits

Figure 4.7 Dimensions for the completely shielded micropackaged circuit in microns.

The micromachined circuits in this study have several transitions incorporated to minimize the mismatch between the probe and shielded geometries (Figure 4.8). Specifically, completely shielded and partially shielded structures have similar transitions, although in one case, half of the shielded region is absent. The first transition occurs between two 50 ohm sections of grounded CPW (GCPW) where the first section (A-B) is the probe feeding pad which has a center conductor width of 100 microns and a slot width of 60 microns.

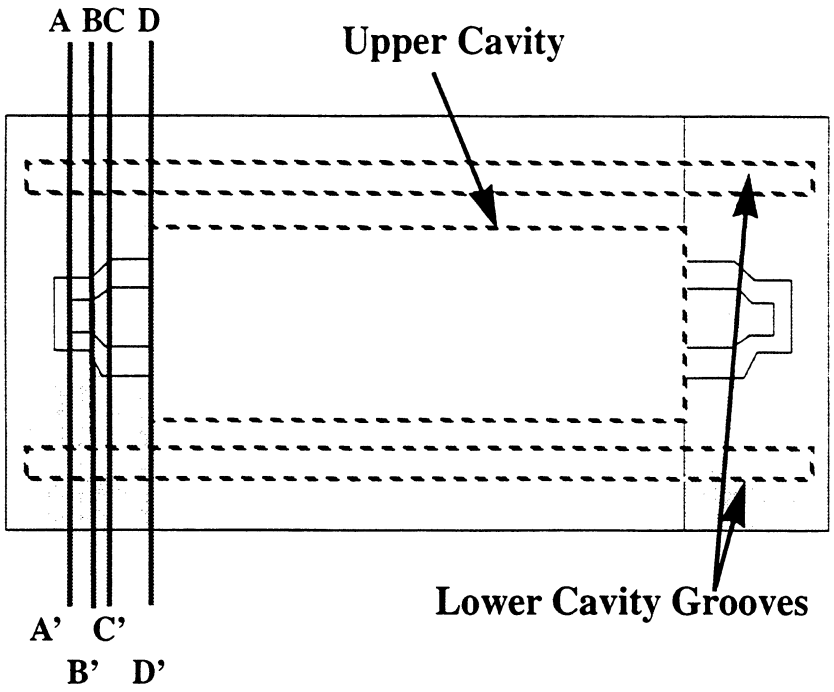


Figure 4.8 Various transitions of a completely shielded micropackaged circuit used for on-wafer robing calibration

This feedline increases linearly to a wider conductor (B-C) having a center conductor width and slot width of 180 and 130 microns, respectively. The next transition is a discontinuity at the D-D' plane that occurs between the open GCPW line and the completely shielded GCPW. At this transition the conducting line dimensions remain the same, but an upper shield has been integrated monolithically and has dimensions that are chosen such that the impedance of the line is not effected by the presence of the shield. The upper region is an air-filled cavity having a width of 1200 microns and height of 280 microns while the lower region is a dielectric-filled cavity that is designed to have a smaller width of 950 microns and height of 350 microns. The lower cavity width is the minimum required to avoid sidewall interference with the field confinement in the slots. Since the calibration reference planes are located inside this shielded region, all measured circuits have similar feedline transitions to allow use of the same calibration standard set.

The calibrated response of a through line for open CPW and upper shielded (US) CPW has been measured and results are shown on Figure 4.9. As indicated by these results, the

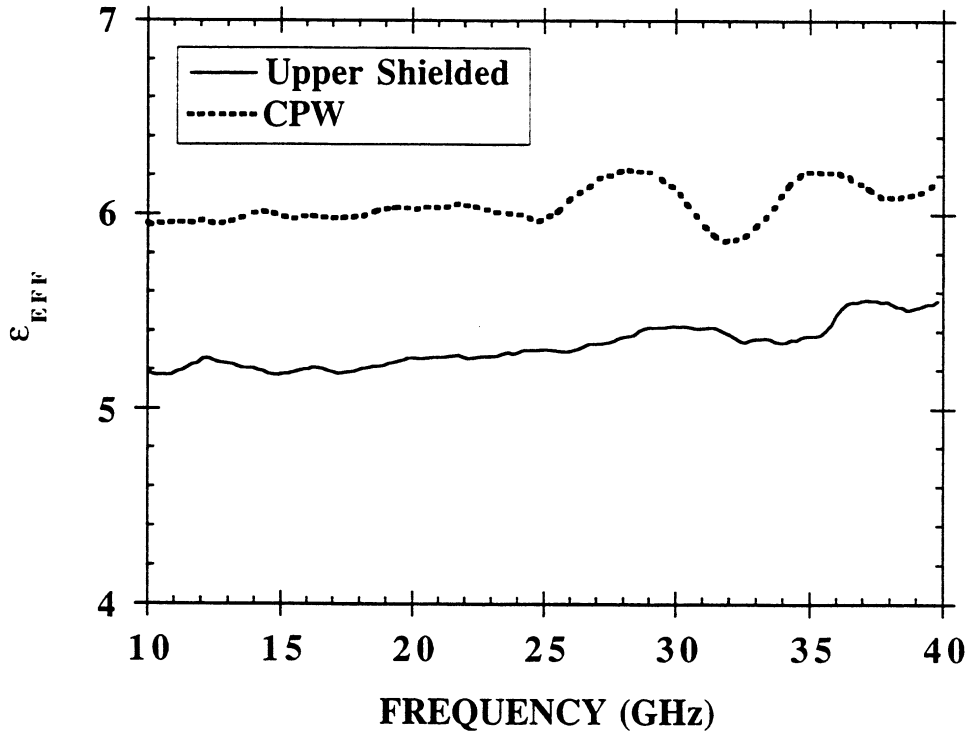


Figure 4.9 Effective dielectric constant for an upper shielded and open CPW through line.

open CPW line suffers from parasitic radiation losses in the form of substrate modes which is indicated by the ripple shown in the data toward the higher frequency end of the band. When the same line is packaged in the upper air region only, coupling into substrate modes is reduced resulting in a flatter response over the entire frequency range.

For the lower shielded (LS) and completely shielded (CS) through line, a plot is shown in Figure 4.10 for the line attenuation in dB/mm which includes the effects of both dielectric and conductor loss. The results shown on the figure indicate that the lower shielded

line has performance comparable to data presented by Taub [19] for losses in coplanar waveguide which is printed on silicon wafers with similar resistivity (3000 ohm-cm) and with the same aspect ratios. It is interesting to observe that attenuation in the completely shielded line (CS) is slightly higher than the lower shielded line (LS) due to additional conductor loss that is present in the upper shield. In conclusion, the data shown indicate

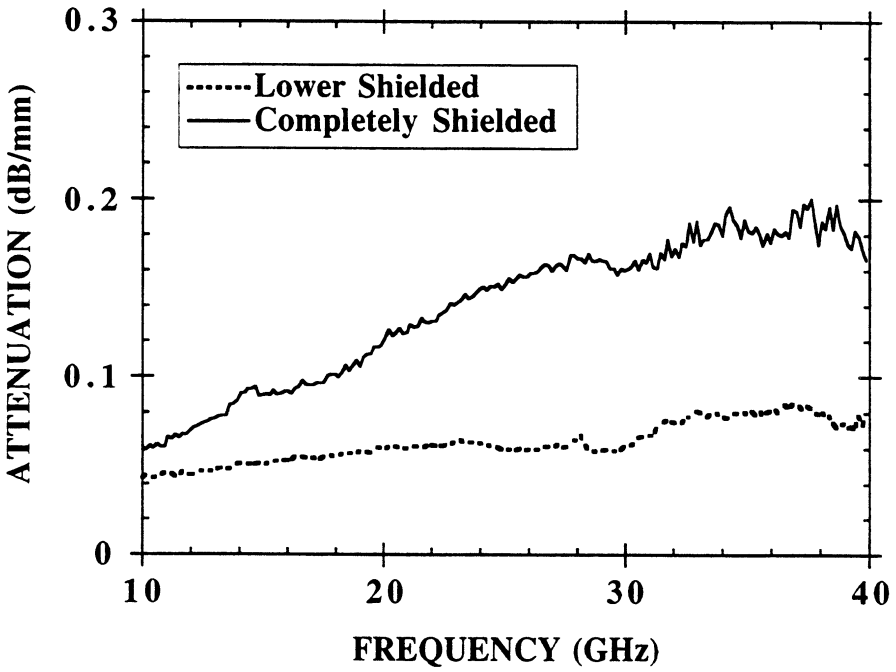


Figure 4.10 Attenuation constant for a completely shielded and lower shielded through line.

that both LS and CS cases provide a favorable alternative to the use of grounded CPW which is known to suffer from excitation of substrate modes. In the open-end series stub section discussed later, a more thorough description of micropackaging effects on circuit performance will be presented in order to show the benefits of either partial or complete shielding compared to open environment circuit designs.

For circuit isolation of a completely shielded configuration, two delays lines, whose lengths differ by 510 microns, are measured where the input signal goes into port 1 of the shorter line and the output signal is measured from port 2 of the longer delay line. The resulting measured isolation is at least -40 dB across the band as seen Figure 4.11 for circuits that are separated by approximately 2.54 millimeters.

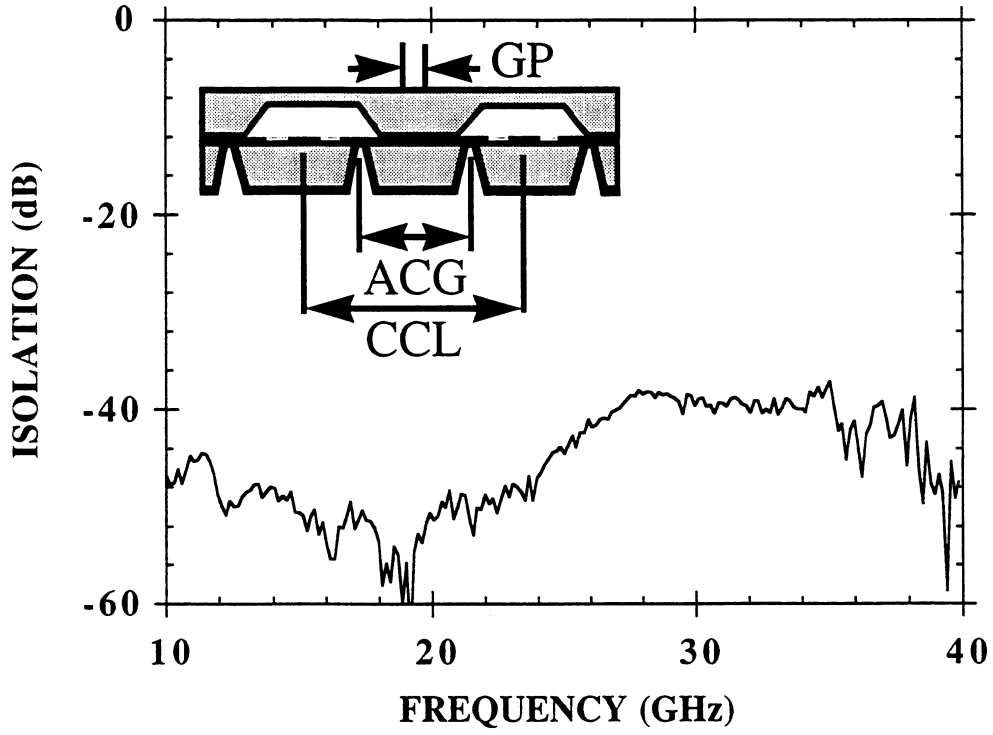


Figure 4.11 Isolation response between two completely shielded delay lines, where delay lines 1 and 2 are 3732 and 3242 microns, respectively. These lines have adjacent ground planes (GP), adjacent channel grooves (ACG) and center conducting lines (CCL) separated by 836, 1330 and 2546 microns, respectively.

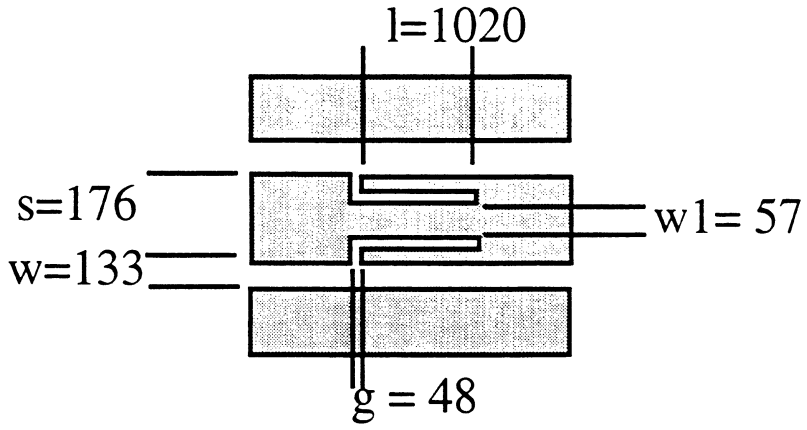
4.2.4 High Frequency Circuit Designs with In-Line Package

4.2.4.a Short-End Tuning Stub

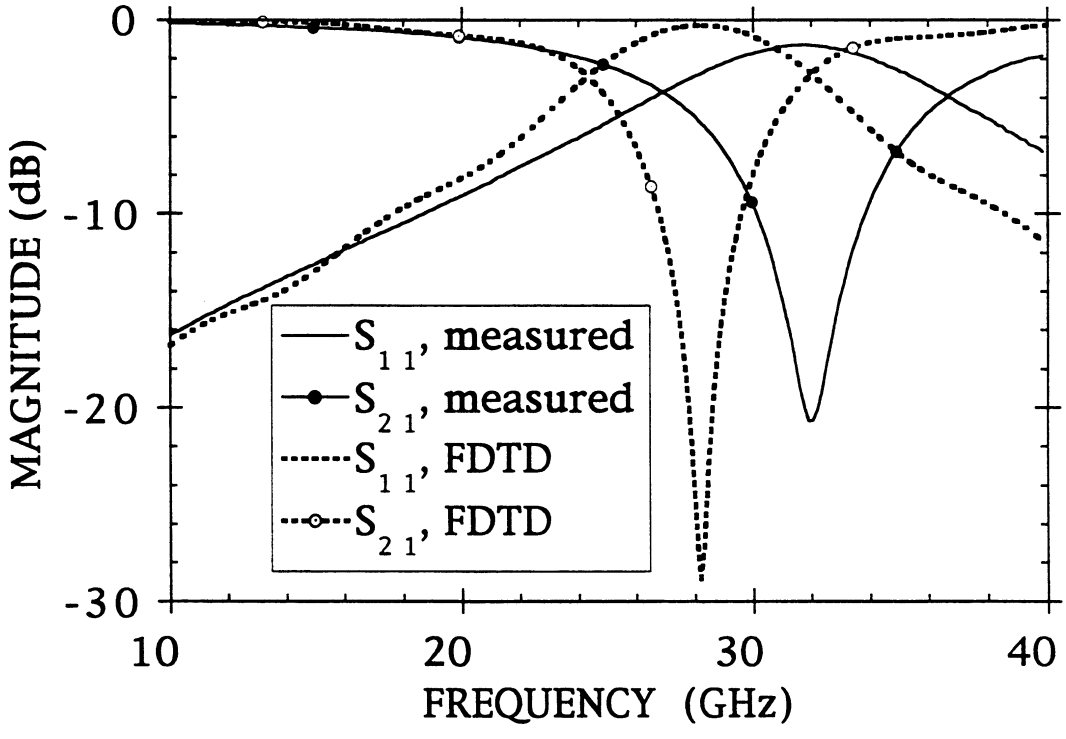
Various simple discontinuities are implemented to show the realization of conventional circuits into micromachined self-packaged design configurations. Figure 4.12a shows the physical dimensions of a series short-end tuning stub element [66] located within a completely shielded embodiment while Figure 4.12b shows a comparison between measured and full wave analysis results. The theoretical and experimental data are plotted and show similar electrical performance except for a shift in the resonant frequency which is attributed to the geometrical variations between the model and actual circuit geometry. Since the theoretical results do not account for losses, the difference in the level of the transmission coefficients is expected. Another geometrical variation that may also be responsible for the observed differences is the trapezoidal shape of the cavity walls as opposed to the rectangular shape assumed by the models. Furthermore, the theoretical model assumes identical widths whereas the upper cavity is actually wider than the lower cavity (Figure 4.7). Both of these effects can alter the circuit parasitic capacitances, thus, modifying the bandwidth and resonant frequency. Lastly, since the model assumes perfectly rectangular corners in the stub fingers, the measured line lengths can appear electrically shorter since the stub fingers suffer from rounding of corners and edges as a result of the fabrication procedures.

4.2.4.b Open-End Tuning Stub

The open-ended tuning stub [66] shown in Figure 4.13 will be used to illustrate the electromagnetic effects from a variety of micropackaging configurations. Performance curves will be shown for the upper (US), lower (LS) and completely shielded (CS) configurations. These results will be compared to open CPW and a discussion will be presented on the nature of the various effects on the circuit response.

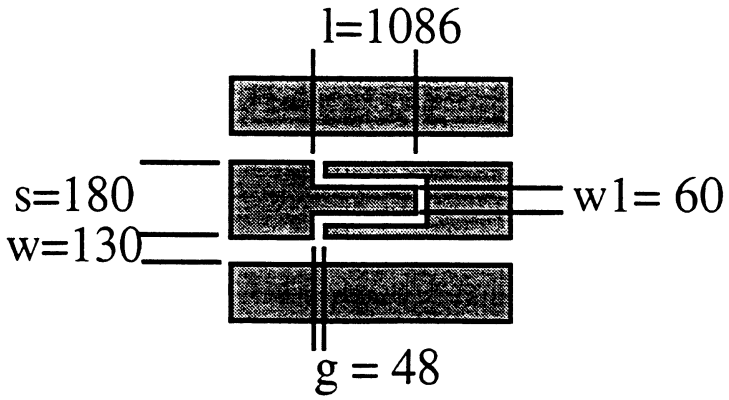


(a)

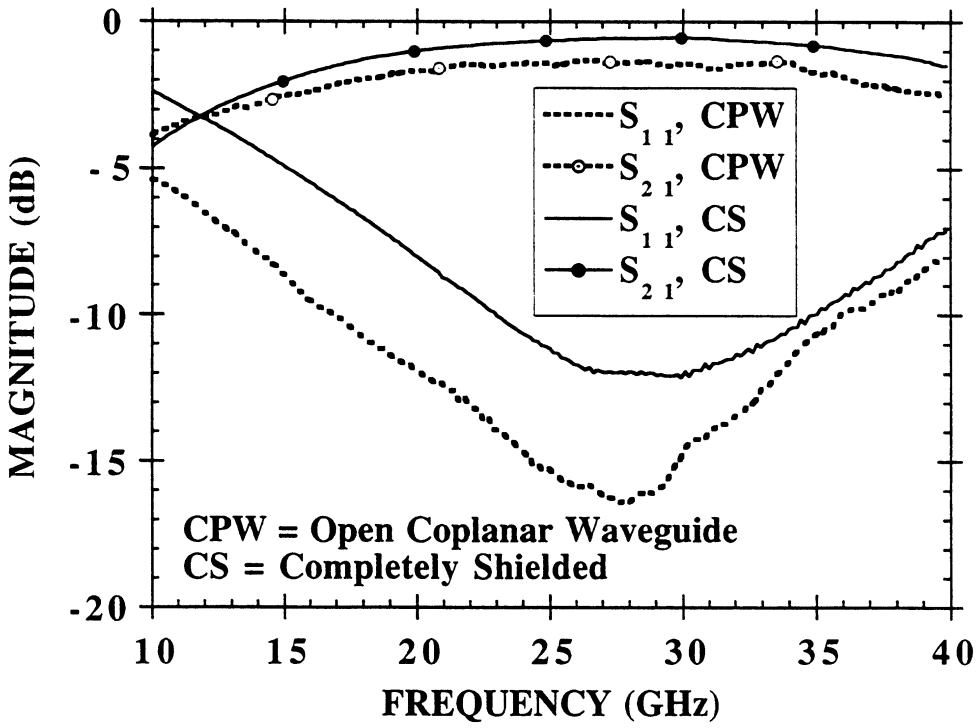


(b)

Figure 4.12 (a) Series short-end tuning stub dimensions in microns. (b) Comparison between FDTD model and measured results for reflection (S_{11}) and transmission (S_{21}) coefficients of a completely shielded short-end tuning stub in the lower view.



(a)



(b)

Figure 4.13 (a) Series open-end tuning stub circuit with dimensions in microns. (b) Comparison of reflection (S11) and transmission (S21) coefficients between open and completely shielded CPW environments of an open-end series stub. in the bottom view.

In the case of open CPW, loosely bound fields tend to leak power strongly and destructively into substrate modes. When shielding occurs in either or both regions, the propagating modes become tightly bound to the line and radiation is reduced significantly compared to the case of the open CPW. The circuit performance shown Figure 4.13 compares the open CPW to the CS geometry. The open CPW shows performance degradation above 25 GHz due to the excitation of a strong substrate mode, while completely shielded circuits exhibit a very smooth response even at higher frequencies due to the reduction of parasitic radiation and surface waves. When comparing the US to the LS configuration (Figure 4.14) for the same circuit geometry, the LS has the smoothest response due to the substantial reduction of substrate leakage. Although the circuit performance for the US show a few ripples at the higher frequencies, overall performance improvements are observed as a nearly symmetric response is obtained. While the LS and CS scattering parameter measurements appear virtually identical in Figure 4.14 and existing differences will become more apparent when observing the total loss data shown in Figure 4.15.

A the total loss comparison of self-packaged components and open environment components, as seen in Figure 4.15, shows that open configurations exhibit the highest overall loss. Of the self-packaged components, the US configuration has the highest loss which is mainly due to conductor loss and excitation of a strong surface waves. The lowest loss is presented by the LS geometry since the fields are primarily confined in the dielectric-filled cavity causing a reduction of parasitic radiation effects into air. In these circuits the LS package size is chosen to be small enough to suppress unwanted resonances. Lastly, the CS geometry exhibits loss performance that is compromised slightly when compared the to LS case due to the presence of the upper shield. In general, however, micropackages with partially or completely shielded environments can offer significant improvement in electrical performance over open environment circuits. In instances where maximum reduction in loss is needed, the lower shielded configuration is the ideal choice while opti-

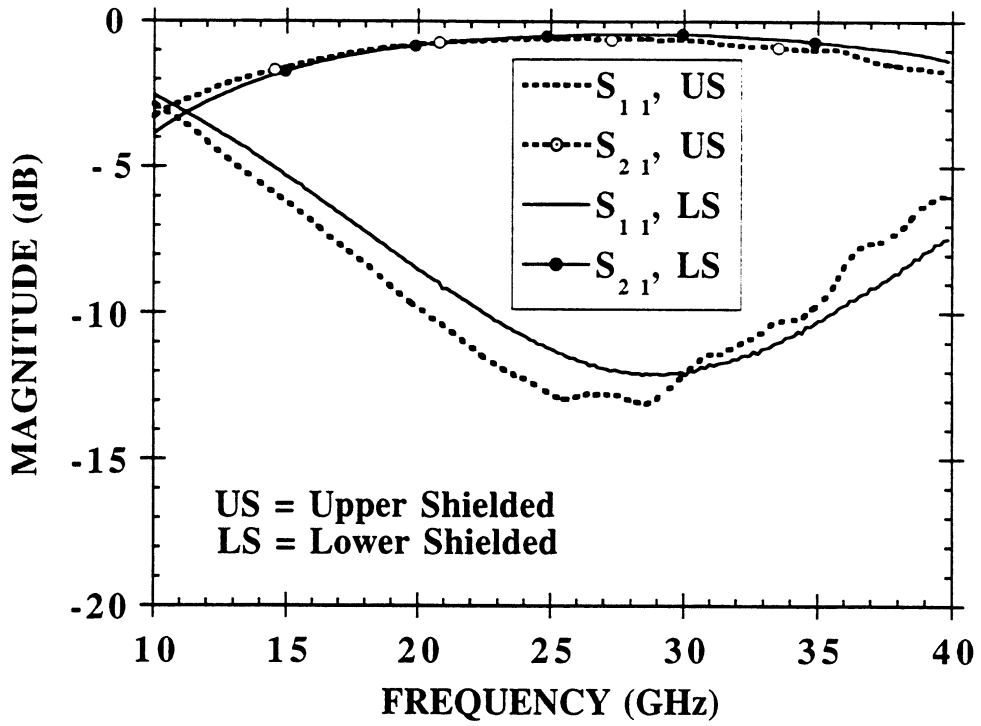


Figure 4.14 Comparison of reflection (S_{11}) and transmission (S_{21}) coefficients between upper and lower shielded CPW environments for an open-end series stub.

mum isolation in either or both regions requires use of the completely shielded configuration.

4.2.4.c Stepped Impedance Filter

A five-section stepped-impedance CS lowpass filter has been designed as shown in Figure 4.16 with high and low impedances of 100 Ω and 20 Ω, respectively. Figure 4.17 show a comparison between measurements and theoretical results derived from quasi-static models where both conductor and dielectric losses are included. In the PUFF model, care was taken to incorporate the specific metallization thickness and the appropriate surface resistivity which correspond to the various sections of microstrip line widths. To realize 100 and 20 ohm impedance steps, 20 and 380 micron wide conductor lines are used with slot widths of 210 and 30 microns. In the low impedance section the line excites a

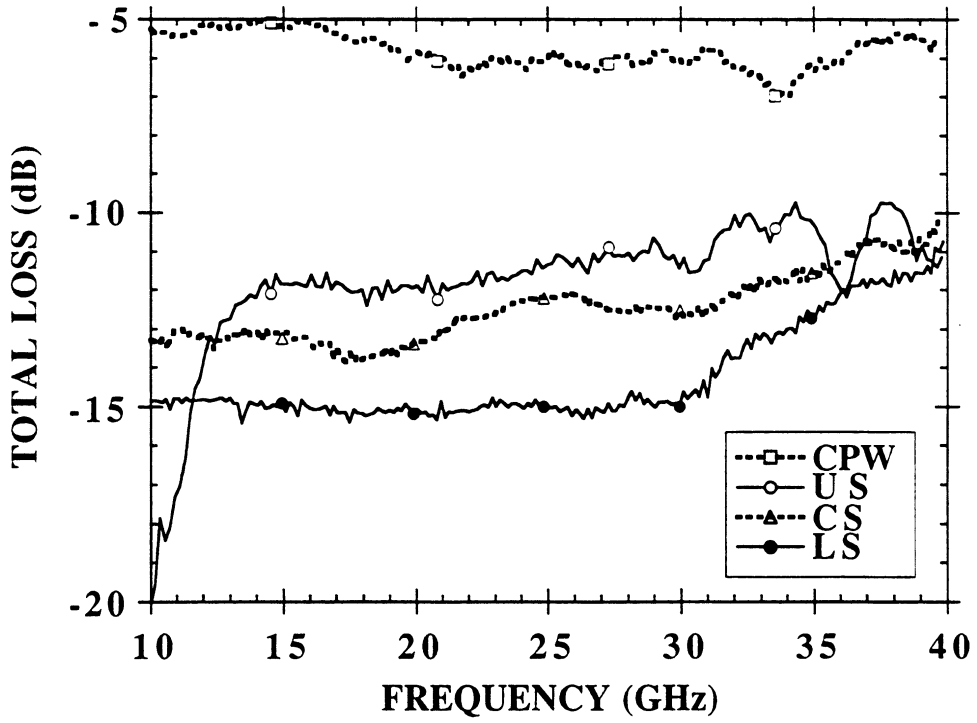
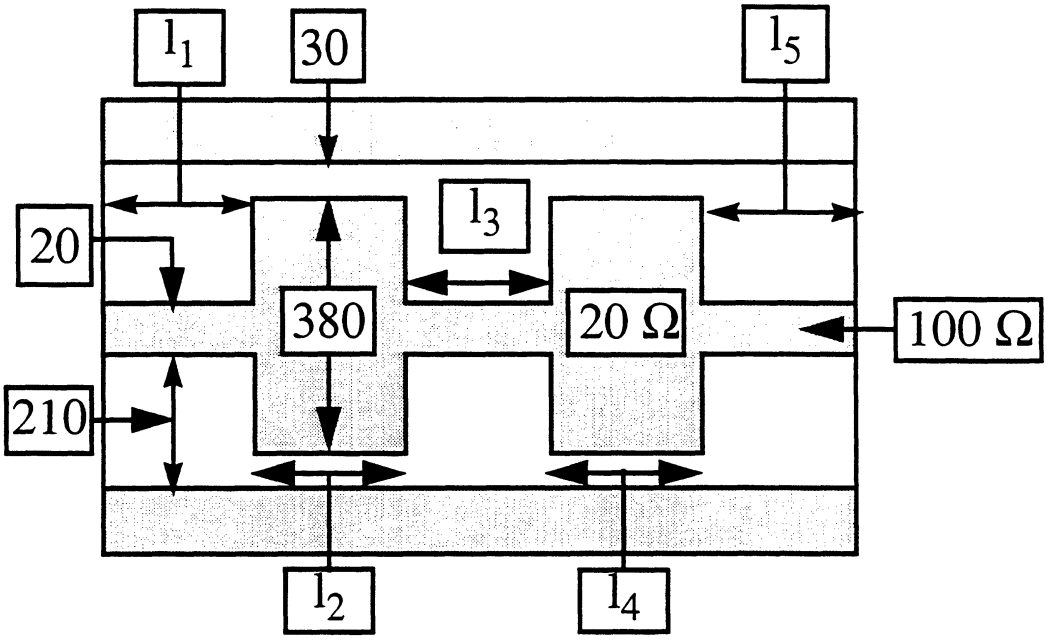


Figure 4.15 Loss comparison of an open-end series stub in open (CPW), upper (US), lower (LS) and completely shielded (CS) environments.

coplanar waveguide mode due to the narrow slot width while the high impedance section excites a microstrip mode. This mixed-mode operation produces parasitic inductances and capacitances that cannot be easily accounted for in the quasi-static model. Despite this limitation however, at relatively low operating frequencies the effects of such parasitics are reduced and, as seen in Figure 4.17, the measurements agree very well with the theoretical data. The total system loss, $(1- |S_{11}|^2 - |S_{21}|^2)$, shown in Figure 4.18 shows good agreement between theory and measured results. This indicates that the circuit has negligible radiation loss and thereby confirms the effectiveness of the micropackage. The level of loss can be attributed to the aspect ratios of the low and high impedance sections which are known to cause higher loss in both the coplanar waveguide mode [68] and the microstrip mode [69].



Line Lengths (microns)
l_1= 988
l_2=703
l_3=940
l_4=722
l_5=988

Table 4.2 Actual Circuit Dimensions

Figure 4.16 Dimensions of a 5-section stepped impedance lowpass filter having low impedance sections of 20 ohms and high impedance sections of 100 ohms.

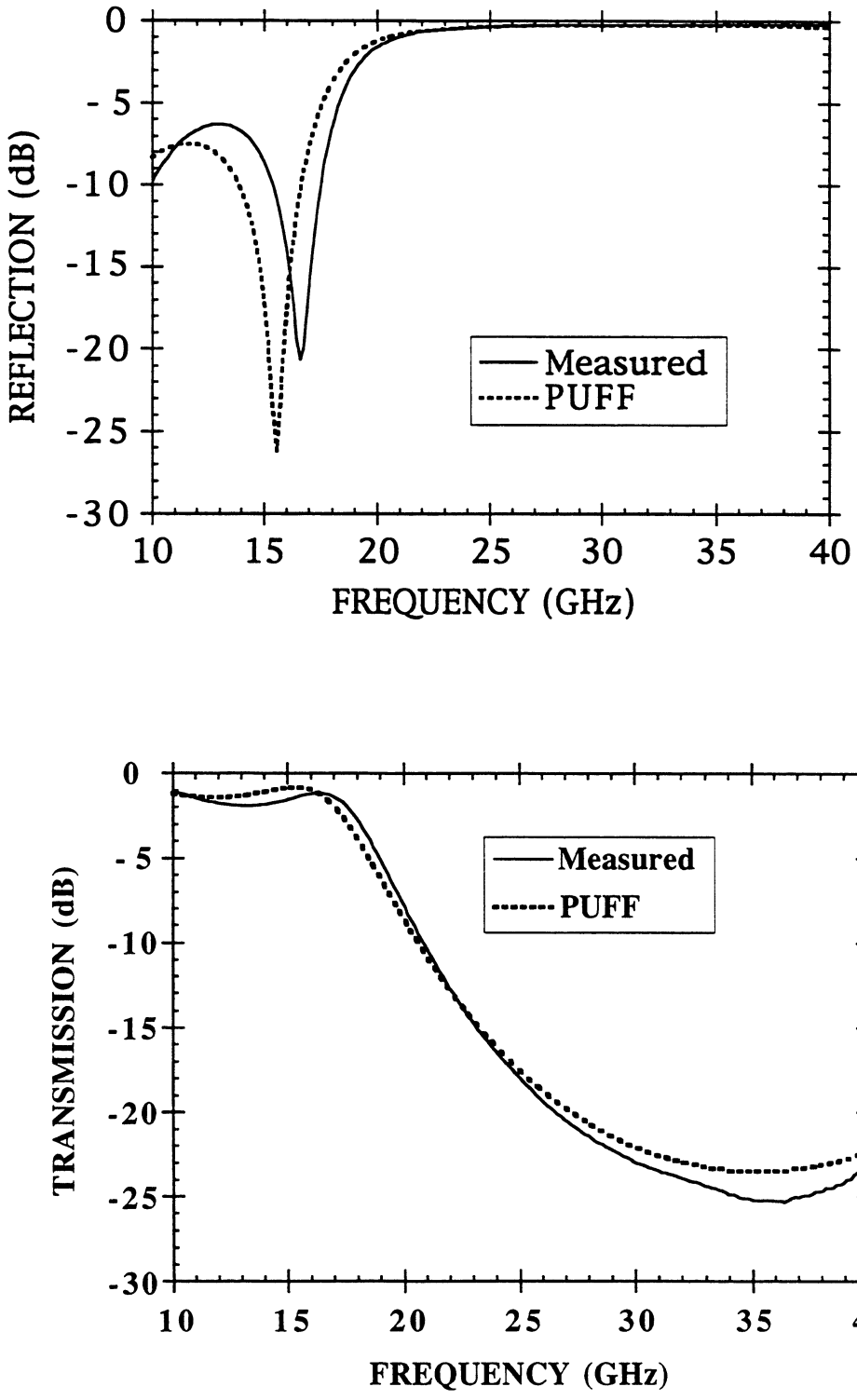


Figure 4.17 Comparison of reflection and transmission coefficient between the PUFF model and measured results for a 5-section stepped impedance lowpass filter.

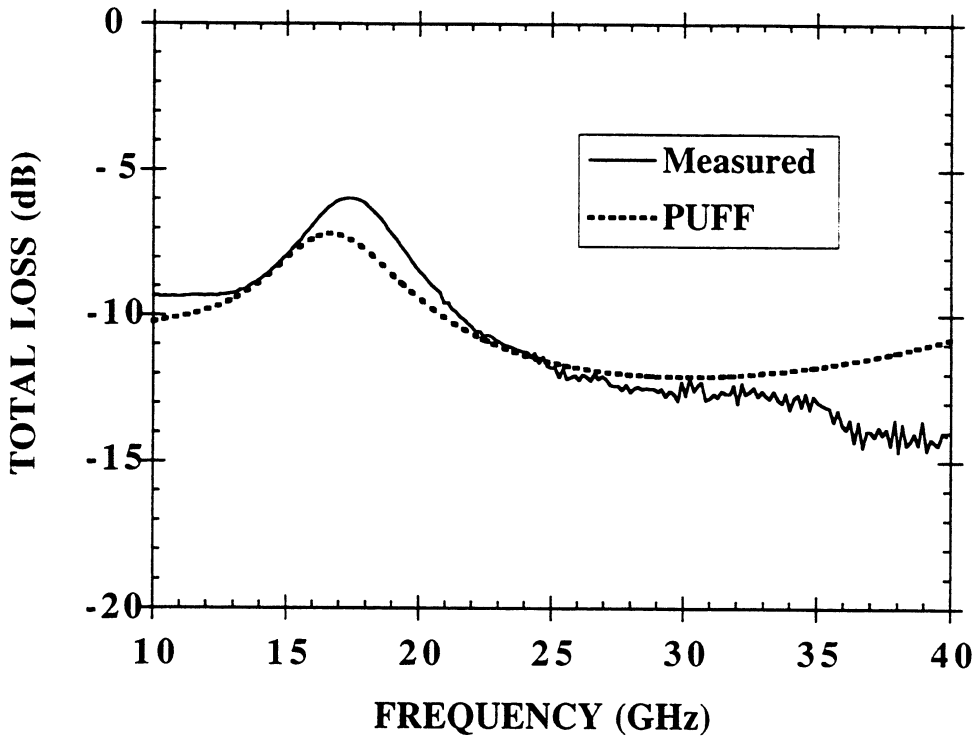


Figure 4.18 Loss comparison between the PUFF model and measured response for a 5-section stepped impedance lowpass filter.

A seven-section stepped impedance filter (Figure 4.19) is realized that illustrates the importance of maintaining a DC ground between the lower shield and the CPW ground. In Figure 4.20, measured and theoretical data are shown, where the measured circuit begins to show effects of substrate mode leakage at 30 GHz that is not predicted in the theoretical model. In this circuit, rf coupling though the oxide dielectric is used to establish grounding between the various ground connections. Comparison between measured data and the ideal transmission line model are also shown where the conductor loss and dielectric has been included. The loss indicates similar effect from the ripple effect shown compared to the computed response of theoretical response. Care has been taken regarding the conductor losses to incorporate the specific metallization thickness and appropriate surface resistivity corresponding to the various sections of line widths. Since low and high impedance

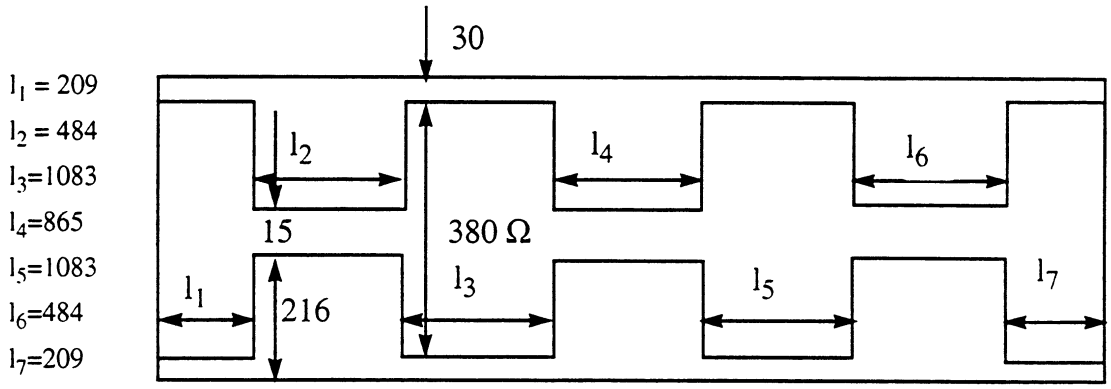


Figure 4.19 Seven-section stepped impedance filter where all dimension are in microns.

lines are used, the low section excites a coplanar waveguide mode due to the narrow slot width while high impedance section excites the microstrip mode. This result in sections of lines that operate in a mixed mode and create parasitics that cannot be easily accounted for in the current model [69]. A modified circuit that has the continuous dc connection between the two ground planes is shown for the five-section stepped impedance filter above shown in Figure 4.16. Validation of the response of a self-packaged filter, shown in Figure 4.22, is provided through a comparison between a theoretical model based on finite difference time domain (FDTD) and experimental measurements. Even though loss effects have been neglected in the model, excellent agreement is observed.

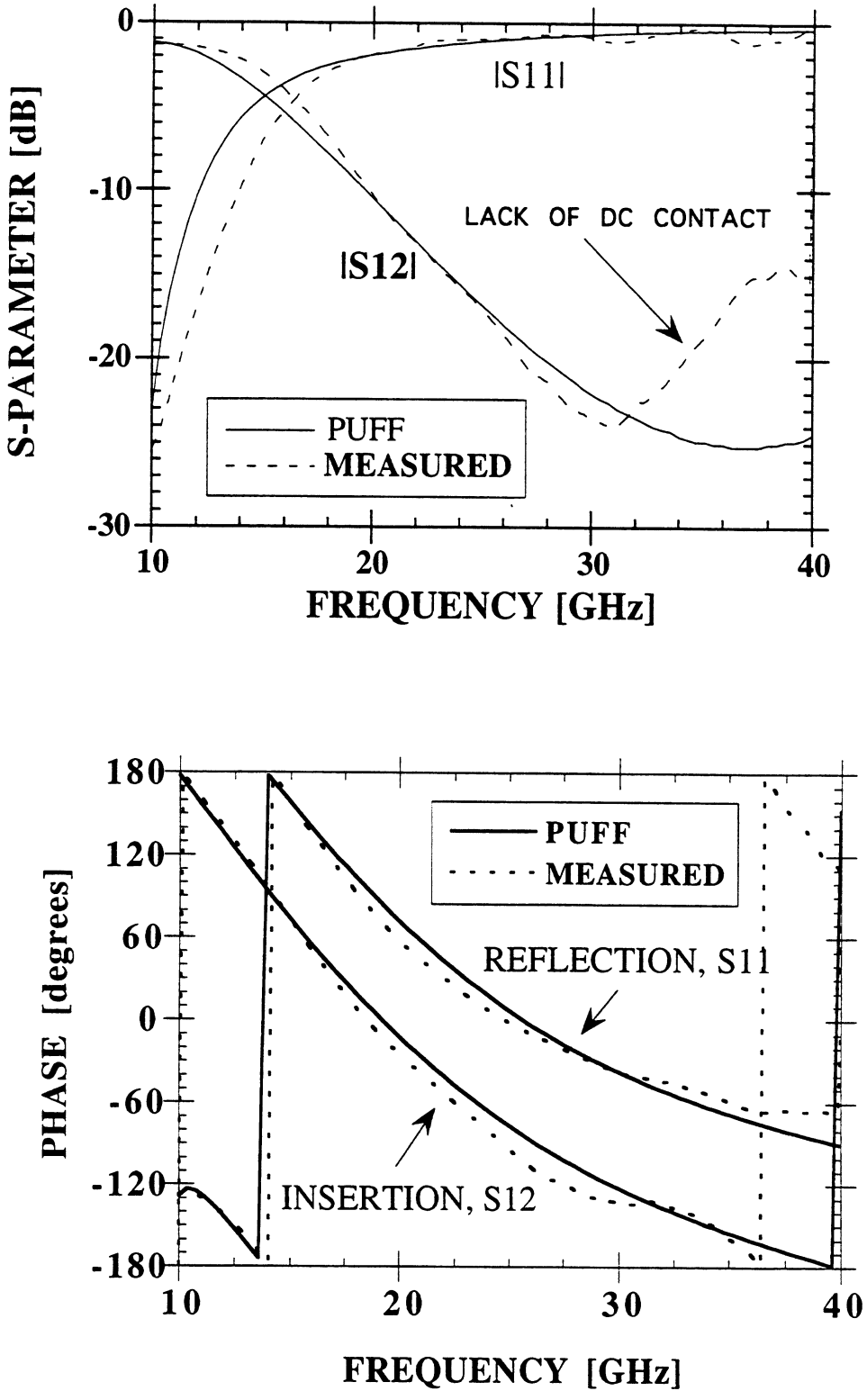


Figure 4.20 Performance of a seven-section stepped impedance filter without dc contact.

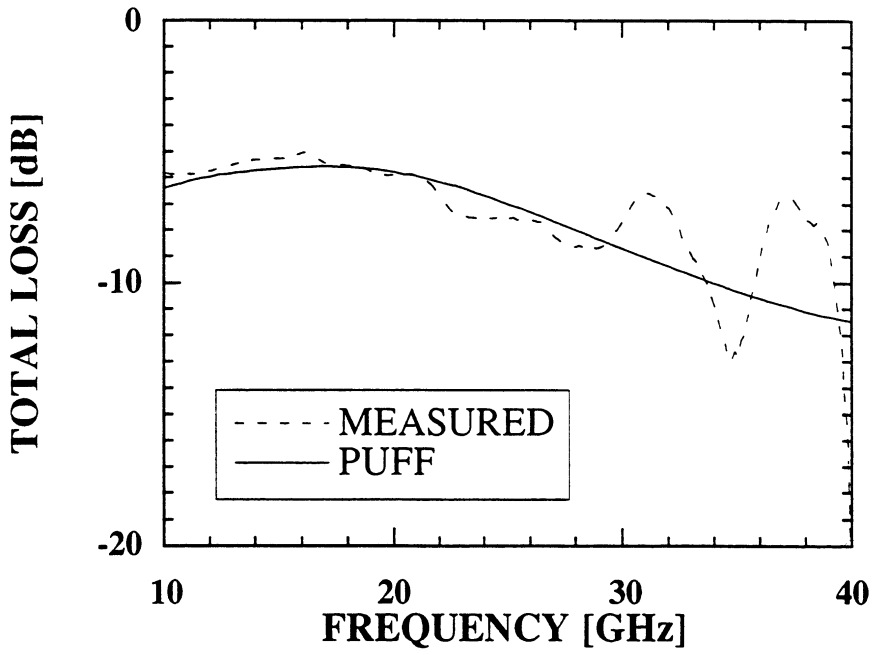


Figure 4.21 Loss Performance for the seven-section stepped impedance filter without dc contact between the planar line ground and the lower shield.

4.2.5 Micromachined Conformally Packaged Circuits

The "in-line" self-packaged circuit has motivated the investigation of monolithic conformal packages that can follow the path of various line geometries, and can be sized in such a way that package resonances are excluded from the desired operating frequency range. Furthermore, this package offers flexibility for use with existing uniplanar technologies and thus can incorporate many types of transmission medium such as microstrip, coplanar waveguide, coaxial line or stripline. Since the concept of conformal packaging can be applied to a very broad range of applications, some investigation is required to evaluate the effects this package has on circuit designs that have non-linear paths within the geometry. In an effort to meet space allocation criteria, many designs that incorporate power dividing and arrays use bends and meander lines to reduce the space required of very long feed lines. Therefore, to illustrate the use of conformal micropackaging to non-

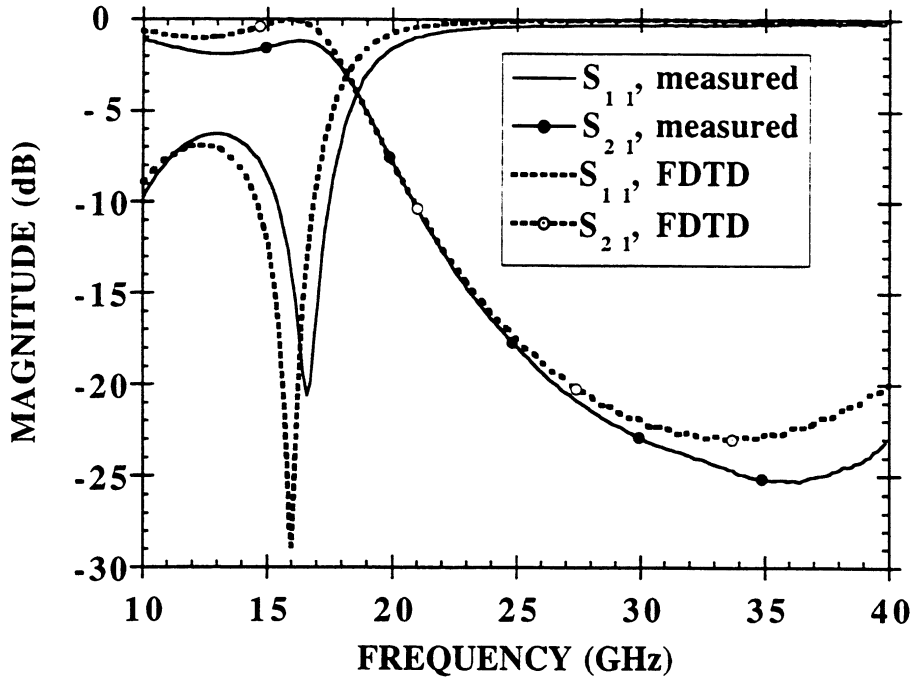


Figure 4.22 Comparison between the FDTD model and measured results for reflection (S_{11}) and transmission (S_{21}) coefficients of a 5-section stepped impedance lowpass filter.

linear topologies, a detector mounting structure and double right angle bend have been selected.

4.2.5.a Microwave Detector Mount

The primary objective of this project is to illustrate the use of micromachining in the development of conformal packages for high frequency mounting structures. This section begins with a discussion of the approach and goals of this work. The conformal package topology issues are summarized, followed by the design of the detector circuit. Next, experimental results and a discussion are presented on the mount characterization. The concluding remarks consist of a general summary and proposed improvements to the detector design.

The detector mount system under consideration uses two diodes mounted hybridly in a balanced arrangement across the slots of a coplanar waveguide-based design (Figure

4.23). To package this mounting structure, a topology is required that shields the planar circuit and accommodates the non-linear or cross-tee junction that is present due to the shunted diodes across the CPW slots. In order to realize this structure, the problem is divided into a detector and a package design. Since the package is the primary objective, there are two main requirements that must be achieved. First, the shield cannot degrade the performance of the detector circuit and second, the diodes cannot be obstructed during the integration of the upper shielding cavity.

The fabricated mounting structure uses three silicon <100> wafers to realize the circuit and shielding package. In the middle wafer, the upper shield has been left completely open in order to verify that the shielding cavity has not obstructed the diode in the space allocated. The package cross-section resembles the two-dimensional self-package described in Chapter 2 with the addition of right-angle corners to accommodate the cross-tee junction for the diodes. In the lower wafer, the circuit is shielded by lower cavity which is defined by the adjacent sidewalls of the v-grooves underneath the ground planes. To complete the circuits, diodes are then mounted hybridly and an additional metallized wafer is placed on top of the middle wafer to completely enclose the mount. While a three wafer system has been used as the prototype, a two wafer system can be easily implemented by replacing the upper two wafers with a single wafer. This will provide a continuous upper shielding enclosure to the mount and reduce the size and weight of each mounting structure. Lastly, all wafers are secured together using adhesion techniques of either resist or silver epoxy.

One of the problems encountered in this design is the issue of overetching. In this layout, there are outward corners underneath the planar line that were overetched in the region of the outer ground plane. In Figure 4.24, the wavy crinkled regions in the ground plane are indications of overetching and ground plane deformation. Since the region underneath the circuit is far away from the lower shielding cavity, it is electrically decoupled from the fields in the slots of the coplanar line. Therefore, this should not impact the

Figure 4.23 Picture of the micromachined diode mounting planar circuit

electrical performance of the circuit. The problem of ground plane deformation, however, limits the overall integrity of the mounting structure. There are two modifications to resolve this issue associated with the metal thickness and supporting dielectric materials. First, metal thicknesses on the order of 3 microns can be achieved through electroplating and provide good step coverage compared to the 1 micron thick evaporated metal used in this case. The evaporated metal is problematic since the dielectric, removed to achieve DC contact, is on the order of 1.2 microns. The result is poor step coverage in that region which adds stress and fatigue to the unsupported thin metal. Second, the inclusion of a tri-dielectric layer of oxide/nitride/oxide can be used as opposed to the single dielectric layer oxide (Figure 4.24) to offer additional support to the metal. The oxide dielectric has been observed to collapse in the regions where there is undercutting and deforms the vertical walls of the masking oxide.

In this coplanar waveguide design, two similar diodes are placed in a parallel arrangement across the CPW slots. Since the diodes are considerably larger than the planar slot widths, the ground planes are deformed and the center conductor is extended to accommodate the length of the diode. Since two diodes are required, similar DC performance is necessary to maintain symmetry in the planar circuit. The HP 8320-HSCH beam lead chip is bonded to the circuit using silver epoxy (EPO-TEK H20-E). The measured series resistance is 16 ohms and a zero-bias junction capacitance is 0.08 pF. The ideality factor, n, is 1.05 and the saturation current, I_s, is 5.25 pA. With the dc parameters known, the matching network can be designed and the system can be evaluated. The planar circuit is modelled after the basic detector circuit shown in Figure 4.25. Specific design requirements [71] used in the development a micromachined detector correspond to the circuit shown in Figure 4.25. A 5 section stepped impedance lowpass filter is designed and has the response shown in Figure 4.22 with dimensions given in Figure 4.16.

Two measurements are required to evaluate the performance of the detector mount. First, the response of the passive circuit is obtained using the on-wafer probing station and

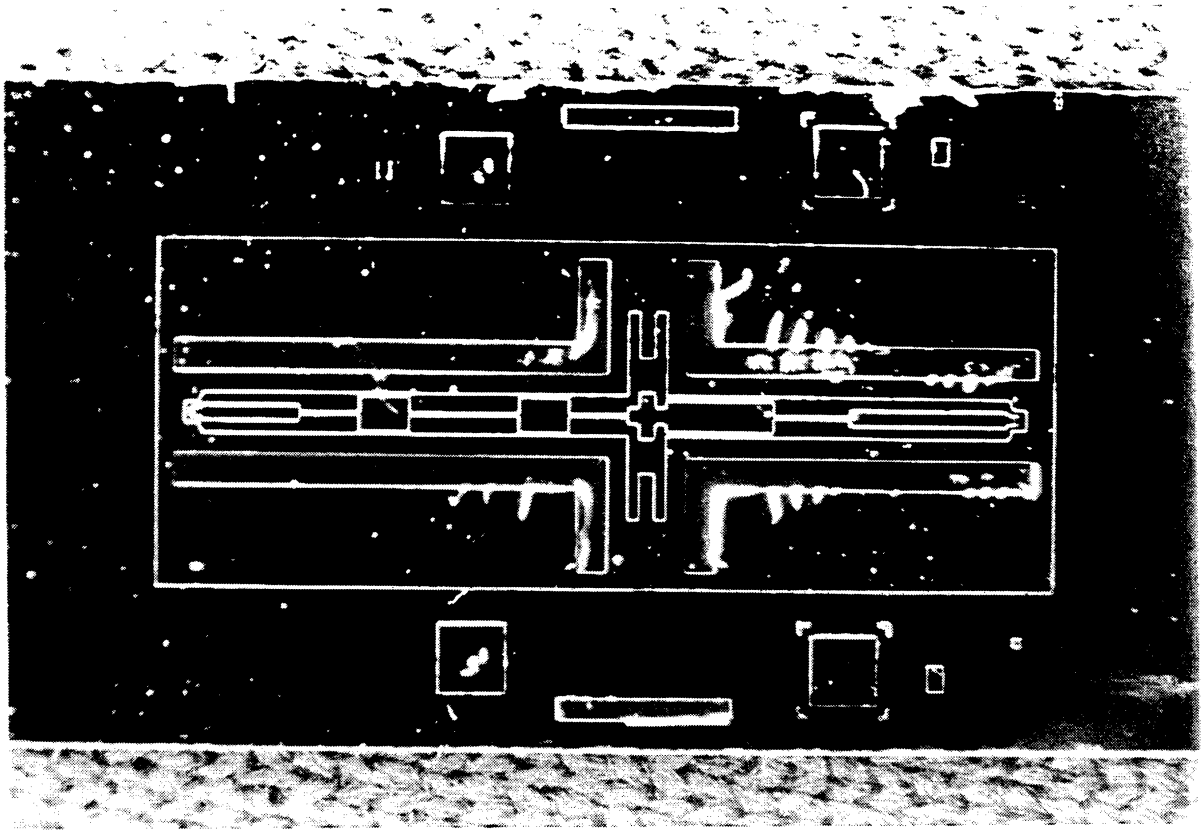


Figure 4.24 Photograph of the micromachined detector circuit.

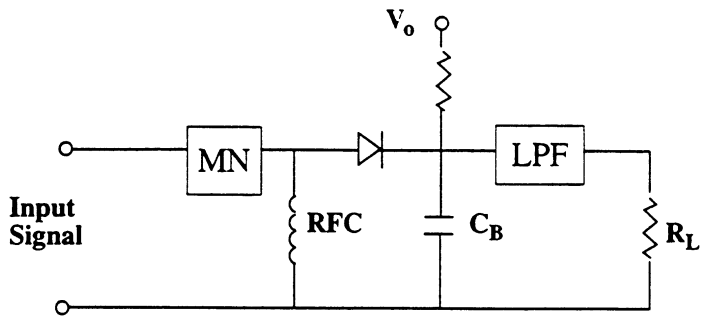


Figure 4.25 General design scheme for a detector circuit, where MN is the matching network, LPF is a lowpass filter, RFC is the RF choke, and CB is the blocking capacitor.

is shown in Figure 4.26. The detector has the best match at 21 GHz (Figure 4.27) and the matching network shows a 750 MHz bandwidth response at -10 db return loss. Second, the detector responsivity is determined for a modulated RF signal. Video detection is defined as the ratio of detected low frequency voltage across the load to the RF power available at the terminals of the circuit. The video detection is done at 21 GHz for a bias current of 20 microampere to the diode pair.

The measurement set-up used to obtain responsivity is shown in Figure 4.28. The bias box sends a bias current to the detector via the high frequency probes. This signal is received from the DC bias port in the back of the test set. The DC output signal is received at the bias box from the circuit and sent to the lock-in amplifier which measures the detected output voltage. The detector is evaluated with a 21 GHz RF signal of that is modulated with a 1 KHz square wave pulse having 50% duty cycle. The responsivity computed from the measurements at 21 GHz for the lower half shielded and completely shielded structure are 1680 and 1810 V/W. The bandwidth of the circuit can be improved by using a wideband matching techniques. Specific to the packaged design, the overall circuit responsivity improves with the inclusion of the shielding structure. The packaged design reduces the parasitics caused by discontinuities in the planar circuit which will

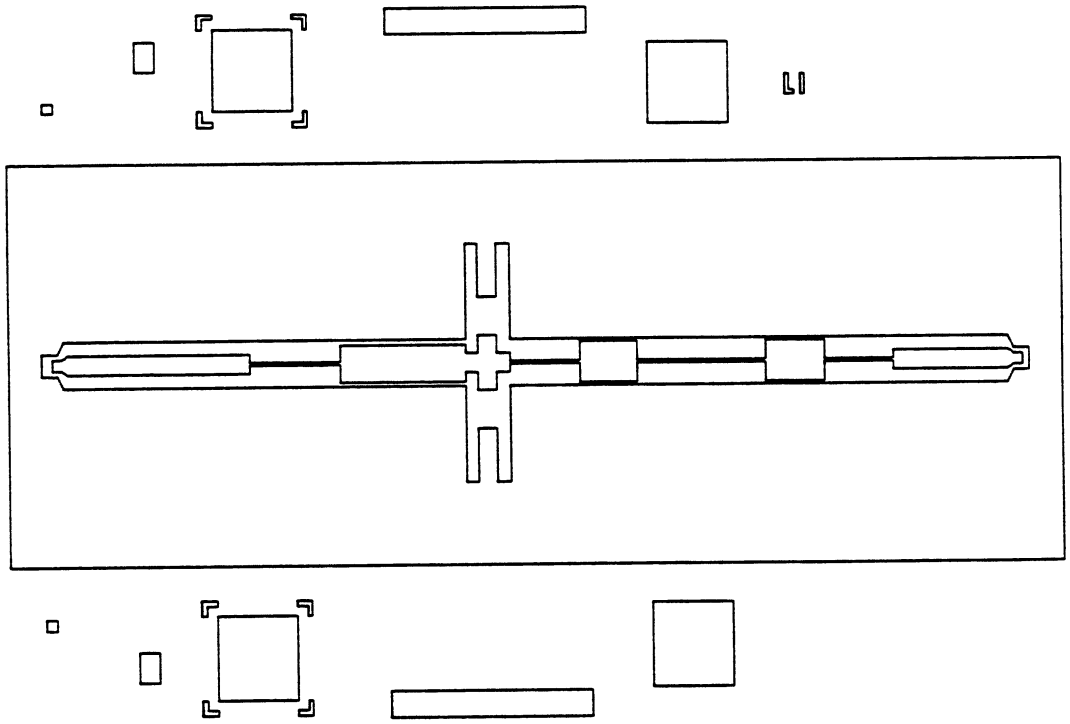


Figure 4.26 Top view of the planar circuit layout of the detector mounting structure.

radiate higher and exhibit substrate mode excitation. A comparison of the diode responsivity to a theoretically modelled one is shown in Figure 4.29. This figure shows a comparison between the measured and computed responsivity, where improvements are observed for the packaged configuration. The details of the derivation are shown in APPENDIX C.

To summarize, a subsystem design has been implemented for a detector mounting structure. It has been evaluated using on-wafer probing for the passive circuit performance as well as the responsivity. The concept of the conformal package has been successfully demonstrated in a hybrid design since the responsivity increases due to the package. This type of package can be used in a hybrid or monolithic designs and a wideband perfor-

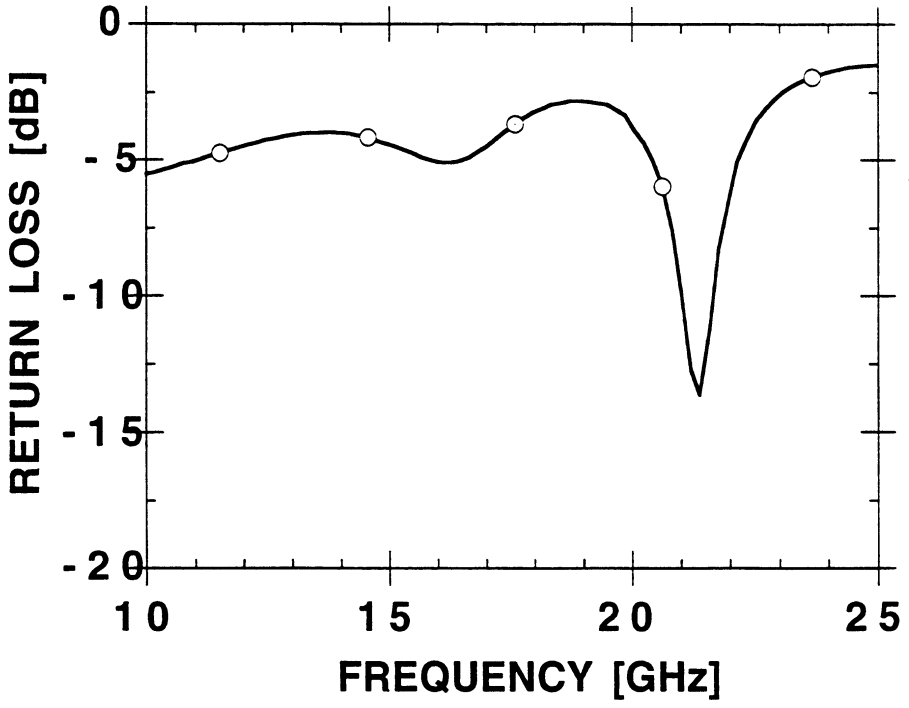


Figure 4.27 Passive circuit response of the detector mounting structure.

mance can be achieved with the use of wideband matching networks such as resistive shunting. To address the narrow bandwidth, a high impedance resistor can be shunted across the diode. This resistor, however, will need to have a series capacitance in order to provide the appropriate RF short and to DC block this load from the LF network. Without this blocking capacitor, the resistor loads the amplifier making the detected signal extremely small. Although consideration was given to the implementation of a wideband design, detector design optimization will not be addressed since the primary objective of this research is to address packaging.

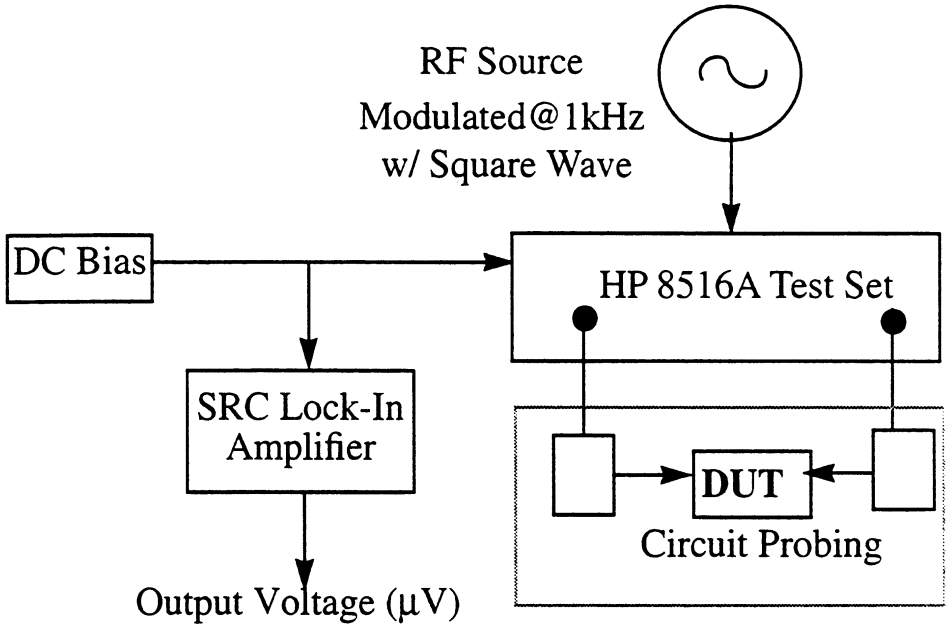


Figure 4.28 Measurement System for the Detector Mounting structure.

4.2.5.b Double Right-Angle Bends

The last section of this chapter introduces the double right-angle bend shown in Figure 4.30 for a open and partially shielded circuit. It has been fabricated using standard procedures for the planar circuit and the upper shielding cavity. In this design, the issue of the convex corners has been improved compared to the one shown in the detector mount. The planar circuit has center conductor and slot width of 180 and 130 microns, respectively and is on 350 micron high resistivity silicon. The upper cavity has been fabricated on low resistivity silicon and is etched 350 microns deep and 1200 microns wide on a 550 micron thick wafer. Both the open and the partially shielded circuit have been mounted on a duroid substrate to reduce the effects of substrate modes excitation found in grounded coplanar waveguide circuits. Note in this case, that the shielding only occurs in the upper half space and the dielectric in the lower region is continuous.

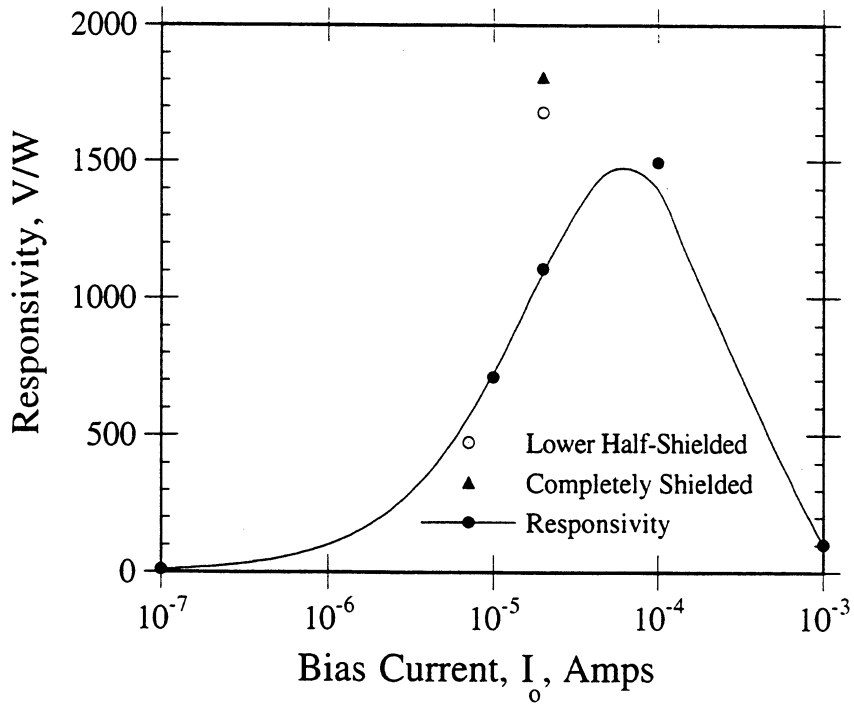


Figure 4.29 Predicted versus computed responsivity of the micromachined detector circuit. The individual data points represent the measured results for the lower half-shielded and completely shielded structure.

The response of the micromachined circuit is shown in Figure 4.31 for the open and the shielded case. The performance is very similar as expected indicating that the effects of the upper cavity are minimal on the circuit performance in this operating range. Similarities between the return and insertion loss phase data of the open and half-shielded structure indicate that the propagation constant is not altered much by the presence of the upper cavity. As the frequency of operation increases beyond the band shown, the upper shielded case has some excitation of parasitic modes that can be minimized in a completely shielded topology. The total loss shown in Figure 4.32 for this circuit is also simi-

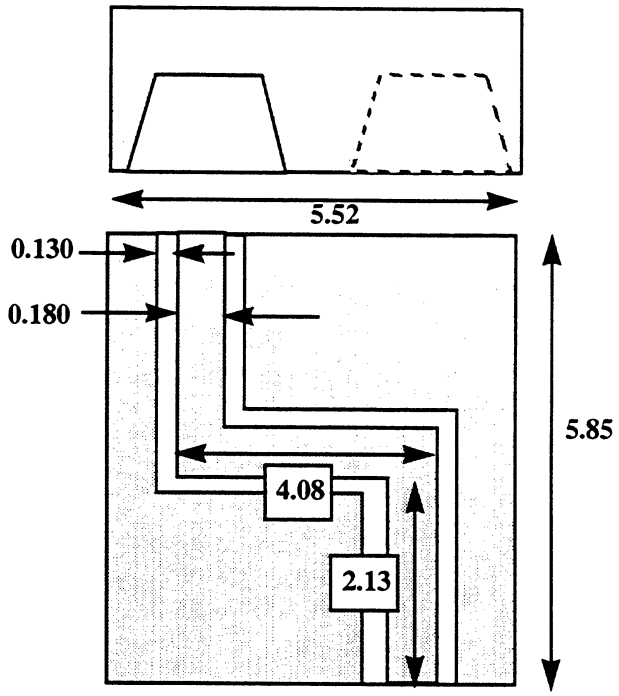


Figure 4.30 Illustration of the double right angle bend. Top drawing shows a front view of the cavity region. Bottom view shows a top view of the circuit geometry. All dimensions are in millimeters.

lar even though it is a little higher by about 0.5 dB in the case of the upper cavity circuit due to the additional conductor of the shielding region.

4.3 SUMMARY AND CONCLUSIONS

The development of micromachined cavities for micropackaging of high frequency circuits has proven successful. The performance of a scaled model version has been shown as the predecessor to the actual micromachined circuits and measured data have been compared to theoretical results. Micromachined packaged circuits have been illustrated in a variety of configurations and are used for representative circuits based on coplanar waveguide transmission line to evaluate the performance. Of the three possible shielding topologies (i.e. upper, lower and completely shielding) a comparison is made between the

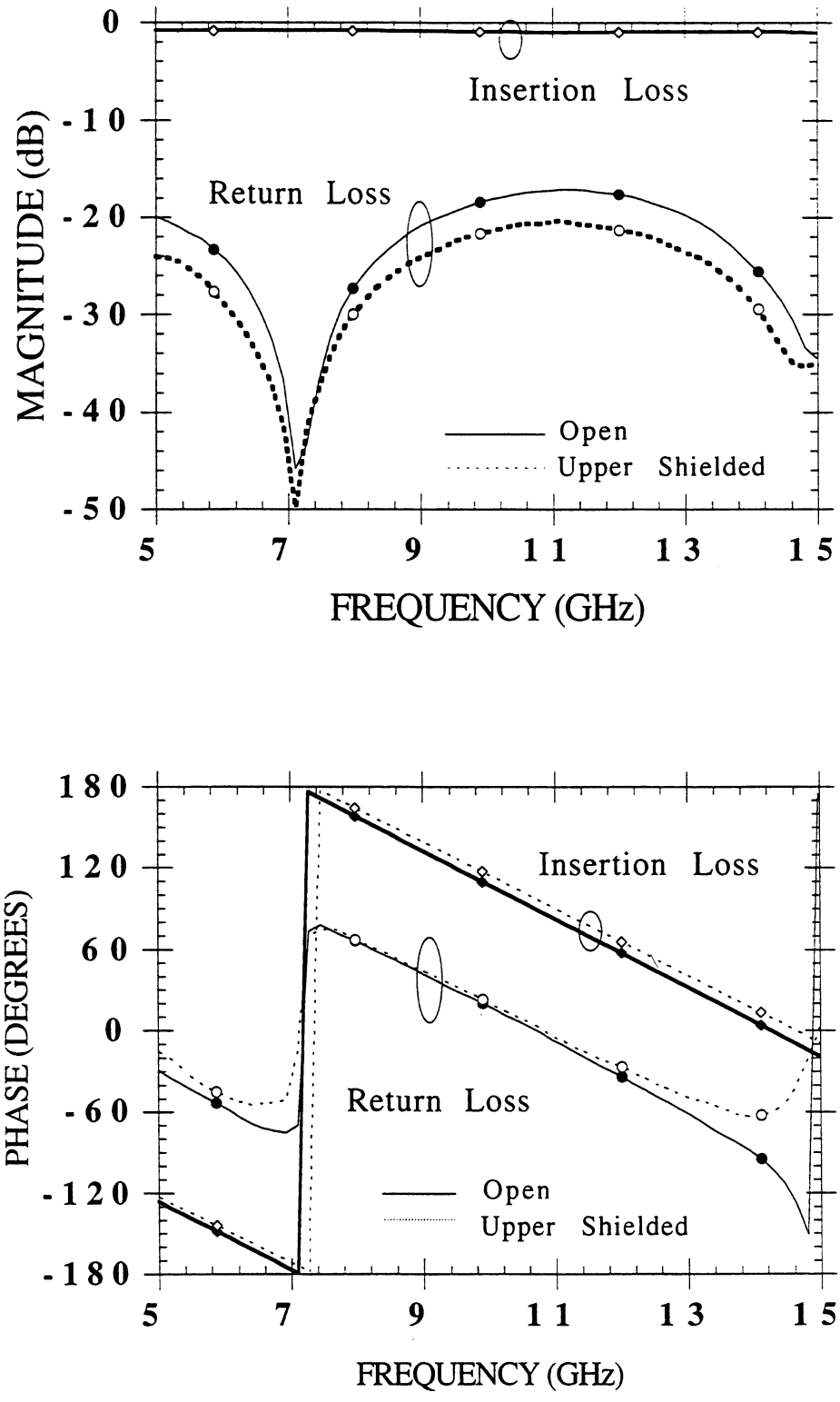


Figure 4.31 Performance of the double right angle bend for the open and upper shielded geometry.

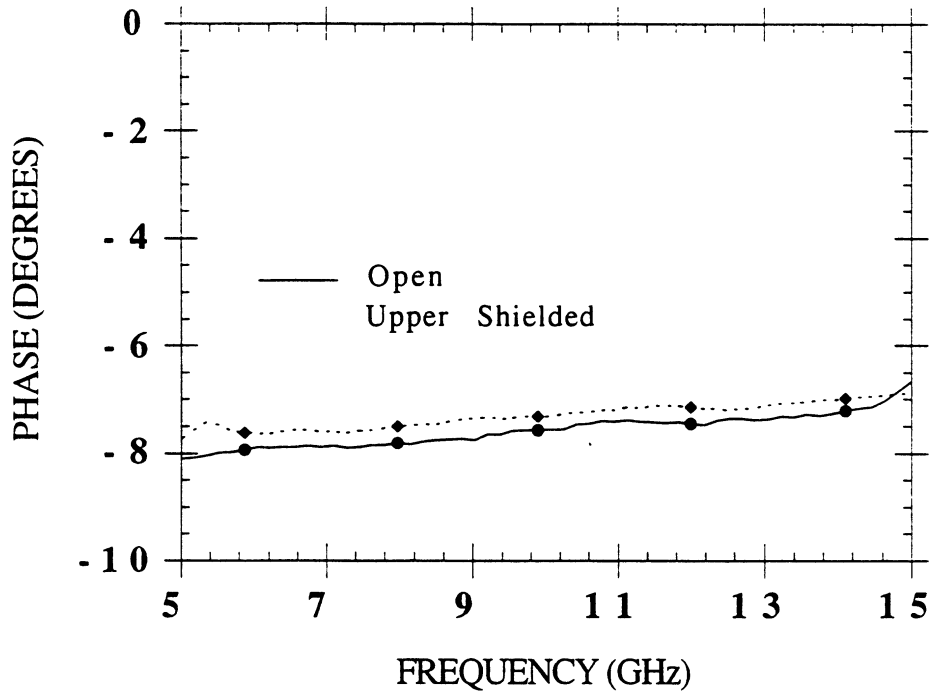


Figure 4.32 Computed Total Loss for the double right angle bend shown in Figure 4.26.

open structure and theoretical predications. In all cases, electrical performance improvements were observed for the variety of planar circuit realized. The most significant improvement have been observed first in the lower shielded circuits, second completely shielded and then the upper shielding.

The response of simple circuit geometries used in conventional planar line designs have been implemented for the "in-line" configurations for through lines, series open and short tuning stubs, as well as a stepped impedance lowpass filter circuits. The measured response has been compared to an open coplanar waveguide circuits having a similar geometry as well as to theoretical models that are based on quasi-static or full-wave techniques. The finite time domain method has proven to be the most flexible modelling

method even though it typically requires intensive computational time and large memory allocation. Since these models are lossless in the case of shielded structures and include radiation loss for the open ones, the improved performance observed in many of the chosen circuits is due to the reduction in the radiation loss caused by planar discontinuities. Finally, the most significant impact of this technology has been seen through the implementation of the continuous via channel that defines the lower shielding cavity. This channel provides direct contact between the upper circuit ground plane of the coplanar waveguide and ground of the lower shield, thereby eliminating the substrates modes that may have been excited under normal operation.

The "in-line" package has been extended to consider paths that are non-linear for the development of conformal packages which have been realized for in a detector mounting structure and a double right angle bend. The flexibility of micromachining techniques is illustrated through these examples and indicates the potential this concept offers to accommodate a variety of planar designs that are common to high frequency circuit design. The issues associated with the cross tee-junction and bends have been discussed and appropriate compensation techniques have been instituted to ensure the realization of the desired cavity geometry requirements. The performance again has been shown in comparison to an open structure for the right angle bend example and indicates goods results in the given frequency range.

In conclusion, the monolithic integration of a shielding cavity to planar circuit design has produced a packaging concept that minimizes the effects of substrate mode excitation and package resonances. The resulting performance improvements are consistent with earlier predictions made in 1991 regarding novel planar circuit technology [11] for the "self-packaged" topology that is represented by a micropackaged cavity surrounding a individual circuit elements. The results obtained for the various topologies show good agreement between measured data and theoretical predictions for the basic high frequency components realized herein. As a result, successful development and characterization of the self-

packaged topology has been achieved and the objective to realize a monolithic package using micromachining techniques for high frequency applications has been satisfied.

CHAPTER V

MICROMACHINED MICROSTRIP ANTENNAS

5.1 INTRODUCTION

High speed systems that are lightweight and small in size require electronic circuits that operate at faster rates with optimum performance. For electronic products in the area of personal communication systems (PCS) and wireless telecommunications, demand for more compact designs with faster operation is increasing. Antennas, such as the microstrip patch, have tremendous potential in today's market to meet such demands. Thus far, its use in microwave and millimeter wave applications has been greatly influenced by its simplicity, conformability, low manufacturing costs [73] and vast availability of design and analysis software. Faster operations and reduced circuit size requires an increase in the frequency of operation and high dielectric constant materials. These requirements, however, have adverse effects on patch antenna performance since the excitation of inherit electromagnetic effects, namely substrate modes, can deteriorate the antenna performance.

Antenna efficiency and bandwidth improvements can be achieved with the reduction of substrate modes in the form of surface waves. Consequently, the radiated power that is typically lost to this mechanism can be focused into more useful space waves. While theoretical models (i.e. quasi-static and full-wave) and experimental data exist that provide insight on the effects of this mechanism, novel design approaches are still required to reduce its excitation. Using the techniques employed to develop high frequency micromachined circuits, alternative solutions are available to aid in the suppression or elimination

of these modes. With specialized processing and advanced design/modelling techniques. these undesired effects can now be accounted for and reduced or eliminated.

Specific to patch designs, optimum performance is dependent on the choice of material and feeding technique applied. Traditional designs have been implemented on low dielectric materials that are electrically thick in order to obtain high efficiency and broad bandwidth [74]. To address the compact design issue for current RF applications however, high dielectric materials are required to provide reduction in physical dimensions. Unfortunately, antenna performance suffers severely in these environments unless surface wave excitation is controlled. The problems associated the excitation of these modes are more pronounced in the high dielectric constant materials than low dielectric ones and results in higher power losses. Since antenna performance is degraded [78-79] when the surface wave power increases, the gain of the antenna is also reduced. To accommodate the requirements imposed by both the passive circuitry and the antenna element, novel geometries can now be realized using silicon micromachining. This technique can be used to selectively alter the substrate underneath the antenna thereby locally reducing the dielectric constant and the amount of material available to support surface waves.

This chapter presents the development and characterization of such an antenna that has been fabricated to provide a reduced "effective" dielectric constant underneath a patch. The characterization includes both theoretical and experimental data for a microwave model as well as the performance of a Ka-Band antenna element. The discussion will begin with a brief summary of microstrip patch antenna design based on an intuitive perspective. The characterization method employed evaluates the design on a microwave model made of Stycast (ε_r=12) that simulates the antenna in a silicon environment. The specific design is then analyzed using full-wave methods prior to the fabrication of the high frequency antenna. Once the micromachined antenna has been realized, the performance is characterized through the measurement of the return loss and radiation pattern. While impedance and radiation patterns are used to evaluate the antenna performance,

these alone cannot provide conclusive results regarding surface wave reduction. The finding of the return loss and radiation thus far are quite encouraging and support future investigation of substrate mode behavior. The existence or reduction of surface waves must be evaluated in terms gain or efficiency measurements and is beyond the scope of this work.

5.2 MICROSTRIP ANTENNA DESIGN AND ANALYSIS

The concept of the microstrip antenna originated in the 1950's [81] and since that time has been explored extensively to provide design and analysis tools for practical design applications. The microstrip patch consists of a lower conductor that functions as the ground plane and an upper conductor that behaves as a resonator (Figure 5.1). In its sim-

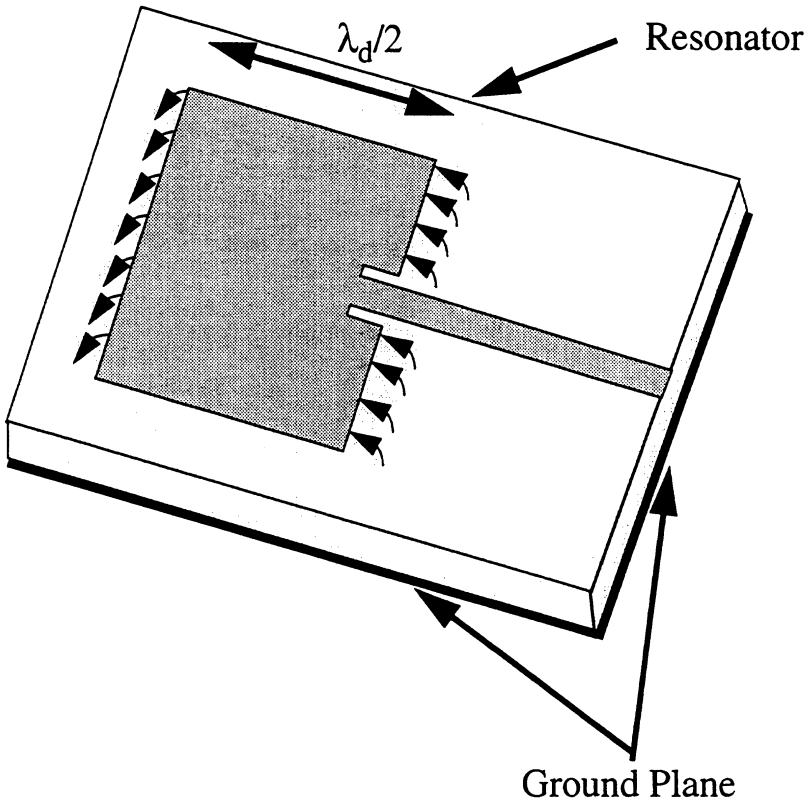


Figure 5.1 Microstrip Patch Antenna.

plest form, rectangular or circular shapes have been used and are easily arrayed in many applications over a broad frequency spectrum (400 MHz to 40GHz). Recently, it is being considered in anti-collision avoidance radar systems that operate at 77 and 94 GHz. The popularity of this antenna will continue to increase since it offers simplicity and ease in fabrication with conventional planar circuit designs.

Design and analysis tools predict antenna parameters such as the resonant frequency, radiation resistance, radiation pattern, gain, directivity and efficiency and range from simple analytic models based on circuit theory or modal analysis to complex ones based on full-wave methods. The former models have the advantage of providing analytic expressions and offer good intuitive perspectives on the physical behavior of the antenna whereas the latter offers solutions to the short-comings of the intuitive approach by accurately evaluating the physical phenomena present in the structure. Practically speaking, both design approaches are still employed where the analytic method is used on simple geometries such as a rectangular or circular patch to provide fast simple results. Full-wave methods, on the other hand, are necessary in the analysis and evaluation of any complex patch geometry, feeding mechanisms, and array designs and offer the most accurate results. Since the antenna in this work is a single rectangular element fed by an inset microstrip line, the intuitive approach will be discussed in the following section since these offer excellent understanding of the patch behavior.

5.2.1 Transmission Line Model

To understand antenna parameters from a basic transmission line theory approach, the patch can be viewed as two radiating slots separated by one half a guided wavelength (λ_0) at a given design frequency (λ_d),

$$\lambda_d/2 = \lambda_o/(2\sqrt{\varepsilon_r}). \tag{5.1}$$

In this model each slot of length *a* is viewed as a narrow slot radiating into a half-space and as a 2-element broadside array where *a* is less than a wavelength and is typically chosen to be half the free-space wavelength in order to reduce the excitation of higher order modes. If the fringing fields are neglected, the resonant frequency can be determined by $f_{ro} = c/(2b\sqrt{\varepsilon_r})$, even though, the fields associated with the fringing capacitance of each slot invariably cause the effective distance between the radiating edges to be slightly larger than the actual separation distance *b*. To compensate for this phenomena, a filling factor *q*, shown in Eq. 5.2 is incorporated which correlates the measured resonance to the calculated resonance and is typically in the range of $0.48\lambda_d < b < 0.49\lambda_d$.

$$f_{ro}^{act} = q\frac{c}{2b\sqrt{\varepsilon_r}} \tag{5.2}$$

The input resonant resistance, R_{in}, shown in Eq. 5.3 is determined from the admittance of each slot [82] and is approximately 120 ohms for a rectangular patch whose radiating edges are half the free-space wavelength separated by half of the guided wavelength in the substrate,

$$R_{in} = \frac{1}{2G_{in}}. \tag{5.3}$$

While the above model provides an easy analog to circuit theory, this approach neglects some basic physical parameters which limit its accuracy. Some of these disadvantages include the restriction to patches with rectangular shapes, empirical determination of the fringing factor *q*, exclusion of the feeding mechanism as well as possible field variations along the radiating edge.

5.2.2 Modal-Expansion Cavity Model

A different approach that inheritly accounts for some of these physical phenomena is based on the *modal expansion model*. The resonant resistance is derived from the radiation and capacitance of the patch for a cavity model having dominant TM_z modes and describes the radiation resistance in terms of the substrate thickness and feed point location. For edge fed antennas, the resistance is typically varies between 100 and 200 ohm for length/width (a/b) ratios of 2:1 with edge fed antennas. In thin substrates this dependance has the strongest impact since the radiation resistance behaves as $\cos^2(\pi y_o)/b$ and rapidly changes when the slot width is very small. For patches with inset feeds, the resonant resistance is given by Eq. 5.4 indicating the cosine square variation between the two radiating slots,

$$R_{rad} = R^e_{rad}\cos^2\left(\frac{\pi y_0}{b}\right). \tag{5.4}$$

The reader is referred to [73], [83] for a more thorough treatment of the modal expansion model.

Finally, the shape and parasitic effects of the resonator as well as multilayer and array configurations can be evaluated using sophisticated full-wave analysis techniques. Although a detailed discussion is not presented here, these are based on method of moments, finite difference time domain (FDTD), finite element, etc. and provide very accurate analysis techniques for high frequency designs [74]. The following books [75-77] offer comprehensive discussions and extended references on microstrip design and analysis while a variety of full-wave methods are summarized in Pozar's book on Microstrip Antenna Design [80].

5.3 ANTENNA CHARACTERIZATION

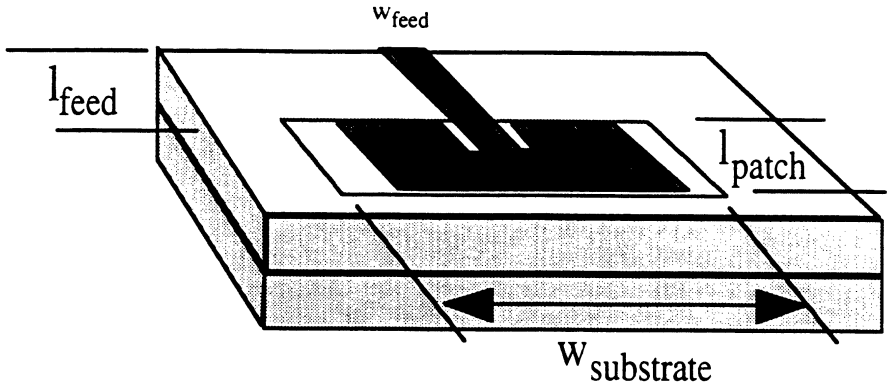
The design approach taken here represents one of a variety of schemes to reduce the dielectric constant of a known substrate and is based on localized lateral removal of material underneath the patch using micromachining techniques. Initially, a low frequency microwave model is implemented and analyzed to refine the circuit design. Next, the corrected circuit design is scaled to the appropriate high frequency design and realized using micromachining techniques. Lastly, the antenna performance is evaluated for input impedance and radiation patterns.

5.3.1 Low Frequency Antenna Design

A low frequency version is first designed using the program PCAAD [85] to model the response of the patch on high and low "effective" dielectric materials. Once determined, the design is realized in a scaled model that replicates the "effectively" reduced dielectric constant. The design parameters are obtained for this antenna and then scaled to the design frequency of 20.28 GHz and analyzed using FDTD full-wave method [86].

The rectangular patch in the low frequency scaled model design uses Stycast material with an effective dielectric constant, $\varepsilon_r = 12$ and is geometrically similar to the one shown in Figure 5.2. To reduce the effective dielectric constant underneath the patch, a 50% Stycast - 50% air medium is created which have thicknesses of 6.6 mm each in the patch region while the microstrip feedline is placed on 13.2 mm thick Stycast. By reducing the thickness of the high index material under the patch, the "effective" dielectric constant is lowered. The antenna based on the design parameters from PCAAD is measured and experimentally tuned using copper tape to the model frequency of 1.075 GHz (Figure 5.3). Since the radiating edge of the patch has a large impedance, an inset 50 ohm microstrip line is used to achieve the necessary match between the 50 ohm feed line and the microstrip patch.

(a)



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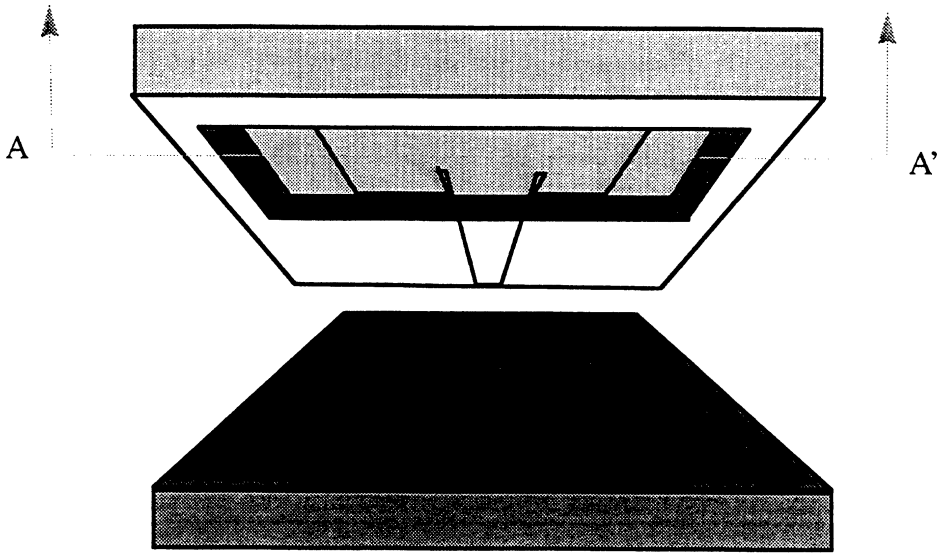
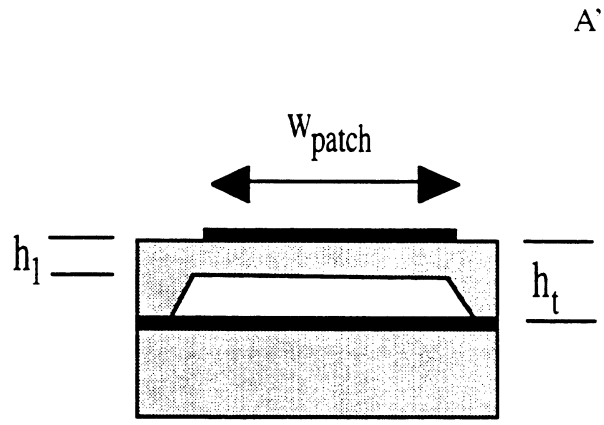


Figure 5.2 Illustration of the micromachined patch antenna configuration. (a) The micromachined patch configuration where the specific parameters are defined in Figure 2. (b) The area below the patch shows where the material has been removed laterally to form an air/dielectric cavity.



(a)

Parameter	Value(mm)
l_{feed}	50.88
l_{patch}	68.26
x	4.76
$w_{substrate}$	153.03
w_{patch}	65.09
h_t	6.6
h_1	3.3

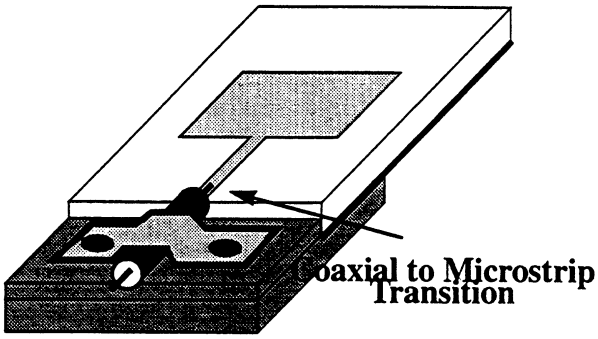
(b)

Figure 5.3 Microwave Model circuit dimensions for the Microstrip Patch Antenna on Stycast, dielectric constant =12.

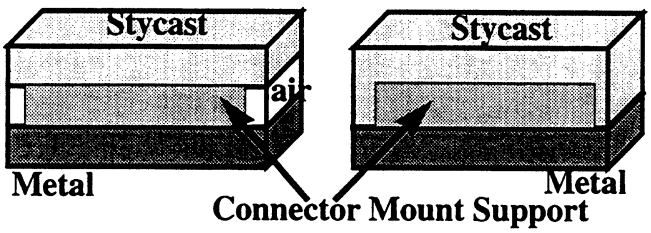
Two cases were initially investigated for the feed line; one has the feed on the mixed dielectric and the other on a continuous dielectric material. The latter was chosen since any reduction of dielectric constant in the area of the feeding network will increase the overall dimensions of the feeding circuitry. In addition, while the mixed substrate under the feedline increases the range of impedances, matching requires an additional trans-

former to match the antenna to the 50 ohm measurement system. By using an inset microstrip, tuning flexibility exists since the slots can be filled after fabrication to tune the antenna.

The low frequency model input response is measured on an HP 8720 Network Analyzer after a full two-port calibration. An electrical delay is incorporated to establish a reference plane at the tip of the coaxial probe, then the probe is soldered to the tip of the test antenna. Figure 5.4 shows the measurement apparatus drawing of the microwave model.



(a)



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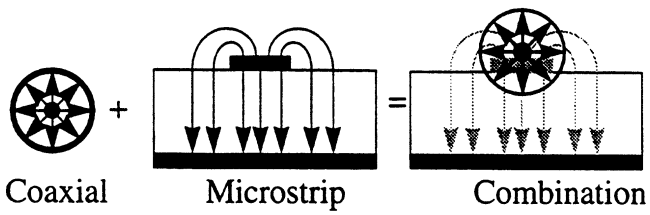


(c)

Figure 5.4 Microwave Model Measurement apparatus

The ground connections required to ensure DC contact between the coaxial cable and the antenna is achieved via the metallic block and the lower microstrip ground of the antenna. This grounding arrangement is used for both the air/dielectric substrate and the dielectric only substrate. Of the two feeding approaches, the continuous dielectric has the best transition of the electric field from the probe into the substrate and proved to be the most repeatable arrangement for exciting the microstrip mode (Figure 5.4b and Figure 5.4c).

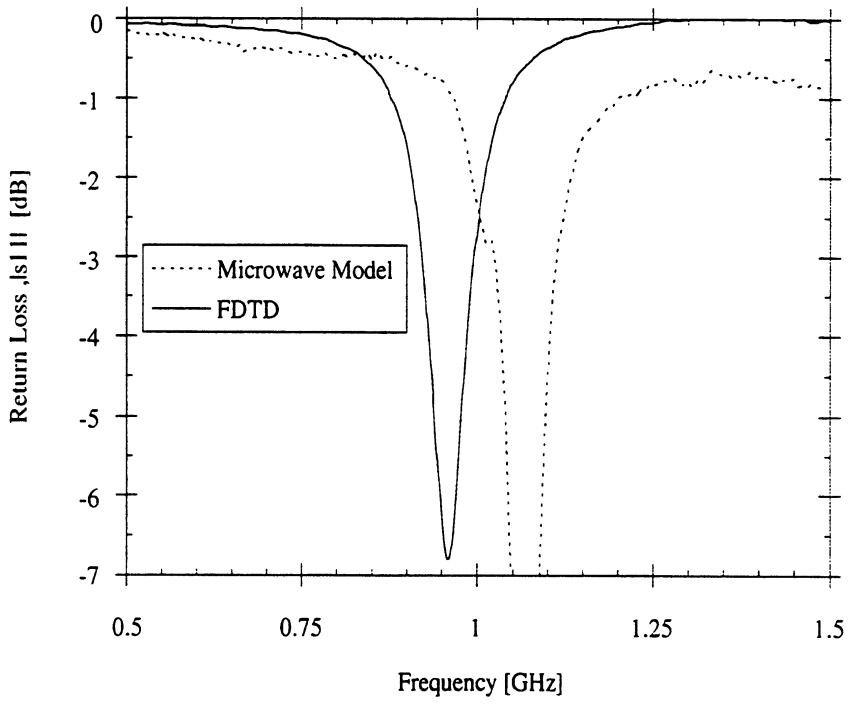
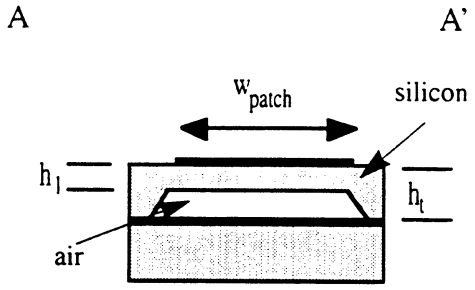


Figure 5.5 Microwave model results.

The return loss of the patch shown in Figure 5.5 is between the microwave model and the theoretical results obtained from the finite difference time-domain method (FDTD) [86]. The high frequency patch design is modelled first on a silicon substrate, then scaled to the low frequency design and compared to the Stycast model. Since the scaled model has large dimensions, this requires the generation of an extremely large mesh and consequently large computational times. Therefore the high frequency case is modelled since



Parameter	100%(mm)	50-50%(mm)
l_{feed}	2.692	2.692
l_{patch}	2.019	3.616
w_{feed}	0.286	0.286
$w_{substrate}$	-------	8.108
w_{patch}	4.08	3.445
h_l	-------	0.165
h_t	0.355	0.355

Figure 5.6 The diagram is a side view of the patch cross-sectional area and the table shows the circuit dimensions of the patch antenna shown in Figure 1.

the dimensions are smaller and the results are then scaled to the low frequency one. The measured and theoretical results are quite similar except for the 100 MHz shift. This can be attributed to the resolution lost during the scaling process, choice of discretization size, and the close placement of the absorbers on the side of the patch. In this case the comparison is adequate for some establishing theoretical prediction of the expected high frequency response although in practical applications these issues must addressed.

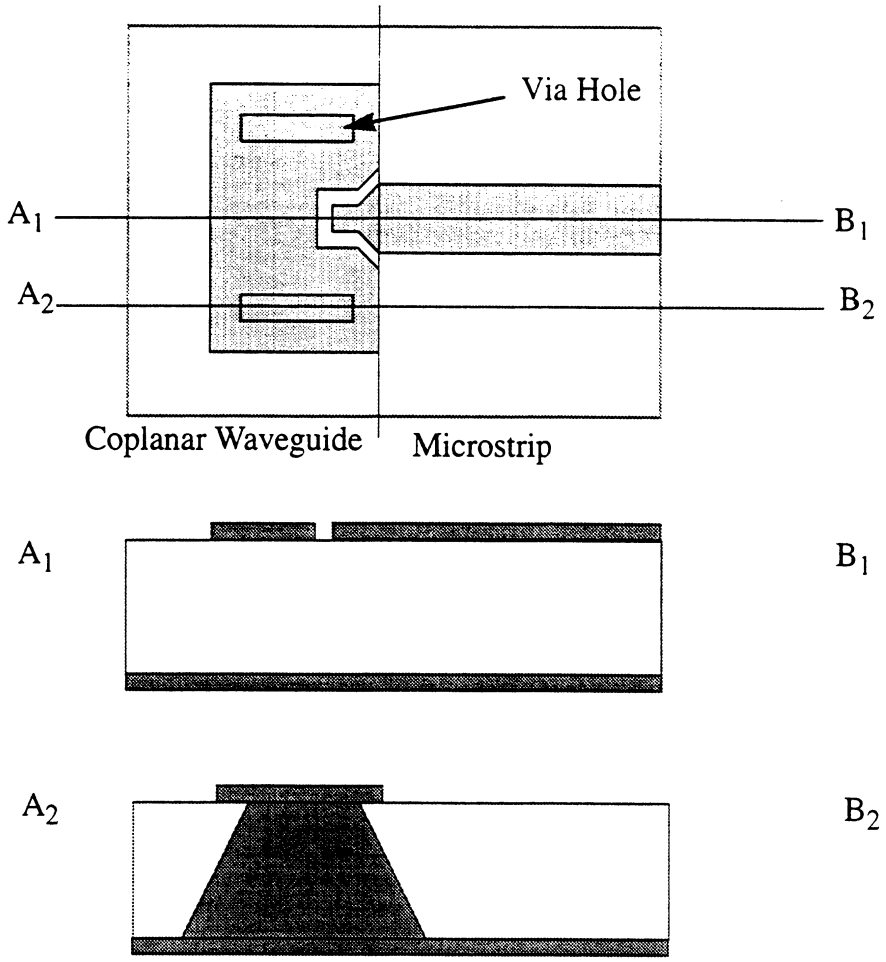
5.3.2 High Frequency Antenna Design

5.3.2.a Fabrication Procedures

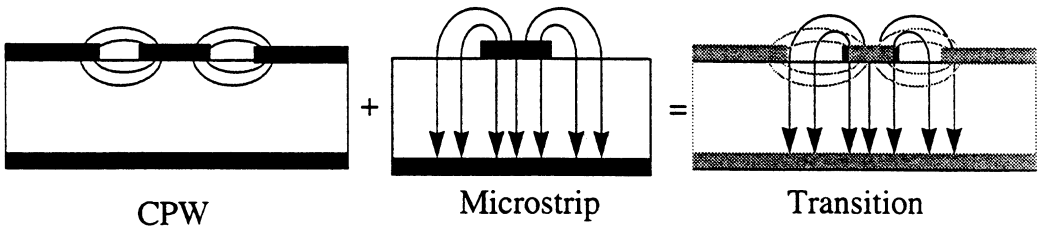
In the high frequency approach, the 20.28 GHz design is fabricated on a silicon using micromachining techniques. In Figure 5.6, the silicon is chemically etched away underneath the patch antenna to approximately half of the wafer thickness in the lateral direction to form a mixed dielectric medium of silicon-air. For specific dimensions see the Table in Figure 5.6 for both the 100% patch and the micromachined one. In this design a single etch step is required to remove the material from underneath the patch and it follows similar procedures to those in Chapter 2 for etching a single sided wafer. The metallization of the patch is electroplated to approximately 3.2 microns thickness. The lower ground plane is achieved by using adhesive copper tape of thickness 25.4 microns. In an earlier phase of the experiment, an aluminum sheet was epoxied to the sample however, the large difference in the thermal coefficient of expansion between the metal and silicon caused severe warping of the wafer during cool down phase. Therefore copper tape method is used as the ground plane and this antenna is then mounted on the thicker metal ground plane of the test fixture.

5.3.2.b Antenna Performance: Return Loss and Capacitor Model

The antenna is first evaluated on the probe station to determine the resonance of the patch. Measurements in the 10 to 40 GHz range are taken using computer controlled HP 8510 Network Analyzer, Alessi Probe Station, and Cascade Microtech coplanar waveguide probes. An SOLT calibration is employed to the establish the reference plane between the probe and feedline. Since the DUT is a radiating element, the microscope present in the measurement set-up was moved and found to have negligible effects on the resonance. In this design, the transition requires launching of the fields into the microstrip patch via coplanar waveguide (see Figure 5.7), therefore via trenches are used to connect



(a)



(b)

Figure 5.7 Transition from cpw to microstrip. (a) Top view of CPW transition to microstrip. (b) Field distribution between two planar circuits.

the ground plane of the CPW to the microstrip line. In order to obtain a good transition, the vias must be secured to a lower metal wafer with silver epoxy to ensure conversion from the cpw mode to the microstrip mode with minimal excitation of higher order modes. Without this procedure, the response is very noisy and the loss due to the conversion of the two field distributions is very high.

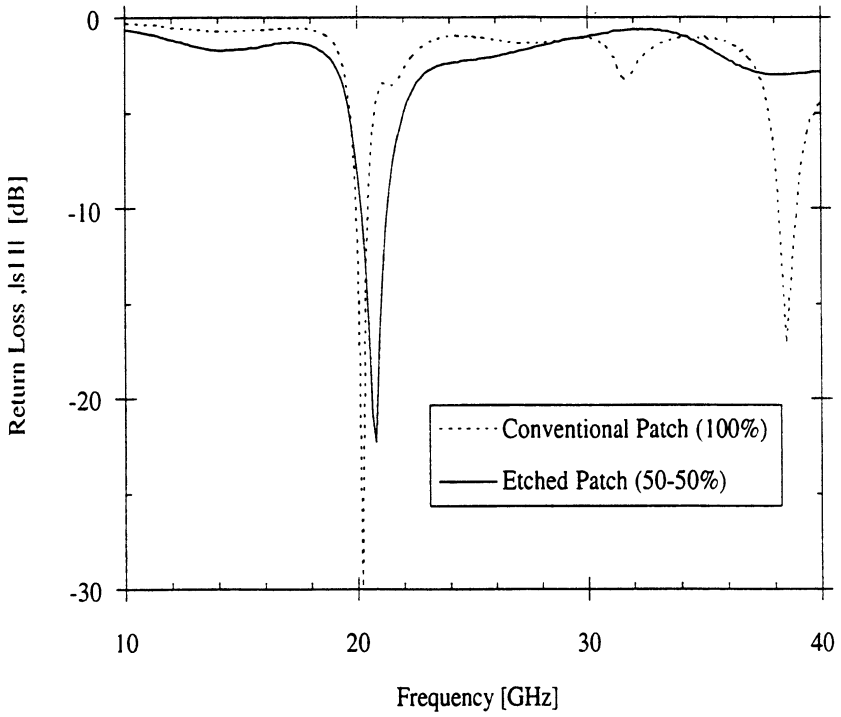


Figure 5.8 Measured results for the patch antenna on conventional 100% silicon and 50-50% silicon-air substrate.

Measured results are shown Figure 5.8 for the 20 GHz patch on silicon substrate and on the micromachined substrate. This indicates that the patch implemented on the unaltered high index material shows the effects of the higher order modes in addition to the slight excitation of surface waves observed in the non-symmetric response at 20.4 GHz.

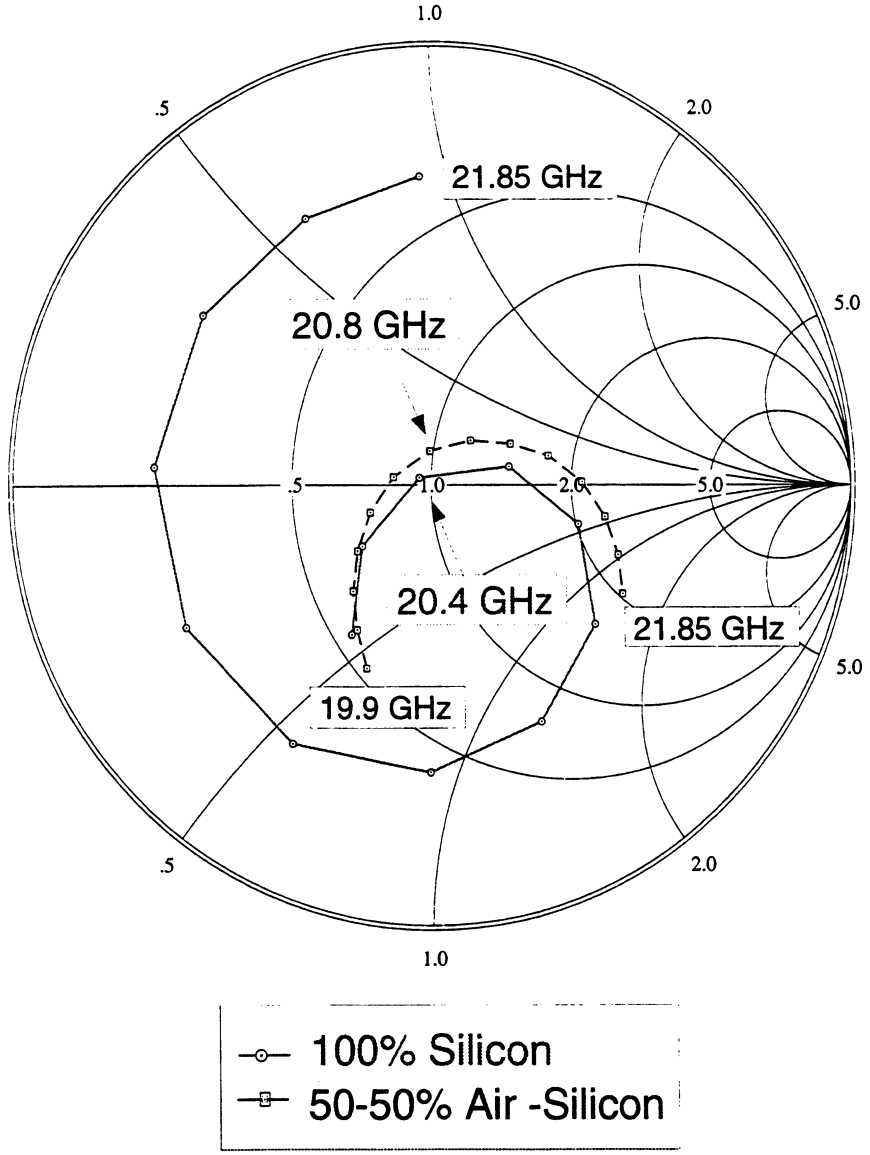


Figure 5.9 The Smith Chart illustrates the improved bandwidth between the micromachined antenna and the conventional one.

For the patch design on the reduced "effective" dielectric constant, the resonant frequency is 20.8 GHz and shows more symmetry indicating that the power lost to substrate modes are reduced. At the upper frequency, the previously observed higher order mode has been shifted out of the measurement range and the bandwidth of the micromachined antenna at -10 dB return loss increases from 2.9% on the regular substrate to 5% on the cored one. Bandwidth is inversely proportional to the The quality factor, Q, is defined as the ratio of

total stored energy in the antenna to the energy dissipated or radiated per cycle, and is inversely proportional to the bandwidth, BW. From the Smith Chart plot shown in Figure 5.9 the Q decreases since the BW is increases for the etched antenna.

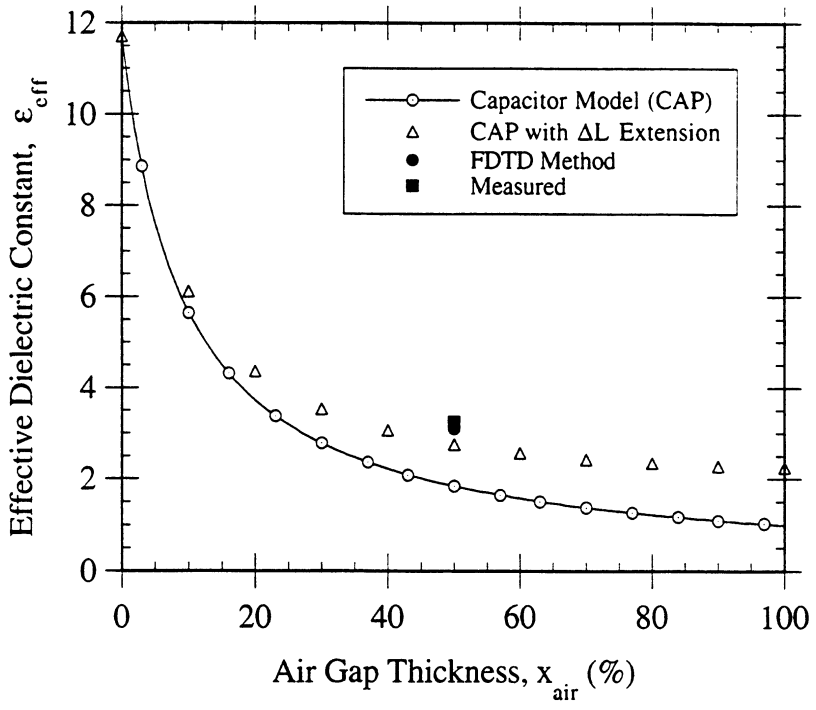


Figure 5.10 Plot of the effective dielectric constant for mixed substrates.

To predict the effective dielectric constant of a mixed substrate medium, a quasi-static model based on series capacitors can be derived. The derivation of the approach is described in APPENDIX D. In Figure 5.10, the plot shows the behavior of the effective dielectric constant, which is proportional to the capacitance of the patch,

$$C = \frac{\varepsilon_r \varepsilon_o A}{d}, \text{ where } \varepsilon_{eff} = \varepsilon_r \varepsilon_o. \tag{5.5}$$

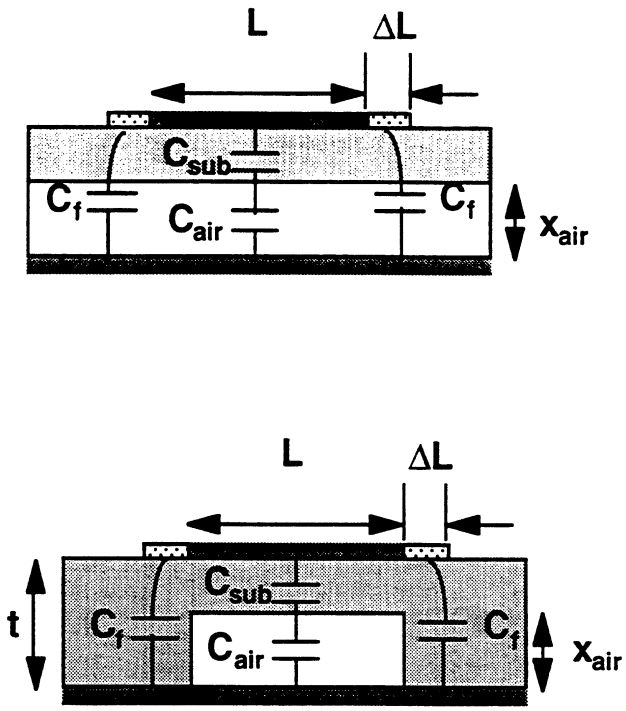


Figure 5.11 The patch antenna and equivalent circuit model used in the capacitor model. C_f is the fringing capacitance, C_{sub} is the substrate capacitance, C_{air} is the capacitance due to the air, t is the total distance between the plates, x_{air} is the height of the air region, L is the resonant length of the antenna and ΔL is the open end effect extension length.

Derivation from the capacitance model yields the following results for the determination of the effective dielectric constant.

$$\varepsilon_{eff} = \frac{C_{total}}{\varepsilon_o} \cdot \frac{d}{A} \text{ and} \tag{5.6}$$

$$\varepsilon_{eff} = \frac{\overline{C}_{total}}{\varepsilon_o} = \varepsilon_{air,\,sub}\left(1 + 2\Delta l \frac{\varepsilon_f}{\varepsilon_{air,\,sub}}\right), \text{ where} \tag{5.7}$$

$$\frac{\varepsilon_f}{\varepsilon_{air.\,sub}} = \frac{\varepsilon_{r1}t + (\varepsilon_{r1} - \varepsilon_{r2}t)\,t_{air}}{\varepsilon_{r1}t + (\varepsilon_{r1} - \varepsilon_{r2})\,t_f}$$
$$\varepsilon_{air.\,sub} = \frac{\varepsilon_{r1}\varepsilon_{r2}t}{\varepsilon_{r1}t + (\varepsilon_{r1} - \varepsilon_{r2}t)\,t_{air}} \tag{5.8}$$

The variables are shown in Figure 5.11 and $\varepsilon_{air,sub}$ represents the ε_r in the mixed substrate region and ε_f is for the fields in the extension length region. When the thickness of the fringing field region and air region are the same, the effective dielectric constant simplifies to the case of the $\varepsilon_{air,\,sub}$ case. Therefore, when the fringing fields of the antenna radiate into the same dielectric composition that is under the patch, the effective dielectric is independent of the extension length.

The function is bounded by the presence of a continuous dielectric medium of silicon (ε_r=11.7) and air (ε_r=1) case. When the extension length due to fringing fields is included, the lower limit for the effective dielectric constant increases to 2 mainly due to the contribution of the high index substrate. A FDTD model for a thru line on a 50% mixed substrate of silicon and air predicts a value of 3.1 while computed effective dielectric constant from measured response of the micromachined antenna is 3.4. Therefore, this simple model with the open end effects can predict the expected dielectric constant within approximately 15%, while the full-wave prediction is approximately 8.8%.

5.3.2.c Antenna Performance: Pattern Measurements

Pattern measurements[1] are obtained for the micromachined patch antenna using OS-50 coaxial connector in the fixture design illustrated in Figure 5.12 and is then mounted on a pedestal that has horizontal rotation only. Since the E-field of the horn antenna points vertically, the H-Plane pattern is obtained by rotating the patch in the horizontal direction. To obtain the E-plane pattern, both transmit and receive antennas must be rotated by 90

1. Measurements were taken at NASA Lewis Research Center in the Low Frequency Antenna Laboratory. See the Appendix for a description of the system set-up.

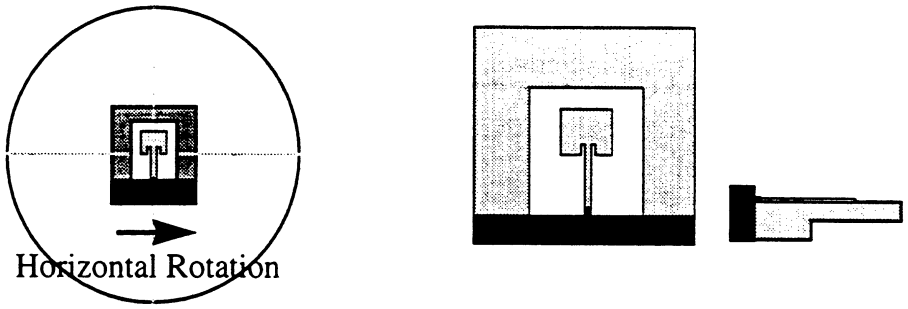


Figure 5.12 Test Fixture apparatus for the pattern measurements.

degrees and similar rotation is used to obtain the field pattern. In this case the rotation angle is actually in the direction of the antenna's feedline. In Figure 5.13, the H-plane pattern is very symmetric for this antenna since the feedline is in normal to the direction of rotation. On the other hand, the E-plane pattern has a ripple at boreside due to the presence of the feedline in the direction of rotation. To reduce the effects of the radiating feed and the coupling from the coaxial connector, absorber is placed over the input line.

5.4 SUMMARY AND FUTURE WORK

Microstrip antennas have been successful developed using micromachining techniques, which produces a reduced effective dielectric constant underneath the patch. The development has been approached from a low frequency scaled model design and the high frequency micromachined one. The low frequency design has been scaled and modelled using finite difference time domain methods to predict the high frequency response. The resolution chosen for the mesh discretization can have a strong impact on accurate predictions of the resonant frequency for the antenna elements since the placement of the feedline point inside the patch is critical. The distance between two radiating edges has an impedance variation of cosine squared and it may be difficult to locate the impedance that

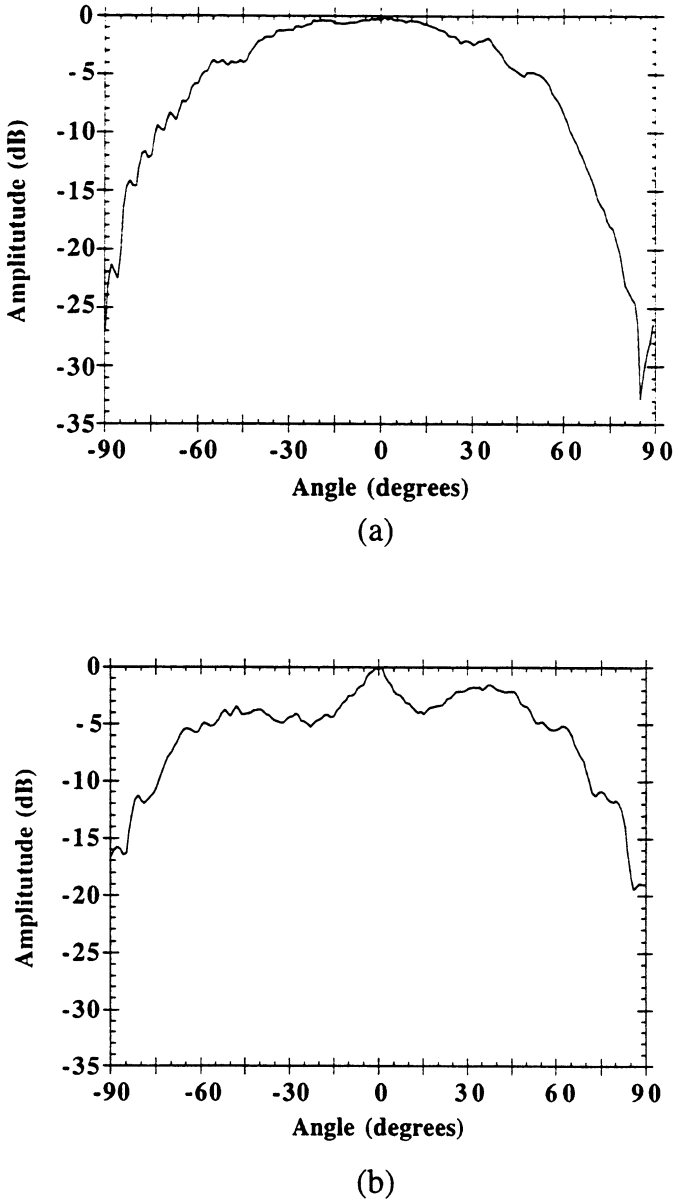


Figure 5.13 Radiation Pattern of the Micromachined antenna.

matches the feed in the model without finer mesh definition. Even though the FDTD is a flexible analysis option for this type of open radiating structure, an enormous amount of computational memory allocation is required.

Two versions of the high frequency design were implemented, one on the unaltered high dielectric material and the other on the etched substrate. A plot and Smith Chart of the return loss are shown for the two antennas and indicates impedance bandwidth

improvement due to the presence of the air/dielectric cavity. The larger bandwidth reflects an increase in the radiated power between the etched antenna compared to the conventional one.

In the future, to clarify and develop an understanding of the mechanisms that affect antenna performance, gain or efficiency measurements must be obtained. Surface wave excitation is a common problem in many high dielectric constant materials and their presence is best determined though measurements based on power consumption. Recently several approaches have been taken to illustrate the impact of surface wave excitation on laminate substrates such as duroid and gallium arsenide substrates [78-79]. Since the amount of radiated power is indicated through gain or efficiency measurements, this will provides true measure of the amount of surface wave reduction that occurs using this micromachining approach.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSIONS

An experimental approach to packaging for high frequency circuit applications has been presented that concentrates on the development and characterization of a novel concept for planar circuit self-packaging using micromachining techniques. The motivation for this work is in response to the shortage of adequate packaging design rules and schemes available for high frequency circuit design. Various design and analysis tools are readily available and have been used in conjunction with state of the art processing techniques from the MEMs community to realize this package using silicon micromachining techniques. As a result, a variety of novel geometries that inhibit unwanted mechanisms common to planar transmission lines have been realized based on this monolithic self-package topology.

The main contribution of this work is the development and extensive characterization of this monolithic micromachined package or micropackage. The treatment of the concept is divided into two main parts, "in-line" and "conformal" packaging. The first one, referred to as "in-line" package, provides metallic shielding that surrounds a coplanar waveguide based transmission line in the upper and lower half-space. This cross-section is extended in one direction longitudinally to accommodate a variety of basic circuit designs such as the through line, series tuning stubs, and filters. The second, or conformal package, is based on the aforementioned cross-sectional topology and is then extended in a

non-linear way to follow the direction of the line or to accommodate multiple input paths. In the specific case of the conformal micropackage, two designs have been used as illustrations of a cross-tee junction and right angle bend: (1) a detector mounting structure and (2) a double right angle bend. The introduction of a packaging approach through the use of micromachining techniques has provided improvement to circuit performance in three main areas. First, substrate mode excitation has been minimized and in some cases eliminated through direct connection between the outer shielding ground and the upper planar one. Second, parasitic radiation that enhances mutual coupling between circuits has been eliminated through the incorporation of the shield. Third, package resonances have been controlled through the design of the shielding topology and exist outside of the frequency of operation.

The concept of micromachining has been extended to include planar antenna problems where a microstrip patch antenna has been investigated. Since surface waves, a form of substrate mode, can have serious impact on the performance of the antenna element, especially in the presence of high index materials, lateral removal of the substrate has been done to reduce the effective dielectric constant of the antenna. Radiation from the element is increased causing a wider bandwidth. The result of the above findings suggest a potentially viable use for this technology toward solving important antenna related problems

In summary, this dissertation has presented a novel concept for high frequency packaging based on micromachining techniques which have also been extended to address planar antenna related problems. Since it offers one approach for the monolithic inclusion of packages to microwave or millimeter wave circuit designs, the findings thus far provide encouraging results and merit further study and evaluation. There are many possible extensions of this work to address problems in the high frequency circuit design area, therefore the next section will highlight several distinct areas for future work.

6.2 FUTURE WORK

Three areas will be discussed in the following sections that will expand the current knowledge base on the use of micromachining techniques to high frequency applications. First, there are a number of processing technologies that can be employed to realize more complex and precisely defined packages. Second, package characterization can be extended to evaluate other planar lines such as stripline technology. Finally several applications will be described that illustrate extensions of this packaging concept to hermetic packages, array problems and vertical integration.

6.2.1 Fabrication Alternatives

The successful development and capability to manufacture micromachined packages will require the establishment of general process recipes that aid in the reproduction of a desired geometry. Thus far the micromachined cavity development has been based solely on standard batch processing and wet etching techniques. Moreover, the assembly of the circuit is based on adhesions methods that may be removable such as photoresist or permanent such as silver conducting epoxy. In order to make this approach viable for practical commercial applications, refinement of the geometry fabrication process and circuit assembly is required.

In the immediate future, a variety of wet and dry etching techniques should be explored to determine dimensional control, reproducibility of specific geometries, and surface roughness profiles. Although EDP has been used extensively for bulk silicon removal, the surface finish may not be appropriate for designs requiring shallow etched depths. Therefore, alternative methods such as KOH-based solutions may be required to achieve better etch depth control and surface smoothness. The utilization of mixed etching processes, consisting of two or more different etching methods, may offer an optimum solution for achieving geometry replication. For the topologies realized herein, the upper cavities have been etched from both sides to depths comparable to half of the wafer thick-

ness such that EDP-based chemical solutions were adequate. On the other hand, as the depth of the cavity is reduced to one fifth or less of the wafer thickness, a slower more controlled etchant such as KOH may be preferred to achieved the desired results. Dry etching techniques may be explored in addition since they offer very accurate image transfer. Some consideration should be given, however, to appropriate metallization techniques employed to cover nearly vertical sidewalls of the cavity. Other wet etching solution, such as tetramethyl ammonium hydroxide and water (TMAHW) [88] and aqueous amine gallate solutions [89], may offer better options for processes based on lower chemical toxicity and waste related issues. Finally, once these various etching options have been investigated on a variety of geometries, the results should be compiled into a design rule database that can be readily accessible as a design tool.

Circuit assembly is a critical issue to address for the successful integration of this packaging concept into existing designs since many systems are used in space and airborne applications that require rigorous space and flight qualification tests. At this time the assembly of the package relies on a human interface for the alignment and adhesion of the multiple wafers. Precise alignment methods for package mounting should be explored further to introduce minimum alignment errors while providing easy solutions for extension into automated procedures. Since the adhesion techniques must be permanent in practical designs, several methods can be investigated which include electrobonding, soldering, in addition to the presently used conducting silver epoxy. Successful inclusion of these modifications to the self-packaged circuit will increase consideration of this approach with existing MMIC designs that are currently being produced in industrial settings.

6.2.2 Extensions to the Micromachined Package Characterization

The self-packaged circuits presented herein are based on coplanar waveguide planar transmission lines that are supported by dielectric materials. This topology serves as the protocol for the micropackaged circuit that has been fabricated using micromachining

techniques. Since the development of this topology, filter designs at W-band [8] have been realized using this packaging concept and membrane-supported microstrip technology. There are three possible configurations that provide the maximum amount of information regarding packaging effects. These are based on the following dielectric combinations for the transmission media of the planar line configuration: (1) air only, (2) air/substrate media and (3) substrate only. Presently in the area of micromachined high frequency circuits, the concept of packaging has been applied to two of the three possible cases, the air dielectric media and the partially filled substrate package. In the air filled case, the conducting line is suspended on the a thin membrane while the partially filled dielectric media presented herein, has the conducting lines are supported on a dielectric substrate.

The last package configuration that requires investigation is the entirely filled substrate geometry that resembles stripline technology. The losses associated with this homogenous media can be evaluated to provide data on the of conductor and dielectric loss mechanisms. Using measured data, the performance of a line in this configuration, along with one in dielectric-free packaged circuits will establish an upper and lower limit for the planar line loss. Coincidentally, the number of planar line geometries that have been realized in this packaging concept will expand and thereby provide a more complete template of standard planar line geometries realized in dielectric, mixed dielectric, and dielectric-free media.

6.2.3 Applications

Even though there are a number of areas in which micromachining techniques can be employed to improve high frequency circuit performance, a couple will be highlighted next to illustrate the flexibility and usefulness of this technology. Two areas are related to packaging and antenna applications. Within the packaging arena, a vast number of arrangements can be made to incorporate a hermetic micropackage into standard MMIC technology. Hermetic package designs independent of a specific circuit elements and can

be constructed exclusively in silicon-based substrates. A hybrid approach to package formation can also be based on schemes utilizing a combination of compatible materials to form the package. Electrically the hermetic micropackage may include the appropriate dc bias and RF lines that are required to feed a conventional MMIC circuit as well as serve as a mount for the specific circuit. In this approach the potential for mass production using batch processing techniques can result in a cost-efficient methods that yield high volume output since the material costs are very low and the manufacturing technology is easily adaptable to existing ones. In addition to cases where partial shielding is required to accommodate design requirements of a MMIC circuits, silicon micromachining techniques can be used to fabricate specific sections of a package configuration.

For antenna applications, large arrays are used to achieve the desired gain and frequency selectivity in many system design requirements. While mobile communication systems depend heavily on reliable transmit and receive capability, it is equally important to reduce the size and volume of antenna elements in order to decrease the cost associated with transporting and manufacturing this electronic equipment. Micromachining techniques can be used in the development of novel array configurations that offer compact circuit design through the simultaneous integration of the planar circuits and antenna elements. The electronic circuitry will be isolated as a result of the shielding package from extraneous propagating signals and the antenna will be isolated from feedline radiation. Finally, the radiation pattern of the antenna element should show improvements as a result of increased available power due to reduced parasitics aided through the incorporation of the self-package.

APPENDICES

APPENDIX A

FABRICATION OF MICROMACHINED CIRCUITS

A.1 Upper Shielded Circuits

In this section a discussion is presented regarding the fabrication of the first generation of upper shielded cavities based on the single strip layout. In this design, a two step process was employed to provide separation of the column of cavities from the larger substrate and the desired cavity depth. The process is based on photolithographic, evaporation, and anisotropic techniques. The following steps are the procedures used to fabricate the first monolithic upper cavity wafer and is based on a two-step etching process. The masking layers used consist of the trilayer dielectric ($SiO_2/Si_3N_4/SiO_2$) with thickness of 7500/3500/4000 Å shown in Figure A.1.

1. Clean the wafers using ACE/IPA solvent solutions followed by a dehydrate bake to remove the solvents from the surface.
2. Protect one side of the wafer with a thick resist (PR 1375) prior to patterning the wafer.
3. Transfer the pattern using photolithographic techniques (PR 1375 also known as 1400-37) and develop using MF351 developing solution.
4. Remove the upper oxide layer using BHF and the middle nitride layer since a plasma etching using CF_4:O_2 (20:0.5).
5. Clean the sample and repattern to protect the cavity regions and while the remaining grooves are left unprotected.
6. Remove last layer of oxide all open regions using the BHF and clean the sample prior to the etch.

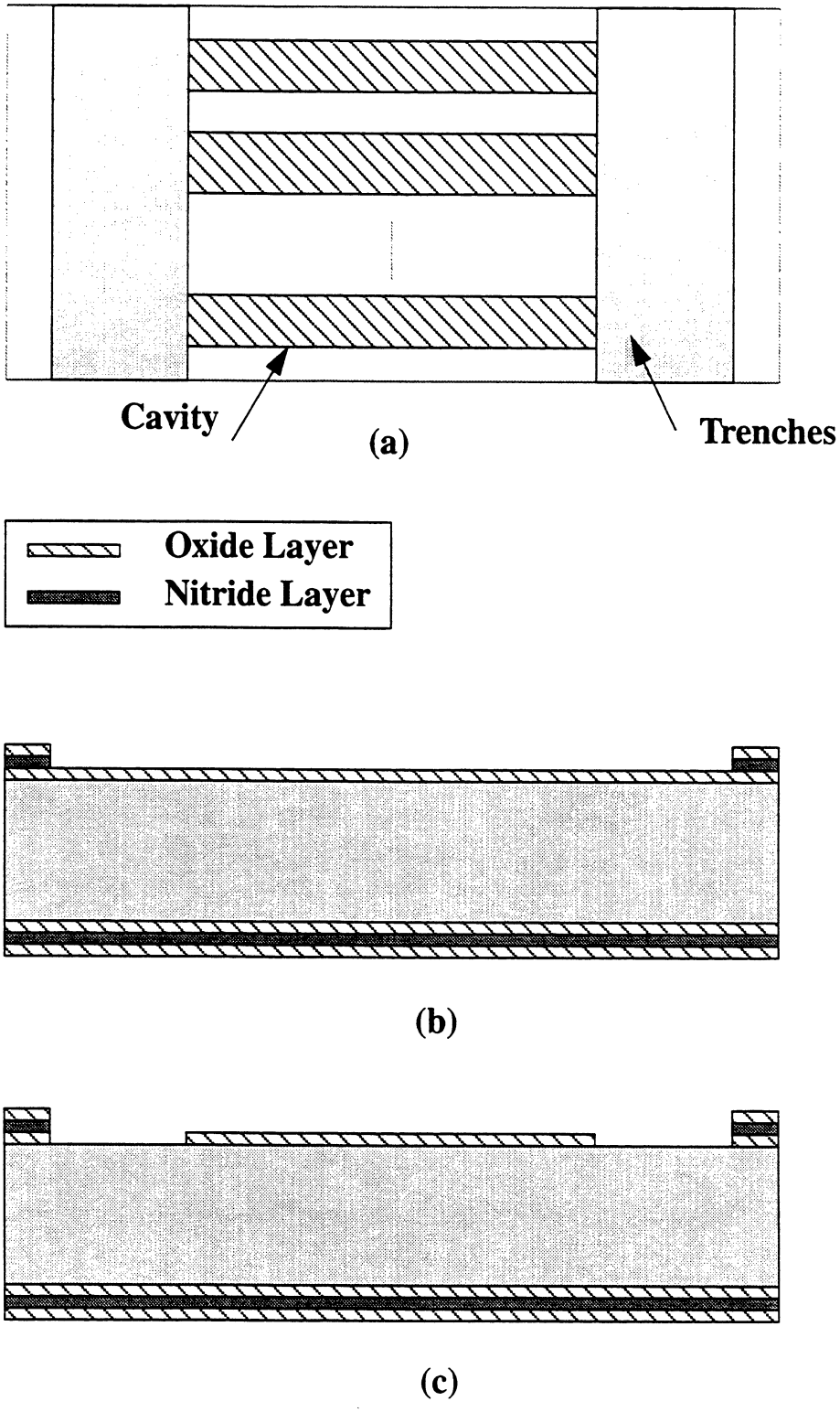


Figure A.1 (a) Top View of the cavity wafer layer scheme. (b) The removal of the oxide and nitride dielectrics to transfer the mask pattern onto the wafer. (c) Lower oxide removed from the trench regions while the oxide remains in the cavity region.

7. Heat the KOH solution consisting of KOH pellets and DI H2O (300g:300ml) to 58° C with a spin speed of 4000 rpm.

8. Place the sample in the etch until 80 microns have been removed.

9. Clean the sample as in Step 1, and perform an oxide etch in the BHF to remove the later oxide in the cavity regions (see Figure A.2). This will also remove the oxide on the outer surface of the entire wafer, however, the nitride is resilient to this etch and serves as the remaining outer masking layer.

10. Clean the sample, and return it to the KOH bath to etch the cavity to the desired depth. The depth is monitored using a calibrated microscope along with etch rulers[1] that have been included for proximity depths.

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1. Etch rulers are rectangular sections that correspond to a desired etch depth and provide a calibration parameter for determining the amount of material removed from the cavity regions.

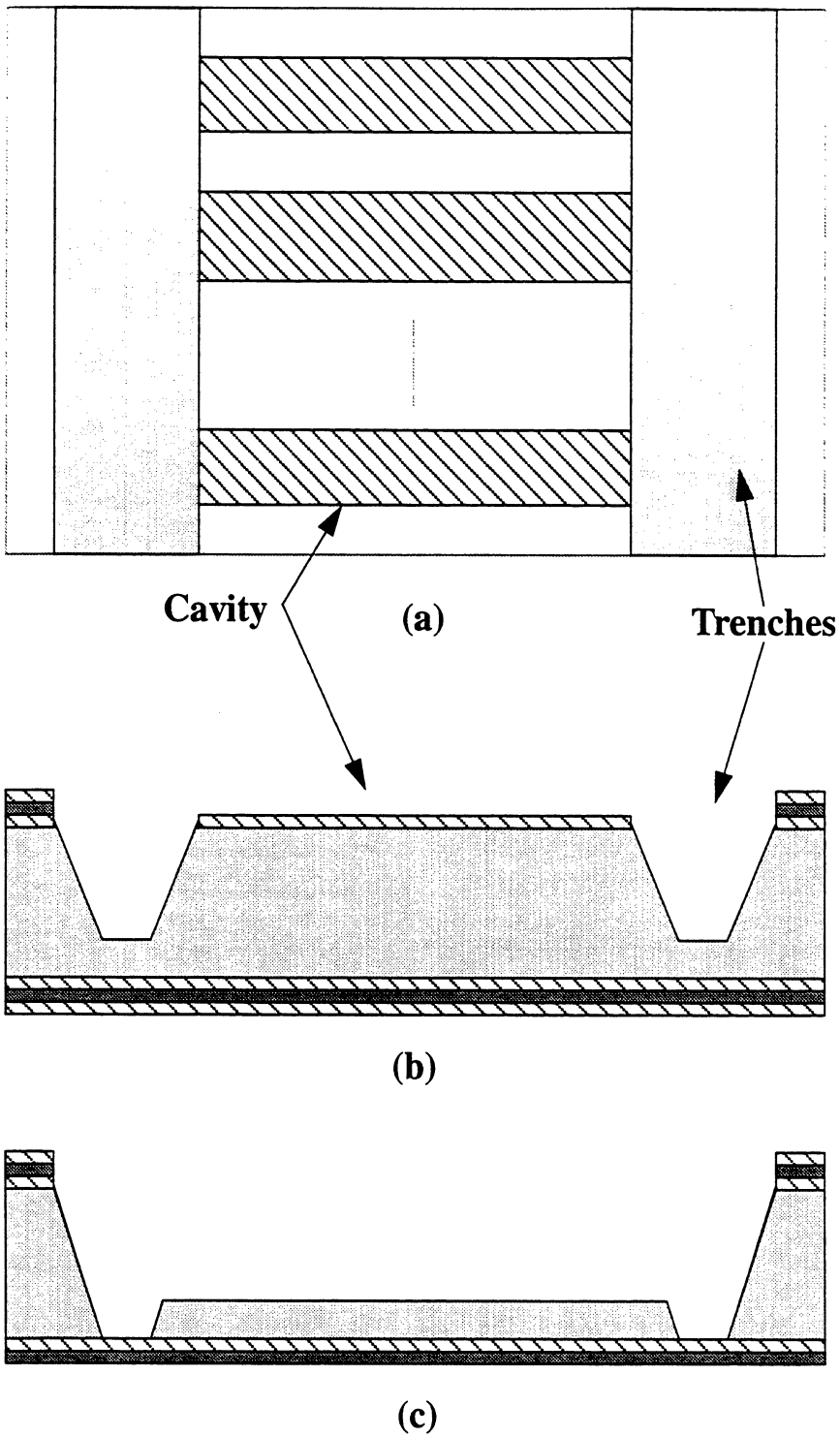


Figure A.2 (a) Top view of a section of the upper cavity wafer where the shaded sections correspond to the cavity and trench regions labeled. (b) The etch profile for the trench region, partly through the wafer. (c) The etched region completely through the wafer with the cavity region etch to the desired depth.

APPENDIX B

BILAYER METALLIZATION PROCESS

This process provides an alternative for achieving thick metallization without using plating techniques.

1. Spin clean using ACE/IPA at 3.5 krpm. Then dehydrate bake for 15 minutes at 90°.
2. Apply HMDS then photoresist Shipley 1818 (replaced Shipley 1350J) at 3.5krpm for 30 seconds. Prebake for 35 minutes at 100 °C.
3. Align and expose for 20 seconds at 10 mW/cm^2.
4. Evaporate a very thin layer (65-80 Å) of aluminum.
5. Air-spin the sample at 5 krpm to remove any particulates. Next apply the HMDS at 3.5 kprm then the Shipley 1818 photoresist at 4 krpm for 30 seconds each. Bake the resist for 30 minutes at 90°C as the prebake step.
6. Pattern and align the wafer for 20 second exposure at 10 mW/cm^2 then develop in MF 351 for 1:45 plus and addition 0:45 seconds to achieve undercut. Postbake the patterned sample for 15 minutes at 100°C.
7. Prior to evaporating, descum the wafer surface to remove any residual resist on the surface of the wafer.
8. Evaporate desired metal system. Different metal systems can be achieved to fulfill this requirement such as chromium/aluminum/gold (Cr/Al/Au) for thickness of 350Å/18kÅ/6kÅ. Soak the samples in acetone overnight for lift-off.

APPENDIX C

DERIVATION OF SYSTEM RESPONSIVITY

In this section a discussion is presented on the derivation of the responsivity of two shunted diodes in a detector circuit. The results of this derivation are shown in Chapter 4 of this thesis. The circuit diagram for the detector circuit is shown in Figure C.1. The sys-

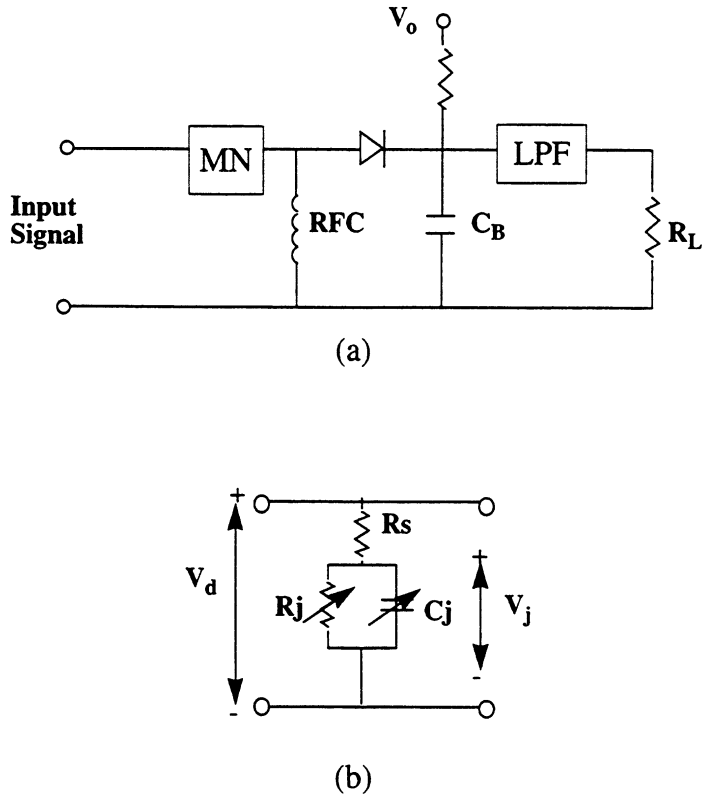


Figure C.1 General design scheme for a detector circuit, where MN is the matching network, LPF is a lowpass filter, RFC is the RF choke, and CB is the blocking capacitor. (b) The diode equivalent circuit.

tem responsivity is defined as the product of the intrinsic voltage sensitivity, β_V, RF efficiency, γ_{RF}, and the LF efficiency, γ_{LF}.

$$\eta = \beta_v \cdot \gamma_{RF} \cdot \gamma_{LF} \tag{C.1}$$

The intrinsic responsivity is based on the measured DC parameters of the diode and can be computed using the following expression [71],

$$\beta_v = \frac{0.5R_L}{\left(\frac{nkT}{qR_j}\right)(R_v + R_L)\left(1 + \frac{R_s}{R_j}\right)\left[\left(1 + \frac{R_j}{R_L}\right) + (2\pi f C_j)^2 R_s R_j\right]}, \text{V/W}, \tag{C.2}$$

where the R_s, and R_j are series resistance and junction resistance, R_v ($=R_s + R_j$) is the video resistance, Cj is the junction capacitance, and R_L is the load impedance. Junction parameters, R_j and C_j, are dependent on the bias current, I_o.

The RF efficiency is based on the equivalent circuit model shown in Figure C.2. The equations for the responsivity are given where the responsivity is defined as the voltage across the diode to the power received at the circuit terminals. The RF efficiency is defined as the ratio of power received at the diode terminals to the incident power to the circuit.

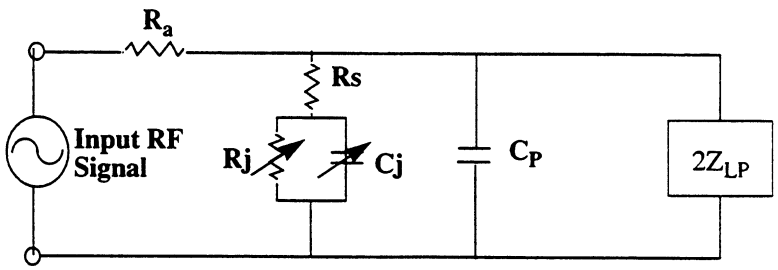


Figure C.2 Equivalent circuit the detector circuit for a single diode elements.

Therefore, the efficiency is determined from the ratio of powers

$$\gamma_{RF} = \frac{\mathrm{Re}\,(P_{dj})}{\mathrm{Re}\,(P_{in})} \tag{C.3}$$

where, P_{dj} is the power at the diode junction and P_{in} is the incident power. This results in

$$\gamma_{RF} = \frac{\mathrm{Re}\,(Z_{dj})}{\mathrm{Re}\,(Z_{in})} \cdot \frac{|Z_{in}|^2}{|Z_{dj} + R_s|^2}, \text{ where} \tag{C.4}$$

$$Z_{dj} = \frac{R_j}{1 + j\omega C_j R_j} \tag{C.4.a}$$

$$Z_{in} = \frac{Z_{pf}(R_s + Z_{dj})}{Z_{pf} + (R_s + Z_{dj})} \tag{C.4.b}$$

$$Z_{pf} = \frac{2Z_{LP}}{1 + j2\omega C_p Z_{LP}}. \tag{C.4.c}$$

The circuit elements are the junction resistance, R_j, and series resistance, R_s, junction capacitance, C_j, parasitic capacitance, C_p, and the lowpass filter, Z_{LP}, response in the measured circuit.

The low frequency efficiency, γ_{LF}, is defined as the ratio of the voltage detected across the load to the voltage detected across the junction of the diode. Lastly, this expression [90] is given as

$$\gamma_{LF} = \frac{R_L}{\sqrt{(R_L + R_s + R_j)^2 + (R_s + R_j)^2 (R_L C_L 2\pi f)^2}}. \tag{C.5}$$

APPENDIX D

EFFECTIVE DIELECTRIC CONSTANT DETERMINATION BASED ON A CAPACITOR MODEL FOR MIXED SUBSTRATES

Consider a parallel plate having dimensions corresponding to the width (w) and length(l) of a patch antenna on an etched substrate (Figure D.1). The total capacitance can be evaluated as two series capacitors based on the substrate and air region.

$$C_{total} = \frac{\varepsilon_{eff} \cdot A}{t} \tag{D.1}$$

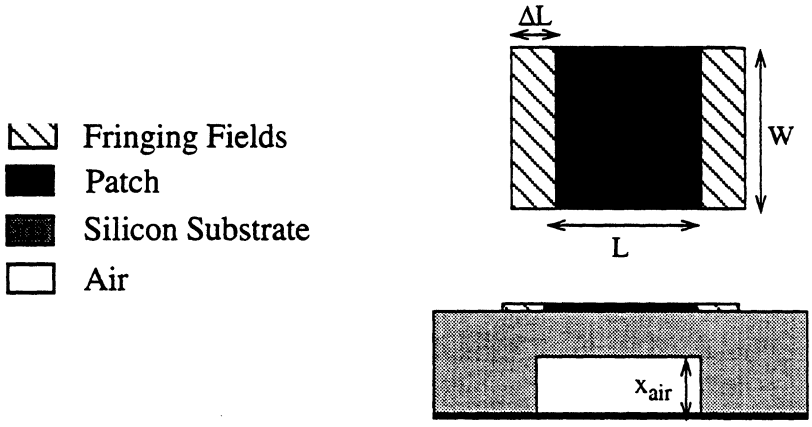
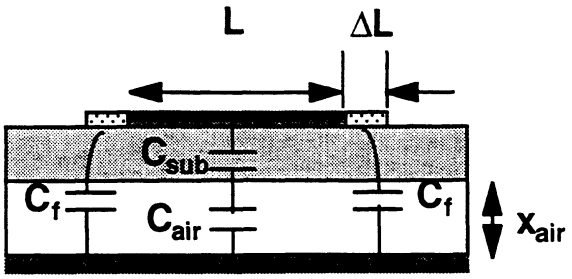


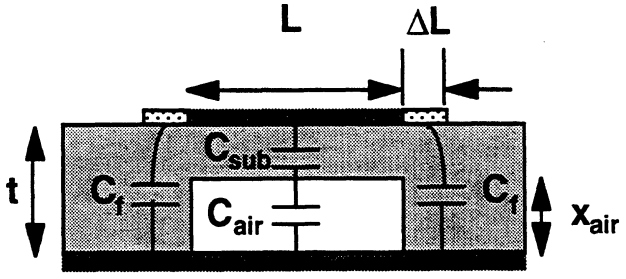
Figure D.1 Micromachined Patch Antenna used in the capacitor model.

In the two-dimensional cross section, there are two cases to evaluate. The first case is a model based on series capacitor under the metal plates that correspond to the amount of silicon and air in the patch region. Since the patch is a resonator, there is an additional

length added to the radiating edges to account for open end effects. The second case considers the open end effects radiating into the continuous silicon substrate region. The additional parasitic capacitance is included as a pair of shunted capacitance as shown in Figure D.2.



(a) Mixed Substrate only



(b) Mixed Substrate with Fringing Fields.

Figure D.2 The patch antenna and equivalent circuit model used in the capacitor model. C_f is the fringing capacitance, C_{sub} is the substrate capacitance, C_{air} is the capacitance due to the air, t is the total distance between the plates, x_{air} is the height of the air region, L is the resonant length of the antenna and ΔL is the open end effect extension length.

The equivalent circuit in Figure D.2 (a) produces a pair of series capacitors that have an area of [w by (l+2Δl)] and thicknesses x_{air} and $t_{dielectric} = t\text{-}x_{air}$ corresponding to air and dielectric thicknesses, respectively. The total capacitance can be computed based on

the following derivation. Begin with the total capacitance given by $C_1=C_{air}$ and $C_2=C_{sub-strate}$. The total capacitance, C_{total}, is determined from

$$\frac{1}{C_{total}} = \frac{1}{C_{sub}} + \frac{1}{C_{air}} = \frac{1}{C_1} + \frac{1}{C_2} \tag{D.2}$$

This simplifies to a total or normalized capacitance of C_{total} or $\bar{C}_{total}$, respectively,

$$C_{total} = \frac{\varepsilon_{r1}\varepsilon_{r2}A\varepsilon_0}{\varepsilon_{r1}t + (\varepsilon_{r2}-\varepsilon_{r1})x_1}$$
$$\bar{C}_{total} = \frac{C_{total}}{A} = \frac{\varepsilon_{r1}\varepsilon_{r2}A\varepsilon_0}{\varepsilon_{r1}t + (\varepsilon_{r2}-\varepsilon_{r1})x_1} \tag{D.3}$$

To determine the effective dielectric constant, ε_{eff},

$$\varepsilon_{eff} = \frac{C_{total}}{\varepsilon_o}\cdot\frac{d}{A}$$
$$\varepsilon_{eff} = \frac{\bar{C}_{total}}{\varepsilon_o} = \varepsilon_{air,\,sub}\left(1 + 2\Delta l\frac{\varepsilon_f}{\varepsilon_{air,\,sub}}\right) \tag{D.4}$$
$$\frac{\varepsilon_f}{\varepsilon_{air,\,sub}} = \frac{\varepsilon_{r1}t + (\varepsilon_{r1}-\varepsilon_{r2}t)\,t_{air}}{\varepsilon_{r1}t + (\varepsilon_{r1}-\varepsilon_{r2})\,t_f}$$
$$\varepsilon_{air,\,sub} = \frac{\varepsilon_{r1}\varepsilon_{r2}t}{\varepsilon_{r1}t + (\varepsilon_{r1}-\varepsilon_{r2}t)\,t_{air}}$$

When the thickness of the fringing field and air thickness are the same, the effective dielectric constant simplifies to the case of the $\varepsilon_{air,\,sub}$ case. Therefore, when the fringing fields of the antenna radiate into the same dielectric composition that is under the patch, the effective dielectric is independent of the extension length.

A similar approach can be taken for Case 2 where the fringing fields are included. The total capacitance is now represented by

$$\frac{1}{C_{total}} = \frac{1}{C_{patch}} + \frac{1}{2C_{fringe}} \tag{D.5}$$

$$C_{total} = C_{patch} + 2C_{fringe}, \text{ where} \tag{D.6}$$

$$C_{total} = \frac{\varepsilon_{patch} A_{patch}}{t} + 2\frac{\varepsilon_{fringe} A_{fringe}}{t}. \tag{D.7}$$

The area for the fringing capacitance is defined by the length Δl and width w, where Δl is defined by the open-end effect expressions [91],

$$\frac{\Delta l}{h} = 0.412\left(\frac{\varepsilon_{re} + 0.3}{\varepsilon_{re} - 0.258}\right)\left(\frac{\frac{w}{h} + 0.262}{\frac{w}{h} + 0.813}\right). \tag{D.8}$$

The remaining parameters are computed using the following expressions for the patch area based on the length, l, and width, w, and the fringing capacitance area of length, Δl, and width, w.

$$C_{patch} = \frac{\varepsilon_{r1}\varepsilon_{r2} A_{patch} \varepsilon_0}{\varepsilon_{r1} t + (\varepsilon_{r2} - \varepsilon_{r1}) t_1} \tag{D.9}$$

$$C_{fringe} = \frac{\varepsilon_{r2} A_{fringe} \varepsilon_0}{t}. \tag{D.10}$$

The final result is the effective dielectric constant based on the total capacitance and the plate area, A_{total}. A plot of the result can be found in Chapter 5 of this thesis.

$$\varepsilon_{eff} = \frac{C_{total} t}{A_{total}}. \tag{D.11}$$

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ABSTRACT

THE DEVELOPMENT AND CHARACTERIZATION OF SELF PACKAGES USING MICROMACHINING TECHNIQUES FOR HIGH FREQUENCY CIRCUIT APPLICATIONS

by

Rhonda Franklin Drayton

Chairperson: Linda P. B. Katehi

The development and characterization of micromachined self-packages for high frequency circuit applications is presented. Micromachining techniques are explored to develop packages for microwave circuits based on coplanar waveguide transmission lines. Half and completely shielded package topologies are realized as self-packaged tuning stubs elements and filters to demonstrate the capability of micromachining a microwave circuit design. The concept is extended to develop the first generation conformal package that follows the direction of an individual line path and provide multiple input access at a cross-junction to a specific line path. Lastly, micromachining is used in a microstrip patch antenna to locally reduce the dielectric constant while the feeding line is maintained on the high index material.

The package and circuit are fabricated in high and low resistivity silicon substrates, respectively, using standard photolithographic and lift-off processing techniques for pattern definition. Evaporation and electro-plating processes are used for metallization, and wet-chemical anisotropic etching processes are used for cavity formation. The planar

transmission line circuits are typically printed on a polished surface of a high resistivity silicon wafer. Lower shielding cavity formation occurs by anisotropically removing silicon material to form the sidewalls of the lower substrate-filled cavity while the upper air-filled cavity is formed by etching the actual cavity into low resistivity silicon using similar processes. Both surfaces are metallized, then the upper cavity is mounted over the circuits to form the completely shielded or self-packaged configuration. This simple two-dimensional shielding geometry extends in either a straight path, referred to as "in-line", or into bending paths, referred to as "conformal".

Passive circuit designs implemented in micromachined self-packages are experimentally characterized to evaluate the effect of this monolithic shielding on the reduction of parasitic radiation, substrate mode excitation, and package resonances. The "in-line" and "conformal" self-packaged designs are characterized using on-wafer probing techniques from 2 to 40 GHz. Basic microwave components such as series open/short tuning stubs, stepped impedance filters, and right angle bends are evaluated since these represent standard elements to many high frequency designs such as filters, switches, couplers, RF chokes, and phase shifters. The main contribution of this work is the characterization of a monolithically integrated micromachined package to planar circuits that offers reduced parasitic radiation as a result of the shielding topology. Poor performance due to the excitation of parallel plate modes in grounded coplanar waveguide circuits is eliminated with to the incorporation of the lower shielding cavity. In antenna problems, this technique has been used to locally reduce the dielectric constant of the antenna while maintaining the feeding line on the high index material. This micromachining approach impacts HF packaging designs, complex circuit designs with RF circuitry and radiating elements, as well as vertical and horizontal circuit integration at microwave and millimeter wave frequencies.