PLANNING AND SCHEDULING IN JAPANESE SEMICONDUCTOR MANUFACTURING

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Technical Report 93-17

July 1993

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1. Introduction

In this paper we describe methods used by some Japanese semiconductor manufacturing companies for long-term planning and short-term scheduling and shop floor control. We begin by providing an overview of semiconductor manufacturing and the role of planning and scheduling functions. Next, we describe our research methods. We then attempt to answer the following questions: i) what tools and techniques do Japanese companies use to do long-term capacity planning in the highly competitive and capital intensive world of semiconductor manufacturing; ii) what tools and techniques do Japanese companies use to deal with scheduling issues in the highly uncertain and volatile environment of wafer fabrication. In addition to a general discussion of our findings in regards to these questions, we examine the specific efforts of four of the companies that we visited in some detail.

2. Semiconductor Manufacturing

Semiconductor manufacturing is among the most complicated and capital intensive manufacturing processes in the world. In this section, we first give an overview of wafer fabrication, which is the most complicated portion of semiconductor manufacturing. We then describe the role of planning and scheduling in this environment.

Overview of Wafer Fabrication

The process for manufacturing integrated circuits consists of four basic phases; these are wafer fabrication, wafer probe, assembly (packaging), and final testing. Wafer fabrication is the phase where hundreds of circuits are layered through successive operations onto a smooth, typically silicon, wafer. In wafer probe the individual circuits are tested electrically using thin probes. The wafers are cut up into individual circuits, and the circuits which fail to meet specifications are discarded. The next phase, assembly, consists of placing the circuits in packages designed to protect them from the environment. A final test is then conducted before the integrated circuits are shipped. For a detailed overview of semiconductor manufacturing, we refer the reader to Sze (1988).

Wafer fabrication is the most costly phase of semiconductor manufacturing. It involves a complex sequence of processing steps with the number of operations typically in the hundreds. These operations must be performed in a very clean environment (called a clean room) and the operators must wear special clothing to avoid introducing excessive contaminants. Wafers move through the wafer fabrication facility in a lot (collection of wafers).

Some of the processing steps are single wafer processes, some steps are performed on an entire lot, and some can process several lots at the same (i.e. they are batch processes). A wafer may go through each of several steps many times as the layers of circuitry are built up on the wafer. The sequence of steps may vary considerably for different products. Production of a particular type of circuit requires a specific sequence of processing steps (deterministic with the exception of rework), with unique processing times at each step for that product type. Each processing step normally follows a very strict "recipe", so that processing times are essentially constant. However, wafer fabrication processing equipment is highly unreliable (machine availability of only 60-75% is common) and the yield losses are often very large, resulting in a highly stochastic production environment.

Planning and Scheduling in Wafer Fabrication

Semiconductor manufacturing is a highly competitive business. In the past, competition has been in the product design arena, but in the last several years the costs to manufacture integrated circuits has become an important competitive factor. As indicated above, wafer fabrication is very capital intensive, with the cost of the next generation of wafer fabrication facilities expected to reach nearly one billion U.S. dollars. In addition to these costs, the increasing pace of product innovation places a premium on the ability of an organization to effectively plan for the long-term (Shimoyashiro, 1992). The magnitude of the investment required makes it imperative to utilize the equipment in an effective manner. Short-term scheduling addresses this need. We describe the scopes of long-term planning and short-term scheduling below.

Long-term planning is concerned with a set of problems that are within the next few months to the next several years. Fordyce et al. (1992) indicate that the following issues are addressed by long-term planning functions: i) decisions about the impact of changes in the product line; ii) decisions about the types and numbers of equipment necessary to produce a given amount of product; iii) decisions about which manufacturing processes should be used to manufacture products; and, iv) decisions about the manpower required. The fact that product life cycles are relatively short and that they overlap with one another makes long-term planning a challenging endeavor. Long-term planning has traditionally been done using spreadsheets. In the last several years, robust performance analysis techniques such as queueing network theory and discrete-event simulation have become increasingly popular.

Short-term scheduling is concerned with the problems of the next hour to the next several months. The issues addressed by short-term scheduling include decisions on: (i) when to release jobs into the manufacturing line; (ii) how much of each product should be produced on a given day; (iii) how much overtime will be necessary; (iv) what priorities should be assigned to the different jobs competing for the same resource and for late jobs; (v) when to perform preventive maintenance; (vi) decisions to reduce time lost to set-ups; (vi) how to reroute product flows when machines are down; and (vii) which machines to use for a given operation given the yields for operations at different machines (Fordyce et al., 1992).

There is little academic literature that addresses the long or short-term planning and scheduling issues in wafer fabrication. This is no doubt due to the difficulty of the problems. The main emphasis of most work on scheduling has been on static systems with deterministic processing times. However, as noted above, in wafer fabrication, the system is dynamic and highly stochastic. Performance evaluation of wafer fabrication facilities using queueing theory is also very difficult. The manufacturing flow in wafer fabrication is represented by a re-entrant flow line (Graves et al. 1983). Essentially, the same wafer visits a particular machine (or machine group) as many as 15- 25 times, and the required processing of the wafer at that machine is different at each visit. Performance evaluation methods using queueing theory have traditionally focused on lines without reentrant flows; very little work has been done on performance evaluation of lines with reentrant flows.

Furthermore, there are also few results on good sequencing policies in wafer fabrication. At any point in time, a typical machine in a wafer fabrication facility has several different types of jobs waiting to be processed whose next operation is at a variety of different machines. Choosing the wrong job to process at a given machine could lead to starvation of a bottleneck downstream. Similarly, it is very important to control the release of new jobs to the network in order to avoid starvation of bottlenecks where possible. Releasing jobs too late can lead to starvation of bottlenecks, while releasing jobs too early can lead to high levels of Work- In-Process Inventory and uncompetitive cycle times.

A few significant papers have addressed this issue of release and sequencing control in wafer fabrication and have had some influence on the strategies used by U.S. semiconductor fabrication firms (Hogg and Fowler, 1991). These include the bottleneck starvation avoidance technique (Glassey and Resende, 1988) and the workload regulating release and sequencing policy(Wein, 1988). U.S. semiconductor manufacturing companies have also been influenced by the kanban release policy (an example is Fordyce et al. (1992) where the implementation of a kanban-like policy at an IBM facility is described), and by closed-loop release policies where the WIP in the facility is kept constant by releasing a job only when one has been completed (a case study describing the implementation of such a policy is Miller (1990)). The purpose of our study was to find out the tools and techniques that Japanese companies have been using for long-term planning and short-term scheduling and to characterize the differences between the approaches taken by U.S. and Japanese companies.

3. Research Method

The Operational Modeling department of SEMATECH (a research consortium composed of eleven semiconductor manufacturers) has been studying the challenges faced by U.S. semiconductor companies in planning and scheduling of wafer fabrication facilities since 1988. These topics have been a major focus of seven SEMATECH Modeling and Simulation Workshops during that time. Hence, our research on how companies address planning and scheduling issues dates back to 1988. In mid-1992, SEMATECH undertook an effort to determine what has been done in this arena throughout the world. We first visited several semiconductor manufacturers in Europe. In early 1993, we conducted extensive interviews with a large number of employees either currently or previously responsible for planning and scheduling at six large Japanese semiconductor manufacturing companies. We asked representatives from each company to describe the current state of the methods they use for planning and scheduling. Where possible, we were given demonstrations of the actual software in use at the fab. We focused on the following issues during our interview: i) What are the problems in planning and scheduling that the companies believe are important, and for which they are developing models; ii) How are new projects on planning and scheduling initiated at the company, (e.g., are they initiated by the demands of the fab manager, or by the suggestions of the research staff etc.), and how does the company decide to commit the resources to develop a planning and scheduling model (e.g., do projects have to be justified on a return-on-investment (ROI) basis?); iii) What are the actual tools that these companies use, e.g., simulation, queueing theory etc. Why did they decide to use these particular tools? iv) How is a model for planning and scheduling that the staff develops evaluated at the company? Who does the evaluation? (e.g., upper management or the actual users of the model in the fab etc.), and v) What are the future objectives of the planning and scheduling departments?

4. Planning and Scheduling Model Development and Tools

In this section, we report our findings on the questions posed in the previous section. We first describe which problems the companies we visited described as important problems that they were trying to solve. We then focus on how planning/scheduling projects are initiated and evaluated at these companies. Finally, we describe the models and tools used by the companies we visited.

Objectives

All of the companies we visited were developing models to address both long-term planning and short-term scheduling issues. Long-range production planning objectives included product-mix planning, equipment utilization planning, capital investment planning, and personnel planning. An important consideration was to develop models to find out the bottlenecks in the production process and how capital should be invested to improve the bottleneck processes. A very important consideration was the magnitude and variability of production lead times. All of the companies identified reduction of lead times as a significant objective. The most common short-term scheduling consideration was the development of a system that would tell operators what job to do next. Providing operators and supervisors correct and timely information was regarded as one of the most important objectives of any tool developed by the scheduling staff. One company told us that the problem with one of the earlier version of their scheduling software was that it was so slow that by the time it told each operator what to do for the next several hours, the system status had changed, and the jobs that the operators were supposed to work on had moved elsewhere. Avoiding setups where possible and making good batching decisions was a common objective of the scheduling software. Another very significant objective was to estimate whether lots would be completed on or before their delivery due date. We were told that managers were very interested in knowing which lots might be late and that development of models that would provide this information was of great importance. Another important objective was to decrease Work-In-Process Inventory levels. We were told at every company that decreasing Work-In-Process inventory levels was a very high priority of upper management. In fact, we were told by one company representative that at one time management measured WIP levels on certain fixed days and the operators made sure that WIP levels were acceptable on these days. Other significant objectives included understanding the impacts of hot lots on cycle-time variability. Hot lots are jobs that are assigned high priority by upper management and they tend to increase cycle times for other jobs as well as general cycle time variability. Finally, another key consideration was what actions to take after equipment failures.

Project Initiation, Development, and Evaluation

One of the significant issues that we focused on during our interviews was the question of how companies decide to undertake a certain planning/scheduling project and how the success or failure of a project is evaluated. Although we found that each company uses different procedures for evaluating the value and success of projects, we found some common characteristics as well. We list some of the common themes we found with respect to project initiation, development, and evaluation below:

1. **Project initiation:** We found that top-down initiation of projects is not uncommon, although companies also have mechanisms whereby the planning/scheduling group can propose a certain project and upper management decides whether to undertake it. For example, at nearly all the companies we visited, upper management was concerned about lead times and WIP levels and initiated projects to cut them. However, there were also projects that were initiated because a member of the staff had proposed it. For example, at one of the companies that we visited, a major annual event for the corporate research department is an exhibition for the operating divisions. At this R&D "open house", the researchers demonstrate and present their work and pitch their proposals. A project is then initiated if the operating divisions think it will be beneficial.

2. **Clear definition of customers and objectives:** We found that members of the planning and scheduling groups in Japan always started out a project with a clear definition of the objectives and the customers. At nearly all of the companies that we visited, the R&D staff had close interaction with the plant managers and operators at the plant. The planning and scheduling R&D staff were aware that the end users of the methods and software that they develop will be the operators at the semiconductor fabrication facilities and emphasized the importance of plant management and workers "buying-in" to the project.

There was a clear emphasis on making the products that the planning and scheduling staff developed easy-to-understand and user-friendly. Furthermore, visualizations, charts and statistics were used heavily in an effort to make the results easier to understand. However, the Japanese companies we visited universally avoided animation in their wafer fabrication models.

We found that it is very common for the tools developed by the planning and scheduling staff to be implemented at the R&D fabs first. If this implementation is successful, then the second stage of the implementation involves development of tools for the production fabs. However, there is a very significant effort to keep plant managers, and operators, involved in the development of scheduling tools from the early stages of the project. Although some U.S. companies emphasize close interaction between plant staff and R&D staff, there are still some U.S. semiconductor manufacturers that have large R&D departments that have appear to have little interaction with the actual production facilities.

3. **Stable teams:** We observed that the planning/scheduling groups in Japanese semiconductor manufacturing firms were very stable. In all but one of the companies that we visited, we were able to talk to the staff members who were involved in the original scheduling tools developed over the last 5-10 years. The stability of the staff, as well as the long-term outlook of the management were common to all the companies we visited. The planning staff regarded their projects as part of a long-term continuous improvement project. Each planning group was thus able to look to the future and articulate what they would like to accomplish in the next 3-4 years, and what milestone the current project represented. This is also in contrast to U.S. semiconductor manufacturing firms where assignments tend to be much more short-term and planning/scheduling staff tend to change more rapidly.

4. **Reliance on "locally developed" programs:** We found that Japanese

companies tend to develop and use their own tools and software, instead of using commercially available software. This is different from the situation in the U.S. where most semiconductor manufacturing companies tend to use commercially available software. The staff at the Japanese companies that we interviewed were aware of the commercially available software specifically written for the semiconductor manufacturing environment. However, all but one of the companies we visited had decided against using commercial software. The three most common reasons given for this choice were:

(a) *Dissatisfaction with available software:* Nearly all of the Japanese companies we visited had tried out (or at least evaluated) some of the commercially available software and found them unsatisfactory. A common complaint was that the commercially available software for keeping track of WIP on the shop floor was too slow. Interestingly, a major U.S. semiconductor manufacturing company that we visited recently converted one of its fabs to what they called a "paperless" fab. In this fab, operators have to look at the computer to decide what to do next, and at the finish of each operation, the data has to be entered into the computer. The WIP tracking program used at this fab is a commercially available package for tracking WIP. We were told by the plant manager of this fab that the bottleneck in the fab is the computer. In fact, for some processes, the time spent for retrieving and entering data from the computer takes more time than the actual processing time. The plant manager told us that the company is studying a major investment to buy faster computers.

(b) *Flexibility:* A major reason given by the companies for development of their own software was that this was more flexible. Although development of software in-house required a larger investment of time and resources in the beginning, the companies felt that it was easier to improve software developed in-house. Clearly, the existence of long term corporate commitment and stable team membership are factors that facilitate in-house development and improvement of software.

(c) *Engineering Pride:* Interestingly, this was also a major reason given for the choice of in-house development of software by most of the companies. Planning/scheduling staff emphasized the strong sense of pride in the work that they did and emphasized that they much preferred using software they developed themselves.

5. **Project evaluation:** The planning and scheduling groups at all the companies that we visited stressed the fact that they did not have to justify a project by performing some sort of return-on-investment computation. This is in contrast to the U.S. where such calculations are rather important in deciding whether a project will be undertaken or not. In fact, the planning/scheduling groups in Japan also stressed the difficulty of making such calculations. For example, the development of a shop-floor control mechanism can be useful because it leads to better WIP tracking and data collection. It is very hard to quantify the benefits of better data collection. Also, the knowledge gained while working on one project can be useful on other projects. For all these reasons, the Japanese companies did not seem to rely on ROI computations when deciding whether to initiate a project.

   Evaluation of the success of the projects is also not based on a simple numerical comparison of the money spent on the project versus the benefits accrued. Rather, at each of the companies, we were told the success of a project was related to the long-term objectives of the company and how the project fit in with those objectives. Interestingly, we were told at several companies that R& D staff were encouraged to publish their findings in practitioner publications, and in fact, significant publications, and the interest that they generated were often regarded as important factors in the success of a project. The planning and scheduling R & D staff at one company explained that the company believed that "potential" customers who see these publications are impressed and hence these publications served as some sort of advertisement. A staff member of the planning and scheduling group at another company said that corporate R&D staff are evaluated according to the 3-P system: patents, publications and performance.

Models and Tools

In this section, we provide brief case histories for the planning and scheduling projects at four Japanese firms.

Toshiba

The present project to develop planning and scheduling tools for semiconductor manufacturing dates back to 1989. Initially, queueing networks were used to model fabs. The emphasis was on bottleneck identification and Work-In-Process inventories. After the start of this effort, upper management became interested in decreasing WIP levels in the fabs. Queueing network models were used to show that fabs could achieve target throughput levels with much less WIP than they had at the time. These queueing network models were based on approximate mean value analysis (Reiser and Lavenberg, 1980). Later, QNA-type (Whitt, 1983) open queueing network models were used for capacity planning, in which optimal capacity parameters such as number of machines were computed automatically by simulated annealing. A result of this phase of the project was a recommendation that the release policy practiced in the fabs (which was similar to the closed-loop release policy in which new work is introduced only when jobs have been completed) be more strictly applied. This recommendation was implemented, decreasing the amount of inventory in the fabs without loss of throughput. Furthermore, the models were used to predict steady-state, long-term, aggregate performance measures. However, these models could not predict how individual lots behave.

Management's interest in a tool to predict the behavior of individual lots (e.g., if a particular lot will be completed before its due date) led to the second-phase of the project. A new simulation program was developed, in C. The program is designed to run every day. The program downloads the current status of the fab from a database, then provides estimates of when each order will be finished, given its current priority. If an important order is predicted to be late, then its priority can be changed, and the simulation run again. Since each simulation run takes only about 5 minutes, this process can be repeated many times.

The simulation software described above has been used by Toshiba to estimate when each order will be completed. The simulation program is currently run once a day. One useful effect of the development of the simulation program has been that it has led to better data collection and tracking. Each time the program is run, the fab is simulated for the duration of one month. The system was first implemented for wafer fabs and was later extended to include testing and assembly. Since the assembly lines are not necessarily within Toshiba, the scope of the model encompasses multiple companies. All the variables in the model are deterministic. Machine failures are taken into account by inflating processing times. That is, processing time is assumed longer than if the machines would not fail. Yield is also taken into account deterministically by predetermined percentages. The developers of the model and the simulation program explain that random phenomena were avoided: (1) for easy interpretation of results; (2) so that a single (and hence short) run will suffice; and (3) to alleviate the task of data gathering.

The main drawback of the deterministic nature of the current simulation program is that it can not be used to assign due dates to incoming orders at a desired confidence level. That is, the information on the current status of the shop floor can not be used to quote customers due dates which can be met a desired percentage of the time. We were told that management had recently become interested in a tool that would aid in quoting customers due dates. There are plans to develop such a model.

The planning/scheduling staff at Toshiba make a significant effort to make their models and software easy-to-understand and use by the production staff at the fabs.

However, we were told that the production staff and the operators at the fabs do have their local agendas and are sometimes more interested in "locally optimal" solutions. New models, methods, or software are accepted only if they have effects visible to them. However, simple, straight-forward models are preferred at all levels of the organization and this is one reason why the models in use are deterministic. In fact, probably the most powerful aspect of the model and software in use at Toshiba is the simplicity and the speed with which it provides solutions. Further details on this project can be found in Fujihara and Yoneda (1992) and Kamimura et al. (1992).

Mitsubishi

Mitsubishi's project leading to the development of a Petri-net based simulator, View, started around 1988. There were two objectives that led them to develop this fab simulator: 1) work load prediction in the fab as a function of the release schedule, tools being down, and work in process, and 2) design and capacity analysis of future factories in terms of the desired number of tools and throughput levels. Therefore, the project's customers were both fab operating personnel and fab designers. View takes inputs from the current factory configuration and input schedules and recipes (with setups). Input parameters that can be varied for analysis are:

1. input quantity by product
2. dispatching rules at each work station (including due dates)
3. current WIP values
4. maximum total WIP levels
5. a deterministic schedule of tool calibrations, failures and repairs.

View output, presented numerically and with graphics, includes

1. tool utilizations

2. dynamic WIP charts for multiple work centers
3. dynamic charts of throughput by work station
4. cycle times by product.

This output is then used for decisions in work load control, process control, and major factory design changes. The View system is centered around a computer-aided scheduling environment for a manufacturing system which utilizes human-computer cooperation to determine operation scheduling. The scheduling editor consists of four components: modeling, simulation, evaluation and editing. A novel approach is taken in the editing component, which incorporates an interactive system that allows an engineer to make and freely modify a desired schedule on a computer display while at the same time satisfying the constraints of the particular systems.

In View, a job shop type production system is modeled. Particular properties include the variety of machines, the variety of products produced, and complex process routings. Manufacturing system performance can be evaluated in many ways depending on the products produced or the manufacturing systems used. The objectives include high machine utilization, and a smooth distribution of work over the entire system. In addition, strong constraints (which must not be violated) and weak constraints (desired but not necessary) are included in the scheduling process. It is noted that their approach is not aimed at determining an optimal solution; it is focused on the human-computer cooperation, where the decision for schedule acceptance is made by the human.

The scheduling task of manufacturing systems can be broken down into three sub tasks: monitoring the current status of facilities and jobs, clarifying the requirements of the facilities and the jobs, and deciding the processing order of jobs. Clearly the last two are the most difficult. To avoid the combinatorial explosion associated with a mathematically optimal solution, Mitsubishi proposes this human-computer cooperative approach utilizing computer simulation and an interactive interface. The human's role is to intuitively evaluate and edit the schedule on a computer display. The computer's role is to handle the complex constraint propagation arising from editing the schedule. The graphics interface was developed on an engineering workstation, which executes the simulation and on which the user can modify the schedule as desired.

With regard to simulation modeling, a timed Petri Net is used to facilitate recognition and analysis of the behavior of complex manufacturing systems. Petri net modeling is used because it facilitates the representation of a complex production line and the simulation of the behavior of system dynamics with very simple, but inflexible, components. This is the only use of Petri Net factory modeling we found in this industry. While Petri Nets are easy to learn and use, they are generally regarded as computationally inefficient and inflexible for large scale simulation modeling. The main strength of Petri Net modeling is that the rule for simulation time advance is very simple (check all conditions to see which activities can be started or ended).

The decision to base the simulation on Petri Nets was made many years ago after an international conference on Petri Nets held in Tokyo. The use of Petri Nets results in a system that allows fab models to be constructed very easily by choosing product/tool icons from a menu and dragging and linking them into a model. The interface does not use physical animation but rather relies on dynamic graphical representation of the relevant performance evaluation information and statistics.

The View system has been used by Mitsubishi in the design of fabs and it is currently in use in their fabs to get production work load predictions. Further details on View are available in Fukuda et al. (1989).

NEC

The development of planning and scheduling tools at NEC dates back to the early 1980's. In this section we focus on the simulation-based PLAN-LSIP set of production planning and evaluation tools. Initially, the corporate research staff carried out some evaluation of U.S. simulation languages; however, they elected to develop their own tools. The development followed the typical historical path from FORTRAN-based text systems to C-based graphics systems using X-Windows and UNIX. In this project, graphical dynamic presentation of information to assist the production staff is strongly emphasized. Dynamic and colorful Gantt and WIP charts are widely used. NEC appears to place a strong focus on the end-user of the system and the importance of the human-system interface.

PLAN-LSIP was developed to assist decision makers in production planning and scheduling in the complex environment surrounding semiconductor manufacturing. This decision support system is intended to support both long-term planning and short-term scheduling in the wafer fabrication area. Essentially, PLAN-LSIP is largely a deterministic simulation. The current status of the shop floor is downloaded (via Ethernet) from the shop floor control system. PLAN- LSIP then performs a simulation of the system to predict the performance for the time period of interest. This information can be displayed to the user using pre-programmed graphical presentation tools or the user can customize their own graphs and tables. This information is used to assist in the planning and scheduling functions. For example, the user can assess the effect of adding a machine for a certain operation by running two simulations and comparing performance measures of interest with and without the additional machine. The simulation provides answers very rapidly (in part, due to the use of deterministic models). Hence, many different alternatives can be evaluated in a relatively short period of time.

Significant quantitative and qualitative results were achieved using the PLAN-LSIP system with a large scale semiconductor manufacturing plant: turnaround time was reduced by 30%, long-range decision making has been improved, and on-time delivery performance was improved.Further details of the PLAN-LSIP system can be found in Homma et al. (1991).

Nippon Telegraph and Telephone Corporation (NTT)

The Manufacturing Systems Technology Laboratory of NTT LSI Laboratories have developed a SEmiconductor MAnufacturing Line Simulator (SEMALIS) with the goals of facility design and operational planning. SEMALIS is written in the general purpose simulation language SLAM-II with considerable use of FORTRAN subroutines. NTT has used SEMALIS to study: 1) the influence (in terms of throughput and cycle time) of additional bottleneck equipment; 2) the effect of equipment failures and maintenance on line performance; 3) the influence of time-constrained processing between process steps (time-constrained processes are those processes that have to be repeated unless the next process is performed within a given time limit, such processes are of considerable importance in wafer fabrication); and 4) the change in line performance when "hot" lots are introduced into steady state manufacturing lines. This tool has been used for long-term planning purposes and NTT is developing separate tools for scheduling. A 220 day (1 year) run of SEMALIS on a Sun Sparc Station takes approximately 1 hour of CPU time; the fact that SEMALIS can provide answers relatively quickly results in an opportunity to evaluate many different alternatives. SEMALIS output provides data on turn-around time, throughput, equipment utilization, lot queuing times at each workstation. We were told that fabs use some sort of closed-loop release policy where a maximum WIP limit is set for the fab.

Two interesting facts differentiate NTT's project from the other companies' projects we described above. The first is that SEMALIS was written in a general purpose simulation language. However, we note that although a general purpose simulation language was used, the software was developed in-house. The second difference is that the reliability of equipment in SEMALIS is handled in a stochastic instead of deterministic manner. As we have noted above, all the other companies used deterministic models for simplicity and to obtain results rapidly.

The current focus at NTT is on developing the capability to do on-line modelling. A detailed description of SEMALIS and some of the results obtained using it can be found in Nakamura et al. (1992).

5. Conclusions

Arguably, the major difference between Japanese modeling practice and many U.S. semiconductor manufacturing companies is *not* that the Japanese choose to develop their own modeling software, but the fact that they *can* develop their own tools. In all of the Japanese companies we visited, we observed the lack of management or professional interest in "quick" models and "dirty" analysis, an emphasis on stable team membership, strong connections with academic and professional community, and very strong computing and analytical skills. All these factors make it possible for these companies to accomplish the development of in-house software to meet specific needs of the project and thus improve their competitive position.

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